

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |
|-----------------|-----------|-------|-----|----|----|----|----|----|----|
| counter_reg | Flip-flop | 5 | Y | N | Y | N | N | N | N |
| shift_reg | Flip-flop | 64 | Y | N | Y | N | N | N | N |
| state_reg | Flip-flop | 2 | Y | N | Y | N | N | N | N |
| operand_a_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |
| operand_b_reg | Flip-flop | 32 | Y | N | Y | N | N | N | N |
| inst_reg | Flip-flop | 3 | Y | N | Y | N | N | N | N |
| output_done_reg | Flip-flop | 1 | N | N | Y | N | N | N | N |

| Register Name | Type | Width | Bus | MB | AR | AS | SR | SS | ST |
|-----------------|-----------|-------|-----|----|----|----|----|----|----|
| counter_nxt_reg | Flip-flop | 5 | Y | N | N | N | N | N | N |