

## File Structure

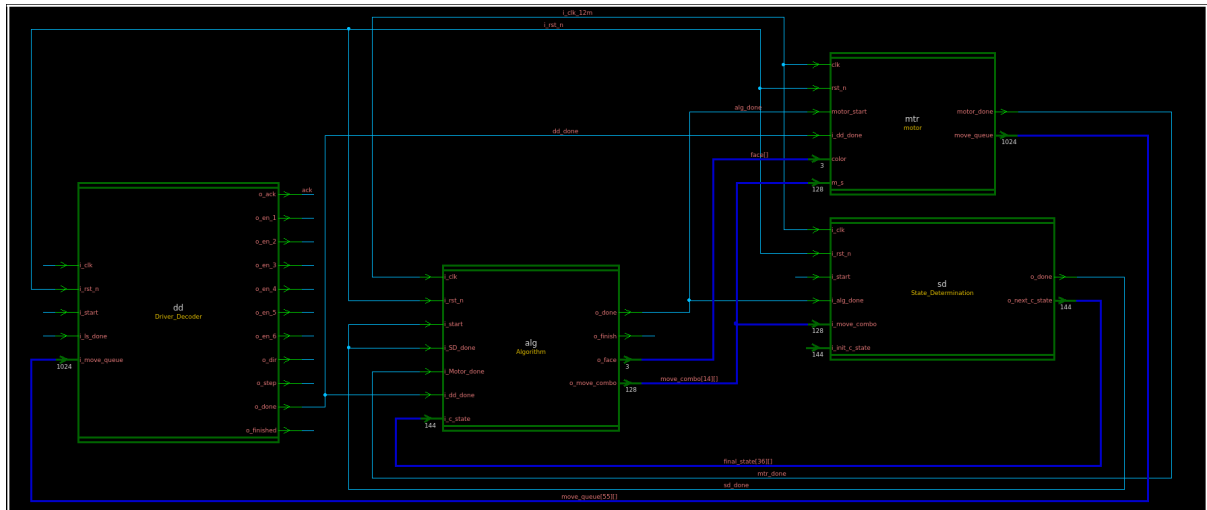
```
team01_final
| team01_final_report.pdf
|
\---src
|   Algorithm.sv
|   I2C_Read.sv
|   I2C_sensor.sv
|   I2C_Setup.sv
|   motor.sv
|   ps2.sv
|   real_Driver_Decoder.sv
|   State_Determination.sv
|   Top.sv
|
+---Altpll
|   | Altpll.bsf
|   | Altpll.cmp
|   | Altpll.html
|   | Altpll.xml
|   | Altpll_bb.v
|   | Altpll_generation.rpt
|   | Altpll_inst.v
|   | Altpll_inst.vhd
|   |
|   \---synthesis
|       | Altpll.debuginfo
|       | Altpll.qip
|       | Altpll.v
|       |
|       \---submodules
|           altera_reset_controller.sdc
|           altera_reset_controller.v
|           altera_reset_synchronizer.v
|           Altpll_altpll_0.v
|
+---DE2_115
|   DE2_115.qsf
|   DE2_115.sdc
|   DE2_115.sv
|   Debounce.sv
|   SevenHexDecoder.sv
|
+---python_file
|   check_if_sv_right.py
|   combo_dec.py
|   Find_corner_edge.py
```

```

| gen_binary_input.py
| pycode.py
| pycode_gen_all.py
| simc_combo_answer.py
| state_trans.py
| state_trans_sv.py
| transition.py
|
|---txt_file
    Back_clockwise.txt
    Back_counterclockwise.txt
    change_view.txt
    Down_clockwise.txt
    Down_counterclockwise.txt
    find_corner.txt
    find_edge.txt
    Front_clockwise.txt
    Front_counterclockwise.txt
    Front_to_top.txt
    Left_clockwise.txt
    Left_counterclockwise.txt
    Right_clockwise.txt
    Right_counterclockwise.txt
    Top_clockwise.txt
    Top_counterclockwise.txt
    transition.sv

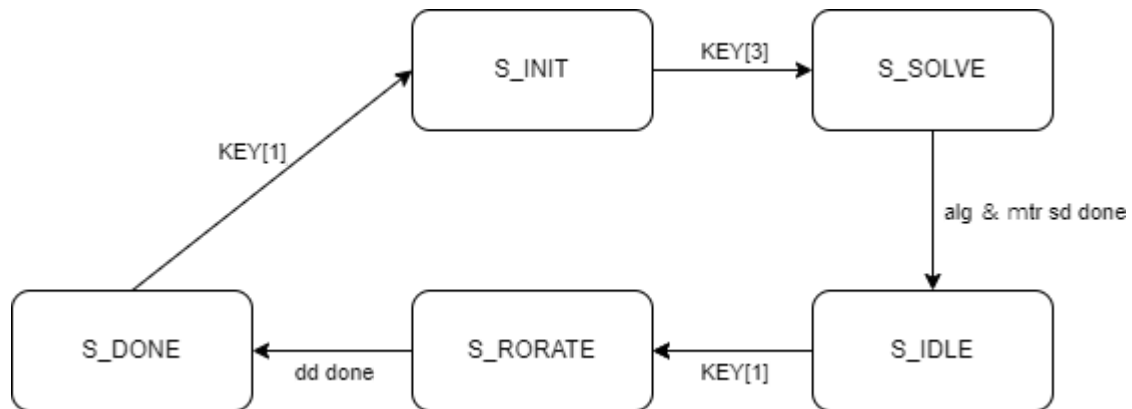
```

## System Architecture

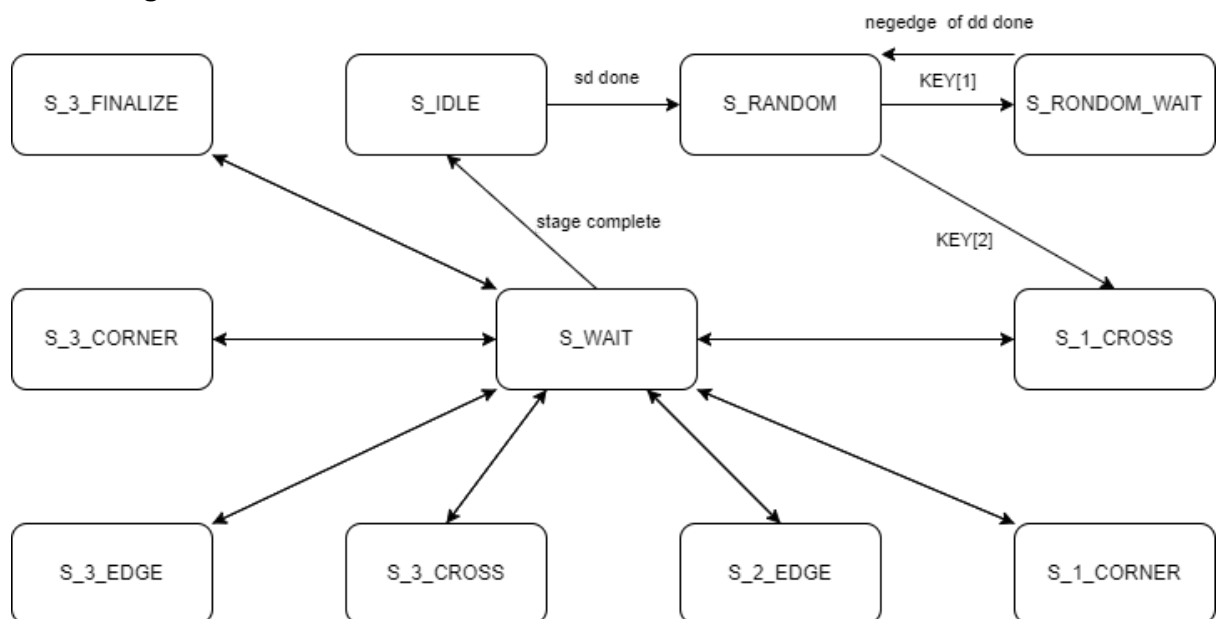


# Hardware Scheduling

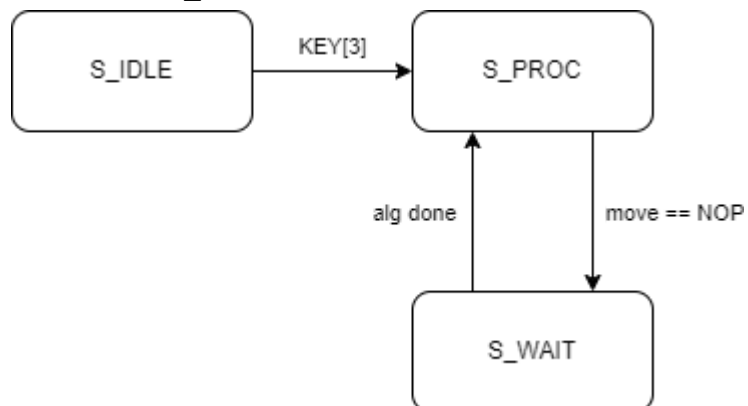
## FSM of Top.sv



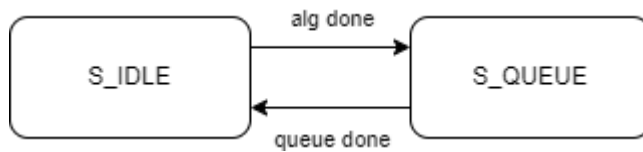
## FSM of Algorithm.sv



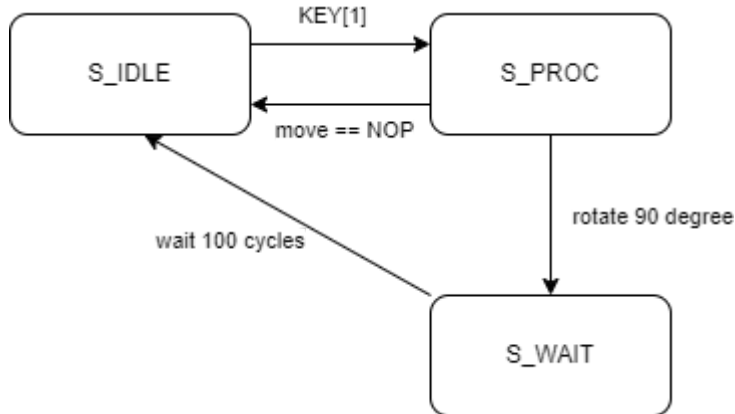
## FSM of State\_Determination.sv



## FSM of motor.sv



## FSM of En\_Ctrl in real\_Driver\_Decoder.sv



## Algorithm Workflow

<https://ruwix.com/the-rubiks-cube/how-to-solve-the-rubiks-cube-beginners-method/>

<https://www.speedcube.com.au/pages/how-to-solve-a-rubiks-cube>

## Fitter Summary

| Fitter Summary                     |   |
|------------------------------------|---|
| Fitter Status                      | Successful - Sun Jun 09 14:38:48 2024       |
| Quartus II 64-Bit Version          | 15.0.0 Build 145 04/22/2015 SJ Full Version |
| Revision Name                      | DE2_115                                     |
| Top-level Entity Name              | DE2_115                                     |
| Family                             | Cyclone IV E                                |
| Device                             | EP4CE115F29C7                               |
| Timing Models                      | Final                                       |
| Total logic elements               | 7,984 / 114,480 ( 7 % )                     |
| Total combinational functions      | 7,921 / 114,480 ( 7 % )                     |
| Dedicated logic registers          | 1,457 / 114,480 ( 1 % )                     |
| Total registers                    | 1457  |
| Total pins                         | 518 / 529 ( 98 % )                          |
| Total virtual pins                 | 0   |
| Total memory bits                  | 0 / 3,981,312 ( 0 % )                       |
| Embedded Multiplier 9-bit elements | 0 / 532 ( 0 % )                             |
| Total PLLs                         | 1 / 4 ( 25 % )                              |

# Timing Analyzer

Top\_plan8.v

Compilation Report - DE2\_115

Algorithm.v

DE2\_115.v

real\_Driver\_Decoder.v

motor.v

DE2\_115.sdc

I2C\_Read.v

Debounce.v

Table of Contents

Device Options

Operating Settings and Conditions

Messages

Suppressed Messages

Flow Messages

Flow Suppressed Messages

Assembler

TimeQuest Timing Analyzer

Summary

Parallel Compilation

SDC File List

Clocks

Slow 1200mV 85C Model

Fmax Summary

Timing Closure Recommendations

Setup Summary

Hold Summary

Recovery Summary

Removal Summary

Minimum Pulse Width Summary

Worst-Case Timing Paths

Datasheet Report

Metastability Summary

Slow 1200mV OC Model

Fast 1200mV OC Model

Multicorner Timing Analysis Summary

Multicorner Datasheet Report Summary

Advanced I/O Timing

Clock Transfers

Report TCCS

Report RSKM

Unconstrained Paths

Messages

Timing Closure Recommendations

Summary [hide details]

This design contains failing setup paths with a worst-case slack of -2.340 ns. Run [Report Timing Closure Recommendations](#) for recommendations on how to close setup timing. For recommendations for any particular path, click the appropriate link in the table below.

Top Failing Paths [hide details]

| Slack     | From                                | To                                   | Recommendations                                      |
|-----------|-------------------------------------|--------------------------------------|--|
| 1: -2.340 | ps2_keyboard_driv...psps2_byte_r[5] | Top:Top Algorithm...ve_combo_r[0][0] | <a href="#">Report recommendations for this path</a> |
| 2: -2.268 | ps2_keyboard_driv...psps2_byte_r[0] | Top:Top Algorithm...ve_combo_r[0][3] | <a href="#">Report recommendations for this path</a> |
| 3: -2.234 | ps2_keyboard_driv...psps2_byte_r[1] | Top:Top Algorithm...ve_combo_r[0][2] | <a href="#">Report recommendations for this path</a> |
| 4: -2.233 | ps2_keyboard_driv...psps2_byte_r[4] | Top:Top Algorithm...ve_combo_r[0][3] | <a href="#">Report recommendations for this path</a> |
| 5: -2.224 | ps2_keyboard_driv...psps2_byte_r[4] | Top:Top Algorithm...ve_combo_r[0][2] | <a href="#">Report recommendations for this path</a> |

Top\_plan8.v

Compilation Report - DE2\_115

Algorithm.v

DE2\_115.v

real\_Driver\_Decoder.v

motor.v

DE2\_115.sdc

I2C\_Read.v

Debounce.v

Table of Contents

Device Options

Operating Settings and Conditions

Messages

Suppressed Messages

Flow Messages

Flow Suppressed Messages

Assembler

TimeQuest Timing Analyzer

Summary

Parallel Compilation

SDC File List

Clocks

Slow 1200mV 85C Model

Fmax Summary

Timing Closure Recommendations

Setup Summary

Hold Summary

Recovery Summary

Removal Summary

Minimum Pulse Width Summary

Worst-Case Timing Paths

Datasheet Report

Metastability Summary

Slow 1200mV OC Model

Fast 1200mV OC Model

Multicorner Timing Analysis Summary

Multicorner Datasheet Report Summary

Advanced I/O Timing

Clock Transfers

Report TCCS

Report RSKM

Unconstrained Paths

Messages

Slow 1200mV 85C Model Setup Summary

|   | Clock                       | Slack  | End Point TNS |
|---|-----------------------------|--------|---------------|
| 1 | p10 altpll_0 sd1 p17 clk[0] | -2.340 | -8.965        |
| 2 | CLOCK_50                    | 16.020 | 0.000         |
| 3 | p10 altpll_0 sd1 p17 clk[2] | 72.288 | 0.000         |

The screenshot shows the Xilinx Vivado IDE interface. The top toolbar contains icons for various tools like 'Top plan8.v', 'Compilation Report - DE2\_115', 'AlgorithmMn.v', 'DE2\_115.v', 'real\_driver\_decoder.v', 'motor.sv', 'DE2\_115.sdc', 'I2C\_Read.sv', and 'Debounce.sv'. The left pane displays the project hierarchy under 'Table of Contents'. The 'Slow 1200mV 85C Model' folder is expanded, showing sub-items like 'Fmax Summary', 'Timing Closure Recommendations', 'Setup Summary', 'Hold Summary', 'Recovery Summary', 'Removal Summary', 'Minimum Pulse Width Summary', 'Worst-Case Timing Paths', 'Datasheet Report', and 'Metastability Summary'. The 'Worst-Case Timing Paths' folder is also expanded, showing various setup, hold, and pulse width constraints. The right pane displays the 'Slow 1200mV 85C Model Setup Summary' table.

|   | Clock                        | Slack  | End Point TNS |
|---|------------------------------|--------|---------------|
| 1 | p10[altpll_0]sd1[p1l7]clk[0] | -1.750 | -6.538        |
| 2 | CLOCK_50                     | 16.382 | 0.000         |
| 3 | p10[altpll_0]sd1[p1l7]clk[2] | 73.249 | 0.000         |

|  |        |                                    |  |                            |                            |              |            |
|--|--------|------------------------------------|--|----------------------------|----------------------------|--------------|------------|
| Top_plan8.v  |        |                                    |  |                            |                            |              |            |
| Compilation Report - DE2_115   |        |                                    |  |                            |                            |              |            |
| Algorithm.v  |        |                                    |  |                            |                            |              |            |
| DE2_115.v  |        |                                    |  |                            |                            |              |            |
| real_Driver_Decoder.v  |        |                                    |  |                            |                            |              |            |
| motor.v  |        |                                    |  |                            |                            |              |            |
| DE2_115.sdc  |        |                                    |  |                            |                            |              |            |
| I2C_Read.v   |        |                                    |  |                            |                            |              |            |
| Debounce.v   |        |                                    |  |                            |                            |              |            |
| Table of Contents  |        |                                    |  |                            |                            |              |            |
| Slow 1200mV OC Model Setup: 'p10[altpl_0]sd1[p17]clk[0]'   |        |                                    |  |                            |                            |              |            |
| <div> <div>Worst-Case Timing Paths</div> <div> <div>Setup: 'p10[altpl_0]sd1[p17]clk[0]'</div> <div>Setup: 'CLOCK_50'</div> <div>Setup: 'p10[altpl_0]sd1[p17]clk[0]'</div> <div>Hold: 'p10[altpl_0]sd1[p17]clk[0]'</div> <div>Hold: 'p10[altpl_0]sd1[p17]clk[2]'</div> <div>Hold: 'CLOCK_50'</div> <div>Minimum Pulse Width: 'CLOCK_5'</div> <div>Minimum Pulse Width: 'CLOCK_2'</div> <div>Minimum Pulse Width: 'CLOCK_3'</div> <div>Minimum Pulse Width: 'p10[altpl_0]sd1[p17]clk[0]'</div> </div> </div> <div> <div>Datasheet Report</div> <div>Metastability Summary</div> <div>Slow 1200mV OC Model</div> <div> <div>Fmax Summary</div> <div>Setup Summary</div> <div>Hold Summary</div> <div>Recovery Summary</div> <div>Removal Summary</div> <div>Minimum Pulse Width Summary</div> </div> <div>Worst-Case Timing Paths</div> <div> <div>Setup: 'p10[altpl_0]sd1[p17]clk[0]'</div> <div>Setup: 'CLOCK_50'</div> <div>Setup: 'p10[altpl_0]sd1[p17]clk[0]'</div> <div>Hold: 'p10[altpl_0]sd1[p17]clk[0]'</div> <div>Hold: 'p10[altpl_0]sd1[p17]clk[2]'</div> <div>Hold: 'CLOCK_50'</div> <div>Minimum Pulse Width: 'CLOCK_5'</div> <div>Minimum Pulse Width: 'CLOCK_2'</div> <div>Minimum Pulse Width: 'CLOCK_3'</div> <div>Minimum Pulse Width: 'p10[altpl_0]sd1[p17]clk[0]'</div> </div> </div> |        |                                    |  |                            |                            |              |            |
|  | Slack  | From Node                          | To Node                                  | Launch Clock               | Latch Clock                | Relationship | Clock Skew |
| 1  | -1.750 | ps2_keyboard_driver:ps2_byte_r[5]  | Top:Top[Algorithm:alg]move_combo_r[0][0] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.482     |
| 2  | -1.636 | ps2_keyboard_driver:ps2_byte_r[1]  | Top:Top[Algorithm:alg]move_combo_r[0][2] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.467     |
| 3  | -1.629 | ps2_keyboard_driver:ps2_byte_r[3]  | Top:Top[Algorithm:alg]move_combo_r[0][0] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.482     |
| 4  | -1.612 | ps2_keyboard_driver:ps2_byte_r[0]  | Top:Top[Algorithm:alg]move_combo_r[0][3] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.482     |
| 5  | -1.602 | ps2_keyboard_driver:ps2_byte_r[4]  | Top:Top[Algorithm:alg]move_combo_r[0][2] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.467     |
| 6  | -1.578 | ps2_keyboard_driver:ps2_byte_r[4]  | Top:Top[Algorithm:alg]move_combo_r[0][3] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.482     |
| 7  | -1.540 | ps2_keyboard_driver:ps2_byte_r[5]  | Top:Top[Algorithm:alg]move_combo_r[0][1] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.466     |
| 8  | -1.530 | ps2_keyboard_driver:ps2_byte_r[3]  | Top:Top[Algorithm:alg]move_combo_r[0][2] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.467     |
| 9  | -1.517 | ps2_keyboard_driver:ps2_byte_r[0]  | Top:Top[Algorithm:alg]move_combo_r[0][2] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.467     |
| 10   | -1.486 | ps2_keyboard_driver:ps2_byte_r[0]  | Top:Top[Algorithm:alg]move_combo_r[0][0] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.482     |
| 11   | -1.458 | ps2_keyboard_driver:ps2_byte_r[4]  | Top:Top[Algorithm:alg]move_combo_r[0][0] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.482     |
| 12   | -1.402 | ps2_keyboard_driver:ps2_byte_r[4]  | Top:Top[Algorithm:alg]move_combo_r[0][1] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.466     |
| 13   | -1.361 | ps2_keyboard_driver:ps2_byte_r[6]  | Top:Top[Algorithm:alg]move_combo_r[0][3] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.482     |
| 14   | -1.353 | ps2_keyboard_driver:ps2_byte_r[1]  | Top:Top[Algorithm:alg]move_combo_r[0][3] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.482     |
| 15   | -1.319 | ps2_keyboard_driver:ps2_byte_r[5]  | Top:Top[Algorithm:alg]move_combo_r[0][2] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.467     |
| 16   | -1.280 | ps2_keyboard_driver:ps2_byte_r[7]  | Top:Top[Algorithm:alg]move_combo_r[0][2] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.467     |
| 17   | -1.279 | ps2_keyboard_driver:ps2_byte_r[1]  | Top:Top[Algorithm:alg]move_combo_r[0][0] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.482     |
| 18   | -1.248 | ps2_keyboard_driver:ps2_byte_r[3]  | Top:Top[Algorithm:alg]move_combo_r[0][3] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.482     |
| 19   | -1.161 | ps2_keyboard_driver:ps2_byte_r[6]  | Top:Top[Algorithm:alg]move_combo_r[0][2] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.467     |
| 20   | -1.150 | ps2_keyboard_driver:ps2_byte_r[1]  | Top:Top[Algorithm:alg]move_combo_r[0][1] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.466     |
| 21   | -1.127 | ps2_keyboard_driver:ps2_byte_r[2]  | Top:Top[Algorithm:alg]move_combo_r[0][2] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.467     |
| 22   | -1.122 | ps2_keyboard_driver:ps2_byte_r[3]  | Top:Top[Algorithm:alg]move_combo_r[0][1] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.466     |
| 23   | -1.056 | ps2_keyboard_driver:ps2_byte_r[6]  | Top:Top[Algorithm:alg]move_combo_r[0][0] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.482     |
| 24   | -1.044 | ps2_keyboard_driver:ps2_byte_r[0]  | Top:Top[Algorithm:alg]move_combo_r[0][1] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.466     |
| 25   | -1.037 | ps2_keyboard_driver:ps2_byte_r[7]  | Top:Top[Algorithm:alg]move_combo_r[0][0] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.482     |
| 26   | -0.961 | ps2_keyboard_driver:ps2_byte_r[2]  | Top:Top[Algorithm:alg]move_combo_r[0][3] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.482     |
| 27   | -0.961 | ps2_keyboard_driver:ps2_byte_r[6]  | Top:Top[Algorithm:alg]move_combo_r[0][1] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.466     |
| 28   | -0.888 | ps2_keyboard_driver:ps2_byte_r[5]  | Top:Top[Algorithm:alg]move_combo_r[0][3] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.482     |
| 29   | -0.662 | ps2_keyboard_driver:ps2_byte_r[7]  | Top:Top[Algorithm:alg]move_combo_r[0][1] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.466     |
| 30   | -0.620 | ps2_keyboard_driver:ps2_byte_r[2]  | Top:Top[Algorithm:alg]move_combo_r[0][1] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.466     |
| 31   | -0.558 | ps2_keyboard_driver:ps2_byte_r[2]  | Top:Top[Algorithm:alg]move_combo_r[0][0] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.482     |
| 32   | -0.550 | ps2_keyboard_driver:ps2_byte_r[7]  | Top:Top[Algorithm:alg]move_combo_r[0][3] | CLOCK_50                   | p10[altpl_0]sd1[p17]clk[0] | 3.333        | -2.482     |
| 33   | 65.481 | Top:Top[Algorithm:alg]color_2_r[2] | Top:Top[Algorithm:alg]move_combo_r[1][2] | p10[altpl_0]sd1[p17]clk[0] | p10[altpl_0]sd1[p17]clk[0] | 83.333       | -0.067     |
| 34   | 65.589 | Top:Top[Algorithm:alg]color_2_r[2] | Top:Top[Algorithm:alg]move_combo_r[7][1] | p10[altpl_0]sd1[p17]clk[0] | p10[altpl_0]sd1[p17]clk[0] | 83.333       | -0.084     |
| 35   | 65.592 | Top:Top[Algorithm:alg]color_2_r[2] | Top:Top[Algorithm:alg]move_combo_r[1][0] | p10[altpl_0]sd1[p17]clk[0] | p10[altpl_0]sd1[p17]clk[0] | 83.333       | -0.062     |
| 36   | 65.631 | Top:Top[Algorithm:alg]color_2_r[2] | Top:Top[Algorithm:alg]move_combo_r[6][3] | p10[altpl_0]sd1[p17]clk[0] | p10[altpl_0]sd1[p17]clk[0] | 83.333       | -0.081     |
| 37   | 65.631 | Top:Top[Algorithm:alg]color_2_r[2] | Top:Top[Algorithm:alg]move_combo_r[6][2] | p10[altpl_0]sd1[p17]clk[0] | p10[altpl_0]sd1[p17]clk[0] | 83.333       | -0.081     |
| 38   | 65.647 | Top:Top[Algorithm:alg]color_2_r[2] | Top:Top[Algorithm:alg]move_combo_r[0][1] | p10[altpl_0]sd1[p17]clk[0] | p10[altpl_0]sd1[p17]clk[0] | 83.333       | 0.321      |

| Multicorner Timing Analysis Summary |                           |        |       |          |         |                     |
|-------------------------------------|---------------------------|--------|-------|----------|---------|---------------------|
|                                     | Clock                     | Setup  | Hold  | Recovery | Removal | Minimum Pulse Width |
| 1                                   | Worst-case Slack          | -2.340 | 0.175 | N/A      | N/A     | 9.266               |
| 1                                   | CLOCK2_50                 | N/A    | N/A   | N/A      | N/A     | 16.000              |
| 2                                   | CLOCK3_50                 | N/A    | N/A   | N/A      | N/A     | 16.000              |
| 3                                   | CLOCK_50                  | 16.020 | 0.183 | N/A      | N/A     | 9.266               |
| 4                                   | p[0]a[tp]_0[sd1]p[7]ck[0] | -2.340 | 0.175 | N/A      | N/A     | 41.357              |
| 5                                   | p[0]a[tp]_0[sd1]p[7]ck[2] | 72.288 | 0.181 | N/A      | N/A     | 249999.708          |
| 2                                   | Design-wide TNS           | -8.965 | 0.0   | 0.0      | 0.0     | 0.0                 |
| 1                                   | CLOCK2_50                 | N/A    | N/A   | N/A      | N/A     | 0.000               |
| 2                                   | CLOCK3_50                 | N/A    | N/A   | N/A      | N/A     | 0.000               |
| 3                                   | CLOCK_50                  | 0.000  | 0.000 | N/A      | N/A     | 0.000               |
| 4                                   | p[0]a[tp]_0[sd1]p[7]ck[0] | -8.965 | 0.000 | N/A      | N/A     | 0.000               |
| 5                                   | p[0]a[tp]_0[sd1]p[7]ck[2] | 0.000  | 0.000 | N/A      | N/A     | 0.000               |

| Unconstrained Paths |                                 |       |       |
|---------------------|---------------------------------|-------|-------|
|                     | Property                        | Setup | Hold  |
| 1                   | Illegal Clocks                  | 0     | 0     |
| 2                   | Unconstrained Clocks            | 1     | 1     |
| 3                   | Unconstrained Input Ports       | 6     | 6     |
| 4                   | Unconstrained Input Port Paths  | 1475  | 1475  |
| 5                   | Unconstrained Output Ports      | 33    | 33    |
| 6                   | Unconstrained Output Port Paths | 15608 | 15608 |