

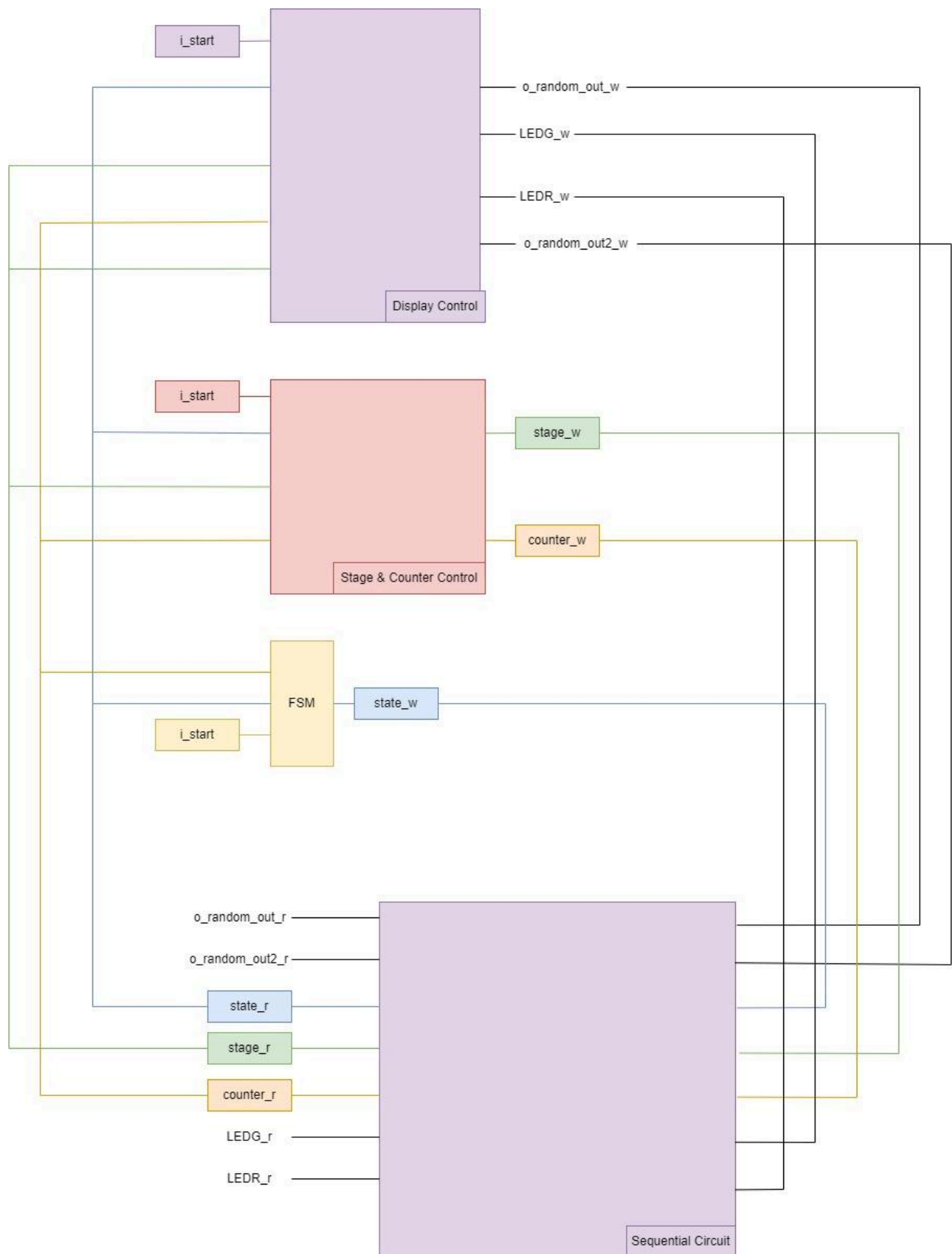
Team01 Lab1 Report

組員:B11901150、B11901152、B11901173

File Structure

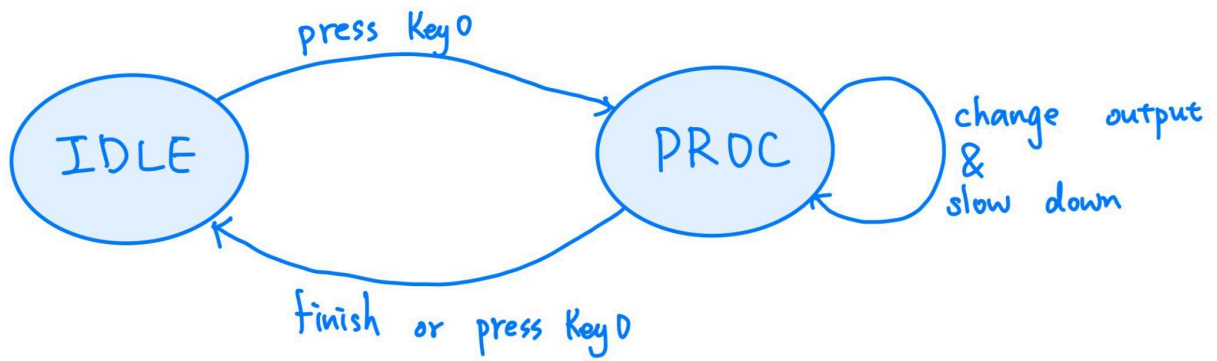
```
team01_lab1/  
├─ team01_lab1_report.pdf  
└─ src/  
    ├─ Top.sv  
    └─ DE2_115/  
        ├─ DE2_115.qsf  
        ├─ DE2_115.sdc  
        ├─ DE2_115.sv  
        ├─ Debounce.sv  
        └─ SevenHexDecoder.sv
```

System Architecture

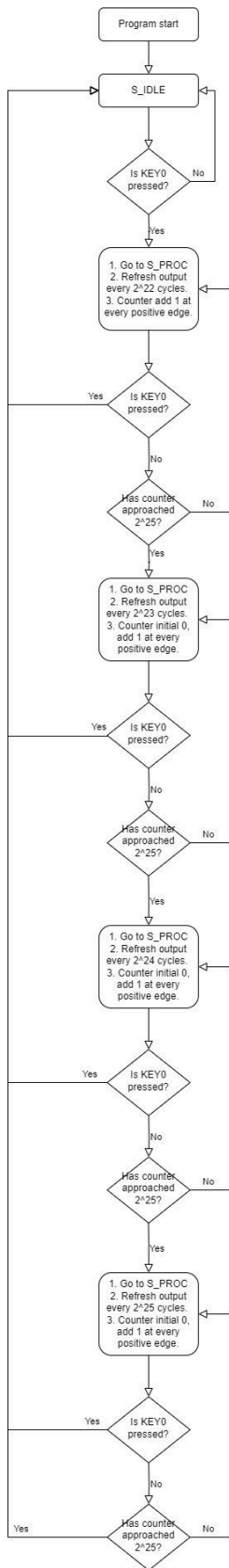


Hardware Scheduling

FSM



Algorithm Workflow



Fitter Summary

Compilation Report - DE2_115




























Table of Contents

- Flow Non-Default Global Sett
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- > Analysis & Synthesis
- ▼ Fitter
 - Summary**
 - Settings
 - Parallel Compilation
 - I/O Assignment Warning
 - Ignored Assignments
 - > Incremental Compilation
 - Pin-Out File
 - > Resource Section
 - > I/O Rules Section
 - Device Options
 - Operating Settings and C
 - > Estimated Delay Added f
 - Messages
 - Suppressed Messages
 - Flow Messages
 - Flow Suppressed Messages
- > Assembler
- ▼ TimeQuest Timing Analyzer
 - Summary
 - Parallel Compilation
 - SDC File List
 - Clocks
 - > Slow 1200mV 85C Model
 - > Slow 1200mV 0C Model
 - > Fast 1200mV 0C Model
 - Multicorner Timing Analy:
 - > Multicorner Datasheet R
 - > Advanced I/O Timin

Fitter Summary

Fitter Status	Successful - Thu Mar 07 22:29:30 2024
Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Full Version
Revision Name	DE2_115
Top-level Entity Name	DE2_115
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	119 / 114,480 (< 1 %)
Total combinational functions	115 / 114,480 (< 1 %)
Dedicated logic registers	54 / 114,480 (< 1 %)
Total registers	54
Total pins	518 / 529 (98 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

Timing Analyzer

Table of Contents		Unconstrained Paths		
 Flow Summary				
 Flow Settings				
 Flow Non-Default Global Settings				
 Flow Elapsed Time				
 Flow OS Summary				
 Flow Log				
>  Analysis & Synthesis				
>  Fitter				
 Flow Messages				
 Flow Suppressed Messages				
>  Assembler				
▼  TimeQuest Timing Analyzer				
 Summary				
 Parallel Compilation				
 SDC File List				
 Clocks				
>  Slow 1200mV 85C Model				
>  Slow 1200mV 0C Model				
>  Fast 1200mV 0C Model				
 Multicorner Timing Analysis S				
>  Multicorner Datasheet Repo				
>  Advanced I/O Timing				
>  Clock Transfers				
 Report TCCS				
 Report RSKM				
 Unconstrained Paths				
 Messages				

	Property	Setup	Hold
1	Illegal Clocks	0	0
2	Unconstrained Clocks	1	1
3	Unconstrained Input Ports	2	2
4	Unconstrained Input Port Paths	57	57
5	Unconstrained Output Ports	26	26
6	Unconstrained Output Port Paths	84	84