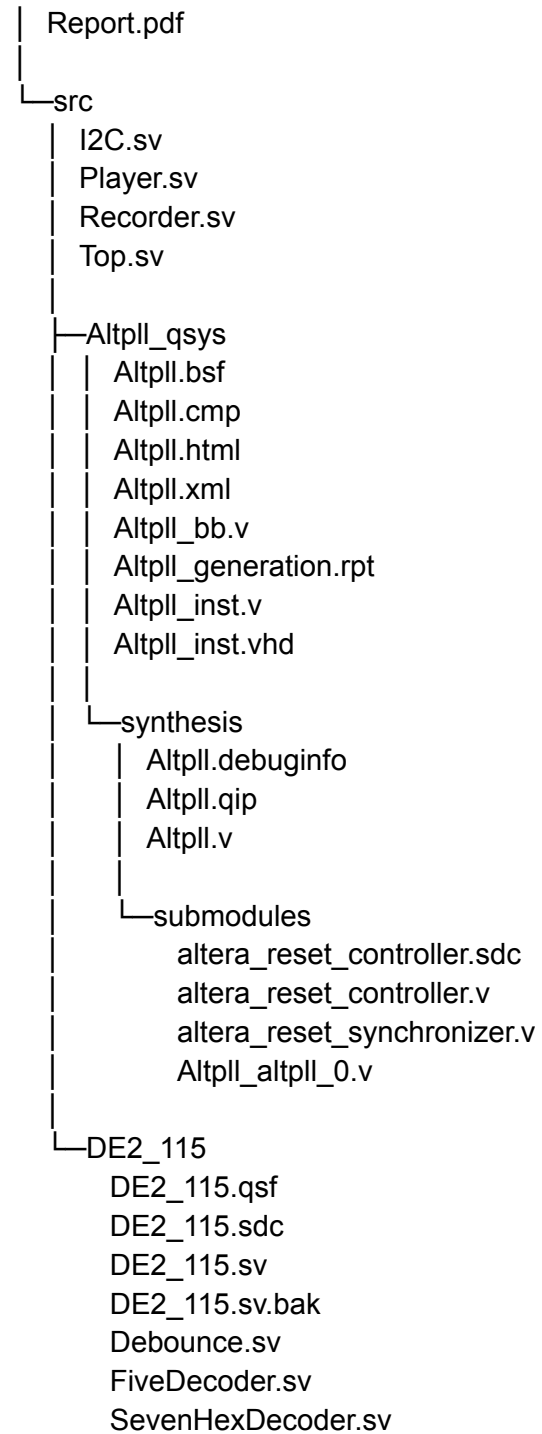


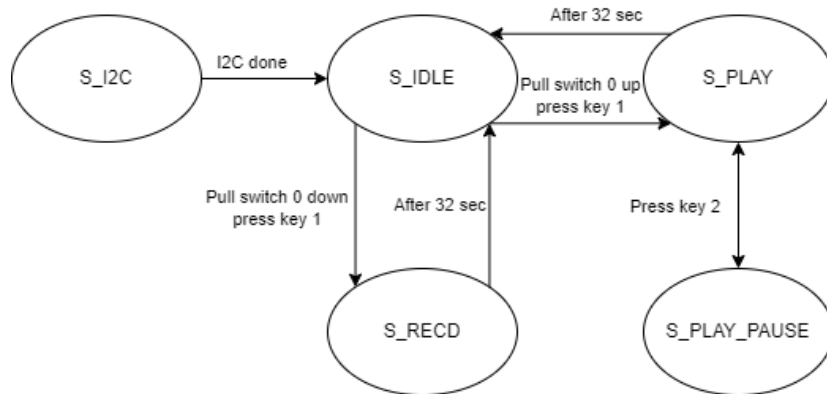
File Structure

team01_lab3

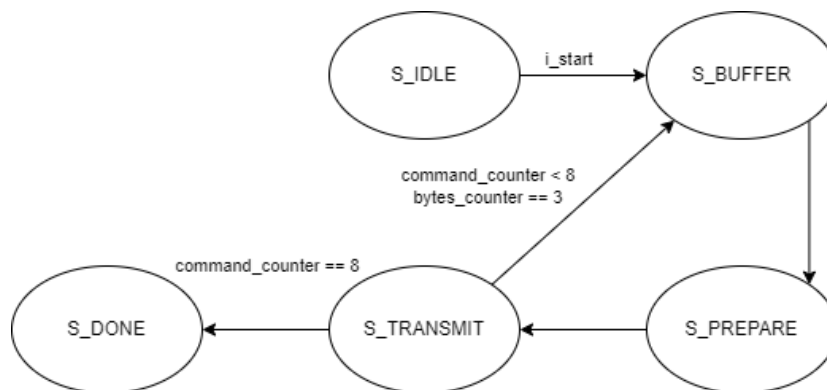


Hardware Scheduling

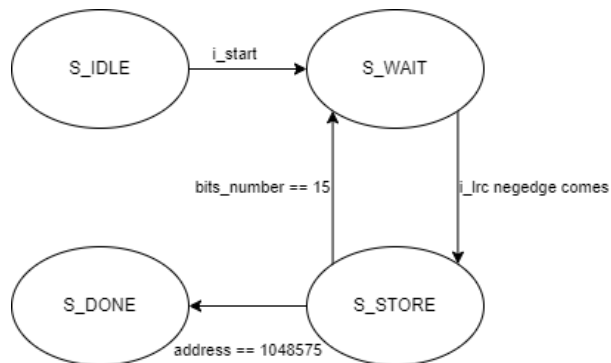
Top FSM:



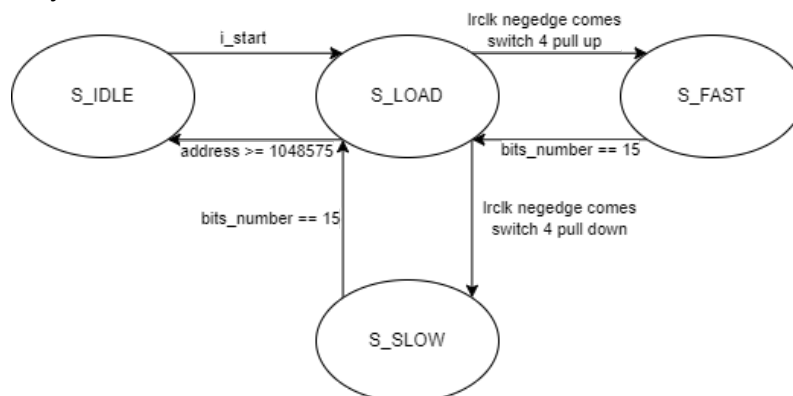
I2C FSM:



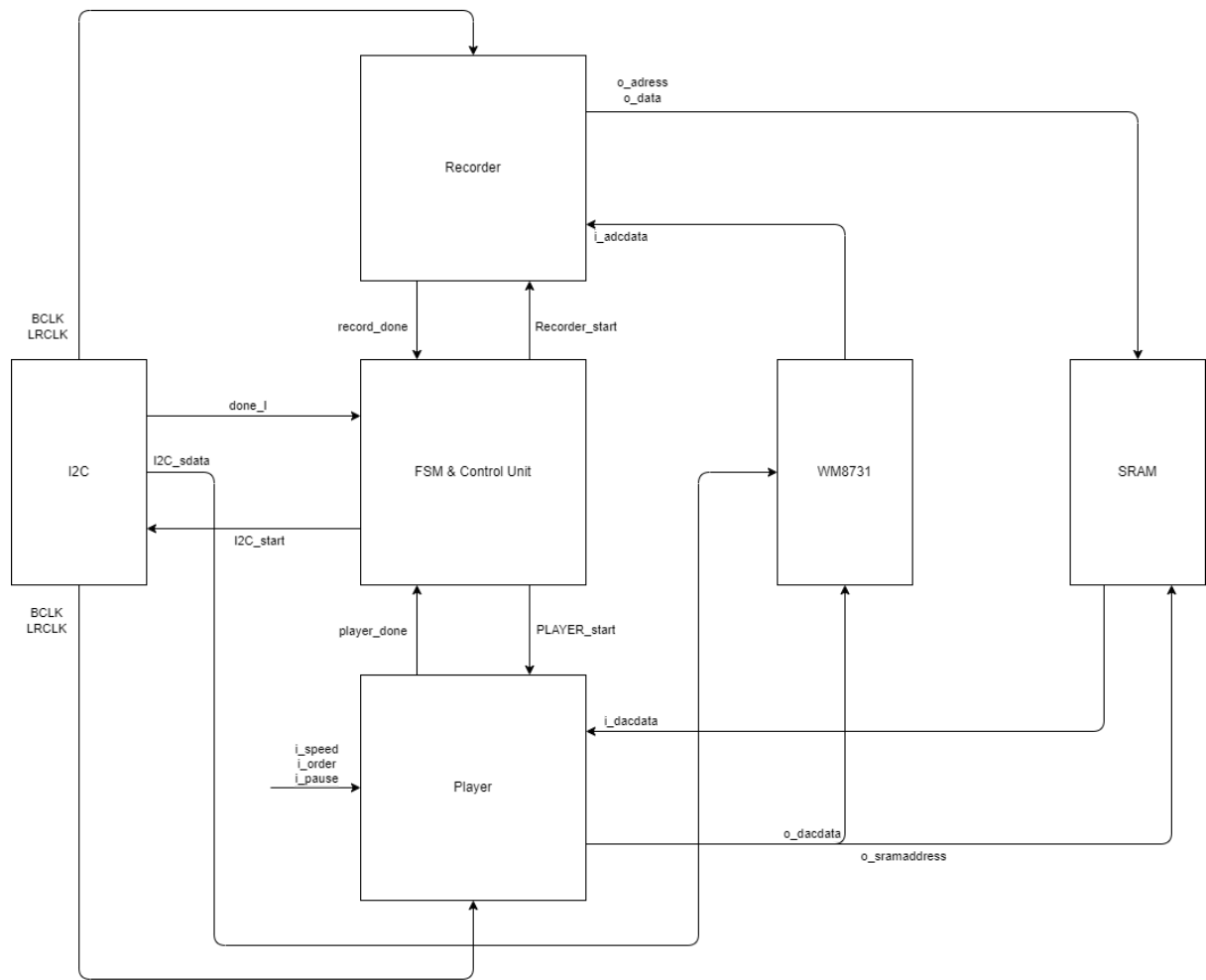
Recorder FSM:



Player FSM:



System Architecture



Fitter Summary

Altpll.v x Compilation Report - DE2_115 x Top.sv x Recorder.sv x Player.sv x DE2_115.sv x FiveDecoder.sv x

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Fitter Summary

Fitter Status	Successful - Fri Apr 19 11:51:00 2024
Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Full Version
Revision Name	DE2_115
Top-level Entity Name	DE2_115
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	1,540 / 114,480 (1 %)
Total combinational functions	1,480 / 114,480 (1 %)
Dedicated logic registers	275 / 114,480 (< 1 %)
Total registers	275
Total pins	480 / 529 (91 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	1 / 4 (25 %)

Timing Analyzer

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Timing Closure Recommendations

Summary [\[hide details\]](#)

This design contains failing setup paths with a worst-case slack of -45.594 ns. Run [Report Timing Closure Recommendations](#) for recommendations on how to close setup timing. For recommendations for any particular path, click the appropriate link in the table below.

Top Failing Paths [\[hide details\]](#)

Slack	From	To	Recommendations
1 -45.594	Top:top0 state_r_S_PLAY	Top:top0 AudPlaye...ayer0 diff_r[14]	Report recommendations for this path
2 -45.592	Top:top0 state_r_S_PLAY	Top:top0 AudPlaye...ayer0 diff_r[14]	Report recommendations for this path
3 -45.582	Top:top0 state_r_S_PLAY	Top:top0 AudPlaye...ayer0 diff_r[14]	Report recommendations for this path
4 -45.581	Top:top0 state_r_S_PLAY	Top:top0 AudPlaye...ayer0 diff_r[14]	Report recommendations for this path
5 -45.580	Top:top0 state_r_S_PLAY	Top:top0 AudPlaye...ayer0 diff_r[14]	Report recommendations for this path

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Slow 1200mV 85C Model Setup Summary

	Clock	Slack	End Point TNS
1	AUD_BCLK	-45.594	-950.366
2	pll0 altpll_0 sd1 pll7 clk[0]	-5.896	-22.038
3	pll0 altpll_0 sd1 pll7 clk[1]	80.603	0.000

Altpll.v	Compilation Report - DE2_115	Top.sv	Recorder.sv	Player.sv	DE2_115.sv	FiveDecoder.sv
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Slow 1200mV 85C Model Setup: 'AUD_BCLK'						
	Slack	From Node	To Node			
1	-45.594	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[14]			
2	-45.340	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[15]			
3	-45.261	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[5]			
4	-45.233	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[16]			
5	-45.173	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[13]			
6	-45.012	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[11]			
7	-45.009	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[7]			
8	-44.924	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[9]			
9	-44.909	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[12]			
10	-44.896	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[8]			
11	-44.872	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[4]			
12	-44.833	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[10]			
13	-44.771	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[3]			
14	-44.751	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[1]			
15	-44.722	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[6]			
16	-44.507	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[2]			
17	-44.010	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[0]			
18	-3.928	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_2nd_r[6]			
19	-3.927	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_2nd_r[5]			
20	-3.927	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_5th_r[1]			
21	-3.835	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_3rd_r[0]			
22	-3.808	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_4th_r[3]			
23	-3.797	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_1st_r[3]			
24	-3.796	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_1st_r[4]			
25	-3.796	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_1st_r[6]			
26	-3.795	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_1st_r[0]			
27	-3.795	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_1st_r[5]			
28	-3.777	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_2nd_r[6]			
29	-3.776	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_2nd_r[5]			
30	-3.776	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_5th_r[1]			
31	-3.716	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_4th_r[6]			
32	-3.712	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_3rd_r[0]			
33	-3.702	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_3rd_r[6]			
34	-3.700	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_2nd_r[1]			
35	-3.697	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_5th_r[2]			
36	-3.695	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_4th_r[5]			
37	-3.694	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_5th_r[0]			
38	-3.694	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_5th_r[4]			

Altpll.v	Compilation Report - DE2_115	Top.sv	Recorder.sv	Player.sv	DE2_115.sv	FiveDecoder.sv
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Slow 1200mV 85C Model Setup: 'AUD_BCLK'						
	Slack	From Node	To Node			
39	-3.693	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_2nd_r[4]			
40	-3.693	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_5th_r[5]			
41	-3.671	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_5th_r[2]			
42	-3.669	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_4th_r[5]			
43	-3.668	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_5th_r[0]			
44	-3.668	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_5th_r[4]			
45	-3.667	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_2nd_r[4]			
46	-3.667	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_5th_r[5]			
47	-3.648	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_1st_r[3]			
48	-3.647	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_1st_r[4]			
49	-3.647	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_1st_r[5]			
50	-3.647	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_1st_r[6]			
51	-3.646	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_1st_r[0]			
52	-3.629	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_2nd_r[3]			
53	-3.628	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_2nd_r[0]			
54	-3.628	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_4th_r[1]			
55	-3.627	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_4th_r[2]			
56	-3.611	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_4th_r[3]			
57	-3.606	Top:top0 PLAYER_start_r	Top:top0 AudPlayer:player0 state_r.S_SLOW			
58	-3.596	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_3rd_r[3]			
59	-3.557	Top:top0 PLAYER_start_r	Top:top0 AudPlayer:player0 state_r.S_FAST			
60	-3.519	Top:top0 PLAYER_start_r	Top:top0 AudPlayer:player0 state_r.S_PAUSE			
61	-3.506	Top:top0 PLAYER_start_r	Top:top0 AudPlayer:player0 state_r.S_IDLE			
62	-3.506	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_2nd_r[3]			
63	-3.505	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_2nd_r[0]			
64	-3.505	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_4th_r[1]			
65	-3.504	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_4th_r[2]			
66	-3.462	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_4th_r[6]			
67	-3.455	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[15]			
68	-3.421	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_3rd_r[6]			
69	-3.419	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_2nd_r[1]			
70	-3.382	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 state_r.S_LOAD			
71	-3.327	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[11]			
72	-3.326	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_3rd_r[3]			
73	-3.304	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[0]			
74	-3.295	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[9]			
75	-3.247	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[1]			
76	-3.243	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[8]			

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Slow 1200mV 85C Model Setup: 'AUD_BCLK'						
	Slack	From Node	To Node			
63	-3.505	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_2nd_r[0]	pll0		
64	-3.505	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_4th_r[1]	pll0		
65	-3.504	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_4th_r[2]	pll0		
66	-3.462	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_4th_r[6]	pll0		
67	-3.455	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[15]	pll0		
68	-3.421	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_3rd_r[6]	pll0		
69	-3.419	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_2nd_r[1]	pll0		
70	-3.382	Top:top0 PLAYER_start_r	Top:top0 AudPlayer:player0 state_r.S_LOAD	pll0		
71	-3.327	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[11]	pll0		
72	-3.326	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_3rd_r[3]	pll0		
73	-3.304	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[0]	pll0		
74	-3.295	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[9]	pll0		
75	-3.247	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[4]	pll0		
76	-3.243	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[8]	pll0		
77	-3.242	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[6]	pll0		
78	-3.220	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[4]	pll0		
79	-3.208	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[12]	pll0		
80	-3.203	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[14]	pll0		
81	-3.187	Top:top0 RECORDER_start_r	Top:top0 AudRecorder:recorder0 state_r.S_STORE	pll0		
82	-3.185	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[13]	pll0		
83	-3.167	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[3]	pll0		
84	-3.158	Top:top0 RECORDER_start_r	Top:top0 AudRecorder:recorder0 state_r.S_WAIT	pll0		
85	-3.150	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_3rd_r[1]	pll0		
86	-3.126	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_2nd_r[2]	pll0		
87	-3.118	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[10]	pll0		
88	-3.112	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[2]	pll0		
89	-3.094	Top:top0 RECORDER_start_r	Top:top0 AudRecorder:recorder0 state_r.S_IDLE	pll0		
90	-3.092	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[7]	pll0		
91	-3.090	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_3rd_r[2]	pll0		
92	-3.082	Debounce:deb2 neg_r	Top:top0 AudPlayer:player0 pause_r	pll0		
93	-3.016	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[5]	pll0		
94	-2.964	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_5th_r[6]	pll0		
95	-2.898	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_4th_r[0]	pll0		
96	33.552	Top:top0 AudPlayer:player0 next_data_r[0]	Top:top0 AudPlayer:player0 diff_r[14]	AUC		
97	33.659	Top:top0 AudPlayer:player0 next_data_r[3]	Top:top0 AudPlayer:player0 diff_r[14]	AUC		
98	33.806	Top:top0 AudPlayer:player0 next_data_r[0]	Top:top0 AudPlayer:player0 diff_r[15]	AUC		
99	33.820	Top:top0 AudPlayer:player0 next_data_r[1]	Top:top0 AudPlayer:player0 diff_r[14]	AUC		
100	33.841	Top:top0 AudPlayer:player0 next_data_r[4]	Top:top0 AudPlayer:player0 diff_r[14]	AUC		

Altpll.v	Compilation Report - DE2_115	Top.sv	Recorder.sv	Player.sv	DE2_115.sv	FiveDecoder.sv
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Slow 1200mV 85C Model Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'						
	Slack	From Node	To Node	Launch Clock		
1	-5.896	Top:top0 AudPlayer:player0 done_r	Top:top0 state_r.S_PLAY	AUD_BCLK		
2	-5.490	Top:top0 AudPlayer:player0 done_r	Top:top0 state_r.S_PLAY_PAUSE	AUD_BCLK		
3	-5.484	Top:top0 AudPlayer:player0 done_r	Top:top0 state_r.S_IDLE	AUD_BCLK		
4	-5.178	Top:top0 AudRecorder:recorder0 done_r	Top:top0 state_r.S_IDLE	AUD_BCLK		
5	-5.168	Top:top0 AudRecorder:recorder0 done_r	Top:top0 state_r.S_REC'D	AUD_BCLK		
6	72.258	Top:top0 five_dec_r[1]	Top:top0 five_dec_r[1]	pll0 altpll_0 sd1 pll7 clk[0]		
7	74.522	Top:top0 five_dec_r[0]	Top:top0 five_dec_r[0]	pll0 altpll_0 sd1 pll7 clk[0]		
8	74.567	Debounce:deb1 neg_r	Top:top0 state_r.S_PLAY	pll0 altpll_0 sd1 pll7 clk[0]		
9	75.018	Top:top0 state_r.S_REC'D	Top:top0 five_dec_r[1]	pll0 altpll_0 sd1 pll7 clk[0]		
10	75.510	Top:top0 state_r.S_PLAY_PAUSE	Top:top0 five_dec_r[1]	pll0 altpll_0 sd1 pll7 clk[0]		
11	75.543	Top:top0 state_r.S_I2C	Top:top0 five_dec_r[1]	pll0 altpll_0 sd1 pll7 clk[0]		
12	76.605	Top:top0 state_r.S_PLAY	Top:top0 five_dec_r[0]	pll0 altpll_0 sd1 pll7 clk[0]		
13	77.505	Debounce:deb1 neg_r	Top:top0 state_r.S_IDLE	pll0 altpll_0 sd1 pll7 clk[0]		
14	77.662	Debounce:deb1 neg_r	Top:top0 state_r.S_REC'D	pll0 altpll_0 sd1 pll7 clk[0]		
15	77.700	Top:top0 state_r.S_IDLE	Top:top0 state_r.S_PLAY	pll0 altpll_0 sd1 pll7 clk[0]		
16	78.222	Debounce:deb2 neg_r	Top:top0 state_r.S_PLAY	pll0 altpll_0 sd1 pll7 clk[0]		
17	78.605	Top:top0 state_r.S_PLAY	Top:top0 PLAYER_start_r	pll0 altpll_0 sd1 pll7 clk[0]		
18	78.683	Top:top0 state_r.S_PLAY	Top:top0 state_r.S_PLAY	pll0 altpll_0 sd1 pll7 clk[0]		
19	78.742	Top:top0 state_r.S_PLAY_PAUSE	Top:top0 state_r.S_PLAY	pll0 altpll_0 sd1 pll7 clk[0]		
20	79.089	Top:top0 state_r.S_PLAY	Top:top0 state_r.S_IDLE	pll0 altpll_0 sd1 pll7 clk[0]		
21	79.126	Top:top0 state_r.S_PLAY_PAUSE	Top:top0 five_dec_r[0]	pll0 altpll_0 sd1 pll7 clk[0]		
22	79.135	Top:top0 state_r.S_I2C	Top:top0 five_dec_r[0]	pll0 altpll_0 sd1 pll7 clk[0]		
23	79.495	Top:top0 state_r.S_PLAY	Top:top0 state_r.S_PLAY_PAUSE	pll0 altpll_0 sd1 pll7 clk[0]		
24	79.840	Debounce:deb0 neg_r	Top:top0 state_r.S_PLAY	pll0 altpll_0 sd1 pll7 clk[0]		
25	79.850	Top:top0 state_r.S_PLAY	Top:top0 led_r[1]	pll0 altpll_0 sd1 pll7 clk[0]		
26	79.851	Top:top0 state_r.S_PLAY	Top:top0 led_r[0]	pll0 altpll_0 sd1 pll7 clk[0]		
27	80.203	Debounce:deb0 neg_r	Top:top0 state_r.S_REC'D	pll0 altpll_0 sd1 pll7 clk[0]		
28	80.222	Debounce:deb0 neg_r	Top:top0 state_r.S_I2C	pll0 altpll_0 sd1 pll7 clk[0]		
29	80.256	Debounce:deb2 neg_r	Top:top0 state_r.S_IDLE	pll0 altpll_0 sd1 pll7 clk[0]		
30	80.408	Top:top0 PLAYER_start_r	Top:top0 PLAYER_start_r	pll0 altpll_0 sd1 pll7 clk[0]		
31	80.417	Debounce:deb0 neg_r	Top:top0 state_r.S_IDLE	pll0 altpll_0 sd1 pll7 clk[0]		
32	80.418	Debounce:deb0 neg_r	Top:top0 state_r.S_PLAY_PAUSE	pll0 altpll_0 sd1 pll7 clk[0]		
33	80.433	Top:top0 state_r.S_REC'D	Top:top0 state_r.S_IDLE	pll0 altpll_0 sd1 pll7 clk[0]		
34	80.548	Debounce:deb2 counter_r[0]	Debounce:deb2 neg_r	pll0 altpll_0 sd1 pll7 clk[0]		
35	80.584	Debounce:deb2 counter_r[2]	Debounce:deb2 neg_r	pll0 altpll_0 sd1 pll7 clk[0]		
36	80.692	Debounce:deb2 counter_r[1]	Debounce:deb2 neg_r	pll0 altpll_0 sd1 pll7 clk[0]		
37	80.819	Top:top0 state_r.S_IDLE	Top:top0 state_r.S_REC'D	pll0 altpll_0 sd1 pll7 clk[0]		
38	80.819	Top:top0 state_r.S_IDLE	Top:top0 state_r.S_IDLE	pll0 altpll_0 sd1 pll7 clk[0]		

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Setup: 'pll0|altpll_0|sd1|pll7|clk[1]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[0]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[1]'

Hold: 'AUD_BCLK'

Minimum Pulse Width: 'CLOCK_50'

Minimum Pulse Width: 'CLOCK2_50'

Minimum Pulse Width: 'CLOCK3_50'

Minimum Pulse Width: 'AUD_BCLK'

Minimum Pulse Width: 'pll0|altpll_0|sc'

Minimum Pulse Width: 'pll0|altpll_0|sc'

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Slow 1200mV 0C Model Setup Summary

	Clock	Slack	End Point TNS
1	AUD_BCLK	-41.301	-867.886
2	pll0 altpll_0 sd1 pll7 clk[0]	-5.394	-20.072
3	pll0 altpll_0 sd1 pll7 clk[1]	80.818	0.000

Table of Contents	Slow 1200mV 0C Model Setup: 'AUD_BCLK'			
<ul style="list-style-type: none"> Setup Summary Hold Summary Recovery Summary Removal Summary Minimum Pulse Width Summary Worst-Case Timing Paths <ul style="list-style-type: none"> Setup: 'AUD_BCLK' Setup: 'pll0 altpll_0 sd1 pll7 clk[0]' Setup: 'pll0 altpll_0 sd1 pll7 clk[1]' Hold: 'pll0 altpll_0 sd1 pll7 clk[0]' Hold: 'pll0 altpll_0 sd1 pll7 clk[1]' Hold: 'AUD_BCLK' Minimum Pulse Width: 'CLOCK_50' Minimum Pulse Width: 'CLOCK2_50' Minimum Pulse Width: 'CLOCK3_50' Minimum Pulse Width: 'AUD_BCLK' Minimum Pulse Width: 'pll0 altpll_0 sc' Minimum Pulse Width: 'pll0 altpll_0 sc' Datasheet Report Metastability Summary Slow 1200mV 0C Model <ul style="list-style-type: none"> Fmax Summary Setup Summary Hold Summary Recovery Summary Removal Summary Minimum Pulse Width Summary Worst-Case Timing Paths <ul style="list-style-type: none"> Setup: 'AUD_BCLK' Setup: 'pll0 altpll_0 sd1 pll7 clk[0]' Setup: 'pll0 altpll_0 sd1 pll7 clk[1]' Hold: 'pll0 altpll_0 sd1 pll7 clk[0]' Hold: 'pll0 altpll_0 sd1 pll7 clk[1]' Hold: 'AUD_BCLK' 	Slack	From Node	To Node	
1	-41.301	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[14]	pll0
2	-41.044	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[5]	pll0
3	-40.999	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[15]	pll0
4	-40.980	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[16]	pll0
5	-40.895	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[13]	pll0
6	-40.783	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[7]	pll0
7	-40.770	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[11]	pll0
8	-40.712	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[9]	pll0
9	-40.706	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[12]	pll0
10	-40.705	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[8]	pll0
11	-40.666	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[4]	pll0
12	-40.606	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[10]	pll0
13	-40.561	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[6]	pll0
14	-40.548	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[3]	pll0
15	-40.537	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[1]	pll0
16	-40.320	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[2]	pll0
17	-39.880	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 diff_r[0]	pll0
18	-3.614	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_2nd_r[6]	pll0
19	-3.613	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_2nd_r[5]	pll0
20	-3.612	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_5th_r[1]	pll0
21	-3.576	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_1st_r[3]	pll0
22	-3.575	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_1st_r[4]	pll0
23	-3.574	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_1st_r[0]	pll0
24	-3.574	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_1st_r[5]	pll0
25	-3.574	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_1st_r[6]	pll0
26	-3.572	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_3rd_r[0]	pll0
27	-3.551	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_4th_r[3]	pll0
28	-3.538	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_4th_r[6]	pll0
29	-3.532	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_5th_r[2]	pll0
30	-3.528	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_2nd_r[4]	pll0
31	-3.525	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_3rd_r[6]	pll0
32	-3.523	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_2nd_r[1]	pll0
33	-3.522	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_3rd_r[0]	pll0
34	-3.520	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_4th_r[5]	pll0
35	-3.519	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_5th_r[0]	pll0
36	-3.518	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_5th_r[4]	pll0
37	-3.518	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_5th_r[5]	pll0
38	-3.518	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_5th_r[2]	pll0

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Slow 1200mV 0C Model Setup: 'AUD_BCLK'						
Setup Summary		Slack	From Node	To Node		
Hold Summary		39 -3.514	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_2nd_r[4]	pll0	
Recovery Summary		40 -3.506	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_4th_r[5]	pll0	
Removal Summary		41 -3.505	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_5th_r[0]	pll0	
Minimum Pulse Width Summary		42 -3.504	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_5th_r[4]	pll0	
Worst-Case Timing Paths		43 -3.504	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_5th_r[5]	pll0	
Setup: 'AUD_BCLK'		44 -3.477	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_1st_r[3]	pll0	
Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'		45 -3.476	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_1st_r[4]	pll0	
Setup: 'pll0 altpll_0 sd1 pll7 clk[1]'		46 -3.475	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_1st_r[0]	pll0	
Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'		47 -3.475	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_1st_r[5]	pll0	
Hold: 'pll0 altpll_0 sd1 pll7 clk[1]'		48 -3.475	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_1st_r[6]	pll0	
Hold: 'AUD_BCLK'		49 -3.452	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_4th_r[3]	pll0	
Minimum Pulse Width: 'CLOCK_50'		50 -3.450	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_2nd_r[6]	pll0	
Minimum Pulse Width: 'CLOCK2_50'		51 -3.449	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_2nd_r[5]	pll0	
Minimum Pulse Width: 'CLOCK3_50'		52 -3.448	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_5th_r[1]	pll0	
Minimum Pulse Width: 'AUD_BCLK'		53 -3.440	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_3rd_r[3]	pll0	
Minimum Pulse Width: 'pll0 altpll_0 sc		54 -3.395	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_2nd_r[0]	pll0	
Minimum Pulse Width: 'pll0 altpll_0 sc		55 -3.395	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_2nd_r[3]	pll0	
Datasheet Report		56 -3.395	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_4th_r[1]	pll0	
Metastability Summary		57 -3.394	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_4th_r[2]	pll0	
Slow 1200mV 0C Model		58 -3.357	Top:top0 PLAYER_start_r	Top:top0 AudPlayer:player0 state_r.S_SLOW	pll0	
Fmax Summary		59 -3.356	Top:top0 PLAYER_start_r	Top:top0 AudPlayer:player0 state_r.S_PAUSE	pll0	
Setup Summary		60 -3.345	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_2nd_r[0]	pll0	
Hold Summary		61 -3.345	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_2nd_r[3]	pll0	
Recovery Summary		62 -3.345	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_4th_r[1]	pll0	
Removal Summary		63 -3.344	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_4th_r[2]	pll0	
Minimum Pulse Width Summary		64 -3.335	Top:top0 PLAYER_start_r	Top:top0 AudPlayer:player0 state_r.S_IDLE	pll0	
Worst-Case Timing Paths		65 -3.333	Top:top0 PLAYER_start_r	Top:top0 AudPlayer:player0 state_r.S_FAST	pll0	
Setup: 'AUD_BCLK'		66 -3.250	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[15]	pll0	
Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'		67 -3.197	Top:top0 PLAYER_start_r	Top:top0 AudPlayer:player0 state_r.S_LOAD	pll0	
Setup: 'pll0 altpll_0 sd1 pll7 clk[1]'		68 -3.154	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[11]	pll0	
Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'		69 -3.148	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_4th_r[6]	pll0	
Hold: 'pll0 altpll_0 sd1 pll7 clk[1]'		70 -3.133	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[9]	pll0	
Hold: 'AUD_BCLK'		71 -3.123	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[0]	pll0	
Minimum Pulse Width: 'CLOCK_50'		72 -3.123	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_3rd_r[6]	pll0	
Minimum Pulse Width: 'CLOCK2_50'		73 -3.121	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_2nd_r[1]	pll0	
Minimum Pulse Width: 'CLOCK3_50'		74 -3.084	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[8]	pll0	
Minimum Pulse Width: 'AUD_BCLK'		75 -3.077	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[1]	pll0	
Minimum Pulse Width: 'pll0 altpll_0 sc		76 -3.066	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[12]	pll0	

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Slow 1200mV 0C Model Setup: 'AUD_BCLK'						
Setup Summary		Slack	From Node	To Node		
Hold Summary		63 -3.344	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_4th_r[2]	pll0	
Recovery Summary		64 -3.335	Top:top0 PLAYER_start_r	Top:top0 AudPlayer:player0 state_r.S_IDLE	pll0	
Removal Summary		65 -3.333	Top:top0 PLAYER_start_r	Top:top0 AudPlayer:player0 state_r.S_FAST	pll0	
Minimum Pulse Width Summary		66 -3.250	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[15]	pll0	
Worst-Case Timing Paths		67 -3.197	Top:top0 PLAYER_start_r	Top:top0 AudPlayer:player0 state_r.S_LOAD	pll0	
Setup: 'AUD_BCLK'		68 -3.154	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[11]	pll0	
Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'		69 -3.148	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_4th_r[6]	pll0	
Setup: 'pll0 altpll_0 sd1 pll7 clk[1]'		70 -3.133	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[9]	pll0	
Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'		71 -3.123	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[0]	pll0	
Hold: 'pll0 altpll_0 sd1 pll7 clk[1]'		72 -3.123	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_3rd_r[6]	pll0	
Hold: 'AUD_BCLK'		73 -3.121	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_2nd_r[1]	pll0	
Minimum Pulse Width: 'CLOCK_50'		74 -3.084	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[8]	pll0	
Minimum Pulse Width: 'CLOCK2_50'		75 -3.077	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[1]	pll0	
Minimum Pulse Width: 'CLOCK3_50'		76 -3.066	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[12]	pll0	
Minimum Pulse Width: 'AUD_BCLK'		77 -3.054	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[14]	pll0	
Minimum Pulse Width: 'pll0 altpll_0 sc		78 -3.054	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[6]	pll0	
Minimum Pulse Width: 'pll0 altpll_0 sc		79 -3.051	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[4]	pll0	
Datasheet Report		80 -3.039	Top:top0 RECORDER_start_r	Top:top0 AudRecorder:recorder0 state_r.S_STORE	pll0	
Metastability Summary		81 -3.038	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_3rd_r[3]	pll0	
Slow 1200mV 0C Model		82 -3.033	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[13]	pll0	
Fmax Summary		83 -3.014	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[3]	pll0	
Setup Summary		84 -2.994	Top:top0 RECORDER_start_r	Top:top0 AudRecorder:recorder0 state_r.S_WAIT	pll0	
Hold Summary		85 -2.982	Debounce:deb2 neg_r	Top:top0 AudPlayer:player0 pause_r	pll0	
Recovery Summary		86 -2.970	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[2]	pll0	
Removal Summary		87 -2.966	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[10]	pll0	
Minimum Pulse Width Summary		88 -2.960	Top:top0 RECORDER_start_r	Top:top0 AudRecorder:recorder0 state_r.S_IDLE	pll0	
Worst-Case Timing Paths		89 -2.900	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_3rd_r[1]	pll0	
Setup: 'AUD_BCLK'		90 -2.881	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[5]	pll0	
Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'		91 -2.862	Top:top0 state_r.S_PLAY	Top:top0 AudPlayer:player0 next_data_r[7]	pll0	
Setup: 'pll0 altpll_0 sd1 pll7 clk[1]'		92 -2.848	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_2nd_r[2]	pll0	
Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'		93 -2.805	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_3rd_r[2]	pll0	
Hold: 'pll0 altpll_0 sd1 pll7 clk[1]'		94 -2.743	Top:top0 five_dec_r[0]	FiveDecoder:dec1 seven_5th_r[6]	pll0	
Hold: 'AUD_BCLK'		95 -2.677	Top:top0 five_dec_r[1]	FiveDecoder:dec1 seven_4th_r[0]	pll0	
Minimum Pulse Width: 'CLOCK_50'		96 38.158	Top:top0 AudPlayer:player0 next_data_r[0]	Top:top0 AudPlayer:player0 diff_r[14]	AUC	
Minimum Pulse Width: 'CLOCK2_50'		97 38.255	Top:top0 AudPlayer:player0 next_data_r[3]	Top:top0 AudPlayer:player0 diff_r[14]	AUC	
Minimum Pulse Width: 'CLOCK3_50'		98 38.411	Top:top0 AudPlayer:player0 next_data_r[4]	Top:top0 AudPlayer:player0 diff_r[14]	AUC	
Minimum Pulse Width: 'AUD_BCLK'		99 38.411	Top:top0 AudPlayer:player0 next_data_r[1]	Top:top0 AudPlayer:player0 diff_r[14]	AUC	
Minimum Pulse Width: 'pll0 altpll_0 sc		100 38.429	Top:top0 AudPlayer:player0 next_data_r[0]	Top:top0 AudPlayer:player0 diff_r[5]	AUC	

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Setup: 'AUD_BCLK'

Setup: 'pll0|altpll_0|sd1|pll7|clk[0]'

Setup: 'pll0|altpll_0|sd1|pll7|clk[1]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[0]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[1]'

Hold: 'AUD_BCLK'

Minimum Pulse Width: 'CLOCK_50'

Minimum Pulse Width: 'CLOCK2_50'

Minimum Pulse Width: 'CLOCK3_50'

Minimum Pulse Width: 'AUD_BCLK'

Minimum Pulse Width: 'pll0|altpll_0|sc'

Minimum Pulse Width: 'pll0|altpll_0|sc'

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Worst-Case Timing Paths

Setup: 'AUD_BCLK'

Setup: 'pll0|altpll_0|sd1|pll7|clk[0]'

Setup: 'pll0|altpll_0|sd1|pll7|clk[1]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[0]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[1]'

Slow 1200mV 0C Model Setup: 'pll0|altpll_0|sd1|pll7|clk[0]'

	Slack	From Node	To Node	Launch Clock
1	-5.394	Top:top0 AudPlayer:player0 done_r	Top:top0 state_r_S_PLAY	AUD_BCLK
2	-5.001	Top:top0 AudPlayer:player0 done_r	Top:top0 state_r_S_PLAY_PAUSE	AUD_BCLK
3	-4.987	Top:top0 AudPlayer:player0 done_r	Top:top0 state_r_S_IDLE	AUD_BCLK
4	-4.722	Top:top0 AudRecorder:recorder0 done_r	Top:top0 state_r_S_IDLE	AUD_BCLK
5	-4.690	Top:top0 AudRecorder:recorder0 done_r	Top:top0 state_r_S_REC'D	AUD_BCLK
6	73.118	Top:top0 five_dec_r[1]	Top:top0 five_dec_r[1]	pll0 altpll_0 sd1 pll7 clk[0]
7	75.181	Debounce:deb1 neg_r	Top:top0 state_r_S_PLAY	pll0 altpll_0 sd1 pll7 clk[0]
8	75.401	Top:top0 five_dec_r[0]	Top:top0 five_dec_r[0]	pll0 altpll_0 sd1 pll7 clk[0]
9	75.582	Top:top0 state_r_S_REC'D	Top:top0 five_dec_r[1]	pll0 altpll_0 sd1 pll7 clk[0]
10	76.039	Top:top0 state_r_S_PLAY_PAUSE	Top:top0 five_dec_r[1]	pll0 altpll_0 sd1 pll7 clk[0]
11	76.114	Top:top0 state_r_S_I2C	Top:top0 five_dec_r[1]	pll0 altpll_0 sd1 pll7 clk[0]
12	77.260	Top:top0 state_r_S_PLAY	Top:top0 five_dec_r[0]	pll0 altpll_0 sd1 pll7 clk[0]
13	77.857	Debounce:deb1 neg_r	Top:top0 state_r_S_IDLE	pll0 altpll_0 sd1 pll7 clk[0]
14	78.019	Debounce:deb1 neg_r	Top:top0 state_r_S_REC'D	pll0 altpll_0 sd1 pll7 clk[0]
15	78.164	Top:top0 state_r_S_IDLE	Top:top0 state_r_S_PLAY	pll0 altpll_0 sd1 pll7 clk[0]
16	78.686	Debounce:deb2 neg_r	Top:top0 state_r_S_PLAY	pll0 altpll_0 sd1 pll7 clk[0]
17	78.927	Top:top0 state_r_S_PLAY	Top:top0 PLAYER_start_r	pll0 altpll_0 sd1 pll7 clk[0]
18	79.063	Top:top0 state_r_S_PLAY	Top:top0 state_r_S_PLAY	pll0 altpll_0 sd1 pll7 clk[0]
19	79.223	Top:top0 state_r_S_PLAY_PAUSE	Top:top0 state_r_S_PLAY	pll0 altpll_0 sd1 pll7 clk[0]
20	79.415	Top:top0 state_r_S_PLAY_PAUSE	Top:top0 state_r_S_IDLE	pll0 altpll_0 sd1 pll7 clk[0]
21	79.515	Top:top0 state_r_S_PLAY_PAUSE	Top:top0 five_dec_r[0]	pll0 altpll_0 sd1 pll7 clk[0]
22	79.549	Top:top0 state_r_S_PLAY_PAUSE	Top:top0 five_dec_r[0]	pll0 altpll_0 sd1 pll7 clk[0]
23	79.812	Top:top0 state_r_S_PLAY	Top:top0 state_r_S_PLAY_PAUSE	pll0 altpll_0 sd1 pll7 clk[0]
24	80.146	Top:top0 state_r_S_PLAY	Top:top0 ledr_r[1]	pll0 altpll_0 sd1 pll7 clk[0]
25	80.149	Top:top0 state_r_S_PLAY	Top:top0 ledr_r[0]	pll0 altpll_0 sd1 pll7 clk[0]
26	80.185	Debounce:deb0 neg_r	Top:top0 state_r_S_PLAY	pll0 altpll_0 sd1 pll7 clk[0]
27	80.521	Debounce:deb2 neg_r	Top:top0 state_r_S_IDLE	pll0 altpll_0 sd1 pll7 clk[0]
28	80.521	Debounce:deb0 neg_r	Top:top0 state_r_S_REC'D	pll0 altpll_0 sd1 pll7 clk[0]
29	80.526	Debounce:deb0 neg_r	Top:top0 state_r_S_I2C	pll0 altpll_0 sd1 pll7 clk[0]
30	80.597	Top:top0 PLAYER_start_r	Top:top0 PLAYER_start_r	pll0 altpll_0 sd1 pll7 clk[0]
31	80.628	Top:top0 state_r_S_REC'D	Top:top0 state_r_S_IDLE	pll0 altpll_0 sd1 pll7 clk[0]
32	80.708	Debounce:deb0 neg_r	Top:top0 state_r_S_PLAY_PAUSE	pll0 altpll_0 sd1 pll7 clk[0]
33	80.708	Debounce:deb0 neg_r	Top:top0 state_r_S_IDLE	pll0 altpll_0 sd1 pll7 clk[0]
34	80.760	Debounce:deb2 counter_r[0]	Debounce:deb2 neg_r	pll0 altpll_0 sd1 pll7 clk[0]
35	80.792	Debounce:deb2 counter_r[2]	Debounce:deb2 neg_r	pll0 altpll_0 sd1 pll7 clk[0]
36	80.883	Debounce:deb2 counter_r[1]	Debounce:deb2 neg_r	pll0 altpll_0 sd1 pll7 clk[0]
37	81.021	Top:top0 state_r_S_IDLE	Top:top0 state_r_S_IDLE	pll0 altpll_0 sd1 pll7 clk[0]
38	81.023	Top:top0 state_r_S_IDLE	Top:top0 state_r_S_REC'D	pll0 altpll_0 sd1 pll7 clk[0]

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Setup: 'pll0|altpll_0|sd1|pll7|clk[1]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[0]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[1]'

Hold: 'AUD_BCLK'

Minimum Pulse Width: 'CLOCK_50'

Minimum Pulse Width: 'CLOCK2_50'

Minimum Pulse Width: 'CLOCK3_50'

Minimum Pulse Width: 'AUD_BCLK'

Minimum Pulse Width: 'pll0|altpll_0|sc'

Minimum Pulse Width: 'pll0|altpll_0|sc'

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	Clock	Slack	End Point TNS
1	AUD_BCLK	-22.224	-480.686
2	pll0 altpll_0 sd1 pll7 clk[0]	-3.037	-11.363
3	pll0 altpll_0 sd1 pll7 clk[1]	81.888	0.000

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Setup: 'pll0|altpll_0|sd1|pll7|clk[1]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[0]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[1]'

Hold: 'AUD_BCLK'

Minimum Pulse Width: 'CLOCK_50'

Minimum Pulse Width: 'CLOCK2_50'

Minimum Pulse Width: 'CLOCK3_50'

Minimum Pulse Width: 'AUD_BCLK'

Minimum Pulse Width: 'pll0|altpll_0|sd1|pll7|clk[0]'

Minimum Pulse Width: 'pll0|altpll_0|sd1|pll7|clk[1]'

Setup: 'AUD_BCLK'

Setup: 'pll0|altpll_0|sd1|pll7|clk[0]'

Setup: 'pll0|altpll_0|sd1|pll7|clk[1]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[0]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[1]'

Hold: 'AUD_BCLK'

Slack

From Node

To Node

1

-22.224

Top:top0|state_r_s_PLAY

Top:top0|AudPlayer:player0|diff_r[14]

pll0

2

-22.096

Top:top0|state_r_s_PLAY

Top:top0|AudPlayer:player0|diff_r[15]

pll0

3

-22.017

Top:top0|state_r_s_PLAY

Top:top0|AudPlayer:player0|diff_r[16]

pll0

4

-22.016

Top:top0|state_r_s_PLAY

Top:top0|AudPlayer:player0|diff_r[5]

pll0

5

-21.960

Top:top0|state_r_s_PLAY

Top:top0|AudPlayer:player0|diff_r[13]

pll0

6

-21.898

Top:top0|state_r_s_PLAY

Top:top0|AudPlayer:player0|diff_r[7]

pll0

7

-21.889

Top:top0|state_r_s_PLAY

Top:top0|AudPlayer:player0|diff_r[11]

pll0

8

-21.874

Top:top0|state_r_s_PLAY

Top:top0|AudPlayer:player0|diff_r[12]

pll0

9

-21.861

Top:top0|state_r_s_PLAY

Top:top0|AudPlayer:player0|diff_r[8]

pll0

10

-21.847

Top:top0|state_r_s_PLAY

Top:top0|AudPlayer:player0|diff_r[4]

pll0

11

-21.847

Top:top0|state_r_s_PLAY

Top:top0|AudPlayer:player0|diff_r[9]

pll0

12

-21.814

Top:top0|state_r_s_PLAY

Top:top0|AudPlayer:player0|diff_r[10]

pll0

13

-21.780

Top:top0|state_r_s_PLAY

Top:top0|AudPlayer:player0|diff_r[3]

pll0

14

-21.762

Top:top0|state_r_s_PLAY

Top:top0|AudPlayer:player0|diff_r[6]

pll0

15

-21.746

Top:top0|state_r_s_PLAY

Top:top0|AudPlayer:player0|diff_r[1]

pll0

16

-21.666

Top:top0|state_r_s_PLAY

Top:top0|AudPlayer:player0|diff_r[2]

pll0

17

-21.402

Top:top0|state_r_s_PLAY

Top:top0|AudPlayer:player0|diff_r[0]

pll0

18

-2.349

Top:top0|five_dec_r[1]

FiveDecoder:dec1|seven_2nd_r[5]

pll0

19

-2.349

Top:top0|five_dec_r[1]

FiveDecoder:dec1|seven_2nd_r[6]

pll0

20

-2.348

Top:top0|five_dec_r[1]

FiveDecoder:dec1|seven_5th_r[1]

pll0

21

-2.288

Top:top0|five_dec_r[0]

FiveDecoder:dec1|seven_4th_r[6]

pll0

22

-2.274

Top:top0|five_dec_r[0]

FiveDecoder:dec1|seven_4th_r[3]

pll0

23

-2.271

Top:top0|five_dec_r[0]

FiveDecoder:dec1|seven_1st_r[3]

pll0

24

-2.269

Top:top0|five_dec_r[0]

FiveDecoder:dec1|seven_1st_r[4]

pll0

25

-2.269

Top:top0|five_dec_r[0]

FiveDecoder:dec1|seven_1st_r[5]

pll0

26

-2.269

Top:top0|five_dec_r[0]

FiveDecoder:dec1|seven_1st_r[6]

pll0

27

-2.268

Top:top0|five_dec_r[0]

FiveDecoder:dec1|seven_1st_r[0]

pll0

28

-2.258

Top:top0|five_dec_r[0]

FiveDecoder:dec1|seven_3rd_r[6]

pll0

29

-2.256

Top:top0|five_dec_r[0]

FiveDecoder:dec1|seven_2nd_r[1]

pll0

30

-2.230

Top:top0|five_dec_r[0]

FiveDecoder:dec1|seven_3rd_r[0]

pll0

31

-2.224

Top:top0|five_dec_r[0]

FiveDecoder:dec1|seven_3rd_r[3]

pll0

32

-2.206

Top:top0|five_dec_r[1]

FiveDecoder:dec1|seven_5th_r[2]

pll0

33

-2.201

Top:top0|five_dec_r[1]

FiveDecoder:dec1|seven_2nd_r[4]

pll0

34

-2.194

Top:top0|five_dec_r[0]

FiveDecoder:dec1|seven_5th_r[2]

pll0

35

-2.189

Top:top0|five_dec_r[0]

FiveDecoder:dec1|seven_2nd_r[4]

pll0

36

-2.177

Top:top0|five_dec_r[1]

FiveDecoder:dec1|seven_4th_r[5]

pll0

37

-2.177

Top:top0|five_dec_r[1]

FiveDecoder:dec1|seven_5th_r[0]

pll0

38

-2.176

Top:top0|five_dec_r[1]

FiveDecoder:dec1|seven_5th_r[4]

pll0

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Setup: 'pll0|altpll_0|sd1|pll7|clk[1]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[0]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[1]'

Hold: 'AUD_BCLK'

Minimum Pulse Width: 'CLOCK_50'

Minimum Pulse Width: 'CLOCK2_50'

Minimum Pulse Width: 'CLOCK3_50'

Minimum Pulse Width: 'AUD_BCLK'

Minimum Pulse Width: 'pll0|altpll_0|sd1|pll7|clk[0]'

Minimum Pulse Width: 'pll0|altpll_0|sd1|pll7|clk[1]'

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Setup: 'pll0|altpll_0|sd1|pll7|clk[0]'

Setup: 'pll0|altpll_0|sd1|pll7|clk[1]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[0]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[1]'

Hold: 'AUD_BCLK'

Fast 1200mV OC Model Setup: 'pll0|altpll_0|sd1|pll7|clk[0]'

	Slack	From Node	To Node	Launch Clock
1	-3.037	Top:top0 AudPlayer:player0 done_r	Top:top0 state_r_s_PLAY	AUD_BCLK
2	-2.844	Top:top0 AudPlayer:player0 done_r	Top:top0 state_r_s_IDLE	AUD_BCLK
3	-2.830	Top:top0 AudPlayer:player0 done_r	Top:top0 state_r_s_PLAY_PAUSE	AUD_BCLK
4	-2.681	Top:top0 AudRecorder:recorder0 done_r	Top:top0 state_r_s_IDLE	AUD_BCLK
5	-2.652	Top:top0 AudRecorder:recorder0 done_r	Top:top0 state_r_s_REC'D	AUD_BCLK
6	77.163	Top:top0 five_dec_r[1]	Top:top0 five_dec_r[1]	pll0 altpll_0 sd1 pll7 clk[0]
7	78.463	Top:top0 five_dec_r[0]	Top:top0 five_dec_r[0]	pll0 altpll_0 sd1 pll7 clk[0]
8	78.579	Debounce:deb1 neg_r	Top:top0 state_r_s_PLAY	pll0 altpll_0 sd1 pll7 clk[0]
9	78.787	Top:top0 state_r_s_REC'D	Top:top0 five_dec_r[1]	pll0 altpll_0 sd1 pll7 clk[0]
10	79.047	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 five_dec_r[1]	pll0 altpll_0 sd1 pll7 clk[0]
11	79.133	Top:top0 state_r_s_I2C	Top:top0 five_dec_r[1]	pll0 altpll_0 sd1 pll7 clk[0]
12	79.681	Top:top0 state_r_s_PLAY	Top:top0 five_dec_r[0]	pll0 altpll_0 sd1 pll7 clk[0]
13	80.222	Debounce:deb1 neg_r	Top:top0 state_r_s_IDLE	pll0 altpll_0 sd1 pll7 clk[0]
14	80.294	Debounce:deb1 neg_r	Top:top0 state_r_s_REC'D	pll0 altpll_0 sd1 pll7 clk[0]
15	80.319	Top:top0 state_r_s_IDLE	Top:top0 state_r_s_PLAY	pll0 altpll_0 sd1 pll7 clk[0]
16	80.606	Debounce:deb2 neg_r	Top:top0 state_r_s_PLAY	pll0 altpll_0 sd1 pll7 clk[0]
17	80.823	Top:top0 state_r_s_PLAY	Top:top0 PLAYER_start_r	pll0 altpll_0 sd1 pll7 clk[0]
18	80.835	Top:top0 state_r_s_PLAY	Top:top0 state_r_s_PLAY	pll0 altpll_0 sd1 pll7 clk[0]
19	80.887	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 state_r_s_PLAY	pll0 altpll_0 sd1 pll7 clk[0]
20	81.066	Top:top0 state_r_s_PLAY	Top:top0 state_r_s_IDLE	pll0 altpll_0 sd1 pll7 clk[0]
21	81.112	Top:top0 state_r_s_PLAY_PAUSE	Top:top0 five_dec_r[0]	pll0 altpll_0 sd1 pll7 clk[0]
22	81.129	Top:top0 state_r_s_I2C	Top:top0 five_dec_r[0]	pll0 altpll_0 sd1 pll7 clk[0]
23	81.260	Top:top0 state_r_s_PLAY	Top:top0 state_r_s_PLAY_PAUSE	pll0 altpll_0 sd1 pll7 clk[0]
24	81.432	Top:top0 state_r_s_PLAY	Top:top0 led_r_r[1]	pll0 altpll_0 sd1 pll7 clk[0]
25	81.434	Top:top0 state_r_s_PLAY	Top:top0 led_r_r[0]	pll0 altpll_0 sd1 pll7 clk[0]
26	81.471	Debounce:deb0 neg_r	Top:top0 state_r_s_PLAY	pll0 altpll_0 sd1 pll7 clk[0]
27	81.635	Debounce:deb0 neg_r	Top:top0 state_r_s_REC'D	pll0 altpll_0 sd1 pll7 clk[0]
28	81.644	Debounce:deb0 neg_r	Top:top0 state_r_s_I2C	pll0 altpll_0 sd1 pll7 clk[0]
29	81.755	Debounce:deb0 neg_r	Top:top0 state_r_s_IDLE	pll0 altpll_0 sd1 pll7 clk[0]
30	81.756	Debounce:deb0 neg_r	Top:top0 state_r_s_PLAY_PAUSE	pll0 altpll_0 sd1 pll7 clk[0]
31	81.837	Debounce:deb2 neg_r	Top:top0 state_r_s_IDLE	pll0 altpll_0 sd1 pll7 clk[0]
32	81.851	Top:top0 state_r_s_REC'D	Top:top0 state_r_s_IDLE	pll0 altpll_0 sd1 pll7 clk[0]
33	81.893	Top:top0 PLAYER_start_r	Top:top0 PLAYER_start_r	pll0 altpll_0 sd1 pll7 clk[0]
34	81.979	Debounce:deb2 counter_r[0]	Debounce:deb2 neg_r	pll0 altpll_0 sd1 pll7 clk[0]
35	81.992	Debounce:deb2 counter_r[2]	Debounce:deb2 neg_r	pll0 altpll_0 sd1 pll7 clk[0]
36	82.040	Debounce:deb2 counter_r[1]	Debounce:deb2 neg_r	pll0 altpll_0 sd1 pll7 clk[0]
37	82.044	Top:top0 state_r_s_IDLE	Top:top0 state_r_s_IDLE	pll0 altpll_0 sd1 pll7 clk[0]
38	82.049	Top:top0 state_r_s_IDLE	Top:top0 state_r_s_REC'D	pll0 altpll_0 sd1 pll7 clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

pll0|altpll_0|sd1|pll7|clk[0]

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Setup: 'pll0|altpll_0|sd1|pll7|clk[1]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[0]'

Hold: 'pll0|altpll_0|sd1|pll7|clk[1]'

Hold: 'AUD_BCLK'

Minimum Pulse Width: 'CLOCK_50'

Minimum Pulse Width: 'CLOCK2_50'

Minimum Pulse Width: 'CLOCK3_50'

Minimum Pulse Width: 'AUD_BCLK'

Minimum Pulse Width: 'pll0|altpll_0|sc

Minimum Pulse Width: 'pll0|altpll_0|sc

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Multicorner Timing Analysis Summary

	Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
1	Worst-case Slack	-45.594	0.158	N/A	N/A	9.574
1	AUD_BCLK	-45.594	0.201	N/A	N/A	40.651
2	CLOCK2_50	N/A	N/A	N/A	N/A	16.000
3	CLOCK3_50	N/A	N/A	N/A	N/A	16.000
4	CLOCK_50	N/A	N/A	N/A	N/A	9.574
5	pll0 altpll_0 sd1 pll7 clk[0]	-5.896	0.158	N/A	N/A	41.372
6	pll0 altpll_0 sd1 pll7 clk[1]	80.603	0.184	N/A	N/A	4999.706
2	Design-wide TNS	-972.404	0.0	0.0	0.0	0.0
1	AUD_BCLK	-950.366	0.000	N/A	N/A	0.000
2	CLOCK2_50	N/A	N/A	N/A	N/A	0.000
3	CLOCK3_50	N/A	N/A	N/A	N/A	0.000
4	CLOCK_50	N/A	N/A	N/A	N/A	0.000
5	pll0 altpll_0 sd1 pll7 clk[0]	-22.038	0.000	N/A	N/A	0.000
6	pll0 altpll_0 sd1 pll7 clk[1]	0.000	0.000	N/A	N/A	0.000

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Unconstrained Paths

	Property	Setup	Hold
1	Illegal Clocks	0	0
2	Unconstrained Clocks	0	0
3	Unconstrained Input Ports	29	29
4	Unconstrained Input Port Paths	840	840
5	Unconstrained Output Ports	95	95
6	Unconstrained Output Port Paths	344	344