1.1 CSL Testbench Examples

FIGURE 1.1 Use on the PLI example

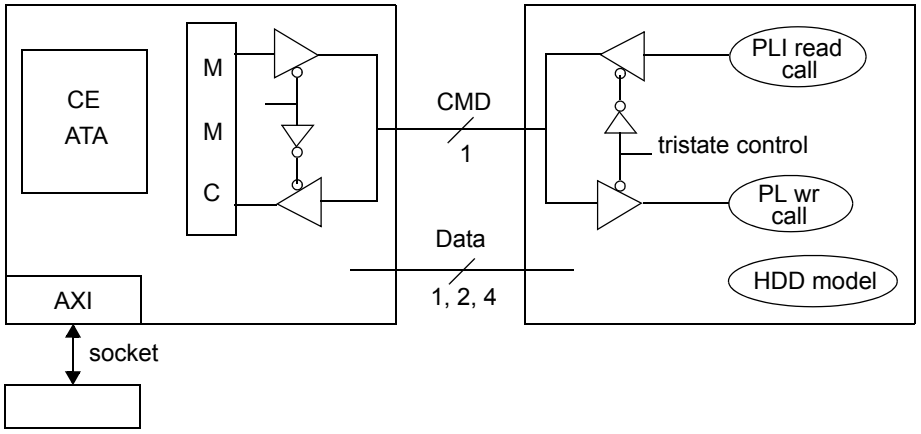
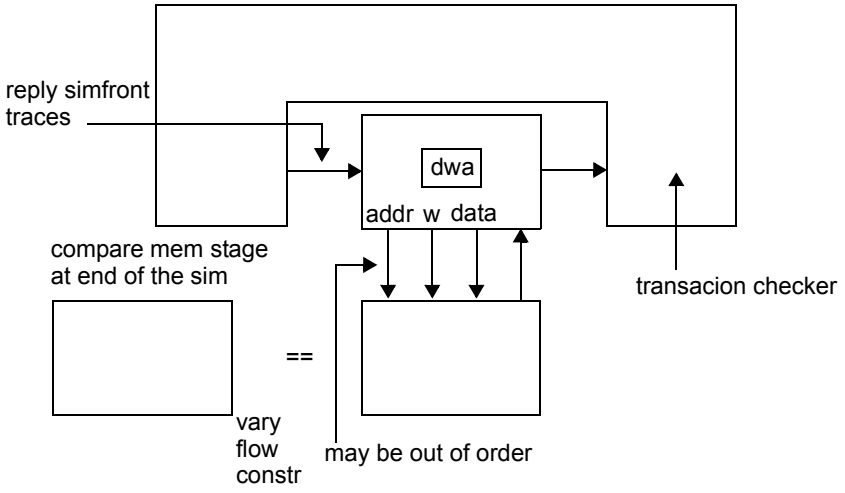


FIGURE 1.2



1.2 Testbench Command Summary

```
   vector_instance.set_instance_name(unit_instance);
add_logic(stall_generation, dut_inst_name);
```

1.3 Testbench commands

```
vector_instance.set_instance_name(unit_instance);
```

DESCRIPTION :

If you have 2 or more instances of the same DUT's in the same TestBench this command allows to associate multiple vector instances with the DUT's instances.This command is called only on a vector instance.

[***Testbench Command Summary***]

EXAMPLE :

CSL Code:

```
csl_unit d{
...
d(){}
...
};

csl_vector d_vec{
...
d_vec(){
set_module_name(d);
}
...
};

csl_unit tb{
...
d d0;
d d1;
d_vec d0_vec;
d_vec d1_vec;
...
tb(){
d0_vec.set_instance_name(d0);
d1_vec.set_instance_name(d1);
}
};
```

```
add_logic(stall_generation, dut_inst_name);
```

DESCRIPTION :

//

[***Testbench Command Summary***]

EXAMPLE :

//

CSL CODE

```
//
```

VERILOG CODE

```
//
```