Table 1.1 Categories

number	mnemonic	Phase description
1	cse	CSL errors
2	csw	CSL warnings
3	dee	Design errors
4	dew	Design warnings
5	ne	Numeric error
6	res	Reserved
7	ssm	Possible Simulation and synthesis mismatch
8	vee	Verilog errors
9	vew	Verilog warnings
10	vhe	VHDL errors
11	vhw	VHDL warnings

Table 1.2 Phases

number	mnemonic	Csl compiler category
1	cct	CSL to CDOM transformation
2	cda	CDOM analysis
3	cdc	CDOM creation
4	cde	CDOM elaboration
5	cg	code generation
6	csa	CSL analysis
7	csb	CSL elab
8	csc	CSL creation
9	csp	CSL parser
10	cst	CSL tree walker
11	prp	preprocessor
12	vep	Verilog parser
13	vet	Verilog tree walker
14	vhp	VHDL parser
15	vht	VHDL tree walker

Table 1.3 Error/warning type

number	mnemonic	error/warning type
1	ase	architectural state element
2	assn	assignment
3	blk	block
4	casn	continuous assign
5	ccd	csl compiler directive
6	ccs	csl clock specification
7	cdir	CSLC directive
8	chrs	charge strength
9	clk	clock
10	cmdl	command line
11	cmnt	comment
12	cmpl	component loop
13	comb	combinational logic
14	comp	component
15	cond	conditional
16	csi	case_item
17	css	case statement
18	cyb	cycle based
19	datl	data loop
20	decl	declaration
21	defd	define declaration
22	dely	delay statement
23	dir	directory
24	diss	disable statement
25	dmsn	dimension
26	drst	drive strength
27	drvc	driver contention
28	dsbl	disable
29	dsgn	design
30	evc	event control
31	expr	expression
32	file	file
33	forc	force
34	func	function
35	gate	gate
36	hid	hierarchy identifier
37	id	identifier
38	inhw	inference hardware
39	init	initialization
40	inst	instantiation
41	lib	library
42	list	list
43	loop	loop
44	mdb	multi driven bus
45	mdn	multi driven net
46	mem	memory
47	mifc	module instance

number	mnemonic	error/warning type
48	mins	module instantiation
49	mmod	macro module
50	mod	module
51	net	net
52	netd	net declaration
53	nett	net type
54	num	numeric
55	parm	parameter
56	pars	parser
57	pli	PLI table
58	port	port
59	pp	preprocessor
60	prim	primitive
61	proc	process
62	prts	part select
63	real	real
64	rel	release
65	rst	reset
66	scop	scope
67	sdir	synopsys compiler directive
68	seq	sequential
69	sig	signal
70	simr	simulation result
71	snsl	sensitivity list
72	spec	specify
73	sply	supply
74	stmt	statement
75	str	string
76	sysc	system call
77	syst	system task
78	task	task
79	tbcd	testbench code
80	time	time bit
81	topo	topologic
82	tri	tristate
83	trns	transistor
84	udir	unknown compiler directive
85	udp	udp
86	unsy	unsythesizable
87	vec	vec

Table 1.4 List of warning and error messages

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	cda	assn	unequal_length_lhs_rhs_cdcs	e					Unequal length LHS and RHS at line @
cse	cda	assn	unequal_length_lhs_rhs_off_one_bit_cdcs	e					Unequal length LHS and RHS off by one bit at line @
cse	cda	ccs	clkspec_clk_name_not_found	e					Clock specification @ clock name @ not found at line @
cse	cda	clk	merge_clk_phases_cdcd	e					Merge clock phases (clock A-phase) vs (clock B-phase) Path for (clock A-phase) at line @
cse	cda	clk	gated_clk_connected_to_clk_data_logic_cdcd	e					Gated clock @ is connected to both clock and data logic at line @
cse	cda	clk	clk_merge_with_data_signals_cdcd	e					Unable to continue trace of clock in clock tree which causes the clock to merge with the data signals at line @
cse	cda	clk	cannot_analyze_the_gated_clk_type_cdcd	e					Clock tree analysis can not analyze the gated clock type @ at line @
cse	cda	clk	cannot_find_the_clk_source_cdcd	e					Cannot find the clock source @ at line @
cse	cda	clk	clk_pin_not_driven_cdcd	e				x	Clock pin @pin is not driven by a clock tree through combinational gates (there must be combinational path from a clock source to @. The user must identify generated clocks by using a -cslc_gen_clk <clock_name>- directive the endpoint of generated clocks. The end point is the end point of the combinational path from a clock source to a combinational gate. at line @
cse	cda	clk	clk_net_from_seq_logic_driver_cdcd	e					Clock net @ derived from sequential logic driver

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									name @ at line @
cse	cda	clk	clk_port_from_seq_logic_driver_cdcd	e					Clock port @ derived from sequential logic driver name @ at line @
cse	cda	clk	clk_sig_from_seq_logic_driver_cdcd	e					Clock signal @ derived from sequential logic driver name @ at line @
cse	cda	clk	merge_clk_data_logic_same_gate_cdcd	e					Merged clock and data logic. A gate is connected to both a clock signal and a data signal. Clock and data signals cannot be connected to the same combinational gate. Do you need to use a gated clock directive to specify a gated clock? End point @ at line @
cse	cda	clk	mux_output_used_as_clk_cdcd	e					Mux output is used as a clock. Either the mux select or al of the mux inputs must be driven by a gated clock at line @
cse	cda	clk	generated_clk_is_selfclked_cdcd	e					Generated clock @ is self -clocked. at line @
cse	cda	clk	comb_logic_loop_in_clk_tree_cdcd	e					Combinational logic loop in clock tree start point @ at line @
cse	cda	clk	clk_enable_is_a_generated_clk_cdcd	e					Clock enable @ is a generated clock @ at line @
cse	cda	clk	generated_clk_has_more_than_one_drive_cdcd	e					Generated clock @ has more than one driver at line @
cse	cda	clk	found_unsupp_gated_clk_cdcd	e					Clock glitch design rule checking found the following unsupported gated clock logic type @ at line @
cse	cda	clk	unsupp_logic_operation_cdcs	w					Unsupported logic operation type @. at line @
cse	cda	clk	unsupp_cl_gated_logic_cdcs	w					Unsupported gated clock logic type. at line @
cse	cda	csi	noncnst_in_iclude_file_cdcs	e					Non-constant in include file @ at line @
cse	cda	datl	comb_logic_loop_in_data_logic_cdcd	e					Combinational logic loop in data logic at line @
cse	cda	datl	comb_logic_loop_in_data_logic_latch_cdcd	e					Combinational logic loop in data logic with Latch Buffer at line @
cse	cda	datl	find_comb_loop_cdcd	e					Component loop A combinational loop was detected which involves a split vector which is part of a combinational loop. Starting point @ at line @
cse	cda	datl	comp_loop_detected_cdcd	e					Component loop detected @ starting point @ at line @
cse	cda	datl	irregular_latch_in_comp_loop_cdcd	e					Irregular latch in component loop. An irregular latch is a latch that can be open continuously for the entire cycle. One latch in the loop must be closed at some point during the clock cycle. starting point @ at line @
cse	cda	drvc	multiply_drvn_net_nontri_gate_cdcs	w					Multiply drivenNet driven by a non-tristate gate at line @
cse	cda	drvc	multiply_drvn_port_nontri_gate_cdcs	w					Multiply drivenPort driven by a non-tristate gate at line @
cse	cda	drvc	multiply_drvn_sig_nontri_gate_cdcs	w					Multiply drivenSignal driven by a non-tristate gate at line @
cse	cda	drvc	incompatible_driver_net_cdcs	w					Incompatible driver of type @ drivingNet_@ multi drivenNet of type @ name @ at line @
cse	cda	drvc	incompatible_driver_port_cdcs	w					Incompatible driver of type @ drivingPort_@ multi drivenPort of type @ name @ at line @
cse	cda	drvc	incompatible_driver_sig_cdcs	w					Incompatible driver of type @ drivingSignal_@

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									multi drivenSignal of type @ name @ at line @
cse	cda	expr	unary_op_in_comparison_cdcs	e					Unary op used in comparison at line @
cse	cda	expr	miss_parenthesis_cdcs	e					Unary op @ with comparison op @ missing precedence parenthesis at line @
cse	cda	init	assn_mem_in_init_blk_cdcs	e					Assign memory in initial block at line @
cse	cda	inst	input_port_drvn_from_inside_mod_cdcs	e					Input port @ being driven from inside of module @ at line @
cse	cda	inst	input_port_drvn_from_inside_entity_cdcs	e					Input port @ being driven from inside of entity @ at line @
cse	cda	inst	input_port_drvn_from_inside_signal_cdcs	e					Input port @ being driven from inside of signal @ at line @
cse	cda	inst	input_port_not_connected_in_parent_mod_cdcs	e					Input port @ not connected in parent module at line @
cse	cda	inst	input_port_not_connected_in_parent_entity_cdcs	e					Input port @ not connected in parent entity at line @
cse	cda	inst	input_port_not_connected_in_parent_signal_cdcs	e					Input port @ not connected in parent signal at line @
cse	cda	mdb	single_comp_contains_multiple_tri_drv_cdcs	w					A single component contains multiple tristate drivers at line @
cse	cda	mdb	unsuppexpr_on_lhs_net_drv_stmt_cdcs	w					Unsupported Expression type type on LHS ofNet driver statement at line @
cse	cda	mdb	unsuppexpr_on_lhs_port_drv_stmt_cdcs	w					Unsupported Expression type type on LHS ofPort driver statement at line @
cse	cda	mdb	unsuppexpr_on_lhs_sig_drv_stmt_cdcs	w					Unsupported Expression type type on LHS ofSignal driver statement at line @
cse	cda	mdb	tri_not_in_top_mod_cdcs	e					Tristate not in top module at line @
cse	cda	mdb	tri_not_in_top_ent_cdcs	e					Tristate not in top entity at line @
cse	cda	mdb	tri_not_in_top_sig_cdcs	e					Tristate not in top signal at line @
cse	cda	mdb	tri_primitive_inst_cdcs	e					Tristate primitive instantiation at line @
cse	cda	mdb	tri_net_only_one_drvr_cdcs	e					Tri Net has only one driver at line @
cse	cda	mdb	tri_port_only_one_drvr_cdcs	e					Tri Port has only one driver at line @
cse	cda	mdb	tri_sig_only_one_drvr_cdcs	e					Tri Signal has only one driver at line @
cse	cda	mod	redef_mod_cdcs	e					Redefined module @ at line @
cse	cda	mod	redef_ent_cdcs	e					Redefined entity @ at line @
cse	cda	mod	redef_signal_cdcs	e					Redefined signal @ at line @
cse	cda	net	tri_and_net_only_one_driver_cdcs	e	?				triandNet @ has only one driver at line @
cse	cda	net	tri_and_port_only_one_driver_cdcs	e	?				triandPort @ has only one driver at line @
cse	cda	net	tri_and_sig_only_one_driver_cdcs	e	?				triandSignal @ has only one driver at line @
cse	cda	net	var_assn_but_never_ref_cdcs	e					Variable @ assigned but never referenced at line @
cse	cda	net	var_never_assn_cdcs	e					Variable @ never assigned at line @
cse	cda	net	var_not_assn_in_all_paths_cdcs	e					Variable @ not being assigned in all paths at line @
cse	cda	net	var_not_in_snsl_cdcs	e					Variable @ not in sensitivity list at line @
cse	cda	net	reg_connected_to_inout_in_inst_cdcs	e					Reg @ connected to inout @ in instantiation @ at line @
cse	cda	net	reg_connectede_to_output_in_inst_cdcs	e					Reg @ connected to output in instantiation at line @
cse	cda	net	reg_used_as_output_of_cont_assn_cdsc	e					Reg @ used as output of continuous assign at line @
cse	cda	net	port_used_prior_to_decl_cdcs	e					Port @ used prior toDeclaration at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	cda	parm	redef_param_cdcs	e					Redefined parameter @ at line @
cse	cda	pp	redef_macro_cdcs	e					Redefined macro @ at line @
cse	cda	prts	vec_index_order_incorrect_cdcs	e					Vector index @ order incorrect at line @
cse	cda	prts	vec_index_truncated_cdcs	e					Vector index @ truncated at line @
cse	cda	seq	seq_latch_connected_to_latch_in_loop_cdcd	e					Latch connected to latch in loop at line @
cse	cda	sply	output_conncet_to_sply_	e					Output @ connect to supply at line @
cse	cda	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_cdcs	e					Arithmetic operator RHS has one less bit than the LHS at line @
cse	cda	stmt	ar_op_unequal_lhs_rhs_cdsc	e					Arithmetic operator unequal width LHS and RHS at line @
cse	cda	stmt	ar_op_unequal_var_on_rhs_cdcs	e					Arithmetic operator unequal width variables @ on RHS at line @
cse	cda	tri	tri_not_in_top_mod_cdcs	e					Tristate @ not in top module at line @
cse	cda	tri	tri_not_in_top_entity_cdcs	e					Tristate @ not in top entity at line @
cse	cda	tri	tri_not_in_top_signal_cdcs	e					Tristate @ not in top signal at line @
cse	cda	tri	tri_prim_ist_cdsc	e					Tristate primitive instantiation @ at line @
cse	cdc	ase	arch_state_el_mod_not_exist_cdccs	e					Architectural state element @ module @ does not exist at line @
cse	cdc	ase	arch_state_el_ent_not_exist_cdccs	e					Architectural state element @ entity @ does not exist at line @
cse	cdc	ase	arch_state_el_unit_not_exist_cdcvs	e					Architectural state element @ unit @ does not exist at line @ at line @
cse	cdc	ase	arch_state_el_missi_clk_name_cdccs	e					Architectural state element @ is missing the clock name at line @
cse	cdc	ase	arch_state_el_miss_mem_name_cdccs	e					Architectural state element @ is missing the memory name at line @
cse	cdc	ase	arch_state_el_miss_the_cdccs	e					Architectural state element @ is missing the @ at line @
cse	cdc	ase	arch_state_el_miss_rst_name_cdccs	e					Architectural state element @ is missing the reset name at line @
cse	cdc	ase	arch_state_el_evtrigg_miss_ev_name_cdcsc	e					Architectural state element @ is event triggered and is missing the event name at line @
cse	cdc	ase	arch_state_el_clk_name_not_found_cdccs	e					Architectural state element @ clock name @ not found at line @
cse	cdc	ase	arch_state_el_mem_name_not_found_cdccs	e					Architectural state element @ memory name @ not found at line @
cse	cdc	ase	arch_state_el_not_found_cdcs	e					Architectural state element @ arch_state_name @ not found at line @
cse	cdc	assn	x_in_rhs_of_assihnment_cdccs	e					x in rhs of assignment at line @
cse	cdc	assn	z_in_rhs_of_assn_default_csi_cdccs	e					x in rhs of assignement in defaultCase item at line @
cse	cdc	assn	z_in_rhs_of_assn_cdccs	e					z in rhs of assignement at line @
cse	cdc	assn	unequal_length_lhs_rhs_cdccs	e					Unequal length LHS and RHS at line @
cse	cdc	assn	unequal_length_lhs_rhs_off_one_bit_cdccs	e					Unequal length LHS and RHS off by one bit at line @
cse	cdc	ccd	ccd_cdir_must_be_cst_expr_cdccs	e				x	CSL directive size must be constant Expression at line @
cse	cdc	ccd	clk_dir_not_applied_to_dsgn_cdccs	w				x	CSL clock directive not applied to design. Could not find clock at line @
cse	cdc	ccd	csl_filter_unused_cdccs	w				x	CSL message filter @ not found. Filter @ is unused. at line @
cse	cdc	ccd	csl_mess_not_filtered_cdccs	w				x	CSL message @ can not be filtered. Filter @ is unused. at line @
cse	cdc	ccd	error_csdir_not_found_cdccs	e				x	Error CSL directive @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									not found. Error @ is unused. at line @
cse	cdc	chrs	ill_val_chrs_cdc	e					Illegal value @ at line @
cse	cdc	clk	clk_name_not_found_cdir_cdccs	e				x	Clock name not found in cslc directive at line @
cse	cdc	clk	expr_sunj_to_different_clk_phases_cdccs	e					Expression subject to different clock phases at line @
cse	cdc	csi	z_csi_not_in_casez_cdc	e					z case item not in casez at line @
cse	cdc	csi	noncstn_rep_in_conc_cdccs	e					Non-constant repeator in concatenation at line @
cse	cdc	decl	decl_array_over_max_size_cdccs	e					Array @ exceeds maximum size limit at line @
cse	cdc	dely	x_or_z_in_dely_cdccs	e					x or z in delay at line @
cse	cdc	dmsn	mem_prts_index_out_of_range_for_mem_cdccs	e					Memory part select [@:@] index @ out range for memory @ at line @
cse	cdc	dmsn	dime_select_for_mem_missing_cdccs	e					Select for memory @ missing at line @
cse	cdc	dmsn	dime_index_out_of_bounds_for_mem_cdccs	e					Index <index> out of bounds for memory @. Range [@: @] at line @
cse	cdc	dmsn	dime_prts_out_of_bounds_for_net_cdccs	e					Part select [@ : @] out of bounds for net @. Range [@ : @] at line @
cse	cdc	dmsn	dime_prts_out_of_bounds_for_port_cdccs	e					Part select [@ : @] out of bounds for port @. Range [@ : @] at line @
cse	cdc	dmsn	dime_prts_out_of_bounds_for_sig_cdccs	e					Part select [@ : @] out of bounds for signal @. Range [@ : @] at line @
cse	cdc	dmsn	dime_prts_reg_cdccs	e					Part select [@ : @] reg @. Range [@ : @] at line @
cse	cdc	drvc	incompatible_drvc_for_net_cdccs	e					Incompatible drivers for Net @ at line @
cse	cdc	drvc	incompatible_drvc_for_port_cdccs	e					Incompatible drivers for Port @ at line @
cse	cdc	drvc	incompatible_drvc_for_sig_cdccs	e					Incompatible drivers for Signal @ at line @
cse	cdc	drvc	drvc_multiple_drive_net_partially_overlap_cdccs	e					Multiple drive Net partially overlap at line @
cse	cdc	drvc	drvc_multiple_drive_port_partially_overlap_cdccs	e					Multiple drive Port partially overlap at line @
cse	cdc	drvc	drvc_multiple_drive_sig_partially_overlap_cdccs	e					Multiple drive Signal partially overlap at line @
cse	cdc	dsgn	dsgn_top_mod_cannot_id_cdccs	e					Top module @ cannot be identified at line @
cse	cdc	dsgn	dsgn_top_entity_cannot_id_cdccs	e					Top entity @ cannot be identified at line @
cse	cdc	dsgn	dsgn_top_unit_cannot_id_cdccs	e					Top unit @ cannot be identified at line @
cse	cdc	dsgn	unit_dsgn_cycle_not_spanning_tree_cdccs	e					Unit design hierarchy contains a cycle. Hierarchy is not a spanning tree. at line @
cse	cdc	expr	expr_prts_indices_1bit_var_cdccs	e					Part select indices 1-bit variable at line @
cse	cdc	expr	expr_prts_must_be_cst_expr_cdccs	e					Part select specifier Expression must be constant Expression at line @
cse	cdc	expr	not_const_expr_cdcsc	e					Repetition multiplier in concatenation is not a constant Expression at line @
cse	cdc	expr	ill_bit_select_expr_cdccs	e					Illegal bit select expression @ at line @
cse	cdc	expr	repetition_multiplier_in_conc_not_const_expr_cdccs	w					Repetition multiplier in concatenation is not a constant Expression at line @
cse	cdc	expr	int_operand_not_1_bit_cdccs	w					Logic operator has integer operands instead of 1-bit operands at line @
cse	cdc	expr	unsupp_expr_cdccs	w					Unsupported Expression type @ at line @
cse	cdc	expr	unsupp_operator_cdccs	w					Unsupported operator type @ at line @
cse	cdc	expr	use_of_sg_bit_const_cdccs	w					Use of single bit constant at line @
cse	cdc	expr	unary_op_in_comparison_cdccs	e					Unary op used in comparison at line @
cse	cdc	expr	x_or_z_in_cond_expr_cdccs	e					x or z in conditional expression at line @
cse	cdc	expr	zero_in_rep_in_conc_cdccs	e					Zero repeator in

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									concatenation at line @
cse	cdc	expr	expr_in_mod_port_dir_cdccs	e					Expression @ in module port dir at line @
cse	cdc	expr	expr_in_ent_port_dir_cdccs	e					Expression @ in entity port dir at line @
cse	cdc	expr	expr_in_sig_port_dir_cdccs	e					Expression @ in unit port dir at line @
cse	cdc	expr	expr_in_inst_cdccs	e					Expression @ in inst i@ at line @
cse	cdc	expr	expr_operator_operands_unequal_lenght_cdccs	e					Expression operator @ operands @ unequal length at line @
cse	cdc	file	cannot_open_filter_specification_file_cdccs	e					Cannot open filter specification file @ at line @
cse	cdc	file	filter_specification_file_missing_cdccs	e					Filter specification file name @ is missing at line @
cse	cdc	file	mismatch_mod_file_name_cdccs	e					Mismatch between module name @ and file name @ at line @
cse	cdc	file	mismatch_ent_file_name_cdccs	e					Mismatch between entity name @ and file name @ at line @
cse	cdc	file	mismatch_sig_file_name_cdccs	e					Mismatch between signal name @ and file name @ at line @
cse	cdc	func	port_not_output_func_cdccs	e					Port @ direction cannot be output at line @
cse	cdc	func	too_many_arg_to_func_cdccs	e					Too many arguments passed to function @ at line @
cse	cdc	func	too_few_arg_to_func_cdccs	e					Too few arguments passed to function @ at line @
cse	cdc	func	undefined_func_cdccs	e					Undefined function @ at line @
cse	cdc	func	funct_expr_cannot_expnaded_cdccs	e					Function expression @ cannot be expanded at line @
cse	cdc	func	funct_not_used_in_expr_cdccs	w					Function @ is not being used in an Expression at line @
cse	cdc	func	func_decl_cdccs	w					Function Declaration @ already declared as another type at line @
cse	cdc	hid	cannot_locate_hier_id_hid_cdccs	e					Can't locate hierarchical identifier @ at line @
cse	cdc	hid	ref_minst_found_in_expr_hid_cdccs	e					References a module instance @ found in an Expression hid at line @
cse	cdc	hid	ref_entity_found_in_expr_hid_cdccs	e					References a entity instance @ found in an Expression hid at line @
cse	cdc	hid	ref_unit_found_in_expr_hid_cdccs	e					References a unit instance @ found in an Expression hid at line @
cse	cdc	hid	hid_reference_not_found_cdccs	e					@ reference not found at line @
cse	cdc	hid	mifc_in_hid_not_exist_cdccs	e					Module instance @ in hid does not exist at line @
cse	cdc	hid	entity_instance_in_hid_not_exist_cdccs	e					Entity instance @ in hid does not exist at line @
cse	cdc	hid	unit_instance_in_hid_not_exist_cdccs	e					Unit instance @ in hid does not exist at line @
cse	cdc	hid	mod_found_in_path_in_dsgn_cdccs	e					Module @ found in path @ in the design at line @
cse	cdc	hid	enity_found_in_path_in_dsgn_cdccs	e					Entity @ found in path @ in the design at line @
cse	cdc	hid	unit_found_in_path_in_dsgn_cdccs	e					Unit @ found in path @ in the design at line @
cse	cdc	hid	hierarchical_id_path_contains_func_cdc	e					Hierarchical ID @ path contains a function at line @
cse	cdc	init	assn_mem_in_init_blk_cdccs	e					Assign memory in initial block at line @
cse	cdc	inst	inst_duplicate_mod_name_cdccs	e					Duplicate port @ in the port list for module @ at line @
cse	cdc	inst	inst_duplicate_entity_name_cdccs	e					Duplicate port @ in the port list for entity @ at line @
cse	cdc	inst	inst_duplicate_unit_name_cdccs	e					Duplicate port @ in the port list for unit @ at line @
cse	cdc	inst	ill_mod_inst_name_cdccs	e					Illegal module instance @ at line @
cse	cdc	inst	ill_entity_inst_name_cdccs	e					Illegal entity instance @ at line @
cse	cdc	inst	ill_unit_inst_name_cdccs	e					Illegal unit instance @ at

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									line @
cse	cdc	inst	inst_name_defined_mod_cdcc	e					Instance name @ already defined in this module at line @
cse	cdc	inst	inst_name_defined_ent_cdcc	e					Instance name @ already defined in this entity at line @
cse	cdc	inst	inst_name_defined_unit_cdcc	e					Instance name @ already defined in this unit at line @
cse	cdc	inst	inst_too_many_bits_cdccs	e					Too many bits for port @ of instance array @, formal @, actual @ at line @
cse	cdc	inst	inst_port_not_connected_var_cdccs	e					Port 'port' of instance array 'array' is not connected to variable at line @
cse	cdc	inst	inst_insufficient_bits_cdccs	e					Insufficient bits for port 'port' of instance array 'array ', formal number, actual number at line @
cse	cdc	inst	inst_mod_name_not_defined_cdccs	e					Module name not defined at line @
cse	cdc	inst	inst_ent_name_not_defined_cdccs	e					Entity name not defined at line @
cse	cdc	inst	inst_unit_name_not_defined_cdccs	e					Unit name not defined at line @
cse	cdc	inst	many_mod_inst_param_assign_cdccs	e					Too many module instance parameter assignments (number > rrumber) at line @
cse	cdc	inst	many_entity_inst_param_assign_cdccs	e					Too many entity instance parameter assignments (number > rrumber) at line @
cse	cdc	inst	many_unit_inst_param_assign_cdccs	e					Too many unit instance parameter assignments (number > rrumber) at line @
cse	cdc	inst	complexexpr_cannot_mapped_inout_port_cdccs	e					Complex Expression @ cannot be mapped to inout port @ at line @
cse	cdc	inst	complexexpr_cannot_mapped_unknown_port_cdccs	e					Complex Expression @ cannot be mapped to unknown type port @ at line @
cse	cdc	inst	netdecl_contains_ill_prts_cdccs	e					Net Declaration [@: @] contains an illegal part select at line @
cse	cdc	inst	regdecl_contains_ill_prts_cdccs	e					Reg Declaration [@ : @] contains an illegal part select at line @
cse	cdc	inst	complex_expr_inst_parent_module_cdccs	e					Complex actual Expression associated with port @ of module @ instantiated in parent module at line @
cse	cdc	inst	complex_expr_inst_entity_parent_module_cdccs	e					Complex actual Expression associated with port @ of entity @ instantiated in parent module at line @
cse	cdc	inst	complex_expr_inst_unit_parent_module_cdccs	e					Complex actual Expression associated with port @ of unit @ instantiated in parent module at line @
cse	cdc	inst	inst_mod_output_port_width_cdccs	e					Mod @ Output port @ width mismatch, actual-width (port-width) at line @
cse	cdc	inst	inst_entity_output_port_width_cdccs	e					Entity @ Output port @ width mismatch, actual-width (port-width) at line @
cse	cdc	inst	inst_unit_output_port_width_cdccs	e					Unit @ Output port @ width mismatch, actual-width (port-width) at line @
cse	cdc	inst	inst_mod_input_port_width_cdccs	e					Mod @ Input port @ width mismatch, actual-width (port-width) at line @
cse	cdc	inst	inst_entity_input_port_width_cdccs	e					Entity @ Input port @ width mismatch, actual-width (port-width) at line @
cse	cdc	inst	inst_unit_input_port_width_cdccs	e					Unit @ Input port @ width mismatch, actual-width (port-width)

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									at line @
cse	cdc	inst	inst_mod_not_define_cdccs	e					Module not defined at line @
cse	cdc	inst	inst_entity_not_define_cdccs	e					Entity not defined at line @
cse	cdc	inst	inst_unit_not_define_cdccs	e					Unit not defined at line @
cse	cdc	inst	mifc_port_actual_formal_width_mismatch_cdccs	w					Module @ instance @ port @ width mismatch, actual width @ formal width @ at line @
cse	cdc	inst	ent_port_actual_formal_width_mismatch_cdccs	w					Entity @ instance @ port @ width mismatch, actual width @ formal width @ at line @
cse	cdc	inst	unit_port_actual_formal_width_mismatch_cdccs	w					Unit @ instance @ port @ width mismatch, actual width @ formal width @ at line @
cse	cdc	inst	inst_differs_in_case_from_mod_cdccs	e					Instance name @ differs in case from module name @ at line @
cse	cdc	inst	inst_differs_in_case_from_ent_cdccs	e					Instance name @ differs in case from entity name @ at line @
cse	cdc	inst	inst_differs_in_case_from_sig_cdccs	e					Instance name @ differs in case from signal name @ at line @
cse	cdc	loop	undet_init_value_loop_cdccs	e					Unable to determine init value for loop at line @
cse	cdc	loop	undet_limit_loop_cdccs	e					Unable to determine limit for loop at line @
cse	cdc	loop	loop_bounds_calculated_int_cdccs	w					Loop bounds are calculated to be integer @, check that this is correct at line @
cse	cdc	loop	expr_lhs_contains_var_bit_select_cdccs	w					Expression in lhs of assignment contains a variable bit select at line @
cse	cdc	loop	loop_bounds_not_const_cdc	w					Loop bounds are non-constant at line @
cse	cdc	loop	loop_ctrl_init_expr_not_const_cdccs	w					Non-constant loop bound. Loop control variable initialization Expression is not a constant Expression at line @
cse	cdc	loop	loop_term_expr_not_const_cdccs	w					Non-constant loop bound. loop terminating Expression could not be evaluated to a constant at line @
cse	cdc	loop	init_expr_reset_by_var_cdccs	e					Non-constant loop bound. initializing Expression reset by variable at line @
cse	cdc	loop	loop_ctrl_var_1_bit_wide_cdccs	w					The loop control variable @ is one bit wide. Check the loop control variable Declaration. at line @
cse	cdc	mdb	bad_mdb_net_cdccs	e					Bad multi-driven Net @ at line @
cse	cdc	mdb	bad_mdb_port_cdccs	e					Bad multi-driven Port @ at line @
cse	cdc	mdb	bad_mdb_signal_cdccs	e					Bad multi-driven Signal @ at line @
cse	cdc	mdb	unsupp_comp_mdb_net_cdccs	e	?				Unsupported component type @ driving in multi-driven Net name at line @
cse	cdc	mdb	unsupp_comp_mdb_port_cdccs	e	?				Unsupported component type @ driving in multi-driven Port name at line @
cse	cdc	mdb	unsupp_comp_mdb_signal_cdccs	e	?				Unsupported component type @ driving in multi-driven Signal name at line @
cse	cdc	mdb	unsupp_comp_drive_mdb_cdccs	e	?				Unsupported component type @ driving multi-driven Net natne at line @
cse	cdc	mdb	unsupp_comp_drive_mdb_port_cdccs	e	?				Unsupported component type @ driving multi-driven Port natne at line @
cse	cdc	mdb	unsupp_comp_drive_mdb_signal_cdccs	e	?				Unsupported component type @ driving multi-driven Signal natne at line @
cse	cdc	mdb	mdb_net_driven_by_trns_cdccs	e					Multiply driven Net driven

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									by transistor primitive type @ at line @
cse	cdc	mdb	mdb_port_driven_by_trns_cdccs	e					Multiply driven Port driven by transistor primitive type @ at line @
cse	cdc	mdb	mdb_sig_driven_by_trns_cdccs	e					Multiply driven Signal driven by transistor primitive type @ at line @
cse	cdc	mdb	mdb_unsupp_comp_drvs_net_cdccs	e					Unsupported component type driving Net drives Net connected to multi-driven Net at line @
cse	cdc	mdb	mdb_unsupp_comp_drvs_port_cdccs	e					Unsupported component type driving Port drives Port connected to multi-driven Port at line @
cse	cdc	mdb	mdb_unsupp_comp_drvs_sig_cdccs	e					Unsupported component type driving Signal drives Signal connected to multi-driven Signal at line @
cse	cdc	mdb	mdb_incompatible_net_drives_multiple_net_cdccs	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Net at line @
cse	cdc	mdb	mdb_incompatible_port_drives_multiple_port_cdccs	e					Incompatible driver driving tandem Port drives Port connected to multi-driven Port at line @
cse	cdc	mdb	mdb_incompatible_sig_drives_multiple_sig_cdccs	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Port at line @
cse	cdc	mdb	mdb_unsupp_LHS_concatenation_cdccs	e					Unsupported LHS concatenation in multi-drive 'device at line @
cse	cdc	mdb	mdb_bus_has_too_many_drivers_cdccs	e					Bus has too many drivers. at line @
cse	cdc	mdb	mdb_always_blk_drive_cdccs	w					Multiple always blocks drive name @ at line @
cse	cdc	mdb	nontri_gate_drives_mdb_net_cdccs	w					non-tri-state gate drives multi-driven Net at line @
cse	cdc	mdb	nontri_gate_drives_mdb_port_cdccs	w					non-tri-state gate drives multi-driven Port at line @
cse	cdc	mdb	nontri_gate_drives_mdb_sig_cdccs	w					non-tri-state gate drives multi-driven Signal at line @
cse	cdc	mem	mem_ref_without_index_cdccs	e					Memory @ referenced without index through hierarchical ID @ at line @
cse	cdc	mifc	port_identifier_mifc_cdccs	e					Port @ at line @
cse	cdc	mifc	mod_output_wire_redecl_reg_cdccs	e					Module @ output port re-declared as type reg after use as implicitly declared wire at line @
cse	cdc	mifc	entity_output_wire_redecl_reg_cdccs	e					Entity @ output port re-declared as type reg after use as implicitly declared wire at line @
cse	cdc	mifc	unit_output_wire_redecl_reg_cdccs	e					Unit @ output port re-declared as type reg after use as implicitly declared wire at line @
cse	cdc	mifc	output_port_is_mem_type_mifc_cdccs	e					Output port @ is memory type at line @
cse	cdc	mifc	mifc_inout_port_is_mem_type_cdccs	e					Inout port @ is memory type at line @
cse	cdc	mifc	mod_output_port_mismatch_actual_witdh_cdccs	w					Module @ output port @ formal to actual width mismatch at line @
cse	cdc	mifc	ent_output_port_mismatch_actual_witdh_cdccs	w					Entity @ output port @ formal to actual width mismatch at line @
cse	cdc	mifc	unit_output_port_mismatch_actual_witdh_cdc	w					Unit @ output port @ formal to actual width mismatch at line @
cse	cdc	mifc	port_name_different_in_upper_lower_case_cdccs	e					Port name @ different in upper lower case at line @
cse	cdc	mifc	port_not_def_in_iodecl_cdccs	e					Port @ not defined in ioDeclaration at line @
cse	cdc	mifc	port_not_def_in_portl_cdccs	e					Port @ not defined in port list at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	cdc	mifc	port_wiredecl_mismatch_cdccs	e					Port @ wireDeclaration mismatch at line @
cse	cdc	mifc	pos_based_null_inst_port_cdccs	e					Position based null instance port at line @
cse	cdc	mifc	last_portdecl_contains_trailcomma_cdccs	e					Last portDeclaration contains a trailing comma at line @
cse	cdc	mins	mins_expr_incompatible_type_cdccs	e					Expression @ has an incompatible argument type @ with the port at line @
cse	cdc	mins	mins_mod_not_exist_cdccs	e					Module @ does not exist at line @
cse	cdc	mins	mins_entity_not_exist_cdccs	e					Entity @ does not exist at line @
cse	cdc	mins	mins_unit_not_exist_cdccs	e					Unit @ does not exist at line @
cse	cdc	mod	dup_declar_name_mod_cdc	e					Duplicate Declaration of port @ at line @
cse	cdc	mod	ill_mod_name_cdccs	e					Illegal module @ at line @
cse	cdc	mod	ill_mod_entity_name_cddcs	e					Illegal entity @ at line @
cse	cdc	mod	ill_mod_unit_name_cdccs	e					Illegal unit @ at line @
cse	cdc	mod	mod_mult_decl_string_cdccs	e					Multiple Declarations of string detected in module @ at line @
cse	cdc	mod	mod_entity_mult_decl_string_cdccs	e					Multiple Declarations of string detected in entity @ at line @
cse	cdc	mod	mod_unit_mult_decl_string_cdccs	e					Multiple Declarations of string detected in unit @ at line @
cse	cdc	mod	mod_mult_def_cdcs	e					Module @ defined in multiple places at line @
cse	cdc	mod	mod_ent_mult_def_cdccs	e					Entity @ defined in multiple places at line @
cse	cdc	mod	mod_unit_mult_def_cdccs	e					Unit @ defined in multiple places at line @
cse	cdc	mod	mod_no_module_found_cdccs	e					No modules found at line @
cse	cdc	mod	mod_no_entity_found_cdccs	e					No entity found at line @
cse	cdc	mod	mod_no_unit_found_cdccs	e					No unit found at line @
cse	cdc	mod	failed_find_mod_cdccs	e					Failed to find module @ at line @
cse	cdc	mod	failed_find_entity_cdccs	e					Failed to find entity @ at line @
cse	cdc	mod	failed_find_unit_cdccs	e					Failed to find unit @ at line @
cse	cdc	mod	empty_mod_cdccs	e					Empty module at line @
cse	cdc	mod	empty_ent_cdccs	e					Empty entity at line @
cse	cdc	mod	empty_unit_cdccs	e					Empty unit at line @
cse	cdc	net	net_implicit_wire_redecl_reg_cdccs	e					Implicitly declared as a wire @ re-declared as a reg @. at line @
cse	cdc	net	undecl_net_in_mod_cdccs	e					Undeclared net @ in module @ at line @
cse	cdc	net	undecl_port_in_mod_cdccs	e					Undeclared port @ in module @ at line @
cse	cdc	net	undecl_sig_in_mod_cdccs	e					Undeclared signal @ in module @ at line @
cse	cdc	net	undecl_net_in_ent_cdccs	e					Undeclared net @ in entity @ at line @
cse	cdc	net	undecl_port_in_ent_cdccs	e					Undeclared port @ in entity @ at line @
cse	cdc	net	undecl_sig_in_ent_cdccs	e					Undeclared signal @ in entity @ at line @
cse	cdc	net	undecl_net_in_sig_cdccs	e					Undeclared net @ in signal @ at line @
cse	cdc	net	undecl_port_in_sig_cdccs	e					Undeclared port @ in signal @ at line @
cse	cdc	net	undecl_sig_in_sig_cdccs	e					Undeclared signal @ in signal @ at line @
cse	cdc	net	port_used_prior_to_decl_cdccs	e					Port @ used prior toDeclaration at line @
cse	cdc	net	1bit_with_prts_cdccs	e					1-bit with part select at line @
cse	cdc	netd	ill_decl_vec_cdccs	e					Illegal Declaration of vector @ at line @
cse	cdc	nett	nett_ill_reg_name_cdccs	e					Illegal register @ at line @
cse	cdc	nett	nett_ill_net_name_cdccs	e					Illegal net @ at line @
cse	cdc	nett	nett_ill_port_name_cdccs	e					Illegal port @ at line @
cse	cdc	nett	nett_ill_signal_name_cdccs	e					Illegal signal @ at line @
cse	cdc	nett	net_scalar_vect_nett_cdccs	e					Net declared as both scalar and vector at line @
cse	cdc	nett	port_scalar_vect_nett_cdccs	e					Port declared as both scalar and vector at line @
cse	cdc	nett	signal_scalar_vect_nett_cdccs	e					Signal declared as both

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									scalar and vector at line @
cse	cdc	nett	hot_mux_not_use_bus_connection_net_cdccs	e					One hot mux can not be used for bus connection between modules Net @ at line @
cse	cdc	nett	hot_mux_not_use_bus_connection_port_cdccs	e					One hot mux can not be used for bus connection between modules Port @ at line @
cse	cdc	nett	hot_mux_not_use_bus_connection_sig_cdccs	e					One hot mux can not be used for bus connection between modules Signal @ at line @
cse	cdc	num	not_allowed_width0_num_cdccs	e					Width 0 not allowed for sized number at line @
cse	cdc	num	real_num_not_allowed_cdccs	e					Real numbers not allowed at line @
cse	cdc	num	found_x_z_in_num_literal_cdccs	e					Found x and/or z value in number literal at line @
cse	cdc	num	too_many_digits_in_sized_num_cdccs	w					Number of digits exceeds the width in a sized number at line @
cse	cdc	num	divide_by_zero_num_cdccs	e					Divide by zero at line @
cse	cdc	num	child_mod_inst_parent_mod_cdccs	e					Child module @ instantiates parent module @ at line @
cse	cdc	num	child_ent_inst_parent_ent_cdccs	e					Child entity @ instantiates entity module @ at line @
cse	cdc	num	child_sig_inst_parent_sig_cdccs	e					Child signal @ instantiates signal module @ at line @
cse	cdc	num	int_decl_incorrect_cdccs	e					Integer Declaration incorrect at line @
cse	cdc	num	int_var_indexed_cdccs	e					Integer variable inedexed at line @
cse	cdc	parm	ill_parm_identifier_cdccs	e					Illegal parameter @ at line @
cse	cdc	parm	value_of_parm_OS_platform_dependent_cdccs	w					Parameter select width > 32. The value is OS and platform dependent at line @
cse	cdc	parm	parm_redefined_cdccs	w					Parameter @ redefined at line @
cse	cdc	port	ill_formal_port_name_cdccs	e					Illegal formal port @ at line @
cse	cdc	pp	text_redefined_replaced_cdccs	w					Text macro redefined and replaced @. Previous definition filename, line number @ New definition filename, line number @ at line @
cse	cdc	pp	endif_or_else_without_ifdef_cdccs	e					Endif-or-else-without ifdef at line @
cse	cdc	prim	z_in_prim_inst_cdccs	e					z in primitive instantiation at line @
cse	cdc	prts	prts_out_of_range_cdccs	e					Parameter @[@ : @]part select is out of range at line @
cse	cdc	prts	ill_prts_inst_array_cdccs	e					Illegal value for part select of instance array 'name' at line @
cse	cdc	prts	const_prts_contains_non_const_selector_cdccs	e					Constant part select @ contains a non-constant selector @ at line @
cse	cdc	prts	bus_index_prts_for_var_out_of_range_cdccs	e					Bus index @ integer of part select [@:@] for variable @ out of range at line @
cse	cdc	prts	bus_prts_for_var_out_of_range_cdccs	e					Bus part select [@:@] for variable @ out of range at line @
cse	cdc	prts	bus_prts_index_out_of_name_for_var_cdccs	e					Bus part select [@:@] index @ out of range for variable @ at line @
cse	cdc	prts	ill_token_in_prts_cdccs	e					Illegal token in part select @ at line @
cse	cdc	prts	incomplete_prts_specification_cdccs	e					Incomplete part select specification @ at line @
cse	cdc	prts	ill_index_in_prts_cdccs	e					Illegal index in part select @ at line @
cse	cdc	prts	negative_index_in_prts_not_allowed_cdccs	e					Negative index in part select @ not allowed at line @
cse	cdc	prts	prts_index_order_reversed_cdccs	e					Part select index order reversed [@ : @] [@ : @] should be [@ : @] at line @
cse	cdc	prts	index_vec_over_max_size_cdccs	w					Vector index @ exceeds the size of the vector.

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									Index truncated at line @
cse	cdc	prts	x_or_z_in_vec_bit_select_index_cdcsc	e					x or z in vector bit select index at line @
cse	cdc	sdir	ignored_synopsis_csdir_csstmt_cdccd	w					Ignored a synopsis case directive which is not applied to a Case statement at line @
cse	cdc	sdir	ignored_synopsis_csdir_miss_end_cdccd	w					Ignored a synopsis case directive which is missing the end<directive> at line @
cse	cdc	simr	inefficient_op_not_a_power_of_2_cdccs	e					Division/modulus by a number not a power of 2. Inefficient simulation operation. at line @
cse	cdc	simr	simr_multiple_init_blk_force_cdccs	w					Multiple initial blocks force @. Unpredictable simulation result at line @
cse	cdc	snsl	incomplete_snsl_cdccs	w					Incomplete sensitivity list. @ is not in the sensitivity list. at line @
cse	cdc	snsl	edge_sns_process_contains_data_pin_snsl_cdccs	e					Edge sensitive process contains a data pin @ in the sensitivity list at line @
cse	cdc	snsl	unsupp_expr_in_snsl_cdccs	w					Unsupported Expression type @ in sensitivity list ' at line @
cse	cdc	snsl	partial_bus_decl_width_cdccs	e	?				partial bus @ declared with width @ width @ at line @
cse	cdc	snsl	contains_inst_name_cdccs	e					Contains instance name @ at line @
cse	cdc	stmt	null_not_allowed_stmt_cdccs	e					Null statement is not allowed here at line @
cse	cdc	stmt	stmt_ill_accept_only_net_reg_mem_cdccs	e					Illegal type @ can only accept net, reg, memory at line @
cse	cdc	stmt	stmt_ill_accept_only_port_reg_mem_cdccs	e					Illegal type @ can only accept port, reg, memory at line @
cse	cdc	stmt	stmt_ill_accept_only_signal_reg_mem_cdccs	e					Illegal type @ can only accept signal, reg, memory at line @
cse	cdc	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_cdccs	e					Arithmetic operator RHS has one less bit than the LHS at line @
cse	cdc	stmt	ar_op_unequal_lhs_rhs_cdccs	e					Arithmetic operator unequal width LHS and RHS at line @
cse	cdc	stmt	ar_op_unequal_var_on_rhs_cdc	e					Arithmetic operator unequal width variables @ on RHS at line @
cse	cdc	stmt	empty_stmt_cdc	e					Empty-statement at line @
cse	cdc	syst	return_var_of_user_used_as_rhs_cdccs	w					Return variable of user system task is used as a RHS variable at line @
cse	cdc	task	ask_var_not_decl_cdccs	e					Variable @ used but not declared at line @
cse	cdc	task	too_few_arg_to_task_cdccs	e					Too few arguments passed to task @ at line @
cse	cdc	tri	instance_not_tri_state_device_cdccs	e					Instance name is not a tri-state device at line @
cse	cdc	tri	unsupp_gate_type_tristate_cdccs	e					Unsupported gate type @ used for tristate at line @
cse	cdc	tri	tri_not_desgn_gate_contention_cdccs	e					Tristate not designed correctly gate @ can cause contention at line @
cse	cdc	tri	unsupp_type_instance_tri_cdcsc	e					Unsupported type instance type used for tristate @ at line @
cse	cdc	tri	incorrect_cont_assign_stmt_tri_gate_cdccs	e					Incorrect continuous assign statement for tristate gate @ at line @
cse	cdc	tri	const_assign_to_multidriven_net_cdccs	e					Constant (constiznt) assigned to multi-driven Net @ at line @
cse	cdc	tri	const_assign_to_multidriven_port_cdccs	e					Constant (constiznt) assigned to multi-driven Port @ at line @
cse	cdc	tri	const_assign_to_multidriven_signal_cdccs	e					Constant (constiznt) assigned to multi-driven Signal @ at line @
cse	cdc	tri	unsupp_expr_for_tri_cdccs	e					Unsupported Expression type @ for tristate at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	cdc	vec	vec_invalid_cdccs	e					Vector @ is invalid. at line @
cse	cdc	vec	vec_mod_not_exist_cdccs	e					Vector @ module name does not exist at line @
cse	cdc	vec	vec_ent_not_exist_cdccs	e					Vector @ entity name does not exist at line @
cse	cdc	vec	vec_unit_not_exist_cdccs	e					Vector @ unit name does not exist at line @
cse	cdc	vec	vec_not_contain_data_sig_cdccs	e					Vector @ does not contain any data signals at line @
cse	cdc	vec	vec_not_contain_clk_sig_cdccs	e					Vector @ does not contain a clock signal at line @
cse	cdc	vec	vec_not_contain_rst_sig_cdccs	e					Vector @ does not contain a reset signal at line @
cse	cdc	vec	vec_stim_not_contain_input_ports_cdccs	e					Vector @ which is a stimulus vector does not contain any input ports at line @
cse	cdc	vec	vec_expect_not_contain_outputs_ports_cdccs	e					Vector @ which is an expect vector does not contain any output ports at line @
cse	cdc	vec	vec_is_missing_the_cdccs	e					Vector @ is missing the @ at line @
cse	cdc	vec	vec_dtsig_not_found_cdccs	e					Vector @ data signals @ not found at line @
cse	cdc	vec	vec_clk_sig_not_found_cdcsc	e					Vector @ clock signal @ not found at line @
cse	cdc	vec	vec_rst_sig_not_found_cdccs	e					Vector @ reset signal @ not found at line @
cse	cdc	vec	vec_stim_input_port_not_found_cdccs	e					Vector @ stimulus vector input port @ not found at line @
cse	cdc	vec	vec_output_port_not_found_cdccs	e					Vector @ output port @ not found at line @
cse	cde	ase	arch_state_el_ev_not_found	e					Architectural state element @ event name @ not found at line @
cse	csa	assn	unequal_length_lhs_rhs_cscs	e					Unequal length LHS and RHS at line @
cse	csa	assn	unequal_length_lhs_rhs_off_one_bit_cscs	e					Unequal length LHS and RHS off by one bit at line @
cse	csa	ccs	clkspec_miss_clk_name	e					Clock specification @ is missing the clock name at line @
cse	csa	clk	merge_clk_phases_cscd	e					Merge clock phases (clock A-phase) vs (clock B-phase) Path for (clock A-phase) at line @
cse	csa	clk	gated_clk_connected_to_clk_data_logic_cscd	e					Gated clock @ is connected to both clock and data logic at line @
cse	csa	clk	clk_merge_with_data_signals_cscd	e					Unable to continue trace of clock in clock tree which causes the clock to merge with the data signals at line @
cse	csa	clk	cannot_analyze_the_gated_clk_type_cscs	e					Clock tree analysis can not analyze the gated clock type @ at line @
cse	csa	clk	cannot_find_the_clk_source_cscd	e					Cannot find the clock source @ at line @
cse	csa	clk	clk_pin_not_driven_cscd	e				x	Clock pin @pin is not driven by a clock tree through combinational gates (there must be combinational path from a clock source to @. The user must identify generated clocks by using a -cslc_gen_clk <clock_name>- directive the endpoint of generated clocks. The end point is the end point of the combinational path from a clock source to a combinational gate. at line @
cse	csa	clk	clk_net_from_seq_logic_driver_cscd	e					Clock net @ derived from sequential logic driver name @ at line @
cse	csa	clk	clk_port_from_seq_logic_driver_cscd	e					Clock port @ derived from sequential logic driver name @ at line @
cse	csa	clk	clk_sig_from_seq_logic_driver_cscd	e					Clock signal @ derived from sequential logic

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									driver name @ at line @
cse	csa	clk	merge_clk_data_logic_same_gate_cscd	e					Merged clock and data logic. A gate is connected to both a clock signal and a data signal. Clock and data signals cannot be connected to the same combinational gate. Do you need to use a gated clock directive to specify a gated clock? End point @ at line @
cse	csa	clk	mux_output_used_as_clk_cscd	e					Mux output is used as a clock. Either the mux select or al of the mux inputs must be driven by a gated clock at line @
cse	csa	clk	generated_clk_is_selfclked_cscd	e					Generated clock @ is self -clocked. at line @
cse	csa	clk	comb_logic_loop_in_clk_tree_cscd	e					Combinational logic loop in clock tree start point @ at line @
cse	csa	clk	clk_enable_is_a_generated_clk_cscd	e					Clock enable @ is a generated clock @ at line @
cse	csa	clk	generated_clk_has_more_than_one_drive_cscd	e					Generated clock @ has more than one driver at line @
cse	csa	clk	found_unsupp_gated_clk_cscd	e					Clock glitch design rule checking found the following unsupported gated clock logic type @ at line @
cse	csa	clk	unsupp_logic_operation_cscs	w					Unsupported logic operation type @. at line @
cse	csa	clk	unsupp_cl_gated_logic_cscs	w					Unsupported gated clock logic type. at line @
cse	csa	clk	unsupp_logic_expr_clk_cscs	w					Unsupported logicExpression type @ at line @
cse	csa	clk	unsupp_logic_expr_clk_cdcs	w					Unsupported logicExpression type @ at line @
cse	csa	csi	noncnst_in_iclude_file_cscs	e					Non-constant in include file @ at line @
cse	csa	datl	comb_logic_loop_in_data_logic_cscd	e					Combinational logic loop in data logic at line @
cse	csa	datl	comb_logic_loop_in_data_logic_latch_cscd	e					Combinational logic loop in data logic with Latch Buffer at line @
cse	csa	datl	find_comb_loop_cscd	e					Component loop A combinational loop was detected which involves a split vector which is part of a combinational loop. Starting point @ at line @
cse	csa	datl	comp_loop_detected_cscd	e					Component loop detected @ starting point @ at line @
cse	csa	datl	irregular_latch_in_comp_loop_cscd	e					Irregular latch in component loop. An irregular latch is a latch that can be open continuously for the entire cycle. One latch in the loop must be closed at some point during the clock cycle. starting point @ at line @
cse	csa	drvc	multiply_drvn_net_nontri_gate_cscs	w					Multiply drivenNet driven by a non-tristate gate at line @
cse	csa	drvc	multiply_drvn_port_nontri_gate_cscs	w					Multiply drivenPort driven by a non-tristate gate at line @
cse	csa	drvc	multiply_drvn_sig_nontri_gate_cscs	w					Multiply drivenSignal driven by a non-tristate gate at line @
cse	csa	drvc	incompatible_driver_net_cscs	w					Incompatible driver of type @ drivingNet_@ multi drivenNet of type @ name @ at line @
cse	csa	drvc	incompatible_driver_port_cscs	w					Incompatible driver of type @ drivingPort_@ multi drivenPort of type @ name @ at line @
cse	csa	drvc	incompatible_driver_sig_cscs	w					Incompatible driver of type @ drivingSignal_@

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									multi drivenSignal of type @ name @ at line @
cse	csa	expr	unary_op_in_comparison_cscs	e					Unary op used in comparison at line @
cse	csa	expr	miss_parenthesis_cscs	e					Unary op @ with comparison op @ missing precedence parenthesis at line @
cse	csa	init	assn_mem_in_init_blk_cscs	e					Assign memory in initial block at line @
cse	csa	inst	input_port_drvn_from_inside_mod_cscs	e					Input port @ being driven from inside of module @ at line @
cse	csa	inst	input_port_drvn_from_inside_entity_cscs	e					Input port @ being driven from inside of entity @ at line @
cse	csa	inst	input_port_drvn_from_inside_signal_cscs	e					Input port @ being driven from inside of signal @ at line @
cse	csa	inst	input_port_not_connected_in_parent_mod_cscs	e					Input port @ not connected in parent module at line @
cse	csa	inst	input_port_not_connected_in_parent_entity_cscs	e					Input port @ not connected in parent entity at line @
cse	csa	inst	input_port_not_connected_in_parent_signal_cscs	e					Input port @ not connected in parent signal at line @
cse	csa	mdb	single_comp_contains_multiple_tri_drv_cscs	w					A single component contains multiple tristate drivers at line @
cse	csa	mdb	unsuppexpr_on_lhs_net_drv_stmt_cscs	w					Unsupported Expression type type on LHS ofNet driver statement at line @
cse	csa	mdb	unsuppexpr_on_lhs_port_drv_stmt_cscs	w					Unsupported Expression type type on LHS ofPort driver statement at line @
cse	csa	mdb	unsuppexpr_on_lhs_sig_drv_stmt_cscs	w					Unsupported Expression type type on LHS ofSignal driver statement at line @
cse	csa	mdb	tri_not_in_top_mod_cscs	e					Tristate not in top module at line @
cse	csa	mdb	tri_not_in_top_ent_cscs	e					Tristate not in top entity at line @
cse	csa	mdb	tri_not_in_top_sig_cscs	e					Tristate not in top signal at line @
cse	csa	mdb	tri_primitive_inst_cscs	e					Tristate primitive instantiation at line @
cse	csa	mdb	tri_net_only_one_drvr_cscs	e					Tri Net has only one driver at line @
cse	csa	mdb	tri_port_only_one_drvr_cscs	e					Tri Port has only one driver at line @
cse	csa	mdb	tri_sig_only_one_drvr_cscs	e					Tri Signal has only one driver at line @
cse	csa	mod	redef_mod_cscs	e					Redefined module @ at line @
cse	csa	mod	redef_ent_cscs	e					Redefined entity @ at line @
cse	csa	mod	redef_signal_cscs	e					Redefined signal @ at line @
cse	csa	net	tri_and_net_only_one_driver_cscs	e	?				triandNet @ has only one driver at line @
cse	csa	net	tri_and_port_only_one_driver_cscs	e	?				triandPort @ has only one driver at line @
cse	csa	net	tri_and_sig_only_one_driver_cscs	e	?				triandSignal @ has only one driver at line @
cse	csa	net	var_assn_but_never_ref_cscs	e					Variable @ assigned but never referenced at line @
cse	csa	net	var_never_assn_cscs	e					Variable @ never assigned at line @
cse	csa	net	var_not_assn_in_all_paths_cscs	e					Variable @ not being assigned in all paths at line @
cse	csa	net	var_not_in_snsl_cscs	e					Variable @ not in sensitivity list at line @
cse	csa	net	reg_connected_to_inout_in_inst_cscs	e					Reg @ connected to inout @ in instantiation @ at line @
cse	csa	net	reg_connectede_to_output_in_inst_cscs	e					Reg @ connected to output in instantiation at line @
cse	csa	net	reg_used_as_output_of_cont_assn_cscs	e					Reg @ used as output of continuous assign at line @
cse	csa	net	port_used_prior_to_decl_cscs	e					Port @ used prior toDeclaration at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	csa	parm	redef_param_cscs	e					Redefined parameter @ at line @
cse	csa	pp	redef_macro_cscs	e					Redefined macro @ at line @
cse	csa	prts	vec_index_order_incorrect_cscs	e					Vector index @ order incorrect at line @
cse	csa	prts	vec_index_truncated_cscs	e					Vector index @ truncated at line @
cse	csa	seq	seq_latch_connected_to_latch_in_loop_cscd	e					Latch connected to latch in loop at line @
cse	csa	sply	output_conncet_to_sply_	e					Output @ connect to supply at line @
cse	csa	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_cscs	e					Arithmetic operator RHS has one less bit than the LHS at line @
cse	csa	stmt	ar_op_unequal_lhs_rhs_cscs	e					Arithmetic operator unequal width LHS and RHS at line @
cse	csa	stmt	ar_op_unequal_var_on_rhs_cscs	e					Arithmetic operator unequal width variables @ on RHS at line @
cse	csa	tri	tri_not_in_top_mod_cscs	e					Tristate @ not in top module at line @
cse	csa	tri	tri_not_in_top_entity_cscs	e					Tristate @ not in top entity at line @
cse	csa	tri	tri_not_in_top_signal_cscs	e					Tristate @ not in top signal at line @
cse	csa	tri	tri_prim_ist_cscs	e					Tristate primitive instantiation @ at line @
cse	csb	ase	arch_state_el_mod_not_exist_csbcs	e					Architectural state element @ module @ does not exist at line @
cse	csb	ase	arch_state_el_ent_not_exist_cbcs	e					Architectural state element @ entity @ does not exist at line @
cse	csb	ase	arch_state_el_unit_not_exist_csbcs	e					Architectural state element @ unit @ does not exist at line @
cse	csb	ase	arch_state_el_missi_clk_name_csbcs	e					Architectural state element @ is missing the clock name at line @
cse	csb	ase	arch_state_el_miss_mem_name_csbcs	e					Architectural state element @ is missing the memory name at line @
cse	csb	ase	arch_state_el_miss_the_csbcs	e					Architectural state element @ is missing the @ at line @
cse	csb	ase	arch_state_el_miss_rst_name_csbcs	e					Architectural state element @ is missing the reset name at line @
cse	csb	ase	arch_state_el_evtrigg_miss_ev_name_csbcs	e					Architectural state element @ is event triggered and is missing the event name at line @
cse	csb	ase	arch_state_el_clk_name_not_found_csbcs	e					Architectural state element @ clock name @ not found at line @
cse	csb	ase	arch_state_el_mem_name_not_found_csbcs	e					Architectural state element @ memory name @ not found at line @
cse	csb	ase	arch_state_el_not_found_csbcs	e					Architectural state element @ arch_state_name @ not found at line @
cse	csb	ase	arch_state_el_rst_not_found	e					Architectural state element @ reset name @e not found at line @
cse	csb	assn	x_in_rhs_of_assihnment_csbcs	e					x in rhs of assignment at line @
cse	csb	assn	z_in_rhs_of_assn_default_csi_csbcs	e					x in rhs of assignement in defaultCase item at line @
cse	csb	assn	z_in_rhs_of_assn_csbcs	e					z in rhs of assignement at line @
cse	csb	assn	unequal_length_lhs_rhs_csbcs	e					Unequal length LHS and RHS at line @
cse	csb	assn	unequal_length_lhs_rhs_off_one_bit_csbcs	e					Unequal length LHS and RHS off by one bit at line @
cse	csb	ccd	ccd_cdir_must_be_cst_expr_csbcs	e				x	CSL directive size must be constant Expression at line @
cse	csb	ccd	clk_dir_not_applied_to_dsgn_csbcs	w				x	CSL clock directive not applied to design. Could not find clock at line @
cse	csb	ccd	csl_filter_unused_csbcs	w				x	CSL message filter @ not found. Filter @ is unused. at line @
cse	csb	ccd	csl_mess_not_filtered_csbcs	w				x	CSL message @ can not be filtered. Filter @ is

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									unused. at line @
cse	csb	ccd	error_csdir_not_found_csbcs	e				x	Error CSL directive @ not found. Error @ is unused. at line @
cse	csb	chrs	ill_val_chrs_csb	e					Illegal value @ at line @
cse	csb	clk	clk_name_not_found_cdir_csbcs	e				x	Clock name not found in cslc directive at line @
cse	csb	clk	expr_sunj_to_different_clk_phases_csbcs	e					Expression subject to different clock phases at line @
cse	csb	csi	z_csi_not_in_casez_csb	e					z case item not in casez at line @
cse	csb	csi	noncstn_rep_in_conc_csbcs	e					Non-constant repeator in concatenation at line @
cse	csb	decl	decl_array_over_max_size_csbcs	e					Array @ exceeds maximum size limit at line @
cse	csb	dely	x_or_z_in_dely_csbcs	e					x or z in delay at line @
cse	csb	dmsn	mem_prts_index_out_of_range_for_mem_csbcs	e					Memory part select [@:@] index @ out range for memory @ at line @
cse	csb	dmsn	dime_select_for_mem_missing_csbcs	e					Select for memory @ missing at line @
cse	csb	dmsn	dime_index_out_of_bounds_for_mem_csbcs	e					Index <index> out of bounds for memory @. Range [@: @] at line @
cse	csb	dmsn	dime_prts_out_of_bounds_for_net_csbcs	e					Part select [@ : @] out of bounds for net @. Range [@ : @] at line @
cse	csb	dmsn	dime_prts_out_of_bounds_for_port_csbcs	e					Part select [@ : @] out of bounds for port @. Range [@ : @] at line @
cse	csb	dmsn	dime_prts_out_of_bounds_for_sig_csbcs	e					Part select [@ : @] out of bounds for signal @. Range [@ : @] at line @
cse	csb	dmsn	dime_prts_reg_csbcs	e					Part select [@ : @] reg @. Range [@ : @] at line @
cse	csb	drvc	incompatible_drvc_for_net_csbcs	e					Incompatible drivers for Net @ at line @
cse	csb	drvc	incompatible_drvc_for_port_csbcs	e					Incompatible drivers for Port @ at line @
cse	csb	drvc	incompatible_drvc_for_sig_csbcs	e					Incompatible drivers for Signal @ at line @
cse	csb	drvc	drvc_multiple_drive_net_partially_overlap_csbcs	e					Multiple drive Net partially overlap at line @
cse	csb	drvc	drvc_multiple_drive_port_partially_overlap_csbcs	e					Multiple drive Port partially overlap at line @
cse	csb	drvc	drvc_multiple_drive_sig_partially_overlap_csbcs	e					Multiple drive Signal partially overlap at line @
cse	csb	dsgn	dsgn_top_mod_cannot_id_csbcs	e					Top module @ cannot be identified at line @
cse	csb	dsgn	dsgn_top_entity_cannot_id_csbcs	e					Top entity @ cannot be identified at line @
cse	csb	dsgn	dsgn_top_unit_cannot_id_csbcs	e					Top unit @ cannot be identified at line @
cse	csb	dsgn	unit_dsgn_cycle_not_spanning_tree_csbcs	e					Unit design hierarchy contains a cycle. Hierarchy is not a spanning tree. at line @
cse	csb	expr	const_expr_nm_var_cscsb	e					Constant Expression contains variable @ at line @
cse	csb	expr	const_expr_usage_cscsb	e					Constant Expression usage at line @
cse	csb	expr	expr_prts_indices_1bit_var_csbcs	e					Part select indices 1-bit variable at line @
cse	csb	expr	expr_prts_must_be_cst_expr_csbcs	e					Part select specifier Expression must be constant Expression at line @
cse	csb	expr	not_const_expr_csbcs	e					Repetition multiplier in concatenation is not a constant Expression at line @
cse	csb	expr	ill_bit_select_expr_csbcs	e					Illegal bit select expression @ at line @
cse	csb	expr	repetition_multiplier_in_conc_not_const_expr_csbcs	w					Repetition multiplier in concatenation is not a constant Expression at line @
cse	csb	expr	int_operand_not_1_bit_csbcs	w					Logic operator has integer operands instead of 1-bit operands at line @
cse	csb	expr	unsupp_expr_csbcs	w					Unsupported Expression type @ at line @
cse	csb	expr	unsupp_operator_csbcs	w					Unsupported operator type @ at line @

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cse	csb	expr	use_of_sg_bit_const_csbcs	w					Use of single bit constant at line @
cse	csb	expr	unary_op_in_comparison_csbcs	e					Unary op used in comparison at line @
cse	csb	expr	x_or_z_in_cond_expr_csbcs	e					x or z in conditional expression at line @
cse	csb	expr	zero_in_rep_in_conc_csbcs	e					Zero repeator in concatenation at line @
cse	csb	expr	expr_in_mod_port_dir_csbcs	e					Expression @ in module port dir at line @
cse	csb	expr	expr_in_ent_port_dir_csbcs	e					Expression @ in entity port dir at line @
cse	csb	expr	expr_in_sig_port_dir_csbcs	e					Expression @ in unit port dir at line @
cse	csb	expr	expr_in_inst_csbcs	e					Expression @ in inst i@ at line @
cse	csb	expr	expr_operator_operands_unequal_lenght_csbcs	e					Expression operator @ operands @ unequal length at line @
cse	csb	file	cannot_open_filter_specification_file_csbcs	e					Cannot open filter specification file @ at line @
cse	csb	file	filter_specification_file_missing_csbcs	e					Filter specification file name @ is missing at line @
cse	csb	file	mismatch_mod_file_name_csbcs	e					Mismatch between module name @ and file name @ at line @
cse	csb	file	mismatch_ent_file_name_csbcs	e					Mismatch between entity name @ and file name @ at line @
cse	csb	file	mismatch_sig_file_name_csbcs	e					Mismatch between signal name @ and file name @ at line @
cse	csb	func	func_arg_miss_cscsb	e					Function call missing argument(s) at line @
cse	csb	func	port_not_output_func_csbcs	e					Port @ direction cannot be output at line @
cse	csb	func	too_many_arg_to_func_csbcs	e					Too many arguments passed to function @ at line @
cse	csb	func	too_few_arg_to_func_csbcs	e					Too few arguments passed to function @ at line @
cse	csb	func	undefined_func_csbcs	e					Undefined function @ at line @
cse	csb	func	funct_expr_cannot_expnaded_csbcs	e					Function expression @ cannot be expanded at line @
cse	csb	func	funct_not_used_in_expr_csbcs	w					Function @ is not being used in an Expression at line @
cse	csb	func	func_decl_csbcs	w					Function Declaration @ already declared as another type at line @
cse	csb	hid	cannot_locate_hier_id_hid_csbcs	e					Can't locate hierarchical identifier @ at line @
cse	csb	hid	ref_minst_found_in_expr_hid_csbcs	e					References a module instance @ found in an Expression hid at line @
cse	csb	hid	ref_entity_found_in_expr_hid_csbcs	e					References a entity instance @ found in an Expression hid at line @
cse	csb	hid	ref_unit_found_in_expr_hid_csbcs	e					References a unit instance @ found in an Expression hid at line @
cse	csb	hid	hid_reference_not_found_csbcs	e					@ reference not found at line @
cse	csb	hid	mifc_in_hid_not_exist_csbcs	e					Module instance @ in hid does not exist at line @
cse	csb	hid	entity_instance_in_hid_not_exist_csbcs	e					Entity instance @ in hid does not exist at line @
cse	csb	hid	unit_instance_in_hid_not_exist_csbcs	e					Unit instance @ in hid does not exist at line @
cse	csb	hid	mod_found_in_path_in_dsgn_csbcs	e					Module @ found in path @ in the design at line @
cse	csb	hid	enity_found_in_path_in_dsgn_csbcs	e					Entity @ found in path @ in the design at line @
cse	csb	hid	unit_found_in_path_in_dsgn_csbcs	e					Unit @ found in path @ in the design at line @
cse	csb	hid	hierarchical_id_path_contains_func_csb	e					Hierarchical ID @ path contains a function at line @
cse	csb	init	assn_mem_in_init_blk_csbcs	e					Assign memory in initial block at line @
cse	csb	inst	inst_duplicate_mod_name_csbcs	e					Duplicate port @ in the port list for module @ at line @
cse	csb	inst	inst_duplicate_entity_name_csbcs	e					Duplicate port @ in the port list for entity @ at

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									line @
cse	csb	inst	inst_duplicate_unit_name_csbcs	e					Duplicate port @ in the port list for unit @ at line @
cse	csb	inst	ill_mod_inst_name_csbcs	e					Illegal module instance @ at line @
cse	csb	inst	ill_entity_inst_name_csbcs	e					Illegal entity instance @ at line @
cse	csb	inst	ill_unit_inst_name_csbcs	e					Illegal unit instance @ at line @
cse	csb	inst	inst_name_defined_mod_csbc	e					Instance name @ already defined in this module at line @
cse	csb	inst	inst_name_defined_ent_csbc	e					Instance name @ already defined in this entity at line @
cse	csb	inst	inst_name_defined_unit_csbc	e					Instance name @ already defined in this unit at line @
cse	csb	inst	inst_too_many_bits_csbcs	e					Too many bits for port @ of instance array @, formal @, actual @ at line @
cse	csb	inst	inst_port_not_connected_var_csbcs	e					Port 'port' of instance array 'array' is not connected to variable at line @
cse	csb	inst	inst_insufficient_bits_csbcs	e					Insufficient bits for port 'port' of instance array 'array ', formal number, actual number at line @
cse	csb	inst	inst_mod_name_not_defined_csbcs	e					Module name not defined at line @
cse	csb	inst	inst_ent_name_not_defined_csbcs	e					Entity name not defined at line @
cse	csb	inst	inst_unit_name_not_defined_csbcs	e					Unit name not defined at line @
cse	csb	inst	many_mod_inst_param_assign_csbcs	e					Too many module instance parameter assignments (number > rrumber) at line @
cse	csb	inst	many_entity_inst_param_assign_csbcs	e					Too many entity instance parameter assignments (number > rrumber) at line @
cse	csb	inst	many_unit_inst_param_assign_csbcs	e					Too many unit instance parameter assignments (number > rrumber) at line @
cse	csb	inst	complexexpr_cannot_mapped_inout_port_csbcs	e					Complex Expression @ cannot be mapped to inout port @ at line @
cse	csb	inst	complexexpr_cannot_mapped_unknown_port_csbcs	e					Complex Expression @ cannot be mapped to unknown type port @ at line @
cse	csb	inst	netdecl_contains_ill_prts_csbcs	e					Net Declaration [@: @] contains an illegal part select at line @
cse	csb	inst	regdecl_contains_ill_prts_csbcs	e					Reg Declaration [@ : @] contains an illegal part select at line @
cse	csb	inst	complex_expr_inst_parent_module_csbcs	e					Complex actual Expression associated with port @ of module @ instantiated in parent module at line @
cse	csb	inst	complex_expr_inst_entity_parent_module_csbcs	e					Complex actual Expression associated with port @ of entity @ instantiated in parent module at line @
cse	csb	inst	complex_expr_inst_unit_parent_module_csbcs	e					Complex actual Expression associated with port @ of unit @ instantiated in parent module at line @
cse	csb	inst	inst_mod_output_port_width_csbcs	e					Mod @ Output port @ width mismatch, actual-width (port-width) at line @
cse	csb	inst	inst_entity_output_port_width_csbcs	e					Entity @ Output port @ width mismatch, actual-width (port-width) at line @
cse	csb	inst	inst_unit_output_port_width_csbcs	e					Unit @ Output port @ width mismatch, actual-width (port-width) at line @
cse	csb	inst	inst_mod_input_port_width_csbcs	e					Mod @ Input port @ width mismatch,

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									actual-width (port-width) at line @
cse	csb	inst	inst_entity_input_port_width_csbcs	e					Entity @ Input port @ width mismatch, actual-width (port-width) at line @
cse	csb	inst	inst_unit_input_port_width_csbcs	e					Unit @ Input port @ width mismatch, actual-width (port-width) at line @
cse	csb	inst	inst_mod_not_define_csbcs	e					Module not defined at line @
cse	csb	inst	inst_entity_not_define_csbcs	e					Entity not defined at line @
cse	csb	inst	inst_unit_not_define_csbcs	e					Unit not defined at line @
cse	csb	inst	mifc_port_actual_formal_width_mismatch_csbcs	w					Module @ instance @ port @ width mismatch, actual width @ formal width @ at line @
cse	csb	inst	ent_port_actual_formal_width_mismatch_csbcs	w					Entity @ instance @ port @ width mismatch, actual width @ formal width @ at line @
cse	csb	inst	unit_port_actual_formal_width_mismatch_csbcs	w					Unit @ instance @ port @ width mismatch, actual width @ formal width @ at line @
cse	csb	inst	inst_differs_in_case_from_mod_csbcs	e					Instance name @ differs in case from module name @ at line @
cse	csb	inst	inst_differs_in_case_from_ent_csbcs	e					Instance name @ differs in case from entity name @ at line @
cse	csb	inst	inst_differs_in_case_from_sig_csbcs	e					Instance name @ differs in case from signal name @ at line @
cse	csb	loop	undet_init_value_loop_csbcs	e					Unable to determine init value for loop at line @
cse	csb	loop	undet_limit_loop_csbcs	e					Unable to determine limit for loop at line @
cse	csb	loop	loop_bounds_calculated_int_csbcs	w					Loop bounds are calculated to be integer @, check that this is correct at line @
cse	csb	loop	expr_lhs_contains_var_bit_select_csbcs	w					Expression in lhs of assignment contains a variable bit select at line @
cse	csb	loop	loop_bounds_not_const_csb	w					Loop bounds are non-constant at line @
cse	csb	loop	loop_ctrl_init_expr_not_const_csbcs	w					Non-constant loop bound. Loop control variable initialization Expression is not a constant Expression at line @
cse	csb	loop	loop_term_expr_not_const_csbcs	w					Non-constant loop bound. loop terminating Expression could not be evaluated to a constant at line @
cse	csb	loop	init_expr_reset_by_var_csbcs	e					Non-constant loop bound. initializing Expression reset by variable at line @
cse	csb	loop	loop_ctrl_var_1_bit_wide_csbcs	w					The loop control variable @ is one bit wide. Check the loop control variable Declaration. at line @
cse	csb	mdb	bad_mdb_net_csbcs	e					Bad multi-driven Net @ at line @
cse	csb	mdb	bad_mdb_port_csbcs	e					Bad multi-driven Port @ at line @
cse	csb	mdb	bad_mdb_signal_csbcs	e					Bad multi-driven Signal @ at line @
cse	csb	mdb	unsupp_comp_mdb_net_csbcs	e	?				Unsupported component type @ driving in multi-driven Net name at line @
cse	csb	mdb	unsupp_comp_mdb_port_csbcs	e	?				Unsupported component type @ driving in multi-driven Port name at line @
cse	csb	mdb	unsupp_comp_mdb_signal_csbcs	e	?				Unsupported component type @ driving in multi-driven Signal name at line @
cse	csb	mdb	unsupp_comp_drive_mdb_csbcs	e	?				Unsupported component type @ driving multi-driven Net natne at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	csb	mdb	unsupp_comp_drive_mdb_port_csbcs	e	?				Unsupported component type @ driving multi-driven Port natne at line @
cse	csb	mdb	unsupp_comp_drive_mdb_signal_csbcs	e	?				Unsupported component type @ driving multi-driven Signal natne at line @
cse	csb	mdb	mdb_net_driven_by_trns_csbcs	e					Multiply driven Net driven by transistor primitive type @ at line @
cse	csb	mdb	mdb_port_driven_by_trns_csbcs	e					Multiply driven Port driven by transistor primitive type @ at line @
cse	csb	mdb	mdb_sig_driven_by_trns_csbcs	e					Multiply driven Signal driven by transistor primitive type @ at line @
cse	csb	mdb	mdb_unsupp_comp_drvs_net_csbcs	e					Unsupported component type driving Net drives Net connected to multi-driven Net at line @
cse	csb	mdb	mdb_unsupp_comp_drvs_port_csbcs	e					Unsupported component type driving Port drives Port connected to multi-driven Port at line @
cse	csb	mdb	mdb_unsupp_comp_drvs_sig_csbcs	e					Unsupported component type driving Signal drives Signal connected to multi-driven Signal at line @
cse	csb	mdb	mdb_incompatible_net_drives_multiple_net_csbcs	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Net at line @
cse	csb	mdb	mdb_incompatible_port_drives_multiple_port_csbcs	e					Incompatible driver driving tandem Port drives Port connected to multi-driven Port at line @
cse	csb	mdb	mdb_incompatible_sig_drives_multiple_sig_csbcs	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Port at line @
cse	csb	mdb	mdb_unsupp_LHS_concatenation_csbcs	e					Unsupported LHS concatenation in multi-drive 'device at line @
cse	csb	mdb	mdb_bus_has_too_many_drivers_csbcs	e					Bus has too many drivers. at line @
cse	csb	mdb	mdb_always_blk_drive_csbcs	w					Multiple always blocks drive name @ at line @
cse	csb	mdb	nontri_gate_drives_mdb_net_csbcs	w					non-tri-state gate drives multi-driven Net at line @
cse	csb	mdb	nontri_gate_drives_mdb_port_csbcs	w					non-tri-state gate drives multi-driven Port at line @
cse	csb	mdb	nontri_gate_drives_mdb_sig_csbcs	w					non-tri-state gate drives multi-driven Signal at line @
cse	csb	mem	mem_ref_without_index_csbcs	e					Memory @ referenced without index through hierarchical ID @ at line @
cse	csb	mifc	port_identifier_mifc_csbcs	e					Port @ at line @
cse	csb	mifc	mod_output_wire_redecl_reg_csbcs	e					Module @ output port re-declared as type reg after use as implicitly declared wire at line @
cse	csb	mifc	entity_output_wire_redecl_reg_csbcs	e					Entity @ output port re-declared as type reg after use as implicitly declared wire at line @
cse	csb	mifc	unit_output_wire_redecl_reg_csbcs	e					Unit @ output port re-declared as type reg after use as implicitly declared wire at line @
cse	csb	mifc	output_port_is_mem_type_mifc_csbcs	e					Output port @ is memory type at line @
cse	csb	mifc	mifc_inout_port_is_mem_type_csbcs	e					Inout port @ is memory type at line @
cse	csb	mifc	mod_output_port_mismatch_actual_witdh_csbcs	w					Module @ output port @ formal to actual width mismatch at line @
cse	csb	mifc	ent_output_port_mismatch_actual_witdh_csbcs	w					Entity @ output port @ formal to actual width mismatch at line @
cse	csb	mifc	unit_output_port_mismatch_actual_witdh_csb	w					Unit @ output port @

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									formal to actual width mismatch at line @
cse	csb	mifc	port_name_different_in_upper_lower_case_csbcs	e					Port name @ different in upper lower case at line @
cse	csb	mifc	port_not_def_in_iodecl_csbcs	e					Port @ not defined in ioDeclaration at line @
cse	csb	mifc	port_not_def_in_portl_csbcs	e					Port @ not defined in port list at line @
cse	csb	mifc	port_wiredecl_mismatch_csbcs	e					Port @ wireDeclaration mismatch at line @
cse	csb	mifc	pos_based_null_inst_port_csbcs	e					Position based null instance port at line @
cse	csb	mifc	last_portdecl_contains_trailcomma_csbcs	e					Last portDeclaration contains a trailing comma at line @
cse	csb	mins	mins_expr_incompatible_type_csbcs	e					Expression @ has an incompatible argument type @ with the port at line @
cse	csb	mins	mins_mod_not_exist_csbcs	e					Module @ does not exist at line @
cse	csb	mins	mins_entity_not_exist_csbcs	e					Entity @ does not exist at line @
cse	csb	mins	mins_unit_not_exist_csbcs	e					Unit @ does not exist at line @
cse	csb	mod	dup_declar_name_mod_csc	e					Duplicate Declaration of port @ at line @
cse	csb	mod	ill_mod_name_csbcs	e					Illegal module @ at line @
cse	csb	mod	ill_mod_entity_name_csbcs	e					Illegal entity @ at line @
cse	csb	mod	ill_mod_unit_name_csbcs	e					Illegal unit @ at line @
cse	csb	mod	mod_mult_decl_string_csbcs	e					Multiple Declarations of string detected in module @ at line @
cse	csb	mod	mod_entity_mult_decl_string_csbcs	e					Multiple Declarations of string detected in entity @ at line @
cse	csb	mod	mod_unit_mult_decl_string_csbcs	e					Multiple Declarations of string detected in unit @ at line @
cse	csb	mod	mod_mult_def_csbcs	e					Module @ defined in multiple places at line @
cse	csb	mod	mod_ent_mult_def_csbcs	e					Entity @ defined in multiple places at line @
cse	csb	mod	mod_unit_mult_def_csbcs	e					unit @ defined in multiple places at line @
cse	csb	mod	mod_no_module_found_csbcs	e					No modules found at line @
cse	csb	mod	mod_no_entity_found_csbcs	e					No entity found at line @
cse	csb	mod	mod_no_unit_found_csbcs	e					No unit found at line @
cse	csb	mod	failed_find_mod_csbcs	e					Failed to find module @ at line @
cse	csb	mod	failed_find_entity_csbcs	e					Failed to find entity @ at line @
cse	csb	mod	failed_find_unit_csbcs	e					Failed to find unit @ at line @
cse	csb	mod	empty_mod_csbcs	e					Empty module at line @
cse	csb	mod	empty_ent_csbcs	e					Empty entity at line @
cse	csb	mod	empty_unit_csbcs	e					Empty unit at line @
cse	csb	net	net_implicit_wire_redecl_reg_csbcs	e					Implicitly declared as a wire @ re-declared as a reg @. at line @
cse	csb	net	undecl_net_in_mod_csbcs	e					Undeclared net @ in module @ at line @
cse	csb	net	undecl_port_in_mod_csbcs	e					Undeclared port @ in module @ at line @
cse	csb	net	undecl_sig_in_mod_csbcs	e					Undeclared signal @ in module @ at line @
cse	csb	net	undecl_net_in_ent_csbcs	e					Undeclared net @ in entity @ at line @
cse	csb	net	undecl_port_in_ent_csbcs	e					Undeclared port @ in entity @ at line @
cse	csb	net	undecl_sig_in_ent_csbcs	e					Undeclared signal @ in entity@ at line @
cse	csb	net	undecl_net_in_sig_csbcs	e					Undeclared net @ in signal @ at line @
cse	csb	net	undecl_port_in_sig_csbcs	e					Undeclared port @ in signal @ at line @
cse	csb	net	undecl_sig_in_sig_csbcs	e					Undeclared signal @ in signal@ at line @
cse	csb	net	port_used_prior_to_decl_csbcs	e					Port @ used prior toDeclaration at line @
cse	csb	net	1bit_with_prts_csbcs	e					1-bit with part select at line @
cse	csb	netd	ill_decl_vec_csbcs	e					Illegal Declaration of vector @ at line @
cse	csb	nett	nett_ill_reg_name_csbcs	e					Illegal register @ at line @
cse	csb	nett	nett_ill_net_name_csbcs	e					Illegal net @ at line @

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cse	csb	nett	nett_ill_port_name_csbcs	e					Illegal port @ at line @
cse	csb	nett	nett_ill_signal_name_csbcs	e					Illegal signal @ at line @
cse	csb	nett	net_scalar_vect_nett_csbcs	e					Net declared as both scalar and vector at line @
cse	csb	nett	port_scalar_vect_nett_csbcs	e					Port declared as both scalar and vector at line @
cse	csb	nett	signal_scalar_vect_nett_csbcs	e					Signal declared as both scalar and vector at line @
cse	csb	nett	hot_mux_not_use_bus_connection_net_csbcs	e					One hot mux can not be used for bus connection between modules Net @ at line @
cse	csb	nett	hot_mux_not_use_bus_connection_port_csbcs	e					One hot mux can not be used for bus connection between modules Port @ at line @
cse	csb	nett	hot_mux_not_use_bus_connection_sig_csbcs	e					One hot mux can not be used for bus connection between modules Signal @ at line @
cse	csb	num	not_allowed_width0_num_csbcs	e					Width 0 not allowed for sized number at line @
cse	csb	num	real_num_not_allowed_csbcs	e					Real numbers not allowed at line @
cse	csb	num	found_x_z_in_num_literal_csbcs	e					Found x and/or z value in number literal at line @
cse	csb	num	too_many_digits_in_sized_num_csbcs	w					Number of digits exceeds the width in a sized number at line @
cse	csb	num	divide_by_zero_num_csbcs	e					Divide by zero at line @
cse	csb	num	child_mod_inst_parent_mod_csbcs	e					Child module @ instantiates parent module @ at line @
cse	csb	num	child_ent_inst_parent_ent_csbcs	e					Child entity @ instantiates entity module @ at line @
cse	csb	num	child_sig_inst_parent_sig_csbcs	e					Child signal @ instantiates signal module @ at line @
cse	csb	num	int_decl_incorrect_csbcs	e					Integer Declaration incorrect at line @
cse	csb	num	int_var_indexed_csbcs	e					Integer variable inedexed at line @
cse	csb	parm	ill_parm_identifier_csbcs	e					Illegal parameter @ at line @
cse	csb	parm	value_of_parm_OS_platform_dependent_csbcs	w					Parameter select width > 32. The value is OS and platform dependent at line @
cse	csb	parm	parm_redefined_csbcs	w					Parameter @ redefined at line @
cse	csb	port	ill_formal_port_name_csbcs	e					Illegal formal port @ at line @
cse	csb	pp	text_redefined_replaced_csbcs	w					Text macro redefined and replaced @. Previous definition filename, line number @ New definition filename, line number @ at line @
cse	csb	pp	endif_or_else_without_ifdef_csbcs	e					Endif-or-else-without ifdef at line @
cse	csb	prim	z_in_prim_inst_csbcs	e					z in primitive instantiation at line @
cse	csb	prts	prts_out_of_range_csbcs	e					Parameter @[@ : @]part select is out of range at line @
cse	csb	prts	ill_prts_inst_array_csbcs	e					Illegal value for part select of instance array 'name' at line @
cse	csb	prts	const_prts_contains_non_const_selector_csbcs	e					Constant part select @ contains a non-constant selector @ at line @
cse	csb	prts	bus_index_prts_for_var_out_of_range_csbcs	e					Bus index @ integer of part select [@:@] for variable @ out of range at line @
cse	csb	prts	bus_prts_for_var_out_of_range_csbcs	e					Bus part select [@:@] for variable @ out of range at line @
cse	csb	prts	bus_prts_index_out_of_name_for_var_csbcs	e					Bus part select [@:@] index @ out of range for variable @ at line @
cse	csb	prts	ill_token_in_prts_csbcs	e					Illegal token in part select @ at line @
cse	csb	prts	incomplete_prts_specification_csbcs	e					Incomplete part select specification @ at line @
cse	csb	prts	ill_index_in_prts_csbcs	e					Illegal index in part select @ at line @

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cse	csb	prts	negative_index_in_prts_not_allowed_csbcs	e					Negative index in part select @ not allowed at line @
cse	csb	prts	prts_index_order_reversed_csbcs	e					Part select index order reversed [@ : @] [@ : @] should be [@ : @] at line @
cse	csb	prts	index_vec_over_max_size_csbcs	w					Vector index @ exceeds the size of the vector. Index truncated at line @
cse	csb	prts	x_or_z_in_vec_bit_select_index_csbcs	e					x or z in vector bit select index at line @
cse	csb	sdir	ignored_synopsis_csdir_csstmt_csbcd	w					Ignored a synopsis case directive which is not applied to a Case statement at line @
cse	csb	sdir	ignored_synopsis_csdir_miss_end_csbcd	w					Ignored a synopsis case directive which is missing the end<directive> at line @
cse	csb	simr	inefficient_op_not_a_power_of_2_csbcs	e					Division/modulus by a number not a power of 2. Inefficient simulation operation. at line @
cse	csb	simr	simr_multiple_init_blk_force_csbcs	w					Multiple initial blocks force @. Unpredictable simulation result at line @
cse	csb	snsl	incomplete_snsl_csbcs	w					Incomplete sensitivity list. @ is not in the sensitivity list. at line @
cse	csb	snsl	edge_sns_process_contains_data_pin_snsl_csbcs	e					Edge sensitive process contains a data pin @ in the sensitivity list at line @
cse	csb	snsl	unsupp_expr_in_snsl_csbcs	w					Unsupported Expression type @ in sensitivity list ' at line @
cse	csb	snsl	partial_bus_decl_width_csbcs	e	?				partial bus @ declared with width @ width @ at line @
cse	csb	snsl	contains_inst_name_csbcs	e					Contains instance name @ at line @
cse	csb	stmt	null_not_allowed_stmt_csbcs	e					Null statement is not allowed here at line @
cse	csb	stmt	stmt_ill_accept_only_net_reg_mem_csbcs	e					Illegal type @ can only accept net, reg, memory at line @
cse	csb	stmt	stmt_ill_accept_only_port_reg_mem_csbcs	e					Illegal type @ can only accept port, reg, memory at line @
cse	csb	stmt	stmt_ill_accept_only_signal_reg_mem_csbcs	e					Illegal type @ can only accept signal, reg, memory at line @
cse	csb	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_csbcs	e					Arithmetic operator RHS has one less bit than the LHS at line @
cse	csb	stmt	ar_op_unequal_lhs_rhs_csbcs	e					Arithmetic operator unequal width LHS and RHS at line @
cse	csb	stmt	ar_op_unequal_var_on_rhs_csb	e					Arithmetic operator unequal width variables @ on RHS at line @
cse	csb	stmt	empty_stmt_csb	e					Empty-statement at line @
cse	csb	syst	return_var_of_user_used_as_rhs_csbcs	w					Return variable of user system task is used as a RHS variable at line @
cse	csb	task	ask_var_not_decl_csbcs	e					Variable @ used but not declared at line @
cse	csb	task	too_few_arg_to_task_csbcs	e					Too few arguments passed to task @ at line @
cse	csb	tri	instance_not_tri_state_device_csbcs	e					Instance name is not a tri-state device at line @
cse	csb	tri	unsupp_gate_type_tristate_csbcs	e					Unsupported gate type @ used for tristate at line @
cse	csb	tri	tri_not_desgn_gate_contention_csbcs	e					Tristate not designed correctly gate @ can cause contention at line @
cse	csb	tri	unsupp_type_instance_tri_csbcs	e					Unsupported type instance type used for tristate @ at line @
cse	csb	tri	incorrect_cont_assign_stmt_tri_gate_csbcs	e					Incorrect continuous assign statement for tristate gate @ at line @
cse	csb	tri	const_assign_to_multidriven_net_csbcs	e					Constant (constiznt) assigned to multi-driven Net @ at line @

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cse	csb	tri	const_assign_to_multidriven_port_csbcs	e					Constant (constiznt) assigned to multi-driven Port @ at line @
cse	csb	tri	const_assign_to_multidriven_signal_csbcs	e					Constant (constiznt) assigned to multi-driven Signal @ at line @
cse	csb	tri	unsupp_expr_for_tri_csbcs	e					Unsupported Expression type @ for tristate at line @
cse	csb	vec	vec_invalid_csbcs	e					Vector @ is invalid. at line @
cse	csb	vec	vec_mod_not_exist_csbcs	e					Vector @ module name does not exist at line @
cse	csb	vec	vec_ent_not_exist_csbcs	e					Vector @ entity name does not exist at line @
cse	csb	vec	vec_unit_not_exist_csbcs	e					Vector @ unit name does not exist at line @
cse	csb	vec	vec_not_contain_data_sig_csbcs	e					Vector @ does not contain any data signals at line @
cse	csb	vec	vec_not_contain_clk_sig_csbcs	e					Vector @ does not contain a clock signal at line @
cse	csb	vec	vec_not_contain_rst_sig_csbcs	e					Vector @ does not contain a reset signal at line @
cse	csb	vec	vec_stim_not_contain_input_ports_csbcs	e					Vector @ which is a stimulus vector does not contain any input ports at line @
cse	csb	vec	vec_expect_not_contain_outputs_ports_csbcs	e					Vector @ which is an expect vector does not contain any output ports at line @
cse	csb	vec	vec_is_missing_the_csbcs	e					Vector @ is missing the @ at line @
cse	csb	vec	vec_dtsig_not_found_csbcs	e					Vector @ data signals @ not found at line @
cse	csb	vec	vec_clk_sig_not_found_csbcs	e					Vector @ clock signal @ not found at line @
cse	csb	vec	vec_rst_sig_not_found_csbcs	e					Vector @ reset signal @ not found at line @
cse	csb	vec	vec_stim_input_port_not_found_csbcs	e					Vector @ stimulus vector input port @ not found at line @
cse	csb	vec	vec_output_port_not_found_csbcs	e					Vector @ output port @ not found at line @
cse	csc	ase	arch_state_el_mod_not_exist_csccs	e					Architectural state element @ module @ does not exist at line @
cse	csc	ase	arch_state_el_ent_not_exist_csccs	e					Architectural state element @ entity @ does not exist at line @
cse	csc	ase	arch_state_el_unit_not_exist_csccs	e					Architectural state element @ unit @ does not exist at line @
cse	csc	ase	arch_state_el_missi_clk_name_csccs	e					Architectural state element @ is missing the clock name at line @
cse	csc	ase	arch_state_el_miss_mem_name_csccs	e					Architectural state element @ is missing the memory name at line @
cse	csc	ase	arch_state_el_miss_the_csccs	e					Architectural state element @ is missing the @ at line @
cse	csc	ase	arch_state_el_miss_rst_name_csccs	e					Architectural state element @ is missing the reset name at line @
cse	csc	ase	arch_state_el_evtrigg_miss_ev_name_csccs	e					Architectural state element @ is event triggered and is missing the event name at line @
cse	csc	ase	arch_state_el_clk_name_not_found_csccs	e					Architectural state element @ clock name @ not found at line @
cse	csc	ase	arch_state_el_mem_name_not_found_csccs	e					Architectural state element @ memory name @ not found at line @
cse	csc	ase	arch_state_el_not_found_csccs	e					Architectural state element @ arch_state_name @ not found at line @
cse	csc	assn	x_in_rhs_of_assihnment_cscc	e					x in rhs of assignment at line @
cse	csc	assn	z_in_rhs_of_assn_default_csi_cscc	e					x in rhs of assignement in defaultCase item at line @
cse	csc	assn	z_in_rhs_of_assn_csccs	e					z in rhs of assignement at line @
cse	csc	assn	unequal_length_lhs_rhs_csccs	e					Unequal length LHS and

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									RHS at line @
cse	csc	assn	unequal_length_lhs_rhs_off_one_bit_csccs	e					Unequal length LHS and RHS off by one bit at line @
cse	csc	ccd	ccd_cdir_must_be_cst_expr_csccs	e				x	CSL directive size must be constant Expression at line @
cse	csc	ccd	clk_dir_not_applied_to_dsgn_csccs	w				x	CSL clock directive not applied to design. Could not find clock at line @
cse	csc	ccd	csl_filter_unused_csccs	w				x	CSL message filter @ not found. Filter @ is unused. at line @
cse	csc	ccd	csl_mess_not_filtered_csccs	w				x	CSL message @ can not be filtered. Filter @ is unused. at line @
cse	csc	ccd	error_csdir_not_found_csccs	e				x	Error CSL directive @ not found. Error @ is unused. at line @
cse	csc	chrs	ill_val_chrs_csc	e					Illegal value @ at line @
cse	csc	clk	clk_name_not_found_cdir_csccs	e				x	Clock name not found in cslc directive at line @
cse	csc	clk	expr_sunj_to_different_clk_phases_csccs	e					Expression subject to different clock phases at line @
cse	csc	csi	z_csi_not_in_casez_csc	e					z case item not in casez at line @
cse	csc	csi	noncstn_rep_in_conc_csccs	e					Non-constant repeator in concatenation at line @
cse	csc	decl	decl_array_over_max_size_csccs	e					Array @ exceeds maximum size limit at line @
cse	csc	dely	x_or_z_in_dely_csccs	e					x or z in delay at line @
cse	csc	dmsn	mem_prts_index_out_of_range_for_mem_csccs	e					Memory part select [@:@] index @ out range for memory @ at line @
cse	csc	dmsn	dime_select_for_mem_missing_csccs	e					Select for memory @ missing at line @
cse	csc	dmsn	dime_index_out_of_bounds_for_mem_csccs	e					Index <index> out of bounds for memory @. Range [@: @] at line @
cse	csc	dmsn	dime_prts_out_of_bounds_for_net_csccs	e					Part select [@ : @] out of bounds for net @. Range [@ : @] at line @
cse	csc	dmsn	dime_prts_out_of_bounds_for_port_csccs	e					Part select [@ : @] out of bounds for port @. Range [@ : @] at line @
cse	csc	dmsn	dime_prts_out_of_bounds_for_sig_csccs	e					Part select [@ : @] out of bounds for signal @. Range [@ : @] at line @
cse	csc	dmsn	dime_prts_reg_csccs	e					Part select [@ : @] reg @. Range [@ : @] at line @
cse	csc	drvc	incompatible_drvc_for_net_csccs	e					Incompatible drivers for Net @ at line @
cse	csc	drvc	incompatible_drvc_for_port_csccs	e					Incompatible drivers for Port @ at line @
cse	csc	drvc	incompatible_drvc_for_sig_csccs	e					Incompatible drivers for Signal @ at line @
cse	csc	drvc	drvc_multiple_drive_net_partially_overlap_csccs	e					Multiple drive Net partially overlap at line @
cse	csc	drvc	drvc_multiple_drive_port_partially_overlap_csccs	e					Multiple drive Port partially overlap at line @
cse	csc	drvc	drvc_multiple_drive_sig_partially_overlap_csccs	e					Multiple drive Signal partially overlap at line @
cse	csc	dsgn	dsgn_top_mod_cannot_id_csccs	e					Top module @ cannot be identified at line @
cse	csc	dsgn	dsgn_top_entity_cannot_id_csccs	e					Top entity @ cannot be identified at line @
cse	csc	dsgn	dsgn_top_unit_cannot_id_csccs	e					Top unit @ cannot be identified at line @
cse	csc	dsgn	unit_dsgn_cycle_not_spanning_tree_csccs	e					Unit design hierarchy contains a cycle. Hierarchy is not a spanning tree. at line @
cse	csc	dsgn	cse_csc_dsgn_has_parent	e					Parent already set at line @ at line @
cse	csc	dsgn	cse_csc_dsgn_empty_list	w					List is empty, no signals added to unit at line @
cse	csc	dsgn	cse_csc_dsgn_empty_group	w					Group is empty at line @
cse	csc	expr	expr_prts_indices_1bit_var_csccs	e					Part select indices 1-bit variable at line @
cse	csc	expr	expr_prts_must_be_cst_expr_csccs	e					Part select specifier Expression must be constant Expression at line @
cse	csc	expr	not_const_expr_csccs	e					Repetition multiplier in concatenation is not a constant Expression at

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									line @
cse	csc	expr	ill_bit_select_expr_csccs	e					Illegal bit select expression @ at line @
cse	csc	expr	repetition_multiplier_in_conc_not_const_expr_csccs	w					Repetition multiplier in concatenation is not a constant Expression at line @
cse	csc	expr	int_operand_not_1_bit_csccs	w					Logic operator has integer operands instead of 1-bit operands at line @
cse	csc	expr	unsupp_expr_csccs	w					Unsupported Expression type @ at line @
cse	csc	expr	unsupp_operator_csccs	w					Unsupported operator type @ at line @
cse	csc	expr	use_of_sg_bit_const_csccs	w					Use of single bit constant at line @
cse	csc	expr	unary_op_in_comparison_csccs	e					Unary op used in comparison at line @
cse	csc	expr	x_or_z_in_cond_expr_csccs	e					x or z in conditional expression at line @
cse	csc	expr	zero_in_rep_in_conc_csccs	e					Zero repeator in concatenation at line @
cse	csc	expr	expr_in_mod_port_dir_csccs	e					Expression @ in module port dir at line @
cse	csc	expr	expr_in_ent_port_dir_csccs	e					Expression @ in entity port dir at line @
cse	csc	expr	expr_in_sig_port_dir_csccs	e					Expression @ in unit port dir at line @
cse	csc	expr	expr_in_inst_csccs	e					Expression @ in inst i@ at line @
cse	csc	expr	expr_operator_operands_unequal_lenght_csccs	e					Expression operator @ operands @ unequal length at line @
cse	csc	file	cannot_open_filter_specification_file_csccs	e					Cannot open filter specification file @ at line @
cse	csc	file	filter_specification_file_missing_csccs	e					Filter specification file name @ is missing at line @
cse	csc	file	mismatch_mod_file_name_csccs	e					Mismatch between module name @ and file name @ at line @
cse	csc	file	mismatch_ent_file_name_csccs	e					Mismatch between entity name @ and file name @ at line @
cse	csc	file	mismatch_sig_file_name_csccs	e					Mismatch between signal name @ and file name @ at line @
cse	csc	func	port_not_output_func_csccs	e					Port @ direction cannot be output at line @
cse	csc	func	too_many_arg_to_func_csccs	e					Too many arguments passed to function @ at line @
cse	csc	func	too_few_arg_to_func_csccs	e					Too few arguments passed to function @ at line @
cse	csc	func	undefined_func_csccs	e					Undefined function @ at line @
cse	csc	func	funct_expr_cannot_expnaded_csccs	e					Function expression @ cannot be expanded at line @
cse	csc	func	funct_not_used_in_expr_csccs	w					Function @ is not being used in an Expression at line @
cse	csc	func	func_decl_csccs	w					Function Declaration @ already declared as another type at line @
cse	csc	func	cse_csc_func_args	e					Invalid arguments at line @
cse	csc	func	cse_csc_func_illegal_state	e					Illegal state for this method @ call at line @
cse	csc	func	cse_csc_func_wrong_arg_nr	e					Wrong number of arguments at line @
cse	csc	hid	cannot_locate_hier_id_hid_csccs	e					Can't locate hierarchical identifier @ at line @
cse	csc	hid	ref_minst_found_in_expr_hid_cscs	e					References a module instance @ found in an Expression hid at line @
cse	csc	hid	ref_entity_found_in_expr_hid_csccs	e					References a entity instance @ found in an Expression hid at line @
cse	csc	hid	ref_unit_found_in_expr_hid_csccs	e					References a unit instance @ found in an Expression hid at line @
cse	csc	hid	hid_reference_not_found_csccs	e					@ reference not found at line @
cse	csc	hid	mifc_in_hid_not_exist_csccs	e					Module instance @ in hid does not exist at line @
cse	csc	hid	entity_instance_in_hid_not_exist_csccs	e					Entity instance @ in hid

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									does not exist at line @
cse	csc	hid	unit_instance_in_hid_not_exist_csccs	e					Unit instance @ in hid does not exist at line @
cse	csc	hid	mod_found_in_path_in_dsgn_csccs	e					Module @ found in path @ in the design at line @
cse	csc	hid	enity_found_in_path_in_dsgn_csccs	e					Entity @ found in path @ in the design at line @
cse	csc	hid	unit_found_in_path_in_dsgn_csccs	e					Unit @ found in path @ in the design at line @
cse	csc	hid	hierarchical_id_path_contains_func_csc	e					Hierarchical ID @ path contains a function at line @
cse	csc	hid	cse_csc_hid_illegal	e					Illegal hierarchical ID @ at line @
cse	csc	id	cse_csc_id_illegal	e					Illegal identifier name @ at line @
cse	csc	init	assn_mem_in_init_blk_csccs	e					Assign memory in initial block at line @
cse	csc	inst	inst_duplicate_mod_name_csccs	e					Duplicate port @ in the port list for module @ at line @
cse	csc	inst	inst_duplicate_entity_name_csccs	e					Duplicate port @ in the port list for entity @ at line @
cse	csc	inst	inst_duplicate_unit_name_csccs	e					Duplicate port @ in the port list for unit @ at line @
cse	csc	inst	ill_mod_inst_name_csccs	e					Illegal module instance @ at line @
cse	csc	inst	ill_entity_inst_name_csccs	e					Illegal entity instance @ at line @
cse	csc	inst	ill_unit_inst_name_csccs	e					Illegal unit instance @ at line @
cse	csc	inst	inst_name_defined_mod_cscc	e					Instance name @ already defined in this module at line @
cse	csc	inst	inst_name_defined_ent_cscc	e					Instance name @ already defined in this entity at line @
cse	csc	inst	inst_name_defined_unit_cscc	e					Instance name @ already defined in this unit at line @
cse	csc	inst	inst_too_many_bits_csccs	e					Too many bits for port @ of instance array @, formal @, actual @ at line @
cse	csc	inst	inst_port_not_connected_var_csccs	e					Port 'port' of instance array 'array' is not connected to variable at line @
cse	csc	inst	inst_insufficient_bits_csccs	e					Insufficient bits for port 'port' of instance array 'array ', formal number, actual number at line @
cse	csc	inst	inst_mod_name_not_defined_csccs	e					Module name not defined at line @
cse	csc	inst	inst_ent_name_not_defined_csccs	e					Entity name not defined at line @
cse	csc	inst	inst_unit_name_not_defined_csccs	e					Unit name not defined at line @
cse	csc	inst	many_mod_inst_param_assign_csccs	e					Too many module instance parameter assignments (number > rrumber) at line @
cse	csc	inst	many_entity_inst_param_assign_csccs	e					Too many entity instance parameter assignments (number > rrumber) at line @
cse	csc	inst	many_unit_inst_param_assign_csccs	e					Too many unit instance parameter assignments (number > rrumber) at line @
cse	csc	inst	complexexpr_cannot_mapped_inout_port_csccs	e					Complex Expression @ cannot be mapped to inout port @ at line @
cse	csc	inst	complexexpr_cannot_mapped_unknown_port_csccs	e					Complex Expression @ cannot be mapped to unknown type port @ at line @
cse	csc	inst	netdecl_contains_ill_prts_csccs	e					Net Declaration [@: @] contains an illegal part select at line @
cse	csc	inst	regdecl_contains_ill_prts_csccs	e					Reg Declaration [@ : @] contains an illegal part select at line @
cse	csc	inst	complex_expr_inst_parent_module_csccs	e					Complex actual Expression associated with port @ of module @ instantiated in parent module at line @
cse	csc	inst	complex_expr_inst_entity_parent_module_csccs	e					Complex actual

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									Expression associated with port @ of entity @ instantiated in parent module at line @
cse	csc	inst	complex_expr_inst_unit_parent_module_csccs	e					Complex actual Expression associated with port @ of unit @ instantiated in parent module at line @
cse	csc	inst	inst_mod_output_port_width_csccs	e					Mod @ Output port @ width mismatch, actual-width (port-width) at line @
cse	csc	inst	inst_entity_output_port_width_csccs	e					Entity @ Output port @ width mismatch, actual-width (port-width) at line @
cse	csc	inst	inst_unit_output_port_width_csccs	e					Unit @ Output port @ width mismatch, actual-width (port-width) at line @
cse	csc	inst	inst_mod_input_port_width_csccs	e					Mod @ Input port @ width mismatch, actual-width (port-width) at line @
cse	csc	inst	inst_entity_input_port_width_csccs	e					Entity @ Intput port @ width mismatch, actual-width (port-width) at line @
cse	csc	inst	inst_unit_input_port_width_csccs	e					Unit @ Input port @ width mismatch, actual-width (port-width) at line @
cse	csc	inst	inst_mod_not_define_csccs	e					Module not defined at line @
cse	csc	inst	inst_entity_not_define_csccs	e					Entity not defined at line @
cse	csc	inst	inst_unit_not_define_csccs	e					Unit not defined at line @
cse	csc	inst	mifc_port_actual_formal_width_mismatch_csccs	w					Module @ instance @ port @ width mismatch, actual width @ formal width @ at line @
cse	csc	inst	ent_port_actual_formal_width_mismatch_csccs	w					Entity @ instance @ port @ width mismatch, actual width @ formal width @ at line @
cse	csc	inst	unit_port_actual_formal_width_mismatch_csccs	w					Unit @ instance @ port @ width mismatch, actual width @ formal width @ at line @
cse	csc	inst	inst_differs_in_case_from_mod_csccs	e					Instance name @ differs in case from module name @ at line @
cse	csc	inst	inst_differs_in_case_from_ent_csccs	e					Instance name @ differs in case from entity name @ at line @
cse	csc	inst	inst_differs_in_case_from_sig_csccs	e					Instance name @ differs in case from signal name @ at line @
cse	csc	loop	undet_init_value_loop_csccs	e					Unable to determine init value for loop at line @
cse	csc	loop	undet_limit_loop_csccs	e					Unable to determine limit for loop at line @
cse	csc	loop	loop_bounds_calculated_int_csccs	w					Loop bounds are calculated to be integer @, check that this is correct at line @
cse	csc	loop	expr_lhs_contains_var_bit_select_csccs	w					Expression in lhs of assignment contains a variable bit select at line @
cse	csc	loop	loop_bounds_not_const_csc	w					Loop bounds are non-constant at line @
cse	csc	loop	loop_ctrl_init_expr_not_const_csccs	w					Non-constant loop bound. Loop control variable initialization Expression is not a constant Expression at line @
cse	csc	loop	loop_term_expr_not_const_csccs	w					Non-constant loop bound. loop terminating Expression could not be evaluated to a constant at line @
cse	csc	loop	init_expr_reset_by_var_csccs	e					Non-constant loop bound. initializing Expression reset by variable at line @
cse	csc	loop	loop_ctrl_var_1_bit_wide_csccs	w					The loop control variable @ is one bit wide. Check the loop control variable

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									Declaration. at line @
cse	csc	mdb	bad_mdb_net_csccs	e					Bad multi-driven Net @ at line @
cse	csc	mdb	bad_mdb_port_csccs	e					Bad multi-driven Port @ at line @
cse	csc	mdb	bad_mdb_signal_csccs	e					Bad multi-driven Signal @ at line @
cse	csc	mdb	unsupp_comp_mdb_net_csccs	e	?				Unsupported component type @ driving in multi-driven Net name at line @
cse	csc	mdb	unsupp_comp_mdb_port_csccs	e	?				Unsupported component type @ driving in multi-driven Port name at line @
cse	csc	mdb	unsupp_comp_mdb_signal_csccs	e	?				Unsupported component type @ driving in multi-driven Signal name at line @
cse	csc	mdb	unsupp_comp_drive_mdb_csccs	e	?				Unsupported component type @ driving multi-driven Net natne at line @
cse	csc	mdb	unsupp_comp_drive_mdb_port_csccs	e	?				Unsupported component type @ driving multi-driven Port natne at line @
cse	csc	mdb	unsupp_comp_drive_mdb_signal_csccs	e	?				Unsupported component type @ driving multi-driven Signal natne at line @
cse	csc	mdb	mdb_net_driven_by_trns_csccs	e					Multiply driven Net driven by transistor primitive type @ at line @
cse	csc	mdb	mdb_port_driven_by_trns_csccs	e					Multiply driven Port driven by transistor primitive type @ at line @
cse	csc	mdb	mdb_sig_driven_by_trns_csccs	e					Multiply driven Signal driven by transistor primitive type @ at line @
cse	csc	mdb	mdb_unsupp_comp_drvs_net_csccs	e					Unsupported component type driving Net drives Net connected to multi-driven Net at line @
cse	csc	mdb	mdb_unsupp_comp_drvs_port_csccs	e					Unsupported component type driving Port drives Port connected to multi-driven Port at line @
cse	csc	mdb	mdb_unsupp_comp_drvs_sig_csccs	e					Unsupported component type driving Signal drives Signal connected to multi-driven Signal at line @
cse	csc	mdb	mdb_incompatible_net_drives_multiple_net_csccs	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Net at line @
cse	csc	mdb	mdb_incompatible_port_drives_multiple_port_csccs	e					Incompatible driver driving tandem Port drives Port connected to multi-driven Port at line @
cse	csc	mdb	mdb_incompatible_sig_drives_multiple_sig_csccs	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Port at line @
cse	csc	mdb	mdb_unsupp_LHS_concatenation_csccs	e					Unsupported LHS concatenation in multi-drive 'device at line @
cse	csc	mdb	mdb_bus_has_too_many_drivers_csccs	e					Bus has too many drivers. at line @
cse	csc	mdb	mdb_always_blk_drive_csccs	w					Multiple always blocks drive name @ at line @
cse	csc	mdb	nontri_gate_drives_mdb_net_csccs	w					non-tri-state gate drives multi-driven Net at line @
cse	csc	mdb	nontri_gate_drives_mdb_port_csccs	w					non-tri-state gate drives multi-driven Port at line @
cse	csc	mdb	nontri_gate_drives_mdb_sig_csccs	w					non-tri-state gate drives multi-driven Signal at line @
cse	csc	mem	mem_ref_without_index_csccs	e					Memory @ referenced without index through hierarchical ID @ at line @
cse	csc	mifc	port_identifier_mifc_csccs	e					Port @ at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	csc	mifc	mod_output_wire_redecl_reg_csccs	e					Module @ output port re-declared as type reg after use as implicitly declared wire at line @
cse	csc	mifc	entity_output_wire_redecl_reg_csccs	e					Entity @ output port re-declared as type reg after use as implicitly declared wire at line @
cse	csc	mifc	unit_output_wire_redecl_reg_csccs	e					Unit @ output port re-declared as type reg after use as implicitly declared wire at line @
cse	csc	mifc	output_port_is_mem_type_mifc_csccs	e					Output port @ is memory type at line @
cse	csc	mifc	mifc_inout_port_is_mem_type_csccs	e					Inout port @ is memory type at line @
cse	csc	mifc	mod_output_port_mismatch_actual_witdh_csccs	w					Module @ output port @ formal to actual width mismatch at line @
cse	csc	mifc	ent_output_port_mismatch_actual_witdh_csccs	w					Entity @ output port @ formal to actual width mismatch at line @
cse	csc	mifc	unit_output_port_mismatch_actual_witdh_csc	w					Unit @ output port @ formal to actual width mismatch at line @
cse	csc	mifc	port_name_different_in_upper_lower_case_csccs	e					Port name @ different in upper lower case at line @
cse	csc	mifc	port_not_def_in_iodecl_csccs	e					Port @ not defined in ioDeclaration at line @
cse	csc	mifc	port_not_def_in_portl_csccs	e					Port @ not defined in port list at line @
cse	csc	mifc	port_wiredecl_mismatch_csccs	e					Port @ wireDeclaration mismatch at line @
cse	csc	mifc	pos_based_null_inst_port_csccs	e					Position based null instance port at line @
cse	csc	mifc	last_portdecl_contains_trailcomma_csccs	e					Last portDeclaration contains a trailing comma at line @
cse	csc	mins	mins_expr_incompatible_type_csccs	e					Expression @ has an incompatible argument type @ with the port at line @
cse	csc	mins	mins_mod_not_exist_csccs	e					Module @ does not exist at line @
cse	csc	mins	mins_entity_not_exist_csccs	e					Entity @ does not exist at line @
cse	csc	mins	mins_unit_not_exist_csccs	e					Unit @ does not exist at line @
cse	csc	mod	dup_declar_name_mod_cscs	e					Duplicate Declaration of port @ at line @
cse	csc	mod	ill_mod_name_csccs	e					Illegal module @ at line @
cse	csc	mod	ill_mod_entity_name_csccs	e					Illegal entity @ at line @
cse	csc	mod	ill_mod_unit_name_csccs	e					Illegal unit @ at line @
cse	csc	mod	mod_mult_decl_string_csccs	e					Multiple Declarations of string detected in module @ at line @
cse	csc	mod	mod_entity_mult_decl_string_csccs	e					Multiple Declarations of string detected in entity @ at line @
cse	csc	mod	mod_unit_mult_decl_string_csccs	e					Multiple Declarations of string detected in unit @ at line @
cse	csc	mod	mod_mult_def_cscsc	e					Module @ defined in multiple places at line @
cse	csc	mod	mod_ent_mult_def_csccs	e					Entity @ defined in multiple places at line @
cse	csc	mod	mod_unit_mult_def_csccs	e					Unit @ defined in multiple places at line @
cse	csc	mod	mod_no_module_found_csccs	e					No modules found at line @
cse	csc	mod	mod_no_entity_found_csccs	e					No entity found at line @
cse	csc	mod	mod_no_unit_found_csccs	e					No unit found at line @
cse	csc	mod	failed_find_mod_csccs	e					Failed to find module @ at line @
cse	csc	mod	failed_find_entity_csccs	e					Failed to find entity @ at line @
cse	csc	mod	failed_find_unit_csccs	e					Failed to find unit @ at line @
cse	csc	mod	empty_mod_csccs	e					Empty module at line @
cse	csc	mod	empty_ent_csccs	e					Empty entity at line @
cse	csc	mod	empty_unit_csccs	e					Empty unit at line @
cse	csc	net	net_implicit_wire_redecl_reg_csccs	e					Implicitly declared as a wire @ re-declared as a reg @. at line @
cse	csc	net	undecl_net_in_mod_csccs	e					Undeclared net @ in module @ at line @
cse	csc	net	undecl_port_in_mod_csccs	e					Undeclared port @ in module @ at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	csc	net	undecl_sig_in_mod_csccs	e					Undeclared signal @ in module @ at line @
cse	csc	net	undecl_net_in_ent_csccs	e					Undeclared net @ in entity @ at line @
cse	csc	net	undecl_port_in_ent_csccs	e					Undeclared port @ in entity @ at line @
cse	csc	net	undecl_sig_in_ent_csccs	e					Undeclared signal @ in entity @ at line @
cse	csc	net	undecl_net_in_sig_csccs	e					Undeclared net @ in signal @ at line @
cse	csc	net	undecl_port_in_sig_csccs	e					Undeclared port @ in signal @ at line @
cse	csc	net	undecl_sig_in_sig_csccs	e					Undeclared signal @ in signal @ at line @
cse	csc	net	port_used_prior_to_decl_csccs	e					Port @ used prior toDeclaration at line @
cse	csc	net	1bit_with_prts_csccs	e					1-bit with part select at line @
cse	csc	netd	ill_decl_vec_csccs	e					Illegal Declaration of vector @ at line @
cse	csc	nett	nett_ill_reg_name_csccs	e					Illegal register @ at line @
cse	csc	nett	nett_ill_net_name_csccs	e					Illegal net @ at line @
cse	csc	nett	nett_ill_port_name_csccs	e					Illegal port @ at line @
cse	csc	nett	nett_ill_signal_name_csccs	e					Illegal signal @ at line @
cse	csc	nett	net_scalar_vect_nett_csccs	e					Net declared as both scalar and vector at line @
cse	csc	nett	port_scalar_vect_nett_csccs	e					Port declared as both scalar and vector at line @
cse	csc	nett	signal_scalar_vect_nett_csccs	e					Signal declared as both scalar and vector at line @
cse	csc	nett	hot_mux_not_use_bus_connection_net_csccs	e					One hot mux can not be used for bus connection between modules Net @ at line @
cse	csc	nett	hot_mux_not_use_bus_connection_port_csccs	e					One hot mux can not be used for bus connection between modules Port @ at line @
cse	csc	nett	hot_mux_not_use_bus_connection_sig_csccs	e					One hot mux can not be used for bus connection between modules Signal @ at line @
cse	csc	num	not_allowed_width0_num_csccs	e					Width 0 not allowed for sized number at line @
cse	csc	num	real_num_not_allowed_csccs	e					Real numbers not allowed at line @
cse	csc	num	found_x_z_in_num_literal_csccs	e					Found x and/or z value in number literal at line @
cse	csc	num	too_many_digits_in_sized_num_csccs	w					Number of digits exceeds the width in a sized number at line @
cse	csc	num	divide_by_zero_num_csccs	e					Divide by zero at line @
cse	csc	num	child_mod_inst_parent_mod_csccs	e					Child module @ instantiates parent module @ at line @
cse	csc	num	child_ent_inst_parent_ent_csccs	e					Child entity @ instantiates entity module @ at line @
cse	csc	num	child_sig_inst_parent_sig_csccs	e					Child signal @ instantiates signal module @ at line @
cse	csc	num	int_decl_incorrect_csccs	e					Integer Declaration incorrect at line @
cse	csc	num	int_var_indexed_csccs	e					Integer variable inedexed at line @
cse	csc	parm	ill_parm_identifier_csccs	e					Illegal parameter @ at line @
cse	csc	parm	value_of_parm_OS_platform_dependent_csccs	w					Parameter select width > 32. The value is OS and platform dependent at line @
cse	csc	parm	parm_redefined_csccs	w					Parameter @ redefined at line @
cse	csc	port	ill_formal_port_name_csccs	e					Illegal formal port @ at line @
cse	csc	pp	text_redefined_replaced_csccs	w					Text macro redefined and replaced @. Previous definition filename, line number @ New definition filename, line number @ at line @
cse	csc	pp	endif_or_else_without_ifdef_csccs	e					Endif-or-else-without ifdef at line @
cse	csc	prim	z_in_prim_inst_csccs	e					z in primitive instantiation at line @
cse	csc	prts	prts_out_of_range_csccs	e					Parameter @[@ : @]part

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									select is out of range at line @
cse	csc	prts	ill_prts_inst_array_csccs	e					Illegal value for part select of instance array 'name' at line @
cse	csc	prts	const_prts_contains_non_const_selector_csccs	e					Constant part select @ contains a non-constant selector @ at line @
cse	csc	prts	bus_index_prts_for_var_out_of_range_csccs	e					Bus index @ integer of part select [@:@] for variable @ out of range at line @
cse	csc	prts	bus_prts_for_var_out_of_range_csccs	e					Bus part select [@:@] for variable @ out of range at line @
cse	csc	prts	bus_prts_index_out_of_name_for_var_csccs	e					Bus part select [@:@] index @ out of range for variable @ at line @
cse	csc	prts	ill_token_in_prts_csccs	e					Illegal token in part select @ at line @
cse	csc	prts	incomplete_prts_specification_csccs	e					Incomplete part select specification @ at line @
cse	csc	prts	ill_index_in_prts_csccs	e					Illegal index in part select @ at line @
cse	csc	prts	negative_index_in_prts_not_allowed_csccs	e					Negative index in part select @ not allowed at line @
cse	csc	prts	prts_index_order_reversed_csccs	e					Part select index order reversed [@ : @] [@ : @] should be [@ : @] at line @
cse	csc	prts	index_vec_over_max_size_csccs	w					Vector index @ exceeds the size of the vector. Index truncated at line @
cse	csc	prts	x_or_z_in_vec_bit_select_index_csccs	e					x or z in vector bit select index at line @
cse	csc	scop	cse_csc_not_scope_holder	e					@ cannot be a scope holder at line @
cse	csc	scop	cse_csc_scop_id_already_defined	e					Id @ already defined in scope @ at line @
cse	csc	sdir	ignored_synopsis_csdir_csstmt_csccd	w					Ignored a synopsis case directive which is not applied to a Case statement at line @
cse	csc	sdir	ignored_synopsis_csdir_miss_end_csccd	w					Ignored a synopsis case directive which is missing the end<directive> at line @
cse	csc	simr	inefficient_op_not_a_power_of_2_csccs	e					Division/modulus by a number not a power of 2. Inefficient simulation operation. at line @
cse	csc	simr	simr_multiple_init_blk_force_csccs	w					Multiple initial blocks force @. Unpredictable simulation result at line @
cse	csc	snsl	incomplete_snsl_csccs	w					Incomplete sensitivity list. @ is not in the sensitivity list. at line @
cse	csc	snsl	edge_sns_process_contains_data_pin_snsl_csccs	e					Edge sensitive process contains a data pin @ in the sensitivity list at line @
cse	csc	snsl	unsupp_expr_in_snsl_csccs	w					Unsupported Expression type @ in sensitivity list ' at line @
cse	csc	snsl	partial_bus_decl_width_csccs	e	?				partial bus @ declared with width @ width @ at line @
cse	csc	snsl	contains_inst_name_csccs	e					Contains instance name @ at line @
cse	csc	stmt	illegal_LHS	e					LHS expression is illegal at line @
cse	csc	stmt	null_not_allowed_stmt_csccs	e					Null statement is not allowed here at line @
cse	csc	stmt	stmt_ill_accept_only_net_reg_mem_csccs	e					Illegal type @ can only accept net, reg, memory at line @
cse	csc	stmt	stmt_ill_accept_only_port_reg_mem_csccs	e					Illegal type @ can only accept port, reg, memory at line @
cse	csc	stmt	stmt_ill_accept_only_signal_reg_mem_csccs	e					Illegal type @ can only accept signal, reg, memory at line @
cse	csc	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_csccs	e					Arithmetic operator RHS has one less bit than the LHS at line @
cse	csc	stmt	ar_op_unequal_lhs_rhs_csccs	e					Arithmetic operator unequal width LHS and RHS at line @
cse	csc	stmt	ar_op_unequal_var_on_rhs_csc	e					Arithmetic operator

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									unequal width variables @ on RHS at line @
cse	csc	stmt	empty_stmt_csc	e					Empty-statement at line @
cse	csc	syst	return_var_of_user_used_as_rhs_csccs	w					Return variable of user system task is used as a RHS variable at line @
cse	csc	task	ask_var_not_decl_csccs	e					Variable @ used but not declared at line @
cse	csc	task	too_few_arg_to_task_csccs	e					Too few arguments passed to task @ at line @
cse	csc	tri	instance_not_tri_state_device_csccs	e					Instance name is not a tri-state device at line @
cse	csc	tri	unsupp_gate_type_tristate_csccs	e					Unsupported gate type @ used for tristate at line @
cse	csc	tri	tri_not_desgn_gate_contention_csccs	e					Tristate not designed correctly gate @ can cause contention at line @
cse	csc	tri	unsupp_type_instance_tri_csccs	e					Unsupported type instance type used for tristate @ at line @
cse	csc	tri	incorrect_cont_assign_stmt_tri_gate_csccs	e					Incorrect continuous assign statement for tristate gate @ at line @
cse	csc	tri	const_assign_to_multidriven_net_csccs	e					Constant (constiznt) assigned to multi-driven Net @ at line @
cse	csc	tri	const_assign_to_multidriven_port_csccs	e					Constant (constiznt) assigned to multi-driven Port @ at line @
cse	csc	tri	const_assign_to_multidriven_signal_csccs	e					Constant (constiznt) assigned to multi-driven Signal @ at line @
cse	csc	tri	unsupp_expr_for_tri_csccs	e					Unsupported Expression type @ for tristate at line @
cse	csc	vec	vec_invalid_csccs	e					Vector @ is invalid. at line @
cse	csc	vec	vec_mod_not_exist_csccs	e					Vector @ module name does not exist at line @
cse	csc	vec	vec_ent_not_exist_csccs	e					Vector @ entity name does not exist at line @
cse	csc	vec	vec_unit_not_exist_csccs	e					Vector @ unit name does not exist at line @
cse	csc	vec	vec_not_contain_data_sig_csccs	e					Vector @ does not contain any data signals at line @
cse	csc	vec	vec_not_contain_clk_sig_csccs	e					Vector @ does not contain a clock signal at line @
cse	csc	vec	vec_not_contain_rst_sig_csccs	e					Vector @ does not contain a reset signal at line @
cse	csc	vec	vec_stim_not_contain_input_ports_csccs	e					Vector @ which is a stimulus vector does not contain any input ports at line @
cse	csc	vec	vec_expect_not_contain_outputs_ports_csccs	e					Vector @ which is an expect vector does not contain any output ports at line @
cse	csc	vec	vec_is_missing_the_csccs	e					Vector @ is missing the @ at line @
cse	csc	vec	vec_dtsig_not_found_csccs	e					Vector @ data signals @ not found at line @
cse	csc	vec	vec_clk_sig_not_found_csccs	e					Vector @ clock signal @ not found at line @
cse	csc	vec	vec_rst_sig_not_found_csccs	e					Vector @ reset signal @ not found at line @
cse	csc	vec	vec_stim_input_port_not_found_csccs	e					Vector @ stimulus vector input port @ not found at line @
cse	csc	vec	vec_output_port_not_found_csccs	e					Vector @ output port @ not found at line @
cse	csp	ccd	CSL_out_ccd	e				x	CSL directive outside of module at line @
cse	csp	ccd	ill_pos_CSLC_ccd_mod_csc	e				x	Illegal position for CSLC directive in module name at line @
cse	csp	ccd	ill_pos_CSLC_ccd_ent_csc	e				x	Illegal position for CSLC directive in entity name at line @
cse	csp	ccd	ill_pos_CSLC_ccd_unit_csc	e				x	Illegal position for CSLC directive in unit name at line @
cse	csp	ccd	misplaced_csdir_ignored_cscs	e				x	Lower case directive in wrong location. Ignored at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	csp	clk	clk_file_cannot_open_cscs	e					Clock file @ cannot be opened at line @
cse	csp	clk	no_clk_source_specified_clk_cscs	e					No clock source specified clock @ at line @
cse	csp	cmdl	ill_cmdl_uselib_dir_path_cscs	e					Illegal 'uselib directory path @ no such directory at line @
cse	csp	cmnt	cse_csp_cmnt_miss_closing_cscs	e					/* comment missing closing */ at line @
cse	csp	csi	miss_char_case_cscs	e					Missing character @ at line @
cse	csp	expr	malformed_unary_expr_ccsp	e					Malformed unary Expression @ at line @
cse	csp	expr	malformed_binary_expr_ccsp	e					Malformed binary Expression @ at line @
cse	csp	expr	malformed_ternary_expr_ccsp	e					Malformed ternary Expression @ at line @
cse	csp	expr	expr_s_cse	e					Expression S at line @
cse	csp	expr	expr_found_reserved_word_cscs	e					Expected identifier but found reserved word @ at line @
cse	csp	expr	expr_concatenation_empty_cscs	e					Concatenation empty at line @
cse	csp	expr	ill_operator_expr_cscs	e					Illegal operator @ at line @
cse	csp	expr	ill_operand_expr_cscs	e					Illegal operand @ at line @
cse	csp	file	cannot_open_file_cscs	e					Cannot open file @ at line @
cse	csp	file	line_lenght_overflow_cscs	e					Line length overflow line_length @ at line @
cse	csp	file	environ_var_in_filel_cscs	e					Environ variable in file list at line @
cse	csp	func	fct_non_block	e					Function definition contains non-blocking assignment at line @
cse	csp	func	undefined_func_cscs	e					Undefined function @ at line @
cse	csp	inst	ill_mod_inst_name_cscs	e					Illegal module instance @ at line @
cse	csp	inst	ill_entity_inst_name_cscs	e					Illegal entity instance @ at line @
cse	csp	inst	ill_unit_inst_name_cscs	e					Illegal unit instance @ at line @
cse	csp	lib	not_open_lib_file_csc	e					Cannot open library file @ at line @
cse	csp	list	trail_comma_list_css	e					Trailing comma in parentheses enclosed list at line @
cse	csp	list	list_miising_comma_cscs	w					Missing comma between @ and name at line @
cse	csp	mem	unknown_latch_in_latch_array_decl_	e					Unknown latch type in latch-array declaration at line @
cse	csp	mifc	mifc_port_type_unsupported_cscs	e					Port type @ unsupported at line @
cse	csp	mmod	mult_css_arg_div	e					Macro @ contains too many actual arguments at line @
cse	csp	mmod	miss_css_arg_div	e					Macro @ is missing some actual arguments at line @
cse	csp	mmod	not_else_css_div	e					Unmatched 'else directive at line @
cse	csp	mmod	not_endif_css_div	e					Unmatched 'endif directive at line @
cse	csp	mmod	not_include_css_div	e					Missing filename for 'include directive at line @
cse	csp	mmod	bad_include_css_div	e					Badly formed include directive at line @
cse	csp	mmod	fmis_include_css_div	e					Filename missing in #include directive at line @
cse	csp	mod	mod_miss_endmodule_cscs	e					Missing endmodule at line @
cse	csp	mod	mod_no_module_found_cscs	e					No modules found at line @
cse	csp	mod	mod_no_entity_found_cscs	e					No entity found at line @
cse	csp	mod	mod_no_unit_found_cscs	e					No unit found at line @
cse	csp	nett	nett_unsupported_reg_cscs	e					Unsupported register type @ at line @
cse	csp	num	radix_h_num_css	ew					Illegal number radix, 'h expected at line @
cse	csp	num	radix_b_num_css	ew					Illegal number radix, 'b expected at line @
cse	csp	num	radix_d_num_css	ew					Illegal number radix, 'd expected at line @
cse	csp	num	radix_o_num_css	ew					Illegal number radix; 'o

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									expected at line @
cse	csp	pars	S_stmt_pars_cs	e					Statement S at line @
cse	csp	port	ill_formal_port_name_cscs	e					Illegal formal port @ at line @
cse	csp	pp	pp_cannot_open_file_not_exist_csc	e					Cannot open include file @, file does not exist at line @
cse	csp	pp	pp_cannot_open_file_not_have_read_perm_cscs	e					Cannot open include file @, file does not have read permission at line @
cse	csp	pp	include_filne	e					Include file @ not found at line @
cse	csp	prts	define_ill_prts_csc	e					Illegal part select specifier, define missing at line @
cse	csp	prts	prts_part_select_cscs	e					Badly formed part select at line @
cse	csp	stmt	miss_comma_stmt_css	e					Missing comma at line @
cse	csp	stmt	miss_semicolon_stmt_css	e					Missing semi colon at line @
cse	csp	stmt	miss_char_stmt_css	e					Missing @ at line @
cse	csp	stmt	wait_kword_stmt_css	e					@ expected at line @
cse	csp	stmt	missing_equal_sign	e					Equal sign missing at line @
cse	csp	stmt	illegal_semi_colon	e					Null (semi colon) found in illegal position at line @
cse	csp	stmt	unparsable	e					Cannot be parsed at line @
cse	csp	stmt	null_not_allowed_stmt_cscs	e					Null statement is not allowed here at line @
cse	csp	str	ill_str_char_found_cscs	e					Illegal character @ found after backslash at line @
cse	csp	udir	other_cdir_cscs	w					Found other compiler directive at line @
cse	prp	file	not_dir_name_file_csp	e					Directory @ does not exist at line @
cse	prp	file	cannot_open_file_ppcs	e					Cannot open file @ at line @
cse	prp	pp	not_incl_directive_pp_ppcs	e					Empty filename for 'include directive at line @
cse	prp	pp	pp_miss_macroname_cs	e					Missing macro name at line @
cse	prp	pp	ill_macroname_pp_cs	e					Illegal macro name @ at line @
cse	prp	pp	pp_text_macro_rec_cs	e					Text macro string used recursively at line @
cse	prp	pp	pp_cannot_open_libfile_ppcs	e					Cannot open library file @ at line @
cse	prp	pp	pp_text_macroname_not_defined_ppcs	e					Text macro (name) not defined at line @
cse	prp	pp	pp_ifdef_miss_macroname_ppcs	e					'ifdef missing macro name at line @
cse	prp	pp	pp_undef_miss_macroname_ppcs	e					'undef missing macro name at line @
cse	prp	pp	pp_miss_endif_directive_ppcs	e					Missing 'endif directive at line @
cse	prp	pp	pp_rec_include_file_ppcs	e					Recursive INCLUDE file @ at line @
cse	prp	pp	cmdl_arg_used_in_def_ppcs	e					Command line argument used in define at line @
cse	prp	pp	pp_undef_macro_ppcs	e					Undef @ not defined macro at line @
cse	prp	pp	include_filne	e					Include file @ not found at line @
cse	vep	ccd	ill_pos_CSLC_ccd_mod_vec	e				x	Illegal position for CSLC directive in module name at line @
cse	vep	ccd	ill_pos_CSLC_ccd_ent_vec	e				x	Illegal position for CSLC directive in entity name at line @
cse	vep	ccd	ill_pos_CSLC_ccd_unit_vec	e				x	Illegal position for CSLC directive in unit name at line @
cse	vep	ccd	misplaced_csdir_ignored_vecs	e				x	Lower case directive in wrong location. Ignored at line @
cse	vep	clk	clk_file_cannot_open_vecs	e					Clock file @ cannot be opened at line @
cse	vep	clk	no_clk_source_specified_clk_vecs	e					No clock source specified clock @ at line @
cse	vep	cmdl	ill_cmdl_uselib_dir_path_vecs	e					Illegal 'uselib directory path @ no such directory at line @
cse	vep	cmnt	cse_vep_cmnt_miss_closing_vecs	e					/* comment missing closing */ at line @
cse	vep	csi	miss_char_case_vecs	e					Missing character @ at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	vep	expr	malformed_unary_expr_cvep	e					Malformed unary Expression @ at line @
cse	vep	expr	malformed_binary_expr_cvep	e					Malformed binary Expression @ at line @
cse	vep	expr	malformed_ternary_expr_cvep	e					Malformed ternary Expression @ at line @
cse	vep	expr	expr_found_reserved_word_vecs	e					Expected identifier but found reserved word @ at line @
cse	vep	expr	expr_concatenation_empty_vecs	e					Concatenation empty at line @
cse	vep	expr	ill_operator_expr_vecs	e					Illegal operator @ at line @
cse	vep	expr	ill_operand_expr_vecs	e					Illegal operand @ at line @
cse	vep	file	cannot_open_file_vecs	e					Cannot open file @ at line @
cse	vep	file	line_lenght_overflow_vecs	e					Line length overflow line_length @ at line @
cse	vep	file	environ_var_in_filel_vecs	e					Environ variable in file list at line @
cse	vep	func	undefined_func_vecs	e					Undefined function @ at line @
cse	vep	inst	ill_mod_inst_name_vecs	e					Illegal module instance @ at line @
cse	vep	inst	ill_entity_inst_name_vecs	e					Illegal entity instance @ at line @
cse	vep	inst	ill_unit_inst_name_vecs	e					Illegal unit instance @ at line @
cse	vep	lib	not_open_lib_file_vec	e					Cannot open library file @ at line @
cse	vep	list	trail_comma_list_csc	e					Trailing comma in parentheses enclosed list at line @
cse	vep	list	list_miising_comma_vecs	w					Missing comma between @ and name at line @
cse	vep	mem	latch_type_miss_in_latch_array_decl_	e					Latch type missing ' in latch-array declaration at line @
cse	vep	mifc	mifc_port_type_unsupported_vecs	e					Port type @ unsupported at line @
cse	vep	mmod	mult_csc_arg_div	e					Macro @ contains too many actual arguments at line @
cse	vep	mmod	miss_csc_arg_div	e					Macro @ is missing some actual arguments at line @
cse	vep	mmod	not_else_csc_div	e					Unmatched 'else directive at line @
cse	vep	mmod	not_endif_csc_div	e					Unmatched 'endif directive at line @
cse	vep	mmod	not_include_csc_div	e					Missing filename for 'include directive at line @
cse	vep	mmod	bad_include_csc_div	e					Badly formed include directive at line @
cse	vep	mmod	fmis_include_csc_div	e					Filename missing in #include directive at line @
cse	vep	mod	mod_miss_endmodule_vecs	e					Missing endmodule at line @
cse	vep	mod	mod_no_module_found_vecs	e					No modules found at line @
cse	vep	mod	mod_no_entity_found_vecs	e					No entity found at line @
cse	vep	mod	mod_no_unit_found_vecs	e					No unit found at line @
cse	vep	nett	nett_unsupported_reg_vecs	e					Unsupported register type @ at line @
cse	vep	num	radix_h_num_csc	ew					Illegal number radix, 'h expected at line @
cse	vep	num	radix_b_num_csc	ew					Illegal number radix, 'b expected at line @
cse	vep	num	radix_d_num_csc	ew					Illegal number radix, 'd expected at line @
cse	vep	num	radix_o_num_csc	ew					Illegal number radix; 'o expected at line @
cse	vep	port	ill_formal_port_name_vecs	e					Illegal formal port @ at line @
cse	vep	pp	pp_cannot_open_file_not_exist_vecs	e					Cannot open include file @, file does not exist at line @
cse	vep	pp	pp_cannot_open_file_not_have_read_perm_vecs	e					Cannot open include file @, file does not have read permission at line @
cse	vep	prts	define_ill_prts_vec	e					Illegal part select specifier, define missing at line @
cse	vep	prts	prts_part_select_vecs	e					Badly formed part select at line @
cse	vep	stmt	miss_comma_stmt_csc	e					Missing comma at line @

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cse	vep	stmt	miss_semicolon_stmt_csc	e					Missing semi colon at line @
cse	vep	stmt	miss_char_stmt_csc	e					Missing @ at line @
cse	vep	stmt	wait_kword_stmt_csc	e					@ expected at line @
cse	vep	stmt	null_not_allowed_stmt_vecs	e					Null statement is not allowed here at line @
cse	vep	str	ill_str_char_found_vecs	e					Illegal character @ found after backslash at line @
cse	vep	udir	other_cdir_vecs	w					Found other compiler directive at line @
cse	vhp	ccd	ill_pos_CSLC_ccd_mod_vhc	e				x	Illegal position for CSLC directive in module name at line @
cse	vhp	ccd	ill_pos_CSLC_ccd_ent_vhc	e				x	Illegal position for CSLC directive in entity name at line @
cse	vhp	ccd	ill_pos_CSLC_ccd_unit_vhc	e				x	Illegal position for CSLC directive in unit name at line @
cse	vhp	ccd	misplaced_csdir_ignored_vhcs	e				x	Lower case directive in wrong location. Ignored at line @
cse	vhp	clk	clk_file_cannot_open_vhcs	e					Clock file @ cannot be opened at line @
cse	vhp	clk	no_clk_source_specified_clk_vhcs	e					No clock source specified clock @ at line @
cse	vhp	cmdl	ill_cmdl_uselib_dir_path_vhcs	e					Illegal 'uselib directory path @ no such directory at line @
cse	vhp	cmnt	cse_vhp_cmnt_miss_closing_vhcs	e					/* comment missing closing */ at line @
cse	vhp	csi	miss_char_case_vhcs	e					Missing character @ at line @
cse	vhp	expr	malformed_unary_expr_cvhp	e					Malformed unary Expression @ at line @
cse	vhp	expr	malformed_binary_expr_cvhp	e					Malformed binary Expression @ at line @
cse	vhp	expr	malformed_ternary_expr_cvhp	e					Malformed ternary Expression @ at line @
cse	vhp	expr	expr_found_reserved_word_vhcs	e					Expected identifier but found reserved word @ at line @
cse	vhp	expr	expr_concatenation_empty_vhcs	e					Concatenation empty at line @
cse	vhp	expr	ill_operator_expr_vhcs	e					Illegal operator @ at line @
cse	vhp	expr	ill_operand_expr_vhcs	e					Illegal operand @ at line @
cse	vhp	file	cannot_open_file_vhcs	e					Cannot open file @ at line @
cse	vhp	file	line_lenght_overflow_vhcs	e					Line length overflow line_length @ at line @
cse	vhp	file	environ_var_in_filel_vhcs	e					Environ variable in file list at line @
cse	vhp	func	undefined_func_vhcs	e					Undefined function @ at line @
cse	vhp	inst	ill_mod_inst_name_vhcs	e					Illegal module instance @ at line @
cse	vhp	inst	ill_entity_inst_name_vhsc	e					Illegal entity instance @ at line @
cse	vhp	inst	ill_unit_inst_name_vhcs	e					Illegal unit instance @ at line @
cse	vhp	lib	not_open_lib_file_vhc	e					Cannot open library file @ at line @
cse	vhp	list	trail_comma_list_csh	e					Trailing comma in parentheses enclosed list at line @
cse	vhp	list	list_miising_comma_vhcs	w					Missing comma between @ and name at line @
cse	vhp	mem	clk_name_miss_in_latch_array_decl_	e					Clock name missing in latch-array directive declaration at line @
cse	vhp	mifc	mifc_port_type_unsupported_vhcs	e					Port type @ unsupported at line @
cse	vhp	mmod	mult_csh_arg_div	e					Macro @ contains too many actual arguments at line @
cse	vhp	mmod	miss_csh_arg_div	e					Macro @ is missing some actual arguments at line @
cse	vhp	mmod	not_else_csh_div	e					Unmatched 'else directive at line @
cse	vhp	mmod	not_endif_csh_div	e					Unmatched 'endif directive at line @
cse	vhp	mmod	not_include_csh_div	e					Missing filename for 'include directive at line @
cse	vhp	mmod	bad_include_csh_div	e					Badly formed include directive at line @

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cse	vhp	mmod	fmis_include_csh_div	e					Filename missing in #include directive at line @
cse	vhp	mod	mod_miss_endmodule_vhcs	e					Missing endmodule at line @
cse	vhp	mod	mod_no_module_found_vhcs	e					No modules found at line @
cse	vhp	mod	mod_no_entity_found_vhcs	e					No entity found at line @
cse	vhp	mod	mod_no_unit_found_vhcs	e					No unit found at line @
cse	vhp	nett	nett_unsupported_reg_vhcs	e					Unsupported register type @ at line @
cse	vhp	num	radix_h_num_csh	ew					Illegal number radix, 'h expected at line @
cse	vhp	num	radix_b_num_csh	ew					Illegal number radix, 'b expected at line @
cse	vhp	num	radix_d_num_csh	ew					Illegal number radix, 'd expected at line @
cse	vhp	num	radix_o_num_csh	ew					Illegal number radix; 'o expected at line @
cse	vhp	port	ill_formal_port_name_vhcs	e					Illegal formal port @ at line @
cse	vhp	pp	pp_cannot_open_file_not_exist_vhcs	e					Cannot open include file @, file does not exist at line @
cse	vhp	pp	pp_cannot_open_file_not_have_read_perm_vhcs	e					Cannot open include file @, file does not have read permission at line @
cse	vhp	prts	define_ill_prts_vhc	e					Illegal part select specifier, define missing at line @
cse	vhp	prts	prts_part_select_vhcs	e					Badly formed part select at line @
cse	vhp	stmt	miss_comma_stmt_csh	e					Missing comma at line @
cse	vhp	stmt	miss_semicolon_stmt_csh	e					Missing semi colon at line @
cse	vhp	stmt	miss_char_stmt_csh	e					Missing @ at line @
cse	vhp	stmt	wait_kword_stmt_csh	e					@ expected at line @
cse	vhp	stmt	null_not_allowed_stmt_vhcs	e					Null statement is not allowed here at line @
cse	vhp	str	ill_str_char_found_vhcs	e					Illegal character @ found after backslash at line @
cse	vhp	udir	other_cdir_vhcs	w					Found other compiler directive at line @
csw	csp	stmt	long_line	w				x	Line too long, maximum line size is @ characters at line @
dee	cda	ccd	dupl_filter_dir_cdde	w				x	Duplicated filter directive @ at line @
dee	cda	ccd	unused_filter_dir_cdde	w				x	Unused filter directive @ at line @
dee	cda	ccd	ill_filter_dir_cdde	w				x	Illegal filter directive @ at line @
dee	cda	clk	clk_array_latches_cannot_mix_latch_types	e					Array-latches which use multiple clocks cannot mix latch types at line @
dee	cda	clk	latch_not_connected_clk_cdde	e					Latch not connected to a clock pin. at line @
dee	cda	clk	FF_not_connected_clk_cdde	e					FF not connected to a clock pin. at line @
dee	cda	clk	clk_source_not_vec_bit_cdde	e					Clock source @ cannot be a vector bit at line @
dee	cda	clk	clk_driven_by_net_cdde	e					The clock source @ is not driven by a clock and is driven by net @. Inferring a net type instead of clock per the clock directive. at line @
dee	cda	clk	clk_driven_by_port_cdde	e					The clock source @ is not driven by a clock and is driven by port @. Inferring a port type instead of clock per the clock directive. at line @
dee	cda	clk	clk_driven_by_signal_cdde	e					The clock source @ is not driven by a clock and is driven by signal @. Inferring a signal type instead of clock per the clock directive. at line @
dee	cda	clk	clk_should_drive_clk_cdde	e					A clock should drive clock @. at line @
dee	cda	clk	clk_source_def_contains_clk_cdde	e					Clock source definition contains a clock at line @
dee	cda	clk	cannot_open_clk_filename_cdde	e					Cannot open the clock file filename at line @
dee	cda	clk	clk_source_specification_error_cdde	e					Clock source specification error at line @

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dee	cda	clk	clck_assign_const_value_cdde	e					Clock @ assigned to constant value. at line @
dee	cda	clk	clk_assign_mux_clk_glitch_cdde	e					Clock @ assigned to multiplexed clock gate with glitch. at line @
dee	cda	clk	clk_assign_phase_shifted_clk_cdde	e					Clock @ assigned to phase shifted clock. at line @
dee	cda	clk	generated_clk_not_driven_by_FF_cdde	e					Generated clock @ is not driven by FF. at line @
dee	cda	clk	clk_source_driven_by_clk_cdde	e					The clock source clock is driven by another clock (reword this msg) at line @
dee	cda	clk	unsupp_logic_op_during_tree_clk_anls_cdde	w					Found unsupported logic operation type @ during clock tree analysis. at line @
dee	cda	clk	unsupp_gated_clk_logic_during_clk_tree_anls_cdde	w					Found unsupported gated clock logic type @ during clock tree analysis. at line @
dee	cda	clk	unsupp_logic_expr_during_clk_tree_anls_cdde	w					Found unsupported logic Expression type @ during clock tree analysis. at line @
dee	cda	clk	unsupp_gated_clk_comp_during_clk_tree_anls_cdde	w					Found unsupported gated clock component type @ during clock tree analysis. 1 at line @
dee	cda	clk	logic_comp_clk_pin_driven_unsupp_1_gate_cdde	w					A logic component clock pin is driven by unsupported clock 1 logic gate. at line @
dee	cda	clk	mux_select_input_driven_gated_clk_cdde	w					Multiplexer both the select @ and input @ are driven by gated clock.. This warning now reports the path from the path from the clock source to the input pin and the dock source to the mux select pin. at line @
dee	cda	clk	one_input_pin_driven_gated_clk_other_not_cdde	w					Multiplexer has one data input @ driven by gated clock @ and the other data pin @ not driven by gated clock. Output @ may be undefined. at line @
dee	cda	clk	unsupp_gated_clk_cdde	w					Unsupported gated clock type @ at line @
dee	cda	clk	unsupp_logic_inst_clk_tree_cdde	w					Unsupported logic instance @ in clock tree logic at line @
dee	cda	clk	unsupp_gated_clk_type_cdde	w					Use of unsupported gated clock type @ at line @
dee	cda	clk	enable_asserted_clk_sig_inactive_cdde	w					The enable signal of a gated clock logic may be asserted when the clock signal is inactive. at line @
dee	cda	clk	unsupp_gated_clk_comp_cdde	w					Unsupported gated clock component type @. at line @
dee	cda	clk	unsupp_logic_gate_comp_clk_pin_cdde	w					By unsupported clock logic gate a logic component clock pin @ at line @
dee	cda	clk	complex_gated_clk_cdde	w					Found complex gated clock @ at line @
dee	cda	clk	mux_select_or_input_pin_drvn_gate_clk_cdde	w					The mux select pin and one or more mux input pins are driven by gated clocks at line @
dee	cda	clk	one_data_pin_driven_gated_clk_other_not_cdde	w					Mux has one data pin driven by gated clock @ and the other data pin @ not driven by gated clock @ at line @
dee	cda	clk	cannot_anls_gated_clk_cdde	w					Cannot analyze gated clock type @ at line @
dee	cda	clk	gated_clk_more_than_1pin_output_cdde	w					Gated clock has more than 1 output pin at line @
dee	cda	clk	no_clknet_in_always_blk_edge_stmt_cdde	w					No clockNet found in always block with edge statement at line @
dee	cda	clk	no_clkport_in_always_blk_edge_stmt_cdde	w					No clockPort found in

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									always block with edge statement at line @
dee	cda	clk	no_clksig_in_always_blk_edge_stmt_cdde	w					No clockSignal found in always block with edge statement at line @
dee	cda	clk	no_clknet_in_always_blk_as_latch_cdde	w					No clockNet found in always block which can be inferred as a latch at line @
dee	cda	clk	no_clkport_in_always_blk_as_latch_cdde	w					No clockPort found in always block which can be inferred as a latch at line @
dee	cda	clk	no_clksig_in_always_blk_as_latch_cdde	w					No clockSignal found in always block which can be inferred as a latch at line @
dee	cda	clk	merged_clk_latch_point_cdde	w					Merged clock @ with latching point at line @
dee	cda	clk	merged_clk_doamins_cdde	w					Merged clock domains clocks @ at line @
dee	cda	clk	clk_domains_mergednet_unknown_cdde	w					Clock domains mergedNets unknown... at line @
dee	cda	clk	clk_domains_mergedport_unknown_cdde	w					Clock domains mergedPorts unknown... at line @
dee	cda	clk	clk_domains_mergedsig_unknown_cdde	w					Clock domains mergedSignals unknown... at line @
dee	cda	clk	merged_clk_phases_cdde	w					Merged clock phases clock @ phase phase @ clock @ phase @ at line @
dee	cda	clk	clk_tree_outputs_more_max_fanout_cdde	w					Clock tree logic has @ outputs which exceeds the maximimum threshold for gated clock fan out at line @
dee	cda	clk	scan_latch_no_domain_cdde	w					Driver of scan latch clock 'clock' has no domain. at line @
dee	cda	clk	clk_dupl_multi_dirs_cdde	w					Clock @ duplicated in multiple clock directives at line @
dee	cda	clk	cannot_locate_clknet_dsgn_cdde	w					Cannot locate the clockNet @ in design at line @
dee	cda	clk	cannot_locate_clkport_dsgn_cdde	w					Cannot locate the clockPortt @ in design at line @
dee	cda	clk	cannot_locate_clksig_dsgn_cdde	w					Cannot locate the clockSignal @ in design at line @
dee	cda	cmpl	comp_loop_split_auto_cdde	w					Component with component loop has been automatically split at line @
dee	cda	comb	comb_level_exceeds_num_cdde	w					Combinational logic cone depth. Level exceeds maximum specified depth @ at line @
dee	cda	css	css_coded_as_ternary_expr_cdde	w					Case statement could be coded as a ternaryExpression at line @
dee	cda	drvc	tri_nontri_drives_net_cdde	w					tristate @ and non-tristate @ drivers onNet at line @
dee	cda	drvc	tri_nontri_drives_port_cdde	w					tristate @ and non-tristate @ drivers onPort at line @
dee	cda	drvc	tri_nontri_drives_sig_cdde	w					tristate @ and non-tristate @ drivers onSignal at line @
dee	cda	func	unm_type_func_task_param_cdde	e					Unmatched type in function/task @ parameter @ at line @
dee	cda	func	unused_func_cdde	e					Unused function @ at line @
dee	cda	inhw	inhw_latch_not_connected_clk_cde	e					Scan latch not connected to clock at line @
dee	cda	inhw	inhw_latch_not_connected_data_in_cdde	e					Scan latch not connected to data in at line @
dee	cda	inhw	inhw_latch_not_connected_output_cdde	e					Scan latch not connected to output at line @
dee	cda	init	init_time_domain_invalid_comp_cdde	w					Initialization time domain contains an Invalid component type @ at line @
dee	cda	inst	wrong_port_order_in_inst_cdde	e					Wrong port order in

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									instantiation @ at line @
dee	cda	inst	unparam_inst_to_param_cdde	e					Unparameterized instantiation to parameter @ at line @
dee	cda	mdb	mdb_contention_cdde	w					Bus contention. at line @
dee	cda	mdb	mdb_connected_to_pull_up_down_cdde	w					Wired bus connected to pull up(s) and pull down(s) at line @
dee	cda	mdb	mdb_net_driven_by_different_driver_cdde	w					Multi-driven Net driven by different driver types at line @
dee	cda	mdb	mdb_port_driven_by_different_driver_cdde	w					Multi-driven Port driven by different driver types at line @
dee	cda	mdb	mdb_sig_driven_by_different_driver_cdde	w					Multi-driven Signal driven by different driver types at line @
dee	cda	mdb	single_mod_net_with_mult_drvtri_cdde	w					Single module drives same multi driven Net with multiple tri-state drivers at line @
dee	cda	mdb	single_mod_port_with_mult_drvtri_cdde	w					Single module drives same multi driven Port with multiple tri-state drivers at line @
dee	cda	mdb	single_mod_sig_with_mult_drvtri_cdde	w					Single module drives same multi driven Signal with multiple tri-state drivers at line @
dee	cda	mdb	single_ent_net_with_mult_drvtri_cdde	w					Single entity drives same multi driven Net with multiple tri-state drivers at line @
dee	cda	mdb	single_ent_port_with_mult_drvtri_cdde	w					Single entity drives same multi driven Port with multiple tri-state drivers at line @
dee	cda	mdb	single_ent_sig_with_mult_drvtri_cdde	w					Single entity drives same multi driven Signal with multiple tri-state drivers at line @
dee	cda	mdb	singlee_unit_with_mult_drvtri_cdde	w					Single unit drives same multi driven Net with multiple tri-state drivers at line @
dee	cda	mdb	single_unitt_with_mult_drvtri_cdde	w					Single unit drives same multi driven Port with multiple tri-state drivers at line @
dee	cda	mdb	single_unit_with_mult_drvtri_cdde	w					Single unit drives same multi driven Signal with multiple tri-state drivers at line @
dee	cda	mdb	expr_on_lhs_mdb_net_cdde	w					Expression type @ on LHS in multi-drivenNet at line @
dee	cda	mdb	expr_on_lhs_mdb_port_cdde	w					Expression type @ on LHS in multi-drivenPort at line @
dee	cda	mdb	wired_net_only_connected_one_drvr_cdde	e					Wired net type only connected to one driver @ at line @
dee	cda	mdb	wired_port_only_connected_one_drvr_cdde	e					Wired port type only connected to one driver @ at line @
dee	cda	mdb	wired_sig_only_connected_one_drvr_cdde	e					Wired signal type only connected to one driver @ at line @
dee	cda	mdb	wired_net_cdde	e					Wired net type @ found at line @
dee	cda	mdb	wired_port_cde	e					Wired port type @ found at line @
dee	cda	mdb	wired_sig_cde	e					Wired signal type @ found at line @
dee	cda	mifc	empty_list_port_module_port_cdde	e					Empty list port at top module port @ at line @
dee	cda	mifc	empty_list_port_entity_port_cdde	e					Empty list port at top entity port @ at line @
dee	cda	mifc	empty_list_port_unit_port_cdde	e					Empty list port at top unit port @ at line @
dee	cda	mifc	mod_csl_max_num_ports_cdde	w				x	Module @ exceeds the maximum number of ports. (trumber read / trumber write ports in use.). Specify the port number threshold with the cslc directive csl_max_num_ports. at line @
dee	cda	mifc	entity_csl_max_num_ports_cdde	w				x	Entity @ exceeds the maximum number of

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									ports. (trumber read / trumber write ports in use.). Specify the port number threshold with the cslc directive csl_max_num_ports. at line @
dee	cda	mifc	unit_csl_max_num_ports_cdde	w				x	Unit @ exceeds the maximum number of ports. (trumber read / trumber write ports in use.). Specify the port number threshold with the cslc directive csl_max_num_ports. at line @
dee	cda	mod	wrong_order_in_port_decl_cdde	e					Wrong order in port declaration at line @
dee	cda	net	net_not_decalred_and_used_in_stmt_cdde	w					Inferred Net @ used in statement.Net not declared at line @
dee	cda	net	port_not_decalred_and_used_in_stmt_cdde	w					Inferred Port @ used in statement.Port not declared at line @
dee	cda	net	sig_not_decalred_and_used_in_stmt_csde	w					Inferred Signal @ used in statement.Signal not declared at line @
dee	cda	net	sig_not_decalred_and_used_in_stmt_cdde	w					Inferred Signal @ used in statement.Signal not declared at line @
dee	cda	rst	FF_without_rst_cdde	e					FF without reset at line @
dee	cda	rst	FF_with_rst_cdde	e					FF with reset. Low power designs reduce the load on the reset line by eliminating reset on FFs at line @
dee	cda	sdir	unmatched_syns_transl_on_off_cdde	e					unmatched synopsys translate off on at line @
dee	cda	seq	unconventional_always_blk_cdde	w					Found unconventional always block at line @
dee	cda	seq	always_blk_cannot_infer_all_outputs_cdde	w					Always block cannot infer all outputs as latches not all outputs can be inferred at line @
dee	cda	seq	irregular_latch_detected_cdde	w	?				Irregular latch detected. Latch may be transparent for longer than one cvcle. at line @
dee	cda	seq	detected_latching_point_cdde	w					Detected a latching point at line @
dee	cda	seq	latch_driven_both_phases_cdde	w					Latch driven by both phases at line @
dee	cda	seq	latch_driven_clk_logic_cdde	w					Latch driven by clock logic at line @
dee	cda	sig	sig_not_exist_in_dsgn_cdde	w					Signal @ does not exist in the design at line @
dee	cda	simr	mixed_edge_type_cdde	e					Mixed edge types at line @
dee	cda	snsl	edge_clk_not_specifiect_cdde	w					Edge type of clock @ is not specified at line @
dee	cda	snsl	edge_incorrect_clk_cdde	w					Edge type of clock @ is incorrect at line @
dee	cda	snsl	expr_type_cdde	w					Expression type @ at line @
dee	cda	sply	nonlib_el_defi_as_sply_cdde	e					Non-library element define name used as supply at line @
dee	cda	task	unused_task_cdde	e					Unused task @ at line @
dee	cda	topo	topo_sort_graph_cdde	w					The topological sort of the graph. at line @
dee	cda	unsy	unsy_case_op_cdde	e					Un-synthesizable case equality operator = = at line @
dee	cda	unsy	unsy_deassn_stmt_cdde	e					Un-synthesizable deassign statement at line @
dee	cda	unsy	unsy_defparam_cdde	e					Un-synthesizable defparam at line @
dee	cda	unsy	unsy_dely_ctrl_cdde	e					Un-synthesizable delay control at line @
dee	cda	unsy	unsy_evctrl_cdde	e					Un-synthesizable event control at line @
dee	cda	unsy	unsy_evdecl_cdde	e					Un-synthesizable event declaration at line @
dee	cda	unsy	unsy_forc_stmt_cdde	e					Un-synthesizable force statement at line @
dee	cda	unsy	unsy_fok_stmt_cdde	e					Un-synthesizable fork statement at line @
dee	cda	unsy	unsy_init_cdde	e					Un-synthesizable initial at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
dee	cda	unsy	unsy_prim_def_cdde	e					Un-synthesizable primitive definition at line @
dee	cda	unsy	unsy_rel_stmt_cdde	e					Un-synthesizable release statement at line @
dee	cda	unsy	unsy_rep_stmt_cdde	e					Un-synthesizable repeat statement at line @
dee	cda	unsy	unsy_time_decl_cdde	e					Un-synthesizable timeDeclaration at line @
dee	cda	unsy	unsy_trns_cdde	e					Un-synthesizable transistor at line @
dee	cda	unsy	unsy_wait_stmt_cdde	e					Un-synthesizable wait statement at line @
dee	cdc	blk	blk_cont_assign_not_allowed_cdcde	e					Procedural continuous assignment is not allowed at line @
dee	cdc	cyb	cyb_stmt_repeat_evc_in_blocking_assign_cdcde	e					Statement intra-assignment repeat event control in blocking assignment detected at line @
dee	cdc	cyb	cyb_stmt_evc_in_blocking_assign_cdcde	e					Statement intra-assignment event control in blocking assignment detected at line @
dee	cdc	cyb	cyb_stmt_repeat_evc_in_non_blk_assign_cdcde	e					Statement intra-assignment repeat event control in non-blocking assignment detected at line @
dee	cdc	cyb	cyb_stmt_evc_in_non_blk_assign_cdcde	e					Statement intra-assignment event control in non-blocking assignment detected at line @
dee	cdc	cyb	cyb_deassign_stmt_not_stimul_cdcde	e					De-assign statement can't be simulated at line @
dee	cdc	cyb	cyb_forever_loop_not_stimul_cdcde	e					Forever-loop is can't be simulated at line @
dee	cdc	dely	inappropriate_form_intra_assign_dely_cdcde	e					Intra-assignmentDelay control in blocking assignment not of form #O or #1 at line @
dee	cdc	forc	cannot_forc_prts_net_cdcde	e					Cannot force a partially selected Net name at line @
dee	cdc	forc	cannot_forc_prts_port_cdcde	e					Cannot force a partially selected Port name at line @
dee	cdc	forc	cannot_forc_prts_signal_cdcde	e					Cannot force a partially selected Signal name at line @
dee	cdc	inst	inst_mult_connections_port_cdcde	e					Port 'port' has multiple connections specified at line @
dee	cdc	inst	inst_unknown_port_name_cdcde	e					Unknown port name @ in named port connection at line @
dee	cdc	inst	too_many_port_connections_inst_cdcde	e					Too many port connections specified for instance @ at line @
dee	cdc	inst	inst_port_mod_width_cdcde	e					Input port @ in module @ width mismatch, actual-width (port-width) at line @
dee	cdc	inst	inst_port_entity_width_cdcde	e					Input port @ in entity @ width mismatch, actual-width (port-width) at line @
dee	cdc	inst	inst_port_unit_width_cdcde	e					Input port @ in unit @ width mismatch, actual-width (port-width) at line @
dee	cdc	inst	inst_output_mod_port_width_cdcde	e					Output port @ in module width mismatch, actual-width (port-width) at line @
dee	cdc	inst	inst_output_entity_port_width_cdcde	e					Output port @ in entity width mismatch, actual-width (port-width) at line @
dee	cdc	inst	inst_output_unit_port_width_cdcde	e					Output port @ in unit width mismatch, actual-width (port-width) at line @
dee	cdc	inst	inst_mod_not_contain_port_cdcde	e					Module @ does not contain Port @ at line @
dee	cdc	inst	inst_entity_not_contain_port_cdcde	e					Entity @ does not contain Port @ at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
dee	cdc	inst	inst_unit_not_contain_port_cdcde	e					Unit @ does not contain Port @ at line @
dee	cdc	inst	inout_port_mod_width_cdcde	e					Inout port @ in module width mismatch, actual width (port-width) at line @
dee	cdc	inst	inout_port_entity_width_cdcde	e					Inout port @ in entity width mismatch, actual width (port-width) at line @
dee	cdc	inst	inout_port_unit_width_cdcde	e					Inout port @ in unit width mismatch, actual width (port-width) at line @
dee	cdc	mdn	mdn_cannot_be_forced_cdcde	e					Multiple drive Net 'name' cannot be forced. at line @
dee	cdc	mdn	mdn_port_cannot_be_forced_cdcde	e					Multiple drive Port 'name' cannot be forced. at line @
dee	cdc	mdn	mdn_signal_cannot_be_forced_cdcde	e					Multiple drive Signal 'name' cannot be forced. at line @
dee	cdc	mifc	mifc_complex_port_decl_not_supported_cdcde	e					Complex port Declaration port of module @ is not supported at line @
dee	cdc	mifc	mifc_entity_complex_port_decl_not_supported_cdcde	e					Complex port Declaration port of entity @ is not supported at line @
dee	cdc	mifc	mifc_unit_complex_port_decl_not_supported_cdcde	e					Complex port Declaration port of unit @ is not supported at line @
dee	cdc	mifc	mifc_unknown_port_direction_cdcde	e					Unknown port direction @ (port) at line @
dee	cdc	mifc	mifc_input_port_is_mem_type_cdcde	e					Input port @ is memory type at line @
dee	cdc	num	num_division_by_zero_cdcde	e					Division by zero at line @
dee	cdc	rel	cannot_rel_prts_net_cdcde	e					Cannot release a partially selected Net name at line @
dee	cdc	rel	cannot_rel_prts_port_cdcde	e					Cannot release a partially selected Port name at line @
dee	cdc	rel	cannot_rel_prts_signal_cdcde	e					Cannot release a partially selected Signal name at line @
dee	cdc	trns	trns_inst_not_allowed_cdcde	e					Transistor-level instantiations @ not allowed at line @
dee	csa	ccd	dupl_filter_dir_csde	w				x	Duplicated filter directive @ at line @
dee	csa	ccd	unused_filter_dir_csde	w				x	Unused filter directive @ at line @
dee	csa	ccd	ill_filter_dir_csde	w				x	Illegal filter directive @ at line @
dee	csa	clk	latch_not_connected_clk_csde	e					Latch not connected to a clock pin. at line @
dee	csa	clk	FF_not_connected_clk_csde	e					FF not connected to a clock pin. at line @
dee	csa	clk	clk_source_not_vec_bit_csde	e					Clock source @ cannot be a vector bit at line @
dee	csa	clk	clk_driven_by_net_csde	e					The clock source @ is not driven by a clock and is driven by net @. Inferring a net type instead of clock per the clock directive. at line @
dee	csa	clk	clk_driven_by_port_csde	e					The clock source @ is not driven by a clock and is driven by port @. Inferring a port type instead of clock per the clock directive. at line @
dee	csa	clk	clk_driven_by_signal_csde	e					The clock source @ is not driven by a clock and is driven by signal @. Inferring a signal type instead of clock per the clock directive. at line @
dee	csa	clk	clk_should_drive_clk_csde	e					A clock should drive clock @. at line @
dee	csa	clk	clk_source_def_contains_clk_csde	e					Clock source definition contains a clock at line @
dee	csa	clk	cannot_open_clk_filename_csde	e					Cannot open the clock file filename at line @
dee	csa	clk	clk_source_specification_error_csde	e					Clock source specification error at line @
dee	csa	clk	clck_assign_const_value_csde	e					Clock @ assigned to constant value. at line @
dee	csa	clk	clk_assign_mux_clk_glitch_csde	e					Clock @ assigned to

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									multiplexed clock gate with glitch. at line @
dee	csa	clk	clk_assign_phase_shifted_clk_csde	e					Clock @ assigned to phase shifted clock. at line @
dee	csa	clk	generated_clk_not_driven_by_FF_csde	e					Generated clock @ is not driven by FF. at line @
dee	csa	clk	clk_source_driven_by_clk_csde	e					The clock source clock is driven by another clock (reword this msg) at line @
dee	csa	clk	unsupp_logic_op_during_tree_clk_anls_csde	w					Found unsupported logic operation type @ during clock tree analysis. at line @
dee	csa	clk	unsupp_gated_clk_logic_during_clk_tree_anls_csde	w					Found unsupported gated clock logic type @ during clock tree analysis. at line @
dee	csa	clk	unsupp_logic_expr_during_clk_tree_anls_csde	w					Found unsupported logic Expression type @ during clock tree analysis. at line @
dee	csa	clk	unsupp_gated_clk_comp_during_clk_tree_anls_csde	w					Found unsupported gated clock component type @ during clock tree analysis. 1 at line @
dee	csa	clk	logic_comp_clk_pin_driven_unsupp_1_gate_csde	w					A logic component clock pin is driven by unsupported clock 1 logic gate. at line @
dee	csa	clk	cslc_primitive_during_clk_tree_anls_csde	w				x	Found complex gated clock CSLC primitive 'primitive' during clock tree analysis. at line @
dee	csa	clk	cslc_primitive_during_clk_tree_anls_cdde	w				x	Found complex gated clock CSLC primitive 'primitive' during clock tree analysis. at line @
dee	csa	clk	mux_select_input_driven_gated_clk_csde	w					Multiplexer both the select @ and input @ are driven by gated clock.. This warning now reports the path from the path from the clock source to the input pin and the dock source to the mux select pin. at line @
dee	csa	clk	one_input_pin_driven_gated_clk_other_not_csde	w					Multiplexer has one data input @ driven by gated clock @ and the other data pin @ not driven by gated clock. Output @ may be undefined. at line @
dee	csa	clk	unsupp_gated_clk_csde	w					Unsupported gated clock type @ at line @
dee	csa	clk	unsupp_logic_inst_clk_tree_csde	w					Unsupported logic instance @ in clock tree logic at line @
dee	csa	clk	unsupp_gated_clk_type_csde	w					Use of unsupported gated clock type @ at line @
dee	csa	clk	enable_asserted_clk_sig_inactive_csde	w					The enable signal of a gated clock logic may be asserted when the clock signal is inactive. at line @
dee	csa	clk	unsupp_gated_clk_comp_csde	w					Unsupported gated clock component type @. at line @
dee	csa	clk	unsupp_logic_gate_comp_clk_pin_csde	w					By unsupported clock logic gate a logic component clock pin @ at line @
dee	csa	clk	complex_gated_clk_csde	w					Found complex gated clock @ at line @
dee	csa	clk	mux_select_or_input_pin_drvn_gate_clk_csde	w					The mux select pin and one or more mux input pins are driven by gated clocks at line @
dee	csa	clk	one_data_pin_driven_gated_clk_other_not_csde	w					Mux has one data pin driven by gated clock @ and the other data pin @ not driven by gated clock @ at line @
dee	csa	clk	cannot_anls_gated_clk_csde	w					Cannot analyze gated clock type @ at line @
dee	csa	clk	gated_clk_more_than_1pin_output_csde	w					Gated clock has more than 1 output pin at line

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									@
dee	csa	clk	no_clknet_in_always_blk_edge_stmt_csde	w					No clockNet found in always block with edge statement at line @
dee	csa	clk	no_clkport_in_always_blk_edge_stmt_csde	w					No clockPort found in always block with edge statement at line @
dee	csa	clk	no_clksig_in_always_blk_edge_stmt_csde	w					No clockSignal found in always block with edge statement at line @
dee	csa	clk	no_clknet_in_always_blk_as_latch_csde	w					No clockNet found in always block which can be inferred as a latch at line @
dee	csa	clk	no_clkport_in_always_blk_as_latch_csde	w					No clockPort found in always block which can be inferred as a latch at line @
dee	csa	clk	no_clksig_in_always_blk_as_latch_csde	w					No clockSignal found in always block which can be inferred as a latch at line @
dee	csa	clk	merged_clk_latch_point_csde	w					Merged clock @ with latching point at line @
dee	csa	clk	merged_clk_doamins_csde	w					Merged clock domains clocks @ at line @
dee	csa	clk	clk_domains_mergednet_unknown_csde	w					Clock domains mergedNets unknown... at line @
dee	csa	clk	clk_domains_mergedport_unknown_csde	w					Clock domains mergedPorts unknown... at line @
dee	csa	clk	clk_domains_mergedsig_unknown_csde	w					Clock domains mergedSignals unknown... at line @
dee	csa	clk	merged_clk_phases_csde	w					Merged clock phases clock @ phase phase @ clock @ phase @ at line @
dee	csa	clk	clk_tree_outputs_more_max_fanout_csde	w					Clock tree logic has @ outputs which exceeds the maximimum threshold for gated clock fan out at line @
dee	csa	clk	scan_latch_no_domain_csde	w					Driver of scan latch clock 'clock' has no domain. at line @
dee	csa	clk	clk_dupl_multi_dirs_csde	w					Clock @ duplicated in multiple clock directives at line @
dee	csa	clk	cannot_locate_clknet_dsgn_csde	w					Cannot locate the clockNet @ in design at line @
dee	csa	clk	cannot_locate_clkport_dsgn_csde	w					Cannot locate the clockPortt @ in design at line @
dee	csa	clk	cannot_locate_clksig_dsgn_csde	w					Cannot locate the clockSignal @ in design at line @
dee	csa	cmpl	comp_loop_split_auto_csde	w					Component with component loop has been automatically split at line @
dee	csa	comb	comb_level_exceeds_num_csde	w					Combinational logic cone depth. Level exceeds maximum specified depth @ at line @
dee	csa	css	css_coded_as_ternary_expr_csde	w					Case statement could be coded as a ternaryExpression at line @
dee	csa	drvc	tri_nontri_drives_net_csde	w					tristate @ and non-tristate @ drivers onNet at line @
dee	csa	drvc	tri_nontri_drives_port_csde	w					tristate @ and non-tristate @ drivers onPort at line @
dee	csa	drvc	tri_nontri_drives_sig_csde	w					tristate @ and non-tristate @ drivers onSignal at line @
dee	csa	func	unm_type_func_task_param_csde	e					Unmatched type in function/task @ parameter @ at line @
dee	csa	func	unused_func_csde	e					Unused function @ at line @
dee	csa	inhw	inhw_latch_not_connected_clk_csde	e					Scan latch not connected to clock at line @
dee	csa	inhw	inhw_latch_not_connected_data_in_csde	e					Scan latch not connected to data in at line @
dee	csa	inhw	inhw_latch_not_connected_output_csde	e					Scan latch not connected to output at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
dee	csa	init	init_time_domain_invalid_comp_csde	w					Initialization time domain contains an Invalid component type @ at line @
dee	csa	inst	wrong_port_order_in_inst_csde	e					Wrong port order in instantiation @ at line @
dee	csa	inst	unparam_inst_to_param_csde	e					Unparameterized instantiation to parameter @ at line @
dee	csa	mdb	mdb_contention_csde	w					Bus contention. at line @
dee	csa	mdb	mdb_connected_to_pull_up_down_csde	w					Wired bus connected to pull up(s) and pull down(s) at line @
dee	csa	mdb	mdb_net_driven_by_different_driver_csde	w					Multi-driven Net driven by different driver types at line @
dee	csa	mdb	mdb_port_driven_by_different_driver_csde	w					Multi-driven Port driven by different driver types at line @
dee	csa	mdb	mdb_sig_driven_by_different_driver_csde	w					Multi-driven Signal driven by different driver types at line @
dee	csa	mdb	single_mod_net_with_mult_drvtri_csde	w					Single module drives same multi driven Net with multiple tri-state drivers at line @
dee	csa	mdb	single_mod_port_with_mult_drvtri_csde	w					Single module drives same multi driven Port with multiple tri-state drivers at line @
dee	csa	mdb	single_mod_sig_with_mult_drvtri_csde	w					Single module drives same multi driven Signal with multiple tri-state drivers at line @
dee	csa	mdb	single_ent_net_with_mult_drvtri_csde	w					Single entity drives same multi driven Net with multiple tri-state drivers at line @
dee	csa	mdb	single_ent_port_with_mult_drvtri_csde	w					Single entity drives same multi driven Port with multiple tri-state drivers at line @
dee	csa	mdb	single_ent_sig_with_mult_drvtri_csde	w					Single entity drives same multi driven Signal with multiple tri-state drivers at line @
dee	csa	mdb	singlee_unit_with_mult_drvtri_csde	w					Single unit drives same multi driven Net with multiple tri-state drivers at line @
dee	csa	mdb	single_unitt_with_mult_drvtri_csde	w					Single unit drives same multi driven Port with multiple tri-state drivers at line @
dee	csa	mdb	single_unit_with_mult_drvtri_csde	w					Single unit drives same multi driven Signal with multiple tri-state drivers at line @
dee	csa	mdb	expr_on_lhs_mdb_port_csde	w					Expression type @ on LHS in multi-drivenPort at line @
dee	csa	mdb	expr_on_lhs_mdb_sig_csde	w					Expression type @ on LHS in multi-drivenSignal at line @
dee	csa	mdb	wired_net_only_connected_one_drvr_csde	e					Wired net type only connected to one driver @ at line @
dee	csa	mdb	wired_port_only_connected_one_drvr_csde	e					Wired port type only connected to one driver @ at line @
dee	csa	mdb	wired_sig_only_connected_one_drvr_csde	e					Wired signal type only connected to one driver @ at line @
dee	csa	mdb	wired_net_csde	e					Wired net type @ found at line @
dee	csa	mdb	wired_port_cde	e					Wired port type @ found at line @
dee	csa	mdb	wired_sig_cde	e					Wired signal type @ found at line @
dee	csa	mifc	empty_list_port_module_port_csde	e					Empty list port at top module port @ at line @
dee	csa	mifc	empty_list_port_entity_port_csde	e					Empty list port at top entity port @ at line @
dee	csa	mifc	empty_list_port_unit_port_csde	e					Empty list port at top unit port @ at line @
dee	csa	mifc	mod_csl_max_num_ports_csde	w				x	Module @ exceeds the maximum number of ports. (trumber read / trumber write ports in use.). Specify the port number threshold with

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									the cslc directive csl_max_num_ports. at line @
dee	csa	mifc	entity_csl_max_num_ports_csde	w				x	Entity @ exceeds the maximum number of ports. (trumber read / trumber write ports in use.). Specify the port number threshold with the cslc directive csl_max_num_ports. at line @
dee	csa	mifc	unit_csl_max_num_ports_csde	w				x	Unit @ exceeds the maximum number of ports. (trumber read / trumber write ports in use.). Specify the port number threshold with the cslc directive csl_max_num_ports. at line @
dee	csa	mod	wrong_order_in_port_decl_csde	e					Wrong order in port declaration at line @
dee	csa	net	net_not_decalred_and_used_in_stmt_csde	w					Inferred Net @ used in statement.Net not declared at line @
dee	csa	net	port_not_decalred_and_used_in_stmt_csde	w					Inferred Port @ used in statement.Port not declared at line @
dee	csa	pp	used_in_def_and_param_name_csde	e					Name @ used in define and parameter name at line @
dee	csa	pp	used_in_def_and_param_name_cdde	e					Name @ used in define and parameter name at line @
dee	csa	rst	FF_without_rst_csde	e					FF without reset at line @
dee	csa	rst	FF_with_rst_csde	e					FF with reset. Low power designs reduce the load on the reset line by eliminating reset on FFs at line @
dee	csa	sdir	unmatched_syns_transl_on_off_csde	e					unmatched synopsys translate off on at line @
dee	csa	seq	unconventional_always_blk_csde	w					Found unconventional always block at line @
dee	csa	seq	always_blk_cannot_infer_all_outputs_csde	w					Always block cannot infer all outputs as latches not all outputs can be inferred at line @
dee	csa	seq	irregular_latch_detected_csde	w	?				Irregular latch detected. Latch may be transparent for longer than one cvcle. at line @
dee	csa	seq	detected_latching_point_csde	w					Detected a latching point at line @
dee	csa	seq	latch_driven_both_phases_csde	w					Latch driven by both phases at line @
dee	csa	seq	latch_driven_clk_logic_csde	w					Latch driven by clock logic at line @
dee	csa	sig	sig_not_exist_in_dsgn_csde	w					Signal @ does not exist in the design at line @
dee	csa	simr	mixed_edge_type_csde	e					Mixed edge types at line @
dee	csa	snsl	edge_clk_not_specifiect_csde	w					Edge type of clock @ is not specified at line @
dee	csa	snsl	edge_incorrect_clk_csde	w					Edge type of clock @ is incorrect at line @
dee	csa	snsl	expr_type_csde	w					Expression type @ at line @
dee	csa	sply	nonlib_el_defi_as_sply_csde	e					Non-library element define name used as supply at line @
dee	csa	task	unused_task_csde	e					Unused task @ at line @
dee	csa	topo	topo_sort_graph_csde	w					The topological sort of the graph. at line @
dee	csa	unsy	unsy_case_op_csde	e					Un-synthesizable case equality operator = = at line @
dee	csa	unsy	unsy_deassn_stmt_csde	e					Un-synthesizable deassign statement at line @
dee	csa	unsy	unsy_defparam_csde	e					Un-synthesizable defparam at line @
dee	csa	unsy	unsy_dely_ctrl_csde	e					Un-synthesizable delay control at line @
dee	csa	unsy	unsy_evctrl_csde	e					Un-synthesizable event control at line @
dee	csa	unsy	unsy_evdecl_csde	e					Un-synthesizable event declaration at line @
dee	csa	unsy	unsy_forc_stmt_csde	e					Un-synthesizable force

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									statement at line @
dee	csa	unsy	unsy_fok_stmt_csde	e					Un-synthesizable fork statement at line @
dee	csa	unsy	unsy_init_csde	e					Un-synthesizable initial at line @
dee	csa	unsy	unsy_prim_def_csde	e					Un-synthesizable primitive definition at line @
dee	csa	unsy	unsy_rel_stmt_csde	e					Un-synthesizable release statement at line @
dee	csa	unsy	unsy_rep_stmt_csde	e					Un-synthesizable repeat statement at line @
dee	csa	unsy	unsy_time_decl_csde	e					Un-synthesizable timeDeclaration at line @
dee	csa	unsy	unsy_trns_csde	e					Un-synthesizable transistor at line @
dee	csa	unsy	unsy_wait_stmt_csde	e					Un-synthesizable wait statement at line @
dee	csb	blk	blk_cont_assign_not_allowed_csbde	e					Procedural continuous assignment is not allowed at line @
dee	csb	cyb	cyb_stmt_repeat_evc_in_blocking_assign_csbde	e					Statement intra-assignment repeat event control in blocking assignment detected at line @
dee	csb	cyb	cyb_stmt_evc_in_blocking_assign_csbde	e					Statement intra-assignment event control in blocking assignment detected at line @
dee	csb	cyb	cyb_stmt_repeat_evc_in_non_blk_assign_csbde	e					Statement intra-assignment repeat event control in non-blocking assignment detected at line @
dee	csb	cyb	cyb_stmt_evc_in_non_blk_assign_csbde	e					Statement intra-assignment event control in non-blocking assignment detected at line @
dee	csb	cyb	cyb_deassign_stmt_not_stimul_csbde	e					De-assign statement can't be simulated at line @
dee	csb	cyb	cyb_forever_loop_not_stimul_csbde	e					Forever-loop is can't be simulated at line @
dee	csb	dely	inappropriate_form_intra_assign_dely_csbde	e					Intra-assignmentDelay control in blocking assignment not of form #O or #1 at line @
dee	csb	forc	cannot_forc_prts_net_csbde	e					Cannot force a partially selected Net name at line @
dee	csb	forc	cannot_forc_prts_port_csbde	e					Cannot force a partially selected Port name at line @
dee	csb	forc	cannot_forc_prts_signal_csbde	e					Cannot force a partially selected Signal name at line @
dee	csb	inst	inst_mult_connections_port_csbde	e					Port 'port' has multiple connections specified at line @
dee	csb	inst	inst_unknown_port_name_csbde	e					Unknown port name @ in named port connection at line @
dee	csb	inst	too_many_port_connections_inst_csbde	e					Too many port connections specified for instance @ at line @
dee	csb	inst	inst_port_mod_width_csbde	e					Input port @ in module @ width mismatch, actual-width (port-width) at line @
dee	csb	inst	inst_port_entity_width_csbde	e					Input port @ in entity @ width mismatch, actual-width (port-width) at line @
dee	csb	inst	inst_port_unit_width_csbde	e					Input port @ in unit @ width mismatch, actual-width (port-width) at line @
dee	csb	inst	inst_output_mod_port_width_csbde	e					Output port @ in module width mismatch, actual-width (port-width) at line @
dee	csb	inst	inst_output_entity_port_width_csbde	e					Output port @ in entity width mismatch, actual-width (port-width) at line @
dee	csb	inst	inst_output_unit_port_width_csbde	e					Output port @ in unit width mismatch, actual-width (port-width)

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									at line @
dee	csb	inst	inst_mod_not_contain_port_csbde	e					Module @ does not contain Port @ at line @
dee	csb	inst	inst_entity_not_contain_port_csbde	e					Entity @ does not contain Port @ at line @
dee	csb	inst	inst_unit_not_contain_port_csbde	e					Unit @ does not contain Port @ at line @
dee	csb	inst	inout_port_mod_width_csbde	e					Inout port @ in module width mismatch, actual width (port-width) at line @
dee	csb	inst	inout_port_entity_width_csbde	e					Inout port @ in entity width mismatch, actual width (port-width) at line @
dee	csb	inst	inout_port_unit_width_csbde	e					Inout port @ in unit width mismatch, actual width (port-width) at line @
dee	csb	mdn	mdn_cannot_be_forced_csbde	e					Multiple drive Net 'name' cannot be forced. at line @
dee	csb	mdn	mdn_port_cannot_be_forced_csbde	e					Multiple drive Port 'name' cannot be forced. at line @
dee	csb	mdn	mdn_signal_cannot_be_forced_csbde	e					Multiple drive Signal 'name' cannot be forced. at line @
dee	csb	mifc	mifc_complex_port_decl_not_supported_csbde	e					Complex port Declaration port of module @ is not supported at line @
dee	csb	mifc	mifc_entity_complex_port_decl_not_supported_csbde	e					Complex port Declaration port of entity @ is not supported at line @
dee	csb	mifc	mifc_unit_complex_port_decl_not_supported_csbde	e					Complex port Declaration port of unit @ is not supported at line @
dee	csb	mifc	mifc_unknown_port_direction_csbde	e					Unknown port direction @ (port) at line @
dee	csb	mifc	mifc_input_port_is_mem_type_csbde	e					Input port @ is memory type at line @
dee	csb	num	num_division_by_zero_csbde	e					Division by zero at line @
dee	csb	rel	cannot_rel_prts_net_csbde	e					Cannot release a partially selected Net name at line @
dee	csb	rel	cannot_rel_prts_port_csbde	e					Cannot release a partially selected Port name at line @
dee	csb	rel	cannot_rel_prts_signal_csbde	e					Cannot release a partially selected Signal name at line @
dee	csb	trns	trns_inst_not_allowed_csbde	e					Transistor-level instantiations @ not allowed at line @
dee	csc	blk	blk_cont_assign_not_allowed_cscde	e					Procedural continuous assignment is not allowed at line @
dee	csc	cyb	cyb_stmt_repeat_evc_in_blocking_assign_cscde	e					Statement intra-assignment repeat event control in blocking assignment detected at line @
dee	csc	cyb	cyb_stmt_evc_in_blocking_assign_cscde	e					Statement intra-assignment event control in blocking assignment detected at line @
dee	csc	cyb	cyb_stmt_repeat_evc_in_non_blk_assign_cscde	e					Statement intra-assignment repeat event control in non-blocking assignment detected at line @
dee	csc	cyb	cyb_stmt_evc_in_non_blk_assign_cscde	e					Statement intra-assignment event control in non-blocking assignment detected at line @
dee	csc	cyb	cyb_deassign_stmt_not_stimul_cscde	e					De-assign statement can't be simulated at line @
dee	csc	cyb	cyb_forever_loop_not_stimul_cscde	e					Forever-loop is can't be simulated at line @
dee	csc	dely	inappropriate_form_intra_assign_dely_cscde	e					Intra-assignmentDelay control in blocking assignment not of form #O or #1 at line @
dee	csc	dmsn	dee_csc_dmsn_already_set_dim	e					Number of dimensions already set at line @
dee	csc	dmsn	dee_csc_dmsn_0dim	e					Number of dimensions can not be 0 at line @
dee	csc	dmsn	dee_csc_dmsn_dim_not_set	e					Number of dimensions not set at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
dee	csc	dmsn	dee_csc_dmsn_illegal_dim	e					Illegal dimensions number at line @
dee	csc	dmsn	dee_csc_dmsn_multidim_object	e					Multi-dimensional object at line @
dee	csc	dsgn	dee_csc_dsgn_illegal	e					Parent should be the design at line @
dee	csc	dsgn	dee_csc_dsgn_illegal_parent	e					Parent should be a unit declaration at line @
dee	csc	dsgn	dee_csc_dsgn_illegal_parent1	e					Parent should be an instance at line @
dee	csc	dsgn	dee_csc_dsgn_already_set_width	e					Width or range already set at line @
dee	csc	forc	cannot_forc_prts_net_cscde	e					Cannot force a partially selected Net name at line @
dee	csc	forc	cannot_forc_prts_port_cscde	e					Cannot force a partially selected Port name at line @
dee	csc	forc	cannot_forc_prts_signal_cscde	e					Cannot force a partially selected Signal name at line @
dee	csc	id	dee_csc_id_name_exists	e					Name @ already exists at line @
dee	csc	id	dee_csc_scop_undefined_scope	e					Undefined scope at line @
dee	csc	inst	inst_mult_connections_port_cscde	e					Port 'port' has multiple connections specified at line @
dee	csc	inst	inst_unknown_port_name_cscde	e					Unknown port name @ in named port connection at line @
dee	csc	inst	too_many_port_connections_inst_cscde	e					Too many port connections specified for instance @ at line @
dee	csc	inst	inst_port_mod_width_cscde	e					Input port @ in module @ width mismatch, actual-width (port-width) at line @
dee	csc	inst	inst_port_entity_width_cscde	e					Input port @ in entity @ width mismatch, actual-width (port-width) at line @
dee	csc	inst	inst_port_unit_width_cscde	e					Input port @ in unit @ width mismatch, actual-width (port-width) at line @
dee	csc	inst	inst_output_mod_port_width_cscde	e					Output port @ in module width mismatch, actual-width (port-width) at line @
dee	csc	inst	inst_output_entity_port_width_cscde	e					Output port @ in entity width mismatch, actual-width (port-width) at line @
dee	csc	inst	inst_output_unit_port_width_cscde	e					Output port @ in unit width mismatch, actual-width (port-width) at line @
dee	csc	inst	inst_mod_not_contain_port_cscde	e					Module @ does not contain Port @ at line @
dee	csc	inst	inst_entity_not_contain_port_cscde	e					Entity @ does not contain Port @ at line @
dee	csc	inst	inst_unit_not_contain_port_cscde	e					Unit @ does not contain Port @ at line @
dee	csc	inst	inout_port_mod_width_cscde	e					Inout port @ in module width mismatch, actual width (port-width) at line @
dee	csc	inst	inout_port_entity_width_cscde	e					Inout port @ in entity width mismatch, actual width (port-width) at line @
dee	csc	inst	inout_port_unit_width_cscde	e					Inout port @ in unit width mismatch, actual width (port-width) at line @
dee	csc	mdn	mdn_cannot_be_forced_cscde	e					Multiple drive Net 'name' cannot be forced. at line @
dee	csc	mdn	mdn_port_cannot_be_forced_cscde	e					Multiple drive Port 'name' cannot be forced. at line @
dee	csc	mdn	mdn_signal_cannot_be_forced_cscde	e					Multiple drive Signal 'name' cannot be forced. at line @
dee	csc	mifc	mifc_complex_port_decl_not_supported_cscde	e					Complex port Declaration port of module @ is not supported at line @
dee	csc	mifc	mifc_entity_complex_port_decl_not_supported_cscde	e					Complex port Declaration port of entity @ is not supported at line @
dee	csc	mifc	mifc_unit_complex_port_decl_not_supported_cscde	e					Complex port Declaration

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									port of unit @ is not supported at line @
dee	csc	mifc	mifc_unknown_port_direction_cscde	e					Unknown port direction @ (port) at line @
dee	csc	mifc	mifc_input_port_is_mem_type_cscde	e					Input port @ is memory type at line @
dee	csc	num	num_division_by_zero_cscde	e					Division by zero at line @
dee	csc	rel	cannot_rel_prts_net_cscde	e					Cannot release a partially selected Net name at line @
dee	csc	rel	cannot_rel_prts_port_cscde	e					Cannot release a partially selected Port name at line @
dee	csc	rel	cannot_rel_prts_signal_cscde	e					Cannot release a partially selected Signal name at line @
dee	csc	scop	dee_csc_scop_cannot_find_object	e					Cannot find object in scope at line @
dee	csc	stmt	dee_csc_stmt_type_expected	e					Illegal type at line @
dee	csc	trns	trns_inst_not_allowed_cscde	e					Transistor-level instantiations @ not allowed at line @
dee	csp	mifc	mifc_unknown_port_direction_csde	e					Unknown port direction for port @ at line @
dee	csp	netd	net_decl_no_range_csde	e					Net declared with no range specification used with bit/part select at line @
dee	csp	netd	netd_port_no_range_csde	e					Port declared with no range specification used with bit/part select at line @
dee	csp	netd	netd_signal_no_range_csde	e					Signal declared with no range specification used with bit/part select at line @
dee	csp	port	port_decl_no_range_csde	e					Port declared with no range specification used with bit/part select at line @
dee	vep	mifc	mifc_unknown_port_direction_vede	e					Unknown port direction for port @ at line @
dee	vep	netd	net_decl_no_range_vede	e					Net declared with no range specification used with bit/part select at line @
dee	vep	netd	netd_port_no_range_vede	e					Port declared with no range specification used with bit/part select at line @
dee	vep	netd	netd_signal_no_range_vede	e					Signal declared with no range specification used with bit/part select at line @
dee	vep	port	port_decl_no_range_vede	e					Port declared with no range specification used with bit/part select at line @
dee	vhp	mifc	mifc_unknown_port_direction_vhde	e					Unknown port direction for port @ at line @
dee	vhp	netd	net_decl_no_range_vhde	e					Net declared with no range specification used with bit/part select at line @
dee	vhp	netd	netd_port_no_range_vhde	e					Port declared with no range specification used with bit/part select at line @
dee	vhp	netd	netd_signal_no_range_vhde	e					Signal declared with no range specification used with bit/part select at line @
dee	vhp	port	port_decl_no_range_vhde	e					Port declared with no range specification used with bit/part select at line @
ne	csp	num	sillnum_hex	e					Illegal character @ at line @
ne	vep	num	cillnum_hex	e					Illegal character @ at line @
ne	vhp	num	hillnum_hex	e					Illegal character @ at line @
res	csa	file	cannot_open_statistic_file_	w					Cannot open statistics file @ at line @
vee	cda	assn	unequal_length_lhs_rhs_cdve	e					Unequal length LHS and RHS at line @
vee	cda	assn	unequal_length_lhs_rhs_off_one_bit_cdve	e					Unequal length LHS and RHS off by one bit at line @
vee	cda	blk	repeat_in_nonblk_assn_cdve	e					Repeat in non-blocking assignment at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	cda	blk	empty_blk_cdve	e					Empty-block at line @
vee	cda	clk	unsupp_logic_operation_cdve	w					Unsupported logic operation type @. at line @
vee	cda	clk	unsupp_cl_gated_logic_cdve	w					Unsupported gated clock logic type. at line @
vee	cda	clk	unsupp_logic_expr_clk_cdve	w					Unsupported logicExpression type @ at line @
vee	cda	csi	duplicate_csi_cdve	e					Duplicate Case item @ at line @
vee	cda	csi	case_sel_contains_real_num_const_cdve	e					Case selector contains a constant real number at line @
vee	cda	csi	csi_contains_real_num_const_cdve	e					Case item contains a constant real number at line @
vee	cda	csi	real_in_csi_cdve	e					Real @ in case item at line @
vee	cda	csi	noncnst_in_iclude_file_cdve	e					Non-constant in include file @ at line @
vee	cda	csi	csi_width_mismatch_cdve	e					Case item @ width mismatch at line @
vee	cda	csi	efault_missing_cdve	e					Default missing at line @
vee	cda	css	not_all_csi_specified_cdve	e					Not allCase items are specified @ at line @
vee	cda	defd	mod_def_within_mod_not_in_include_cdde	e					Module define within module but not in include at line @
vee	cda	defd	ent_def_within_ent_not_in_include_cdde	e					Entity define within entity but not in include at line @
vee	cda	defd	unit_def_within_unit_not_in_include_cdde	e					Unit define within unit but not in include at line @
vee	cda	dely	comb_blk_contains_dely_assn_cdve	e					Combinational block contains delay assignement at line @
vee	cda	dely	seq_blk_contains_dely_assn_cdde	e					Sequential block contains delay assignement at line @
vee	cda	dely	comb_blk_dely_between_stms_cdve	e					Combinational block contains delay between statements at line @
vee	cda	dely	seq_blk_dely_between_stmt_cdve	e					Sequential block contains delay between statements at line @
vee	cda	dely	dely_in_nonblk_assn_comb_cdve	e					Delay in nonblocking assignement in combinational at line @
vee	cda	dely	dely_in_nonblk_assn_seq_cdve	e					Delay in nonblocking assignement in sequential at line @
vee	cda	drst	drvs_not_in_lib_cdve	e					Drive strength @ not in library at line @
vee	cda	drvc	output_arg_appers_rhs_cdve	w					Output argument @ of user system task appears in RHS and is driven elsewhere at line @
vee	cda	drvc	multiple_init_blk_drvc_cdve	w					Multiple initial blocks force 'narne' at line @
vee	cda	drvc	net_multiple_always_blk_cdve	w					Net @ multiple always blocks at line @
vee	cda	drvc	port_multiple_always_blk_cdve	w					Port @ multiple always blocks at line @
vee	cda	drvc	sig_multiple_always_blk_cdve	w					Signal @ multiple always blocks at line @
vee	cda	drvc	net_multiple_stmt_cdve	w					Net @ multiple statements with in the same always at line @
vee	cda	drvc	port_multiple_stmt_cdve	w					Port @ multiple statements with in the same always at line @
vee	cda	drvc	sig_multiple_stmt_cdve	w					Signal @ multiple statements with in the same always at line @
vee	cda	drvc	multiply_drvn_net_nontri_gate_cdve	w					Multiply drivenNet driven by a non-tristate gate at line @
vee	cda	drvc	multiply_drvn_port_nontri_gate_cdve	w					Multiply drivenPort driven by a non-tristate gate at line @
vee	cda	drvc	multiply_drvn_sig_nontri_gate_cdve	w					Multiply drivenSignal driven by a non-tristate gate at line @
vee	cda	drvc	incompatible_driver_net_cdve	w					Incompatible driver of type @ drivingNet_@ multi drivenNet of type @ name @ at line @
vee	cda	drvc	incompatible_driver_port_cdve	w					Incompatible driver of

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									type @ drivingPort_@ multi drivenPort of type @ name @ at line @
vee	cda	drvc	incompatible_driver_sig_cdve	w					Incompatible driver of type @ drivingSignal_@ multi drivenSignal of type @ name @ at line @
vee	cda	dsbl	dsbl_used_cdve	e					Disable used at line @
vee	cda	evc	embedded_ectl_cdve	e					Embedded-event-control at line @
vee	cda	expr	unary_op_in_comparison_cdve	e					Unary op used in comparison at line @
vee	cda	expr	shift_by_non_constcdve_	e					Shift by non constant @ at line @
vee	cda	expr	miss_parenthesis_cdve	e					Unary op @ with comparison op @ missing precedence parenthesis at line @
vee	cda	forc	no_release_stmt_in_init_blk_cdve	w					Force @ statement in the initial block and there is no release statement.for @ at line @
vee	cda	forc	no_force_stmt_in_init_blk_cdve	w	?				Release @ statement in the and there is no force statement.for @ at line @
vee	cda	forc	forcing_input_port_cdve	e					Forcing input port @ at line @
vee	cda	func	return_value_not_at_end_of_func_cdve	e					Return value not at end of function at line @
vee	cda	func	time_and_evctrl_in_func_cdve	e					Time and event control in function at line @
vee	cda	func	func_call_itself_rec_cdve	e					Function @ calling itself recursively at line @
vee	cda	gate	error_output_terminal_cdve	w			x		IEEE 1364-1995 error output terminal @. This will compile and simulate correctly on commercial verilog simulators at line @
vee	cda	init	assn_mem_in_init_blk_cdve	e					Assign memory in initial block at line @
vee	cda	inst	input_port_drvn_from_inside_mod_cdve	e					Input port @ being driven from inside of module @ at line @
vee	cda	inst	input_port_drvn_from_inside_entity_cdve	e					Input port @ being driven from inside of entity @ at line @
vee	cda	inst	input_port_drvn_from_inside_signal_cdve	e					Input port @ being driven from inside of signal @ at line @
vee	cda	inst	input_port_not_connected_in_parent_mod_cdve	e					Input port @ not connected in parent module at line @
vee	cda	inst	input_port_not_connected_in_parent_entity_cdve	e					Input port @ not connected in parent entity at line @
vee	cda	inst	input_port_not_connected_in_parent_signal_cdve	e					Input port @ not connected in parent signal at line @
vee	cda	mdb	single_comp_contains_multiple_tri_drv_cdve	w					A single component contains multiple tristate drivers at line @
vee	cda	mdb	unsuppexpr_on_lhs_net_drv_stmt_cdve	w					Unsupported Expression type type on LHS ofNet driver statement at line @
vee	cda	mdb	unsuppexpr_on_lhs_port_drv_stmt_cdve	w					Unsupported Expression type type on LHS ofPort driver statement at line @
vee	cda	mdb	unsuppexpr_on_lhs_sig_drv_stmt_cdve	w					Unsupported Expression type type on LHS ofSignal driver statement at line @
vee	cda	mdb	tri_not_in_top_mod_cdve	e					Tristate not in top module at line @
vee	cda	mdb	tri_not_in_top_ent_cdve	e					Tristate not in top entity at line @
vee	cda	mdb	tri_not_in_top_sig_cdve	e					Tristate not in top signal at line @
vee	cda	mdb	tri_primitive_inst_cdve	e					Tristate primitive instantiation at line @
vee	cda	mdb	tri_net_only_one_drvr_cdve	e					Tri Net has only one driver at line @
vee	cda	mdb	tri_port_only_one_drvr_cdve	e					Tri Port has only one driver at line @
vee	cda	mdb	tri_sig_only_one_drvr_cdve	e					Tri Signal has only one driver at line @
vee	cda	mem	single_bit_mem_cdve	e					Single bit memory @ at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	cda	mod	redef_mod_cdve	e					Redefined module @ at line @
vee	cda	mod	redef_ent_cdve	e					Redefined entity @ at line @
vee	cda	mod	redef_signal_cdve	e					Redefined signal @ at line @
vee	cda	net	tri_and_net_only_one_driver_cdve	e	?				triandNet @ has only one driver at line @
vee	cda	net	tri_and_port_only_one_driver_cdve	e	?				triandPort @ has only one driver at line @
vee	cda	net	tri_and_sig_only_one_driver_cdve	e	?				triandSignal @ has only one driver at line @
vee	cda	net	var_assn_but_never_ref_cdve	e					Variable @ assigned but never referenced at line @
vee	cda	net	var_never_assn_cdve	e					Variable @ never assigned at line @
vee	cda	net	var_not_assn_in_all_paths_cdve	e					Variable @ not being assigned in all paths at line @
vee	cda	net	var_not_in_snsl_cdve	e					Variable @ not in sensitivity list at line @
vee	cda	net	reg_connected_to_inout_in_inst_cdve	e					Reg @ connected to inout @ in instantiation @ at line @
vee	cda	net	reg_connectede_to_output_in_inst_cdve	e					Reg @ connected to output in instantiation at line @
vee	cda	net	reg_used_as_output_of_cont_assn_cdve	e					Reg @ used as output of continuous assign at line @
vee	cda	net	port_used_prior_to_decl_cdve	e					Port @ used prior toDeclaration at line @
vee	cda	net	dupl_sig_in_snsl_cdve	e					Duplicate signal @ in sensitivity list at line @
vee	cda	netd	var_never_assigned_cdve	e					Variable @ never assigned at line @
vee	cda	num	assignment_contains_real_num_const_cdve	e					Assignment contains a real number constant at line @
vee	cda	parm	unused_parm_cdve	e					Unused parameter @ at line @
vee	cda	parm	redef_param_cdve	e					Redefined parameter @ at line @
vee	cda	pp	redef_macro_cdve	e					Redefined macro @ at line @
vee	cda	prts	prts_on_vec_net_not_allowed_cdve	w					Part select @ on a vectored Net may not be allowed according to IEEE 1364-1995 at line @
vee	cda	prts	prts_on_vec_port_not_allowed_cdve	w					Part select @ on a vectored Port may not be allowed according to IEEE 1364-1995 at line @
vee	cda	prts	prts_on_vec_sig_not_allowed_cdve	w					Part select @ on a vectored Signal may not be allowed according to IEEE 1364-1995 at line @
vee	cda	prts	out_of_range_bit_ref_cdve	e					Out of range bus bit referenced at line @
vee	cda	prts	vec_index_order_incorrect_cdve	e					Vector index @ order incorrect at line @
vee	cda	prts	vec_index_truncated_cdve	e					Vector index @ truncated at line @
vee	cda	sdir	sdir_compiler_cdve	e					Found synopsys compiler directive at line @
vee	cda	seq	blk_not_in_lib_cdve	e					Block @ not in library at line @
vee	cda	sig	sig_will_float_when_rel_cdve	e					Signal @ will float when it is released at line @
vee	cda	snsl	var_modified_in_snsl_cdve	e					Variable @ modified in sense list at line @
vee	cda	snsl	var_in_snsl_unsused_in_blk_cdve	e					Variable @ in sensitivity list not used in block at line @
vee	cda	snsl	rhs_var_noi_in_snsl_cdve	e					RHS variable not in sensitivity list at line @
vee	cda	spec	spec_blk_found_cdve	e					Specify block found at line @
vee	cda	sply	sply_being_driven_cdve	e					Supply being driven at line @
vee	cda	sply	sply_not_def_user_keyword_cdve	e					Supply not defined with user defined keyword at line @
vee	cda	sply	sply_not_in_lib_cdve	e					Supply not in library at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	cda	sply	output_conncet_to_sply_	e					Output @ connect to supply at line @
vee	cda	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_cdve	e					Arithmetic operator RHS has one less bit than the LHS at line @
vee	cda	stmt	ar_op_unequal_lhs_rhs_cdve	e					Arithmetic operator unequal width LHS and RHS at line @
vee	cda	stmt	ar_op_unequal_var_on_rhs_cdve	e					Arithmetic operator unequal width variables @ on RHS at line @
vee	cda	task	task_call_iteslf_rec_cdve	e					Task @ calling itself recursively at line @
vee	cda	time	time_var_bit_used_cdde	e					Time variable bit used at line @
vee	cda	tri	tri_not_in_top_mod_cdve	e					Tristate @ not in top module at line @
vee	cda	tri	tri_not_in_top_entity_cdve	e					Tristate @ not in top entity at line @
vee	cda	tri	tri_not_in_top_signal_cdve	e					Tristate @ not in top signal at line @
vee	cda	tri	tri_prim_ist_cdve	e					Tristate primitive instantiation @ at line @
vee	cda	udp	upd_not_supported_cdve	e					UDPs are not supported at line @
vee	cdc	assn	x_in_rhs_of_assihnment_cdcve	e					x in rhs of assignment at line @
vee	cdc	assn	z_in_rhs_of_assn_default_csi_cdcve	e					x in rhs of assignement in defaultCase item at line @
vee	cdc	assn	z_in_rhs_of_assn_cdcve	e					z in rhs of assignement at line @
vee	cdc	assn	unequal_length_lhs_rhs_cdcve	e					Unequal length LHS and RHS at line @
vee	cdc	assn	unequal_length_lhs_rhs_off_one_bit_cdcve	e					Unequal length LHS and RHS off by one bit at line @
vee	cdc	blk	blk_ill_block_id_cdv	e					Illegal block @ at line @
vee	cdc	blk	nonblocking_assign_in_comb_always_blk_cdcve	e					Non blockinq aasignment in combinational always block at line @
vee	cdc	blk	seq_blk_contains_blk_assn_cdcve	e					Sequential block contains blocking assignement at line @
vee	cdc	casn	LHS_not_reg_casn_vhve	e					LHS cannot be a register @ at line @
vee	cdc	ccd	ccd_cdir_must_be_cst_expr_cdcve	e				x	CSL directive size must be constant Expression at line @
vee	cdc	clk	clk_name_not_found_cdir_cdcve	e				x	Clock name not found in cslc directive at line @
vee	cdc	clk	expr_sunj_to_different_clk_phases_cdcve	e					Expression subject to different clock phases at line @
vee	cdc	cmdl	cannot_use_librescan_with_liborder_specified_cdcve	e					Cannot use +librescan when +liborder has already been specified at line @
vee	cdc	cmdl	cannot_use_liborder_with_librescan_specified_cdcve	e					Cannot use +liborder when +librescan has already been specified at line @
vee	cdc	cond	if_case_question_cond_cdcve	e					If/case conditional expression expr syntax error at line @
vee	cdc	cond	if_no_else_in_comb_blk_cdcve	e					If no else in combinational block at line @
vee	cdc	cond	if_no_else_in_comb_blk_cdcvh	e					If no else in combinational block at line @
vee	cdc	csi	xcsi_not_in_casex_cdcve	e					xCase item not in casex at line @
vee	cdc	csi	noncnst_csi_cdcve	e					Non-constantCase item @ at line @
vee	cdc	csi	noncnst_dely_cdcve	e					Non-constant delay @ at line @
vee	cdc	csi	noncstn_rep_in_conc_cdcve	e					Non-constant repeator in concatenation at line @
vee	cdc	css	sns_pragma_full_case_cdcve	e					Assume a full case, missing default or synopsys pragma full case. at line @
vee	cdc	cyb	repeat_in_delay_cyb_cdv	e					Repeat clause in delay not supported at line @
vee	cdc	cyb	repeat_in_event_control_cyb_cdv	e					Repeat clause in event control not supported at line @
vee	cdc	cyb	event_id_not_supported_cyb_cdv	e					@ event id is not supported at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	cdc	cyb	ill_proc_assign_cyb_cdv	e					Illegal procedural continuous assignment statement at line @
vee	cdc	cyb	ill_deassign_cyb_cdv	e					Illegal de-assign statement at line @
vee	cdc	cyb	ill_force_cyb_cdv	e					Illegal force statement at line @
vee	cdc	cyb	ill_release_cyb_cdv	e					Illegal release statement at line @
vee	cdc	cyb	repeat_as_delay_cyb_cdv	e					Repeat as delay not supported at line @
vee	cdc	cyb	repeat_as_event_control_cyb_cdv	e					Repeat as event control not supported at line @
vee	cdc	cyb	wait_statement_not_cyb_cdv	e					Wait statement is not supported at line @
vee	cdc	cyb	disable_statement_not_cyb_cdv	e					Disable statement is not supported at line @
vee	cdc	cyb	events_not_supported_cyb_cdv	e					Events are not supported at line @
vee	cdc	cyb	fork_join_blocks_not_supported_cyb_cdv	e					Fork/join blocks are not supported at line @
vee	cdc	cyb	unsupp_function_return_time_cyb_cdv	e					Unsupported function return time at line @
vee	cdc	cyb	not_supp_events_cyb_cdv	e					Events are not supported at line @
vee	cdc	cyb	repeat_in_delay_or_event_cyb_cdv	e					Repeat clause in delay or Event control at line @
vee	cdc	cyb	ill_proc_cont_assign_stmt_cyb_cdv	e					Illegal procedural continuous assignment statement at line @
vee	cdc	cyb	ill_deassign_cyb_stmt_cdc	e					Illegal de-assign statement at line @
vee	cdc	cyb	ill_force_stmt_cyb_cdv	e					Illegal force statement at line @
vee	cdc	cyb	ill_release_stmt_cyb_cdv	e					Illegal release statement at line @
vee	cdc	cyb	repeat_not_supp_as_delay_or_event_cyb_cdv	e					Repeat as delay or event control not supported at line @
vee	cdc	cyb	not_supp_wait_stmt_cyb_cdv	e					Wait statement is not supported at line @
vee	cdc	cyb	not_supp_disable_stmt_cyb_cdv	e					Disable statement is not supported at line @
vee	cdc	cyb	supp_not_events_cyb_cdv	e					Events are not supported at line @
vee	cdc	cyb	not_supp_fork_join_blocks_cyb_cdv	e					Fork/join blocks are not supported at line @
vee	cdc	cyb	not_supp_UDP_cyb_cdv	e					UDPs are not supported at line @
vee	cdc	cyb	not_supp_defparam_cyb_cdv	e					Defparam is not supported at line @
vee	cdc	cyb	specify_blk_not_supported_cdcve	e					Specify blocks are not supported at line @
vee	cdc	cyb	mintypmax_expr_not_supp_cdcve	w					mintypmax Expressions are not supported at line @
vee	cdc	decl	decl_array_over_max_size_cdcve	e					Array @ exceeds maximum size limit at line @
vee	cdc	dely	max_val_dly_cdv	e					Too many delay values, max @ at line @
vee	cdc	dely	found_gate_dely_not_allowed_cdcve	e					Found gate delay which are not allowed at line @
vee	cdc	dely	found_dely_in_casn_not_allowed_cdcve	e					Found delay in continuous assignment which are not allowed at line @
vee	cdc	dely	dely_ignoring_dely_specification_cdcve	e					Delay Ignoring delay specification in Net Declaration at line @
vee	cdc	dely	dely_ignoring_dely_specification_port_cdcve	e					Delay Ignoring delay specification in Port Declaration at line @
vee	cdc	dely	dely_ignoring_dely_specification_sig_cdcve	e					Delay Ignoring delay specification in Signal Declaration at line @
vee	cdc	dely	dely_ignoring_dely_before_stmt_cdcve	e					Delay Ignoring delay before statement at line @
vee	cdc	dely	x_or_z_in_dely_cdcve	e					x or z in delay at line @
vee	cdc	dely	non_int_dely_cdcve	e					Non integer delay at line @
vee	cdc	dmsn	mem_prts_index_out_of_range_for_mem_cdcve	e					Memory part select [@:@] index @ out range for memory @ at line @
vee	cdc	dmsn	dime_select_for_mem_missing_cdcve	e					Select for memory @ missing at line @
vee	cdc	dmsn	dime_index_out_of_bounds_for_mem_cdcve	e					Index <index> out of bounds for memory @.

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									Range [@: @] at line @
vee	cdc	dmsn	dime_prts_out_of_bounds_for_net_cdcve	e					Part select [@ : @] out of bounds for net @. Range [@ : @] at line @
vee	cdc	dmsn	dime_prts_out_of_bounds_for_port_cdcve	e					Part select [@ : @] out of bounds for port @. Range [@ : @] at line @
vee	cdc	dmsn	dime_prts_out_of_bounds_for_sig_cdcve	e					Part select [@ : @] out of bounds for signal @. Range [@ : @] at line @
vee	cdc	dmsn	dime_prts_reg_cdcve	e					Part select [@ : @] reg @. Range [@ : @] at line @
vee	cdc	drvc	incompatible_drvc_for_net_cdcve	e					Incompatible drivers for Net @ at line @
vee	cdc	drvc	incompatible_drvc_for_port_cdcve	e					Incompatible drivers for Port @ at line @
vee	cdc	drvc	incompatible_drvc_for_sig_cdcve	e					Incompatible drivers for Signal @ at line @
vee	cdc	drvc	drvc_multiple_drive_net_partially_overlap_cdcve	e					Multiple drive Net partially overlap at line @
vee	cdc	drvc	drvc_multiple_drive_port_partially_overlap_cdcve	e					Multiple drive Port partially overlap at line @
vee	cdc	drvc	drvc_multiple_drive_sig_partially_overlap_cdcve	e					Multiple drive Signal partially overlap at line @
vee	cdc	dsgn	dsgn_top_mod_cannot_id_cdcve	e					Top module @ cannot be identified at line @
vee	cdc	dsgn	dsgn_top_entity_cannot_id_cdcve	e					Top entity @ cannot be identified at line @
vee	cdc	dsgn	dsgn_top_unit_cannot_id_cdcve	e					Top unit @ cannot be identified at line @
vee	cdc	dsgn	unit_dsgn_cycle_not_spanning_tree_cdcve	e					Unit design hierarchy contains a cycle. Hierarchy is not a spanning tree. at line @
vee	cdc	evc	not_allowed_edge_trigger_cdcve	e					Edge trigger is not allowed in this location at line @
vee	cdc	evc	ectl_in_assn_cdcve	e					Event control in assignement at line @
vee	cdc	expr	expr_prts_indices_1bit_var_cdcve	e					Part select indices 1-bit variable at line @
vee	cdc	expr	expr_prts_must_be_cst_expr_cdcve	e					Part select specifier Expression must be constant Expression at line @
vee	cdc	expr	not_const_expr_cdcve	e					Repetition multiplier in concatenation is not a constant Expression at line @
vee	cdc	expr	ill_bit_select_expr_cdcve	e					Illegal bit select expression @ at line @
vee	cdc	expr	equality_operator_detected_cdcve	e					Use of operator === detected at line @
vee	cdc	expr	notequal_operator_detected_cdcve	e					Use of operator !== detected at line @
vee	cdc	expr	ill_parm_value_cdcve	e					Illegal parameter value at line @
vee	cdc	expr	repetition_multiplier_in_conc_not_const_expr_cdcve	w					Repetition multiplier in concatenation is not a constant Expression at line @
vee	cdc	expr	int_operand_not_1_bit_cdcve	w					Logic operator has integer operands instead of 1-bit operands at line @
vee	cdc	expr	unsupp_expr_cdcve	w					Unsupported Expression type @ at line @
vee	cdc	expr	unsupp_operator_cdcve	w					Unsupported operator type @ at line @
vee	cdc	expr	use_of_sg_bit_const_cdcve	w					Use of single bit constant at line @
vee	cdc	expr	unary_op_in_comparison_cdcve	e					Unary op used in comparison at line @
vee	cdc	expr	nonconst_repeator_in_conc_cdcve	e					Non constant repeator in concatention at line @
vee	cdc	expr	x_or_z_in_cond_expr_cdcve	e					x or z in conditional expression at line @
vee	cdc	expr	zero_in_rep_in_conc_cdcve	e					Zero repeator in concatenation at line @
vee	cdc	expr	expr_in_mod_port_dir_cdcve	e					Expression @ in module port dir at line @
vee	cdc	expr	expr_in_ent_port_dir_cdcve	e					Expression @ in entity port dir at line @
vee	cdc	expr	expr_in_sig_port_dir_cdcve	e					Expression @ in unit port dir at line @
vee	cdc	expr	expr_in_inst_cdcve	e					Expression @ in inst i@ at line @
vee	cdc	expr	expr_operator_operands_unequal_lenght_cdcve	e					Expression operator @ operands @ unequal

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									length at line @
vee	cdc	file	cannot_open_filter_specification_file_cdcve	e					Cannot open filter specification file @ at line @
vee	cdc	file	filter_specification_file_missing_cdcve	e					Filter specification file name @ is missing at line @
vee	cdc	file	mismatch_mod_file_name_cdcve	e					Mismatch between module name @ and file name @ at line @
vee	cdc	file	mismatch_ent_file_name_cdcve	e					Mismatch between entity name @ and file name @ at line @
vee	cdc	file	mismatch_sig_file_name_cdcve	e					Mismatch between signal name @ and file name @ at line @
vee	cdc	forc	ill_forc_obj_type_cdcve	e					Illegal force object type @ at line @
vee	cdc	func	ill_func_return_type_cdv	e					Illegal function return type at line @
vee	cdc	func	ill_func_cdv	e					Illegal function @ at line @
vee	cdc	func	port_not_output_func_cdve	e					Port @ direction cannot be output at line @
vee	cdc	func	ill_use_func_cdcve	e					Illegal use of function @ at line @
vee	cdc	func	func_not_define_cdcve	e					Function @ not defined at line @
vee	cdc	func	too_many_arg_to_func_cdcve	e					Too many arguments passed to function @ at line @
vee	cdc	func	too_few_arg_to_func_cdcve	e					Too few arguments passed to function @ at line @
vee	cdc	func	undefined_func_cdcve	e					Undefined function @ at line @
vee	cdc	func	funct_expr_cannot_expnaded_cdcve	e					Function expression @ cannot be expanded at line @
vee	cdc	func	funct_not_used_in_expr_cdcve	w					Function @ is not being used in an Expression at line @
vee	cdc	func	func_decl_cdcve	w					Function Declaration @ already declared as another type at line @
vee	cdc	func	func_param_cdc	e					Found function parameter @ at line @
vee	cdc	func	unmatched_funct_param_cdcve	e					Unmatched function parameter @ at line @
vee	cdc	gate	ill_output_pin_name_gate_cdv	e					Illegal output terminal Expression pin @ at line @
vee	cdc	hid	cannot_locate_hier_id_hid_cdcve	e					Can't locate hierarchical identifier @ at line @
vee	cdc	hid	ref_minst_found_in_expr_hid_cdcve	e					References a module instance @ found in an Expression hid at line @
vee	cdc	hid	ref_entity_found_in_expr_hid_cdcve	e					References a entity instance @ found in an Expression hid at line @
vee	cdc	hid	ref_unit_found_in_expr_hid_cdcve	e					References a unit instance @ found in an Expression hid at line @
vee	cdc	hid	ref_in_eexpr_hid_cdcve	e					References a module instance @ passed as argument to PLI task call is also found in an Expression @ at line @
vee	cdc	hid	ref_in_expr_hid_cdcve	e					References a entity instance @ passed as argument to PLI task call is also found in an Expression @ at line @
vee	cdc	hid	reff_in_expr_hid_cdcve	e					References a unit instance @ passed as argument to PLI task call is also found in an Expression @ at line @
vee	cdc	hid	hid_name_traverses_into_func	e					Hid @ name traverses into a function @ at line @
vee	cdc	hid	hid_ref_mod_out_arg_sytk_cdcve	e					Hid @ referencing a module instance passed as 'out' type argument to a system task @ at line @
vee	cdc	hid	hid_ref_entity_out_arg_sytk_cdcve	e					Hid @ referencing a entity instance passed as 'out' type argument to a system task @ at line @
vee	cdc	hid	hid_ref_unit_out_arg_sytk_cdcve	e					Hid @ referencing a unit

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									instance passed as 'out' type argument to a system task @ at line @
vee	cdc	hid	hid_reference_not_found_cdcve	e					@ reference not found at line @
vee	cdc	hid	mifc_in_hid_not_exist_cdcve	e					Module instance @ in hid does not exist at line @
vee	cdc	hid	entity_instance_in_hid_not_exist_cdcve	e					Entity instance @ in hid does not exist at line @
vee	cdc	hid	unit_instance_in_hid_not_exist_cdcve	e					Unit instance @ in hid does not exist at line @
vee	cdc	hid	mod_found_in_path_in_dsgn_cdcve	e					Module @ found in path @ in the design at line @
vee	cdc	hid	enity_found_in_path_in_dsgn_cdcve	e					Entity @ found in path @ in the design at line @
vee	cdc	hid	unit_found_in_path_in_dsgn_cdcve	e					Unit @ found in path @ in the design at line @
vee	cdc	hid	hierarchical_id_path_contains_func_cdc	e					Hierarchical ID @ path contains a function at line @
vee	cdc	id	ill_terminal_id_cdv	e					Illegal terminal identifier at line @
vee	cdc	init	assn_mem_in_init_blk_cdcve	e					Assign memory in initial block at line @
vee	cdc	inst	inst_duplicate_mod_name_cdcve	e					Duplicate port @ in the port list for module @ at line @
vee	cdc	inst	inst_duplicate_entity_name_cdcve	e					Duplicate port @ in the port list for entity @ at line @
vee	cdc	inst	inst_duplicate_unit_name_cdcve	e					Duplicate port @ in the port list for unit @ at line @
vee	cdc	inst	miss_declparam_inst_cdv	e					Parameter Declaration missing value at line @
vee	cdc	inst	ill_mod_inst_name_cdcve	e					Illegal module instance @ at line @
vee	cdc	inst	ill_entity_inst_name_cdcve	e					Illegal entity instance @ at line @
vee	cdc	inst	ill_unit_inst_name_cdcve	e					Illegal unit instance @ at line @
vee	cdc	inst	inst_name_defined_mod_cdv	e					Instance name @ already defined in this module at line @
vee	cdc	inst	inst_name_defined_ent_cdv	e					Instance name @ already defined in this entity at line @
vee	cdc	inst	inst_name_defined_unit_cdv	e					Instance name @ already defined in this unit at line @
vee	cdc	inst	inst_too_many_bits_cdcve	e					Too many bits for port @ of instance array @, formal @, actual @ at line @
vee	cdc	inst	inst_port_not_connected_var_cdcve	e					Port 'port' of instance array 'array' is not connected to variable at line @
vee	cdc	inst	inst_insufficient_bits_cdcve	e					Insufficient bits for port 'port' of instance array 'array ', formal number, actual number at line @
vee	cdc	inst	inst_mod_name_not_defined_cdcve	e					Module name not defined at line @
vee	cdc	inst	inst_ent_name_not_defined_cdcve	e					Entity name not defined at line @
vee	cdc	inst	inst_unit_name_not_defined_cdcve	e					Unit name not defined at line @
vee	cdc	inst	many_mod_inst_param_assign_cdcve	e					Too many module instance parameter assignments (number > rrumber) at line @
vee	cdc	inst	many_entity_inst_param_assign_cdcve	e					Too many entity instance parameter assignments (number > rrumber) at line @
vee	cdc	inst	many_unit_inst_param_assign_cdcve	e					Too many unit instance parameter assignments (number > rrumber) at line @
vee	cdc	inst	complexexpr_cannot_mapped_inout_port_cdcve	e					Complex Expression @ cannot be mapped to inout port @ at line @
vee	cdc	inst	complexexpr_cannot_mapped_unknown_port_cdcve	e					Complex Expression @ cannot be mapped to unknown type port @ at line @
vee	cdc	inst	netdecl_contains_ill_prts_cdcve	e					Net Declaration [@: @] contains an illegal part select at line @
vee	cdc	inst	regdecl_contains_ill_prts_cdcve	e					Reg Declaration [@ : @]

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									contains an illegal part select at line @
vee	cdc	inst	complex_expr_inst_parent_module_cdcve	e					Complex actual Expression associated with port @ of module @ instantiated in parent module at line @
vee	cdc	inst	complex_expr_inst_entity_parent_module_cdcve	e					Complex actual Expression associated with port @ of entity @ instantiated in parent module at line @
vee	cdc	inst	complex_expr_inst_unit_parent_module_cdcve	e					Complex actual Expression associated with port @ of unit @ instantiated in parent module at line @
vee	cdc	inst	inst_mod_output_port_width_cdcve	e					Mod @ Output port @ width mismatch, actual-width (port-width) at line @
vee	cdc	inst	inst_entity_output_port_width_cdcve	e					Entity @ Output port @ width mismatch, actual-width (port-width) at line @
vee	cdc	inst	inst_unit_output_port_width_cdcve	e					Unit @ Output port @ width mismatch, actual-width (port-width) at line @
vee	cdc	inst	inst_mod_input_port_width_cdcve	e					Mod @ Input port @ width mismatch, actual-width (port-width) at line @
vee	cdc	inst	inst_entity_input_port_width_cdcve	e					Entity @ Input port @ width mismatch, actual-width (port-width) at line @
vee	cdc	inst	inst_unit_input_port_width_cdcve	e					Unit @ Input port @ width mismatch, actual-width (port-width) at line @
vee	cdc	inst	inst_mod_not_define_cdcve	e					Module not defined at line @
vee	cdc	inst	inst_entity_not_define_cdcve	e					Entity not defined at line @
vee	cdc	inst	inst_unit_not_define_cdcve	e					Unit not defined at line @
vee	cdc	inst	miss_mifc_name_cdcve	w			x		Missing module instance name. This syntax is an error according to IEEE 1364-1995 but is allowed by commercial Verilog compilers at line @
vee	cdc	inst	miss_ent_instance_name_cdcve	w			x		Missing entity instance name. This syntax is an error according to IEEE 1364-1995 but is allowed by commercial Verilog compilers at line @
vee	cdc	inst	miss_unit_instance_name_cdcve	w			x		Missing unit instance name. This syntax is an error according to IEEE 1364-1995 but is allowed by commercial Verilog compilers at line @
vee	cdc	inst	mifc_port_actual_formal_width_mismatch_cdcve	w					Module @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vee	cdc	inst	ent_port_actual_formal_width_mismatch_cdcve	w					Entity @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vee	cdc	inst	unit_port_actual_formal_width_mismatch_cdcve	w					Unit @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vee	cdc	inst	unmatched_port_connect_in_inst_cdcve	e					Unmatched port @ connect in instance @ at line @
vee	cdc	inst	inst_differs_in_case_from_mod_cdcev	e					Instance name @ differs in case from module name @ at line @
vee	cdc	inst	inst_differs_in_case_from_ent_cdcve	e					Instance name @ differs in case from entity name @ at line @
vee	cdc	inst	inst_differs_in_case_from_sig_cdcve	e					Instance name @ differs in case from signal name @ at line @
vee	cdc	lib	lib_name_not_mod_declaration_cdv	e					Library file @ doesn't contain a module Declaration at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	cdc	lib	lib_name_not_entity_declaration_cdv	e					Library file @ doesn't contain a entity Declaration at line @
vee	cdc	lib	lib_name_not_unit_declaration_cdv	e					Library file @ doesn't contain a unit Declaration at line @
vee	cdc	lib	lib_not_contain_supply_cdcve	e					Library does not contain supply @ at line @
vee	cdc	loop	initial_value_unknown_loop_cdcve	e					While control initial variable @ unassigned. Initial value unknown at line @
vee	cdc	loop	while_loop_not_assign_stmt_controlvar_cdcve	e					While loop body does not contain an assignment statement for control variable @ at line @
vee	cdc	loop	assign_stmt_not_last_while_loop_cdcve	e					Assignment statement for control variable @ not last statement in while loop at line @
vee	cdc	loop	undet_init_value_loop_cdcve	e					Unable to determine init value for loop at line @
vee	cdc	loop	undet_limit_loop_cdcve	e					Unable to determine limit for loop at line @
vee	cdc	loop	loop_bounds_calculated_int_cdcve	w					Loop bounds are calculated to be integer @, check that this is correct at line @
vee	cdc	loop	expr_lhs_contains_var_bit_select_cdcve	w					Expression in lhs of assignment contains a variable bit select at line @
vee	cdc	loop	loop_bounds_not_const_cdc	w					Loop bounds are non-constant at line @
vee	cdc	loop	loop_ctrl_init_expr_not_const_cdcve	w					Non-constant loop bound. Loop control variable initialization Expression is not a constant Expression at line @
vee	cdc	loop	loop_term_expr_not_const_cdcve	w					Non-constant loop bound. loop terminating Expression could not be evaluated to a constant at line @
vee	cdc	loop	init_expr_reset_by_var_cdcve	e					Non-constant loop bound. initializing Expression reset by variable at line @
vee	cdc	loop	loop_ctrl_var_1_bit_wide_cdcve	w					The loop control variable @ is one bit wide. Check the loop control variable Declaration. at line @
vee	cdc	mdb	bad_mdb_net_cdcve	e					Bad multi-driven Net @ at line @
vee	cdc	mdb	bad_mdb_port_cdcve	e					Bad multi-driven Port @ at line @
vee	cdc	mdb	bad_mdb_signal_cdcve	e					Bad multi-driven Signal @ at line @
vee	cdc	mdb	unsupp_comp_mdb_net_cdcve	e	?				Unsupported component type @ driving in multi-driven Net name at line @
vee	cdc	mdb	unsupp_comp_mdb_port_cdcve	e	?				Unsupported component type @ driving in multi-driven Port name at line @
vee	cdc	mdb	unsupp_comp_mdb_signal_cdcve	e	?				Unsupported component type @ driving in multi-driven Signal name at line @
vee	cdc	mdb	unsupp_comp_drive_mdb_cdcve	e	?				Unsupported component type @ driving multi-driven Net natne at line @
vee	cdc	mdb	unsupp_comp_drive_mdb_port_cdcve	e	?				Unsupported component type @ driving multi-driven Port natne at line @
vee	cdc	mdb	unsupp_comp_drive_mdb_signal_cdcev	e	?				Unsupported component type @ driving multi-driven Signal natne at line @
vee	cdc	mdb	mdb_net_driven_by_trns_cdcve	e					Multiply driven Net driven by transistor primitive type @ at line @
vee	cdc	mdb	mdb_port_driven_by_trns_cdcve	e					Multiply driven Port driven by transistor primitive type @ at line @
vee	cdc	mdb	mdb_sig_driven_by_trns_cdcve	e					Multiply driven Signal

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									driven by transistor primitive type @ at line @
vee	cdc	mdb	mdb_unsupp_comp_drvs_net_cdcve	e					Unsupported component type driving Net drives Net connected to multi-driven Net at line @
vee	cdc	mdb	mdb_unsupp_comp_drvs_port_cdcve	e					Unsupported component type driving Port drives Port connected to multi-driven Port at line @
vee	cdc	mdb	mdb_unsupp_comp_drvs_sig_cdcve	e					Unsupported component type driving Signal drives Signal connected to multi-driven Signal at line @
vee	cdc	mdb	mdb_incompatible_net_drives_multiple_net_cdcve	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Net at line @
vee	cdc	mdb	mdb_incompatible_port_drives_multiple_port_cdcve	e					Incompatible driver driving tandem Port drives Port connected to multi-driven Port at line @
vee	cdc	mdb	mdb_incompatible_sig_drives_multiple_sig_cdcve	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Port at line @
vee	cdc	mdb	mdb_unsupp_LHS_concatenation_cdcve	e					Unsupported LHS concatenation in multi-drive 'device at line @
vee	cdc	mdb	mdb_bus_has_too_many_drivers_cdcve	e					Bus has too many drivers. at line @
vee	cdc	mdb	mdb_always_blk_drive_cdcve	w					Multiple always blocks drive name @ at line @
vee	cdc	mdb	nontri_gate_drives_mdb_net_cdcve	w					non-tri-state gate drives multi-driven Net at line @
vee	cdc	mdb	nontri_gate_drives_mdb_port_cdcve	w					non-tri-state gate drives multi-driven Port at line @
vee	cdc	mdb	nontri_gate_drives_mdb_sig_cdcve	w					non-tri-state gate drives multi-driven Signal at line @
vee	cdc	mem	mem_prts_cdve	e					Memories do not support part select specifier at line @
vee	cdc	mem	ill_ref_mem_name_cdv	e					Illegal hid reference to memory (name) at line @
vee	cdc	mem	mem_ref_without_index_cdcve	e					Memory @ referenced without index through hierarchical ID @ at line @
vee	cdc	mifc	mifc_not_array_cdve	e					Ports may not be an array at line @
vee	cdc	mifc	port_identifier_mifc_cdcve	e					Port @ at line @
vee	cdc	mifc	mifc_mod_input_port_decl_as_reg_cdcve	e					Module @ input port @ declared as type reg at line @
vee	cdc	mifc	mifc_entity_input_port_decl_as_reg_cdcve	e					Entity @ input port @ declared as type reg at line @
vee	cdc	mifc	mifc_unit_input_port_decl_as_reg_cdcve	e					Unit @ input port @ declared as type reg at line @
vee	cdc	mifc	mod_output_wire_redecl_reg_cdcve	e					Module @ output port re-declared as type reg after use as implicitly declared wire at line @
vee	cdc	mifc	entity_output_wire_redecl_reg_cdcve	e					Entity @ output port re-declared as type reg after use as implicitly declared wire at line @
vee	cdc	mifc	unit_output_wire_redecl_reg_cdcve	e					Unit @ output port re-declared as type reg after use as implicitly declared wire at line @
vee	cdc	mifc	output_port_is_mem_type_mifc_cdcve	e					Output port @ is memory type at line @
vee	cdc	mifc	mifc_inout_port_is_mem_type_cdcve	e					Inout port @ is memory type at line @
vee	cdc	mifc	mod_output_port_mismatch_actual_witdh_cdcve	w					Module @ output port @ formal to actual width mismatch at line @
vee	cdc	mifc	ent_output_port_mismatch_actual_witdh_cdcve	w					Entity @ output port @ formal to actual width mismatch at line @
vee	cdc	mifc	unit_output_port_mismatch_actual_witdh_cdc	w					Unit @ output port @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									formal to actual width mismatch at line @
vee	cdc	mifc	port_name_different_in_upper_lower_case_cdcve	e					Port name @ different in upper lower case at line @
vee	cdc	mifc	port_not_def_in_iodecl_cdcve	e					Port @ not defined in ioDeclaration at line @
vee	cdc	mifc	port_not_def_in_portl_cdcve	e					Port @ not defined in port list at line @
vee	cdc	mifc	port_wiredecl_mismatch_cdcve	e					Port @ wireDeclaration mismatch at line @
vee	cdc	mifc	pos_based_null_inst_port_cdcve	e					Position based null instance port at line @
vee	cdc	mifc	last_portdecl_contains_trailcomma_cdcve	e					Last portDeclaration contains a trailing comma at line @
vee	cdc	mins	mins_expr_incompatible_type_cdcve	e					Expression @ has an incompatible argument type @ with the port at line @
vee	cdc	mins	mins_mod_not_exist_cdcve	e					Module @ does not exist at line @
vee	cdc	mins	mins_entity_not_exist_cdcve	e					Entity @ does not exist at line @
vee	cdc	mins	mins_unit_not_exist_cdcve	e					Unit @ does not exist at line @
vee	cdc	mins	undefined_instance_cdcve	e					Undefined instance @ at line @
vee	cdc	mod	mod_param_bad_number_cdv	e					Module name @ parameter list contains an Incorrect number of parameter overrides at line @
vee	cdc	mod	mod_entity_param_bad_number_cdv	e					Entity name @ parameter list contains an Incorrect number of parameter overrides at line @
vee	cdc	mod	mod_unit_param_bad_number_cdv	e					Unit name @ parameter list contains an Incorrect number of parameter overrides at line @
vee	cdc	mod	ill_mod_name_cdcve	e					Illegal module @ at line @
vee	cdc	mod	ill_mod_entity_name_cdcve	e					Illegal entity @ at line @
vee	cdc	mod	ill_mod_unit_name_cdcve	e					Illegal unit @ at line @
vee	cdc	mod	mod_mult_decl_string_cdcve	e					Multiple Declarations of string detected in module @ at line @
vee	cdc	mod	mod_entity_mult_decl_string_cdcve	e					Multiple Declarations of string detected in entity @ at line @
vee	cdc	mod	mod_unit_mult_decl_string_cdcve	e					Multiple Declarations of string detected in unit @ at line @
vee	cdc	mod	mod_mult_def_cdcve	e					Module @ defined in multiple places at line @
vee	cdc	mod	mod_ent_mult_def_cdcve	e					Entity @ defined in multiple places at line @
vee	cdc	mod	mod_unit_mult_def_cdcve	e					Unit @ defined in multiple places at line @
vee	cdc	mod	mod_no_module_found_cdcve	e					No modules found at line @
vee	cdc	mod	mod_no_entity_found_cdcve	e					No entity found at line @
vee	cdc	mod	mod_no_unit_found_cdcve	e					No unit found at line @
vee	cdc	mod	failed_find_mod_cdcve	e					Failed to find module @ at line @
vee	cdc	mod	failed_find_entity_cdcve	e					Failed to find entity @ at line @
vee	cdc	mod	failed_find_unit_cdcve	e					Failed to find unit @ at line @
vee	cdc	mod	undefined_mod_cdcve	e					Undefined module @ at line @
vee	cdc	mod	undefined_ent_cdcve	e					Undefined entity @ at line @
vee	cdc	mod	undefined_unit_cdcve	e					Undefined unit @ at line @
vee	cdc	mod	unexpandable_macromodule_cdcve	e					Unexpandable macromodule @ at line @
vee	cdc	mod	non_interconnect_in_hierarchical_mod_cdcve	e					Non interconnect in hierarchical module @ at line @
vee	cdc	mod	non_interconnect_in_hierarchical_ent_cdcve	e					Non interconnect in hierarchical entity @ at line @
vee	cdc	mod	non_interconnect_in_hierarchical_sig_cdcve	e					Non interconnect in hierarchical signal @ at line @
vee	cdc	mod	empty_mod_cdcve	e					Empty module at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	cdc	mod	empty_ent_cdcve	e					Empty entity at line @
vee	cdc	mod	empty_unit_cdcve	e					Empty unit at line @
vee	cdc	net	namereg_not_on_LHS_stmt_net_cdv	e					Register @ cannot be used on LHS of this assignment statement at line @
vee	cdc	net	net_implicit_wire_redecl_reg_cdcve	e					Implicitly declared as a wire @ re-declared as a reg @. at line @
vee	cdc	net	time_var_decl_cdcve	e					Time variable @ declared at line @
vee	cdc	net	time_var_bit_used_cdcve	e					Time variable @ bit used at line @
vee	cdc	net	undecl_net_in_mod_cdcve	e					Undeclared net @ in module @ at line @
vee	cdc	net	undecl_port_in_mod_cdcve	e					Undeclared port @ in module @ at line @
vee	cdc	net	undecl_sig_in_mod_cdcve	e					Undeclared signal @ in module @ at line @
vee	cdc	net	undecl_net_in_ent_cdcve	e					Undeclared net @ in entity @ at line @
vee	cdc	net	undecl_port_in_ent_cdcve	e					Undeclared port @ in entity @ at line @
vee	cdc	net	undecl_sig_in_ent_cdcve	e					Undeclared signal @ in entity @ at line @
vee	cdc	net	undecl_net_in_sig_cdcve	e					Undeclared net @ in signal @ at line @
vee	cdc	net	undecl_port_in_sig_cdcve	e					Undeclared port @ in signal @ at line @
vee	cdc	net	undecl_sig_in_sig_cdcve	e					Undeclared signal @ in signal @ at line @
vee	cdc	net	port_used_prior_to_decl_cdcve	e					Port @ used prior toDeclaration at line @
vee	cdc	net	1bit_with_prts_cdcve	e					1-bit with part select at line @
vee	cdc	netd	ill_decl_vec_cdcve	e					Illegal Declaration of vector @ at line @
vee	cdc	nett	nett_ill_reg_name_cdcve	e					Illegal register @ at line @
vee	cdc	nett	nett_ill_net_name_cdcve	e					Illegal net @ at line @
vee	cdc	nett	nett_ill_port_name_cdcve	e					Illegal port @ at line @
vee	cdc	nett	nett_ill_signal_name_cdcve	e					Illegal signal @ at line @
vee	cdc	nett	net_scalar_vect_nett_cdcve	e					Net declared as both scalar and vector at line @
vee	cdc	nett	port_scalar_vect_nett_cdcve	e					port declared as both scalar and vector at line @
vee	cdc	nett	signal_scalar_vect_nett_cdcve	e					Signal declared as both scalar and vector at line @
vee	cdc	nett	hot_mux_not_use_bus_connection_net_cdcve	e					One hot mux can not be used for bus connection between modules Net @ at line @
vee	cdc	nett	hot_mux_not_use_bus_connection_port_cdcve	e					One hot mux can not be used for bus connection between modules Port @ at line @
vee	cdc	nett	hot_mux_not_use_bus_connection_sig_cdcve	e					One hot mux can not be used for bus connection between modules Signal @ at line @
vee	cdc	nett	reg_connected_inst_inout_cdcve	e					Reg @ connnected to instantiation @ inout @ at line @
vee	cdc	nett	ill_net_in_proc_assn_cdcve	e					Illegal net type type in procedural assignement at line @
vee	cdc	nett	ill_port_in_proc_assn_cdcve	e					Illegal port type type in procedural assignement at line @
vee	cdc	nett	ill_sig_in_proc_assn_cdcve	e					Illegal signal type type in procedural assignement at line @
vee	cdc	num	not_allowed_width0_num_cdcve	e					Width 0 not allowed for sized number at line @
vee	cdc	num	real_num_not_allowed_cdcve	e					Real numbers not allowed at line @
vee	cdc	num	found_x_z_in_num_literal_cdcve	e					Found x and/or z value in number literal at line @
vee	cdc	num	too_many_digits_in_sized_num_cdcve	w					Number of digits exceeds the width in a sized number at line @
vee	cdc	num	divide_by_zero_num_cdcve	e					Divide by zero at line @
vee	cdc	num	child_mod_inst_parent_mod_cdcve	e					Child module @ instantiates parent module @ at line @
vee	cdc	num	child_ent_inst_parent_ent_cdcve	e					Child entity @ instantiates entity module

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									@ at line @
vee	cdc	num	child_sig_inst_parent_sig_cdcve	e					Child signal @ instantiates signal module @ at line @
vee	cdc	num	int_decl_incorrect_cdcve	e					Integer Declaration incorrect at line @
vee	cdc	num	int_var_indexed_cdcve	e					Integer variable inedexed at line @
vee	cdc	parm	parm_redecl_as_reg_name_cdv	e					Parameter re-declared as reg @ at line @
vee	cdc	parm	parm_redecl_as_port_port_cdv	e					Parameter re-declared as port @ at line @
vee	cdc	parm	parm_redecl_as_net_name_cdv	e					Parameter re-declared as Net @ at line @
vee	cdc	parm	parm_redecl_as_port_name_cdv	e					Parameter re-declared as Port @ at line @
vee	cdc	parm	parm_redecl_as_signal_name_cdv	e					Parameter re-declared as Signal @ at line @
vee	cdc	parm	duplicate_decl_parm_name_cdv	e					Duplicate declaration of parameter name @ at line @
vee	cdc	parm	ill_parm_identifier_cdcve	e					Illegal parameter @ at line @
vee	cdc	parm	value_of_parm_OS_platform_dependent_cdcve	w					Parameter select width > 32. The value is OS and platform dependent at line @
vee	cdc	parm	parm_redefined_cdcve	w					Parameter @ redefined at line @
vee	cdc	pars	endfunction_miss_cyb_cdv	e					Endfunction missing at line @
vee	cdc	pars	endtask_miss_pars_cdv	e					Endtask missing at line @
vee	cdc	pars	endmodule_miss_pars_cdc	e					Endmodule missing at line @
vee	cdc	pars	miss_cont_assign_pars_cdc	e					Missing = sign for continuous assignment at line @
vee	cdc	pli	user_syst_not_listed_in_pli_table_cdcve	e					User system task @ is not listed in PLI table at line @
vee	cdc	port	ill_formal_port_name_cdcve	e					Illegal formal port @ at line @
vee	cdc	pp	text_redefined_replaced_cdcve	w					Text macro redefined and replaced @. Previous definition filename, line number @ New definition filename, line number @ at line @
vee	cdc	pp	undefined_macro_cdcve	e					Undefined macro @ at line @
vee	cdc	pp	include_file_contains_nonconst_cdcve	e					Include file contains non constant @ at line @
vee	cdc	pp	endif_or_else_without_ifdef_cdcve	e					Endif-or-else-without ifdef at line @
vee	cdc	prim	z_in_prim_inst_cdcve	e					z in primitive instantiation at line @
vee	cdc	prim	prim_instan_cdcve	e					Primitive instantiation @ at line @
vee	cdc	proc	proc_blk_missing_evc_cdcve	e					Always block missing event control at line @
vee	cdc	prts	type_prts_cdve	e					Type @ does not support part select specifier at line @
vee	cdc	prts	prts_out_of_range_cdcve	e					Parameter @[@ : @]part select is out of range at line @
vee	cdc	prts	ill_prts_inst_array_cdcve	e					Illegal value for part select of instance array 'name' at line @
vee	cdc	prts	const_prts_contains_non_const_selector_cdcve	e					Constant part select @ contains a non-constant selector @ at line @
vee	cdc	prts	bus_index_prts_for_var_out_of_range_cdcve	e					Bus index @ integer of part select [@:@] for variable @ out of range at line @
vee	cdc	prts	bus_prts_for_var_out_of_range_cdcve	e					Bus part select [@:@] for variable @ out of range at line @
vee	cdc	prts	bus_prts_index_out_of_name_for_var_cdcve	e					Bus part select [@:@] index @ out of range for variable @ at line @
vee	cdc	prts	ill_token_in_prts_cdcve	e					Illegal token in part select @ at line @
vee	cdc	prts	incomplete_prts_specification_cdcve	e					Incomplete part select specification @ at line @
vee	cdc	prts	ill_index_in_prts_cdcve	e					Illegal index in part select @ at line @
vee	cdc	prts	negative_index_in_prts_not_allowed_cdcve	e					Negative index in part

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									select @ not allowed at line @
vee	cdc	prts	prts_index_order_reversed_cdcve	e					Part select index order reversed [@ : @] [@ : @] should be [@ : @] at line @
vee	cdc	prts	index_vec_over_max_size_cdcve	w					Vector index @ exceeds the size of the vector. Index truncated at line @
vee	cdc	prts	x_or_z_in_vec_bit_select_index_cdcve	e					x or z in vector bit select index at line @
vee	cdc	real	real_cdcve	e					Real @ at line @
vee	cdc	real	real_in_assn_cdcve	e					Real @ in assignement at line @
vee	cdc	real	real_in_csi_cdcve	e					Real @ inCase item at line @
vee	cdc	real	real_in_comparaison_cdcve	e					Real @ in comparaison at line @
vee	cdc	rel	ill_rel_obj_type_cdcve	e					Illegal release object type type at line @
vee	cdc	scop	var_erd_in_scope_cdcve	e					Variable @ redfined in scope @ at line @
vee	cdc	simr	inefficient_op_not_a_power_of_2_cdcve	e					Division/modulus by a number not a power of 2. Inefficient simulation operation. at line @
vee	cdc	simr	simr_multiple_init_blk_force_cdcve	w					Multiple initial blocks force @. Unpredictable simulation result at line @
vee	cdc	snsl	incomplete_snsl_cdcve	w					Incomplete sensitivity list. @ is not in the sensitivity list. at line @
vee	cdc	snsl	edge_sns_process_contains_data_pin_snsl_cdcve	e					Edge sensitive process contains a data pin @ in the sensitivity list at line @
vee	cdc	snsl	unsupp_expr_in_snsl_cdcve	w					Unsupported Expression type @ in sensitivity list ' at line @
vee	cdc	snsl	always_blk_is_miss_snsl_cdcve	e					Always block is missing sensitivity list at line @
vee	cdc	snsl	not_all_bits_snsvar_used_cdc	e					Not all bus bits of sensitivity variable @ are used in process at line @
vee	cdc	snsl	partial_bus_decl_width_cdcve	e	?				partial bus @ declared with width @ width @ at line @
vee	cdc	snsl	contains_inst_name_cdcve	e					Contains instance name @ at line @
vee	cdc	snsl	bus_indexed_in_snsl_cdcve	e					Bus @ indexed in sensitivity list at line @
vee	cdc	stmt	ill_register_assign_cdv	e					Illegal register assignment statement at line @
vee	cdc	stmt	null_not_allowed_stmt_cdcve	e					Null statement is not allowed here at line @
vee	cdc	stmt	id_expected_FHSexpr_force_stmt_cdcve	e					Simple identifier expected for LHS Expression in force-statement at line @
vee	cdc	stmt	id_expected_FHSexpr_release_stmt_cdcve	e					Simple identifier expected for LHS Expression in release-statement at line @
vee	cdc	stmt	stmt_ill_accept_only_net_reg_mem_cdcve	e					Illegal type @ can only accept net, reg, memory at line @
vee	cdc	stmt	stmt_ill_accept_only_port_reg_mem_cdcve	e					Illegal type @ can only accept port, reg, memory at line @
vee	cdc	stmt	stmt_ill_accept_only_signal_reg_mem_cdcve	e					Illegal type @ can only accept signal, reg, memory at line @
vee	cdc	stmt	while_stmt_usage_disc_cdcve	w					While statement usage discouraged at line @
vee	cdc	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_cdcve	e					Arithmetic operator RHS has one less bit than the LHS at line @
vee	cdc	stmt	ar_op_unequal_lhs_rhs_cdcve	e					Arithmetic operator unequal width LHS and RHS at line @
vee	cdc	stmt	ar_op_unequal_var_on_rhs_cdc	e					Arithmetic operator unequal width variables @ on RHS at line @
vee	cdc	stmt	empty_stmt_cdc	e					Empty-statement at line @
vee	cdc	syst	ill_syst_task_arg_cdcve	e					Illegal system task @ Argument @ at line @
vee	cdc	syst	csdir_converts_syts_cdcve	w				x	Lower case converts the

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									system task $realtime return value to an integer at line @
vee	cdc	syst	return_var_of_user_used_as_rhs_cdcve	w					Return variable of user system task is used as a RHS variable at line @
vee	cdc	task	miss_task_name_stmst_body_cdv	e					Task @ body statement missing at line @
vee	cdc	task	ill_task_cdv	e					Illegal task @ at line @
vee	cdc	task	ill_use_task_cdcve	e					Illegal use of task @ at line @
vee	cdc	task	ask_var_not_decl_cdcve	e					Variable @ used but not declared at line @
vee	cdc	task	task_not_defined_cdcve	e					Task @ not defined at line @
vee	cdc	task	too_few_arg_to_task_cdcve	e					Too few arguments passed to task @ at line @
vee	cdc	task	undefined_task_cdcve	e					Undefined task @ at line @
vee	cdc	task	syts_output_port_drvs_nonsqs_logic_comp_cdcve	w					User system task output port drives non-sequential logic component at line @
vee	cdc	task	undefioned_task_	e					Undefined task @ at line @
vee	cdc	task	task_decl_error_vhve	e					Task declaration error at line @
vee	cdc	task	func_task_parm_cdcve	e					Found function parameter @ at line @
vee	cdc	task	unmatched_task_param_cdcve	e					Unmatched task parameter @ at line @
vee	cdc	tbcd	found_forever_tbcd_cdcve	e					Found forever at line @
vee	cdc	tbcd	behavioral_code_mod_cdcve	e					Behavioral code in module @ at line @
vee	cdc	tbcd	behavioral_code_ent_cdcve	e					Behavioral code in entity @ at line @
vee	cdc	tbcd	behavioral_code_unit_cdcve	e					Behavioral code in unit @ at line @
vee	cdc	tri	instance_not_tri_state_device_cdcve	e					Instance name is not a tri-state device at line @
vee	cdc	tri	unsupp_gate_type_tristate_cdcve	e					Unsupported gate type @ used for tristate at line @
vee	cdc	tri	tri_not_desgn_gate_contention_cdcve	e					Tristate not designed correctly gate @ can cause contention at line @
vee	cdc	tri	unsupp_type_instance_tri_cdcve	e					Unsupported type instance type used for tristate @ at line @
vee	cdc	tri	incorrect_cont_assign_stmt_tri_gate_cdcve	e					Incorrect continuous assign statement for tristate gate @ at line @
vee	cdc	tri	const_assign_to_multidriven_net_cdcve	e					Constant (constiznt) assigned to multi-driven Net @ at line @
vee	cdc	tri	const_assign_to_multidriven_port_cdcve	e					Constant (constiznt) assigned to multi-driven Port @ at line @
vee	cdc	tri	const_assign_to_multidriven_signal_cdcve	e					Constant (constiznt) assigned to multi-driven Signal @ at line @
vee	cdc	tri	unsupp_expr_for_tri_cdcve	e					Unsupported Expression type @ for tristate at line @
vee	cdc	unsy	cs_equality_op_cdcve	e					Case equality operator == at line @
vee	cdc	unsy	deassign_stmt_cdcve	e					Deassign statement at line @
vee	cdc	unsy	defparam_cdcve	e					Defparam at line @
vee	cdc	unsy	dely_ctrl_cdcve	e					Delay control at line @
vee	cdc	unsy	ev_ctrl_cdcve	e					Event control at line @
vee	cdc	unsy	time_decl_cdcve	e					Time Declaration at line @
vee	cdc	unsy	wait_stmt_unsy_cdcve	e					Wait statement at line @
vee	csa	assn	unequal_length_lhs_rhs_csve	e					Unequal length LHS and RHS at line @
vee	csa	assn	unequal_length_lhs_rhs_off_one_bit_csve	e					Unequal length LHS and RHS off by one bit at line @
vee	csa	blk	repeat_in_nonblk_assn_csve	e					Repeat in non-blocking assignment at line @
vee	csa	blk	empty_blk_csve	e					Empty-block at line @
vee	csa	clk	unsupp_logic_operation_csve	w					Unsupported logic operation type @. at line @
vee	csa	clk	unsupp_cl_gated_logic_csve	w					Unsupported gated clock logic type. at line @
vee	csa	clk	unsupp_logic_expr_clk_csve	w					Unsupported

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									logicExpression type @ at line @
vee	csa	csi	duplicate_csi_csve	e					Duplicate Case item @ at line @
vee	csa	csi	case_sel_contains_real_num_const_csve	e					Case selector contains a constant real number at line @
vee	csa	csi	csi_contains_real_num_const_csve	e					Case item contains a constant real number at line @
vee	csa	csi	real_in_csi_csve	e					Real @ in case item at line @
vee	csa	csi	noncnst_in_iclude_file_csve	e					Non-constant in include file @ at line @
vee	csa	csi	csi_width_mismatch_csve	e					Case item @ width mismatch at line @
vee	csa	csi	efault_missing_csve	e					Default missing at line @
vee	csa	css	not_all_csi_specified_csve	e					Not allCase items are specified @ at line @
vee	csa	defd	mod_def_within_mod_not_in_include_csde	e					Module define within module but not in include at line @
vee	csa	defd	ent_def_within_ent_not_in_include_csde	e					Entity define within entity but not in include at line @
vee	csa	defd	unit_def_within_unit_not_in_include_csde	e					Unit define within unit but not in include at line @
vee	csa	dely	comb_blk_contains_dely_assn_csve	e					Combinational block contains delay assignement at line @
vee	csa	dely	seq_blk_contains_dely_assn_csde	e					Sequential block contains delay assignement at line @
vee	csa	dely	comb_blk_dely_between_stms_csve	e					Combinational block contains delay between statements at line @
vee	csa	dely	seq_blk_dely_between_stmt_csve	e					Sequential block contains delay between statements at line @
vee	csa	dely	dely_in_nonblk_assn_comb_cscve	e					Delay in nonblocking assignement in combinational at line @
vee	csa	dely	dely_in_nonblk_assn_seq_csve	e					Delay in nonblocking assignement in sequential at line @
vee	csa	drst	drvs_not_in_lib_csve	e					Drive strength @ not in library at line @
vee	csa	drvc	output_arg_appers_rhs_csve	w					Output argument @ of user system task appears in RHS and is driven elsewhere at line @
vee	csa	drvc	multiple_init_blk_drvc_csve	w					Multiple initial blocks force 'narne' at line @
vee	csa	drvc	net_multiple_always_blk_csve	w					Net @ multiple always blocks at line @
vee	csa	drvc	port_multiple_always_blk_csve	w					Port @ multiple always blocks at line @
vee	csa	drvc	sig_multiple_always_blk_csve	w					Signal @ multiple always blocks at line @
vee	csa	drvc	net_multiple_stmt_csve	w					Net @ multiple statements with in the same always at line @
vee	csa	drvc	port_multiple_stmt_csve	w					Port @ multiple statements with in the same always at line @
vee	csa	drvc	sig_multiple_stmt_csve	w					Signal @ multiple statements with in the same always at line @
vee	csa	drvc	multiply_drvn_net_nontri_gate_csve	w					Multiply drivenNet driven by a non-tristate gate at line @
vee	csa	drvc	multiply_drvn_port_nontri_gate_csve	w					Multiply drivenPort driven by a non-tristate gate at line @
vee	csa	drvc	multiply_drvn_sig_nontri_gate_csve	w					Multiply drivenSignal driven by a non-tristate gate at line @
vee	csa	drvc	incompatible_driver_net_csve	w					Incompatible driver of type @ drivingNet_@ multi drivenNet of type @ name @ at line @
vee	csa	drvc	incompatible_driver_port_csve	w					Incompatible driver of type @ drivingPort_@ multi drivenPort of type @ name @ at line @
vee	csa	drvc	incompatible_driver_sig_csve	w					Incompatible driver of type @ drivingSignal_@ multi drivenSignal of type @ name @ at line @
vee	csa	dsbl	dsbl_used_csev	e					Disable used at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	csa	evc	embedded_ectl_csve	e					Embedded-event-control at line @
vee	csa	expr	unary_op_in_comparison_csve	e					Unary op used in comparison at line @
vee	csa	expr	shift_by_non_const_csve	e					Shift by non constant @ at line @
vee	csa	expr	miss_parenthesis_csve	e					Unary op @ with comparison op @ missing precedence parenthesis at line @
vee	csa	forc	no_release_stmt_in_init_blk_csve	w					Force @ statement in the initial block and there is no release statement.for @ at line @
vee	csa	forc	no_force_stmt_in_init_blk_csve	w	?				Release @ statement in the and there is no force statement.for @ at line @
vee	csa	forc	forcing_input_port_csve	e					Forcing input port @ at line @
vee	csa	func	return_value_not_at_end_of_func_csve	e					Return value not at end of function at line @
vee	csa	func	time_and_evctrl_in_func_csve	e					Time and event control in function at line @
vee	csa	func	func_call_itself_rec_csve	e					Function @ calling itself recursively at line @
vee	csa	gate	error_output_terminal_csve	w			x		IEEE 1364-1995 error output terminal @. This will compile and simulate correctly on commercial verilog simulators at line @
vee	csa	init	assn_mem_in_init_blk_csve	e					Assign memory in initial block at line @
vee	csa	inst	input_port_drvn_from_inside_mod_csve	e					Input port @ being driven from inside of module @ at line @
vee	csa	inst	input_port_drvn_from_inside_entity_csve	e					Input port @ being driven from inside of entity @ at line @
vee	csa	inst	input_port_drvn_from_inside_signal_csve	e					Input port @ being driven from inside of signal @ at line @
vee	csa	inst	input_port_not_connected_in_parent_mod_csve	e					Input port @ not connected in parent module at line @
vee	csa	inst	input_port_not_connected_in_parent_entity_csve	e					Input port @ not connected in parent entity at line @
vee	csa	inst	input_port_not_connected_in_parent_signal_csve	e					Input port @ not connected in parent signal at line @
vee	csa	mdb	single_comp_contains_multiple_tri_drv_cdve	w					A single component contains multiple tristate drivers at line @
vee	csa	mdb	unsuppexpr_on_lhs_net_drv_stmt_csve	w					Unsupported Expression type type on LHS ofNet driver statement at line @
vee	csa	mdb	unsuppexpr_on_lhs_port_drv_stmt_csve	w					Unsupported Expression type type on LHS ofPort driver statement at line @
vee	csa	mdb	unsuppexpr_on_lhs_sig_drv_stmt_csve	w					Unsupported Expression type type on LHS ofSignaldriver statement at line @
vee	csa	mdb	tri_not_in_top_mod_csve	e					Tristate not in top module at line @
vee	csa	mdb	tri_not_in_top_ent_csve	e					Tristate not in top entity at line @
vee	csa	mdb	tri_not_in_top_sig_csve	e					Tristate not in top signal at line @
vee	csa	mdb	tri_primitive_inst_csve	e					Tristate primitive instantiation at line @
vee	csa	mdb	tri_net_only_one_drvr_csve	e					Tri Net has only one driver at line @
vee	csa	mdb	tri_port_only_one_drvr_csve	e					Tri Port has only one driver at line @
vee	csa	mdb	tri_sig_only_one_drvr_csve	e					Tri Signal has only one driver at line @
vee	csa	mem	single_bit_mem_csve	e					Single bit memory @ at line @
vee	csa	mod	redef_mod_csve	e					Redefined module @ at line @
vee	csa	mod	redef_ent_csve	e					Redefined entity @ at line @
vee	csa	mod	redef_signal_csve	e					Redefined signal @ at line @
vee	csa	net	tri_and_net_only_one_driver_csve	e	?				triandNet @ has only one driver at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	csa	net	tri_and_port_only_one_driver_csve	e	?				triandPort @ has only one driver at line @
vee	csa	net	tri_and_sig_only_one_driver_csve	e	?				triandSignal @ has only one driver at line @
vee	csa	net	var_assn_but_never_ref_csve	e					Variable @ assigned but never referenced at line @
vee	csa	net	var_never_assn_csve	e					Variable @ never assigned at line @
vee	csa	net	var_not_assn_in_all_paths_csve	e					Variable @ not being assigned in all paths at line @
vee	csa	net	var_not_in_snsl_csve	e					Variable @ not in sensitivity list at line @
vee	csa	net	reg_connected_to_inout_in_inst_csve	e					Reg @ connected to inout @ in instantiation @ at line @
vee	csa	net	reg_connectede_to_output_in_inst_csve	e					Reg @ connected to output in instantiation at line @
vee	csa	net	reg_used_as_output_of_cont_assn_csve	e					Reg @ used as output of continuous assign at line @
vee	csa	net	port_used_prior_to_decl_csve	e					Port @ used prior toDeclaration at line @
vee	csa	net	dupl_sig_in_snsl_csve	e					Duplicate signal @ in sensitivity list at line @
vee	csa	netd	var_never_assigned_csve	e					Variable @ never assigned at line @
vee	csa	num	assignment_contains_real_num_const_csve	e					Assignment contains a real number constant at line @
vee	csa	parm	unused_parm_csve	e					Unused parameter @ at line @
vee	csa	parm	redef_param_csve	e					Redefined parameter @ at line @
vee	csa	pp	redef_macro_csve	e					Redefined macro @ at line @
vee	csa	prts	prts_on_vec_net_not_allowed_csve	w					Part select @ on a vectored Net may not be allowed according to IEEE 1364-1995 at line @
vee	csa	prts	prts_on_vec_port_not_allowed_csve	w					Part select @ on a vectored Port may not be allowed according to IEEE 1364-1995 at line @
vee	csa	prts	prts_on_vec_sig_not_allowed_csve	w					Part select @ on a vectored Signal may not be allowed according to IEEE 1364-1995 at line @
vee	csa	prts	out_of_range_bit_ref_csve	e					Out of range bus bit referenced at line @
vee	csa	prts	vec_index_order_incorrect_csve	e					Vector index @ order incorrect at line @
vee	csa	prts	vec_index_truncated_csve	e					Vector index @ truncated at line @
vee	csa	sdir	sdir_compiler_csve	e					Found synopsys compiler directive at line @
vee	csa	seq	blk_not_in_lib_csve	e					Block @ not in library at line @
vee	csa	sig	sig_will_float_when_rel_csve	e					Signal @ will float when it is released at line @
vee	csa	snsl	var_modified_in_snsl_csve	e					Variable @ modified in sense list at line @
vee	csa	snsl	var_in_snsl_unsused_in_blk_csve	e					Variable @ in sensitivity list not used in block at line @
vee	csa	snsl	rhs_var_noi_in_snsl_csve	e					RHS variable not in sensitivity list at line @
vee	csa	spec	spec_blk_found_csev	e					Specify block found at line @
vee	csa	sply	sply_being_driven_csve	e					Supply being driven at line @
vee	csa	sply	sply_not_def_user_keyword_csve	e					Supply not defined with user defined keyword at line @
vee	csa	sply	sply_not_in_lib_csve	e					Supply not in library at line @
vee	csa	sply	output_conncet_to_sply_	e					Output @ connect to supply at line @
vee	csa	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_csve	e					Arithmetic operator RHS has one less bit than the LHS at line @
vee	csa	stmt	ar_op_unequal_lhs_rhs_csve	e					Arithmetic operator unequal width LHS and RHS at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	csa	stmt	ar_op_unequal_var_on_rhs_csve	e					Arithmetic operator unequal width variables @ on RHS at line @
vee	csa	task	task_call_iteslf_rec_csve	e					Task @ calling itself recursively at line @
vee	csa	time	time_var_bit_used_csde	e					Time variable bit used at line @
vee	csa	tri	tri_not_in_top_mod_csve	e					Tristate @ not in top module at line @
vee	csa	tri	tri_not_in_top_entity_csve	e					Tristate @ not in top entity at line @
vee	csa	tri	tri_not_in_top_signal_csve	e					Tristate @ not in top signal at line @
vee	csa	tri	tri_prim_ist_csve	e					Tristate primitive instantiation @ at line @
vee	csa	udp	upd_not_supported_csve	e					UDPs are not supported at line @
vee	csb	assn	x_in_rhs_of_assihnment_csbve	e					x in rhs of assignment at line @
vee	csb	assn	z_in_rhs_of_assn_default_csi_csbve	e					x in rhs of assignement in defaultCase item at line @
vee	csb	assn	z_in_rhs_of_assn_csbve	e					z in rhs of assignement at line @
vee	csb	assn	unequal_length_lhs_rhs_csbve	e					Unequal length LHS and RHS at line @
vee	csb	assn	unequal_length_lhs_rhs_off_one_bit_csbve	e					Unequal length LHS and RHS off by one bit at line @
vee	csb	blk	blk_ill_block_id_csv	e					Illegal block @ at line @
vee	csb	blk	nonblocking_assign_in_comb_always_blk_csbve	e					Non blockinq aasignment in combinational always block at line @
vee	csb	blk	seq_blk_contains_blk_assn_csbve	e					Sequential block contains blocking assignement at line @
vee	csb	casn	LHS_not_reg_casn_veve	e					LHS cannot be a register @ at line @
vee	csb	ccd	ccd_cdir_must_be_cst_expr_csbve	e				x	CSL directive size must be constant Expression at line @
vee	csb	clk	clk_name_not_found_cdir_csbve	e				x	Clock name not found in cslc directive at line @
vee	csb	clk	expr_sunj_to_different_clk_phases_csbve	e					Expression subject to different clock phases at line @
vee	csb	cmdl	cannot_use_librescan_with_liborder_specified_csbve	e					Cannot use +librescan when +liborder has already been specified at line @
vee	csb	cmdl	cannot_use_liborder_with_librescan_specified_csbve	e					Cannot use +liborder when +librescan has already been specified at line @
vee	csb	cond	if_case_question_cond_csbve	e					If/case conditional expression expr syntax error at line @
vee	csb	cond	if_no_else_in_comb_blk_csbve	e					If no else in combinational block at line @
vee	csb	cond	if_no_else_in_comb_blk_csbvh	e					If no else in combinational block at line @
vee	csb	csi	xcsi_not_in_casex_csbve	e					xCase item not in casex at line @
vee	csb	csi	noncnst_csi_csbve	e					Non-constantCase item @ at line @
vee	csb	csi	noncnst_dely_csbve	e					Non-constant delay @ at line @
vee	csb	csi	noncstn_rep_in_conc_csbve	e					Non-constant repeator in concatenation at line @
vee	csb	css	sns_pragma_full_case_csbve	e					Assume a full case, missing default or synopsys pragma full case. at line @
vee	csb	cyb	repeat_in_delay_cyb_csv	e					Repeat clause in delay not supported at line @
vee	csb	cyb	repeat_in_event_control_cyb_csv	e					Repeat clause in event control not supported at line @
vee	csb	cyb	event_id_not_supported_cyb_csv	e					@ event id is not supported at line @
vee	csb	cyb	ill_proc_assign_cyb_csv	e					Illegal procedural continuous assignment statement at line @
vee	csb	cyb	ill_deassign_cyb_csv	e					Illegal de-assign statement at line @
vee	csb	cyb	ill_force_cyb_csv	e					Illegal force statement at line @
vee	csb	cyb	ill_release_cyb_csv	e					Illegal release statement

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									at line @
vee	csb	cyb	repeat_as_delay_cyb_csv	e					Repeat as delay not supported at line @
vee	csb	cyb	repeat_as_event_control_cyb_csv	e					Repeat as event control not supported at line @
vee	csb	cyb	wait_statement_not_cyb_csv	e					Wait statement is not supported at line @
vee	csb	cyb	disable_statement_not_cyb_csv	e					Disable statement is not supported at line @
vee	csb	cyb	events_not_supported_cyb_csv	e					Events are not supported at line @
vee	csb	cyb	fork_join_blocks_not_supported_cyb_csv	e					Fork/join blocks are not supported at line @
vee	csb	cyb	unsupp_function_return_time_cyb_csv	e					Unsupported function return time at line @
vee	csb	cyb	not_supp_events_cyb_csv	e					Events are not supported at line @
vee	csb	cyb	repeat_in_delay_or_event_cyb_csv	e					Repeat clause in delay or Event control at line @
vee	csb	cyb	ill_proc_cont_assign_stmt_cyb_csv	e					Illegal procedural continuous assignment statement at line @
vee	csb	cyb	ill_deassign_cyb_stmt_csv	e					Illegal de-assign statement at line @
vee	csb	cyb	ill_force_stmt_cyb_csv	e					Illegal force statement at line @
vee	csb	cyb	ill_release_stmt_cyb_csv	e					Illegal release statement at line @
vee	csb	cyb	repeat_not_supp_as_delay_or_event_cyb_csv	e					Repeat as delay or event control not supported at line @
vee	csb	cyb	not_supp_wait_stmt_cyb_csv	e					Wait statement is not supported at line @
vee	csb	cyb	not_supp_disable_stmt_cyb_csv	e					Disable statement is not supported at line @
vee	csb	cyb	supp_not_events_cyb_csv	e					Events are not supported at line @
vee	csb	cyb	not_supp_fork_join_blocks_cyb_csv	e					Fork/join blocks are not supported at line @
vee	csb	cyb	not_supp_UDP_cyb_csv	e					UDPs are not supported at line @
vee	csb	cyb	not_supp_defparam_cyb_csv	e					Defparam is not supported at line @
vee	csb	cyb	specify_blk_not_supported_csbve	e					Specify blocks are not supported at line @
vee	csb	cyb	mintypmax_expr_not_supp_csbve	w					mintypmax Expressions are not supported at line @
vee	csb	decl	decl_array_over_max_size_csbve	e					Array @ exceeds maximum size limit at line @
vee	csb	dely	max_val_dly_csv	e					Too many delay values, max @ at line @
vee	csb	dely	found_gate_dely_not_allowed_csbve	e					Found gate delay which are not allowed at line @
vee	csb	dely	found_dely_in_casn_not_allowed_csbve	e					Found delay in continuous assignment which are not allowed at line @
vee	csb	dely	dely_ignoring_dely_specification_csbve	e					Delay Ignoring delay specification in Net Declaration at line @
vee	csb	dely	dely_ignoring_dely_specification_port_csbve	e					Delay Ignoring delay specification in Port Declaration at line @
vee	csb	dely	dely_ignoring_dely_specification_sig_csbve	e					Delay Ignoring delay specification in Signal Declaration at line @
vee	csb	dely	dely_ignoring_dely_before_stmt_csbve	e					Delay Ignoring delay before statement at line @
vee	csb	dely	x_or_z_in_dely_csbve	e					x or z in delay at line @
vee	csb	dely	non_int_dely_csbve	e					Non integer delay at line @
vee	csb	dmsn	mem_prts_index_out_of_range_for_mem_csbve	e					Memory part select [@:@] index @ out range for memory @ at line @
vee	csb	dmsn	dime_select_for_mem_missing_csbve	e					Select for memory @ missing at line @
vee	csb	dmsn	dime_index_out_of_bounds_for_mem_csbve	e					Index <index> out of bounds for memory @. Range [@: @] at line @
vee	csb	dmsn	dime_prts_out_of_bounds_for_net_csbve	e					Part select [@ : @] out of bounds for net @. Range [@ : @] at line @
vee	csb	dmsn	dime_prts_out_of_bounds_for_port_csbve	e					Part select [@ : @] out of bounds for port @. Range [@ : @] at line @
vee	csb	dmsn	dime_prts_out_of_bounds_for_sig_csbve	e					Part select [@ : @] out of

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									bounds for signal @. Range [@ : @] at line @
vee	csb	dmsn	dime_prts_reg_csbve	e					Part select [@ : @] reg @. Range [@ : @] at line @
vee	csb	drvc	incompatible_drvc_for_net_csbve	e					Incompatible drivers for Net @ at line @
vee	csb	drvc	incompatible_drvc_for_port_csbve	e					Incompatible drivers for Port @ at line @
vee	csb	drvc	incompatible_drvc_for_sig_csbve	e					Incompatible drivers for Signal @ at line @
vee	csb	drvc	drvc_multiple_drive_net_partially_overlap_csbve	e					Multiple drive Net partially overlap at line @
vee	csb	drvc	drvc_multiple_drive_port_partially_overlap_csbve	e					Multiple drive Port partially overlap at line @
vee	csb	drvc	drvc_multiple_drive_sig_partially_overlap_csbve	e					Multiple drive Signal partially overlap at line @
vee	csb	dsgn	dsgn_top_mod_cannot_id_csbve	e					Top module @ cannot be identified at line @
vee	csb	dsgn	dsgn_top_entity_cannot_id_csbve	e					Top entity @ cannot be identified at line @
vee	csb	dsgn	dsgn_top_unit_cannot_id_csbve	e					Top unit @ cannot be identified at line @
vee	csb	dsgn	unit_dsgn_cycle_not_spanning_tree_csbve	e					Unit design hierarchy contains a cycle. Hierarchy is not a spanning tree. at line @
vee	csb	evc	not_allowed_edge_trigger_csbve	e					Edge trigger is not allowed in this location at line @
vee	csb	evc	ectl_in_assn_csbve	e					Event control in assignement at line @
vee	csb	expr	expr_prts_indices_1bit_var_csbve	e					Part select indices 1-bit variable at line @
vee	csb	expr	expr_prts_must_be_cst_expr_csbve	e					Part select specifier Expression must be constant Expression at line @
vee	csb	expr	not_const_expr_csbve	e					Repetition multiplier in concatenation is not a constant Expression at line @
vee	csb	expr	ill_bit_select_expr_csbve	e					Illegal bit select expression @ at line @
vee	csb	expr	equality_operator_detected_csbve	e					Use of operator === detected at line @
vee	csb	expr	notequal_operator_detected_csbve	e					Use of operator !== detected at line @
vee	csb	expr	ill_parm_value_csbve	e					Illegal parameter value at line @
vee	csb	expr	repetition_multiplier_in_conc_not_const_expr_csbve	w					Repetition multiplier in concatenation is not a constant Expression at line @
vee	csb	expr	int_operand_not_1_bit_csbve	w					Logic operator has integer operands instead of 1-bit operands at line @
vee	csb	expr	unsupp_expr_csbve	w					Unsupported Expression type @ at line @
vee	csb	expr	unsupp_operator_csbve	w					Unsupported operator type @ at line @
vee	csb	expr	use_of_sg_bit_const_csbve	w					Use of single bit constant at line @
vee	csb	expr	unary_op_in_comparison_csbve	e					Unary op used in comparison at line @
vee	csb	expr	nonconst_repeator_in_conc_csbve	e					Non constant repeator in concatention at line @
vee	csb	expr	x_or_z_in_cond_expr_csbve	e					x or z in conditional expression at line @
vee	csb	expr	zero_in_rep_in_conc_csbve	e					Zero repeator in concatenation at line @
vee	csb	expr	expr_in_mod_port_dir_csbve	e					Expression @ in module port dir at line @
vee	csb	expr	expr_in_ent_port_dir_csbve	e					Expression @ in entity port dir at line @
vee	csb	expr	expr_in_sig_port_dir_csbve	e					Expression @ in unit port dir at line @
vee	csb	expr	expr_in_inst_csbve	e					Expression @ in inst i@ at line @
vee	csb	expr	expr_operator_operands_unequal_lenght_csbve	e					Expression operator @ operands @ unequal length at line @
vee	csb	file	cannot_open_filter_specification_file_csbve	e					Cannot open filter specification file @ at line @
vee	csb	file	filter_specification_file_missing_csbve	e					Filter specification file name @ is missing at line @
vee	csb	file	mismatch_mod_file_name_csbve	e					Mismatch between

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									module name @ and file name @ at line @
vee	csb	file	mismatch_ent_file_name_csbve	e					Mismatch between entity name @ and file name @ at line @
vee	csb	file	mismatch_sig_file_name_csbve	e					Mismatch between signal name @ and file name @ at line @
vee	csb	forc	ill_forc_obj_type_csbve	e					Illegal force object type @ at line @
vee	csb	func	ill_func_return_type_csv	e					Illegal function return type at line @
vee	csb	func	ill_func_csv	e					Illegal function @ at line @
vee	csb	func	port_not_output_func_csbve	e					Port @ direction cannot be output at line @
vee	csb	func	ill_use_func_csbve	e					Illegal use of function @ at line @
vee	csb	func	func_not_define_csbve	e					Function @ not defined at line @
vee	csb	func	too_many_arg_to_func_csbve	e					Too many arguments passed to function @ at line @
vee	csb	func	too_few_arg_to_func_csbve	e					Too few arguments passed to function @ at line @
vee	csb	func	undefined_func_csbve	e					Undefined function @ at line @
vee	csb	func	funct_expr_cannot_expnaded_csbve	e					Function expression @ cannot be expanded at line @
vee	csb	func	funct_not_used_in_expr_csbve	w					Function @ is not being used in an Expression at line @
vee	csb	func	func_decl_csbve	w					Function Declaration @ already declared as another type at line @
vee	csb	func	func_param_csb	e					Found function parameter @ at line @
vee	csb	func	unmatched_funct_param_csbve	e					Unmatched function parameter @ at line @
vee	csb	gate	ill_output_pin_name_gate_csv	e					Illegal output terminal Expression pin @ at line @
vee	csb	hid	cannot_locate_hier_id_hid_csbve	e					Can't locate hierarchical identifier @ at line @
vee	csb	hid	ref_minst_found_in_expr_hid_csbve	e					References a module instance @ found in an Expression hid at line @
vee	csb	hid	ref_entity_found_in_expr_hid_csbve	e					References a entity instance @ found in an Expression hid at line @
vee	csb	hid	ref_unit_found_in_expr_hid_csbve	e					References a unit instance @ found in an Expression hid at line @
vee	csb	hid	ref_in_eexpr_hid_csbve	e					References a module instance @ passed as argument to PLI task call is also found in an Expression @ at line @
vee	csb	hid	ref_in_expr_hid_csbve	e					References a entity instance @ passed as argument to PLI task call is also found in an Expression @ at line @
vee	csb	hid	reff_in_expr_hid_csbve	e					References a unit instance @ passed as argument to PLI task call is also found in an Expression @ at line @
vee	csb	hid	hid_name_traverses_into_func	e					Hid @ name traverses into a function @ at line @
vee	csb	hid	hid_ref_mod_out_arg_sytk_csbve	e					Hid @ referencing a module instance passed as 'out' type argument to a system task @ at line @
vee	csb	hid	hid_ref_entity_out_arg_sytk_csbve	e					Hid @ referencing a entity instance passed as 'out' type argument to a system task @ at line @
vee	csb	hid	hid_ref_unit_out_arg_sytk_csbve	e					Hid @ referencing a unit instance passed as 'out' type argument to a system task @ at line @
vee	csb	hid	hid_reference_not_found_csbve	e					@ reference not found at line @
vee	csb	hid	mifc_in_hid_not_exist_csbve	e					Module instance @ in hid does not exist at line @
vee	csb	hid	entity_instance_in_hid_not_exist_csbve	e					Entity instance @ in hid

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									does not exist at line @
vee	csb	hid	unit_instance_in_hid_not_exist_csbve	e					Unit instance @ in hid does not exist at line @
vee	csb	hid	mod_found_in_path_in_dsgn_csbve	e					Module @ found in path @ in the design at line @
vee	csb	hid	enity_found_in_path_in_dsgn_csbve	e					Entity @ found in path @ in the design at line @
vee	csb	hid	unit_found_in_path_in_dsgn_csbve	e					Unit @ found in path @ in the design at line @
vee	csb	hid	hierarchical_id_path_contains_func_csb	e					Hierarchical ID @ path contains a function at line @
vee	csb	id	ill_terminal_id_csv	e					Illegal terminal identifier at line @
vee	csb	init	assn_mem_in_init_blk_csbve	e					Assign memory in initial block at line @
vee	csb	inst	inst_duplicate_mod_name_csbve	e					Duplicate port @ in the port list for module @ at line @
vee	csb	inst	inst_duplicate_entity_name_csbve	e					Duplicate port @ in the port list for entity @ at line @
vee	csb	inst	inst_duplicate_unit_name_csbve	e					Duplicate port @ in the port list for unit @ at line @
vee	csb	inst	miss_declparam_inst_csv	e					Parameter Declaration missing value at line @
vee	csb	inst	ill_mod_inst_name_csbve	e					Illegal module instance @ at line @
vee	csb	inst	ill_entity_inst_name_csbve	e					Illegal entity instance @ at line @
vee	csb	inst	ill_unit_inst_name_csbve	e					Illegal unit instance @ at line @
vee	csb	inst	inst_name_defined_mod_csv	e					Instance name @ already defined in this module at line @
vee	csb	inst	inst_name_defined_ent_csv	e					Instance name @ already defined in this entity at line @
vee	csb	inst	inst_name_defined_unit_csv	e					Instance name @ already defined in this unit at line @
vee	csb	inst	inst_too_many_bits_csbve	e					Too many bits for port @ of instance array @, formal @, actual @ at line @
vee	csb	inst	inst_port_not_connected_var_csbve	e					Port 'port' of instance array 'array' is not connected to variable at line @
vee	csb	inst	inst_insufficient_bits_csbve	e					Insufficient bits for port 'port' of instance array 'array ', formal number, actual number at line @
vee	csb	inst	inst_mod_name_not_defined_cssbve	e					Module name not defined at line @
vee	csb	inst	inst_ent_name_not_defined_csbve	e					Entity name not defined at line @
vee	csb	inst	inst_unit_name_not_defined_csbve	e					Unit name not defined at line @
vee	csb	inst	many_mod_inst_param_assign_csbve	e					Too many module instance parameter assignments (number > rrumber) at line @
vee	csb	inst	many_entity_inst_param_assign_csbve	e					Too many entity instance parameter assignments (number > rrumber) at line @
vee	csb	inst	many_unit_inst_param_assign_csbve	e					Too many unit instance parameter assignments (number > rrumber) at line @
vee	csb	inst	complexexpr_cannot_mapped_inout_port_csbve	e					Complex Expression @ cannot be mapped to inout port @ at line @
vee	csb	inst	complexexpr_cannot_mapped_unknown_port_csbve	e					Complex Expression @ cannot be mapped to unknown type port @ at line @
vee	csb	inst	netdecl_contains_ill_prts_csbve	e					Net Declaration [@: @] contains an illegal part select at line @
vee	csb	inst	regdecl_contains_ill_prts_csbve	e					Reg Declaration [@ : @] contains an illegal part select at line @
vee	csb	inst	complex_expr_inst_parent_module_csbve	e					Complex actual Expression associated with port @ of module @ instantiated in parent module at line @
vee	csb	inst	complex_expr_inst_entity_parent_module_csbve	e					Complex actual

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									Expression associated with port @ of entity @ instantiated in parent module at line @
vee	csb	inst	complex_expr_inst_unit_parent_module_csbve	e					Complex actual Expression associated with port @ of unit @ instantiated in parent module at line @
vee	csb	inst	inst_mod_output_port_width_csbve	e					Mod @ Output port @ width mismatch, actual-width (port-width) at line @
vee	csb	inst	inst_entity_output_port_width_csbve	e					Entity @ Output port @ width mismatch, actual-width (port-width) at line @
vee	csb	inst	inst_unit_output_port_width_csbve	e					Unit @ Output port @ width mismatch, actual-width (port-width) at line @
vee	csb	inst	inst_mod_input_port_width_csbve	e					Mod @ Input port @ width mismatch, actual-width (port-width) at line @
vee	csb	inst	inst_entity_input_port_width_csbve	e					Entity @ Input port @ width mismatch, actual-width (port-width) at line @
vee	csb	inst	inst_unit_input_port_width_csbve	e					Unit @ Input port @ width mismatch, actual-width (port-width) at line @
vee	csb	inst	inst_mod_not_define_csbve	e					Module not defined at line @
vee	csb	inst	inst_entity_not_define_csbve	e					Entity not defined at line @
vee	csb	inst	inst_unit_not_define_csbve	e					Unit not defined at line @
vee	csb	inst	miss_mifc_name_csbve	w			x		Missing module instance name. This syntax is an error according to IEEE 1364-1995 but is allowed by commercial Verilog compilers at line @
vee	csb	inst	miss_ent_instance_name_csbve	w			x		Missing entity instance name. This syntax is an error according to IEEE 1364-1995 but is allowed by commercial Verilog compilers at line @
vee	csb	inst	miss_unit_instance_name_csbve	w			x		Missing unit instance name. This syntax is an error according to IEEE 1364-1995 but is allowed by commercial Verilog compilers at line @
vee	csb	inst	mifc_port_actual_formal_width_mismatch_csbve	w					Module @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vee	csb	inst	ent_port_actual_formal_width_mismatch_csbve	w					Entity @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vee	csb	inst	unit_port_actual_formal_width_mismatch_csbve	w					Unit @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vee	csb	inst	unmatched_port_connect_in_inst_csbve	e					Unmatched port @ connect in instance @ at line @
vee	csb	inst	inst_differs_in_case_from_mod_csbve	e					Instance name @ differs in case from module name @ at line @
vee	csb	inst	inst_differs_in_case_from_ent_csbve	e					Instance name @ differs in case from entity name @ at line @
vee	csb	inst	inst_differs_in_case_from_sig_csbve	e					Instance name @ differs in case from signal name @ at line @
vee	csb	lib	lib_name_not_mod_declaration_csv	e					Library file @ doesn't contain a module Declaration at line @
vee	csb	lib	lib_name_not_entity_declaration_csv	e					Library file @ doesn't contain a entity Declaration at line @
vee	csb	lib	lib_name_not_unit_declaration_csv	e					Library file @ doesn't contain a unit Declaration at line @
vee	csb	lib	lib_not_contain_supply_csbve	e					Library does not contain supply @ at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	csb	loop	initial_value_unknown_loop_csbve	e					While control initial variable @ unassigned. Initial value unknown at line @
vee	csb	loop	while_loop_not_assign_stmt_controlvar_csbve	e					While loop body does not contain an assignment statement for control variable @ at line @
vee	csb	loop	assign_stmt_not_last_while_loop_csbve	e					Assignment statement for control variable @ not last statement in while loop at line @
vee	csb	loop	undet_init_value_loop_csbve	e					Unable to determine init value for loop at line @
vee	csb	loop	undet_limit_loop_csbve	e					Unable to determine limit for loop at line @
vee	csb	loop	loop_bounds_calculated_int_csbve	w					Loop bounds are calculated to be integer @, check that this is correct at line @
vee	csb	loop	expr_lhs_contains_var_bit_select_csbve	w					Expression in lhs of assignment contains a variable bit select at line @
vee	csb	loop	loop_bounds_not_const_csb	w					Loop bounds are non-constant at line @
vee	csb	loop	loop_ctrl_init_expr_not_const_csbve	w					Non-constant loop bound. Loop control variable initialization Expression is not a constant Expression at line @
vee	csb	loop	loop_term_expr_not_const_csbve	w					Non-constant loop bound. loop terminating Expression could not be evaluated to a constant at line @
vee	csb	loop	init_expr_reset_by_var_csbve	e					Non-constant loop bound. initializing Expression reset by variable at line @
vee	csb	loop	loop_ctrl_var_1_bit_wide_csbve	w					The loop control variable @ is one bit wide. Check the loop control variable Declaration. at line @
vee	csb	mdb	bad_mdb_net_csbve	e					Bad multi-driven Net @ at line @
vee	csb	mdb	bad_mdb_port_csbve	e					Bad multi-driven Port @ at line @
vee	csb	mdb	bad_mdb_signal_csbve	e					Bad multi-driven Signal @ at line @
vee	csb	mdb	unsupp_comp_mdb_net_csbve	e	?				Unsupported component type @ driving in multi-driven Net name at line @
vee	csb	mdb	unsupp_comp_mdb_port_csbve	e	?				Unsupported component type @ driving in multi-driven Port name at line @
vee	csb	mdb	unsupp_comp_mdb_signal_csbve	e	?				Unsupported component type @ driving in multi-driven Signal name at line @
vee	csb	mdb	unsupp_comp_drive_mdb_csbve	e	?				Unsupported component type @ driving multi-driven Net natne at line @
vee	csb	mdb	unsupp_comp_drive_mdb_port_csbve	e	?				Unsupported component type @ driving multi-driven Port natne at line @
vee	csb	mdb	unsupp_comp_drive_mdb_signal_csbve	e	?				Unsupported component type @ driving multi-driven Signal natne at line @
vee	csb	mdb	mdb_net_driven_by_trns_csbve	e					Multiply driven Net driven by transistor primitive type @ at line @
vee	csb	mdb	mdb_port_driven_by_trns_csbve	e					Multiply driven Port driven by transistor primitive type @ at line @
vee	csb	mdb	mdb_sig_driven_by_trns_csbve	e					Multiply driven Signal driven by transistor primitive type @ at line @
vee	csb	mdb	mdb_unsupp_comp_drvs_net_csbve	e					Unsupported component type driving Net drives Net connected to multi-driven Net at line @
vee	csb	mdb	mdb_unsupp_comp_drvs_port_csbve	e					Unsupported component

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									type driving Port drives Port connected to multi-driven Port at line @
vee	csb	mdb	mdb_unsupp_comp_drvs_sig_csbve	e					Unsupported component type driving Signal drives Signal connected to multi-driven Signal at line @
vee	csb	mdb	mdb_incompatible_net_drives_multiple_net_csbve	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Net at line @
vee	csb	mdb	mdb_incompatible_port_drives_multiple_port_csbve	e					Incompatible driver driving tandem Port drives Port connected to multi-driven Port at line @
vee	csb	mdb	mdb_incompatible_sig_drives_multiple_sig_csbve	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Port at line @
vee	csb	mdb	mdb_unsupp_LHS_concatenation_csbve	e					Unsupported LHS concatenation in multi-drive 'device at line @
vee	csb	mdb	mdb_bus_has_too_many_drivers_csbve	e					Bus has too many drivers. at line @
vee	csb	mdb	mdb_always_blk_drive_csbve	w					Multiple always blocks drive name @ at line @
vee	csb	mdb	nontri_gate_drives_mdb_net_csbve	w					non-tri-state gate drives multi-driven Net at line @
vee	csb	mdb	nontri_gate_drives_mdb_port_csbve	w					non-tri-state gate drives multi-driven Port at line @
vee	csb	mdb	nontri_gate_drives_mdb_sig_csbve	w					non-tri-state gate drives multi-driven Signal at line @
vee	csb	mem	mem_prts_csve	e					Memories do not support part select specifier at line @
vee	csb	mem	ill_ref_mem_name_csv	e					Illegal hid reference to memory (name) at line @
vee	csb	mem	mem_ref_without_index_csbve	e					Memory @ referenced without index through hierarchical ID @ at line @
vee	csb	mifc	mifc_not_array_csve	e					Ports may not be an array at line @
vee	csb	mifc	port_identifier_mifc_csbve	e					Port @ at line @
vee	csb	mifc	mifc_mod_input_port_decl_as_reg_csbve	e					Module @ input port @ declared as type reg at line @
vee	csb	mifc	mifc_enity_input_port_decl_as_reg_csbve	e					Entity @ input port @ declared as type reg at line @
vee	csb	mifc	mifc_unit_input_port_decl_as_reg_csbve	e					Unit @ input port @ declared as type reg at line @
vee	csb	mifc	mod_output_wire_redecl_reg_csbve	e					Module @ output port re-declared as type reg after use as implicitly declared wire at line @
vee	csb	mifc	entity_output_wire_redecl_reg_csbve	e					Entity @ output port re-declared as type reg after use as implicitly declared wire at line @
vee	csb	mifc	unit_output_wire_redecl_reg_csbve	e					Unit @ output port re-declared as type reg after use as implicitly declared wire at line @
vee	csb	mifc	output_port_is_mem_type_mifc_csbve	e					Output port @ is memory type at line @
vee	csb	mifc	mifc_inout_port_is_mem_type_csbve	e					Inout port @ is memory type at line @
vee	csb	mifc	mod_output_port_mismatch_actual_witdh_csbve	w					Module @ output port @ formal to actual width mismatch at line @
vee	csb	mifc	ent_output_port_mismatch_actual_witdh_csbve	w					Entity @ output port @ formal to actual width mismatch at line @
vee	csb	mifc	unit_output_port_mismatch_actual_witdh_csb	w					Unit @ output port @ formal to actual width mismatch at line @
vee	csb	mifc	port_name_different_in_upper_lower_case_csbve	e					Port name @ different in upper lower case at line @
vee	csb	mifc	port_not_def_in_iodecl_csbve	e					Port @ not defined in ioDeclaration at line @
vee	csb	mifc	port_not_def_in_portl_csbve	e					Port @ not defined in

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									port list at line @
vee	csb	mifc	port_wiredecl_mismatch_csbve	e					Port @ wireDeclaration mismatch at line @
vee	csb	mifc	pos_based_null_inst_port_csbve	e					Position based null instance port at line @
vee	csb	mifc	last_portdecl_contains_trailcomma_csbve	e					Last portDeclaration contains a trailing comma at line @
vee	csb	mins	mins_expr_incompatible_type_csbve	e					Expression @ has an incompatible argument type @ with the port at line @
vee	csb	mins	mins_mod_not_exist_csbve	e					Module @ does not exist at line @
vee	csb	mins	mins_entity_not_exist_csbve	e					Entity @ does not exist at line @
vee	csb	mins	mins_unit_not_exist_csbve	e					Unit @ does not exist at line @
vee	csb	mins	undefined_instance_csbve	e					Undefined instance @ at line @
vee	csb	mod	mod_param_bad_number_csv	e					Module name @ parameter list contains an Incorrect number of parameter overrides at line @
vee	csb	mod	mod_entity_param_bad_number_csv	e					Entity name @ parameter list contains an Incorrect number of parameter overrides at line @
vee	csb	mod	mod_unit_param_bad_number_csv	e					Unit name @ parameter list contains an Incorrect number of parameter overrides at line @
vee	csb	mod	ill_mod_name_csbve	e					Illegal module @ at line @
vee	csb	mod	ill_mod_entity_name_csbve	e					Illegal entity @ at line @
vee	csb	mod	ill_mod_unit_name_csbve	e					Illegal unit @ at line @
vee	csb	mod	mod_mult_decl_string_csbve	e					Multiple Declarations of string detected in module @ at line @
vee	csb	mod	mod_entity_mult_decl_string_csbve	e					Multiple Declarations of string detected in entity @ at line @
vee	csb	mod	mod_unit_mult_decl_string_csbve	e					Multiple Declarations of string detected in unit @ at line @
vee	csb	mod	mod_mult_def_csbve	e					Module @ defined in multiple places at line @
vee	csb	mod	mod_ent_mult_def_csbve	e					Entity @ defined in multiple places at line @
vee	csb	mod	mod_unit_mult_def_csbve	e					Unit @ defined in multiple places at line @
vee	csb	mod	mod_no_module_found_csbve	e					No modules found at line @
vee	csb	mod	mod_no_entity_found_csbve	e					No entity found at line @
vee	csb	mod	mod_no_unit_found_csbve	e					No unit found at line @
vee	csb	mod	failed_find_mod_csbve	e					Failed to find module @ at line @
vee	csb	mod	failed_find_entity_csbve	e					Failed to find entity @ at line @
vee	csb	mod	failed_find_unit_csbve	e					Failed to find unit @ at line @
vee	csb	mod	undefined_mod_csbve	e					Undefined module @ at line @
vee	csb	mod	undefined_ent_csbve	e					Undefined entity @ at line @
vee	csb	mod	undefined_unit_csbve	e					Undefined unit @ at line @
vee	csb	mod	unexpandable_macromodule_csbve	e					Unexpandable macromodule @ at line @
vee	csb	mod	non_interconnect_in_hierarchical_mod_csbve	e					Non interconnect in hierarchical module @ at line @
vee	csb	mod	non_interconnect_in_hierarchical_ent_csbve	e					Non interconnect in hierarchical entity @ at line @
vee	csb	mod	non_interconnect_in_hierarchical_sig_csbve	e					Non interconnect in hierarchical signal @ at line @
vee	csb	mod	empty_mod_csbve	e					Empty module at line @
vee	csb	mod	empty_ent_csbve	e					Empty entity at line @
vee	csb	mod	empty_unit_csbve	e					Empty unit at line @
vee	csb	net	namereg_not_on_LHS_stmt_net_csv	e					Register @ cannot be used on LHS of this assignment statement at line @
vee	csb	net	net_implicit_wire_redecl_reg_csbve	e					Implicitly declared as a wire @ re-declared as a

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									reg @. at line @
vee	csb	net	time_var_decl_csbve	e					Time variable @ declared at line @
vee	csb	net	time_var_bit_used_csbve	e					Time variable @ bit used at line @
vee	csb	net	undecl_net_in_mod_csbve	e					Undeclared net @ in module @ at line @
vee	csb	net	undecl_port_in_mod_csbve	e					Undeclared port @ in module @ at line @
vee	csb	net	undecl_sig_in_mod_csbve	e					Undeclared signal @ in module @ at line @
vee	csb	net	undecl_net_in_ent_csbve	e					Undeclared net @ in entity @ at line @
vee	csb	net	undecl_port_in_ent_csbve	e					Undeclared port @ in entity @ at line @
vee	csb	net	undecl_sig_in_ent_csbve	e					Undeclared signal @ in entity @ at line @
vee	csb	net	undecl_net_in_sig_csbve	e					Undeclared net @ in signal @ at line @
vee	csb	net	undecl_port_in_sig_csbve	e					Undeclared port @ in signal @ at line @
vee	csb	net	undecl_sig_in_sig_csbve	e					Undeclared signal @ in signal @ at line @
vee	csb	net	port_used_prior_to_decl_csbve	e					Port @ used prior toDeclaration at line @
vee	csb	net	1bit_with_prts_csbve	e					1-bit with part select at line @
vee	csb	netd	ill_decl_vec_csbve	e					Illegal Declaration of vector @ at line @
vee	csb	nett	nett_ill_reg_name_csbve	e					Illegal register @ at line @
vee	csb	nett	nett_ill_net_name_csbve	e					Illegal net @ at line @
vee	csb	nett	nett_ill_port_name_csbve	e					Illegal port @ at line @
vee	csb	nett	nett_ill_signal_name_csbve	e					Illegal signal @ at line @
vee	csb	nett	net_scalar_vect_nett_csbve	e					Net declared as both scalar and vector at line @
vee	csb	nett	port_scalar_vect_nett_csbve	e					Port declared as both scalar and vector at line @
vee	csb	nett	signal_scalar_vect_nett_csbve	e					Signal declared as both scalar and vector at line @
vee	csb	nett	hot_mux_not_use_bus_connection_net_csbve	e					One hot mux can not be used for bus connection between modules Net @ at line @
vee	csb	nett	hot_mux_not_use_bus_connection_port_csbve	e					One hot mux can not be used for bus connection between modules Port @ at line @
vee	csb	nett	hot_mux_not_use_bus_connection_sig_csbve	e					One hot mux can not be used for bus connection between modules Signal @ at line @
vee	csb	nett	reg_connected_inst_inout_csbve	e					Reg @ connnected to instantiation @ inout @ at line @
vee	csb	nett	ill_net_in_proc_assn_csbve	e					Illegal net type type in procedural assignement at line @
vee	csb	nett	ill_port_in_proc_assn_csbve	e					Illegal port type type in procedural assignement at line @
vee	csb	nett	ill_sig_in_proc_assn_csbve	e					Illegal signal type type in procedural assignement at line @
vee	csb	num	not_allowed_width0_num_csbve	e					Width 0 not allowed for sized number at line @
vee	csb	num	real_num_not_allowed_csbve	e					Real numbers not allowed at line @
vee	csb	num	found_x_z_in_num_literal_csbve	e					Found x and/or z value in number literal at line @
vee	csb	num	too_many_digits_in_sized_num_csbve	w					Number of digits exceeds the width in a sized number at line @
vee	csb	num	divide_by_zero_num_csbve	e					Divide by zero at line @
vee	csb	num	child_mod_inst_parent_mod_csbve	e					Child module @ instantiates parent module @ at line @
vee	csb	num	child_ent_inst_parent_ent_csbve	e					Child entity @ instantiates entity module @ at line @
vee	csb	num	child_sig_inst_parent_sig_csbve	e					Child signal @ instantiates signal module @ at line @
vee	csb	num	int_decl_incorrect_csbve	e					Integer Declaration incorrect at line @
vee	csb	num	int_var_indexed_csbve	e					Integer variable inedexed at line @

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vee	csb	parm	parm_redecl_as_reg_name_csv	e					Parameter re-declared as reg @ at line @
vee	csb	parm	parm_redecl_as_port_port_csv	e					Parameter re-declared as port @ at line @
vee	csb	parm	parm_redecl_as_net_name_csv	e					Parameter re-declared as Net @ at line @
vee	csb	parm	parm_redecl_as_port_name_csv	e					Parameter re-declared as Port @ at line @
vee	csb	parm	parm_redecl_as_signal_name_csv	e					Parameter re-declared as Signal @ at line @
vee	csb	parm	duplicate_decl_parm_name_csv	e					Duplicate declaration of parameter name @ at line @
vee	csb	parm	ill_parm_identifier_csbve	e					Illegal parameter @ at line @
vee	csb	parm	value_of_parm_OS_platform_dependent_csbve	w					Parameter select width > 32. The value is OS and platform dependent at line @
vee	csb	parm	parm_redefined_csbve	w					Parameter @ redefined at line @
vee	csb	pars	endfunction_miss_cyb_csv	e					Endfunction missing at line @
vee	csb	pars	endtask_miss_pars_csv	e					Endtask missing at line @
vee	csb	pars	endmodule_miss_pars_csv	e					Endmodule missing at line @
vee	csb	pars	miss_cont_assign_pars_csv	e					Missing = sign for continuous assignment at line @
vee	csb	pli	user_syst_not_listed_in_pli_table_csbve	e					User system task @ is not listed in PLI table at line @
vee	csb	port	ill_formal_port_name_csbve	e					Illegal formal port @ at line @
vee	csb	pp	text_redefined_replaced_csbve	w					Text macro redefined and replaced @. Previous definition filename, line number @ New definition filename, line number @ at line @
vee	csb	pp	undefined_macro_csbve	e					Undefined macro @ at line @
vee	csb	pp	include_file_contains_nonconst_csbve	e					Include file contains non constant @ at line @
vee	csb	pp	endif_or_else_without_ifdef_csbve	e					Endif-or-else-without ifdef at line @
vee	csb	prim	z_in_prim_inst_csbve	e					z in primitive instantiation at line @
vee	csb	prim	prim_instan_csbve	e					Primitive instantiation @ at line @
vee	csb	proc	proc_blk_missing_evc_csbve	e					Always block missing event control at line @
vee	csb	prts	prts_out_of_range_csbve	e					Parameter @[@ : @]part select is out of range at line @
vee	csb	prts	ill_prts_inst_array_csbve	e					Illegal value for part select of instance array 'name' at line @
vee	csb	prts	const_prts_contains_non_const_selector_csbve	e					Constant part select @ contains a non-constant selector @ at line @
vee	csb	prts	bus_index_prts_for_var_out_of_range_csbve	e					Bus index @ integer of part select [@:@] for variable @ out of range at line @
vee	csb	prts	bus_prts_for_var_out_of_range_csbve	e					Bus part select [@:@] for variable @ out of range at line @
vee	csb	prts	bus_prts_index_out_of_name_for_var_csbve	e					Bus part select [@:@] index @ out of range for variable @ at line @
vee	csb	prts	ill_token_in_prts_csbve	e					Illegal token in part select @ at line @
vee	csb	prts	incomplete_prts_specification_csbve	e					Incomplete part select specification @ at line @
vee	csb	prts	ill_index_in_prts_csbve	e					Illegal index in part select @ at line @
vee	csb	prts	negative_index_in_prts_not_allowed_csbve	e					Negative index in part select @ not allowed at line @
vee	csb	prts	prts_index_order_reversed_csbve	e					Part select index order reversed [@ : @] [@ : @] should be [@ : @] at line @
vee	csb	prts	index_vec_over_max_size_csbve	w					Vector index @ exceeds the size of the vector. Index truncated at line @
vee	csb	prts	x_or_z_in_vec_bit_select_index_csbve	e					x or z in vector bit select index at line @

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vee	csb	real	real_csbve	e					Real @ at line @
vee	csb	real	real_in_assn_csbve	e					Real @ in assignement at line @
vee	csb	real	real_in_csi_csbve	e					Real @ inCase item at line @
vee	csb	real	real_in_comparaison_csbve	e					Real @ in comparaison at line @
vee	csb	rel	ill_rel_obj_type_csbve	e					Illegal release object type type at line @
vee	csb	scop	var_erd_in_scope_csbve	e					Variable @ redfined in scope @ at line @
vee	csb	simr	inefficient_op_not_a_power_of_2_csbve	e					Division/modulus by a number not a power of 2. Inefficient simulation operation. at line @
vee	csb	simr	simr_multiple_init_blk_force_csbve	w					Multiple initial blocks force @. Unpredictable simulation result at line @
vee	csb	snsl	incomplete_snsl_csbve	w					Incomplete sensitivity list. @ is not in the sensitivity list. at line @
vee	csb	snsl	edge_sns_process_contains_data_pin_snsl_csbve	e					Edge sensitive process contains a data pin @ in the sensitivity list at line @
vee	csb	snsl	unsupp_expr_in_snsl_csbve	w					Unsupported Expression type @ in sensitivity list ' at line @
vee	csb	snsl	always_blk_is_miss_snsl_csbve	e					Always block is missing sensitivity list at line @
vee	csb	snsl	not_all_bits_snsvar_used_csb	e					Not all bus bits of sensitivity variable @ are used in process at line @
vee	csb	snsl	partial_bus_decl_width_csbve	e	?				partial bus @ declared with width @ width @ at line @
vee	csb	snsl	contains_inst_name_csbve	e					Contains instance name @ at line @
vee	csb	snsl	bus_indexed_in_snsl_csbve	e					Bus @ indexed in sensitivity list at line @
vee	csb	stmt	ill_register_assign_csv	e					Illegal register assignment statement at line @
vee	csb	stmt	null_not_allowed_stmt_csbve	e					Null statement is not allowed here at line @
vee	csb	stmt	id_expected_FHSexpr_force_stmt_csbve	e					Simple identifier expected for LHS Expression in force-statement at line @
vee	csb	stmt	id_expected_FHSexpr_release_stmt_csbve	e					Simple identifier expected for LHS Expression in release-statement at line @
vee	csb	stmt	stmt_ill_accept_only_net_reg_mem_csbve	e					Illegal type @ can only accept net, reg, memory at line @
vee	csb	stmt	stmt_ill_accept_only_port_reg_mem_csbve	e					Illegal type @ can only accept port, reg, memory at line @
vee	csb	stmt	stmt_ill_accept_only_signal_reg_mem_csbve	e					Illegal type @ can only accept signal, reg, memory at line @
vee	csb	stmt	while_stmt_usage_disc_csbve	w					While statement usage discouraged at line @
vee	csb	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_csbve	e					Arithmetic operator RHS has one less bit than the LHS at line @
vee	csb	stmt	ar_op_unequal_lhs_rhs_csbve	e					Arithmetic operator unequal width LHS and RHS at line @
vee	csb	stmt	ar_op_unequal_var_on_rhs_csb	e					Arithmetic operator unequal width variables @ on RHS at line @
vee	csb	stmt	empty_stmt_csb	e					Empty-statement at line @
vee	csb	syst	ill_syst_task_arg_csbve	e					Illegal system task @ Argument @ at line @
vee	csb	syst	csdir_converts_syts_csbve	w				x	Lower case converts the system task $realtime return value to an integer at line @
vee	csb	syst	return_var_of_user_used_as_rhs_csbve	w					Return variable of user system task is used as a RHS variable at line @
vee	csb	task	miss_task_name_stmst_body_csv	e					Task @ body statement missing at line @
vee	csb	task	ill_task_csv	e					Illegal task @ at line @
vee	csb	task	ill_use_task_csbve	e					Illegal use of task @ at line @

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vee	csb	task	ask_var_not_decl_csbve	e					Variable @ used but not declared at line @
vee	csb	task	task_not_defined_csbve	e					Task @ not defined at line @
vee	csb	task	too_few_arg_to_task_csbve	e					Too few arguments passed to task @ at line @
vee	csb	task	undefined_task_csbve	e					Undefined task @ at line @
vee	csb	task	syts_output_port_drvs_nonsqs_logic_comp_csbve	w					User system task output port drives non-sequential logic component at line @
vee	csb	task	undefioned_task_	e					Undefined task @ at line @
vee	csb	task	task_decl_error_veve	e					Task declaration error at line @
vee	csb	task	func_task_parm_csbve	e					Found function parameter @ at line @
vee	csb	task	unmatched_task_param_csbve	e					Unmatched task parameter @ at line @
vee	csb	tbcd	found_forever_tbcd_csbve	e					Found forever at line @
vee	csb	tbcd	behavioral_code_mod_csbve	e					Behavioral code in module @ at line @
vee	csb	tbcd	behavioral_code_ent_csbve	e					Behavioral code in entity @ at line @
vee	csb	tbcd	behavioral_code_unit_csbve	e					Behavioral code in unit @ at line @
vee	csb	tri	instance_not_tri_state_device_csbve	e					Instance name is not a tri-state device at line @
vee	csb	tri	unsupp_gate_type_tristate_csbve	e					Unsupported gate type @ used for tristate at line @
vee	csb	tri	tri_not_desgn_gate_contention_csbve	e					Tristate not designed correctly gate @ can cause contention at line @
vee	csb	tri	unsupp_type_instance_tri_csbve	e					Unsupported type instance type used for tristate @ at line @
vee	csb	tri	incorrect_cont_assign_stmt_tri_gate_csbve	e					Incorrect continuous assign statement for tristate gate @ at line @
vee	csb	tri	const_assign_to_multidriven_net_csbve	e					Constant (constiznt) assigned to multi-driven Net @ at line @
vee	csb	tri	const_assign_to_multidriven_port_csbve	e					Constant (constiznt) assigned to multi-driven Port @ at line @
vee	csb	tri	const_assign_to_multidriven_signal_csbve	e					Constant (constiznt) assigned to multi-driven Signal @ at line @
vee	csb	tri	unsupp_expr_for_tri_csbve	e					Unsupported Expression type @ for tristate at line @
vee	csb	unsy	cs_equality_op_csbve	e					Case equality operator == at line @
vee	csb	unsy	deassign_stmt_csbve	e					Deassign statement at line @
vee	csb	unsy	defparam_csbve	e					Defparam at line @
vee	csb	unsy	dely_ctrl_csbve	e					Delay control at line @
vee	csb	unsy	ev_ctrl_csbve	e					Event control at line @
vee	csb	unsy	time_decl_csbve	e					Time Declaration at line @
vee	csb	unsy	wait_stmt_unsy_csbve	e					Wait statement at line @
vee	csc	assn	x_in_rhs_of_assihnment_cscve	e					x in rhs of assignment at line @
vee	csc	assn	z_in_rhs_of_assn_default_csi_cscve	e					x in rhs of assignement in defaultCase item at line @
vee	csc	assn	z_in_rhs_of_assn_cscve	e					z in rhs of assignement at line @
vee	csc	assn	unequal_length_lhs_rhs_cscve	e					Unequal length LHS and RHS at line @
vee	csc	assn	unequal_length_lhs_rhs_off_one_bit_cscve	e					Unequal length LHS and RHS off by one bit at line @
vee	csc	blk	blk_ill_block_id_csve	e					Illegal block @ at line @
vee	csc	blk	nonblocking_assign_in_comb_always_blk_cscve	e					Non blockinq aasignment in combinational always block at line @
vee	csc	blk	seq_blk_contains_blk_assn_cscve	e					Sequential block contains blocking assignement at line @
vee	csc	casn	LHS_not_reg_casn_csve	e					LHS cannot be a register @ at line @
vee	csc	ccd	ccd_cdir_must_be_cst_expr_cscve	e				x	CSL directive size must be constant Expression at line @
vee	csc	clk	clk_name_not_found_cdir_cscve	e				x	Clock name not found in

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									cslc directive at line @
vee	csc	clk	expr_sunj_to_different_clk_phases_cscve	e					Expression subject to different clock phases at line @
vee	csc	cmdl	cannot_use_librescan_with_liborder_specified_cscve	e					Cannot use +librescan when +liborder has already been specified at line @
vee	csc	cmdl	cannot_use_liborder_with_librescan_specified_cscve	e					Cannot use +liborder when +librescan has already been specified at line @
vee	csc	cond	if_case_question_cond_cscve	e					If/case conditional expression expr syntax error at line @
vee	csc	cond	if_no_else_in_comb_blk_cscve	e					If no else in combinational block at line @
vee	csc	csi	xcsi_not_in_casex_cscve	e					xCase item not in casex at line @
vee	csc	csi	noncnst_csi_cscve	e					Non-constantCase item @ at line @
vee	csc	csi	noncnst_dely_cscve	e					Non-constant delay @ at line @
vee	csc	csi	noncstn_rep_in_conc_cscve	e					Non-constant repeator in concatenation at line @
vee	csc	css	sns_pragma_full_case_cscve	e					Assume a full case, missing default or synopsys pragma full case. at line @
vee	csc	cyb	repeat_in_delay_cyb_csve	e					Repeat clause in delay not supported at line @
vee	csc	cyb	repeat_in_event_control_cyb_csve	e					Repeat clause in event control not supported at line @
vee	csc	cyb	event_id_not_supported__cyb_csve	e					@ event id is not supported at line @
vee	csc	cyb	ill_proc_assign_cyb_csve	e					Illegal procedural continuous assignment statement at line @
vee	csc	cyb	ill_deassign_cyb_csve	e					Illegal de-assign statement at line @
vee	csc	cyb	ill_force_cyb_csve	e					Illegal force statement at line @
vee	csc	cyb	ill_release_cyb_csve	e					Illegal release statement at line @
vee	csc	cyb	repeat_as_delay_cyb_csve	e					Repeat as delay not supported at line @
vee	csc	cyb	repeat_as_event_control_cyb_csve	e					Repeat as event control not supported at line @
vee	csc	cyb	wait_statement_not_cyb_csve	e					Wait statement is not supported at line @
vee	csc	cyb	disable_statement_not_cyb_csve	e					Disable statement is not supported at line @
vee	csc	cyb	events_not_supported_cyb_csve	e					Events are not supported at line @
vee	csc	cyb	fork_join_blocks_not_supported_cyb_csve	e					Fork/join blocks are not supported at line @
vee	csc	cyb	unsupp_function_return_time_cyb_csve	e					Unsupported function return time at line @
vee	csc	cyb	not_supp_events_cyb_csve	e					Events are not supported at line @
vee	csc	cyb	repeat_in_delay_or_event_cyb_csve	e					Repeat clause in delay or Event control at line @
vee	csc	cyb	ill_proc_cont_assign_stmt_cyb_csve	e					Illegal procedural continuous assignment statement at line @
vee	csc	cyb	ill_deassign_cyb_stmt_csve	e					Illegal de-assign statement at line @
vee	csc	cyb	ill_force_stmt_cyb_csve	e					Illegal force statement at line @
vee	csc	cyb	ill_release_stmt_cyb_csve	e					Illegal release statement at line @
vee	csc	cyb	repeat_not_supp_as_delay_or_event_cyb_csve	e					Repeat as delay or event control not supported at line @
vee	csc	cyb	not_supp_wait_stmt_cyb_csve	e					Wait statement is not supported at line @
vee	csc	cyb	not_supp_disable_stmt_cyb_csve	e					Disable statement is not supported at line @
vee	csc	cyb	supp_not_events_cyb_csve	e					Events are not supported at line @
vee	csc	cyb	not_supp_fork_join_blocks_cyb_csve	e					Fork/join blocks are not supported at line @
vee	csc	cyb	not_supp_UDP_cyb_csve	e					UDPs are not supported at line @
vee	csc	cyb	not_supp_defparam_cyb_csve	e					Defparam is not supported at line @
vee	csc	cyb	specify_blk_not_supported_cscve	e					Specify blocks are not supported at line @

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vee	csc	cyb	mintypmax_expr_not_supp_cscve	w					mintypmax Expressions are not supported at line @
vee	csc	decl	decl_array_over_max_size_cscve	e					Array @ exceeds maximum size limit at line @
vee	csc	dely	max_val_dly_csve	e					Too many delay values, max @ at line @
vee	csc	dely	found_gate_dely_not_allowed_cscve	e					Found gate delay which are not allowed at line @
vee	csc	dely	found_dely_in_casn_not_allowed_cscve	e					Found delay in continuous assignment which are not allowed at line @
vee	csc	dely	dely_ignoring_dely_specification_cscve	e					Delay Ignoring delay specification in Net Declaration at line @
vee	csc	dely	dely_ignoring_dely_specification_port_cscve	e					Delay Ignoring delay specification in Port Declaration at line @
vee	csc	dely	dely_ignoring_dely_specification_sig_cscve	e					Delay Ignoring delay specification in Signal Declaration at line @
vee	csc	dely	dely_ignoring_dely_before_stmt_cscve	e					Delay Ignoring delay before statement at line @
vee	csc	dely	x_or_z_in_dely_cscve	e					x or z in delay at line @
vee	csc	dely	non_int_dely_cscve	e					Non integer delay at line @
vee	csc	dmsn	mem_prts_index_out_of_range_for_mem_cscve	e					Memory part select [@:@] index @ out range for memory @ at line @
vee	csc	dmsn	dime_select_for_mem_missing_cscve	e					Select for memory @ missing at line @
vee	csc	dmsn	dime_index_out_of_bounds_for_mem_cscve	e					Index <index> out of bounds for memory @. Range [@: @] at line @
vee	csc	dmsn	dime_prts_out_of_bounds_for_net_cscve	e					Part select [@ : @] out of bounds for net @. Range [@ : @] at line @
vee	csc	dmsn	dime_prts_out_of_bounds_for_port_cscve	e					Part select [@ : @] out of bounds for port @. Range [@ : @] at line @
vee	csc	dmsn	dime_prts_out_of_bounds_for_sig_cscve	e					Part select [@ : @] out of bounds for signal @. Range [@ : @] at line @
vee	csc	dmsn	dime_prts_reg_cscve	e					Part select [@ : @] reg @. Range [@ : @] at line @
vee	csc	drvc	incompatible_drvc_for_net_cscve	e					Incompatible drivers for Net @ at line @
vee	csc	drvc	incompatible_drvc_for_port_cscve	e					Incompatible drivers for Port @ at line @
vee	csc	drvc	incompatible_drvc_for_sig_cscve	e					Incompatible drivers for Signal @ at line @
vee	csc	drvc	drvc_multiple_drive_net_partially_overlap_cscve	e					Multiple drive Net partially overlap at line @
vee	csc	drvc	drvc_multiple_drive_port_partially_overlap_cscve	e					Multiple drive Port partially overlap at line @
vee	csc	drvc	drvc_multiple_drive_sig_partially_overlap_cscve	e					Multiple drive Signal partially overlap at line @
vee	csc	dsgn	dsgn_top_mod_cannot_id_cscve	e					Top module @ cannot be identified at line @
vee	csc	dsgn	dsgn_top_entity_cannot_id_cscve	e					Top entity @ cannot be identified at line @
vee	csc	dsgn	dsgn_top_unit_cannot_id_cscve	e					Top unit @ cannot be identified at line @
vee	csc	dsgn	unit_dsgn_cycle_not_spanning_tree_cscve	e					Unit design hierarchy contains a cycle. Hierarchy is not a spanning tree. at line @
vee	csc	evc	not_allowed_edge_trigger_cscve	e					Edge trigger is not allowed in this location at line @
vee	csc	evc	ectl_in_assn_cscve	e					Event control in assignement at line @
vee	csc	expr	const_expr_nm_var_vecsc	e					Constant Expression contains variable @ at line @
vee	csc	expr	const_expr_usage_vecsc	e					Constant Expression usage at line @
vee	csc	expr	expr_prts_indices_1bit_var_cscve	e					Part select indices 1-bit variable at line @
vee	csc	expr	expr_prts_must_be_cst_expr_cscve	e					Part select specifier Expression must be constant Expression at line @
vee	csc	expr	not_const_expr_cscve	e					Repetition multiplier in concatenation is not a

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									constant Expression at line @
vee	csc	expr	ill_bit_select_expr_cscve	e					Illegal bit select expression @ at line @
vee	csc	expr	equality_operator_detected_cscve	e					Use of operator === detected at line @
vee	csc	expr	notequal_operator_detected_cscve	e					Use of operator !== detected at line @
vee	csc	expr	ill_parm_value_cscve	e					Illegal parameter value at line @
vee	csc	expr	repetition_multiplier_in_conc_not_const_expr_cscve	w					Repetition multiplier in concatenation is not a constant Expression at line @
vee	csc	expr	int_operand_not_1_bit_cscve	w					Logic operator has integer operands instead of 1-bit operands at line @
vee	csc	expr	unsupp_expr_cscve	w					Unsupported Expression type @ at line @
vee	csc	expr	unsupp_operator_cscve	w					Unsupported operator type @ at line @
vee	csc	expr	use_of_sg_bit_const_cscve	w					Use of single bit constant at line @
vee	csc	expr	unary_op_in_comparison_cscve	e					Unary op used in comparison at line @
vee	csc	expr	nonconst_repeator_in_conc_cscve	e					Non constant repeator in concatention at line @
vee	csc	expr	x_or_z_in_cond_expr_cscve	e					x or z in conditional expression at line @
vee	csc	expr	zero_in_rep_in_conc_cscve	e					Zero repeator in concatenation at line @
vee	csc	expr	expr_in_mod_port_dir_cscve	e					Expression @ in module port dir at line @
vee	csc	expr	expr_in_ent_port_dir_cscve	e					Expression @ in entity port dir at line @
vee	csc	expr	expr_in_sig_port_dir_cscve	e					Expression @ in unit port dir at line @
vee	csc	expr	expr_in_inst_cscve	e					Expression @ in inst i@ at line @
vee	csc	expr	expr_operator_operands_unequal_lenght_cscve	e					Expression operator @ operands @ unequal length at line @
vee	csc	file	cannot_open_filter_specification_file_cscve	e					Cannot open filter specification file @ at line @
vee	csc	file	filter_specification_file_missing_cscve	e					Filter specification file name @ is missing at line @
vee	csc	file	mismatch_mod_file_name_cscve	e					Mismatch between module name @ and file name @ at line @
vee	csc	file	mismatch_ent_file_name_cscve	e					Mismatch between entity name @ and file name @ at line @
vee	csc	file	mismatch_sig_file_name_cscve	e					Mismatch between signal name @ and file name @ at line @
vee	csc	forc	ill_forc_obj_type_cscve	e					Illegal force object type @ at line @
vee	csc	func	func_arg_miss_vecsc	e					Function call missing argument(s) at line @
vee	csc	func	ill_func_return_type_csve	e					Illegal function return type at line @
vee	csc	func	ill_func_csve	e					Illegal function @ at line @
vee	csc	func	port_not_output_func_cscve	e					Port @ direction cannot be output at line @
vee	csc	func	ill_use_func_cscve	e					Illegal use of function @ at line @
vee	csc	func	func_not_define_cscve	e					Function @ not defined at line @
vee	csc	func	too_many_arg_to_func_cscve	e					Too many arguments passed to function @ at line @
vee	csc	func	too_few_arg_to_func_cscve	e					Too few arguments passed to function @ at line @
vee	csc	func	undefined_func_cscve	e					Undefined function @ at line @
vee	csc	func	funct_expr_cannot_expnaded_cscve	e					Function expression @ cannot be expanded at line @
vee	csc	func	funct_not_used_in_expr_cscve	w					Function @ is not being used in an Expression at line @
vee	csc	func	func_decl_cscve	w					Function Declaration @ already declared as another type at line @
vee	csc	func	func_param_csc	e					Found function

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									parameter @ at line @
vee	csc	func	unmatched_funct_param_cscve	e					Unmatched function parameter @ at line @
vee	csc	gate	ill_output_pin_name_gate_csve	e					Illegal output terminal Expression pin @ at line @
vee	csc	hid	cannot_locate_hier_id_hid_cscve	e					Can't locate hierarchical identifier @ at line @
vee	csc	hid	ref_minst_found_in_expr_hid_cscve	e					References a module instance @ found in an Expression hid at line @
vee	csc	hid	ref_entity_found_in_expr_hid_cscve	e					References a entity instance @ found in an Expression hid at line @
vee	csc	hid	ref_unit_found_in_expr_hid_cscve	e					References a unit instance @ found in an Expression hid at line @
vee	csc	hid	ref_in_eexpr_hid_cscve	e					References a module instance @ passed as argument to PLI task call is also found in an Expression @ at line @
vee	csc	hid	ref_in_expr_hid_cscve	e					References a entity instance @ passed as argument to PLI task call is also found in an Expression @ at line @
vee	csc	hid	reff_in_expr_hid_cscve	e					References a unit instance @ passed as argument to PLI task call is also found in an Expression @ at line @
vee	csc	hid	hid_name_traverses_into_func	e					Hid @ name traverses into a function @ at line @
vee	csc	hid	hid_ref_mod_out_arg_sytk_cscve	e					Hid @ referencing a module instance passed as 'out' type argument to a system task @ at line @
vee	csc	hid	hid_ref_entity_out_arg_sytk_cscve	e					Hid @ referencing a entity instance passed as 'out' type argument to a system task @ at line @
vee	csc	hid	hid_ref_unit_out_arg_sytk_cscve	e					Hid @ referencing a unit instance passed as 'out' type argument to a system task @ at line @
vee	csc	hid	hid_reference_not_found_cscve	e					@ reference not found at line @
vee	csc	hid	mifc_in_hid_not_exist_cscve	e					Module instance @ in hid does not exist at line @
vee	csc	hid	entity_instance_in_hid_not_exist_cscve	e					Entity instance @ in hid does not exist at line @
vee	csc	hid	unit_instance_in_hid_not_exist_cscve	e					Unit instance @ in hid does not exist at line @
vee	csc	hid	mod_found_in_path_in_dsgn_cscve	e					Module @ found in path @ in the design at line @
vee	csc	hid	enity_found_in_path_in_dsgn_cscve	e					Entity @ found in path @ in the design at line @
vee	csc	hid	unit_found_in_path_in_dsgn_cscve	e					Unit @ found in path @ in the design at line @
vee	csc	hid	hierarchical_id_path_contains_func_csc	e					Hierarchical ID @ path contains a function at line @
vee	csc	id	ill_terminal_id_csve	e					Illegal terminal identifier at line @
vee	csc	init	assn_mem_in_init_blk_cscve	e					Assign memory in initial block at line @
vee	csc	inst	inst_duplicate_mod_name_cscve	e					Duplicate port @ in the port list for module @ at line @
vee	csc	inst	inst_duplicate_entity_name_cscve	e					Duplicate port @ in the port list for entity @ at line @
vee	csc	inst	inst_duplicate_unit_name_cscve	e					Duplicate port @ in the port list for unit @ at line @
vee	csc	inst	miss_declparam_inst_csve	e					Parameter Declaration missing value at line @
vee	csc	inst	ill_mod_inst_name_cscve	e					Illegal module instance @ at line @
vee	csc	inst	ill_entity_inst_name_cscve	e					Illegal entity instance @ at line @
vee	csc	inst	ill_unit_inst_name_cscve	e					Illegal unit instance @ at line @
vee	csc	inst	inst_name_defined_mod_csve	e					Instance name @ already defined in this module at line @
vee	csc	inst	inst_name_defined_ent_csve	e					Instance name @ already defined in this

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									entity at line @
vee	csc	inst	inst_name_defined_unit_csve	e					Instance name @ already defined in this unit at line @
vee	csc	inst	inst_too_many_bits_cscve	e					Too many bits for port @ of instance array @, formal @, actual @ at line @
vee	csc	inst	inst_port_not_connected_var_cscve	e					Port 'port' of instance array 'array' is not connected to variable at line @
vee	csc	inst	inst_insufficient_bits_cscve	e					Insufficient bits for port 'port' of instance array 'array ', formal number, actual number at line @
vee	csc	inst	inst_mod_name_not_defined_cscve	e					Module name not defined at line @
vee	csc	inst	inst_ent_name_not_defined_cscve	e					Entity name not defined at line @
vee	csc	inst	inst_unit_name_not_defined_cscve	e					Unit name not defined at line @
vee	csc	inst	many_mod_inst_param_assign_cscve	e					Too many module instance parameter assignments (number > rrumber) at line @
vee	csc	inst	many_entity_inst_param_assign_cscve	e					Too many entity instance parameter assignments (number > rrumber) at line @
vee	csc	inst	many_unit_inst_param_assign_cscve	e					Too many unit instance parameter assignments (number > rrumber) at line @
vee	csc	inst	complexexpr_cannot_mapped_inout_port_cscve	e					Complex Expression @ cannot be mapped to inout port @ at line @
vee	csc	inst	complexexpr_cannot_mapped_unknown_port_cscve	e					Complex Expression @ cannot be mapped to unknown type port @ at line @
vee	csc	inst	netdecl_contains_ill_prts_cscve	e					Net Declaration [@: @] contains an illegal part select at line @
vee	csc	inst	regdecl_contains_ill_prts_cscve	e					Reg Declaration [@ : @] contains an illegal part select at line @
vee	csc	inst	complex_expr_inst_parent_module_cscve	e					Complex actual Expression associated with port @ of module @ instantiated in parent module at line @
vee	csc	inst	complex_expr_inst_entity_parent_module_cscve	e					Complex actual Expression associated with port @ of entity @ instantiated in parent module at line @
vee	csc	inst	complex_expr_inst_unit_parent_module_cscve	e					Complex actual Expression associated with port @ of unit @ instantiated in parent module at line @
vee	csc	inst	inst_mod_output_port_width_cscve	e					Mod @ Output port @ width mismatch, actual-width (port-width) at line @
vee	csc	inst	inst_entity_output_port_width_cscve	e					Entity @ Output port @ width mismatch, actual-width (port-width) at line @
vee	csc	inst	inst_unit_output_port_width_cscve	e					Unit @ Output port @ width mismatch, actual-width (port-width) at line @
vee	csc	inst	inst_mod_input_port_width_cscve	e					Mod @ Input port @ width mismatch, actual-width (port-width) at line @
vee	csc	inst	inst_entity_input_port_width_cscve	e					Entity @ Input port @ width mismatch, actual-width (port-width) at line @
vee	csc	inst	inst_unit_input_port_width_cscve	e					Unit @ Input port @ width mismatch, actual-width (port-width) at line @
vee	csc	inst	inst_mod_not_define_cscve	e					Module not defined at line @
vee	csc	inst	inst_entity_not_define_cscve	e					Entity not defined at line @
vee	csc	inst	inst_unit_not_define_cscve	e					Unit not defined at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	csc	inst	miss_mifc_name_cscve	w			x		Missing module instance name. This syntax is an error according to IEEE 1364-1995 but is allowed by commercial Verilog compilers at line @
vee	csc	inst	miss_ent_instance_name_cscve	w			x		Missing entity instance name. This syntax is an error according to IEEE 1364-1995 but is allowed by commercial Verilog compilers at line @
vee	csc	inst	miss_unit_instance_name_cscve	w			x		Missing unit instance name. This syntax is an error according to IEEE 1364-1995 but is allowed by commercial Verilog compilers at line @
vee	csc	inst	mifc_port_actual_formal_width_mismatch_cscve	w					Module @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vee	csc	inst	mifc_port_actual_formal_width_mismatch_cscvh	w					Module @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vee	csc	inst	ent_port_actual_formal_width_mismatch_cscve	w					Entity @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vee	csc	inst	unit_port_actual_formal_width_mismatch_cscve	w					Unit @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vee	csc	inst	unmatched_port_connect_in_inst_cscve	e					Unmatched port @ connect in instance @ at line @
vee	csc	inst	inst_differs_in_case_from_mod_cscve	e					Instance name @ differs in case from module name @ at line @
vee	csc	inst	inst_differs_in_case_from_ent_cscve	e					Instance name @ differs in case from entity name @ at line @
vee	csc	inst	inst_differs_in_case_from_sig_cscve	e					Instance name @ differs in case from signal name @ at line @
vee	csc	lib	lib_name_not_mod_declaration_csve	e					Library file @ doesn't contain a module Declaration at line @
vee	csc	lib	lib_name_not_entity_declaration_csve	e					Library file @ doesn't contain a entity Declaration at line @
vee	csc	lib	lib_name_not_unit_declaration_csve	e					Library file @ doesn't contain a unit Declaration at line @
vee	csc	lib	lib_not_contain_supply_cscve	e					Library does not contain supply @ at line @
vee	csc	loop	while_initial_value_unknown_loop_cscve	e					While control initial variable @ unassigned. Initial value unknown at line @
vee	csc	loop	while_loop_not_assign_stmt_controlvar_cscve	e					While loop body does not contain an assignment statement for control variable @ at line @
vee	csc	loop	assign_stmt_not_last_while_loop_cscve	e					Assignment statement for control variable @ not last statement in while loop at line @
vee	csc	loop	undet_init_value_loop_cscve	e					Unable to determine init value for loop at line @
vee	csc	loop	undet_limit_loop_cscve	e					Unable to determine limit for loop at line @
vee	csc	loop	loop_bounds_calculated_int_cscve	w					Loop bounds are calculated to be integer @, check that this is correct at line @
vee	csc	loop	expr_lhs_contains_var_bit_select_cscve	w					Expression in lhs of assignment contains a variable bit select at line @
vee	csc	loop	loop_bounds_not_const_csc	w					Loop bounds are non-constant at line @
vee	csc	loop	loop_ctrl_init_expr_not_const_cscve	w					Non-constant loop bound. Loop control variable initialization Expression is not a constant Expression at line @
vee	csc	loop	loop_term_expr_not_const_cscve	w					Non-constant loop bound. loop terminating

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									Expression could not be evaluated to a constant at line @
vee	csc	loop	init_expr_reset_by_var_cscve	e					Non-constant loop bound. initializing Expression reset by variable at line @
vee	csc	loop	loop_ctrl_var_1_bit_wide_cscve	w					The loop control variable @ is one bit wide. Check the loop control variable Declaration. at line @
vee	csc	mdb	bad_mdb_net_cscve	e					Bad multi-driven Net @ at line @
vee	csc	mdb	bad_mdb_port_cscve	e					Bad multi-driven Port @ at line @
vee	csc	mdb	bad_mdb_signal_cscve	e					Bad multi-driven Signal @ at line @
vee	csc	mdb	unsupp_comp_mdb_net_cscve	e	?				Unsupported component type @ driving in multi-driven Net name at line @
vee	csc	mdb	unsupp_comp_mdb_port_cscve	e	?				Unsupported component type @ driving in multi-driven Port name at line @
vee	csc	mdb	unsupp_comp_mdb_signal_cscve	e	?				Unsupported component type @ driving in multi-driven Signal name at line @
vee	csc	mdb	unsupp_comp_drive_mdb_cscve	e	?				Unsupported component type @ driving multi-driven Net natne at line @
vee	csc	mdb	unsupp_comp_drive_mdb_port_cscve	e	?				Unsupported component type @ driving multi-driven Port natne at line @
vee	csc	mdb	unsupp_comp_drive_mdb_signal_cscve	e	?				Unsupported component type @ driving multi-driven Signal natne at line @
vee	csc	mdb	mdb_net_driven_by_trns_cscve	e					Multiply driven Net driven by transistor primitive type @ at line @
vee	csc	mdb	mdb_port_driven_by_trns_cscve	e					Multiply driven Port driven by transistor primitive type @ at line @
vee	csc	mdb	mdb_sig_driven_by_trns_cscve	e					Multiply driven Signal driven by transistor primitive type @ at line @
vee	csc	mdb	mdb_unsupp_comp_drvs_net_cscve	e					Unsupported component type driving Net drives Net connected to multi-driven Net at line @
vee	csc	mdb	mdb_unsupp_comp_drvs_port_cscve	e					Unsupported component type driving Port drives Port connected to multi-driven Port at line @
vee	csc	mdb	mdb_unsupp_comp_drvs_sig_cscve	e					Unsupported component type driving Signal drives Signal connected to multi-driven Signal at line @
vee	csc	mdb	mdb_incompatible_net_drives_multiple_net_cscve	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Net at line @
vee	csc	mdb	mdb_incompatible_port_drives_multiple_port_cscve	e					Incompatible driver driving tandem Port drives Port connected to multi-driven Port at line @
vee	csc	mdb	mdb_incompatible_sig_drives_multiple_sig_cscve	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Port at line @
vee	csc	mdb	mdb_unsupp_LHS_concatenation_cscve	e					Unsupported LHS concatenation in multi-drive 'device at line @
vee	csc	mdb	mdb_bus_has_too_many_drivers_cscve	e					Bus has too many drivers. at line @
vee	csc	mdb	mdb_always_blk_drive_cscve	w					Multiple always blocks drive name @ at line @
vee	csc	mdb	nontri_gate_drives_mdb_net_cscve	w					non-tri-state gate drives multi-driven Net at line @
vee	csc	mdb	nontri_gate_drives_mdb_port_cscve	w					non-tri-state gate drives

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									multi-driven Port at line @
vee	csc	mdb	nontri_gate_drives_mdb_sig_cscve	w					non-tri-state gate drives multi-driven Signal at line @
vee	csc	mem	mem_prts_csvee	e					Memories do not support part select specifier at line @
vee	csc	mem	ill_ref_mem_name_csve	e					Illegal hid reference to memory (name) at line @
vee	csc	mem	mem_ref_without_index_cscve	e					Memory @ referenced without index through hierarchical ID @ at line @
vee	csc	mifc	mifc_not_array_csvee	e					Ports may not be an array at line @
vee	csc	mifc	port_identifier_mifc_cscve	e					Port @ at line @
vee	csc	mifc	mifc_mod_input_port_decl_as_reg_cscve	e					Module @ input port @ declared as type reg at line @
vee	csc	mifc	mifc_entity_input_port_decl_as_reg_cscve	e					Entity @ input port @ declared as type reg at line @
vee	csc	mifc	mifc_unit_input_port_decl_as_reg_cscve	e					Unit @ input port @ declared as type reg at line @
vee	csc	mifc	mod_output_wire_redecl_reg_cscve	e					Module @ output port re-declared as type reg after use as implicitly declared wire at line @
vee	csc	mifc	enity_output_wire_redecl_reg_cscve	e					Entity @ output port re-declared as type reg after use as implicitly declared wire at line @
vee	csc	mifc	unit_output_wire_redecl_reg_cscve	e					Unit @ output port re-declared as type reg after use as implicitly declared wire at line @
vee	csc	mifc	output_port_is_mem_type_mifc_cscve	e					Output port @ is memory type at line @
vee	csc	mifc	mifc_inout_port_is_mem_type_cscve	e					Inout port @ is memory type at line @
vee	csc	mifc	mod_output_port_mismatch_actual_witdh_cscve	w					Module @ output port @ formal to actual width mismatch at line @
vee	csc	mifc	ent_output_port_mismatch_actual_witdh_cscve	w					Entity @ output port @ formal to actual width mismatch at line @
vee	csc	mifc	unit_output_port_mismatch_actual_witdh_csc	w					Unit @ output port @ formal to actual width mismatch at line @
vee	csc	mifc	port_name_different_in_upper_lower_case_cscve	e					Port name @ different in upper lower case at line @
vee	csc	mifc	port_not_def_in_iodecl_cscve	e					Port @ not defined in ioDeclaration at line @
vee	csc	mifc	port_not_def_in_portl_cscve	e					Port @ not defined in port list at line @
vee	csc	mifc	port_wiredecl_mismatch_cscve	e					Port @ wireDeclaration mismatch at line @
vee	csc	mifc	pos_based_null_inst_port_cscve	e					Position based null instance port at line @
vee	csc	mifc	last_portdecl_contains_trailcomma_cscve	e					Last portDeclaration contains a trailing comma at line @
vee	csc	mins	mins_expr_incompatible_type_cscve	e					Expression @ has an incompatible argument type @ with the port at line @
vee	csc	mins	mins_mod_not_exist_cscve	e					Module @ does not exist at line @
vee	csc	mins	mins_entity_not_exist_cscve	e					Entity @ does not exist at line @
vee	csc	mins	mins_unit_not_exist_cscve	e					Unit @ does not exist at line @
vee	csc	mins	undefined_instance_cscve	e					Undefined instance @ at line @
vee	csc	mod	mod_param_bad_number_csve	e					Module name @ parameter list contains an Incorrect number of parameter overrides at line @
vee	csc	mod	mod_entity_param_bad_number_csve	e					Entity name @ parameter list contains an Incorrect number of parameter overrides at line @
vee	csc	mod	mod_unit_param_bad_number_csve	e					Unit name @ parameter list contains an Incorrect number of parameter overrides at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	csc	mod	ill_mod_name_cscve	e					Illegal module @ at line @
vee	csc	mod	ill_mod_entity_name_cscve	e					Illegal entity @ at line @
vee	csc	mod	ill_mod_unit_name_cscve	e					Illegal unit @ at line @
vee	csc	mod	mod_mult_decl_string_cscve	e					Multiple Declarations of string detected in module @ at line @
vee	csc	mod	mod_entity_mult_decl_string_cscve	e					Multiple Declarations of string detected in entity @ at line @
vee	csc	mod	mod_unit_mult_decl_string_cscve	e					Multiple Declarations of string detected in unit @ at line @
vee	csc	mod	mod_mult_def_cscve	e					Module @ defined in multiple places at line @
vee	csc	mod	mod_ent_mult_def_cscve	e					Entity @ defined in multiple places at line @
vee	csc	mod	mod_unit_mult_def_cscve	e					Unit @ defined in multiple places at line @
vee	csc	mod	mod_no_module_found_cscve	e					No modules found at line @
vee	csc	mod	mod_no_entity_found_cscve	e					No entity found at line @
vee	csc	mod	mod_no_unit_found_cscve	e					No unit found at line @
vee	csc	mod	failed_find_mod_cscve	e					Failed to find module @ at line @
vee	csc	mod	failed_find_entity_cscve	e					Failed to find entity @ at line @
vee	csc	mod	failed_find_unit_cscve	e					Failed to find unit @ at line @
vee	csc	mod	undefined_mod_cscve	e					Undefined module @ at line @
vee	csc	mod	undefined_ent_cscve	e					Undefined entity @ at line @
vee	csc	mod	undefined_unit_cscve	e					Undefined unit @ at line @
vee	csc	mod	unexpandable_macromodule_cscve	e					Unexpandable macromodule @ at line @
vee	csc	mod	non_interconnect_in_hierarchical_mod_cscve	e					Non interconnect in hierarchical module @ at line @
vee	csc	mod	non_interconnect_in_hierarchical_ent_cscve	e					Non interconnect in hierarchical entity @ at line @
vee	csc	mod	non_interconnect_in_hierarchical_sig_cscve	e					Non interconnect in hierarchical signal @ at line @
vee	csc	mod	empty_mod_cscve	e					Empty module at line @
vee	csc	mod	empty_ent_cscve	e					Empty entity at line @
vee	csc	mod	empty_unit_cscve	e					Empty unit at line @
vee	csc	net	namereg_not_on_LHS_stmt_net_csve	e					Register @ cannot be used on LHS of this assignment statement at line @
vee	csc	net	net_implicit_wire_redecl_reg_cscve	e					Implicitly declared as a wire @ re-declared as a reg @. at line @
vee	csc	net	time_var_decl_cscve	e					Time variable @ declared at line @
vee	csc	net	time_var_bit_used_cscve	e					Time variable @ bit used at line @
vee	csc	net	undecl_net_in_mod_cscve	e					Undeclared net @ in module @ at line @
vee	csc	net	undecl_port_in_mod_cscve	e					Undeclared port @ in module @ at line @
vee	csc	net	undecl_sig_in_mod_cscve	e					Undeclared signal @ in module @ at line @
vee	csc	net	undecl_net_in_ent_cscve	e					Undeclared net @ in entity @ at line @
vee	csc	net	undecl_port_in_ent_cscve	e					Undeclared port @ in entity @ at line @
vee	csc	net	undecl_sig_in_ent_cscve	e					Undeclared signal @ in entity @ at line @
vee	csc	net	undecl_net_in_sig_cscve	e					Undeclared net @ in signal@ at line @
vee	csc	net	undecl_port_in_sig_cscve	e					Undeclared port @ in signal @ at line @
vee	csc	net	undecl_sig_in_sig_cscve	e					Undeclared signal @ in signal @ at line @
vee	csc	net	port_used_prior_to_decl_cscve	e					Port @ used prior toDeclaration at line @
vee	csc	net	1bit_with_prts_cscve	e					1-bit with part select at line @
vee	csc	netd	ill_decl_vec_cscve	e					Illegal Declaration of vector @ at line @
vee	csc	nett	nett_ill_reg_name_cscve	e					Illegal register @ at line @
vee	csc	nett	nett_ill_net_name_cscve	e					Illegal net @ at line @
vee	csc	nett	nett_ill_port_name_cscve	e					Illegal port @ at line @
vee	csc	nett	nett_ill_signal_name_cscve	e					Illegal signal @ at line @

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vee	csc	nett	net_scalar_vect_nett_cscve	e					Net declared as both scalar and vector at line @
vee	csc	nett	port_scalar_vect_nett_cscve	e					Port declared as both scalar and vector at line @
vee	csc	nett	signal_scalar_vect_nett_cscve	e					Signal declared as both scalar and vector at line @
vee	csc	nett	hot_mux_not_use_bus_connection_net_cscve	e					One hot mux can not be used for bus connection between modules Net @ at line @
vee	csc	nett	hot_mux_not_use_bus_connection_port_cscve	e					One hot mux can not be used for bus connection between modules Port @ at line @
vee	csc	nett	hot_mux_not_use_bus_connection_sig_cscve	e					One hot mux can not be used for bus connection between modules Signal @ at line @
vee	csc	nett	reg_connected_inst_inout_cscve	e					Reg @ connnected to instantiation @ inout @ at line @
vee	csc	nett	ill_net_in_proc_assn_cscve	e					Illegal net type type in procedural assignement at line @
vee	csc	nett	ill_port_in_proc_assn_cscve	e					Illegal port type type in procedural assignement at line @
vee	csc	nett	ill_sig_in_proc_assn_cscve	e					Illegal signal type type in procedural assignement at line @
vee	csc	num	not_allowed_width0_num_cscve	e					Width 0 not allowed for sized number at line @
vee	csc	num	real_num_not_allowed_cscve	e					Real numbers not allowed at line @
vee	csc	num	found_x_z_in_num_literal_cscve	e					Found x and/or z value in number literal at line @
vee	csc	num	too_many_digits_in_sized_num_cscve	w					Number of digits exceeds the width in a sized number at line @
vee	csc	num	divide_by_zero_num_cscve	e					Divide by zero at line @
vee	csc	num	child_mod_inst_parent_mod_cscve	e					Child module @ instantiates parent module @ at line @
vee	csc	num	child_ent_inst_parent_ent_cscve	e					Child entity @ instantiates entity module @ at line @
vee	csc	num	child_sig_inst_parent_sig_cscve	e					Child signal @ instantiates signal module @ at line @
vee	csc	num	int_decl_incorrect_cscve	e					Integer Declaration incorrect at line @
vee	csc	num	int_var_indexed_cscve	e					Integer variable inedexed at line @
vee	csc	parm	parm_redecl_as_reg_name_csve	e					Parameter re-declared as reg @ at line @
vee	csc	parm	parm_redecl_as_port_port_csve	e					Parameter re-declared as port @ at line @
vee	csc	parm	parm_redecl_as_net_name_csve	e					Parameter re-declared as Net @ at line @
vee	csc	parm	parm_redecl_as_port_name_csve	e					Parameter re-declared as Port @ at line @
vee	csc	parm	parm_redecl_as_signal_name_csve	e					Parameter re-declared as Signal @ at line @
vee	csc	parm	duplicate_decl_parm_name_csve	e					Duplicate declaration of parameter name @ at line @
vee	csc	parm	ill_parm_identifier_cscve	e					Illegal parameter @ at line @
vee	csc	parm	value_of_parm_OS_platform_dependent_cscve	w					Parameter select width > 32. The value is OS and platform dependent at line @
vee	csc	parm	parm_redefined_cscve	w					Parameter @ redefined at line @
vee	csc	pars	endfunction_miss_pars_csve	e					Endfunction missing at line @
vee	csc	pars	endtask_miss_pars_csve	e					Endtask missing at line @
vee	csc	pars	endmodule_miss_pars_csve	e					Endmodule missing at line @
vee	csc	pars	miss_cont_assign_pars_csve	e					Missing = sign for continuous assignment at line @
vee	csc	pli	user_syst_not_listed_in_pli_table_cscve	e					User system task @ is not listed in PLI table at line @
vee	csc	port	ill_formal_port_name_cscve	e					Illegal formal port @ at

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									line @
vee	csc	pp	text_redefined_replaced_cscve	w					Text macro redefined and replaced @. Previous definition filename, line number @ New definition filename, line number @ at line @
vee	csc	pp	undefined_macro_cscve	e					Undefined macro @ at line @
vee	csc	pp	include_file_contains_nonconst_cscve	e					Include file contains non constant @ at line @
vee	csc	pp	endif_or_else_without_ifdef_cscve	e					Endif-or-else-without ifdef at line @
vee	csc	prim	z_in_prim_inst_cscve	e					z in primitive instantiation at line @
vee	csc	prim	prim_instan_cscve	e					Primitive instantiation @ at line @
vee	csc	proc	proc_blk_missing_evc_cscve	e					Always block missing event control at line @
vee	csc	prts	type_prts_csvee	e					Type @ does not support part select specifier at line @
vee	csc	prts	type_prts_csve	e					Type @ does not support part select specifier at line @
vee	csc	prts	prts_out_of_range_cscve	e					Parameter @[@ : @]part select is out of range at line @
vee	csc	prts	ill_prts_inst_array_cscve	e					Illegal value for part select of instance array 'name' at line @
vee	csc	prts	const_prts_contains_non_const_selector_cscve	e					Constant part select @ contains a non-constant selector @ at line @
vee	csc	prts	bus_index_prts_for_var_out_of_range_cscve	e					Bus index @ integer of part select [@:@] for variable @ out of range at line @
vee	csc	prts	bus_prts_for_var_out_of_range_cscve	e					Bus part select [@:@] for variable @ out of range at line @
vee	csc	prts	bus_prts_index_out_of_name_for_var_cscve	e					Bus part select [@:@] index @ out of range for variable @ at line @
vee	csc	prts	ill_token_in_prts_cscve	e					Illegal token in part select @ at line @
vee	csc	prts	incomplete_prts_specification_cscve	e					Incomplete part select specification @ at line @
vee	csc	prts	ill_index_in_prts_cscve	e					Illegal index in part select @ at line @
vee	csc	prts	negative_index_in_prts_not_allowed_cscve	e					Negative index in part select @ not allowed at line @
vee	csc	prts	prts_index_order_reversed_cscve	e					Part select index order reversed [@ : @] [@ : @] should be [@ : @] at line @
vee	csc	prts	index_vec_over_max_size_cscve	w					Vector index @ exceeds the size of the vector. Index truncated at line @
vee	csc	prts	x_or_z_in_vec_bit_select_index_cscve	e					x or z in vector bit select index at line @
vee	csc	real	real_cscve	e					Real @ at line @
vee	csc	real	real_in_assn_cscve	e					Real @ in assignement at line @
vee	csc	real	real_in_csi_cscve	e					Real @ inCase item at line @
vee	csc	real	real_in_comparaison_cscve	e					Real @ in comparaison at line @
vee	csc	rel	ill_rel_obj_type_cscve	e					Illegal release object type type at line @
vee	csc	scop	var_erd_in_scope_cscve	e					Variable @ redfined in scope @ at line @
vee	csc	simr	inefficient_op_not_a_power_of_2_cscve	e					Division/modulus by a number not a power of 2. Inefficient simulation operation. at line @
vee	csc	simr	simr_multiple_init_blk_force_cscve	w					Multiple initial blocks force @. Unpredictable simulation result at line @
vee	csc	snsl	incomplete_snsl_cscve	w					Incomplete sensitivity list. @ is not in the sensitivity list. at line @
vee	csc	snsl	edge_sns_process_contains_data_pin_snsl_cscve	e					Edge sensitive process contains a data pin @ in the sensitivity list at line @
vee	csc	snsl	unsupp_expr_in_snsl_cscve	w					Unsupported Expression type @ in sensitivity list ' at line @

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vee	csc	snsl	always_blk_is_miss_snsl_cscve	e					Always block is missing sensitivity list at line @
vee	csc	snsl	not_all_bits_snsvar_used_csc	e					Not all bus bits of sensitivity variable @ are used in process at line @
vee	csc	snsl	partial_bus_decl_width_cscve	e	?				partial bus @ declared with width @ width @ at line @
vee	csc	snsl	contains_inst_name_cscve	e					Contains instance name @ at line @
vee	csc	snsl	bus_indexed_in_snsl_cscve	e					Bus @ indexed in sensitivity list at line @
vee	csc	stmt	ill_register_assign_csve	e					Illegal register assignment statement at line @
vee	csc	stmt	null_not_allowed_stmt_cscve	e					Null statement is not allowed here at line @
vee	csc	stmt	id_expected_FHSexpr_force_stmt_cscve	e					Simple identifier expected for LHS Expression in force-statement at line @
vee	csc	stmt	id_expected_FHSexpr_release_stmt_cscve	e					Simple identifier expected for LHS Expression in release-statement at line @
vee	csc	stmt	stmt_ill_accept_only_net_reg_mem_cscve	e					Illegal type @ can only accept net, reg, memory at line @
vee	csc	stmt	stmt_ill_accept_only_port_reg_mem_cscve	e					Illegal type @ can only accept port, reg, memory at line @
vee	csc	stmt	stmt_ill_accept_only_signal_reg_mem_cscve	e					Illegal type @ can only accept signal, reg, memory at line @
vee	csc	stmt	while_stmt_usage_disc_cscve	w					While statement usage discouraged at line @
vee	csc	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_cscve	e					Arithmetic operator RHS has one less bit than the LHS at line @
vee	csc	stmt	ar_op_unequal_lhs_rhs_cscve	e					Arithmetic operator unequal width LHS and RHS at line @
vee	csc	stmt	ar_op_unequal_var_on_rhs_csc	e					Arithmetic operator unequal width variables @ on RHS at line @
vee	csc	stmt	empty_stmt_csc	e					Empty-statement at line @
vee	csc	syst	ill_syst_task_arg_cscve	e					Illegal system task @ Argument @ at line @
vee	csc	syst	csdir_converts_syts_cscve	w				x	Lower case converts the system task $realtime return value to an integer at line @
vee	csc	syst	return_var_of_user_used_as_rhs_cscve	w					Return variable of user system task is used as a RHS variable at line @
vee	csc	task	miss_task_name_stmst_body_csve	e					Task @ body statement missing at line @
vee	csc	task	ill_task_csve	e					Illegal task @ at line @
vee	csc	task	ill_use_task_cscve	e					Illegal use of task @ at line @
vee	csc	task	ask_var_not_decl_cscve	e					Variable @ used but not declared at line @
vee	csc	task	task_not_defined_cscve	e					Task @ not defined at line @
vee	csc	task	too_few_arg_to_task_cscve	e					Too few arguments passed to task @ at line @
vee	csc	task	undefined_task_cscve	e					Undefined task @ at line @
vee	csc	task	syts_output_port_drvs_nonsqs_logic_comp_cscve	w					User system task output port drives non-sequential logic component at line @
vee	csc	task	undefioned_task_	e					Undefined task @ at line @
vee	csc	task	task_decl_error_csve	e					Task declaration error at line @
vee	csc	task	func_task_parm_cscve	e					Found function parameter @ at line @
vee	csc	task	unmatched_task_param_cscve	e					Unmatched task parameter @ at line @
vee	csc	tbcd	found_forever_tbcd_cscve	e					Found forever at line @
vee	csc	tbcd	behavioral_code_mod_cscve	e					Behavioral code in module @ at line @
vee	csc	tbcd	behavioral_code_ebt_cscve	e					Behavioral code in entity @ at line @
vee	csc	tbcd	behavioral_code_unit_cscve	e					Behavioral code in unit @ at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	csc	tri	instance_not_tri_state_device_cscve	e					Instance name is not a tri-state device at line @
vee	csc	tri	unsupp_gate_type_tristate_cscve	e					Unsupported gate type @ used for tristate at line @
vee	csc	tri	tri_not_desgn_gate_contention_cscve	e					Tristate not designed correctly gate @ can cause contention at line @
vee	csc	tri	unsupp_type_instance_tri_cscve	e					Unsupported type instance type used for tristate @ at line @
vee	csc	tri	incorrect_cont_assign_stmt_tri_gate_cscve	e					Incorrect continuous assign statement for tristate gate @ at line @
vee	csc	tri	const_assign_to_multidriven_net_cscve	e					Constant (constiznt) assigned to multi-driven Net @ at line @
vee	csc	tri	const_assign_to_multidriven_port_cscve	e					Constant (constiznt) assigned to multi-driven Port @ at line @
vee	csc	tri	const_assign_to_multidriven_signal_cscve	e					Constant (constiznt) assigned to multi-driven Signal @ at line @
vee	csc	tri	unsupp_expr_for_tri_cscve	e					Unsupported Expression type @ for tristate at line @
vee	csc	unsy	cs_equality_op_cscve	e					Case equality operator == at line @
vee	csc	unsy	deassign_stmt_cscve	e					Deassign statement at line @
vee	csc	unsy	defparam_cscve	e					Defparam at line @
vee	csc	unsy	dely_ctrl_cscve	e					Delay control at line @
vee	csc	unsy	ev_ctrl_cscve	e					Event control at line @
vee	csc	unsy	time_decl_cscve	e					Time Declaration at line @
vee	csc	unsy	wait_stmt_unsy_cscve	e					Wait statement at line @
vee	csp	ccd	misplaced_csdir_ignored_csve	e				x	Lower case directive in wrong location. Ignored at line @
vee	csp	cmdl	ill_incdir_path_dir_cmdl_csve	e					Illegal +incdir+ path @ directory does not exist at line @
vee	csp	cmdl	ill_path_cmdl_csve	e					Illegal -y path @ directory does not exist at line @
vee	csp	cmdl	cmdl_bad_uselib_libtext_csve	e					Bad 'uselib syntax expected dir, file, 'libext or clear , got character-string at line @
vee	csp	cmdl	ill_cmdl_uselib_dir_path_csve	e					Illegal 'uselib directory path @ no such directory at line @
vee	csp	cmnt	vee_csp_cmnt_miss_closing_csve	e					/* comment missing closing */ at line @
vee	csp	csi	miss_char_case_csve	e					Missing character @ at line @
vee	csp	csi	colon_for_case_csi_csp	e					Colon expected for Case item at line @
vee	csp	cyb	mintypmax_expr_cyb_vcsp	e					Mintypmax Expressions are not supported at line @
vee	csp	cyb	found_id_cyb_csv	e					Found event id syntax in the design at line @
vee	csp	cyb	cyb_ev_var_not_supp_csve	e					Event variables are not supported at line @
vee	csp	evc	not_evc_stmt_csve	e					Cannot use event control statement in this position at line @
vee	csp	expr	expr_found_reserved_word_csve	e					Expected identifier but found reserved word @ at line @
vee	csp	expr	expr_concatenation_empty_csve	e					Concatenation empty at line @
vee	csp	expr	ill_operator_expr_csve	e					Illegal operator @ at line @
vee	csp	expr	ill_operand_expr_csve	e					Illegal operand @ at line @
vee	csp	file	cannot_open_file_csve	e					Cannot open file @ at line @
vee	csp	file	line_lenght_overflow_csve	e					Line length overflow line_length @ at line @
vee	csp	file	environ_var_in_filel_csve	e					Environ variable in file list at line @
vee	csp	func	var_redecl_func_csve	e					Variable re-declared as a function @ at line @
vee	csp	func	func_def_multiple_csve	e					Function @ defined in multiple places (list all places it is defined here) at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	csp	func	ill_use_func_csve	e					Illegal use of function @ at line @
vee	csp	func	undefined_func_csve	e					Undefined function @ at line @
vee	csp	gate	gate_inst_miss_input_csve	e					Gate instance @ is missing input connections at line @
vee	csp	inst	inst_both_formal_order_csv	e					Port list cannot contain both formal to actual mappings and ordered port connections at line @
vee	csp	inst	ill_mod_inst_name_csve	e					Illegal module instance @ at line @
vee	csp	inst	ill_entity_inst_name_csve	e					Illegal entity instance @ at line @
vee	csp	inst	ill_unit_inst_name_csve	e					Illegal unit instance @ at line @
vee	csp	inst	empty_parm_mod_inst_csve	e					Empty parameter list for module instantiation @ at line @
vee	csp	inst	empty_parm_ent_inst_csve	e					Empty parameter list for entity instantiation @ at line @
vee	csp	inst	empty_parm_unit_inst_csve	e					Empty parameter list for unit instantiation @ at line @
vee	csp	lib	not_open_lib_file_csve	e					Cannot open library file @ at line @
vee	csp	list	trail_comma_list_vcs	e					Trailing comma in parentheses enclosed list at line @
vee	csp	list	list_miising_comma_csve	w					Missing comma between @ and name at line @
vee	csp	mifc	mifc_port_type_unsupported_csve	e					Port type @ unsupported at line @
vee	csp	mmod	mult_vcs_arg_div	e					Macro @ contains too many actual arguments at line @
vee	csp	mmod	miss_vcs_arg_div	e					Macro @ is missing some actual arguments at line @
vee	csp	mmod	not_else_vcs_div	e					Unmatched 'else directive at line @
vee	csp	mmod	not_endif_vcs_div	e					Unmatched 'endif directive at line @
vee	csp	mmod	not_include_vcs_div	e					Missing filename for 'include directive at line @
vee	csp	mmod	bad_include_vcs_div	e					Badly formed include directive at line @
vee	csp	mmod	fmis_include_vcs_div	e					Filename missing in #include directive at line @
vee	csp	mod	not_mod_item_csv	e					Not a module item @ at line @
vee	csp	mod	not_mod_entity_item_csv	e					Not a entity item @ at line @
vee	csp	mod	not_mod_unit_item_csv	e					Not a unit item @ at line @
vee	csp	mod	mod_miss_endmodule_csve	e					Missing endmodule at line @
vee	csp	mod	mod_no_module_found_csve	e					No modules found at line @
vee	csp	mod	mod_no_entity_found_csve	e					No entity found at line @
vee	csp	mod	mod_no_unit_found_csve	e					No unit found at line @
vee	csp	nett	nett_unsupported_reg_csve	e					Unsupported register type @ at line @
vee	csp	num	radix_h_num_vcs	ew					Illegal number radix, 'h expected at line @
vee	csp	num	radix_b_num_vcs	ew					Illegal number radix, 'b expected at line @
vee	csp	num	radix_d_num_vcs	ew					Illegal number radix, 'd expected at line @
vee	csp	num	radix_o_num_vcs	ew					Illegal number radix; 'o expected at line @
vee	csp	port	ill_formal_port_name_csve	e					Illegal formal port @ at line @
vee	csp	port	implicitly_decl_net_bit_part_select_csve	e					Implicitly declared Net (inferred 1-bit width) used with bit/part select at line @
vee	csp	port	implicitly_decl_port_bit_part_select_csve	e					Implicitly declared Port (inferred 1-bit width) used with bit/part select at line @
vee	csp	port	implicitly_decl_signal_bit_part_select_csve	e					Implicitly declared Signal (inferred 1-bit width) used with bit/part select at line @

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vee	csp	pp	ill_macronm_match_pp_csve	e					Illegal macro name @ matches existing compiler directive - illegal according to IEEE 1364-1995 S at line @
vee	csp	pp	pp_cannot_open_file_not_exist_csve	e					Cannot open include file @, file does not exist at line @
vee	csp	pp	pp_cannot_open_file_not_have_read_perm_csve	e					Cannot open include file @, file does not have read permission at line @
vee	csp	prts	prts_part_select_csve	e					Badly formed part select at line @
vee	csp	sdir	synopsys_cdir_csve	w					Found Synopsys compiler directive at line @
vee	csp	sig	not_define_wire_type_csv	e					Wire type @ at line @
vee	csp	stmt	miss_comma_stmt_vcs	e					Missing comma at line @
vee	csp	stmt	miss_semicolon_stmt_vcs	e					Missing semi colon at line @
vee	csp	stmt	miss_char_stmt_vcs	e					Missing @ at line @
vee	csp	stmt	wait_kword_stmt_vcs	e					@ expected at line @
vee	csp	stmt	null_not_allowed_stmt_csve	e					Null statement is not allowed here at line @
vee	csp	str	ill_str_char_found_csve	e					Illegal character @ found after backslash at line @
vee	csp	sysc	system_call_csve	w					Found system call @ at line @
vee	csp	task	redeclared_var_task_csve	e					Variable re-declared as a task @ at line @
vee	csp	task	task_def_multiple_csve	e					Task @ defined in multiple places (list all places it is defined here) at line @
vee	csp	task	ill_use_task_csve	e					Illegal use of task @ at line @
vee	csp	task	cannot_redefine_ve_sytk_csve	e			x		Cannot redefine Verilog system task @ at line @
vee	csp	task	task_decl_error_csvh	e					Task declaration error at line @
vee	csp	udir	other_cdir_csve	w					Found other compiler directive at line @
vee	prp	file	not_dir_name_file_vep	e					Directory @ does not exist at line @
vee	prp	file	cannot_open_file_ppve	e					Cannot open file @ at line @
vee	prp	pp	not_incl_directive_pp_ppve	e					Empty filename for 'include directive at line @
vee	prp	pp	pp_miss_macroname_ve	e					Missing macro name at line @
vee	prp	pp	ill_macroname_pp_ve	e					Illegal macro name @ at line @
vee	prp	pp	pp_text_macro_rec_ve	e					Text macro string used recursively at line @
vee	prp	pp	pp_cannot_open_libfile_ppve	e					Cannot open library file @ at line @
vee	prp	pp	pp_text_macroname_not_defined_ppve	e					Text macro (name) not defined at line @
vee	prp	pp	pp_ifdef_miss_macroname_ppve	e					'ifdef missing macro name at line @
vee	prp	pp	pp_undef_miss_macroname_ppve	e					'undef missing macro name at line @
vee	prp	pp	pp_miss_endif_directive_ppve	e					Missing 'endif directive at line @
vee	prp	pp	pp_rec_include_file_ppve	e					Recursive INCLUDE file @ at line @
vee	prp	pp	cannot_undef_nonexistent_macro	e					Attempt to 'undef a nonexistent macro @ at line @
vee	prp	pp	cmdl_arg_used_in_def_ppve	e					Command line argument used in define at line @
vee	prp	pp	pp_undef_macro_ppve	e					Undef @ not defined macro at line @
vee	vep	blk	multiple_declaration_blk	e					Named block register @ame declared in multiple locations at line @
vee	vep	ccd	misplaced_csdir_ignored_veve	e				x	Lower case directive in wrong location. Ignored at line @
vee	vep	cmdl	ill_incdir_path_dir_cmdl_veve	e					Illegal +incdir+ path @ directory does not exist at line @
vee	vep	cmdl	ill_path_cmdl_veve	e					Illegal -y path @ directory does not exist at line @
vee	vep	cmdl	cmdl_bad_uselib_libtext_veve	e					Bad 'uselib syntax expected dir, file, 'libext

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									or clear , got character-string at line @
vee	vep	cmdl	ill_cmdl_uselib_dir_path_veve	e					Illegal 'uselib directory path @ no such directory at line @
vee	vep	cmnt	vee_vep_cmnt_miss_closing_veve	e					/* comment missing closing */ at line @
vee	vep	csi	miss_char_case_veve	e					Missing character @ at line @
vee	vep	csi	colon_for_case_csi_vev	e					Colon expected for Case item at line @
vee	vep	cyb	mintypmax_expr_cyb_vvep	e					Mintypmax Expressions are not supported at line @
vee	vep	cyb	found_id_cyb_vev	e					Found event id syntax in the design at line @
vee	vep	cyb	cyb_ev_var_not_supp_veve	e					Event variables are not supported at line @
vee	vep	evc	not_evc_stmt_veve	e					Cannot use event control statement in this position at line @
vee	vep	expr	expr_s_vee	e					Expression S at line @
vee	vep	expr	expr_found_reserved_word_veve	e					Expected identifier but found reserved word @ at line @
vee	vep	expr	expr_concatenation_empty_veve	e					Concatenation empty at line @
vee	vep	expr	ill_operator_expr_veve	e					Illegal operator @ at line @
vee	vep	expr	ill_operand_expr_veve	e					Illegal operand @ at line @
vee	vep	file	cannot_open_file_veve	e					Cannot open file @ at line @
vee	vep	file	line_lenght_overflow_veve	e					Line length overflow line_length @ at line @
vee	vep	file	environ_var_in_filel_veve	e					Environ variable in file list at line @
vee	vep	func	var_redecl_func_veve	e					Variable re-declared as a function @ at line @
vee	vep	func	func_def_multiple_veve	e					Function @ defined in multiple places (list all places it is defined here) at line @
vee	vep	func	ill_use_func_veve	e					Illegal use of function @ at line @
vee	vep	func	undefined_func_veve	e					Undefined function @ at line @
vee	vep	gate	gate_inst_miss_input_veve	e					Gate instance @ is missing input connections at line @
vee	vep	inst	inst_both_formal_order_vev	e					Port list cannot contain both formal to actual mappings and ordered port connections at line @
vee	vep	inst	ill_mod_inst_name_veve	e					Illegal module instance @ at line @
vee	vep	inst	ill_entity_inst_name_veve	e					Illegal entity instance @ at line @
vee	vep	inst	ill_unit_inst_name_veve	e					Illegal unit instance @ at line @
vee	vep	inst	empty_parm_mod_inst_veve	e					Empty parameter list for module instantiation @ at line @
vee	vep	inst	empty_parm_ent_inst_veve	e					Empty parameter list for entity instantiation @ at line @
vee	vep	inst	empty_parm_unit_inst_veve	e					Empty parameter list for unit instantiation @ at line @
vee	vep	lib	not_open_lib_file_veve	e					Cannot open library file @ at line @
vee	vep	list	trail_comma_list_vcc	e					Trailing comma in parentheses enclosed list at line @
vee	vep	list	list_miising_comma_veve	w					Missing comma between @ and name at line @
vee	vep	mifc	mifc_port_type_unsupported_veve	e					Port type @ unsupported at line @
vee	vep	mmod	mult_vcc_arg_div	e					Macro @ contains too many actual arguments at line @
vee	vep	mmod	miss_vcc_arg_div	e					Macro @ is missing some actual arguments at line @
vee	vep	mmod	not_else_vcc_div	e					Unmatched 'else directive at line @
vee	vep	mmod	not_endif_vcc_div	e					Unmatched 'endif directive at line @
vee	vep	mmod	not_include_vcc_div	e					Missing filename for

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									'include directive at line @
vee	vep	mmod	bad_include_vcc_div	e					Badly formed include directive at line @
vee	vep	mmod	fmis_include_vcc_div	e					Filename missing in #include directive at line @
vee	vep	mod	not_mod_item_vev	e					Not a module item @ at line @
vee	vep	mod	not_mod_entity_item_vev	e					Not a entity item @ at line @
vee	vep	mod	not_mod_unit_item_vev	e					Not a unit item @ at line @
vee	vep	mod	mod_miss_endmodule_veve	e					Missing endmodule at line @
vee	vep	mod	mod_no_module_found_veve	e					No modules found at line @
vee	vep	mod	mod_no_entity_found_veve	e					No entity found at line @
vee	vep	mod	mod_no_unit_found_veve	e					No unit found at line @
vee	vep	nett	nett_unsupported_reg_veve	e					Unsupported register type @ at line @
vee	vep	num	radix_h_num_vcc	ew					Illegal number radix, 'h expected at line @
vee	vep	num	radix_b_num_vcc	ew					Illegal number radix, 'b expected at line @
vee	vep	num	radix_d_num_vcc	ew					Illegal number radix, 'd expected at line @
vee	vep	num	radix_o_num_vcc	ew					Illegal number radix; 'o expected at line @
vee	vep	pars	S_stmt_pars_ve	e					Statement S at line @
vee	vep	port	ill_formal_port_name_veev	e					Illegal formal port @ at line @
vee	vep	port	implicitly_decl_net_bit_part_select_veve	e					Implicitly declared Net (inferred 1-bit width) used with bit/part select at line @
vee	vep	port	implicitly_decl_port_bit_part_select_veve	e					Implicitly declared Port (inferred 1-bit width) used with bit/part select at line @
vee	vep	port	implicitly_decl_signal_bit_part_select_veve	e					Implicitly declared Signal (inferred 1-bit width) used with bit/part select at line @
vee	vep	pp	ill_macronm_match_pp_veve	e					Illegal macro name @ matches existing compiler directive - illegal according to IEEE 1364-1995 S at line @
vee	vep	pp	pp_cannot_open_file_not_exist_veve	e					Cannot open include file @, file does not exist at line @
vee	vep	pp	pp_cannot_open_file_not_have_read_perm_veve	e					Cannot open include file @, file does not have read permission at line @
vee	vep	pp	include_filne	e					Include file @ not found at line @
vee	vep	prts	prts_part_select_veve	e					Badly formed part select at line @
vee	vep	sdir	synopsys_cdir_veve	w					Found Synopsys compiler directive at line @
vee	vep	sig	not_define_wire_type_vev	e					Wire type @ at line @
vee	vep	stmt	miss_comma_stmt_vcc	e					Missing comma at line @
vee	vep	stmt	miss_semicolon_stmt_vcc	e					Missing semi colon at line @
vee	vep	stmt	miss_char_stmt_vcc	e					Missing @ at line @
vee	vep	stmt	wait_kword_stmt_vcc	e					@ expected at line @
vee	vep	stmt	null_not_allowed_stmt_veve	e					Null statement is not allowed here at line @
vee	vep	str	ill_str_char_found_veve	e					Illegal character @ found after backslash at line @
vee	vep	sysc	system_call_veve	w					Found system call @ at line @
vee	vep	task	redeclared_var_task_veve	e					Variable re-declared as a task @ at line @
vee	vep	task	task_def_multiple_veve	e					Task @ defined in multiple places (list all places it is defined here) at line @
vee	vep	task	ill_use_task_veve	e					Illegal use of task @ at line @
vee	vep	task	cannot_redefine_ve_sytk_veve	e			x		Cannot redefine Verilog system task @ at line @
vee	vep	task	task_decl_error_vevh	e					Task declaration error at line @
vee	vep	udir	other_cdir_veve	w					Found other compiler directive at line @
vee	vhp	ccd	misplaced_csdir_ignored_vhve	e				x	Lower case directive in

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									wrong location. Ignored at line @
vee	vhp	cmdl	ill_incdir_path_dir_cmdl_vhve	e					Illegal +incdir+ path @ directory does not exist at line @
vee	vhp	cmdl	ill_path_cmdl_vhve	e					Illegal -y path @ directory does not exist at line @
vee	vhp	cmdl	cmdl_bad_uselib_libtext_vhve	e					Bad 'uselib syntax expected dir, file, 'libext or clear , got character-string at line @
vee	vhp	cmdl	ill_cmdl_uselib_dir_path_vhve	e					Illegal 'uselib directory path @ no such directory at line @
vee	vhp	cmnt	vee_vhp_cmnt_miss_closing_vhve	e					/* comment missing closing */ at line @
vee	vhp	csi	miss_char_case_vhve	e					Missing character @ at line @
vee	vhp	csi	colon_for_case_csi_vhv	e					Colon expected for Case item at line @
vee	vhp	cyb	mintypmax_expr_cyb_vvhp	e					Mintypmax Expressions are not supported at line @
vee	vhp	cyb	found_id_cyb_vhv	e					Found event id syntax in the design at line @
vee	vhp	cyb	cyb_ev_var_not_supp_vhve	e					Event variables are not supported at line @
vee	vhp	evc	not_evc_stmt_vhve	e					Cannot use event control statement in this position at line @
vee	vhp	expr	expr_found_reserved_word_vhve	e					Expected identifier but found reserved word @ at line @
vee	vhp	expr	expr_concatenation_empty_vhve	e					Concatenation empty at line @
vee	vhp	expr	ill_operator_expr_vhve	e					Illegal operator @ at line @
vee	vhp	expr	ill_operand_expr_vhve	e					Illegal operand @ at line @
vee	vhp	file	cannot_open_file_vhve	e					Cannot open file @ at line @
vee	vhp	file	line_lenght_overflow_vhve	e					Line length overflow line_length @ at line @
vee	vhp	file	environ_var_in_filel_vhve	e					Environ variable in file list at line @
vee	vhp	func	var_redecl_func_vhve	e					Variable re-declared as a function @ at line @
vee	vhp	func	func_def_multiple_vhve	e					Function @ defined in multiple places (list all places it is defined here) at line @
vee	vhp	func	ill_use_func_vhve	e					Illegal use of function @ at line @
vee	vhp	func	undefined_func_vhve	e					Undefined function @ at line @
vee	vhp	gate	gate_inst_miss_input_vhve	e					Gate instance @ is missing input connections at line @
vee	vhp	inst	inst_both_formal_order_vhv	e					Port list cannot contain both formal to actual mappings and ordered port connections at line @
vee	vhp	inst	ill_mod_inst_name_vhve	e					Illegal module instance @ at line @
vee	vhp	inst	ill_entity_inst_name_vhve	e					Illegal entity instance @ at line @
vee	vhp	inst	ill_unit_inst_name_vhve	e					Illegal unit instance @ at line @
vee	vhp	inst	empty_parm_mod_inst_vhve	e					Empty parameter list for module instantiation @ at line @
vee	vhp	inst	empty_parm_ent_inst_vhve	e					Empty parameter list for entity instantiation @ at line @
vee	vhp	inst	empty_parm_unit_inst_vhve	e					Empty parameter list for unit instantiation @ at line @
vee	vhp	lib	not_open_lib_file_vhve	e					Cannot open library file @ at line @
vee	vhp	list	trail_comma_list_vch	e					Trailing comma in parentheses enclosed list at line @
vee	vhp	list	list_miising_comma_vhve	w					Missing comma between @ and name at line @
vee	vhp	mifc	mifc_port_type_unsupported_vhve	e					Port type @ unsupported at line @
vee	vhp	mmod	mult_vch_arg_div	e					Macro @ contains too many actual arguments

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									at line @
vee	vhp	mmod	miss_vch_arg_div	e					Macro @ is missing some actual arguments at line @
vee	vhp	mmod	not_else_vch_div	e					Unmatched 'else directive at line @
vee	vhp	mmod	not_endif_vch_div	e					Unmatched 'endif directive at line @
vee	vhp	mmod	not_include_vch_div	e					Missing filename for 'include directive at line @
vee	vhp	mmod	bad_include_vch_div	e					Badly formed include directive at line @
vee	vhp	mmod	fmis_include_vch_div	e					Filename missing in #include directive at line @
vee	vhp	mod	not_mod_item_vhv	e					Not a module item @ at line @
vee	vhp	mod	not_mod_entity_item_vhv	e					Not a entity item @ at line @
vee	vhp	mod	not_mod_unit_item_vhv	e					Not a unit item @ at line @
vee	vhp	mod	mod_miss_endmodule_vhve	e					Missing endmodule at line @
vee	vhp	mod	mod_no_module_found_vhve	e					No modules found at line @
vee	vhp	mod	mod_no_entity_found_vhve	e					No entity found at line @
vee	vhp	mod	mod_no_unit_found_vhve	e					No unit found at line @
vee	vhp	nett	nett_unsupported_reg_vhve	e					Unsupported register type @ at line @
vee	vhp	num	radix_h_num_vch	ew					Illegal number radix, 'h expected at line @
vee	vhp	num	radix_b_num_vch	ew					Illegal number radix, 'b expected at line @
vee	vhp	num	radix_d_num_vch	ew					Illegal number radix, 'd expected at line @
vee	vhp	num	radix_o_num_vch	ew					Illegal number radix; 'o expected at line @
vee	vhp	port	ill_formal_port_name_vhve	e					Illegal formal port @ at line @
vee	vhp	port	implicitly_decl_net_bit_part_select_vhve	e					Implicitly declared Net (inferred 1-bit width) used with bit/part select at line @
vee	vhp	port	implicitly_decl_port_bit_part_select_vhve	e					Implicitly declared Port (inferred 1-bit width) used with bit/part select at line @
vee	vhp	port	implicitly_decl_signal_bit_part_select_vhve	e					Implicitly declared Signal (inferred 1-bit width) used with bit/part select at line @
vee	vhp	pp	ill_macronm_match_pp_vhve	e					Illegal macro name @ matches existing compiler directive - illegal according to IEEE 1364-1995 S at line @
vee	vhp	pp	pp_cannot_open_file_not_exist_vhve	e					Cannot open include file @, file does not exist at line @
vee	vhp	pp	pp_cannot_open_file_not_have_read_perm_vhve	e					Cannot open include file @, file does not have read permission at line @
vee	vhp	prts	prts_part_select_vhve	e					Badly formed part select at line @
vee	vhp	sdir	synopsys_cdir_vhve	w					Found Synopsys compiler directive at line @
vee	vhp	sig	not_define_wire_type_vhv	e					Wire type @ at line @
vee	vhp	stmt	miss_comma_stmt_vch	e					Missing comma at line @
vee	vhp	stmt	miss_semicolon_stmt_vch	e					Missing semi colon at line @
vee	vhp	stmt	miss_char_stmt_vch	e					Missing @ at line @
vee	vhp	stmt	wait_kword_stmt_vch	e					@ expected at line @
vee	vhp	stmt	null_not_allowed_stmt_vhve	e					Null statement is not allowed here at line @
vee	vhp	str	ill_str_char_found_vhve	e					Illegal character @ found after backslash at line @
vee	vhp	sysc	system_call_vhve	w					Found system call @ at line @
vee	vhp	task	redeclared_var_task_vhve	e					Variable re-declared as a task @ at line @
vee	vhp	task	task_def_multiple_vhve	e					Task @ defined in multiple places (list all places it is defined here) at line @
vee	vhp	task	ill_use_task_vhve	e					Illegal use of task @ at line @
vee	vhp	task	cannot_redefine_ve_sytk_vhve	e			x		Cannot redefine Verilog

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									system task @ at line @
vee	vhp	task	task_decl_error_vhvh	e					Task declaration error at line @
vee	vhp	udir	other_cdir_vhve	w					Found other compiler directive at line @
vhe	cda	assn	unequal_length_lhs_rhs_cdvh	e					Unequal length LHS and RHS at line @
vhe	cda	assn	unequal_length_lhs_rhs_off_one_bit_cdvh	e					Unequal length LHS and RHS off by one bit at line @
vhe	cda	blk	var_not_assigned_in_all_branches_cdve	e					Variable @ not assigned in all branches at line @
vhe	cda	clk	unsupp_logic_operation_cdvh	w					Unsupported logic operation type @. at line @
vhe	cda	clk	unsupp_cl_gated_logic_cdvh	w					Unsupported gated clock logic type. at line @
vhe	cda	clk	unsupp_logic_expr_clk_cdvh	w					Unsupported logicExpression type @ at line @
vhe	cda	csi	noncnst_in_iclude_file_cdvh	e					Non-constant in include file @ at line @
vhe	cda	drvc	multiply_drvn_net_nontri_gate_cdvh	w					Multiply drivenNet driven by a non-tristate gate at line @
vhe	cda	drvc	multiply_drvn_port_nontri_gate_cdvh	w					Multiply drivenPort driven by a non-tristate gate at line @
vhe	cda	drvc	multiply_drvn_sig_nontri_gate_cdvh	w					Multiply drivenSignal driven by a non-tristate gate at line @
vhe	cda	drvc	incompatible_driver_net_cdvh	w					Incompatible driver of type @ drivingNet_@ multi drivenNet of type @ name @ at line @
vhe	cda	drvc	incompatible_driver_port_cdvh	w					Incompatible driver of type @ drivingPort_@ multi drivenPort of type @ name @ at line @
vhe	cda	drvc	incompatible_driver_sig_cdvh	w					Incompatible driver of type @ drivingSignal_@ multi drivenSignal of type @ name @ at line @
vhe	cda	expr	unary_op_in_comparison_cdvh	e					Unary op used in comparison at line @
vhe	cda	expr	miss_parenthesis_cdvh	e					Unary op @ with comparison op @ missing precedence parenthesis at line @
vhe	cda	init	assn_mem_in_init_blk_cdvh	e					Assign memory in initial block at line @
vhe	cda	inst	input_port_drvn_from_inside_mod_cdvh	e					Input port @ being driven from inside of module @ at line @
vhe	cda	inst	input_port_drvn_from_inside_entity_cdvh	e					Input port @ being driven from inside of entity @ at line @
vhe	cda	inst	input_port_drvn_from_inside_signal_cdvh	e					Input port @ being driven from inside of signal @ at line @
vhe	cda	inst	input_port_not_connected_in_parent_mod_cdvh	e					Input port @ not connected in parent module at line @
vhe	cda	inst	input_port_not_connected_in_parent_entity_cdvh	e					Input port @ not connected in parent entity at line @
vhe	cda	inst	input_port_not_connected_in_parent_signal_cdvh	e					Input port @ not connected in parent signal at line @
vhe	cda	mdb	single_comp_contains_multiple_tri_drv_cdvh	w					A single component contains multiple tristate drivers at line @
vhe	cda	mdb	unsuppexpr_on_lhs_net_drv_stmt_cdvh	w					Unsupported Expression type type on LHS ofNet driver statement at line @
vhe	cda	mdb	unsuppexpr_on_lhs_port_drv_stmt_cdvh	w					Unsupported Expression type type on LHS ofPort driver statement at line @
vhe	cda	mdb	unsuppexpr_on_lhs_sig_drv_stmt_cdvh	w					Unsupported Expression type type on LHS ofSignal driver statement at line @
vhe	cda	mdb	tri_not_in_top_mod_cdvh	e					Tristate not in top module at line @
vhe	cda	mdb	tri_not_in_top_ent_cdvh	e					Tristate not in top entity at line @
vhe	cda	mdb	tri_not_in_top_sig_cdvh	e					Tristate not in top signal at line @
vhe	cda	mdb	tri_primitive_inst_cdvh	e					Tristate primitive

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									instantiation at line @
vhe	cda	mdb	tri_net_only_one_drvr_cdvh	e					Tri Net has only one driver at line @
vhe	cda	mdb	tri_port_only_one_drvr_cdvh	e					Tri Port has only one driver at line @
vhe	cda	mdb	tri_sig_only_one_drvr_cdvh	e					Tri Signal has only one driver at line @
vhe	cda	mod	redef_mod_cdvh	e					Redefined module @ at line @
vhe	cda	mod	redef_ent_cdvh	e					Redefined entity @ at line @
vhe	cda	mod	redef_signal_cdvh	e					Redefined signal @ at line @
vhe	cda	net	tri_and_net_only_one_driver_cdvh	e	?				triandNet @ has only one driver at line @
vhe	cda	net	tri_and_port_only_one_driver_cdvh	e	?				triandPort @ has only one driver at line @
vhe	cda	net	tri_and_sig_only_one_driver_cdvh	e	?				triandSignal @ has only one driver at line @
vhe	cda	net	var_assn_but_never_ref_cdvh	e					Variable @ assigned but never referenced at line @
vhe	cda	net	var_never_assn_cdvh	e					Variable @ never assigned at line @
vhe	cda	net	var_not_assn_in_all_paths_cdvh	e					Variable @ not being assigned in all paths at line @
vhe	cda	net	var_not_in_snsl_cdvh	e					Variable @ not in sensitivity list at line @
vhe	cda	net	reg_connected_to_inout_in_inst_cdvh	e					Reg @ connected to inout @ in instantiation @ at line @
vhe	cda	net	reg_connectede_to_output_in_inst_cdvh	e					Reg @ connected to output in instantiation at line @
vhe	cda	net	reg_used_as_output_of_cont_assn_cdvh	e					Reg @ used as output of continuous assign at line @
vhe	cda	net	port_used_prior_to_decl_cdvh	e					Port @ used prior toDeclaration at line @
vhe	cda	num	var_modulus_by_0_cdve	e					Variable @ modulus by zero at line @
vhe	cda	parm	redef_param_cdvh	e					Redefined parameter @ at line @
vhe	cda	pp	redef_macro_cdvh	e					Redefined macro @ at line @
vhe	cda	prts	vec_index_order_incorrect_cdvh	e					Vector index @ order incorrect at line @
vhe	cda	prts	vec_index_truncated_cdvh	e					Vector index @ truncated at line @
vhe	cda	sig	sig_will_float_when_rel_cdvh	e					Signal @ will float when it is released at line @
vhe	cda	sply	output_conncet_to_sply_	e					Output @ connect to supply at line @
vhe	cda	stmt	miss_else_stmt_cdvh	e					Missing else statement at line @
vhe	cda	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_cdvh	e					Arithmetic operator RHS has one less bit than the LHS at line @
vhe	cda	stmt	ar_op_unequal_lhs_rhs_cdvh	e					Arithmetic operator unequal width LHS and RHS at line @
vhe	cda	tri	tri_not_in_top_mod_cdvh	e					Tristate @ not in top module at line @
vhe	cda	tri	tri_not_in_top_entity_cdvh	e					Tristate @ not in top entity at line @
vhe	cda	tri	tri_not_in_top_signal_cdvh	e					Tristate @ not in top signal at line @
vhe	cda	tri	tri_prim_ist_cdvh	e					Tristate primitive instantiation @ at line @
vhe	cdc	assn	x_in_rhs_of_assihnment_cdcvh	e					x in rhs of assignment at line @
vhe	cdc	assn	z_in_rhs_of_assn_default_csi_cdcvh	e					x in rhs of assignement in defaultCase item at line @
vhe	cdc	assn	z_in_rhs_of_assn_cdcvh	e					z in rhs of assignement at line @
vhe	cdc	assn	unequal_length_lhs_rhs_cdcvh	e					Unequal length LHS and RHS at line @
vhe	cdc	assn	unequal_length_lhs_rhs_off_one_bit_cdcvh	e					Unequal length LHS and RHS off by one bit at line @
vhe	cdc	ccd	ccd_cdir_must_be_cst_expr_cdcvh	e				x	CSL directive size must be constant Expression at line @
vhe	cdc	clk	clk_name_not_found_cdir_cdcvh	e				x	Clock name not found in cslc directive at line @
vhe	cdc	clk	expr_sunj_to_different_clk_phases_cdcvh	e					Expression subject to different clock phases at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	cdc	cond	if_case_cond_expr_cdcve	e					If/case conditional expression @ syntax error at line @
vhe	cdc	cond	if_no_else_cdcve	e					If no else at line @
vhe	cdc	csi	xcsi_not_in_casex_cdcvh	e					xCase item not in casex at line @
vhe	cdc	csi	noncstn_rep_in_conc_cdcvh	e					Non-constant repeator in concatenation at line @
vhe	cdc	csi	cond_expr_in_csi_cdcvh	e					Conditional Expression inCase item at line @
vhe	cdc	csi	full_case_has_default_cdcvh	e					Full case has default at line @
vhe	cdc	css	sns_pragma_full_case_cdcvh	e					Assume a full case, missing default or synopsys pragma full case. at line @
vhe	cdc	decl	decl_array_over_max_size_cdcvh	e					Array @ exceeds maximum size limit at line @
vhe	cdc	dely	x_or_z_in_dely_cdcvh	e					x or z in delay at line @
vhe	cdc	dmsn	mem_prts_index_out_of_range_for_mem_cdcvh	e					Memory part select [@:@] index @ out range for memory @ at line @
vhe	cdc	dmsn	dime_select_for_mem_missing_cdcvh	e					Select for memory @ missing at line @
vhe	cdc	dmsn	dime_index_out_of_bounds_for_mem_cdcvh	e					Index <index> out of bounds for memory @. Range [@: @] at line @
vhe	cdc	dmsn	dime_prts_out_of_bounds_for_net_cdcvh	e					Part select [@ : @] out of bounds for net @. Range [@ : @] at line @
vhe	cdc	dmsn	dime_prts_out_of_bounds_for_port_cdcvh	e					Part select [@ : @] out of bounds for port @. Range [@ : @] at line @
vhe	cdc	dmsn	dime_prts_out_of_bounds_for_sig_cdcvh	e					Part select [@ : @] out of bounds for signal @. Range [@ : @] at line @
vhe	cdc	dmsn	dime_prts_reg_cdcvh	e					Part select [@ : @] reg @. Range [@ : @] at line @
vhe	cdc	drvc	incompatible_drvc_for_net_cdcvh	e					Incompatible drivers for Net @ at line @
vhe	cdc	drvc	incompatible_drvc_for_port_cdcvh	e					Incompatible drivers for Port @ at line @
vhe	cdc	drvc	incompatible_drvc_for_sig_cdcvh	e					Incompatible drivers for Signal @ at line @
vhe	cdc	drvc	drvc_multiple_drive_net_partially_overlap_cdcvh	e					Multiple drive Net partially overlap at line @
vhe	cdc	drvc	drvc_multiple_drive_port_partially_overlap_cdcvh	e					Multiple drive Port partially overlap at line @
vhe	cdc	drvc	drvc_multiple_drive_sig_partially_overlap_cdcvh	e					Multiple drive Signal partially overlap at line @
vhe	cdc	dsgn	dsgn_top_mod_cannot_id_cdcvh	e					Top module @ cannot be identified at line @
vhe	cdc	dsgn	dsgn_top_entity_cannot_id_cdcvh	e					Top entity @ cannot be identified at line @
vhe	cdc	dsgn	dsgn_top_unit_cannot_id_cdcvh	e					Top unit @ cannot be identified at line @
vhe	cdc	dsgn	unit_dsgn_cycle_not_spanning_tree_cdcvh	e					Unit design hierarchy contains a cycle. Hierarchy is not a spanning tree. at line @
vhe	cdc	expr	const_expr_nm_var_vhcdc	e					Constant Expression contains variable @ at line @
vhe	cdc	expr	const_expr_usage_vhcdc	e					Constant Expression usage at line @
vhe	cdc	expr	expr_prts_indices_1bit_var_cdcvh	e					Part select indices 1-bit variable at line @
vhe	cdc	expr	expr_prts_must_be_cst_expr_cdcvh	e					Part select specifier Expression must be constant Expression at line @
vhe	cdc	expr	not_const_expr_cdcvh	e					Repetition multiplier in concatenation is not a constant Expression at line @
vhe	cdc	expr	ill_bit_select_expr_cdcvh	e					Illegal bit select expression @ at line @
vhe	cdc	expr	repetition_multiplier_in_conc_not_const_expr_cdcvh	w					Repetition multiplier in concatenation is not a constant Expression at line @
vhe	cdc	expr	int_operand_not_1_bit_cdcvh	w					Logic operator has integer operands instead of 1-bit operands at line @
vhe	cdc	expr	unsupp_expr_cdcvh	w					Unsupported Expression type @ at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	cdc	expr	unsupp_operator_cdcvh	w					Unsupported operator type @ at line @
vhe	cdc	expr	use_of_sg_bit_const_cdcvh	w					Use of single bit constant at line @
vhe	cdc	expr	unary_op_in_comparison_cdcvh	e					Unary op used in comparison at line @
vhe	cdc	expr	x_or_z_in_cond_expr_cdcvh	e					x or z in conditional expression at line @
vhe	cdc	expr	zero_in_rep_in_conc_cdcvh	e					Zero repeator in concatenation at line @
vhe	cdc	expr	expr_in_mod_port_dir_cdcvh	e					Expression @ in module port dir at line @
vhe	cdc	expr	expr_in_ent_port_dir_cdcvh	e					Expression @ in entity port dir at line @
vhe	cdc	expr	expr_in_sig_port_dir_cdcvh	e					Expression @ in unit port dir at line @
vhe	cdc	expr	expr_in_inst_cdcvh	e					Expression @ in inst i@ at line @
vhe	cdc	expr	expr_operator_operands_unequal_lenght_cdcvh	e					Expression operator @ operands @ unequal length at line @
vhe	cdc	file	cannot_open_filter_specification_file_cdcvh	e					Cannot open filter specification file @ at line @
vhe	cdc	file	filter_specification_file_missing_cdcvh	e					Filter specification file name @ is missing at line @
vhe	cdc	file	mismatch_mod_file_name_cdcvh	e					Mismatch between module name @ and file name @ at line @
vhe	cdc	file	mismatch_ent_file_name_cdcvh	e					Mismatch between entity name @ and file name @ at line @
vhe	cdc	file	mismatch_sig_file_name_cdcvh	e					Mismatch between signal name @ and file name @ at line @
vhe	cdc	func	func_arg_miss_vhcdc	e					Function call missing argument(s) at line @
vhe	cdc	func	port_not_output_func_cdvh	e					Port @ direction cannot be output at line @
vhe	cdc	func	too_many_arg_to_func_cdcvh	e					Too many arguments passed to function @ at line @
vhe	cdc	func	too_few_arg_to_func_cdcvh	e					Too few arguments passed to function @ at line @
vhe	cdc	func	undefined_func_cscvh	e					Undefined function @ at line @
vhe	cdc	func	undefined_func_cdcvh	e					Undefined function @ at line @
vhe	cdc	func	funct_expr_cannot_expnaded_cdcvh	e					Function expression @ cannot be expanded at line @
vhe	cdc	func	funct_not_used_in_expr_cdcvh	w					Function @ is not being used in an Expression at line @
vhe	cdc	func	func_decl_cdcvh	w					Function Declaration @ already declared as another type at line @
vhe	cdc	hid	cannot_locate_hier_id_hid_cdcvh	e					Can't locate hierarchical identifier @ at line @
vhe	cdc	hid	ref_minst_found_in_expr_hid_cdcvh	e					References a module instance @ found in an Expression hid at line @
vhe	cdc	hid	ref_entity_found_in_expr_hid_cdcvh	e					References a entity instance @ found in an Expression hid at line @
vhe	cdc	hid	ref_unit_found_in_expr_hid_cdcvh	e					References a unit instance @ found in an Expression hid at line @
vhe	cdc	hid	hid_reference_not_found_cdcvh	e					@ reference not found at line @
vhe	cdc	hid	mifc_in_hid_not_exist_cdcvh	e					Module instance @ in hid does not exist at line @
vhe	cdc	hid	entity_instance_in_hid_not_exist_cdcvh	e					Entity instance @ in hid does not exist at line @
vhe	cdc	hid	unit_instance_in_hid_not_exist_cdcvh	e					Unit instance @ in hid does not exist at line @
vhe	cdc	hid	mod_found_in_path_in_dsgn_cdcvh	e					Module @ found in path @ in the design at line @
vhe	cdc	hid	enity_found_in_path_in_dsgn_cdcvh	e					Entity @ found in path @ in the design at line @
vhe	cdc	hid	unit_found_in_path_in_dsgn_cdcvh	e					Unit @ found in path @ in the design at line @
vhe	cdc	hid	hierarchical_id_path_contains_func_cdc	e					Hierarchical ID @ path contains a function at line @
vhe	cdc	init	assn_mem_in_init_blk_cdcvh	e					Assign memory in initial block at line @
vhe	cdc	inst	inst_duplicate_mod_name_cdcvh	e					Duplicate port @ in the

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									port list for module @ at line @
vhe	cdc	inst	inst_duplicate_entity_name_cdcvh	e					Duplicate port @ in the port list for entity @ at line @
vhe	cdc	inst	inst_duplicate_unit_name_cdcvh	e					Duplicate port @ in the port list for unit @ at line @
vhe	cdc	inst	ill_mod_inst_name_cdcvh	e					Illegal module instance @ at line @
vhe	cdc	inst	ill_entity_inst_name_cdcvh	e					Illegal entity instance @ at line @
vhe	cdc	inst	ill_unit_inst_name_cdcvh	e					Illegal unit instance @ at line @
vhe	cdc	inst	inst_name_defined_mod_cdcvh	e					Instance name @ already defined in this module at line @
vhe	cdc	inst	inst_name_defined_ent_cdcvh	e					Instance name @ already defined in this entity at line @
vhe	cdc	inst	inst_name_defined_unit_cdcvh	e					Instance name @ already defined in this unit at line @
vhe	cdc	inst	inst_too_many_bits_cdcvh	e					Too many bits for port @ of instance array @, formal @, actual @ at line @
vhe	cdc	inst	inst_port_not_connected_var_cdcvh	e					Port 'port' of instance array 'array' is not connected to variable at line @
vhe	cdc	inst	inst_insufficient_bits_cdcvh	e					Insufficient bits for port 'port' of instance array 'array ', formal number, actual number at line @
vhe	cdc	inst	inst_mod_name_not_defined_cdcvh	e					Module name not defined at line @
vhe	cdc	inst	inst_ent_name_not_defined_cdcvh	e					Entity name not defined at line @
vhe	cdc	inst	inst_unit_name_not_defined_cdcvh	e					Unit name not defined at line @
vhe	cdc	inst	many_mod_inst_param_assign_cdcvh	e					Too many module instance parameter assignments (number > rrumber) at line @
vhe	cdc	inst	many_entity_inst_param_assign_cdcvh	e					Too many entity instance parameter assignments (number > rrumber) at line @
vhe	cdc	inst	many_unit_inst_param_assign_cdcvh	e					Too many unit instance parameter assignments (number > rrumber) at line @
vhe	cdc	inst	complexexpr_cannot_mapped_inout_port_cdcvh	e					Complex Expression @ cannot be mapped to inout port @ at line @
vhe	cdc	inst	complexexpr_cannot_mapped_unknown_port_cdcvh	e					Complex Expression @ cannot be mapped to unknown type port @ at line @
vhe	cdc	inst	netdecl_contains_ill_prts_cdcvh	e					Net Declaration [@: @] contains an illegal part select at line @
vhe	cdc	inst	regdecl_contains_ill_prts_cdcvh	e					Reg Declaration [@ : @] contains an illegal part select at line @
vhe	cdc	inst	complex_expr_inst_parent_module_cdcvh	e					Complex actual Expression associated with port @ of module @ instantiated in parent module at line @
vhe	cdc	inst	complex_expr_inst_entity_parent_module_cdcvh	e					Complex actual Expression associated with port @ of entity @ instantiated in parent module at line @
vhe	cdc	inst	complex_expr_inst_unit_parent_module_cdcvh	e					Complex actual Expression associated with port @ of unit @ instantiated in parent module at line @
vhe	cdc	inst	inst_mod_output_port_width_cdcvh	e					Mod @ Output port @ width mismatch, actual-width (port-width) at line @
vhe	cdc	inst	inst_entity_output_port_width_cdcvh	e					Entity @ Output port @ width mismatch, actual-width (port-width) at line @
vhe	cdc	inst	inst_unit_output_port_width_cdcvh	e					Unit @ Output port @ width mismatch,

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									actual-width (port-width) at line @
vhe	cdc	inst	inst_mod_input_port_width_cdcvh	e					Mod @ Input port @ width mismatch, actual-width (port-width) at line @
vhe	cdc	inst	inst_entity_input_port_width_cdcvh	e					Entity @ Input port @ width mismatch, actual-width (port-width) at line @
vhe	cdc	inst	inst_unit_input_port_width_cdcvh	e					Unit @ Input port @ width mismatch, actual-width (port-width) at line @
vhe	cdc	inst	inst_mod_not_define_cdcvh	e					Module not defined at line @
vhe	cdc	inst	inst_entity_not_define_cdcvh	e					Entity not defined at line @
vhe	cdc	inst	inst_unit_not_define_cdcvh	e					Unit not defined at line @
vhe	cdc	inst	mifc_port_actual_formal_width_mismatch_cdcvh	w					Module @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vhe	cdc	inst	ent_port_actual_formal_width_mismatch_cdcvh	w					Entity @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vhe	cdc	inst	unit_port_actual_formal_width_mismatch_cdcvh	w					Unit @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vhe	cdc	inst	inst_differs_in_case_from_mod_cdcvh	e					Instance name @ differs in case from module name @ at line @
vhe	cdc	inst	inst_differs_in_case_from_ent_cdcvh	e					Instance name @ differs in case from entity name @ at line @
vhe	cdc	inst	inst_differs_in_case_from_sig_cdcvh	e					Instance name @ differs in case from signal name @ at line @
vhe	cdc	loop	undet_init_value_loop_cdcvh	e					Unable to determine init value for loop at line @
vhe	cdc	loop	undet_limit_loop_cdcvh	e					Unable to determine limit for loop at line @
vhe	cdc	loop	loop_bounds_calculated_int_cdcvh	w					Loop bounds are calculated to be integer @, check that this is correct at line @
vhe	cdc	loop	expr_lhs_contains_var_bit_select_cdcvh	w					Expression in lhs of assignment contains a variable bit select at line @
vhe	cdc	loop	loop_bounds_not_const_cdc	w					Loop bounds are non-constant at line @
vhe	cdc	loop	loop_ctrl_init_expr_not_const_cdcvh	w					Non-constant loop bound. Loop control variable initialization Expression is not a constant Expression at line @
vhe	cdc	loop	loop_term_expr_not_const_cdcve	w					Non-constant loop bound. loop terminating Expression could not be evaluated to a constant at line @
vhe	cdc	loop	init_expr_reset_by_var_cdcvh	e					Non-constant loop bound. initializing Expression reset by variable at line @
vhe	cdc	loop	loop_ctrl_var_1_bit_wide_cdcvh	w					The loop control variable @ is one bit wide. Check the loop control variable Declaration. at line @
vhe	cdc	mdb	bad_mdb_net_cdcvh	e					Bad multi-driven Net @ at line @
vhe	cdc	mdb	bad_mdb_port_cdcvh	e					Bad multi-driven Port @ at line @
vhe	cdc	mdb	bad_mdb_signal_cdcvh	e					Bad multi-driven Signal @ at line @
vhe	cdc	mdb	unsupp_comp_mdb_net_cdcvh	e	?				Unsupported component type @ driving in multi-driven Net name at line @
vhe	cdc	mdb	unsupp_comp_mdb_port_cdcvh	e	?				Unsupported component type @ driving in multi-driven Port name at line @
vhe	cdc	mdb	unsupp_comp_mdb_signal_cdcvh	e	?				Unsupported component type @ driving in multi-driven Signal name at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	cdc	mdb	unsupp_comp_drive_mdb_cdcvh	e	?				Unsupported component type @ driving multi-driven Net natne at line @
vhe	cdc	mdb	unsupp_comp_drive_mdb_port_cdcvh	e	?				Unsupported component type @ driving multi-driven Port natne at line @
vhe	cdc	mdb	unsupp_comp_drive_mdb_signal_cdcvh	e	?				Unsupported component type @ driving multi-driven Signal natne at line @
vhe	cdc	mdb	mdb_net_driven_by_trns_cdcvh	e					Multiply driven Net driven by transistor primitive type @ at line @
vhe	cdc	mdb	mdb_port_driven_by_trns_cdcvh	e					Multiply driven Port driven by transistor primitive type @ at line @
vhe	cdc	mdb	mdb_sig_driven_by_trns_cdcvh	e					Multiply driven Signal driven by transistor primitive type @ at line @
vhe	cdc	mdb	mdb_unsupp_comp_drvs_net_cdcvh	e					Unsupported component type driving Net drives Net connected to multi-driven Net at line @
vhe	cdc	mdb	mdb_unsupp_comp_drvs_port_cdcvh	e					Unsupported component type driving Port drives Port connected to multi-driven Port at line @
vhe	cdc	mdb	mdb_unsupp_comp_drvs_sig_cdcvh	e					Unsupported component type driving Signal drives Signal connected to multi-driven Signal at line @
vhe	cdc	mdb	mdb_incompatible_net_drives_multiple_net_cdcvh	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Net at line @
vhe	cdc	mdb	mdb_incompatible_port_drives_multiple_port_cdcvh	e					Incompatible driver driving tandem Port drives Port connected to multi-driven Port at line @
vhe	cdc	mdb	mdb_incompatible_sig_drives_multiple_sig_cdcvh	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Port at line @
vhe	cdc	mdb	mdb_unsupp_LHS_concatenation_cdcvh	e					Unsupported LHS concatenation in multi-drive 'device at line @
vhe	cdc	mdb	mdb_bus_has_too_many_drivers_cdcvh	e					Bus has too many drivers. at line @
vhe	cdc	mdb	mdb_always_blk_drive_cdcvh	w					Multiple always blocks drive name @ at line @
vhe	cdc	mdb	nontri_gate_drives_mdb_net_cdcvh	w					non-tri-state gate drives multi-driven Net at line @
vhe	cdc	mdb	nontri_gate_drives_mdb_port_cdcvh	w					non-tri-state gate drives multi-driven Port at line @
vhe	cdc	mdb	nontri_gate_drives_mdb_sig_cdcvh	w					non-tri-state gate drives multi-driven Signal at line @
vhe	cdc	mem	mem_prts_cdv	e					Memories do not support part select specifier at line @
vhe	cdc	mem	mem_ref_without_index_cdcvh	e					Memory @ referenced without index through hierarchical ID @ at line @
vhe	cdc	mem	ill_mem_cdcvh	e					Illegal memory @ at line @
vhe	cdc	mifc	mifc_not_array_cdv	e					Ports may not be an array at line @
vhe	cdc	mifc	port_identifier_mifc_cdcvh	e					Port @ at line @
vhe	cdc	mifc	mod_output_wire_redecl_reg_cdcvh	e					Module @ output port re-declared as type reg after use as implicitly declared wire at line @
vhe	cdc	mifc	entity_output_wire_redecl_reg_cdcvh	e					Entity @ output port re-declared as type reg after use as implicitly declared wire at line @
vhe	cdc	mifc	unit_output_wire_redecl_reg_cdcvh	e					Unit @ output port re-declared as type reg after use as implicitly declared wire at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	cdc	mifc	output_port_is_mem_type_mifc_cdcvh	e					Output port @ is memory type at line @
vhe	cdc	mifc	mifc_inout_port_is_mem_type_cdcvh	e					Inout port @ is memory type at line @
vhe	cdc	mifc	mod_output_port_mismatch_actual_witdh_cdcvh	w					Module @ output port @ formal to actual width mismatch at line @
vhe	cdc	mifc	ent_output_port_mismatch_actual_witdh_cdcvh	w					Entity @ output port @ formal to actual width mismatch at line @
vhe	cdc	mifc	unit_output_port_mismatch_actual_witdh_cdc	w					Unit @ output port @ formal to actual width mismatch at line @
vhe	cdc	mifc	port_name_different_in_upper_lower_case_cdcvh	e					Port name @ different in upper lower case at line @
vhe	cdc	mifc	port_not_def_in_iodecl_cdcvh	e					Port @ not defined in ioDeclaration at line @
vhe	cdc	mifc	port_not_def_in_portl_cdcvh	e					Port @ not defined in port list at line @
vhe	cdc	mifc	port_wiredecl_mismatch_cdcvh	e					Port @ wireDeclaration mismatch at line @
vhe	cdc	mifc	pos_based_null_inst_port_cdcvh	e					Position based null instance port at line @
vhe	cdc	mifc	last_portdecl_contains_trailcomma_cdcvh	e					Last portDeclaration contains a trailing comma at line @
vhe	cdc	mins	mins_expr_incompatible_type_cdcvh	e					Expression @ has an incompatible argument type @ with the port at line @
vhe	cdc	mins	mins_mod_not_exist_cdcvh	e					Module @ does not exist at line @
vhe	cdc	mins	mins_entity_not_exist_cdcvh	e					Entity @ does not exist at line @
vhe	cdc	mins	mins_unit_not_exist_cdcvh	e					Unit @ does not exist at line @
vhe	cdc	mod	dup_declar_name_mod_cdv	e					Duplicate Declaration of port @ at line @
vhe	cdc	mod	ill_mod_name_cdcvh	e					Illegal module @ at line @
vhe	cdc	mod	ill_mod_entity_name_cdcvh	e					Illegal entity @ at line @
vhe	cdc	mod	ill_mod_unit_name_cdcvh	e					Illegal unit @ at line @
vhe	cdc	mod	mod_mult_decl_string_cdcvh	e					Multiple Declarations of string detected in module @ at line @
vhe	cdc	mod	mod_entity_mult_decl_string_cdcvh	e					Multiple Declarations of string detected in entity @ at line @
vhe	cdc	mod	mod_unit_mult_decl_string_cdcvh	e					Multiple Declarations of string detected in unit @ at line @
vhe	cdc	mod	mod_mult_def_cdcvh	e					Module @ defined in multiple places at line @
vhe	cdc	mod	mod_ent_mult_def_cdcvh	e					Entity @ defined in multiple places at line @
vhe	cdc	mod	mod_unit_mult_def_cdcvh	e					Unit @ defined in multiple places at line @
vhe	cdc	mod	mod_no_module_found_cdcvh	e					No modules found at line @
vhe	cdc	mod	mod_no_entity_found_cdcvh	e					No entity found at line @
vhe	cdc	mod	mod_no_unit_found_cdcvh	e					No unit found at line @
vhe	cdc	mod	failed_find_mod_cdcvh	e					Failed to find module @ at line @
vhe	cdc	mod	failed_find_entity_cdcvh	e					Failed to find entity @ at line @
vhe	cdc	mod	failed_find_unit_cdcvh	e					Failed to find unit @ at line @
vhe	cdc	mod	empty_mod_cdcvh	e					Empty module at line @
vhe	cdc	mod	empty_ent_cdcvh	e					Empty entity at line @
vhe	cdc	mod	empty_unit_cdcvh	e					Empty unit at line @
vhe	cdc	net	net_implicit_wire_redecl_reg_cdcvh	e					Implicitly declared as a wire @ re-declared as a reg @. at line @
vhe	cdc	net	undecl_net_in_mod_cdcvh	e					Undeclared net @ in module @ at line @
vhe	cdc	net	undecl_port_in_mod_cdcvh	e					Undeclared port @ in module @ at line @
vhe	cdc	net	undecl_sig_in_mod_cdcvh	e					Undeclared signal @ in module @ at line @
vhe	cdc	net	undecl_net_in_ent_cdcvh	e					Undeclared net @ in entity @ at line @
vhe	cdc	net	undecl_port_in_ent_cdcvh	e					Undeclared port @ in entity @ at line @
vhe	cdc	net	undecl_sig_in_ent_cdcvh	e					Undeclared signal @ in entity @ at line @
vhe	cdc	net	undecl_net_in_sig_cdcvh	e					Undeclared net @ in signal @ at line @
vhe	cdc	net	undecl_port_in_sig_cdcvh	e					Undeclared port @ in signal @ at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	cdc	net	undecl_sig_in_sig_cdcvh	e					Undeclared signal @ in signal @ at line @
vhe	cdc	net	port_used_prior_to_decl_cdcvh	e					Port @ used prior toDeclaration at line @
vhe	cdc	net	1bit_with_prts_cdcvh	e					1-bit with part select at line @
vhe	cdc	netd	ill_decl_vec_cdcvh	e					Illegal Declaration of vector @ at line @
vhe	cdc	nett	nett_ill_reg_name_cdcvh	e					Illegal register @ at line @
vhe	cdc	nett	nett_ill_net_name_cdcvh	e					Illegal net @ at line @
vhe	cdc	nett	nett_ill_port_name_cdcvh	e					Illegal port @ at line @
vhe	cdc	nett	nett_ill_signal_name_cdcvh	e					Illegal signal @ at line @
vhe	cdc	nett	net_scalar_vect_nett_cdcvh	e					Net declared as both scalar and vector at line @
vhe	cdc	nett	port_scalar_vect_nett_cdcvh	e					Port declared as both scalar and vector at line @
vhe	cdc	nett	signal_scalar_vect_nett_cdcvh	e					Signal declared as both scalar and vector at line @
vhe	cdc	nett	hot_mux_not_use_bus_connection_net_cdcvh	e					One hot mux can not be used for bus connection between modules Net @ at line @
vhe	cdc	nett	hot_mux_not_use_bus_connection_port_cdcvh	e					One hot mux can not be used for bus connection between modules Port @ at line @
vhe	cdc	nett	hot_mux_not_use_bus_connection_sig_cdcvh	e					One hot mux can not be used for bus connection between modules Signal @ at line @
vhe	cdc	num	not_allowed_width0_num_cdcvh	e					Width 0 not allowed for sized number at line @
vhe	cdc	num	real_num_not_allowed_cdcvh	e					Real numbers not allowed at line @
vhe	cdc	num	found_x_z_in_num_literal_cdcvh	e					Found x and/or z value in number literal at line @
vhe	cdc	num	too_many_digits_in_sized_num_cdcvh	w					Number of digits exceeds the width in a sized number at line @
vhe	cdc	num	divide_by_zero_num_cdcvh	e					Divide by zero at line @
vhe	cdc	num	child_mod_inst_parent_mod_cdcvh	e					Child module @ instantiates parent module @ at line @
vhe	cdc	num	child_ent_inst_parent_ent_cdcvh	e					Child entity @ instantiates entity module @ at line @
vhe	cdc	num	child_sig_inst_parent_sig_cdcvh	e					Child signal @ instantiates signal module @ at line @
vhe	cdc	num	int_decl_incorrect_cdcvh	e					Integer Declaration incorrect at line @
vhe	cdc	num	int_var_indexed_cdcvh	e					Integer variable inedexed at line @
vhe	cdc	parm	ill_parm_identifier_cdcvh	e					Illegal parameter @ at line @
vhe	cdc	parm	value_of_parm_OS_platform_dependent_cdcvh	w					Parameter select width > 32. The value is OS and platform dependent at line @
vhe	cdc	parm	parm_redefined_cdcvh	w					Parameter @ redefined at line @
vhe	cdc	port	ill_formal_port_name_cdcvh	e					Illegal formal port @ at line @
vhe	cdc	pp	text_redefined_replaced_cdcvh	w					Text macro redefined and replaced @. Previous definition filename, line number @ New definition filename, line number @ at line @
vhe	cdc	pp	endif_or_else_without_ifdef_cdcvh	e					Endif-or-else-without ifdef at line @
vhe	cdc	prim	z_in_prim_inst_cdcvh	e					z in primitive instantiation at line @
vhe	cdc	prts	type_prts_cdv	e					Type @ does not support part select specifier at line @
vhe	cdc	prts	prts_out_of_range_cdcvh	e					Parameter @[@ : @]part select is out of range at line @
vhe	cdc	prts	ill_prts_inst_array_cdcvh	e					Illegal value for part select of instance array 'name' at line @
vhe	cdc	prts	const_prts_contains_non_const_selector_cdcvh	e					Constant part select @ contains a non-constant selector @ at line @
vhe	cdc	prts	bus_index_prts_for_var_out_of_range_cdcvh	e					Bus index @ integer of

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									part select [@:@] for variable @ out of range at line @
vhe	cdc	prts	bus_prts_for_var_out_of_range_cdcvh	e					Bus part select [@:@] for variable @ out of range at line @
vhe	cdc	prts	bus_prts_index_out_of_name_for_var_cdcvh	e					Bus part select [@:@] index @ out of range for variable @ at line @
vhe	cdc	prts	ill_token_in_prts_cdcvh	e					Illegal token in part select @ at line @
vhe	cdc	prts	incomplete_prts_specification_cdcvh	e					Incomplete part select specification @ at line @
vhe	cdc	prts	ill_index_in_prts_cdcvh	e					Illegal index in part select @ at line @
vhe	cdc	prts	negative_index_in_prts_not_allowed_cdcvh	e					Negative index in part select @ not allowed at line @
vhe	cdc	prts	prts_index_order_reversed_cdcvh	e					Part select index order reversed [@ : @] [@ : @] should be [@ : @] at line @
vhe	cdc	prts	index_vec_over_max_size_cdcvh	w					Vector index @ exceeds the size of the vector. Index truncated at line @
vhe	cdc	prts	x_or_z_in_vec_bit_select_index_cdcvh	e					x or z in vector bit select index at line @
vhe	cdc	simr	inefficient_op_not_a_power_of_2_cdcvh	e					Division/modulus by a number not a power of 2. Inefficient simulation operation. at line @
vhe	cdc	simr	simr_multiple_init_blk_force_cdcvh	w					Multiple initial blocks force @. Unpredictable simulation result at line @
vhe	cdc	snsl	incomplete_snsl_cdcvh	w					Incomplete sensitivity list. @ is not in the sensitivity list. at line @
vhe	cdc	snsl	edge_sns_process_contains_data_pin_snsl_cdcvh	e					Edge sensitive process contains a data pin @ in the sensitivity list at line @
vhe	cdc	snsl	unsupp_expr_in_snsl_cdcvh	w					Unsupported Expression type @ in sensitivity list ' at line @
vhe	cdc	snsl	partial_bus_decl_width_cdcvh	e	?				partial bus @ declared with width @ width @ at line @
vhe	cdc	snsl	contains_inst_name_cdcvh	e					Contains instance name @ at line @
vhe	cdc	stmt	null_not_allowed_stmt_cdcvh	e					Null statement is not allowed here at line @
vhe	cdc	stmt	stmt_ill_accept_only_net_reg_mem_cdcvh	e					Illegal type @ can only accept net, reg, memory at line @
vhe	cdc	stmt	stmt_ill_accept_only_port_reg_mem_cdcvh	e					Illegal type @ can only accept port, reg, memory at line @
vhe	cdc	stmt	stmt_ill_accept_only_signal_reg_mem_cdcvh	e					Illegal type @ can only accept signal, reg, memory at line @
vhe	cdc	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_cdcvh	e					Arithmetic operator RHS has one less bit than the LHS at line @
vhe	cdc	stmt	ar_op_unequal_lhs_rhs_cdcvh	e					Arithmetic operator unequal width LHS and RHS at line @
vhe	cdc	stmt	ar_op_unequal_var_on_rhs_cdc	e					Arithmetic operator unequal width variables @ on RHS at line @
vhe	cdc	stmt	empty_stmt_cdc	e					Empty-statement at line @
vhe	cdc	syst	return_var_of_user_used_as_rhs_cdcvh	w					Return variable of user system task is used as a RHS variable at line @
vhe	cdc	task	ask_var_not_decl_cdcvh	e					Variable @ used but not declared at line @
vhe	cdc	task	too_many_arg_to_task_cdcve	e					Too many arguments passed to task @ at line @
vhe	cdc	task	too_few_arg_to_task_cdcvh	e					Too few arguments passed to task @ at line @
vhe	cdc	tri	instance_not_tri_state_device_cdcvh	e					Instance name is not a tri-state device at line @
vhe	cdc	tri	unsupp_gate_type_tristate_cdcvh	e					Unsupported gate type @ used for tristate at line @
vhe	cdc	tri	tri_not_desgn_gate_contention_cdcvh	e					Tristate not designed correctly gate @ can cause contention at line

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									@
vhe	cdc	tri	unsupp_type_instance_tri_cdcvh	e					Unsupported type instance type used for tristate @ at line @
vhe	cdc	tri	incorrect_cont_assign_stmt_tri_gate_cdcvh	e					Incorrect continuous assign statement for tristate gate @ at line @
vhe	cdc	tri	const_assign_to_multidriven_net_cdcvh	e					Constant (constiznt) assigned to multi-driven Net @ at line @
vhe	cdc	tri	const_assign_to_multidriven_port_cdcvh	e					Constant (constiznt) assigned to multi-driven Port @ at line @
vhe	cdc	tri	const_assign_to_multidriven_signal_cdcvh	e					Constant (constiznt) assigned to multi-driven Signal @ at line @
vhe	cdc	tri	unsupp_expr_for_tri_cdcvh	e					Unsupported Expression type @ for tristate at line @
vhe	csa	assn	unequal_length_lhs_rhs_csvh	e					Unequal length LHS and RHS at line @
vhe	csa	assn	unequal_length_lhs_rhs_off_one_bit_csvh	e					Unequal length LHS and RHS off by one bit at line @
vhe	csa	blk	var_not_assigned_in_all_branches_csve	e					Variable @ not assigned in all branches at line @
vhe	csa	clk	unsupp_logic_operation_csvh	w					Unsupported logic operation type @. at line @
vhe	csa	clk	unsupp_cl_gated_logic_csvh	w					Unsupported gated clock logic type. at line @
vhe	csa	clk	unsupp_logic_expr_clk_csvh	w					Unsupported logicExpression type @ at line @
vhe	csa	csi	noncnst_in_iclude_file_csvh	e					Non-constant in include file @ at line @
vhe	csa	drvc	multiply_drvn_net_nontri_gate_csvh	w					Multiply drivenNet driven by a non-tristate gate at line @
vhe	csa	drvc	multiply_drvn_port_nontri_gate_csvh	w					Multiply drivenPort driven by a non-tristate gate at line @
vhe	csa	drvc	multiply_drvn_sig_nontri_gate_csvh	w					Multiply drivenSignal driven by a non-tristate gate at line @
vhe	csa	drvc	incompatible_driver_net_csvh	w					Incompatible driver of type @ drivingNet_@ multi drivenNet of type @ name @ at line @
vhe	csa	drvc	incompatible_driver_port_csvh	w					Incompatible driver of type @ drivingPort_@ multi drivenPort of type @ name @ at line @
vhe	csa	drvc	incompatible_driver_sig_csvh	w					Incompatible driver of type @ drivingSignal_@ multi drivenSignal of type @ name @ at line @
vhe	csa	expr	unary_op_in_comparison_csvh	e					Unary op used in comparison at line @
vhe	csa	expr	miss_parenthesis_csvh	e					Unary op @ with comparison op @ missing precedence parenthesis at line @
vhe	csa	init	assn_mem_in_init_blk_csvh	e					Assign memory in initial block at line @
vhe	csa	inst	input_port_drvn_from_inside_mod_csvh	e					Input port @ being driven from inside of module @ at line @
vhe	csa	inst	input_port_drvn_from_inside_entity_csvh	e					Input port @ being driven from inside of entity @ at line @
vhe	csa	inst	input_port_drvn_from_inside_signal_csvh	e					Input port @ being driven from inside of signal @ at line @
vhe	csa	inst	input_port_not_connected_in_parent_mod_csvh	e					Input port @ not connected in parent module at line @
vhe	csa	inst	input_port_not_connected_in_parent_entitycsvh	e					Input port @ not connected in parent entity at line @
vhe	csa	inst	input_port_not_connected_in_parent_signal_csvh	e					Input port @ not connected in parent signal at line @
vhe	csa	mdb	single_comp_contains_multiple_tri_drv_csvh	w					A single component contains multiple tristate drivers at line @
vhe	csa	mdb	unsuppexpr_on_lhs_net_drv_stmt_csvh	w					Unsupported Expression type type on LHS ofNet driver statement at line @
vhe	csa	mdb	unsuppexpr_on_lhs_port_drv_stmt_csvh	w					Unsupported Expression

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									type type on LHS ofPort driver statement at line @
vhe	csa	mdb	unsuppexpr_on_lhs_sig_drv_stmt_csvh	w					Unsupported Expression type type on LHS ofSignal driver statement at line @
vhe	csa	mdb	tri_not_in_top_mod_csvh	e					Tristate not in top module at line @
vhe	csa	mdb	tri_not_in_top_ent_csvh	e					Tristate not in top entity at line @
vhe	csa	mdb	tri_not_in_top_sig_csvh	e					Tristate not in top signal at line @
vhe	csa	mdb	tri_primitive_inst_csvh	e					Tristate primitive instantiation at line @
vhe	csa	mdb	tri_net_only_one_drvr_csvh	e					Tri Net has only one driver at line @
vhe	csa	mdb	tri_port_only_one_drvr_csvh	e					Tri Port has only one driver at line @
vhe	csa	mdb	tri_sig_only_one_drvr_csvh	e					Tri Signal has only one driver at line @
vhe	csa	mod	redef_mod_csvh	e					Redefined module @ at line @
vhe	csa	mod	redef_ent_csvh	e					Redefined entity @ at line @
vhe	csa	mod	redef_signal_csvh	e					Redefined signal @ at line @
vhe	csa	net	tri_and_net_only_one_driver_csvh	e	?				triandNet @ has only one driver at line @
vhe	csa	net	tri_and_port_only_one_driver_csvh	e	?				triandPort @ has only one driver at line @
vhe	csa	net	tri_and_sig_only_one_driver_csvh	e	?				triandSignal @ has only one driver at line @
vhe	csa	net	var_assn_but_never_ref_csvh	e					Variable @ assigned but never referenced at line @
vhe	csa	net	var_never_assn_csvh	e					Variable @ never assigned at line @
vhe	csa	net	var_not_assn_in_all_paths_csvh	e					Variable @ not being assigned in all paths at line @
vhe	csa	net	var_not_in_snsl_csvh	e					Variable @ not in sensitivity list at line @
vhe	csa	net	reg_connected_to_inout_in_inst_csvh	e					Reg @ connected to inout @ in instantiation @ at line @
vhe	csa	net	reg_connectede_to_output_in_inst_csvh	e					Reg @ connected to output in instantiation at line @
vhe	csa	net	reg_used_as_output_of_cont_assn_csvh	e					Reg @ used as output of continuous assign at line @
vhe	csa	net	port_used_prior_to_decl_csvh	e					Port @ used prior toDeclaration at line @
vhe	csa	num	var_modulus_by_0_csve	e					Variable @ modulus by zero at line @
vhe	csa	parm	redef_param_csvh	e					Redefined parameter @ at line @
vhe	csa	pp	redef_macro_csvh	e					Redefined macro @ at line @
vhe	csa	prts	vec_index_order_incorrect_csvh	e					Vector index @ order incorrect at line @
vhe	csa	prts	vec_index_truncated_csvh	e					Vector index @ truncated at line @
vhe	csa	sig	sig_will_float_when_rel_csvh	e					Signal @ will float when it is released at line @
vhe	csa	sply	output_conncet_to_sply_	e					Output @ connect to supply at line @
vhe	csa	stmt	miss_else_stmt_csvh	e					Missing else statement at line @
vhe	csa	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_csvh	e					Arithmetic operator RHS has one less bit than the LHS at line @
vhe	csa	stmt	ar_op_unequal_lhs_rhs_scvh	e					Arithmetic operator unequal width LHS and RHS at line @
vhe	csa	stmt	ar_op_unequal_var_on_rhs_csvh	e					Arithmetic operator unequal width variables @ on RHS at line @
vhe	csa	stmt	ar_op_unequal_var_on_rhs_cdvh	e					Arithmetic operator unequal width variables @ on RHS at line @
vhe	csa	tri	tri_not_in_top_mod_csvh	e					Tristate @ not in top module at line @
vhe	csa	tri	tri_not_in_top_entity_csvh	e					Tristate @ not in top entity at line @
vhe	csa	tri	tri_not_in_top_signal_csvh	e					Tristate @ not in top signal at line @
vhe	csa	tri	tri_prim_ist_csvh	e					Tristate primitive instantiation @ at line @

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vhe	csb	assn	x_in_rhs_of_assihnment_csbvh	e					x in rhs of assignment at line @
vhe	csb	assn	z_in_rhs_of_assn_default_csi_csbvh	e					x in rhs of assignement in defaultCase item at line @
vhe	csb	assn	z_in_rhs_of_assn_csbvh	e					z in rhs of assignement at line @
vhe	csb	assn	unequal_length_lhs_rhs_csbvh	e					Unequal length LHS and RHS at line @
vhe	csb	assn	unequal_length_lhs_rhs_off_one_bit_csbvh	e					Unequal length LHS and RHS off by one bit at line @
vhe	csb	ccd	ccd_cdir_must_be_cst_expr_csbvh	e				x	CSL directive size must be constant Expression at line @
vhe	csb	clk	clk_name_not_found_cdir_csbvh	e				x	Clock name not found in cslc directive at line @
vhe	csb	clk	expr_sunj_to_different_clk_phases_csbvh	e					Expression subject to different clock phases at line @
vhe	csb	cond	if_case_cond_expr_csbve	e					If/case conditional expression @ syntax error at line @
vhe	csb	cond	if_no_else_csbve	e					If no else at line @
vhe	csb	csi	xcsi_not_in_casex_csbvh	e					xCase item not in casex at line @
vhe	csb	csi	noncstn_rep_in_conc_csbvh	e					Non-constant repeator in concatenation at line @
vhe	csb	csi	cond_expr_in_csi_csbvh	e					Conditional Expression inCase item at line @
vhe	csb	csi	full_case_has_default_csbvh	e					Full case has default at line @
vhe	csb	css	sns_pragma_full_case_csbvh	e					Assume a full case, missing default or synopsys pragma full case. at line @
vhe	csb	decl	decl_array_over_max_size_csbvh	e					Array @ exceeds maximum size limit at line @
vhe	csb	dely	x_or_z_in_dely_csbvh	e					x or z in delay at line @
vhe	csb	dmsn	mem_prts_index_out_of_range_for_mem_csbvh	e					Memory part select [@:@] index @ out range for memory @ at line @
vhe	csb	dmsn	dime_select_for_mem_missing_csbvh	e					Select for memory @ missing at line @
vhe	csb	dmsn	dime_index_out_of_bounds_for_mem_csbvh	e					Index <index> out of bounds for memory @. Range [@: @] at line @
vhe	csb	dmsn	dime_prts_out_of_bounds_for_net_csbvh	e					Part select [@ : @] out of bounds for net @. Range [@ : @] at line @
vhe	csb	dmsn	dime_prts_out_of_bounds_for_port_csbvh	e					Part select [@ : @] out of bounds for port @. Range [@ : @] at line @
vhe	csb	dmsn	dime_prts_out_of_bounds_for_sig_csbvh	e					Part select [@ : @] out of bounds for signal @. Range [@ : @] at line @
vhe	csb	dmsn	dime_prts_reg_csbvh	e					Part select [@ : @] reg @. Range [@ : @] at line @
vhe	csb	drvc	incompatible_drvc_for_net_csbvh	e					Incompatible drivers for Net @ at line @
vhe	csb	drvc	incompatible_drvc_for_port_csbvh	e					Incompatible drivers for Port @ at line @
vhe	csb	drvc	incompatible_drvc_for_sig_csbvh	e					Incompatible drivers for Signal @ at line @
vhe	csb	drvc	drvc_multiple_drive_net_partially_overlap_csbvh	e					Multiple drive Net partially overlap at line @
vhe	csb	drvc	drvc_multiple_drive_port_partially_overlap_csbvh	e					Multiple drive Port partially overlap at line @
vhe	csb	drvc	drvc_multiple_drive_sig_partially_overlap_csbvh	e					Multiple drive Signal partially overlap at line @
vhe	csb	dsgn	dsgn_top_mod_cannot_id_csbvh	e					Top module @ cannot be identified at line @
vhe	csb	dsgn	dsgn_top_entity_cannot_id_csbvh	e					Top entity @ cannot be identified at line @
vhe	csb	dsgn	dsgn_top_unit_cannot_id_csbvh	e					Top unit @ cannot be identified at line @
vhe	csb	dsgn	unit_dsgn_cycle_not_spanning_tree_csbvh	e					Unit design hierarchy contains a cycle. Hierarchy is not a spanning tree. at line @
vhe	csb	expr	expr_prts_indices_1bit_var_csbvh	e					Part select indices 1-bit variable at line @
vhe	csb	expr	expr_prts_must_be_cst_expr_csbvh	e					Part select specifier Expression must be constant Expression at line @
vhe	csb	expr	not_const_expr_csbvh	e					Repetition multiplier in

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									concatenation is not a constant Expression at line @
vhe	csb	expr	ill_bit_select_expr_csbvh	e					Illegal bit select expression @ at line @
vhe	csb	expr	repetition_multiplier_in_conc_not_const_expr_csbvh	w					Repetition multiplier in concatenation is not a constant Expression at line @
vhe	csb	expr	int_operand_not_1_bit_csbvh	w					Logic operator has integer operands instead of 1-bit operands at line @
vhe	csb	expr	unsupp_expr_csbvh	w					Unsupported Expression type @ at line @
vhe	csb	expr	unsupp_operator_csbvh	w					Unsupported operator type @ at line @
vhe	csb	expr	use_of_sg_bit_const_csbvh	w					Use of single bit constant at line @
vhe	csb	expr	unary_op_in_comparison_csbvh	e					Unary op used in comparison at line @
vhe	csb	expr	x_or_z_in_cond_expr_csbvh	e					x or z in conditional expression at line @
vhe	csb	expr	zero_in_rep_in_conc_csbvh	e					Zero repeator in concatenation at line @
vhe	csb	expr	expr_in_mod_port_dir_csbvh	e					Expression @ in module port dir at line @
vhe	csb	expr	expr_in_ent_port_dir_csbvh	e					Expression @ in entity port dir at line @
vhe	csb	expr	expr_in_sig_port_dir_csbvh	e					Expression @ in unit port dir at line @
vhe	csb	expr	expr_in_inst_csbvh	e					Expression @ in inst i@ at line @
vhe	csb	expr	expr_operator_operands_unequal_lenght_csbvh	e					Expression operator @ operands @ unequal length at line @
vhe	csb	file	cannot_open_filter_specification_file_csbvh	e					Cannot open filter specification file @ at line @
vhe	csb	file	filter_specification_file_missing_csbvh	e					Filter specification file name @ is missing at line @
vhe	csb	file	mismatch_mod_file_name_csbvh	e					Mismatch between module name @ and file name @ at line @
vhe	csb	file	mismatch_ent_file_name_csbvh	e					Mismatch between entity name @ and file name @ at line @
vhe	csb	file	mismatch_sig_file_name_csbvh	e					Mismatch between signal name @ and file name @ at line @
vhe	csb	func	port_not_output_func_csbvh	e					Port @ direction cannot be output at line @
vhe	csb	func	too_many_arg_to_func_csbvh	e					Too many arguments passed to function @ at line @
vhe	csb	func	too_few_arg_to_func_csbvh	e					Too few arguments passed to function @ at line @
vhe	csb	func	undefined_func_csbvh	e					Undefined function @ at line @
vhe	csb	func	funct_expr_cannot_expnaded_csbvh	e					Function expression @ cannot be expanded at line @
vhe	csb	func	funct_not_used_in_expr_csbvh	w					Function @ is not being used in an Expression at line @
vhe	csb	func	func_decl_csbvh	w					Function Declaration @ already declared as another type at line @
vhe	csb	hid	cannot_locate_hier_id_hid_csbvh	e					Can't locate hierarchical identifier @ at line @
vhe	csb	hid	ref_minst_found_in_expr_hid_csbvh	e					References a module instance @ found in an Expression hid at line @
vhe	csb	hid	ref_entity_found_in_expr_hid_csbvh	e					References a entity instance @ found in an Expression hid at line @
vhe	csb	hid	ref_unit_found_in_expr_hid_csbch	e					References a unit instance @ found in an Expression hid at line @
vhe	csb	hid	hid_reference_not_found_csbvh	e					@ reference not found at line @
vhe	csb	hid	mifc_in_hid_not_exist_csbvh	e					Module instance @ in hid does not exist at line @
vhe	csb	hid	entity_instance_in_hid_not_exist_csbvh	e					Entity instance @ in hid does not exist at line @
vhe	csb	hid	unit_instance_in_hid_not_exist_csbvh	e					Unit instance @ in hid does not exist at line @
vhe	csb	hid	mod_found_in_path_in_dsgn_csbvh	e					Module @ found in path

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									@ in the design at line @
vhe	csb	hid	enity_found_in_path_in_dsgn_csbvh	e					Entity @ found in path @ in the design at line @
vhe	csb	hid	unit_found_in_path_in_dsgn_csbvh	e					Unit @ found in path @ in the design at line @
vhe	csb	hid	hierarchical_id_path_contains_func_csb	e					Hierarchical ID @ path contains a function at line @
vhe	csb	init	assn_mem_in_init_blk_csbvh	e					Assign memory in initial block at line @
vhe	csb	inst	inst_duplicate_mod_name_csbvh	e					Duplicate port @ in the port list for module @ at line @
vhe	csb	inst	inst_duplicate_entity_name_csbvh	e					Duplicate port @ in the port list for entity @ at line @
vhe	csb	inst	inst_duplicate_unit_name_csbvh	e					Duplicate port @ in the port list for unit @ at line @
vhe	csb	inst	ill_mod_inst_name_csbvh	e					Illegal module instance @ at line @
vhe	csb	inst	ill_entity_inst_name_csbvh	e					Illegal entity instance @ at line @
vhe	csb	inst	ill_unit_inst_name_csbvh	e					Illegal unit instance @ at line @
vhe	csb	inst	inst_name_defined_mod_csbvh	e					Instance name @ already defined in this module at line @
vhe	csb	inst	inst_name_defined_ent_csbvh	e					Instance name @ already defined in this entity at line @
vhe	csb	inst	inst_name_defined_unit_csbvh	e					Instance name @ already defined in this unit at line @
vhe	csb	inst	inst_too_many_bits_csbvh	e					Too many bits for port @ of instance array @, formal @, actual @ at line @
vhe	csb	inst	inst_port_not_connected_var_csbvh	e					Port 'port' of instance array 'array' is not connected to variable at line @
vhe	csb	inst	inst_insufficient_bits_csbvh	e					Insufficient bits for port 'port' of instance array 'array ', formal number, actual number at line @
vhe	csb	inst	inst_mod_name_not_defined_csbvh	e					Module name not defined at line @
vhe	csb	inst	inst_ent_name_not_defined_csbvh	e					Entity name not defined at line @
vhe	csb	inst	inst_unit_name_not_defined_csbvh	e					Unit name not defined at line @
vhe	csb	inst	many_mod_inst_param_assign_csbvh	e					Too many module instance parameter assignments (number > rrumber) at line @
vhe	csb	inst	many_entity_inst_param_assign_csbvh	e					Too many entity instance parameter assignments (number > rrumber) at line @
vhe	csb	inst	many_unit_inst_param_assign_csbvh	e					Too many unit instance parameter assignments (number > rrumber) at line @
vhe	csb	inst	complexexpr_cannot_mapped_inout_port_csbvh	e					Complex Expression @ cannot be mapped to inout port @ at line @
vhe	csb	inst	complexexpr_cannot_mapped_unknown_port_csbvh	e					Complex Expression @ cannot be mapped to unknown type port @ at line @
vhe	csb	inst	netdecl_contains_ill_prts_csbvh	e					Net Declaration [@: @] contains an illegal part select at line @
vhe	csb	inst	regdecl_contains_ill_prts_csbvh	e					Reg Declaration [@ : @] contains an illegal part select at line @
vhe	csb	inst	complex_expr_inst_parent_module_csbvh	e					Complex actual Expression associated with port @ of module @ instantiated in parent module at line @
vhe	csb	inst	complex_expr_inst_entity_parent_module_csbvh	e					Complex actual Expression associated with port @ of entity @ instantiated in parent module at line @
vhe	csb	inst	complex_expr_inst_unit_parent_module_csbvh	e					Complex actual Expression associated with port @ of unit @ instantiated in parent

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									module at line @
vhe	csb	inst	inst_mod_output_port_width_csbvh	e					Mod @ Output port @ width mismatch, actual-width (port-width) at line @
vhe	csb	inst	inst_entity_output_port_width_csbvh	e					Entity @ Output port @ width mismatch, actual-width (port-width) at line @
vhe	csb	inst	inst_unit_output_port_width_csbvh	e					Unit @ Output port @ width mismatch, actual-width (port-width) at line @
vhe	csb	inst	inst_mod_input_port_width_csbvh	e					Mod @ Input port @ width mismatch, actual-width (port-width) at line @
vhe	csb	inst	inst_entity_input_port_width_csbvh	e					Entity @ Input port @ width mismatch, actual-width (port-width) at line @
vhe	csb	inst	inst_unit_input_port_width_csbvh	e					Unit @ Input port @ width mismatch, actual-width (port-width) at line @
vhe	csb	inst	inst_mod_not_define_csbvh	e					Module not defined at line @
vhe	csb	inst	inst_entity_not_define_csbvh	e					Entity not defined at line @
vhe	csb	inst	inst_unit_not_define_csbvh	e					Unit not defined at line @
vhe	csb	inst	mifc_port_actual_formal_width_mismatch_csbvh	w					Module @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vhe	csb	inst	ent_port_actual_formal_width_mismatch_csbvh	w					Entity @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vhe	csb	inst	unit_port_actual_formal_width_mismatch_csbvh	w					Unit @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vhe	csb	inst	inst_differs_in_case_from_mod_csbvh	e					Instance name @ differs in case from module name @ at line @
vhe	csb	inst	inst_differs_in_case_from_ent_csbvh	e					Instance name @ differs in case from entity name @ at line @
vhe	csb	inst	inst_differs_in_case_from_sig_csbvh	e					Instance name @ differs in case from signal name @ at line @
vhe	csb	loop	undet_init_value_loop_csbvh	e					Unable to determine init value for loop at line @
vhe	csb	loop	undet_limit_loop_csbvh	e					Unable to determine limit for loop at line @
vhe	csb	loop	loop_bounds_calculated_int_csbvh	w					Loop bounds are calculated to be integer @, check that this is correct at line @
vhe	csb	loop	expr_lhs_contains_var_bit_select_csbvh	w					Expression in lhs of assignment contains a variable bit select at line @
vhe	csb	loop	loop_bounds_not_const_csb	w					Loop bounds are non-constant at line @
vhe	csb	loop	loop_ctrl_init_expr_not_const_csbvh	w					Non-constant loop bound. Loop control variable initialization Expression is not a constant Expression at line @
vhe	csb	loop	loop_term_expr_not_const_csbve	w					Non-constant loop bound. loop terminating Expression could not be evaluated to a constant at line @
vhe	csb	loop	init_expr_reset_by_var_csbvh	e					Non-constant loop bound. initializing Expression reset by variable at line @
vhe	csb	loop	loop_ctrl_var_1_bit_wide_csbvh	w					The loop control variable @ is one bit wide. Check the loop control variable Declaration. at line @
vhe	csb	mdb	bad_mdb_net_csbvh	e					Bad multi-driven Net @ at line @
vhe	csb	mdb	bad_mdb_port_csbvh	e					Bad multi-driven Port @ at line @
vhe	csb	mdb	bad_mdb_signal_csbvh	e					Bad multi-driven Signal @ at line @
vhe	csb	mdb	unsupp_comp_mdb_net_csbvh	e	?				Unsupported component

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									type @ driving in multi-driven Net name at line @
vhe	csb	mdb	unsupp_comp_mdb_port_csbvh	e	?				Unsupported component type @ driving in multi-driven Port name at line @
vhe	csb	mdb	unsupp_comp_mdb_signal_csbvh	e	?				Unsupported component type @ driving in multi-driven Signal name at line @
vhe	csb	mdb	unsupp_comp_drive_mdb_csbvh	e	?				Unsupported component type @ driving multi-driven Net natne at line @
vhe	csb	mdb	unsupp_comp_drive_mdb_port_csbvh	e	?				Unsupported component type @ driving multi-driven Port natne at line @
vhe	csb	mdb	unsupp_comp_drive_mdb_signal_csbvh	e	?				Unsupported component type @ driving multi-driven Signal natne at line @
vhe	csb	mdb	mdb_net_driven_by_trns_csbvh	e					Multiply driven Net driven by transistor primitive type @ at line @
vhe	csb	mdb	mdb_port_driven_by_trns_csbvh	e					Multiply driven Port driven by transistor primitive type @ at line @
vhe	csb	mdb	mdb_sig_driven_by_trns_csbvh	e					Multiply driven Signal driven by transistor primitive type @ at line @
vhe	csb	mdb	mdb_unsupp_comp_drvs_net_csbvh	e					Unsupported component type driving Net drives Net connected to multi-driven Net at line @
vhe	csb	mdb	mdb_unsupp_comp_drvs_port_csbvh	e					Unsupported component type driving Port drives Port connected to multi-driven Port at line @
vhe	csb	mdb	mdb_unsupp_comp_drvs_sig_csbvh	e					Unsupported component type driving Signal drives Signal connected to multi-driven Signal at line @
vhe	csb	mdb	mdb_incompatible_net_drives_multiple_net_csbvh	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Net at line @
vhe	csb	mdb	mdb_incompatible_port_drives_multiple_port_csbvh	e					Incompatible driver driving tandem Port drives Port connected to multi-driven Port at line @
vhe	csb	mdb	mdb_incompatible_sig_drives_multiple_sig_csbvh	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Port at line @
vhe	csb	mdb	mdb_unsupp_LHS_concatenation_csbvh	e					Unsupported LHS concatenation in multi-drive 'device at line @
vhe	csb	mdb	mdb_bus_has_too_many_drivers_csbvh	e					Bus has too many drivers. at line @
vhe	csb	mdb	mdb_always_blk_drive_csbvh	w					Multiple always blocks drive name @ at line @
vhe	csb	mdb	nontri_gate_drives_mdb_net_csbvh	w					non-tri-state gate drives multi-driven Net at line @
vhe	csb	mdb	nontri_gate_drives_mdb_port_csbvh	w					non-tri-state gate drives multi-driven Port at line @
vhe	csb	mdb	nontri_gate_drives_mdb_sig_csbvh	w					non-tri-state gate drives multi-driven Signal at line @
vhe	csb	mem	mem_prts_csv	e					Memories do not support part select specifier at line @
vhe	csb	mem	mem_ref_without_index_csbvh	e					Memory @ referenced without index through hierarchical ID @ at line @
vhe	csb	mem	ill_mem_csbvh	e					Illegal memory @ at line @
vhe	csb	mifc	mifc_not_array_csv	e					Ports may not be an array at line @
vhe	csb	mifc	port_identifier_mifc_cssbvh	e					Port @ at line @
vhe	csb	mifc	mod_output_wire_redecl_reg_csbvh	e					Module @ output port

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									re-declared as type reg after use as implicitly declared wire at line @
vhe	csb	mifc	entity_output_wire_redecl_reg_csbvh	e					Entity @ output port re-declared as type reg after use as implicitly declared wire at line @
vhe	csb	mifc	unit_output_wire_redecl_reg_csbvh	e					Unit @ output port re-declared as type reg after use as implicitly declared wire at line @
vhe	csb	mifc	output_port_is_mem_type_mifc_csbvh	e					Output port @ is memory type at line @
vhe	csb	mifc	mifc_inout_port_is_mem_type_csbvh	e					Inout port @ is memory type at line @
vhe	csb	mifc	mod_output_port_mismatch_actual_witdh_csbvh	w					Module @ output port @ formal to actual width mismatch at line @
vhe	csb	mifc	ent_output_port_mismatch_actual_witdh_csbvh	w					Entity @ output port @ formal to actual width mismatch at line @
vhe	csb	mifc	unit_output_port_mismatch_actual_witdh_csb	w					Unit @ output port @ formal to actual width mismatch at line @
vhe	csb	mifc	port_name_different_in_upper_lower_case_csbvh	e					Port name @ different in upper lower case at line @
vhe	csb	mifc	port_not_def_in_iodecl_csbvh	e					Port @ not defined in ioDeclaration at line @
vhe	csb	mifc	port_not_def_in_portl_csbvh	e					Port @ not defined in port list at line @
vhe	csb	mifc	port_wiredecl_mismatch_csbvh	e					Port @ wireDeclaration mismatch at line @
vhe	csb	mifc	pos_based_null_inst_port_csbvh	e					Position based null instance port at line @
vhe	csb	mifc	last_portdecl_contains_trailcomma_csbvh	e					Last portDeclaration contains a trailing comma at line @
vhe	csb	mins	mins_expr_incompatible_type_csbvh	e					Expression @ has an incompatible argument type @ with the port at line @
vhe	csb	mins	mins_mod_not_exist_csbvh	e					Module @ does not exist at line @
vhe	csb	mins	mins_entity_not_exist_csbvh	e					Entity @ does not exist at line @
vhe	csb	mins	mins_unit_not_exist_csbvh	e					Unit @ does not exist at line @
vhe	csb	mod	dup_declar_name_mod_csv	e					Duplicate Declaration of port @ at line @
vhe	csb	mod	ill_mod_name_csbvh	e					Illegal module @ at line @
vhe	csb	mod	ill_mod_entity_name_csbvh	e					Illegal entity @ at line @
vhe	csb	mod	ill_mod_unit_name_csbvh	e					Illegal unit @ at line @
vhe	csb	mod	mod_mult_decl_string_csbvh	e					Multiple Declarations of string detected in module @ at line @
vhe	csb	mod	mod_entity_mult_decl_string_csbvh	e					Multiple Declarations of string detected in entity @ at line @
vhe	csb	mod	mod_unit_mult_decl_string_csbvh	e					Multiple Declarations of string detected in unit @ at line @
vhe	csb	mod	mod_mult_def_csbvh	e					Module @ defined in multiple places at line @
vhe	csb	mod	mod_ent_mult_def_csbvh	e					Entity @ defined in multiple places at line @
vhe	csb	mod	mod_unit_mult_def_csbvh	e					Unit @ defined in multiple places at line @
vhe	csb	mod	mod_no_module_found_csbvh	e					No modules found at line @
vhe	csb	mod	mod_no_entity_found_csbvh	e					No entity found at line @
vhe	csb	mod	mod_no_unit_found_csbvh	e					No unit found at line @
vhe	csb	mod	failed_find_mod_csbvh	e					Failed to find module @ at line @
vhe	csb	mod	failed_find_entity_csbvh	e					Failed to find entity @ at line @
vhe	csb	mod	failed_find_unit_csbvh	e					Failed to find unit @ at line @
vhe	csb	mod	empty_mod_csbvh	e					Empty module at line @
vhe	csb	mod	empty_ent_csbvh	e					Empty entity at line @
vhe	csb	mod	empty_unit_csbvh	e					Empty unit at line @
vhe	csb	net	net_implicit_wire_redecl_reg_csbvh	e					Implicitly declared as a wire @ re-declared as a reg @. at line @
vhe	csb	net	undecl_net_in_mod_csbvh	e					Undeclared net @ in module @ at line @
vhe	csb	net	undecl_port_in_mod_csbvh	e					Undeclared port @ in module @ at line @
vhe	csb	net	undecl_sig_in_mod_csbvh	e					Undeclared signal @ in

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									module @ at line @
vhe	csb	net	undecl_net_in_ent_csbvh	e					Undeclared net @ in entity @ at line @
vhe	csb	net	undecl_port_in_ent_csbvh	e					Undeclared port @ in entity @ at line @
vhe	csb	net	undecl_sig_in_ent_csbvh	e					Undeclared signal @ in entity @ at line @
vhe	csb	net	undecl_net_in_sig_csbvh	e					Undeclared net @ in signal @ at line @
vhe	csb	net	undecl_port_in_sig_csbvh	e					Undeclared port @ in signal @ at line @
vhe	csb	net	undecl_sig_in_sig_csbvh	e					Undeclared signal @ in signal @ at line @
vhe	csb	net	port_used_prior_to_decl_csbvh	e					Port @ used prior toDeclaration at line @
vhe	csb	net	1bit_with_prts_csbvh	e					1-bit with part select at line @
vhe	csb	netd	ill_decl_vec_csbvh	e					Illegal Declaration of vector @ at line @
vhe	csb	nett	nett_ill_reg_name_csbvh	e					Illegal register @ at line @
vhe	csb	nett	nett_ill_net_name_csbvh	e					Illegal net @ at line @
vhe	csb	nett	nett_ill_port_name_csbvh	e					Illegal port @ at line @
vhe	csb	nett	nett_ill_signal_name_csbvh	e					Illegal signal @ at line @
vhe	csb	nett	net_scalar_vect_nett_csbvh	e					Net declared as both scalar and vector at line @
vhe	csb	nett	port_scalar_vect_nett_csbvh	e					Port declared as both scalar and vector at line @
vhe	csb	nett	signal_scalar_vect_nett_csbvh	e					Signal declared as both scalar and vector at line @
vhe	csb	nett	hot_mux_not_use_bus_connection_net_csbvh	e					One hot mux can not be used for bus connection between modules Net @ at line @
vhe	csb	nett	hot_mux_not_use_bus_connection_port_csbvh	e					One hot mux can not be used for bus connection between modules Port @ at line @
vhe	csb	nett	hot_mux_not_use_bus_connection_sig_csbvh	e					One hot mux can not be used for bus connection between modules Signal @ at line @
vhe	csb	num	not_allowed_width0_num_csbvh	e					Width 0 not allowed for sized number at line @
vhe	csb	num	real_num_not_allowed_csbvh	e					Real numbers not allowed at line @
vhe	csb	num	found_x_z_in_num_literal_csbvh	e					Found x and/or z value in number literal at line @
vhe	csb	num	too_many_digits_in_sized_num_csbvh	w					Number of digits exceeds the width in a sized number at line @
vhe	csb	num	divide_by_zero_num_csbvh	e					Divide by zero at line @
vhe	csb	num	child_mod_inst_parent_mod_csbvh	e					Child module @ instantiates parent module @ at line @
vhe	csb	num	child_ent_inst_parent_ent_csbvh	e					Child entity @ instantiates entity module @ at line @
vhe	csb	num	child_sig_inst_parent_sig_csbvh	e					Child signal @ instantiates signal module @ at line @
vhe	csb	num	int_decl_incorrect_csbvh	e					Integer Declaration incorrect at line @
vhe	csb	num	int_var_indexed_csbvh	e					Integer variable inedexed at line @
vhe	csb	parm	ill_parm_identifier_cssbvh	e					Illegal parameter @ at line @
vhe	csb	parm	value_of_parm_OS_platform_dependent_csbvh	w					Parameter select width > 32. The value is OS and platform dependent at line @
vhe	csb	parm	parm_redefined_csbvh	w					Parameter @ redefined at line @
vhe	csb	port	ill_formal_port_name_csbvh	e					Illegal formal port @ at line @
vhe	csb	pp	text_redefined_replaced_csbvh	w					Text macro redefined and replaced @. Previous definition filename, line number @ New definition filename, line number @ at line @
vhe	csb	pp	endif_or_else_without_ifdef_csbvh	e					Endif-or-else-without ifdef at line @
vhe	csb	prim	z_in_prim_inst_csbvh	e					z in primitive instantiation at line @
vhe	csb	prts	type_prts_csv	e					Type @ does not support part select specifier at

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									line @
vhe	csb	prts	prts_out_of_range_csbvh	e					Parameter @[@ : @]part select is out of range at line @
vhe	csb	prts	ill_prts_inst_array_csbvh	e					Illegal value for part select of instance array 'name' at line @
vhe	csb	prts	const_prts_contains_non_const_selector_csbvh	e					Constant part select @ contains a non-constant selector @ at line @
vhe	csb	prts	bus_index_prts_for_var_out_of_range_csbvh	e					Bus index @ integer of part select [@:@] for variable @ out of range at line @
vhe	csb	prts	bus_prts_for_var_out_of_range_csbvh	e					Bus part select [@:@] for variable @ out of range at line @
vhe	csb	prts	bus_prts_index_out_of_name_for_var_csbvh	e					Bus part select [@:@] index @ out of range for variable @ at line @
vhe	csb	prts	ill_token_in_prts_csbvh	e					Illegal token in part select @ at line @
vhe	csb	prts	incomplete_prts_specification_csbvh	e					Incomplete part select specification @ at line @
vhe	csb	prts	ill_index_in_prts_csbvh	e					Illegal index in part select @ at line @
vhe	csb	prts	negative_index_in_prts_not_allowed_csbvh	e					Negative index in part select @ not allowed at line @
vhe	csb	prts	prts_index_order_reversed_csbvh	e					Part select index order reversed [@ : @] [@ : @] should be [@ : @] at line @
vhe	csb	prts	index_vec_over_max_size_csbvh	w					Vector index @ exceeds the size of the vector. Index truncated at line @
vhe	csb	prts	x_or_z_in_vec_bit_select_index_csbvh	e					x or z in vector bit select index at line @
vhe	csb	simr	inefficient_op_not_a_power_of_2_csbvh	e					Division/modulus by a number not a power of 2. Inefficient simulation operation. at line @
vhe	csb	simr	simr_multiple_init_blk_force_csbvh	w					Multiple initial blocks force @. Unpredictable simulation result at line @
vhe	csb	snsl	incomplete_snsl_csbvh	w					Incomplete sensitivity list. @ is not in the sensitivity list. at line @
vhe	csb	snsl	edge_sns_process_contains_data_pin_snsl_csbvh	e					Edge sensitive process contains a data pin @ in the sensitivity list at line @
vhe	csb	snsl	unsupp_expr_in_snsl_csbvh	w					Unsupported Expression type @ in sensitivity list ' at line @
vhe	csb	snsl	partial_bus_decl_width_csbvh	e	?				partial bus @ declared with width @ width @ at line @
vhe	csb	snsl	contains_inst_name_csbvh	e					Contains instance name @ at line @
vhe	csb	stmt	null_not_allowed_stmt_csbvh	e					Null statement is not allowed here at line @
vhe	csb	stmt	stmt_ill_accept_only_net_reg_mem_csbvh	e					Illegal type @ can only accept net, reg, memory at line @
vhe	csb	stmt	stmt_ill_accept_only_port_reg_mem_csbvh	e					Illegal type @ can only accept port, reg, memory at line @
vhe	csb	stmt	stmt_ill_accept_only_signal_reg_mem_csbvh	e					Illegal type @ can only accept signal, reg, memory at line @
vhe	csb	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_csbvh	e					Arithmetic operator RHS has one less bit than the LHS at line @
vhe	csb	stmt	ar_op_unequal_lhs_rhs_csbvh	e					Arithmetic operator unequal width LHS and RHS at line @
vhe	csb	stmt	ar_op_unequal_var_on_rhs_csb	e					Arithmetic operator unequal width variables @ on RHS at line @
vhe	csb	stmt	empty_stmt_csb	e					Empty-statement at line @
vhe	csb	syst	return_var_of_user_used_as_rhs_csbvh	w					Return variable of user system task is used as a RHS variable at line @
vhe	csb	task	ask_var_not_decl_csbvh	e					Variable @ used but not declared at line @
vhe	csb	task	too_many_arg_to_task_csbve	e					Too many arguments passed to task @ at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	csb	task	too_few_arg_to_task_csbvh	e					Too few arguments passed to task @ at line @
vhe	csb	tri	instance_not_tri_state_device_csbvh	e					Instance name is not a tri-state device at line @
vhe	csb	tri	unsupp_gate_type_tristate_csbvh	e					Unsupported gate type @ used for tristate at line @
vhe	csb	tri	tri_not_desgn_gate_contention_csbvh	e					Tristate not designed correctly gate @ can cause contention at line @
vhe	csb	tri	unsupp_type_instance_tri_csbvh	e					Unsupported type instance type used for tristate @ at line @
vhe	csb	tri	incorrect_cont_assign_stmt_tri_gate_csbvh	e					Incorrect continuous assign statement for tristate gate @ at line @
vhe	csb	tri	const_assign_to_multidriven_net_csbvh	e					Constant (constiznt) assigned to multi-driven Net @ at line @
vhe	csb	tri	const_assign_to_multidriven_port_csbvh	e					Constant (constiznt) assigned to multi-driven Port @ at line @
vhe	csb	tri	const_assign_to_multidriven_signal_csbvh	e					Constant (constiznt) assigned to multi-driven Signal @ at line @
vhe	csb	tri	unsupp_expr_for_tri_csbvh	e					Unsupported Expression type @ for tristate at line @
vhe	csc	assn	x_in_rhs_of_assihnment_cscvh	e					x in rhs of assignment at line @
vhe	csc	assn	z_in_rhs_of_assn_default_csi_cscvh	e					x in rhs of assignement in defaultCase item at line @
vhe	csc	assn	z_in_rhs_of_assn_cscvh	e					z in rhs of assignement at line @
vhe	csc	assn	unequal_length_lhs_rhs_cscvh	e					Unequal length LHS and RHS at line @
vhe	csc	assn	unequal_length_lhs_rhs_off_one_bit_cscvh	e					Unequal length LHS and RHS off by one bit at line @
vhe	csc	ccd	ccd_cdir_must_be_cst_expr_cscvh	e				x	CSL directive size must be constant Expression at line @
vhe	csc	clk	clk_name_not_found_cdir_cscvh	e				x	Clock name not found in cslc directive at line @
vhe	csc	clk	expr_sunj_to_different_clk_phases_cscvh	e					Expression subject to different clock phases at line @
vhe	csc	cond	if_case_cond_expr_cscve	e					If/case conditional expression @ syntax error at line @
vhe	csc	cond	if_no_else_cscve	e					If no else at line @
vhe	csc	csi	xcsi_not_in_casex_cscvh	e					xCase item not in casex at line @
vhe	csc	csi	noncstn_rep_in_conc_cscvh	e					Non-constant repeator in concatenation at line @
vhe	csc	csi	cond_expr_in_csi_cscvh	e					Conditional Expression inCase item at line @
vhe	csc	csi	full_case_has_default_cscvh	e					Full case has default at line @
vhe	csc	css	sns_pragma_full_case_cscvh	e					Assume a full case, missing default or synopsys pragma full case. at line @
vhe	csc	decl	decl_array_over_max_size_cscvh	e					Array @ exceeds maximum size limit at line @
vhe	csc	dely	x_or_z_in_dely_cscvh	e					x or z in delay at line @
vhe	csc	dmsn	mem_prts_index_out_of_range_for_mem_cscvh	e					Memory part select [@:@] index @ out range for memory @ at line @
vhe	csc	dmsn	dime_select_for_mem_missing_cscvh	e					Select for memory @ missing at line @
vhe	csc	dmsn	dime_index_out_of_bounds_for_mem_cscvh	e					Index <index> out of bounds for memory @. Range [@: @] at line @
vhe	csc	dmsn	dime_prts_out_of_bounds_for_net_cscvh	e					Part select [@ : @] out of bounds for net @. Range [@ : @] at line @
vhe	csc	dmsn	dime_prts_out_of_bounds_for_port_cscvh	e					Part select [@ : @] out of bounds for port @. Range [@ : @] at line @
vhe	csc	dmsn	dime_prts_out_of_bounds_for_sig_cscvh	e					Part select [@ : @] out of bounds for signal @. Range [@ : @] at line @
vhe	csc	dmsn	dime_prts_reg_cscvh	e					Part select [@ : @] reg @. Range [@ : @] at line @

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vhe	csc	drvc	incompatible_drvc_for_net_cscvh	e					Incompatible drivers for Net @ at line @
vhe	csc	drvc	incompatible_drvc_for_port_cscvh	e					Incompatible drivers for Port @ at line @
vhe	csc	drvc	incompatible_drvc_for_sig_cscvh	e					Incompatible drivers for Signal @ at line @
vhe	csc	drvc	drvc_multiple_drive_net_partially_overlap_cscvh	e					Multiple drive Net partially overlap at line @
vhe	csc	drvc	drvc_multiple_drive_port_partially_overlap_cscvh	e					Multiple drive Port partially overlap at line @
vhe	csc	drvc	drvc_multiple_drive_sig_partially_overlap_cscvh	e					Multiple drive Signal partially overlap at line @
vhe	csc	dsgn	dsgn_top_mod_cannot_id_cscvh	e					Top module @ cannot be identified at line @
vhe	csc	dsgn	dsgn_top_entity_cannot_id_cscvh	e					Top entity @ cannot be identified at line @
vhe	csc	dsgn	dsgn_top_unit_cannot_id_cscvh	e					Top unit @ cannot be identified at line @
vhe	csc	dsgn	unit_dsgn_cycle_not_spanning_tree_cscvh	e					Unit design hierarchy contains a cycle. Hierarchy is not a spanning tree. at line @
vhe	csc	expr	expr_prts_indices_1bit_var_cscvh	e					Part select indices 1-bit variable at line @
vhe	csc	expr	expr_prts_must_be_cst_expr_cscvh	e					Part select specifier Expression must be constant Expression at line @
vhe	csc	expr	not_const_expr_cscvh	e					Repetition multiplier in concatenation is not a constant Expression at line @
vhe	csc	expr	ill_bit_select_expr_cscvh	e					Illegal bit select expression @ at line @
vhe	csc	expr	repetition_multiplier_in_conc_not_const_expr_cscvh	w					Repetition multiplier in concatenation is not a constant Expression at line @
vhe	csc	expr	int_operand_not_1_bit_cscvh	w					Logic operator has integer operands instead of 1-bit operands at line @
vhe	csc	expr	unsupp_expr_cscvh	w					Unsupported Expression type @ at line @
vhe	csc	expr	unsupp_operator_cscvh	w					Unsupported operator type @ at line @
vhe	csc	expr	use_of_sg_bit_const_cscvh	w					Use of single bit constant at line @
vhe	csc	expr	unary_op_in_comparison_cscvh	e					Unary op used in comparison at line @
vhe	csc	expr	x_or_z_in_cond_expr_cscvh	e					x or z in conditional expression at line @
vhe	csc	expr	zero_in_rep_in_conc_cscvh	e					Zero repeator in concatenation at line @
vhe	csc	expr	expr_in_mod_port_dir_cscvh	e					Expression @ in module port dir at line @
vhe	csc	expr	expr_in_ent_port_dir_cscvh	e					Expression @ in entity port dir at line @
vhe	csc	expr	expr_in_sig_port_dir_cscvh	e					Expression @ in unit port dir at line @
vhe	csc	expr	expr_in_inst_cscvh	e					Expression @ in inst i@ at line @
vhe	csc	expr	expr_operator_operands_unequal_lenght_cscvh	e					Expression operator @ operands @ unequal length at line @
vhe	csc	file	cannot_open_filter_specification_file_cscvh	e					Cannot open filter specification file @ at line @
vhe	csc	file	filter_specification_file_missing_cscvh	e					Filter specification file name @ is missing at line @
vhe	csc	file	mismatch_mod_file_name_cscvh	e					Mismatch between module name @ and file name @ at line @
vhe	csc	file	mismatch_ent_file_name_cscvh	e					Mismatch between entity name @ and file name @ at line @
vhe	csc	file	mismatch_sig_file_name_cscvh	e					Mismatch between signal name @ and file name @ at line @
vhe	csc	func	port_not_output_func_cscvh	e					Port @ direction cannot be output at line @
vhe	csc	func	too_many_arg_to_func_cscvh	e					Too many arguments passed to function @ at line @
vhe	csc	func	too_few_arg_to_func_cscvh	e					Too few arguments passed to function @ at line @
vhe	csc	func	funct_expr_cannot_expnaded_cscvh	e					Function expression @ cannot be expanded at

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									line @
vhe	csc	func	funct_not_used_in_expr_cscvh	w					Function @ is not being used in an Expression at line @
vhe	csc	func	func_decl_cscvh	w					Function Declaration @ already declared as another type at line @
vhe	csc	func	undefined_func_cscvh	e					Undefined function @ at line @
vhe	csc	hid	cannot_locate_hier_id_hid_cscvh	e					Can't locate hierarchical identifier @ at line @
vhe	csc	hid	ref_minst_found_in_expr_hid_cscvh	e					References a module instance @ found in an Expression hid at line @
vhe	csc	hid	ref_entity_found_in_expr_hid_cscvh	e					References a entity instance @ found in an Expression hid at line @
vhe	csc	hid	ref_unit_found_in_expr_hid_cscvh	e					References a unit instance @ found in an Expression hid at line @
vhe	csc	hid	hid_reference_not_found_cscvh	e					@ reference not found at line @
vhe	csc	hid	mifc_in_hid_not_exist_cscvh	e					Module instance @ in hid does not exist at line @
vhe	csc	hid	entity_instance_in_hid_not_exist_cscvh	e					Entity instance @ in hid does not exist at line @
vhe	csc	hid	unit_instance_in_hid_not_exist_cscvh	e					Unit instance @ in hid does not exist at line @
vhe	csc	hid	mod_found_in_path_in_dsgn_cscvh	e					Module @ found in path @ in the design at line @
vhe	csc	hid	enity_found_in_path_in_dsgn_cscvh	e					Entity @ found in path @ in the design at line @
vhe	csc	hid	unit_found_in_path_in_dsgn_cscvh	e					Unit @ found in path @ in the design at line @
vhe	csc	hid	hierarchical_id_path_contains_func_csc	e					Hierarchical ID @ path contains a function at line @
vhe	csc	init	assn_mem_in_init_blk_cscvh	e					Assign memory in initial block at line @
vhe	csc	inst	inst_duplicate_mod_name_cscvh	e					Duplicate port @ in the port list for module @ at line @
vhe	csc	inst	inst_duplicate_entity_name_cscvh	e					Duplicate port @ in the port list for entity @ at line @
vhe	csc	inst	inst_duplicate_unit_name_cscvh	e					Duplicate port @ in the port list for unit @ at line @
vhe	csc	inst	ill_mod_inst_name_cscvh	e					Illegal module instance @ at line @
vhe	csc	inst	ill_entity_inst_name_cscvh	e					Illegal entity instance @ at line @
vhe	csc	inst	ill_unit_inst_name_cscvh	e					Illegal unit instance @ at line @
vhe	csc	inst	inst_name_defined_mod_cscvh	e					Instance name @ already defined in this module at line @
vhe	csc	inst	inst_name_defined_ent_cscvh	e					Instance name @ already defined in this entity at line @
vhe	csc	inst	inst_name_defined_unit_cscvh	e					Instance name @ already defined in this unit at line @
vhe	csc	inst	inst_too_many_bits_cscvh	e					Too many bits for port @ of instance array @, formal @, actual @ at line @
vhe	csc	inst	inst_port_not_connected_var_cscvh	e					Port 'port' of instance array 'array' is not connected to variable at line @
vhe	csc	inst	inst_insufficient_bits_cscvh	e					Insufficient bits for port 'port' of instance array 'array ', formal number, actual number at line @
vhe	csc	inst	inst_mod_name_not_defined_cscvh	e					Module name not defined at line @
vhe	csc	inst	inst_ent_name_not_defined_cscvh	e					Entity name not defined at line @
vhe	csc	inst	inst_unit_name_not_defined_cscvh	e					Unit name not defined at line @
vhe	csc	inst	many_mod_inst_param_assign_cscvh	e					Too many module instance parameter assignments (number > rrumber) at line @
vhe	csc	inst	many_entity_inst_param_assign_cscvh	e					Too many entity instance parameter assignments (number > rrumber) at line @
vhe	csc	inst	many_unit_inst_param_assign_cscvh	e					Too many unit instance

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									parameter assignments (number > rrumber) at line @
vhe	csc	inst	complexexpr_cannot_mapped_inout_port_cscvh	e					Complex Expression @ cannot be mapped to inout port @ at line @
vhe	csc	inst	complexexpr_cannot_mapped_unknown_port_cscvh	e					Complex Expression @ cannot be mapped to unknown type port @ at line @
vhe	csc	inst	netdecl_contains_ill_prts_cscvh	e					Net Declaration [@: @] contains an illegal part select at line @
vhe	csc	inst	regdecl_contains_ill_prts_cscvh	e					Reg Declaration [@ : @] contains an illegal part select at line @
vhe	csc	inst	complex_expr_inst_parent_module_cscvh	e					Complex actual Expression associated with port @ of module @ instantiated in parent module at line @
vhe	csc	inst	complex_expr_inst_entity_parent_module_cscvh	e					Complex actual Expression associated with port @ of entity @ instantiated in parent module at line @
vhe	csc	inst	complex_expr_inst_unit_parent_module_cscvh	e					Complex actual Expression associated with port @ of unit @ instantiated in parent module at line @
vhe	csc	inst	inst_mod_output_port_width_cscvh	e					Mod @ Output port @ width mismatch, actual-width (port-width) at line @
vhe	csc	inst	inst_entity_output_port_width_cscvh	e					Entity @ Output port @ width mismatch, actual-width (port-width) at line @
vhe	csc	inst	inst_unit_output_port_width_cscvh	e					Unit @ Output port @ width mismatch, actual-width (port-width) at line @
vhe	csc	inst	inst_mod_input_port_width_cscvh	e					Mod @ Input port @ width mismatch, actual-width (port-width) at line @
vhe	csc	inst	inst_entity_input_port_width_cscvh	e					Entity @ Input port @ width mismatch, actual-width (port-width) at line @
vhe	csc	inst	inst_unit_input_port_width_cscvh	e					Unit @ Input port @ width mismatch, actual-width (port-width) at line @
vhe	csc	inst	inst_mod_not_define_cscvh	e					Module not defined at line @
vhe	csc	inst	inst_entity_not_define_cscvh	e					Entity not defined at line @
vhe	csc	inst	inst_unit_not_define_cscvh	e					Unit not defined at line @
vhe	csc	inst	ent_port_actual_formal_width_mismatch_cscvh	w					Entity @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vhe	csc	inst	unit_port_actual_formal_width_mismatch_cscvh	w					Unit @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vhe	csc	inst	inst_differs_in_case_from_mod_cscvh	e					Instance name @ differs in case from module name @ at line @
vhe	csc	inst	inst_differs_in_case_from_ent_cscvh	e					Instance name @ differs in case from entity name @ at line @
vhe	csc	inst	inst_differs_in_case_from_sig_cscvh	e					Instance name @ differs in case from signal name @ at line @
vhe	csc	loop	undet_init_value_loop_cscvh	e					Unable to determine init value for loop at line @
vhe	csc	loop	undet_limit_loop_cscvh	e					Unable to determine limit for loop at line @
vhe	csc	loop	loop_bounds_calculated_int_cscvh	w					Loop bounds are calculated to be integer @, check that this is correct at line @
vhe	csc	loop	expr_lhs_contains_var_bit_select_cscvh	w					Expression in lhs of assignment contains a variable bit select at line @
vhe	csc	loop	loop_bounds_not_const_csc	w					Loop bounds are non-constant at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	csc	loop	loop_ctrl_init_expr_not_const_cscvh	w					Non-constant loop bound. Loop control variable initialization Expression is not a constant Expression at line @
vhe	csc	loop	loop_term_expr_not_const_cscve	w					Non-constant loop bound. loop terminating Expression could not be evaluated to a constant at line @
vhe	csc	loop	init_expr_reset_by_var_cscvh	e					Non-constant loop bound. initializing Expression reset by variable at line @
vhe	csc	loop	loop_ctrl_var_1_bit_wide_cscvh	w					The loop control variable @ is one bit wide. Check the loop control variable Declaration. at line @
vhe	csc	mdb	bad_mdb_net_cscvh	e					Bad multi-driven Net @ at line @
vhe	csc	mdb	bad_mdb_port_cscvh	e					Bad multi-driven Port @ at line @
vhe	csc	mdb	bad_mdb_signal_cscvh	e					Bad multi-driven Signal @ at line @
vhe	csc	mdb	unsupp_comp_mdb_net_cscvh	e	?				Unsupported component type @ driving in multi-driven Net name at line @
vhe	csc	mdb	unsupp_comp_mdb_port_cscvh	e	?				Unsupported component type @ driving in multi-driven Port name at line @
vhe	csc	mdb	unsupp_comp_mdb_signal_cscvh	e	?				Unsupported component type @ driving in multi-driven Signal name at line @
vhe	csc	mdb	unsupp_comp_drive_mdb_cscvh	e	?				Unsupported component type @ driving multi-driven Net natne at line @
vhe	csc	mdb	unsupp_comp_drive_mdb_port_cscvh	e	?				Unsupported component type @ driving multi-driven Port natne at line @
vhe	csc	mdb	unsupp_comp_drive_mdb_signal_cscvh	e	?				Unsupported component type @ driving multi-driven Signal natne at line @
vhe	csc	mdb	mdb_net_driven_by_trns_cscvh	e					Multiply driven Net driven by transistor primitive type @ at line @
vhe	csc	mdb	mdb_port_driven_by_trns_cscvh	e					Multiply driven Port driven by transistor primitive type @ at line @
vhe	csc	mdb	mdb_sig_driven_by_trns_cscvh	e					Multiply driven Signal driven by transistor primitive type @ at line @
vhe	csc	mdb	mdb_unsupp_comp_drvs_net_cscvh	e					Unsupported component type driving Net drives Net connected to multi-driven Net at line @
vhe	csc	mdb	mdb_unsupp_comp_drvs_port_cscvh	e					Unsupported component type driving Port drives Port connected to multi-driven Port at line @
vhe	csc	mdb	mdb_unsupp_comp_drvs_sig_cscvh	e					Unsupported component type driving Signal drives Signal connected to multi-driven Signal at line @
vhe	csc	mdb	mdb_incompatible_net_drives_multiple_net_cscvh	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Net at line @
vhe	csc	mdb	mdb_incompatible_port_drives_multiple_port_cscvh	e					Incompatible driver driving tandem Port drives Port connected to multi-driven Port at line @
vhe	csc	mdb	mdb_incompatible_sig_drives_multiple_sig_cscvh	e					Incompatible driver driving tandem Net drives Net connected to multi-driven Port at line @
vhe	csc	mdb	mdb_unsupp_LHS_concatenation_cscvh	e					Unsupported LHS concatenation in multi-drive 'device at line

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									@
vhe	csc	mdb	mdb_bus_has_too_many_drivers_cscvh	e					Bus has too many drivers. at line @
vhe	csc	mdb	mdb_always_blk_drive_cscvh	w					Multiple always blocks drive name @ at line @
vhe	csc	mdb	nontri_gate_drives_mdb_net_cscvh	w					non-tri-state gate drives multi-driven Net at line @
vhe	csc	mdb	nontri_gate_drives_mdb_port_cscvh	w					non-tri-state gate drives multi-driven Port at line @
vhe	csc	mdb	nontri_gate_drives_mdb_sig_cscvh	w					non-tri-state gate drives multi-driven Signal at line @
vhe	csc	mem	mem_prts_csvh	e					Memories do not support part select specifier at line @
vhe	csc	mem	mem_ref_without_index_cscvh	e					Memory @ referenced without index through hierarchical ID @ at line @
vhe	csc	mem	ill_mem_cscvh	e					Illegal memory @ at line @
vhe	csc	mifc	mifc_not_array_csvh	e					Ports may not be an array at line @
vhe	csc	mifc	port_identifier_mifc_cscvh	e					Port @ at line @
vhe	csc	mifc	mod_output_wire_redecl_reg_cscvh	e					Module @ output port re-declared as type reg after use as implicitly declared wire at line @
vhe	csc	mifc	entity_output_wire_redecl_reg_cscvh	e					Entity @ output port re-declared as type reg after use as implicitly declared wire at line @
vhe	csc	mifc	unit_output_wire_redecl_reg_cscvh	e					Unit @ output port re-declared as type reg after use as implicitly declared wire at line @
vhe	csc	mifc	output_port_is_mem_type_mifc_cscvh	e					Output port @ is memory type at line @
vhe	csc	mifc	mifc_inout_port_is_mem_type_cscvh	e					Inout port @ is memory type at line @
vhe	csc	mifc	mod_output_port_mismatch_actual_witdh_cscvh	w					Module @ output port @ formal to actual width mismatch at line @
vhe	csc	mifc	ent_output_port_mismatch_actual_witdh_cscvh	w					Entity @ output port @ formal to actual width mismatch at line @
vhe	csc	mifc	unit_output_port_mismatch_actual_witdh_csc	w					Unit @ output port @ formal to actual width mismatch at line @
vhe	csc	mifc	port_name_different_in_upper_lower_case_cscvh	e					Port name @ different in upper lower case at line @
vhe	csc	mifc	port_not_def_in_iodecl_cscvh	e					Port @ not defined in ioDeclaration at line @
vhe	csc	mifc	port_not_def_in_portl_cscvh	e					Port @ not defined in port list at line @
vhe	csc	mifc	port_wiredecl_mismatch_cscvh	e					Port @ wireDeclaration mismatch at line @
vhe	csc	mifc	pos_based_null_inst_port_cscvh	e					Position based null instance port at line @
vhe	csc	mifc	last_portdecl_contains_trailcomma_cscvh	e					Last portDeclaration contains a trailing comma at line @
vhe	csc	mins	mins_expr_incompatible_type_cscvh	e					Expression @ has an incompatible argument type @ with the port at line @
vhe	csc	mins	mins_mod_not_exist_cscvh	e					Module @ does not exist at line @
vhe	csc	mins	mins_entity_not_exist_cscvh	e					Entity @ does not exist at line @
vhe	csc	mins	mins_unit_not_exist_cscvh	e					Unit @ does not exist at line @
vhe	csc	mod	dup_declar_name_mod_csvh	e					Duplicate Declaration of port @ at line @
vhe	csc	mod	ill_mod_name_cscvh	e					Illegal module @ at line @
vhe	csc	mod	ill_mod_entity_name_cscvh	e					Illegal entity @ at line @
vhe	csc	mod	ill_mod_unit_name_cscvh	e					Illegal unit @ at line @
vhe	csc	mod	mod_mult_decl_string_cscvh	e					Multiple Declarations of string detected in module @ at line @
vhe	csc	mod	mod_entity_mult_decl_string_cscvh	e					Multiple Declarations of string detected in entity @ at line @
vhe	csc	mod	mod_unit_mult_decl_string_cscvh	e					Multiple Declarations of string detected in unit @ at line @
vhe	csc	mod	mod_mult_def_cscvh	e					Module @ defined in

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									multiple places at line @
vhe	csc	mod	mod_ent_mult_def_cscvh	e					Entity @ defined in multiple places at line @
vhe	csc	mod	mod_unit_mult_def_cscvh	e					Unit @ defined in multiple places at line @
vhe	csc	mod	mod_no_module_found_cscvh	e					No modules found at line @
vhe	csc	mod	mod_no_entity_found_cscvh	e					No entity found at line @
vhe	csc	mod	mod_no_unit_found_cscvh	e					No unit found at line @
vhe	csc	mod	failed_find_mod_cscvh	e					Failed to find module @ at line @
vhe	csc	mod	failed_find_entity_cscvh	e					Failed to find entity @ at line @
vhe	csc	mod	failed_find_unit_cscvh	e					Failed to find unit @ at line @
vhe	csc	mod	empty_mod_cscvh	e					Empty module at line @
vhe	csc	mod	empty_ent_cscvh	e					Empty entity at line @
vhe	csc	mod	empty_unit_cscvh	e					Empty unit at line @
vhe	csc	net	net_implicit_wire_redecl_reg_cscvh	e					Implicitly declared as a wire @ re-declared as a reg @. at line @
vhe	csc	net	undecl_net_in_mod_cscvh	e					Undeclared net @ in module @ at line @
vhe	csc	net	undecl_port_in_mod_cscvh	e					Undeclared port @ in module @ at line @
vhe	csc	net	undecl_sig_in_mod_cscvh	e					Undeclared signal @ in module @ at line @
vhe	csc	net	undecl_net_in_ent_cscvh	e					Undeclared net @ in entity @ at line @
vhe	csc	net	undecl_port_in_ent_cscvh	e					Undeclared port @ in entity @ at line @
vhe	csc	net	undecl_sig_in_ent_cscvh	e					Undeclared signal @ in entity @ at line @
vhe	csc	net	undecl_net_in_sig_cscvh	e					Undeclared net @ in signal @ at line @
vhe	csc	net	undecl_port_in_sig_cscvh	e					Undeclared port @ in signal @ at line @
vhe	csc	net	undecl_sig_in_sig_cscvh	e					Undeclared signal @ in signal @ at line @
vhe	csc	net	port_used_prior_to_decl_cscvh	e					Port @ used prior toDeclaration at line @
vhe	csc	net	1bit_with_prts_cscvh	e					1-bit with part select at line @
vhe	csc	netd	ill_decl_vec_cscvh	e					Illegal Declaration of vector @ at line @
vhe	csc	nett	nett_ill_reg_name_cscvh	e					Illegal register @ at line @
vhe	csc	nett	nett_ill_net_name_cscvh	e					Illegal net @ at line @
vhe	csc	nett	nett_ill_port_name_cscvh	e					Illegal port @ at line @
vhe	csc	nett	nett_ill_signal_name_cscvh	e					Illegal signal @ at line @
vhe	csc	nett	net_scalar_vect_nett_cscvh	e					Net declared as both scalar and vector at line @
vhe	csc	nett	port_scalar_vect_nett_cscvh	e					Port declared as both scalar and vector at line @
vhe	csc	nett	signal_scalar_vect_nett_cscvh	e					Signal declared as both scalar and vector at line @
vhe	csc	nett	hot_mux_not_use_bus_connection_net_cscvh	e					One hot mux can not be used for bus connection between modules Net @ at line @
vhe	csc	nett	hot_mux_not_use_bus_connection_port_cscvh	e					One hot mux can not be used for bus connection between modules Port @ at line @
vhe	csc	nett	hot_mux_not_use_bus_connection_sig_cscvh	e					One hot mux can not be used for bus connection between modules Signal @ at line @
vhe	csc	num	not_allowed_width0_num_cscvh	e					Width 0 not allowed for sized number at line @
vhe	csc	num	real_num_not_allowed_cscvh	e					Real numbers not allowed at line @
vhe	csc	num	found_x_z_in_num_literal_cscvh	e					Found x and/or z value in number literal at line @
vhe	csc	num	too_many_digits_in_sized_num_cscvh	w					Number of digits exceeds the width in a sized number at line @
vhe	csc	num	divide_by_zero_num_cscvh	e					Divide by zero at line @
vhe	csc	num	unknown_num_base_cscvh	e					Unkown number base @ at line @
vhe	csc	num	child_mod_inst_parent_mod_cscvh	e					Child module @ instantiates parent module @ at line @
vhe	csc	num	child_ent_inst_parent_ent_cscvh	e					Child entity @ instantiates entity module @ at line @
vhe	csc	num	child_sig_inst_parent_sig_cscvh	e					Child signal @

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									instantiates signal module @ at line @
vhe	csc	num	int_decl_incorrect_cscvh	e					Integer Declaration incorrect at line @
vhe	csc	num	int_var_indexed_cscvh	e					Integer variable inedexed at line @
vhe	csc	parm	ill_parm_identifier_cscvh	e					Illegal parameter @ at line @
vhe	csc	parm	value_of_parm_OS_platform_dependent_cscvh	w					Parameter select width > 32. The value is OS and platform dependent at line @
vhe	csc	parm	parm_redefined_cscvh	w					Parameter @ redefined at line @
vhe	csc	port	ill_formal_port_name_cscvh	e					Illegal formal port @ at line @
vhe	csc	pp	text_redefined_replaced_cscvh	w					Text macro redefined and replaced @. Previous definition filename, line number @ New definition filename, line number @ at line @
vhe	csc	pp	endif_or_else_without_ifdef_cscvh	e					Endif-or-else-without ifdef at line @
vhe	csc	prim	z_in_prim_inst_cscvh	e					z in primitive instantiation at line @
vhe	csc	prts	type_prts_csvh	e					Type @ does not support part select specifier at line @
vhe	csc	prts	prts_out_of_range_cscvh	e					Parameter @[@ : @]part select is out of range at line @
vhe	csc	prts	ill_prts_inst_array_cscvh	e					Illegal value for part select of instance array 'name' at line @
vhe	csc	prts	const_prts_contains_non_const_selector_cscvh	e					Constant part select @ contains a non-constant selector @ at line @
vhe	csc	prts	bus_index_prts_for_var_out_of_range_cscvh	e					Bus index @ integer of part select [@:@] for variable @ out of range at line @
vhe	csc	prts	bus_prts_for_var_out_of_range_cscvh	e					Bus part select [@:@] for variable @ out of range at line @
vhe	csc	prts	bus_prts_index_out_of_name_for_var_cscvh	e					Bus part select [@:@] index @ out of range for variable @ at line @
vhe	csc	prts	ill_token_in_prts_cscvh	e					Illegal token in part select @ at line @
vhe	csc	prts	incomplete_prts_specification_cscvh	e					Incomplete part select specification @ at line @
vhe	csc	prts	ill_index_in_prts_cscvh	e					Illegal index in part select @ at line @
vhe	csc	prts	negative_index_in_prts_not_allowed_cscvh	e					Negative index in part select @ not allowed at line @
vhe	csc	prts	prts_index_order_reversed_cscvh	e					Part select index order reversed [@ : @] [@ : @] should be [@ : @] at line @
vhe	csc	prts	index_vec_over_max_size_cscvh	w					Vector index @ exceeds the size of the vector. Index truncated at line @
vhe	csc	prts	x_or_z_in_vec_bit_select_index_cscvh	e					x or z in vector bit select index at line @
vhe	csc	simr	inefficient_op_not_a_power_of_2_cscvh	e					Division/modulus by a number not a power of 2. Inefficient simulation operation. at line @
vhe	csc	simr	simr_multiple_init_blk_force_cscvh	w					Multiple initial blocks force @. Unpredictable simulation result at line @
vhe	csc	snsl	incomplete_snsl_cscvh	w					Incomplete sensitivity list. @ is not in the sensitivity list. at line @
vhe	csc	snsl	edge_sns_process_contains_data_pin_snsl_cscvh	e					Edge sensitive process contains a data pin @ in the sensitivity list at line @
vhe	csc	snsl	unsupp_expr_in_snsl_cscvh	w					Unsupported Expression type @ in sensitivity list ' at line @
vhe	csc	snsl	partial_bus_decl_width_cscvh	e	?				partial bus @ declared with width @ width @ at line @
vhe	csc	snsl	contains_inst_name_cscvh	e					Contains instance name @ at line @
vhe	csc	stmt	null_not_allowed_stmt_cscvh	e					Null statement is not allowed here at line @

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vhe	csc	stmt	stmt_ill_accept_only_net_reg_mem_cscvh	e					Illegal type @ can only accept net, reg, memory at line @
vhe	csc	stmt	stmt_ill_accept_only_port_reg_mem_cscvh	e					Illegal type @ can only accept port, reg, memory at line @
vhe	csc	stmt	stmt_ill_accept_only_signal_reg_mem_cscvh	e					Illegal type @ can only accept signal, reg, memory at line @
vhe	csc	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_cscvh	e					Arithmetic operator RHS has one less bit than the LHS at line @
vhe	csc	stmt	ar_op_unequal_lhs_rhs_cscvh	e					Arithmetic operator unequal width LHS and RHS at line @
vhe	csc	stmt	ar_op_unequal_var_on_rhs_csc	e					Arithmetic operator unequal width variables @ on RHS at line @
vhe	csc	stmt	empty_stmt_csc	e					Empty-statement at line @
vhe	csc	syst	return_var_of_user_used_as_rhs_cscvh	w					Return variable of user system task is used as a RHS variable at line @
vhe	csc	task	ask_var_not_decl_cscvh	e					Variable @ used but not declared at line @
vhe	csc	task	too_many_arg_to_task_cscve	e					Too many arguments passed to task @ at line @
vhe	csc	task	too_few_arg_to_task_cscvh	e					Too few arguments passed to task @ at line @
vhe	csc	tri	instance_not_tri_state_device_cscvh	e					Instance name is not a tri-state device at line @
vhe	csc	tri	unsupp_gate_type_tristate_cscvh	e					Unsupported gate type @ used for tristate at line @
vhe	csc	tri	tri_not_desgn_gate_contention_cscvh	e					Tristate not designed correctly gate @ can cause contention at line @
vhe	csc	tri	unsupp_type_instance_tri_cscvh	e					Unsupported type instance type used for tristate @ at line @
vhe	csc	tri	incorrect_cont_assign_stmt_tri_gate_cscvh	e					Incorrect continuous assign statement for tristate gate @ at line @
vhe	csc	tri	const_assign_to_multidriven_net_cscvh	e					Constant (constiznt) assigned to multi-driven Net @ at line @
vhe	csc	tri	const_assign_to_multidriven_port_cscvh	e					Constant (constiznt) assigned to multi-driven Port @ at line @
vhe	csc	tri	const_assign_to_multidriven_signal_cscvh	e					Constant (constiznt) assigned to multi-driven Signal @ at line @
vhe	csc	tri	unsupp_expr_for_tri_cscvh	e					Unsupported Expression type @ for tristate at line @
vhe	csp	ccd	misplaced_csdir_ignored_csvh	e				x	Lower case directive in wrong location. Ignored at line @
vhe	csp	cmdl	ill_cmdl_uselib_dir_path_csvh	e					Illegal 'uselib directory path @ no such directory at line @
vhe	csp	cmnt	vhe_csp_cmnt_miss_closing_csvh	e					/* comment missing closing */ at line @
vhe	csp	csi	miss_char_case_csvh	e					Missing character @ at line @
vhe	csp	expr	malformed_unary_expr_vcsp	e					Malformed unary Expression @ at line @
vhe	csp	expr	malformed_binary_expr_vcsp	e					Malformed binary Expression @ at line @
vhe	csp	expr	malformed_ternary_expr_vcsp	e					Malformed ternary Expression @ at line @
vhe	csp	expr	expr_found_reserved_word_csvh	e					Expected identifier but found reserved word @ at line @
vhe	csp	expr	expr_concatenation_empty_csvh	e					Concatenation empty at line @
vhe	csp	expr	ill_operator_expr_csvh	e					Illegal operator @ at line @
vhe	csp	expr	ill_operand_expr_csvh	e					Illegal operand @ at line @
vhe	csp	file	cannot_open_file_csvh	e					Cannot open file @ at line @
vhe	csp	file	line_lenght_overflow_csvh	e					Line length overflow line_length @ at line @
vhe	csp	file	environ_var_in_filel_csvh	e					Environ variable in file list at line @
vhe	csp	func	undefined_func_csvh	e					Undefined function @ at

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									line @
vhe	csp	inst	ill_mod_inst_name_csvh	e					Illegal module instance @ at line @
vhe	csp	inst	ill_entity_inst_name_csvh	e					Illegal entity instance @ at line @
vhe	csp	inst	ill_unit_inst_name_csvh	e					Illegal unit instance @ at line @
vhe	csp	lib	not_open_lib_file_csvh	e					Cannot open library file @ at line @
vhe	csp	list	trail_comma_list_vhs	e					Trailing comma in parentheses enclosed list at line @
vhe	csp	list	list_miising_comma_csvh	w					Missing comma between @ and name at line @
vhe	csp	mifc	mifc_port_type_unsupported_csvh	e					Port type @ unsupported at line @
vhe	csp	mmod	mult_vhs_arg_div	e					Macro @ contains too many actual arguments at line @
vhe	csp	mmod	miss_vhs_arg_div	e					Macro @ is missing some actual arguments at line @
vhe	csp	mmod	not_else_vhs_div	e					Unmatched 'else directive at line @
vhe	csp	mmod	not_endif_vhs_div	e					Unmatched 'endif directive at line @
vhe	csp	mmod	not_include_vhs_div	e					Missing filename for 'include directive at line @
vhe	csp	mmod	bad_include_vhs_div	e					Badly formed include directive at line @
vhe	csp	mmod	fmis_include_vhs_div	e					Filename missing in #include directive at line @
vhe	csp	mod	mod_miss_endmodule_csvh	e					Missing endmodule at line @
vhe	csp	mod	mod_no_module_found_csvh	e					No modules found at line @
vhe	csp	mod	mod_no_entity_found_csvh	e					No entity found at line @
vhe	csp	mod	mod_no_unit_found_csvh	e					No unit found at line @
vhe	csp	nett	nett_unsupported_reg_csvh	e					Unsupported register type @ at line @
vhe	csp	num	radix_h_num_vhs	ew					Illegal number radix, 'h expected at line @
vhe	csp	num	radix_b_num_vhs	ew					Illegal number radix, 'b expected at line @
vhe	csp	num	radix_d_num_vhs	ew					Illegal number radix, 'd expected at line @
vhe	csp	num	radix_o_num_vhs	ew					Illegal number radix; 'o expected at line @
vhe	csp	parm	mod_parm_miss_csv	e					Module @ parameter declaration missing value at line @
vhe	csp	parm	entity_parm_miss_csv	e					Module @ parameter declaration missing value at line @
vhe	csp	parm	unit_parm_miss_csv	e					Module @ parameter declaration missing value at line @
vhe	csp	port	ill_formal_port_name_csvh	e					Illegal formal port @ at line @
vhe	csp	pp	pp_cannot_open_file_not_exist_csvh	e					Cannot open include file @, file does not exist at line @
vhe	csp	pp	pp_cannot_open_file_not_have_read_perm_csvh	e					Cannot open include file @, file does not have read permission at line @
vhe	csp	prts	define_ill_prts_csv	e					Illegal part select specifier, define missing at line @
vhe	csp	prts	prts_part_select_csvh	e					Badly formed part select at line @
vhe	csp	sdir	synopsys_cdir_csvh	w					Found Synopsys compiler directive at line @
vhe	csp	stmt	miss_comma_stmt_vhs	e					Missing comma at line @
vhe	csp	stmt	miss_semicolon_stmt_vhs	e					Missing semi colon at line @
vhe	csp	stmt	miss_char_stmt_vhs	e					Missing @ at line @
vhe	csp	stmt	wait_kword_stmt_vhs	e					@ expected at line @
vhe	csp	stmt	null_not_allowed_stmt_csvh	e					Null statement is not allowed here at line @
vhe	csp	str	ill_str_char_found_csvh	e					Illegal character @ found after backslash at line @
vhe	csp	sysc	system_call_csvh	w					Found system call @ at line @
vhe	csp	udir	other_cdir_csvh	w					Found other compiler directive at line @
vhe	prp	file	not_dir_name_file_vhp	e					Directory @ does not

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									exist at line @
vhe	prp	file	cannot_open_file_ppvh	e					Cannot open file @ at line @
vhe	prp	pp	not_incl_directive_pp_ppvh	e					Empty filename for 'include directive at line @
vhe	prp	pp	pp_miss_macroname_vh	e					Missing macro name at line @
vhe	prp	pp	ill_macroname_pp_vh	e					Illegal macro name @ at line @
vhe	prp	pp	pp_text_macro_rec_vh	e					Text macro string used recursively at line @
vhe	prp	pp	pp_cannot_open_libfile_ppvh	e					Cannot open library file @ at line @
vhe	prp	pp	pp_text_macroname_not_defined_ppvh	e					Text macro (name) not defined at line @
vhe	prp	pp	pp_ifdef_miss_macroname_ppvh	e					'ifdef missing macro name at line @
vhe	prp	pp	pp_undef_miss_macroname_ppvh	e					'undef missing macro name at line @
vhe	prp	pp	pp_miss_endif_directive_ppvh	e					Missing 'endif directive at line @
vhe	prp	pp	pp_rec_include_file_ppvh	e					Recursive INCLUDE file @ at line @
vhe	prp	pp	cmdl_arg_used_in_def_ppvh	e					Command line argument used in define at line @
vhe	prp	pp	pp_undef_macro_ppvh	e					Undef @ not defined macro at line @
vhe	vep	ccd	misplaced_csdir_ignored_vevh	e				x	Lower case directive in wrong location. Ignored at line @
vhe	vep	cmdl	ill_cmdl_uselib_dir_path_vhve	e					Illegal 'uselib directory path @ no such directory at line @
vhe	vep	cmnt	vhe_vep_cmnt_miss_closing_vevh	e					/* comment missing closing */ at line @
vhe	vep	csi	miss_char_case_vevh	e					Missing character @ at line @
vhe	vep	expr	malformed_unary_expr_vvep	e					Malformed unary Expression @ at line @
vhe	vep	expr	malformed_binary_expr_vvep	e					Malformed binary Expression @ at line @
vhe	vep	expr	malformed_ternary_expr_vvep	e					Malformed ternary Expression @ at line @
vhe	vep	expr	expr_found_reserved_word_vevh	e					Expected identifier but found reserved word @ at line @
vhe	vep	expr	expr_concatenation_empty_vevh	e					Concatenation empty at line @
vhe	vep	expr	ill_operator_expr_vevh	e					Illegal operator @ at line @
vhe	vep	expr	ill_operand_expr_vevh	e					Illegal operand @ at line @
vhe	vep	file	cannot_open_file_vevh	e					Cannot open file @ at line @
vhe	vep	file	line_lenght_overflow_vevh	e					Line length overflow line_length @ at line @
vhe	vep	file	environ_var_in_filel_vevh	e					Environ variable in file list at line @
vhe	vep	func	undefined_func_vevh	e					Undefined function @ at line @
vhe	vep	inst	ill_mod_inst_name_vevh	e					Illegal module instance @ at line @
vhe	vep	inst	ill_entity_inst_name_vevh	e					Illegal entity instance @ at line @
vhe	vep	inst	ill_unit_inst_name_vevh	e					Illegal unit instance @ at line @
vhe	vep	lib	not_open_lib_file_vevh	e					Cannot open library file @ at line @
vhe	vep	list	trail_comma_list_vhc	e					Trailing comma in parentheses enclosed list at line @
vhe	vep	list	list_miising_comma_vevh	w					Missing comma between @ and name at line @
vhe	vep	mifc	mifc_port_type_unsupported_vevh	e					Port type @ unsupported at line @
vhe	vep	mmod	mult_vhc_arg_div	e					Macro @ contains too many actual arguments at line @
vhe	vep	mmod	miss_vhc_arg_div	e					Macro @ is missing some actual arguments at line @
vhe	vep	mmod	not_else_vhc_div	e					Unmatched 'else directive at line @
vhe	vep	mmod	not_endif_vhc_div	e					Unmatched 'endif directive at line @
vhe	vep	mmod	not_include_vhc_div	e					Missing filename for 'include directive at line @
vhe	vep	mmod	bad_include_vhc_div	e					Badly formed include

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									directive at line @
vhe	vep	mmod	fmis_include_vhc_div	e					Filename missing in #include directive at line @
vhe	vep	mod	mod_miss_endmodule_vevh	e					Missing endmodule at line @
vhe	vep	mod	mod_no_module_found_vevh	e					No modules found at line @
vhe	vep	mod	mod_no_entity_found_vevh	e					No entity found at line @
vhe	vep	mod	mod_no_unit_found_vevh	e					No unit found at line @
vhe	vep	nett	nett_unsupported_reg_vevh	e					Unsupported register type @ at line @
vhe	vep	num	radix_h_num_vhc	ew					Illegal number radix, 'h expected at line @
vhe	vep	num	radix_b_num_vhc	ew					Illegal number radix, 'b expected at line @
vhe	vep	num	radix_d_num_vhc	ew					Illegal number radix, 'd expected at line @
vhe	vep	num	radix_o_num_vhc	ew					Illegal number radix; 'o expected at line @
vhe	vep	parm	mod_parm_miss_vev	e					Module @ parameter declaration missing value at line @
vhe	vep	parm	entity_parm_miss_vev	e					Module @ parameter declaration missing value at line @
vhe	vep	parm	unit_parm_miss_vev	e					Module @ parameter declaration missing value at line @
vhe	vep	port	ill_formal_port_name_vevh	e					Illegal formal port @ at line @
vhe	vep	pp	pp_cannot_open_file_not_exist_vevh	e					Cannot open include file @, file does not exist at line @
vhe	vep	pp	pp_cannot_open_file_not_have_read_perm_vevh	e					Cannot open include file @, file does not have read permission at line @
vhe	vep	prts	define_ill_prts_vev	e					Illegal part select specifier, define missing at line @
vhe	vep	prts	prts_part_select_vevh	e					Badly formed part select at line @
vhe	vep	sdir	synopsys_cdir_evvh	w					Found Synopsys compiler directive at line @
vhe	vep	stmt	miss_comma_stmt_vhc	e					Missing comma at line @
vhe	vep	stmt	miss_semicolon_stmt_vhc	e					Missing semi colon at line @
vhe	vep	stmt	miss_char_stmt_vhc	e					Missing @ at line @
vhe	vep	stmt	wait_kword_stmt_vhc	e					@ expected at line @
vhe	vep	stmt	null_not_allowed_stmt_vevh	e					Null statement is not allowed here at line @
vhe	vep	str	ill_str_char_found_vevh	e					Illegal character @ found after backslash at line @
vhe	vep	sysc	system_call_vevh	w					Found system call @ at line @
vhe	vep	udir	other_cdir_vevh	w					Found other compiler directive at line @
vhe	vhp	ccd	misplaced_csdir_ignored_vhvh	e				x	Lower case directive in wrong location. Ignored at line @
vhe	vhp	cmdl	ill_cmdl_uselib_dir_path_vhvh	e					Illegal 'uselib directory path @ no such directory at line @
vhe	vhp	cmnt	vhe_vhp_cmnt_miss_closing_vhvh	e					/* comment missing closing */ at line @
vhe	vhp	csi	miss_char_case_vhvh	e					Missing character @ at line @
vhe	vhp	expr	malformed_unary_expr_vvhp	e					Malformed unary Expression @ at line @
vhe	vhp	expr	malformed_binary_expr_vvhp	e					Malformed binary Expression @ at line @
vhe	vhp	expr	malformed_ternary_expr_vvhp	e					Malformed ternary Expression @ at line @
vhe	vhp	expr	expr_s_vhe	e					Expression S at line @
vhe	vhp	expr	expr_found_reserved_word_vhvh	e					Expected identifier but found reserved word @ at line @
vhe	vhp	expr	expr_concatenation_empty_vhvh	e					Concatenation empty at line @
vhe	vhp	expr	ill_operator_expr_vhvh	e					Illegal operator @ at line @
vhe	vhp	expr	ill_operand_expr_vhvh	e					Illegal operand @ at line @
vhe	vhp	file	cannot_open_file_vhvh	e					Cannot open file @ at line @
vhe	vhp	file	line_lenght_overflow_vhvh	e					Line length overflow line_length @ at line @
vhe	vhp	file	environ_var_in_filel_vhvh	e					Environ variable in file list

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									at line @
vhe	vhp	func	undefined_func_vhvh	e					Undefined function @ at line @
vhe	vhp	inst	ill_mod_inst_name_vhvh	e					Illegal module instance @ at line @
vhe	vhp	inst	ill_entity_inst_name_vhvh	e					Illegal entity instance @ at line @
vhe	vhp	inst	ill_unit_inst_name_vhvh	e					Illegal unit instance @ at line @
vhe	vhp	lib	not_open_lib_file_vhvh	e					Cannot open library file @ at line @
vhe	vhp	list	trail_comma_list_vhh	e					Trailing comma in parentheses enclosed list at line @
vhe	vhp	list	list_miising_comma_vhvh	w					Missing comma between @ and name at line @
vhe	vhp	mifc	mifc_port_type_unsupported_vhvh	e					Port type @ unsupported at line @
vhe	vhp	mmod	mult_vhh_arg_div	e					Macro @ contains too many actual arguments at line @
vhe	vhp	mmod	miss_vhh_arg_div	e					Macro @ is missing some actual arguments at line @
vhe	vhp	mmod	not_else_vhh_div	e					Unmatched 'else directive at line @
vhe	vhp	mmod	not_endif_vhh_div	e					Unmatched 'endif directive at line @
vhe	vhp	mmod	not_include_vhh_div	e					Missing filename for 'include directive at line @
vhe	vhp	mmod	bad_include_vhh_div	e					Badly formed include directive at line @
vhe	vhp	mmod	fmis_include_vhh_div	e					Filename missing in #include directive at line @
vhe	vhp	mod	mod_miss_endmodule_vhvh	e					Missing endmodule at line @
vhe	vhp	mod	mod_no_module_found_vhvh	e					No modules found at line @
vhe	vhp	mod	mod_no_entity_found_vhvh	e					No entity found at line @
vhe	vhp	mod	mod_no_unit_found_vhvh	e					No unit found at line @
vhe	vhp	nett	nett_unsupported_reg_vhvh	e					Unsupported register type @ at line @
vhe	vhp	num	radix_h_num_vhh	ew					Illegal number radix, 'h expected at line @
vhe	vhp	num	radix_b_num_vhh	ew					Illegal number radix, 'b expected at line @
vhe	vhp	num	radix_d_num_vhh	ew					Illegal number radix, 'd expected at line @
vhe	vhp	num	radix_o_num_vhh	ew					Illegal number radix; 'o expected at line @
vhe	vhp	parm	mod_parm_miss_vhv	e					Module @ parameter declaration missing value at line @
vhe	vhp	parm	entity_parm_miss_vhv	e					Module @ parameter declaration missing value at line @
vhe	vhp	parm	unit_parm_miss_vhv	e					Module @ parameter declaration missing value at line @
vhe	vhp	pars	S_stmt_pars_vh	e					Statement S at line @
vhe	vhp	port	ill_formal_port_name_vhvh	e					Illegal formal port @ at line @
vhe	vhp	pp	pp_cannot_open_file_not_exist_vhvh	e					Cannot open include file @, file does not exist at line @
vhe	vhp	pp	pp_cannot_open_file_not_have_read_perm_vhvh	e					Cannot open include file @, file does not have read permission at line @
vhe	vhp	pp	include_filne	e					Include file @ not found at line @
vhe	vhp	prts	define_ill_prts_vhv	e					Illegal part select specifier, define missing at line @
vhe	vhp	prts	prts_part_select_vhvh	e					Badly formed part select at line @
vhe	vhp	sdir	synopsys_cdir_vhvh	w					Found Synopsys compiler directive at line @
vhe	vhp	stmt	miss_comma_stmt_vhh	e					Missing comma at line @
vhe	vhp	stmt	miss_semicolon_stmt_vhh	e					Missing semi colon at line @
vhe	vhp	stmt	miss_char_stmt_vhh	e					Missing @ at line @
vhe	vhp	stmt	wait_kword_stmt_vhh	e					@ expected at line @
vhe	vhp	stmt	null_not_allowed_stmt_vhvh	e					Null statement is not allowed here at line @
vhe	vhp	str	ill_str_char_found_vhvh	e					Illegal character @ found after backslash at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	vhp	sysc	system_call_vhvh	w					Found system call @ at line @
vhe	vhp	udir	other_cdir_vhvh	w					Found other compiler directive at line @