Table 1.1 Categories

number	mnemonic	Phase description							
1	cse	CSL errors							
2	CSW	CSL warnings							
3	dee Design errors								
4	dew Design warnings								
5	Numeric error								
6	res	Reserved							
7	ssm	Possible Simulation and synthesis							
		mismatch							
8	vee	Verilog errors							
9	vew	Verilog warnings							
10	vhe VHDL errors								
11	vhw	VHDL warnings							

Table 1.2 Phases

number	mnemonic	Csl compiler category						
1	cct	CSL to CDOM transformation						
2	cda	CDOM analysis						
3	cdc	CDOM creation						
4								
5	cg	code generation						
6	csa	CSL analysis						
7	csb	CSL elab						
8	CSC	CSL creation						
9	csp	CSL parser						
10	cst	CSL tree walker						
11	prp	preprocessor						
12	vep	Verilog parser						
13	vet	Verilog tree walker						
14	vhp	VHDL parser						
15	vht	VHDL tree walker						

Table 1.3 Error/warning type

number	mnemonic	error/warning type
1	ase	architectural state element
2	assn	assignment
3	blk	block
4	casn	continuous assign
5	ccd	csl compiler directive
6	ccs	csl clock specification
7	cdir	CSLC directive
8	chrs	charge strength
9	clk	clock
10	cmdl	command line
11	cmnt	comment
12	cmpl	component loop
13	comb	combinational logic
14	comp	component
15	cond	conditional
16	csi	case_item
17	CSS	case statement
18	cyb	cycle based
19	datl	data loop
20	decl	declaration
21	defd	define declaration
22	dely	delay statement
23	dir	directory
24	diss	disable statement
25	dmsn	dimension
26	drst	drive strength
27	drvc	driver contention
28	dsbl	disable
29	dsgn	design
30	evc	event control
31	expr	expression
32	file	file
33	forc	force
34	func	function
35	gate	gate
36	hid	hierarchy identifier
37	id	identifier
38	inhw	inference hardware
39	init	initialization
40	inst	instantiation
41	lib	library
42	list	list
43	loop	loop
44	mdb	multi driven bus
45	mdn	multi driven net
46	mem	memory
47	mifc	module instance

number	mnemonic	error/warning type					
48	mins	module instantiation					
49	mmod	macro module					
50	mod	module					
51	net	net					
52	netd	net declaration					
53	nett	net type					
54	num	numeric					
55	parm	parameter					
56	pars	parser					
57	pli	PLI table					
58	port	port					
59	pp	preprocessor					
60	prim	primitive					
61	proc	process					
62	prts	part select					
63	real	real					
64	rel	release					
65	rst	reset					
66	scop	scope					
67	sdir	synopsys compiler directive					
68	seq	sequential					
69	sig	signal					
70	simr	simulation result					
71	snsl	sensitivity list					
72	spec	specify					
73	sply	supply					
74	stmt	statement					
75	str	string					
76	sysc	system call					
77	syst	system task					
78	task	task					
79	tbcd	testbench code					
80	time	time bit					
81	topo	topologic					
82	tri	tristate					
83	trns	transistor					
84	udir	unknown compiler directive					
85	udp	udp					
86	unsy	unsythesizable					
87	vec	vec					
		·					

Table 1.4 List of warning and error messages

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	
cse	cda	assn	unequal_length_lhs_rhs_cdcs	е					Unequal length LHS and
									RHS at line @
cse	cda	assn	unequal_length_lhs_rhs_off_one_bit_cdcs	е					Unequal length LHS and
									RHS off by one bit at line
									@
cse	cda	ccs	clkspec_clk_name_not_found	е					Clock specification @
									clock name @ not found
									at line @
cse	cda	clk	merge_clk_phases_cdcd	е					Merge clock phases
									(clock A-phase) vs (clock
									B-phase) Path for (clock
									A-phase) at line @
cse	cda	clk	gated_clk_connected_to_clk_data_logic_cdcd	е					Gated clock @ is
									connected to both clock
	292	alle	alle marga with data aignala adad						and data logic at line @ Unable to continue trace
cse	cda	clk	clk_merge_with_data_signals_cdcd	е					of clock in clock tree
									which causes the clock
									to merge with the data
									signals at line @
cse	cda	clk	cannot_analyze_the_gated_clk_type_cdcd	е					Clock tree analysis can
036	cua	CIK	carinot_analyze_the_gated_cik_type_cdcd						not analyze the gated
									clock type @ at line @
cse	cda	clk	cannot_find_the_clk_source_cdcd	е					Cannot find the clock
000	000	0	5d5a5_555d55_5d5d						source @ at line @
cse	cda	clk	clk pin not driven cdcd	е				Х	Clock pin @pin is not
									driven by a clock tree
									through combinational
									gates (there must be
									combinational path from
									a clock source to @. The
									user must identify
									generated clocks by
									using a -cslc_gen_clk
									<clock_name>- directive</clock_name>
									the endpoint of
									generated clocks. The
									end point is the end point
									of the combinational path
									from a clock source to a
									combinational gate. at
		-0.	ally make frame and lands which the						line @
cse	cda	clk	clk_net_from_seq_logic_driver_cdcd	е					Clock net @ derived from
	l				l				sequential logic driver

cse		Туре	Name	W/E	V 1995	V2001	Sys_ver	Csl	Desc name @ at line @
030	cda	clk	clk_port_from_seq_logic_driver_cdcd	е					Clock port @ derived from sequential logic
cse	cda	clk	clk_sig_from_seq_logic_driver_cdcd	е					driver name @ at line @ Clock signal @ derived
			_ 0						from sequential logic driver name @ at line @
cse	cda	clk	merge_clk_data_logic_same_gate_cdcd	е					Merged clock and data
									logic. A gate is connected to both a
									clock signal and a data signal. Clock and data
									signals cannot be
									connected to the same combinational gate. Do
									you need to use a gated clock directive to specify
									a gated clock? End point @ at line @
cse	cda	clk	mux_output_used_as_clk_cdcd	е					Mux output is used as a
									clock. Either the mux select or al of the mux
									inputs must be driven by a gated clock at line @
cse	cda	clk	generated_clk_is_selfclked_cdcd	е					Generated clock @ is self -clocked. at line @
cse	cda	clk	comb_logic_loop_in_clk_tree_cdcd	е					Combinational logic loop
									in clock tree start point @ at line @
cse	cda	clk	clk_enable_is_a_generated_clk_cdcd	е					Clock enable @ is a generated clock @ at line
cse	cda	clk	generated clk has more than one drive cdcd	е					@ Generated clock @ has
030	cua	CIK	generated_cik_nas_more_man_one_diffe_cutod						more than one driver at
cse	cda	clk	found_unsupp_gated_clk_cdcd	е					line @ Clock glitch design rule
									checking found the following unsupported
									gated clock logic type @ at line @
cse	cda	clk	unsupp_logic_operation_cdcs	w					Unsupported logic
									operation type @. at line @
cse	cda	clk	unsupp_cl_gated_logic_cdcs	w					Unsupported gated clock logic type. at line @
cse	cda	csi	noncnst_in_iclude_file_cdcs	е					Non-constant in include file @ at line @
cse	cda	datl	comb_logic_loop_in_data_logic_cdcd	е					Combinational logic loop in data logic at line @
cse	cda	datl	comb_logic_loop_in_data_logic_latch_cdcd	е					Combinational logic loop
									in data logic with Latch Buffer at line @
cse	cda	datl	find_comb_loop_cdcd	е					Component loop A combinational loop was
									detected which involves a split vector which is
									part of a combinational
									loop. Starting point @ at line @
cse	cda	datl	comp_loop_detected_cdcd	е					Component loop detected @ starting point
cse	cda	datl	irregular latch in comp loop cdcd	е					@ at line @ Irregular latch in
CSE	cua	uali	irregular_iatcri_irr_comp_loop_cucu	6					component loop. An
									irregular latch is a latch that can be open
									continuously for the entire cycle. One latch in
									the loop must be closed
									at some point during the clock cycle. starting point
cse	cda	drvc	multiply_drvn_net_nontri_gate_cdcs	W					@ at line @ Multiply drivenNet driven
									by a non-tristate gate at line @
cse	cda	drvc	multiply_drvn_port_nontri_gate_cdcs	w					Multiply drivenPort driven
									by a non-tristate gate at line @
cse	cda	drvc	multiply_drvn_sig_nontri_gate_cdcs	W					Multiply drivenSignal driven by a non-tristate
cse	cda	drvc	incompatible_driver_net_cdcs	w					gate at line @ Incompatible driver of
		-	• • • • • • • • • • • • • • • • • • • •						type @ drivingNet_@ multi drivenNet of type @
		-	5						name @ at line @
cse	cda	drvc	incompatible_driver_port_cdcs	W					Incompatible driver of type @ drivingPort_@
									multi drivenPort of type
									@ name @ at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
							•		multi drivenSignal of type @ name @ at line @
cse	cda	expr	unary_op_in_comparison_cdcs	е					Unary op used in comparison at line @
cse	cda	expr	miss_parenthesis_cdcs	е					Unary op @ with
									comparison op @ missing precedence
cse	cda	init	assn_mem_in_init_blk_cdcs	е					parenthesis at line @ Assign memory in initial
cse	cda	inst	input_port_drvn_from_inside_mod_cdcs	е					block at line @ Input port @ being driven
036	cua	IIISt	input_port_drvit_from_maide_friod_cucs	6					from inside of module @
cse	cda	inst	input_port_drvn_from_inside_entity_cdcs	е					at line @ Input port @ being driven
									from inside of entity @ at line @
cse	cda	inst	input_port_drvn_from_inside_signal_cdcs	е					Input port @ being driven from inside of signal @ at
000	cda	inat	input part not connected in parent mod adea						line @ Input port @ not
cse	cua	inst	input_port_not_connected_in_parent_mod_cdcs	е					connected in parent
cse	cda	inst	input_port_not_connected_in_parent_entity_cdcs	е					module at line @ Input port @ not
									connected in parent entity at line @
cse	cda	inst	input_port_not_connected_in_parent_signal_cdcs	е					Input port @ not connected in parent
									signal at line @
cse	cda	mdb	single_comp_contains_multiple_tri_drv_cdcs	W					A single component contains multiple tristate
cse	cda	mdb	unsuppexpr_on_lhs_net_drv_stmt_cdcs	w					drivers at line @ Unsupported Expression
			., ,						type type on LHS ofNet driver statement at line
000	cda	mdb	ungunnovar on the port dry etmt edge						@ Unsupported Expression
cse	cua	mub	unsuppexpr_on_lhs_port_drv_stmt_cdcs	W					type type on LHS ofPort
									driver statement at line @
cse	cda	mdb	unsuppexpr_on_lhs_sig_drv_stmt_cdcs	W					Unsupported Expression type type on LHS
									ofSignal driver statement at line @
cse	cda	mdb	tri_not_in_top_mod_cdcs	е					Tristate not in top module at line @
cse	cda	mdb	tri_not_in_top_ent_cdcs	е					Tristate not in top entity
cse	cda	mdb	tri_not_in_top_sig_cdcs	е					at line @ Tristate not in top signal
cse	cda	mdb	tri_primitive_inst_cdcs	е					at line @ Tristate primitive
cse	cda	mdb	tri_net_only_one_drvr_cdcs	е					instantiation at line @ Tri Net has only one
cse	cda	mdb	tri port only one dryr cdcs	е					driver at line @ Tri Port has only one
									driver at line @
cse	cda	mdb	tri_sig_only_one_drvr_cdcs	е					Tri Signal has only one driver at line @
cse	cda	mod	redef_mod_cdcs	е					Redefined module @ at line @
cse	cda	mod	redef_ent_cdcs	е					Redefined entity @ at line @
cse	cda	mod	redef_signal_cdcs	е					Redefined signal @ at line @
cse	cda	net	tri_and_net_only_one_driver_cdcs	е	?				triandNet @ has only one
cse	cda	net	tri_and_port_only_one_driver_cdcs	е	?				driver at line @ triandPort @ has only
cse	cda	net	tri_and_sig_only_one_driver_cdcs	е	?				one driver at line @ triandSignal @ has only
cse	cda	net	var assn but never ref cdcs	е					one driver at line @ Variable @ assigned but
000	odd	1100	vai_uooi1_but_110v01_101_0000						never referenced at line
cse	cda	net	var_never_assn_cdcs	е					@ Variable @ never
cse	cda	net	var_not_assn_in_all_paths_cdcs	е					assigned at line @ Variable @ not being
									assigned in all paths at line @
cse	cda	net	var_not_in_snsl_cdcs	е					Variable @ not in sensitivity list at line @
cse	cda	net	reg_connected_to_inout_in_inst_cdcs	е					Reg @ connected to
									inout @ in instantiation @ at line @
cse	cda	net	reg_connectede_to_output_in_inst_cdcs	е					Reg @ connected to output in instantiation at
cse	cda	net	reg_used_as_output_of_cont_assn_cdsc	е					line @ Reg @ used as output of
330	Jua		. 5g_2555_55_654;pat_51_5511_6551_655						continuous assign at line
cse	cda	net	port_used_prior_to_decl_cdcs	е					Port @ used prior
					1				toDeclaration at line @

	В		N	W/E   W/400	110004		
cse	Phase cda	<b>Type</b> parm	Name redef_param_cdcs	W/E V1995	V2001	Sys_ver C	Redefined parameter @
cse	cda	pp	redef_macro_cdcs	е			at line @ Redefined macro @ at
cse	cda	prts	vec_index_order_incorrect_cdcs	е			line @ Vector index @ order
cse	cda	prts	vec_index_truncated_cdcs	е			incorrect at line @ Vector index @ truncated
cse	cda	seq	seq_latch_connected_to_latch_in_loop_cdcd	е			at line @ Latch connected to latch
cse	cda	sply	output_conncet_to_sply_	е			in loop at line @ Output @ connect to
cse	cda	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_cdcs	е			supply at line @ Arithmetic operator RHS
			•				has one less bit than the LHS at line @
cse	cda	stmt	ar_op_unequal_lhs_rhs_cdsc	е			Arithmetic operator unequal width LHS and RHS at line @
cse	cda	stmt	ar_op_unequal_var_on_rhs_cdcs	е			Arithmetic operator unequal width variables
	ada	4=:	tri not in ton mod adag				@ on RHS at line @ Tristate @ not in top
cse	cda	tri	tri_not_in_top_mod_cdcs	е			module at line @
cse	cda	tri	tri_not_in_top_entity_cdcs	е			Tristate @ not in top entity at line @
cse	cda	tri	tri_not_in_top_signal_cdcs	е			Tristate @ not in top signal at line @
cse	cda	tri	tri_prim_ist_cdsc	е			Tristate primitive instantiation @ at line @
cse	cdc	ase	arch_state_el_mod_not_exist_cdccs	е			Architectural state element @ module @
cse	cdc	ase	arch state el ent not exist cdccs	e			does not exist at line @ Architectural state
			4.012-01-01-01-01-01-01-01-01-01-01-01-01-01-				element @ entity @ does not exist at line @
cse	cdc	ase	arch_state_el_unit_not_exist_cdcvs	е			Architectural state element @ unit @ does
							not exist at line @ at line @
cse	cdc	ase	arch_state_el_missi_clk_name_cdccs	е			Architectural state element @ is missing the
cse	cdc	ase	arch_state_el_miss_mem_name_cdccs	е			clock name at line @ Architectural state
							element @ is missing the memory name at line @
cse	cdc	ase	arch_state_el_miss_the_cdccs	е			Architectural state element @ is missing the
cse	cdc	ase	arch_state_el_miss_rst_name_cdccs	е			@ at line @ Architectural state
							element @ is missing the reset name at line @
cse	cdc	ase	arch_state_el_evtrigg_miss_ev_name_cdcsc	е			Architectural state element @ is event
							triggered and is missing the event name at line @
cse	cdc	ase	arch_state_el_clk_name_not_found_cdccs	е			Architectural state element @ clock name
cse	cdc	ase	arch_state_el_mem_name_not_found_cdccs	e			@ not found at line @ Architectural state
CSE	cuc	ase	arch_state_ei_mem_name_not_round_cuccs				element @ memory name @ not found at line
			and state of set found ada	_			@
cse	cdc	ase	arch_state_el_not_found_cdcs	е			Architectural state element @
							arch_state_name @ not found at line @
cse	cdc	assn	x_in_rhs_of_assihnment_cdccs	е			x in rhs of assignment at line @
cse	cdc	assn	z_in_rhs_of_assn_default_csi_cdccs	е			x in rhs of assignement in defaultCase item at
cse	cdc	assn	z_in_rhs_of_assn_cdccs	е			line @ z in rhs of assignement
cse	cdc	assn	unequal_length_lhs_rhs_cdccs	e			at line @ Unequal length LHS and
cse	cdc	assn	unequal_length_lhs_rhs_off_one_bit_cdccs	e			RHS at line @ Unequal length LHS and
			· · · · · · · · · · · · · · · · · · ·				RHS off by one bit at line
cse	cdc	ccd	ccd_cdir_must_be_cst_expr_cdccs	е			CSL directive size must be constant Expression at line @
cse	cdc	ccd	clk_dir_not_applied_to_dsgn_cdccs	w			x CSL clock directive not applied to design. Could
cse	cdc	ccd	csl_filter_unused_cdccs	W			not find clock at line @  x
cse	cdc	ccd	csl_mess_not_filtered_cdccs	w			unused. at line @ x CSL message @ can not
							be filtered. Filter @ is unused. at line @
cse	cdc	ccd	error_csdir_not_found_cdccs	е			x Error CSL directive @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
-		. , , , ,			11000	12001	<b> </b>		not found. Error @ is
cse	cdc	chrs	ill_val_chrs_cdc	е					unused. at line @ Illegal value @ at line @
cse	cdc	clk	clk_name_not_found_cdir_cdccs	e				Х	Clock name not found in
									cslc directive at line @
cse	cdc	clk	expr_sunj_to_different_clk_phases_cdccs	е					Expression subject to different clock phases at
									line @
cse	cdc	csi	z_csi_not_in_casez_cdc	е					z case item not in casez at line @
cse	cdc	csi	noncstn_rep_in_conc_cdccs	е					Non-constant repeator in
			- ,						concatenation at line @
cse	cdc	decl	decl_array_over_max_size_cdccs	е					Array @ exceeds maximum size limit at
									line @
cse	cdc	dely	x_or_z_in_dely_cdccs	е					x or z in delay at line @
cse	cdc	dmsn	mem_prts_index_out_of_range_for_mem_cdccs	е					Memory part select [@:@] index @ out
									range for memory @ at
		d							line @
cse	cdc	dmsn	dime_select_for_mem_missing_cdccs	е					Select for memory @ missing at line @
cse	cdc	dmsn	dime_index_out_of_bounds_for_mem_cdccs	е					Index <index> out of</index>
									bounds for memory @. Range [@: @] at line @
cse	cdc	dmsn	dime_prts_out_of_bounds_for_net_cdccs	е					Part select [@ : @] out of
									bounds for net @. Range
cse	cdc	dmsn	dime_prts_out_of_bounds_for_port_cdccs	е					[@ : @] at line @ Part select [@ : @] out of
030	cuc	dilloll	dime_pres_out_or_bounds_tor_port_oucos						bounds for port @.
		d	diana anta anta af la anada fan air ada-a						Range [@ : @] at line @
cse	cdc	dmsn	dime_prts_out_of_bounds_for_sig_cdccs	е					Part select [@ : @] out of bounds for signal @.
									Range [@ : @] at line @
cse	cdc	dmsn	dime_prts_reg_cdccs	е					Part select [@ : @] reg @. Range [@ : @] at line
									@. Range [@ : @] at line @
cse	cdc	drvc	incompatible_drvc_for_net_cdccs	е					Incompatible drivers for
cse	cdc	drvc	incompatible_drvc_for_port_cdccs	е					Net @ at line @ Incompatible drivers for
CSE	cuc	uivc	incompatible_divc_ioi_port_caccs	6					Port @ at line @
cse	cdc	drvc	incompatible_drvc_for_sig_cdccs	е					Incompatible drivers for
cse	cdc	drvc	drvc_multiple_drive_net_partially_overlap_cdccs	е					Signal @ at line @ Multiple drive Net
									partially overlap at line @
cse	cdc	drvc	drvc_multiple_drive_port_partially_overlap_cdccs	е					Multiple drive Port partially overlap at line @
cse	cdc	drvc	drvc_multiple_drive_sig_partially_overlap_cdccs	е					Multiple drive Signal
									partially overlap at line @
cse	cdc	dsgn	dsgn_top_mod_cannot_id_cdccs	е					Top module @ cannot be identified at line @
cse	cdc	dsgn	dsgn_top_entity_cannot_id_cdccs	е					Top entity @ cannot be
cse	cdc	dsgn	dsgn_top_unit_cannot_id_cdccs	е					identified at line @ Top unit @ cannot be
036	cuc	usgii	usgri_top_urin_carinot_id_cuccs						identified at line @
cse	cdc	dsgn	unit_dsgn_cycle_not_spanning_tree_cdccs	е					Unit design hierarchy
									contains a cycle. Hierarchy is not a
									spanning tree. at line @
cse	cdc	expr	expr_prts_indices_1bit_var_cdccs	е					Part select indices 1-bit
cse	cdc	expr	expr_prts_must_be_cst_expr_cdccs	е					variable at line @ Part select specifier
									Expression must be
									constant Expression at line @
cse	cdc	expr	not_const_expr_cdcsc	е					Repetition multiplier in
									concatenation is not a
									constant Expression at line @
cse	cdc	expr	ill_bit_select_expr_cdccs	е					Illegal bit select
cse	cdc	expr	repetition_multiplier_in_conc_not_const_expr_cdccs	w					expression @ at line @ Repetition multiplier in
CSE	cuc	expi	repetition_multiplier_in_conc_not_const_expr_cuces	VV					concatenation is not a
									constant Expression at
cse	cdc	expr	int_operand_not_1_bit_cdccs	w					line @ Logic operator has
	000	onp.	opoia.iaiot_						integer operands instead
									of 1-bit operands at line @
cse	cdc	expr	unsupp_expr_cdccs	W					Unsupported Expression
		-							type @ at line @
cse	cdc	expr	unsupp_operator_cdccs	W					Unsupported operator type @ at line @
cse	cdc	expr	use_of_sg_bit_const_cdccs	w					Use of single bit constant
			5						at line @
cse	cdc	expr	unary_op_in_comparison_cdccs	е					Unary op used in comparison at line @
cse	cdc	expr	x_or_z_in_cond_expr_cdccs	е					x or z in conditional
cse	cdc	expr	zero_in_rep_in_conc_cdccs	е					expression at line @ Zero repeator in
USE	cut	evhi	Zero_iii_rep_iii_conc_caccs	E	1			<u> </u>	Zero repeator in

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	cdc	expr	expr_in_mod_port_dir_cdccs	е					concatenation at line @ Expression @ in module
cse	cdc	expr	expr_in_ent_port_dir_cdccs	е					port dir at line @ Expression @ in entity
		-							port dir at line @
cse	cdc	expr	expr_in_sig_port_dir_cdccs	е					Expression @ in unit port dir at line @
cse	cdc	expr	expr_in_inst_cdccs	е					Expression @ in inst i@ at line @
cse	cdc	expr	expr_operator_operands_unequal_lenght_cdccs	е					Expression operator @ operands @ unequal
000	cdc	file	cannot open filter specification file cdccs						length at line @ Cannot open filter
cse	cuc	ille	cannot_open_inter_specification_ine_cuccs	е					specification file @ at line
cse	cdc	file	filter_specification_file_missing_cdccs	е					@ Filter specification file
									name @ is missing at line @
cse	cdc	file	mismatch_mod_file_name_cdccs	е					Mismatch between module name @ and file
		£:1 -	rianatah ant Ela gara-						name @ at line @
cse	cdc	file	mismatch_ent_file_name_cdccs	е					Mismatch between entity name @ and file name
cse	cdc	file	mismatch_sig_file_name_cdccs	е					@ at line @ Mismatch between signal
			_ 0						name @ and file name @ at line @
cse	cdc	func	port_not_output_func_cdccs	е					Port @ direction cannot
cse	cdc	func	too_many_arg_to_func_cdccs	е					be output at line @ Too many arguments
									passed to function @ at line @
cse	cdc	func	too_few_arg_to_func_cdccs	е					Too few arguments passed to function @ at
000	cdc	func	undefined_func_cdccs	е					line @ Undefined function @ at
cse									line @
cse	cdc	func	funct_expr_cannot_expnaded_cdccs	е					Function expression @ cannot be expanded at
cse	cdc	func	funct_not_used_in_expr_cdccs	w					line @ Function @ is not being
									used in an Expression at line @
cse	cdc	func	func_decl_cdccs	w					Function Declaration @
									already declared as another type at line @
cse	cdc	hid	cannot_locate_hier_id_hid_cdccs	е					Can't locate hierarchical identifier @ at line @
cse	cdc	hid	ref_minst_found_in_expr_hid_cdccs	е					References a module instance @ found in an
cse	cdc	hid	ref entity found in expr hid cdccs	е					Expression hid at line @ References a entity
CSE	cuc	IIIu	rei_enuty_tound_in_expl_ind_cuccs	6					instance @ found in an
cse	cdc	hid	ref_unit_found_in_expr_hid_cdccs	е					Expression hid at line @ References a unit
									instance @ found in an Expression hid at line @
cse	cdc	hid	hid_reference_not_found_cdccs	е					@ reference not found at line @
cse	cdc	hid	mifc_in_hid_not_exist_cdccs	е					Module instance @ in hid does not exist at line @
cse	cdc	hid	entity_instance_in_hid_not_exist_cdccs	е					Entity instance @ in hid
cse	cdc	hid	unit_instance_in_hid_not_exist_cdccs	е					does not exist at line @ Unit instance @ in hid
cse	cdc	hid	mod_found_in_path_in_dsgn_cdccs	е					does not exist at line @ Module @ found in path
cse	cdc	hid	enity_found_in_path_in_dsgn_cdccs	е					@ in the design at line @ Entity @ found in path @
									in the design at line @
cse	cdc	hid	unit_found_in_path_in_dsgn_cdccs	е					Unit @ found in path @ in the design at line @
cse	cdc	hid	hierarchical_id_path_contains_func_cdc	е					Hierarchical ID @ path contains a function at line
cse	cdc	init	assn_mem_in_init_blk_cdccs	е					@ Assign memory in initial
cse	cdc	inst	inst_duplicate_mod_name_cdccs	е					block at line @  Duplicate port @ in the
USE	cuc	11151	iiiai_uupiicate_iiiou_iiaiiie_cuccs	е					port list for module @ at
cse	cdc	inst	inst_duplicate_entity_name_cdccs	е					line @ Duplicate port @ in the
									port list for entity @ at line @
cse	cdc	inst	inst_duplicate_unit_name_cdccs	е					Duplicate port @ in the port list for unit @ at line
	e al .	ie - t	III mag of times are not						. @
cse	cdc	inst	ill_mod_inst_name_cdccs	е					Illegal module instance @ at line @
cse	cdc	inst	ill_entity_inst_name_cdccs	е				[	Illegal entity instance @ at line @
cse	cdc	inst	ill_unit_inst_name_cdccs	е					Illegal unit instance @ at

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl Desc
cse	cdc	inst	inst_name_defined_mod_cdcc	е				line @ Instance name @ already defined in this module at line @
cse	cdc	inst	inst_name_defined_ent_cdcc	е				Instance name @ already defined in this entity at line @
cse	cdc	inst	inst_name_defined_unit_cdcc	е				Instance name @ already defined in this unit at line @
cse	cdc	inst	inst_too_many_bits_cdccs	е				Too many bits for port @ of instance array @, formal @, actual @ at line @
cse	cdc	inst	inst_port_not_connected_var_cdccs	е				Port 'port' of instance array 'array' is not connected to variable at
cse	cdc	inst	inst_insufficient_bits_cdccs	е				line @ Insufficient bits for port 'port' of instance array 'array', formal number, actual number at line @
cse	cdc	inst	inst_mod_name_not_defined_cdccs	е				Module name not defined
cse	cdc	inst	inst_ent_name_not_defined_cdccs	е				at line @ Entity name not defined
cse	cdc	inst	inst_unit_name_not_defined_cdccs	е				at line @ Unit name not defined at
cse	cdc	inst	many_mod_inst_param_assign_cdccs	е				line @ Too many module instance parameter
								assignments (number > rrumber) at line @
cse	cdc	inst	many_entity_inst_param_assign_cdccs	е				Too many entity instance parameter assignments (number > rrumber) at
cse	cdc	inst	many_unit_inst_param_assign_cdccs	е				line @ Too many unit instance parameter assignments (number > rrumber) at line @
cse	cdc	inst	complexexpr_cannot_mapped_inout_port_cdccs	е				Complex Expression @ cannot be mapped to
cse	cdc	inst	complexexpr_cannot_mapped_unknown_port_cdccs	е				inout port @ at line @  Complex Expression @ cannot be mapped to unknown type port @ at line @
cse	cdc	inst	netdecl_contains_ill_prts_cdccs	е				Net Declaration [@: @] contains an illegal part select at line @
cse	cdc	inst	regdecl_contains_ill_prts_cdccs	е				Reg Declaration [@ : @] contains an illegal part select at line @
cse	cdc	inst	complex_expr_inst_parent_module_cdccs  complex_expr_inst_entity_parent_module_cdccs	e e				Complex actual Expression associated with port @ of module @ instantiated in parent module at line @ Complex actual Expression associated with port @ of entity @ instantiated in parent
cse	cdc	inst	complex_expr_inst_unit_parent_module_cdccs	е				module at line @ Complex actual Expression associated with port @ of unit @ instantiated in parent module at line @
cse	cdc	inst	inst_mod_output_port_width_cdccs	е				Mod @ Output port @ width mismatch, actual-width ( port-width )
cse	cdc	inst	inst_entity_output_port_width_cdccs	е				at line @ Entity @ Output port @ width mismatch, actual-width ( port-width )
cse	cdc	inst	inst_unit_output_port_width_cdccs	е				at line @ Unit @ Output port @ width mismatch, actual-width ( port-width ) at line @
cse	cdc	inst	inst_mod_input_port_width_cdccs	е				Mod @ Input port @ width mismatch, actual-width ( port-width ) at line @
cse	cdc	inst	inst_entity_input_port_width_cdccs	е				Entity @ Input port @ width mismatch, actual-width ( port-width ) at line @
cse	cdc	inst	inst_unit_input_port_width_cdccs	е				Unit @ Input port @ width mismatch, actual-width ( port-width )

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	cdc	inst	inst_mod_not_define_cdccs	е					at line @ Module not defined at
cse	cdc	inst	inst_entity_not_define_cdccs	е					line @ Entity not defined at line
cse	cdc	inst	inst_unit_not_define_cdccs	е					@ Unit not defined at line @
cse	cdc	inst	mifc_port_actual_formal_width_mismatch_cdccs	W					Module @ instance @ port @ width mismatch, actual width @ formal width @ at line @
cse	cdc	inst	ent_port_actual_formal_width_mismatch_cdccs	W					Entity @ instance @ port @ width mismatch, actual width @ formal
cse	cdc	inst	unit_port_actual_formal_width_mismatch_cdccs	w					width @ at line @ Unit @ instance @ port @ width mismatch, actual width @ formal
cse	cdc	inst	inst_differs_in_case_from_mod_cdccs	е					width @ at line @ Instance name @ differs in case from module
cse	cdc	inst	inst_differs_in_case_from_ent_cdccs	е					name @ at line @ Instance name @ differs in case from entity name @ at line @
cse	cdc	inst	inst_differs_in_case_from_sig_cdccs	е					Instance name @ differs in case from signal name @ at line @
cse	cdc	loop	undet_init_value_loop_cdccs undet_limit_loop_cdccs	e					Unable to determine init value for loop at line @ Unable to determine limit
									for loop at line @
cse	cdc	loop	loop_bounds_calculated_int_cdccs expr_lhs_contains_var_bit_select_cdccs	w					Loop bounds are calculated to be integer @, check that this is correct at line @ Expression in lhs of assignment contains a
cse	cdc	loop	loop_bounds_not_const_cdc	W					variable bit select at line @ Loop bounds are
cse	cdc	Іоор	loop_ctrl_init_expr_not_const_cdccs	W					non-constant at line @ Non-constant loop bound. Loop control variable initialization Expression is not a constant Expression at
cse	cdc	loop	loop_term_expr_not_const_cdccs	w					line @ Non-constant loop bound. loop terminating Expression could not be evaluated to a constant at line @
cse	cdc	loop	init_expr_reset_by_var_cdccs	е					Non-constant loop bound. initializing Expression reset by variable at line @
cse	cdc	loop	loop_ctrl_var_1_bit_wide_cdccs	W					The loop control variable @ is one bit wide. Check the loop control variable Declaration. at line @
cse	cdc	mdb	bad_mdb_net_cdccs	е					Bad multi-driven Net @ at line @
cse	cdc	mdb	bad_mdb_port_cdccs	е					Bad multi-driven Port @ at line @
cse	cdc	mdb	bad_mdb_signal_cdccs	е					Bad multi-driven Signal @ at line @
cse	cdc	mdb	unsupp_comp_mdb_net_cdccs	е	?				Unsupported component type @ driving in multi-driven Net name at line @
cse	cdc	mdb	unsupp_comp_mdb_port_cdccs	е	?				Unsupported component type @ driving in multi-driven Port name at
cse	cdc	mdb	unsupp_comp_mdb_signal_cdccs	е	?				line @ Unsupported component type @ driving in multi-driven Signal name
cse	cdc	mdb	unsupp_comp_drive_mdb_cdccs	е	?				at line @ Unsupported component type @ driving multi-driven Net natne at
cse	cdc	mdb	unsupp_comp_drive_mdb_port_cdccs	е	?				line @ Unsupported component type @ driving multi-driven Port natne at line @
cse	cdc	mdb	unsupp_comp_drive_mdb_signal_cdccs	е	?				Unsupported component type @ driving multi-driven Signal natne
cse	cdc	mdb	mdb_net_driven_by_trns_cdccs	е					at line @ Multiply driven Net driven

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	cdc	mdb	mdb_port_driven_by_trns_cdccs	е			•		by transistor primitive type @ at line @ Multiply driven Port driven by transistor primitive type @ at line
cse	cdc	mdb	mdb_sig_driven_by_trns_cdccs	е					@ Multiply driven Signal
CSE	cac	mub	mub_sig_unveri_by_titis_cuccs	6					driven by transistor primitive type @ at line @
cse	cdc	mdb	mdb_unsupp_comp_drvs_net_cdccs	е					Unsupported component type driving Net drives Net connected to multi-driven Net at line @
cse	cdc	mdb	mdb_unsupp_comp_drvs_port_cdccs	е					Unsupported component type driving Port drives Port connected to multi-driven Port at line @
cse	cdc	mdb	mdb_unsupp_comp_drvs_sig_cdccs	е					Unsupported component type driving Signal drives Signal connected to multi-driven Signal at line @
cse	cdc	mdb	mdb_incompatible_net_drives_multiple_net_cdccs	е					Incompatible driver driving tandem Net drives Net connected to multi-driven Net at line @
cse	cdc	mdb	mdb_incompatible_port_drives_multiple_port_cdccs	е					Incompatible driver driving tandem Port drives Port connected to multi-driven Port at line @
cse	cdc	mdb	mdb_incompatible_sig_drives_multiple_sig_cdccs	е					Incompatible driver driving tandem Net drives Net connected to multi-driven Port at line
cse	cdc	mdb	mdb_unsupp_LHS_concatenation_cdccs	е					Unsupported LHS concatenation in multi-drive 'device at line @
cse	cdc	mdb	mdb_bus_has_too_many_drivers_cdccs	е					Bus has too many drivers, at line @
cse	cdc	mdb	mdb_always_blk_drive_cdccs	w					Multiple always blocks
cse	cdc	mdb	nontri_gate_drives_mdb_net_cdccs	w					drive name @ at line @ non-tri-state gate drives
cse	cdc	mdb	nontri_gate_drives_mdb_port_cdccs	w					multi-driven Net at line @ non-tri-state gate drives multi-driven Port at line @
cse	cdc	mdb	nontri_gate_drives_mdb_sig_cdccs	w					non-tri-state gate drives multi-driven Signal at line @
cse	cdc	mem	mem_ref_without_index_cdccs	е					Memory @ referenced without index through hierarchical ID @ at line @
cse	cdc cdc	mifc mifc	port_identifier_mifc_cdccs mod_output_wire_redecl_reg_cdccs	e e					Port @ at line @ Module @ output port re-declared as type reg after use as implicitly declared wire at line @
cse	cdc	mifc	entity_output_wire_redecl_reg_cdccs	е					Entity @ output port re-declared as type reg after use as implicitly declared wire at line @
cse	cdc	mifc	unit_output_wire_redecl_reg_cdccs	е					Unit @ output port re-declared as type reg after use as implicitly declared wire at line @
cse	cdc	mifc	output_port_is_mem_type_mifc_cdccs	е					Output port @ is memory type at line @
cse	cdc	mifc	mifc_inout_port_is_mem_type_cdccs	е					Inout port @ is memory type at line @
cse	cdc	mifc	mod_output_port_mismatch_actual_witdh_cdccs	w					Module @ output port @ formal to actual width mismatch at line @
cse	cdc	mifc	ent_output_port_mismatch_actual_witdh_cdccs	w					Entity @ output port @ formal to actual width mismatch at line @
cse	cdc	mifc	unit_output_port_mismatch_actual_witdh_cdc	W					Unit @ output port @ formal to actual width mismatch at line @
cse	cdc	mifc	port_name_different_in_upper_lower_case_cdccs	е					Port name @ different in upper lower case at line @
cse	cdc	mifc	port_not_def_in_iodecl_cdccs	е					Port @ not defined in ioDeclaration at line @
cse	cdc	mifc	port_not_def_in_portl_cdccs	е				L	Port @ not defined in port list at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc Port @ wireDeclaration
cse	cdc	mifc	port_wiredecl_mismatch_cdccs	е					mismatch at line @
cse	cdc	mifc	pos_based_null_inst_port_cdccs	е					Position based null instance port at line @
cse	cdc	mifc	last_portdecl_contains_trailcomma_cdccs	е					Last portDeclaration contains a trailing comma at line @
cse	cdc	mins	mins_expr_incompatible_type_cdccs	е					Expression @ has an
									incompatible argument type @ with the port at line @
cse	cdc	mins	mins_mod_not_exist_cdccs	е					Module @ does not exist at line @
cse	cdc	mins	mins_entity_not_exist_cdccs	е					Entity @ does not exist at line @
cse	cdc	mins	mins_unit_not_exist_cdccs	е					Unit @ does not exist at line @
cse	cdc	mod	dup_declar_name_mod_cdc	е					Duplicate Declaration of port @ at line @
cse	cdc	mod	ill_mod_name_cdccs	е					Illegal module @ at line @
cse	cdc	mod	ill_mod_entity_name_cddcs	е					Illegal entity @ at line @
cse	cdc	mod	ill_mod_unit_name_cdccs	е					Illegal unit @ at line @
cse	cdc	mod	mod_mult_decl_string_cdccs	е					Multiple Declarations of string detected in module @ at line @
cse	cdc	mod	mod_entity_mult_decl_string_cdccs	е					Multiple Declarations of string detected in entity  @ at line @
cse	cdc	mod	mod_unit_mult_decl_string_cdccs	е					Multiple Declarations of string detected in unit @ at line @
cse	cdc	mod	mod_mult_def_cdcs	е					Module @ defined in multiple places at line @
cse	cdc	mod	mod_ent_mult_def_cdccs	е					Entity @ defined in
cse	cdc	mod	mod_unit_mult_def_cdccs	е					multiple places at line @ Unit @ defined in
cse	cdc	mod	mod_no_module_found_cdccs	е					multiple places at line @ No modules found at line
cse	cdc	mod	mod_no_entity_found_cdccs	е					@ No entity found at line @
cse	cdc	mod	mod_no_unit_found_cdccs	e					No unit found at line @
cse	cdc	mod	failed_find_mod_cdccs	е					Failed to find module @
cse	cdc	mod	failed_find_entity_cdccs	е					at line @ Failed to find entity @ at line @
cse	cdc	mod	failed_find_unit_cdccs	е					Failed to find unit @ at line @
cse	cdc	mod	empty_mod_cdccs	е					Empty module at line @
cse	cdc	mod	empty_ent_cdccs	е					Empty entity at line @
cse	cdc	mod	empty_unit_cdccs	е					Empty unit at line @
cse	cdc	net	net_implicit_wire_redecl_reg_cdccs	е					Implicitly declared as a wire @ re-declared as a reg @. at line @
cse	cdc	net	undecl_net_in_mod_cdccs	е					Undeclared net @ in module @ at line @
cse	cdc	net	undecl_port_in_mod_cdccs	е					Undeclared port @ in module @ at line @
cse	cdc	net	undecl_sig_in_mod_cdccs	е					Undeclared signal @ in module @ at line @
cse	cdc	net	undecl_net_in_ent_cdccs	е					Undeclared net @ in entity @ at line @
cse	cdc	net	undecl_port_in_ent_cdccs	е					Undeclared port @ in entity @ at line @
cse	cdc	net	undecl_sig_in_ent_cdccs	е					Undeclared signal @ in
cse	cdc	net	undecl_net_in_sig_cdccs	е					entity @ at line @ Undeclared net @ in
cse	cdc	net	undecl_port_in_sig_cdccs	е					signal @ at line @ Undeclared port @ in
cse	cdc	net	undecl_sig_in_sig_cdccs	е					signal @ at line @ Undeclared signal @ in
cse	cdc	net	port_used_prior_to_decl_cdccs	е					signal @ at line @ Port @ used prior
cse	cdc	net	1bit_with_prts_cdccs	е					toDeclaration at line @ 1-bit with part select at
cse	cdc	netd	ill_decl_vec_cdccs	е					line @ Illegal Declaration of
cse	cdc	nett	nett_ill_reg_name_cdccs	е					vector @ at line @ Illegal register @ at line
cse	cdc	nett	nett ill net name cdccs	е					@ Illegal net @ at line @
cse	cdc	nett	nett_ill_port_name_cdccs	e					Illegal port @ at line @
cse	cdc	nett	nett_ill_signal_name_cdccs	е					Illegal signal @ at line @
cse	cdc	nett	net_scalar_vect_nett_cdccs	е					Net declared as both scalar and vector at line @
cse	cdc	nett	port_scalar_vect_nett_cdccs	е					Port declared as both scalar and vector at line
cse	cdc	nett	signal_scalar_vect_nett_cdccs	е					Signal declared as both

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									scalar and vector at line @
cse	cdc	nett	hot_mux_not_use_bus_connection_net_cdccs	е					One hot mux can not be used for bus connection between modules Net @ at line @
cse	cdc	nett	hot_mux_not_use_bus_connection_port_cdccs	е					One hot mux can not be used for bus connection between modules Port @
cse	cdc	nett	hot_mux_not_use_bus_connection_sig_cdccs	е					at line @ One hot mux can not be
									used for bus connection between modules Signal @ at line @
cse	cdc	num	not_allowed_width0_num_cdccs	е					Width 0 not allowed for sized number at line @
cse	cdc	num	real_num_not_allowed_cdccs	е					Real numbers not allowed at line @
cse	cdc	num	found_x_z_in_num_literal_cdccs	е					Found x and/or z value in number literal at line @
cse	cdc	num	too_many_digits_in_sized_num_cdccs	W					Number of digits exceeds the width in a sized number at line @
cse	cdc cdc	num num	divide_by_zero_num_cdccs child_mod_inst_parent_mod_cdccs	e e					Divide by zero at line @ Child module @
030	odo	nam	oma_mod_mst_parem_mod_caces						instantiates parent module @ at line @
cse	cdc	num	child_ent_inst_parent_ent_cdccs	е					Child entity @ instantiates entity module @ at line @
cse	cdc	num	child_sig_inst_parent_sig_cdccs	е					Child signal @ instantiates signal
cse	cdc	num	int_decl_incorrect_cdccs	е					module @ at line @ Integer Declaration
cse	cdc	num	int_var_indexed_cdccs	е					incorrect at line @ Integer variable inedexed
cse	cdc	parm	ill_parm_identifier_cdccs	е					at line @  Illegal parameter @ at
cse	cdc	parm	value_of_parm_OS_platform_dependent_cdccs	W					line @ Parameter select width >
cse	cuc	paiiii	value_u_pami_os_piatiomi_uependent_cuccs	v					32. The value is OS and platform dependent at line @
cse	cdc	parm	parm_redefined_cdccs	W					Parameter @ redefined at line @
cse	cdc	port	ill_formal_port_name_cdccs	е					Illegal formal port @ at line @
cse	cdc	pp	text_redefined_replaced_cdccs	w					Text macro redefined and replaced @. Previous definition filename, line number @ New definition filename, line number @ at line @
cse	cdc	pp	endif_or_else_without_ifdef_cdccs	е					Endif-or-else-without ifdef at line @
cse	cdc	prim	z_in_prim_inst_cdccs	е					z in primitive instantiation at line @
cse	cdc	prts	prts_out_of_range_cdccs	е					Parameter @[@ : @]part select is out of range at line @
cse	cdc	prts	ill_prts_inst_array_cdccs	е					Illegal value for part select of instance array
cse	cdc	prts	const_prts_contains_non_const_selector_cdccs	е					'name' at line @  Constant part select @ contains a non-constant selector @ at line @
cse	cdc	prts	bus_index_prts_for_var_out_of_range_cdccs	е					Bus index @ integer of part select [@:@] for variable @ out of range at line @
cse	cdc	prts	bus_prts_for_var_out_of_range_cdccs	е					Bus part select [@:@] for variable @ out of range at line @
cse	cdc	prts	bus_prts_index_out_of_name_for_var_cdccs	е					Bus part select [@:@] index @ out of range for variable @ at line @
cse	cdc	prts	ill_token_in_prts_cdccs	е					Illegal token in part select @ at line @
cse	cdc	prts	incomplete_prts_specification_cdccs	е					Incomplete part select specification @ at line @
cse	cdc	prts	ill_index_in_prts_cdccs	е					Illegal index in part select
cse	cdc	prts	negative_index_in_prts_not_allowed_cdccs	е					@ at line @  Negative index in part select @ not allowed at line @
cse	cdc	prts	prts_index_order_reversed_cdccs	е					Part select index order reversed [@ : @] [@ : @] should be [@ : @] at line
cse	cdc	prts	index_vec_over_max_size_cdccs	W					@ Vector index @ exceeds the size of the vector.

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl Desc	$\neg$
cse	cdc	prts	x_or_z_in_vec_bit_select_index_cdcsc	е				Index truncated at line x or z in vector bit se index at line @	
cse	cdc	sdir	ignored_synopsis_csdir_csstmt_cdccd	W				Ignored a synopsis of directive which is no	ot
cse	cdc	sdir	ignored_synopsis_csdir_miss_end_cdccd	w				applied to a Case statement at line @ Ignored a synopsis condirective which is missiphe end <directive> at</directive>	ase sing
cse	cdc	simr	inefficient_op_not_a_power_of_2_cdccs	е				Division/modulus by number not a power of Inefficient simulation operation, at line @	of 2. on
cse	cdc	simr	simr_multiple_init_blk_force_cdccs	W				Multiple initial block force @. Unpredictal simulation result at li	ks ble
cse	cdc	snsl	incomplete_snsl_cdccs	W				Incomplete sensitivity @ is not in the sensit list. at line @	
cse	cdc	snsl	edge_sns_process_contains_data_pin_snsl_cdccs	е				Edge sensitive proce contains a data pin @ the sensitivity list at I	⊉ in
cse	cdc	snsl	unsupp_expr_in_snsl_cdccs	w				Unsupported Express type @ in sensitivity l	
cse	cdc	snsl	partial_bus_decl_width_cdccs	е	?			at line @ partial bus @ declar with width @ width @ line @	
cse	cdc	snsl	contains_inst_name_cdccs	е				Contains instance na @ at line @	ıme
cse	cdc	stmt	null_not_allowed_stmt_cdccs	е				Null statement is no allowed here at line	@
cse	cdc	stmt	stmt_ill_accept_only_net_reg_mem_cdccs	е				Illegal type @ can of accept net, reg, mem at line @	
cse	cdc	stmt	stmt_ill_accept_only_port_reg_mem_cdccs	е				Illegal type @ can of accept port, reg, men at line @	
cse	cdc	stmt	stmt_ill_accept_only_signal_reg_mem_cdccs	е				Illegal type @ can of accept signal, reg memory at line @	,
cse	cdc	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_cdccs	е				Arithmetic operator R has one less bit than LHS at line @	RHS
cse	cdc	stmt	ar_op_unequal_lhs_rhs_cdccs	е				Arithmetic operato unequal width LHS a RHS at line @	
cse	cdc	stmt	ar_op_unequal_var_on_rhs_cdc	е				Arithmetic operato unequal width variab @ on RHS at line @	oles @
cse	cdc	stmt	empty_stmt_cdc	е				Empty-statement at I @	ine
cse	cdc	syst	return_var_of_user_used_as_rhs_cdccs	W				Return variable of us system task is used a RHS variable at line	as a
cse	cdc	task	ask_var_not_decl_cdccs	е				Variable @ used but declared at line @	not
cse	cdc	task	too_few_arg_to_task_cdccs	е				Too few arguments passed to task @ at @	S
cse	cdc	tri	instance_not_tri_state_device_cdccs	е				Instance name is no tri-state device at line	e @
cse	cdc	tri	unsupp_gate_type_tristate_cdccs	е				Unsupported gate ty @ used for tristate at @	
cse	cdc	tri	tri_not_desgn_gate_contention_cdccs	е				Tristate not designe correctly gate @ ca cause contention at l	an
cse	cdc	tri	unsupp_type_instance_tri_cdcsc	е				Unsupported type instance type used to tristate @ at line @	for
cse	cdc	tri	incorrect_cont_assign_stmt_tri_gate_cdccs	е				Incorrect continuou assign statement for tristate gate @ at line	or or
cse	cdc	tri	const_assign_to_multidriven_net_cdccs	е				Constant (constizm assigned to multi-driv	ıt)
cse	cdc	tri	const_assign_to_multidriven_port_cdccs	е				Net @ at line @ Constant (constizn assigned to multi-driv	
cse	cdc	tri	const_assign_to_multidriven_signal_cdccs	е				Port @ at line @ Constant (constizn assigned to multi-driv Signal @ at line @	it) ven
cse	cdc	tri	unsupp_expr_for_tri_cdccs	е				Unsupported Express type @ for tristate at @	sion

Cat	Phase cdc	<b>Type</b> vec	Name vec_invalid_cdccs	W/E	V1995	V2001	Sys_ver	Csl	Desc Vector @ is invalid. at
cse	cdc	vec	vec_mvalid_cdccs	е					line @
				е					does not exist at line @
cse	cdc	vec	vec_ent_not_exist_cdccs	е					Vector @ entity name does not exist at line @
cse	cdc	vec	vec_unit_not_exist_cdccs	е					Vector @ unit name does not exist at line @
cse	cdc	vec	vec_not_contain_data_sig_cdccs	е					Vector @ does not contain any data signals
cse	cdc	vec	vec_not_contain_clk_sig_cdccs	е					at line @ Vector @ does not
			-						contain a clock signal at line @
cse	cdc	vec	vec_not_contain_rst_sig_cdccs	е					Vector @ does not contain a reset signal at
cse	cdc	vec	vec_stim_not_contain_input_ports_cdccs	е					line @ Vector @ which is a
									stimulus vector does not contain any input ports at
cse	cdc	vec	vec_expect_not_contain_outputs_ports_cdccs	е					line @  Vector @ which is an
000	odo	100	100_0xp001_1101_0011talli1_00xp0110_p0110_00000						expect vector does not contain any output ports
									at line @
cse	cdc	vec	vec_is_missing_the_cdccs	е					Vector @ is missing the @ at line @
cse	cdc	vec	vec_dtsig_not_found_cdccs	е					Vector @ data signals @ not found at line @
cse	cdc	vec	vec_clk_sig_not_found_cdcsc	е					Vector @ clock signal @ not found at line @
cse	cdc	vec	vec_rst_sig_not_found_cdccs	е					Vector @ reset signal @ not found at line @
cse	cdc	vec	vec_stim_input_port_not_found_cdccs	е					Vector @ stimulus vector input port @ not found at
cse	cdc	vec	vec_output_port_not_found_cdccs	е					line @ Vector @ output port @
cse	cde	ase	arch_state_el_ev_not_found	е					not found at line @ Architectural state
									element @ event name @ not found at line @
cse	csa	assn	unequal_length_lhs_rhs_cscs	е					Unequal length LHS and RHS at line @
cse	csa	assn	unequal_length_lhs_rhs_off_one_bit_cscs	е					Unequal length LHS and RHS off by one bit at line
cse	csa	ccs	clkspec_miss_clk_name	е					Clock specification @ is missing the clock name at line @
cse	csa	clk	merge_clk_phases_cscd	е					Merge clock phases (clock A-phase) vs (clock B-phase) Path for (clock
cse	csa	clk	gated_clk_connected_to_clk_data_logic_cscd	е					A-phase) at line @ Gated clock @ is
									connected to both clock and data logic at line @
cse	csa	clk	clk_merge_with_data_signals_cscd	е					Unable to continue trace of clock in clock tree
									which causes the clock to merge with the data
cse	csa	clk	cannot_analyze_the_gated_clk_type_cscs	е					signals at line @ Clock tree analysis can
									not analyze the gated clock type @ at line @
cse	csa	clk	cannot_find_the_clk_source_cscd	е					Cannot find the clock source @ at line @
cse	csa	clk	clk_pin_not_driven_cscd	е				Х	Clock pin @pin is not driven by a clock tree
									through combinational gates (there must be
									combinational path from a clock source to @. The
									user must identify generated clocks by
									using a -cslc_gen_clk <clock_name>- directive</clock_name>
									the endpoint of
									generated clocks. The end point is the end point of the combinational path
									of the combinational path from a clock source to a combinational gate. at line @
cse	csa	clk	clk_net_from_seq_logic_driver_cscd	е					Clock net @ derived from sequential logic driver
cse	csa	clk	clk_port_from_seq_logic_driver_cscd	е					name @ at line @ Clock port @ derived
									from sequential logic driver name @ at line @
cse	csa	clk	clk_sig_from_seq_logic_driver_cscd	е					Clock signal @ derived from sequential logic
		1		_1	1	1	I.	1	nom sequential logic

CSE CSA CIK MILE COMPLICATION OF CONTROL OF	SC
cse csa cik generated_cik_is_selfciked_cscd e desertated_cik_cscd e connected to combinations of cse csa cik generated_cik_is_selfciked_cscd e desertated_cik_is_selfciked_cscd e desertated_cik_cscd e desertated_cik_cs	k and data gate is
cse csa cik generated_cik_is_selfciked_cscd e Consistations in clock tires at line cse csa cik generated_cik_is_selfciked_cscd e Consistations in clock tires at line cse csa cik generated_cik_is_selfciked_cscd e Consistations in clock tires at line cse csa cik generated_cik_is_selfciked_cscd e Consistations in clock tires at line cse csa cik clocked e Consistations in clock tires at line cse csa cik generated_cik_is_selfciked_cscd e Consistations in clock tires at line cse csa cik clocked e Consistations in clock tires at line cse csa cik generated_cik_has_more_than_one_drive_cscd e Generated clock cse csa cik generated_cik_has_more_than_one_drive_cscd e Generated clocked cse csa cik found_unsupp_gated_cik_cscd e Cockgition in clock gitters in csc cse csa cik unsupp_logic_operation_cscs w Cockgition to clock gitters at line cse csa cik unsupp_logic_operation_cscs w Cockgition to clock gitters at line cse csa cik unsupp_logic_expr_cik_cscs w Cockgition to	and a data
cse csa clk mux_output_used_as_clk_cscd e Mux_output a gated clock directive and gated clock directive and gated clock clock elements of self-clocked elements of self-clocked combinations of combinations and clock trees at line cse csa clk comb_logic_loop_in_elk_tree_cscd e Combinations in clock trees at line cse csa clk clk_enable_is_a_generated_clk_cscd e Generated clock_cscd elements of generated clock_cscd directive and generated_clk_has_more_than_one_drive_cscd elements directive and generated clock_cscd directive and generated clock_cscd directive and generated_clk_has_more_than_one_drive_cscd elements directive and generated_clk_cscd directive and generated_clk_generated_clk_cscd directive and generated_clk_generated_clk_generated_clk_generated_clk_generated_clk_generated_clk_generated_clk_generated_clk_generated_clk_generated_generated_clk_generated_generated_generated_generated_generated_generated_generated_generated_generated_generated_generated_generated_generated_generated_generated_generated_generated_generated_g	annot be
cse csa cik mux_output_used_as_cik_cscd e csa cik mux_output_used_as_cik_cscd e csa cik mux_output_used_as_cik_cscd e csa cik generated_cik_is_selfciked_cscd e disputs must b a gated clock. Eithe select or al a gated clock cse csa cik comb_logic_loop_in_cik_tree_cscd e csa cik comb_logic_loop_in_cik_tree_cscd e comb_indicate comb_logic_loop_in_cik_tree_cscd e comb_indicate comb	al gate. Do
Gese   Csa   Cik   mux_output_used_as_clk_cscd   e	e to specify
clock. Eithe select or ale inputs must be a gated clock   combination   clock tree   component   clock   clo	
select or al a jagated clob decreased cik generated_cik_is_selfciked_cscd e Generated comb_logic_loop_in_cik_tree_cssd e Generated comb_logic_loop_in_cik_tree_cssd e Generated comb_logic_loop_in_cik_tree_cssd e Generated comb_loop.  CSE CSA CIK CIK_enable_is_a_generated_Cik_cscd e Generated compensation or clock trees at line comb_loop.  CSE CSA CIK generated_Cik_has_more_than_one_drive_cscd e Generated compensation or clock generated compensation or clock generated compensation or clock generated compensation or clock generated clock.  CSE CSA CIK generated_Cik_has_more_than_one_drive_cscd e Generated clock generated	
cse csa clk	of the mux
Self-clocked   Combinations   Self-clocked   Combinations   Conditional   Conditiona	k at line @
CSE	
cse csa clk generated_clk_has_more_than_one_drive_cscd e Generated_cl more than or line checking following un gated_clck_cscd e Unsupp_operation_cscs w Unsupported logic_type.  cse csa clk unsupp_logic_operation_cscs w Unsupported logic_type.  cse csa clk unsupp_logic_expr_clk_cscs w Unsupported logic_type.  cse csa clk unsupp_logic_expr_clk_cscs w Unsupported logic_type.  cse csa clk unsupp_logic_expr_clk_cdcs w Unsuppologic_type.  cse csa clk unsupp_logic_expr_clk_cdcs w Unsuppologic_type.  cse csa clk unsupp_logic_expr_clk_cdcs w Unsuppologic_types.  cse csa clk unsupp_logic_expr_clk_cdcs w Unsuppologic_types.  cse csa clk unsupp_logic_expr_clk_cdcs w Component file @ at comb_logic_loop_in_data_logic_cscd e Combinations in data logic at line in data logic.  cse csa datl comb_logic_loop_in_data_logic_latch_cscd e Combinations in data logic.  cse csa datl comb_loop_cscd e Component combinations detected with a split vecto part of a component combinations detected with a split vecto part of a component combinations detected with a split vecto part of a component combinations detected with a split vector part of a component combinations detected with a split vector part of a component combinations detected with a split vector part of a component combinations detected with a split vector part of a component combinations detected with a split vector part of a component combinations detected with a split vector part of a component combinations detected with a split vector part of a component combination detected with a split vector part of a component combination detected with a split vector part of a component combination detected with a split vector part of a component combination detected with a split vector part of a component combination detected with a split vector part of a component combination detected with a split vector part of a component combination detected with a split vector part of a component combination detected with a split vector part of a component combination detected with a split vector part	tart point @
more than or line   Clock glitch of checking following ungated clock to at line   Clock glitch of checking for following ungated clock to at line   Clock glitch of checking for following ungated clock to at line   Clock glitch of checking for following ungated clock to at line   Clock glitch of checking for following ungated clock to at line   Clock glitch of checking for following ungated clock to at line   Clock glitch of checking for following ungated clock to at line   Clock glitch of checking for following ungated clock to at line   Clock glitch of checking following ungated clock to at line   Clock glitch of checking following ungated clock to at line   Clock glitch of checking following ungated clock to a logic type. In the component of the clock glitch of clock	ck @ at lin
cse csa clk unsupp_logic_operation_cscs w Unsupport operation type cse csa clk unsupp_logic_expr_clk_cscs w Unsupport operation type cse csa clk unsupp_logic_expr_clk_cscs w Unsupported logic type. i Cse csa clk unsupp_logic_expr_clk_cscs w Unsupp logicExpress cse csa clk unsupp_logic_expr_clk_cdcs w Unsupp logicExpress at line cse csa csi noncnst_in_iclude_file_cscs w Unsupp logicExpress at line cse csa datl comb_logic_loop_in_data_logic_cscd e Combinations in data logic cse csa datl comb_logic_loop_in_data_logic_latch_cscd e  cse csa datl comb_logic_loop_in_data_logic_latch_cscd e  cse csa datl comb_logic_loop_cscd e  cse csa datl comb_logic_loop_cscd e  cse csa datl comb_logic_loop_cscd e  cse csa datl comb_loop_cscd e  cse csa datl irregular_latch_in_comp_loop_cscd e  cse csa datl comp_loop_detected_cscd e  cse csa datl irregular_latch_in_comp_loop_cscd e  continuous entire cycle. C	ne driver at @
cse csa clk unsupp_logic_operation_cscs w Unsuppoperation type cse csa clk unsupp_logic_expr_clk_cscs w Unsupported logic type. i cse csa clk unsupp_logic_expr_clk_cscs w Unsupp logicExpress at line cse csa clk unsupp_logic_expr_clk_cscs w Unsupp logicExpress at line cse csa clk unsupp_logic_expr_clk_cdcs w Unsupp logicExpress at line cse csa csi noncnst_in_iclude_file_cscs e Non-constant file @ at cse csa datl comb_logic_loop_in_data_logic_cscd e Combinations in data logic cse csa datl comb_logic_loop_in_data_logic_latch_cscd e Combinations in data logic cse csa datl find_comb_loop_cscd e Componer combinations detected white a split vecto part of a com loop. Starting cse csa datl comp_loop_detected_cscd e Componer combinations detected with detect	
cse csa clk unsupp_cl_gated_logic_cscs w Unsupported logic type.:  cse csa clk unsupp_logic_expr_clk_cscs w UnsuppologicExpress at line  cse csa clk unsupp_logic_expr_clk_cdcs w Unsupp_logicExpress at line  cse csa csi noncnst_in_iclude_file_cscs e Non-constant file @ at cse csa datl comb_logic_loop_in_data_logic_cscd e Combinationa in data logic  cse csa datl comb_logic_loop_in_data_logic_latch_cscd e Combinationa in data logic  cse csa datl find_comb_loop_cscd e Combinationa combinationa detected whice a split vector part of a com loop. Starting  cse csa datl comp_loop_detected_cscd e Componer  cse csa datl irregular_latch_in_comp_loop_cscd e Componer  cse csa datl irregular_latch_in_comp_loop_cscd e Componer  cse csa datl comp_loop_detected_cscd e Componer  cse csa datl irregular_latch_in_comp_loop_cscd e Componer  componer  cse csa datl irregular_latch_in_comp_loop_cscd e Componer  c	ogic type @ e @
cse csa clk unsupp_logic_expr_clk_cscs w logic type. i cse csa clk unsupp_logic_expr_clk_cdcs w logicExpressi at line cse csa csi unsupp_logic_expr_clk_cdcs w logicExpressi at line cse csa csi noncnst_in_iclude_file_cscs e file @ at line cse csa datl comb_logic_loop_in_data_logic_cscd e Combinationa cse csa datl comb_logic_loop_in_data_logic_latch_cscd e Combinationa in data logic cse csa datl find_comb_loop_cscd e Combinationa cse csa datl comb_logic_loop_in_data_logic_latch_cscd e Combinationa in data logic Buffer at cse csa datl find_comb_loop_cscd e Componer combinationa detected white a split vecto part of a com loop. Starting line cse csa datl irregular_latch_in_comp_loop_cscd e Irregular component irregular latch that can b continuous entire cycle.	e @. at line
CSE	
CSE   CSA   CSI   Non-constant file @ at line	ion type @ e @
cse csa datl comb_logic_loop_in_data_logic_cscd e Combinationa in data logic cse csa datl comb_logic_loop_in_data_logic_latch_cscd e Combinationa in data logic Buffer at cse csa datl find_comb_loop_cscd e Component combinationa detected whice a split vector part of a component cse csa datl comp_loop_detected_cscd e Component irregular latch that can be continuous entire cycle. Cese csa datl csp. csp. csa datl csp. csp. csp. csa datl csp. csp. csp. csp. csp. csp. csp. csp.	ion type @ e @
cse csa datl comb_logic_loop_in_data_logic_latch_cscd e Combinationa in data logic Buffer at Componer combinationa detected white a split vector part of a compliance cse csa datl comp_loop_detected_cscd e Componer detected @ st @ at liregular_latch_in_comp_loop_cscd e Irregular component irregular latch that can be continuous entire cycle. Cerebrate in data logic Combinationa data logic Buffer at Componer combinational detected white a split vector part of a compliance component irregular latch that can be continuous entire cycle. Cerebrate component irregular latch.	
cse         csa         datl         comb_logic_loop_in_data_logic_latch_cscd         e         Combinations in data logic. Buffer at Componer combinations detected whice a split vector part of a comploop. Starting line.           cse         csa         datl         comp_loop_detected_cscd         e         componer combinations detected whice a split vector part of a comploop. Starting line.           cse         csa         datl         comp_loop_detected_cscd         e         componer detected @ st @ at lir @ at lir component irregular latch that can be continuous entire cycle. Component irregular latch in continuous entire cycle. Comp	
cse csa datl find_comb_loop_cscd e Componer combinations detected white a split vector part of a com loop. Starting line  cse csa datl comp_loop_detected_cscd e Componer detected @ st @ at lir  cse csa datl irregular_latch_in_comp_loop_cscd e Irregular latch_that can be continuous entire cycle. Component irregular latch_continuous entire cycle. Component combinations detected white a split vector part of a component irregular latch_that can be continuous entire cycle. Component component irregular latch_continuous entire cycle. Component combinations detected white a split vector part of a component irregular_latch_comp_loop_cscd e component irregular_latch_continuous entire cycle. Component irregular_latch_con	al logic loop with Latch
cse csa datl comp_loop_detected_cscd e Component irregular latch that can be continuous entire cycle. Component cycle c	
cse csa datl comp_loop_detected_cscd e Compone detected @ st @ at lir component irregular latch that can b continuous entire cycle. Component irre component irre component irre continuous entire cycle. Component irre component irregular latch that can b continuous entire cycle. Component irregular latch that can b continuous entire cycle.	ch involves
cse csa datl comp_loop_detected_cscd e Compone detected @ st	nbinational
cse csa datl irregular_latch_in_comp_loop_cscd e Irregular component irregular latcl that can b continuous entire cycle. C	
cse csa datl irregular_latch_in_comp_loop_cscd e Irregular latch_in_component irregular latch_in_component irregular latch_in_continuous entire cycle. C	ent loop tarting poir
component irregular latcl that can continuous entire cycle. C	
that can b continuous entire cycle. C	t loop. An
entire cycle. C	oe open
at some point	t be closed
clock cycle. st	tarting poin
Cse csa drvc multiply_drvn_net_nontri_gate_cscs w Multiply driver	nNet driver
by a non-trist	
cse csa drvc multiply_drvn_port_nontri_gate_cscs w Multiply_driver by a non-trist	
cse csa drvc multiply_drvn_sig_nontri_gate_cscs w Multiply driv	@
driven by a n	non-tristate
cse csa drvc incompatible_driver_net_cscs w Incompatible_driver_net_cscs	e driver of
type @ drivi	et of type @
cse csa drvc incompatible_driver_port_cscs w Incompatible	
type @ drivin	ngPort_@
multi drivenP @ name @	at line @
cse csa drvc incompatible_driver_sig_cscs w Incompatible	e driver of gSignal_@

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl Desc
								multi drivenSignal of type @ name @ at line @
cse	csa	expr	unary_op_in_comparison_cscs	е				Unary op used in comparison at line @
cse	csa	expr	miss_parenthesis_cscs	е				Unary op @ with
								comparison op @ missing precedence
cse	csa	init	assn_mem_in_init_blk_cscs	е				parenthesis at line @ Assign memory in initial
cse	csa	inst	input_port_drvn_from_inside_mod_cscs	е				block at line @ Input port @ being drive
								from inside of module @ at line @
cse	csa	inst	input_port_drvn_from_inside_entity_cscs	е				Input port @ being drive from inside of entity @ a
		inat	input part drup from incide signal acco					line @
cse	csa	inst	input_port_drvn_from_inside_signal_cscs	е				from inside of signal @ a
cse	csa	inst	input_port_not_connected_in_parent_mod_cscs	е				line @ Input port @ not
								connected in parent module at line @
cse	csa	inst	input_port_not_connected_in_parent_entity_cscs	е				Input port @ not connected in parent
cse	csa	inst	input port not connected in parent signal cscs	е				entity at line @ Input port @ not
036	USA	iiist	input_port_not_connected_in_parent_signal_cscs					connected in parent
cse	csa	mdb	single_comp_contains_multiple_tri_drv_cscs	w				signal at line @ A single component
								contains multiple tristate drivers at line @
cse	csa	mdb	unsuppexpr_on_lhs_net_drv_stmt_cscs	W				Unsupported Expression type type on LHS ofNet
								driver statement at line @
cse	csa	mdb	unsuppexpr_on_lhs_port_drv_stmt_cscs	w				Unsupported Expression type type on LHS ofPort
								driver statement at line
cse	csa	mdb	unsuppexpr_on_lhs_sig_drv_stmt_cscs	w				@ Unsupported Expression
								type type on LHS ofSignal driver statemen
cse	csa	mdb	tri_not_in_top_mod_cscs	е				at line @ Tristate not in top modul
cse	csa	mdb	tri_not_in_top_ent_cscs	е				at line @ Tristate not in top entity
cse	csa	mdb	tri_not_in_top_sig_cscs	е				at line @ Tristate not in top signa
cse	csa	mdb	tri_primitive_inst_cscs	е				at line @ Tristate primitive
cse	csa	mdb	tri_net_only_one_drvr_cscs	е				instantiation at line @ Tri Net has only one
			,					driver at line @
cse	csa	mdb	tri_port_only_one_drvr_cscs	е				Tri Port has only one driver at line @
cse	csa	mdb	tri_sig_only_one_drvr_cscs	е				Tri Signal has only one driver at line @
cse	csa	mod	redef_mod_cscs	е				Redefined module @ at line @
cse	csa	mod	redef_ent_cscs	е				Redefined entity @ at line @
cse	csa	mod	redef_signal_cscs	е				Redefined signal @ at line @
cse	csa	net	tri_and_net_only_one_driver_cscs	е	?			triandNet @ has only on
cse	csa	net	tri_and_port_only_one_driver_cscs	е	?			driver at line @ triandPort @ has only
cse	csa	net	tri_and_sig_only_one_driver_cscs	е	?			one driver at line @ triandSignal @ has only
cse	csa	net	var_assn_but_never_ref_cscs	е				one driver at line @ Variable @ assigned bu
								never referenced at line @
cse	csa	net	var_never_assn_cscs	е				Variable @ never assigned at line @
cse	csa	net	var_not_assn_in_all_paths_cscs	е				Variable @ not being assigned in all paths at
			was and in such asset					line @
cse	csa	net	var_not_in_snsl_cscs	е				Variable @ not in sensitivity list at line @
cse	csa	net	reg_connected_to_inout_in_inst_cscs	е				Reg @ connected to inout @ in instantiation
cse	csa	net	reg_connectede_to_output_in_inst_cscs	е				@ at line @ Reg @ connected to
								output in instantiation at line @
cse	csa	net	reg_used_as_output_of_cont_assn_cscs	е				Reg @ used as output of continuous assign at line
000	000	net	port_used_prior_to_decl_cscs	е				Port @ used prior
cse	csa	HEL	port_useu_prior_to_udci_cscs	6				toDeclaration at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	csa	parm	redef_param_cscs	е					Redefined parameter @ at line @
cse	csa	pp	redef_macro_cscs	е					Redefined macro @ at line @
cse	csa	prts	vec_index_order_incorrect_cscs	е					Vector index @ order incorrect at line @
cse	csa	prts	vec_index_truncated_cscs	е					Vector index @ truncated at line @
cse	csa	seq	seq_latch_connected_to_latch_in_loop_cscd	е					Latch connected to latch
cse	csa	sply	output_conncet_to_sply_	е					in loop at line @ Output @ connect to
cse	csa	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_cscs	е					supply at line @ Arithmetic operator RHS
									has one less bit than the LHS at line @
cse	csa	stmt	ar_op_unequal_lhs_rhs_cscs	е					Arithmetic operator unequal width LHS and
cse	csa	stmt	ar_op_unequal_var_on_rhs_cscs	е					RHS at line @ Arithmetic operator
000	oou	Ottill	ar_op_arioquar_var_ori_mo_cccc						unequal width variables  @ on RHS at line @
cse	csa	tri	tri_not_in_top_mod_cscs	е					Tristate @ not in top
cse	csa	tri	tri_not_in_top_entity_cscs	е					module at line @ Tristate @ not in top
cse	csa	tri	tri_not_in_top_signal_cscs	е					entity at line @ Tristate @ not in top
cse	csa	tri	tri_prim_ist_cscs	е					signal at line @ Tristate primitive
cse	csb	ase	arch_state_el_mod_not_exist_csbcs	е					instantiation @ at line @ Architectural state
									element @ module @ does not exist at line @
cse	csb	ase	arch_state_el_ent_not_exist_cbcs	е					Architectural state element @ entity @ does
000	csb	ase	arch_state_el_unit_not_exist_csbcs						not exist at line @  Architectural state
cse	CSD	ase	arch_state_ei_unit_not_exist_csbcs	е					element @ unit @ does
cse	csb	ase	arch_state_el_missi_clk_name_csbcs	е					not exist at line @ Architectural state
									element @ is missing the clock name at line @
cse	csb	ase	arch_state_el_miss_mem_name_csbcs	е					Architectural state element @ is missing the
cse	csb	ase	arch_state_el_miss_the_csbcs	е					memory name at line @ Architectural state
									element @ is missing the @ at line @
cse	csb	ase	arch_state_el_miss_rst_name_csbcs	е					Architectural state element @ is missing the
cse	csb	ase	arch_state_el_evtrigg_miss_ev_name_csbcs	е					reset name at line @ Architectural state
000	000	400	arsn_state_sr_svangg_mass_sv_name_sssss						element @ is event triggered and is missing
	aab		arch state at all, name not found ashes						the event name at line @
cse	csb	ase	arch_state_el_clk_name_not_found_csbcs	е					Architectural state element @ clock name
cse	csb	ase	arch_state_el_mem_name_not_found_csbcs	е					@ not found at line @ Architectural state
									element @ memory name @ not found at line
cse	csb	ase	arch_state_el_not_found_csbcs	е					@ Architectural state
									element @ arch_state_name @ not
cse	csb	ase	arch state el rst not found	е					found at line @ Architectural state
									element @ reset name @e not found at line @
cse	csb	assn	x_in_rhs_of_assihnment_csbcs	е					x in rhs of assignment at
cse	csb	assn	z_in_rhs_of_assn_default_csi_csbcs	е					x in rhs of assignement
									in defaultCase item at line @
cse	csb	assn	z_in_rhs_of_assn_csbcs	е					z in rhs of assignement at line @
cse	csb	assn	unequal_length_lhs_rhs_csbcs	е					Unequal length LHS and RHS at line @
cse	csb	assn	unequal_length_lhs_rhs_off_one_bit_csbcs	е					Unequal length LHS and RHS off by one bit at line
cse	csb	ccd	ccd_cdir_must_be_cst_expr_csbcs	е				х	@ CSL directive size must
								•	be constant Expression at line @
cse	csb	ccd	clk_dir_not_applied_to_dsgn_csbcs	w				Х	CSL clock directive not applied to design. Could
000	coh	604	ool filter upuned sehes					v	not find clock at line @
cse	csb	ccd	csl_filter_unused_csbcs	W				Х	CSL message filter @ not found. Filter @ is
cse	csb	ccd	csl_mess_not_filtered_csbcs	w				Х	unused. at line @ CSL message @ can not
									be filtered. Filter @ is

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ve	r Csl	
cse	csb	ccd	error_csdir_not_found_csbcs	е				х	unused. at line @ Error CSL directive @ not found. Error @ is unused. at line @
cse	csb csb	chrs	ill_val_chrs_csb clk_name_not_found_cdir_csbcs	e e				х	Illegal value @ at line @ Clock name not found in
								^	cslc directive at line @
cse	csb	clk	expr_sunj_to_different_clk_phases_csbcs	е					Expression subject to different clock phases at line @
cse	csb	csi	z_csi_not_in_casez_csb	е					z case item not in casez at line @
cse	csb	csi	noncstn_rep_in_conc_csbcs	е					Non-constant repeator in
cse	csb	decl	decl_array_over_max_size_csbcs	е					Array @ exceeds maximum size limit at
cse	csb	dely	x_or_z_in_dely_csbcs	е					line @ x or z in delay at line @
cse	csb	dmsn	mem_prts_index_out_of_range_for_mem_csbcs	е					Memory part select [@:@] index @ out range for memory @ at line @
cse	csb	dmsn	dime_select_for_mem_missing_csbcs	е					Select for memory @ missing at line @
cse	csb	dmsn	dime_index_out_of_bounds_for_mem_csbcs	е					Index <index> out of bounds for memory @.</index>
cse	csb	dmsn	dime_prts_out_of_bounds_for_net_csbcs	е					Range [@: @] at line @ Part select [@: @] out of bounds for net @. Range
cse	csb	dmsn	dime_prts_out_of_bounds_for_port_csbcs	е					[@ : @] at line @ Part select [@ : @] out of bounds for port @. Range [@ : @] at line @
cse	csb	dmsn	dime_prts_out_of_bounds_for_sig_csbcs	е					Part select [@ : @] out of bounds for signal @. Range [@ : @] at line @
cse	csb	dmsn	dime_prts_reg_csbcs	е					Part select [@ : @] reg @. Range [@ : @] at line
cse	csb	drvc	incompatible_drvc_for_net_csbcs	е					Incompatible drivers for
cse	csb	drvc	incompatible_drvc_for_port_csbcs	е					Net @ at line @ Incompatible drivers for
cse	csb	drvc	incompatible_drvc_for_sig_csbcs	е					Port @ at line @ Incompatible drivers for
cse	csb	drvc	drvc_multiple_drive_net_partially_overlap_csbcs	е					Signal @ at line @  Multiple drive Net partially overlap at line @
cse	csb	drvc	drvc_multiple_drive_port_partially_overlap_csbcs	е					Multiple drive Port
cse	csb	drvc	drvc_multiple_drive_sig_partially_overlap_csbcs	е					partially overlap at line @ Multiple drive Signal partially overlap at line @
cse	csb	dsgn	dsgn_top_mod_cannot_id_csbcs	е					Top module @ cannot be identified at line @
cse	csb	dsgn	dsgn_top_entity_cannot_id_csbcs	е					Top entity @ cannot be identified at line @
cse	csb	dsgn	dsgn_top_unit_cannot_id_csbcs	е					Top unit @ cannot be identified at line @
cse	csb	dsgn	unit_dsgn_cycle_not_spanning_tree_csbcs	е					Unit design hierarchy contains a cycle.
									Hierarchy is not a spanning tree. at line @
cse	csb	expr	const_expr_nm_var_cscsb	е					Constant Expression contains variable @ at line @
cse	csb	expr	const_expr_usage_cscsb	е					Constant Expression
cse	csb	expr	expr_prts_indices_1bit_var_csbcs	е					usage at line @ Part select indices 1-bit
cse	csb	expr	expr_prts_must_be_cst_expr_csbcs	е					variable at line @ Part select specifier Expression must be
									constant Expression at line @
cse	csb	expr	not_const_expr_csbcs	е					Repetition multiplier in concatenation is not a constant Expression at
cse	csb	expr	ill_bit_select_expr_csbcs	е					line @ Illegal bit select
cse	csb	expr	repetition_multiplier_in_conc_not_const_expr_csbcs	W					expression @ at line @ Repetition multiplier in concatenation is not a constant Expression at
cse	csb	expr	int_operand_not_1_bit_csbcs	W					line @ Logic operator has integer operands instead of 1-bit operands at line
cse	csb	expr	unsupp_expr_csbcs	w					of 1-bit operands at line @ Unsupported Expression
cse	csb	expr	unsupp_operator_csbcs	W					type @ at line @ Unsupported operator
300	300	-vbi	453pp_operator_00000						type @ at line @

Section   Sect	Cat	Phase csb	<b>Type</b> expr	Name use_of_sg_bit_const_csbcs	W/E	V1995	V2001	Sys_ver	Csl	<b>Desc</b> Use of single bit constant
Case   Cab   Paper   Case   Cab   Case   C	cse	csb	expr	unary op in comparison csbcs	е					
Seb			·	7-1 1 -						comparison at line @ x or z in conditional
Expression @ in module   Expression @ in @ in module   Expression @ in @	cse	csb	expr	zero_in_rep_in_conc_csbcs	е					
Expression @ in ent ent ent ent ent ent ent ent ent en	cse	csb		expr_in_mod_port_dir_csbcs	е					Expression @ in module
Expression   Enumit port   Expression   Expression   Enumit port   dirt it line   Expression   Enumit port   dirt it line   Expression   Enumit port   dirt it line   Expression   Enumit port   Expression   Ex	cse	csb	expr	expr_in_ent_port_dir_csbcs	е					Expression @ in entity
Seb	cse	csb	expr	expr_in_sig_port_dir_csbcs	е					Expression @ in unit port
Expression operator   Expression   Expression operator   Express	cse	csb	expr	expr_in_inst_csbcs	е					Expression @ in inst i@
Length at line @   Cannot open_filter_specification_file_nsbcs   e   Cannot open filter specification_file_nsbcs   e   Cannot open_filter_specification_file_missing_csbcs   e   Cannot open_file_nsine_dsbcs   e   Cannot open_file_nsine_dsbcs   e   Cannot open_file_nsine_dsbcs   e   Filter_specification file_name @ is missing at line @   Mismatch_between mismatch_between file_name @ is missing at line @   Mismatch_between mismatch_site_file_name_csbcs   e   Mismatch_between signal module name @ and file_name @ is mismatch_site_file_name_csbcs   e   Mismatch_between signal name @ and file_name @ and	cse	csb	expr	expr_operator_operands_unequal_lenght_csbcs	е					Expression operator @
See Sb file filter_specification_file_missing_csbcs										
CSB	cse	csb	file	cannot_open_filter_specification_file_csbcs	е					specification file @ at line
See   Cab   file   mismatch_mod_file_name_cabcs   e   mismatch_mod_file_name_cabcs   e   mismatch_ent_file_name_cabcs   e   mismatch_ent_file_name_cabcs   e   mismatch_ent_file_name_cabcs   e   mismatch_ent_file_name_cabcs   e   mismatch_sig_file_name_cabcs	cse	csb	file	filter_specification_file_missing_csbcs	е					Filter specification file
module name @ and file name @ at line @ all file @ and file name @ at line @ all file @ at line @ all file @ at line @ at										line @
Mismatch_ent_file_name_csbcs   e	cse	csb	file	mismatch_mod_file_name_csbcs	е					module name @ and file
	cse	csb	file	mismatch_ent_file_name_csbcs	е					Mismatch between entity
cse csb func func_arg_miss_cscsb e Function call missing arguments) at line @ at line @ func_arg_miss_cscsb e Function call missing arguments) at line @ argument(s) at line @ func_csbcs e Function call missing arguments at line @ func_csbcs e Func func_expr_cannot_expnaded_csbcs e Func func_expr_cannot_expnaded_csbcs e Func func_expr_cannot_expnaded_csbcs e Func func_not_used_in_expr_csbcs w Func func_sbcs e Function expression expression expression expression expression e Function expression e Function expression e										@ at line @
CSB	cse	csb	file	mismatch_sig_file_name_csbcs	е					name @ and file name
CSB   CSB   UIUNC   DOT_IND_LUPL_CSBCS   E   DOT_IND_CSBCS   E	cse	csb	func	func_arg_miss_cscsb	е					Function call missing
CSE   CSB   Tunc   Too_many_arg_to_func_csbcs   e	cse	csb	func	port_not_output_func_csbcs	е					
CSE   CSB   func   Too_few_arg_to_func_csbcs   e   Too few arguments passed to function @ at line @	cse	csb	func	too_many_arg_to_func_csbcs	е					Too many arguments
cse csb func  cs										
CSE         CSB         func         undefined func_csbcs         e         Undefined function @ at line @ cannot be expanded at line @ cannot locate in expression in in the e	cse	csb	func	too_few_arg_to_func_csbcs	е					passed to function @ at
CSE	cse	csb	func	undefined_func_csbcs	е					Undefined function @ at
See   CSb   func   funct_not_used_in_expr_csbcs   w   Function @ Is not being used in an Expression at line @ Is not being used in an Expression at line @ Is not being used in an Expression at line @ Is not being used in an Expression at line @ Is not being used in an Expression at line @ Is not being used in an Expression at line @ Is not being used in an Expression at line @ Is not being used in an Expression at line @ Is not being used in an Expression at line @ Is not being used in an Expression at line @ Is not being used in an Expression at line @ Is not being used in an Expression hid at line @ Is not be used used used used used used used use	cse	csb	func	funct_expr_cannot_expnaded_csbcs	е					Function expression @
cse   csb   func   func_decl_csbcs   w     Function Declaration @ already declared as another type at line @			£	for the state of t						line @
cse         csb         func         function Declaration @ already declaration @ already declared as another type at line @ cannot_locate_hier_id_hid_csbcs         e         Function Declaration @ already declared as another type at line @ can thorate hier pipe at line @ can thora	cse	CSD	tunc	tunct_not_used_in_expr_csbcs	W					used in an Expression at
CSE         cSb         hid         cannot_locate_hier_id_hid_csbcs         e         Can't locate hierarchical identifier @ at line @ identifier @ at line @ instance @ found in an Expression hid at line @ Expression hid at line	cse	csb	func	func_decl_csbcs	w					Function Declaration @
CSE	cse	csb	hid	cannot_locate_hier_id_hid_csbcs	е					Can't locate hierarchical
Expression hid at line @ References a entity instance @ found in an Expression hid at line @ References a entity instance @ found in an Expression hid at line @ References a unit instance @ found in an Expression hid at line @ References a unit instance @ found in an Expression hid at line @ References a unit instance @ found in an Expression hid at line @ @ reference not found at line @ @ Module instance @ in hid does not exist at line @	cse	csb	hid	ref_minst_found_in_expr_hid_csbcs	е					References a module
cse csb hid ref_unit_found_in_expr_hid_csbcs e References a unit instance @ found in an Expression hid at line @ References a unit instance @ found in an Expression hid at line @ @ reference not found at line @ Module instance @ in hid does not exist at line @ does not exist at line @ Entity instance @ in hid does not exist at line @ Entity instance @ in hid does not exist at line @ Unit instance @ in hid does not exist at line @ Unit instance @ in hid does not exist at line @ Unit instance @ in hid does not exist at line @ Unit instance @ in hid does not exist at line @ Entity instance @ in hid does not exist at line @ Unit instance @ in hid does not exist at line @ Entity instance @ in hid does not exist at line @ Unit instance @ in hid does not exist at line @ Entity @ found in path @ in the design at line @										
CSE   CSB   hid   ref_unit_found_in_expr_hid_csbcs   e     References a unit instance @ found in an Expression hid at line @   Preference not found at line @   Pre	cse	csb	hid	ref_entity_found_in_expr_hid_csbcs	е					
instance @ found in an Expression hid at line @ @ reference not found at line @ @ Gese	CSE	csh	hid	ref unit found in expr hid cshos	P					
cse       csb       hid       hid_reference_not_found_csbcs       e       @ reference not found at line @         cse       csb       hid       mifc_in_hid_not_exist_csbcs       e       Module instance @ in hid does not exist at line @         cse       csb       hid       entity_instance_in_hid_not_exist_csbcs       e       Entity instance @ in hid does not exist at line @         cse       csb       hid       unit_instance_in_hid_not_exist_csbcs       e       Unit instance @ in hid does not exist at line @         cse       csb       hid       mod_found_in_path_in_dsgn_csbcs       e       Module @ found in path @         cse       csb       hid       enity_found_in_path_in_dsgn_csbcs       e       Enity @ found in path @         cse       csb       hid       unit_found_in_path_in_dsgn_csbcs       e       Unit @ found in path @         cse       csb       hid       unit_found_in_path_in_dsgn_csbcs       e       Unit @ found in path @         cse       csb       hid       hierarchical_id_path_contains_func_csb       e       Hierarchical ID @ path contains a function at line @         cse       csb       init       assn_mem_in_init_blk_csbcs       e       Duplicate port @ in the port list for module @ at line @         cse       csb       inst       inst_dupl		002		. oaoaaopa_oosoo						instance @ found in an
cse       csb       hid       mifc_in_hid_not_exist_csbcs       e       Module instance @ in hid does not exist at line @         cse       csb       hid       entity_instance_in_hid_not_exist_csbcs       e       Entity instance @ in hid does not exist at line @         cse       csb       hid       unit_instance_in_hid_not_exist_csbcs       e       Unit instance @ in hid does not exist at line @         cse       csb       hid       mod_found_in_path_in_dsgn_csbcs       e       Module @ found in path @ in the design at line @         cse       csb       hid       enity_found_in_path_in_dsgn_csbcs       e       Entity @ found in path @ in the design at line @         cse       csb       hid       unit_found_in_path_in_dsgn_csbcs       e       Unit @ found in path @ in the design at line @         cse       csb       hid       hierarchical_id_path_contains_func_csb       e       Hierarchical ID @ path contains a function at line @         cse       csb       init       assn_mem_in_init_blk_csbcs       e       Assign memory in initial block at line @         cse       csb       inst       inst_duplicate_mod_name_csbcs       e       Duplicate port @ in the port @	cse	csb	hid	hid_reference_not_found_csbcs	е					@ reference not found at
cse       csb       hid       entity_instance_in_hid_not_exist_csbcs       e       Entity instance @ in hid does not exist at line @ Unit instance @ in hid does not exist at line @ Unit instance @ in hid does not exist at line @ Unit instance @ in hid does not exist at line @ Winth does not exist at line @ Module @ found in path @ in the design at line @ in the design at line @ Entity @ found in path @ in the design at line @ in the design at line @ in the design at line @ Winth design at line Winth design a	cse	csb	hid	mifc_in_hid_not_exist_csbcs	е					Module instance @ in hid
cse       csb       hid       unit_instance_in_hid_not_exist_csbcs       e       Unit instance @ in hid does not exist at line @ Module @ found in path @ in the design at line @ in the design at line @ Entity @ found in path @ in the design at line @ in the design at line @ in the design at line @ Entity @ found in path @ in the design at line @ Unit @ found in path @ in the design at line @ Entity @ found in path @ in the design at line @ Unit @ found in path @ in the design at line @ Entity @	cse	csb	hid	entity_instance_in_hid_not_exist_csbcs	е					Entity instance @ in hid
cse       csb       hid       mod_found_in_path_in_dsgn_csbcs       e       Module @ found in path @ in the design at line @ Entity @ found in path @ in the design at line @ in the design at lin	cse	csb	hid	unit_instance_in_hid_not_exist_csbcs	е					Unit instance @ in hid
cse       csb       hid       enity_found_in_path_in_dsgn_csbcs       e       Entity @ found in path @ in the design at line @ Unit @ found in path @ in the design at line @ In the In the line In the line @ In the In the line In the	cse	csb	hid	mod_found_in_path_in_dsgn_csbcs	е					Module @ found in path
cse     csb     hid     unit_found_in_path_in_dsgn_csbcs     e     Unit @ found in path @ in the design at line @ in the design at line @ in the design at line @       cse     csb     hid     hierarchical_id_path_contains_func_csb     e     Hierarchical ID @ path contains a function at line @ in the path is function at line @       cse     csb     init     assn_mem_in_init_blk_csbcs     e     Assign memory in initial block at line @ in the port list for module @ at line @       cse     csb     inst     inst_duplicate_mod_name_csbcs     e     Duplicate port @ in the port list for module @ at line @       cse     csb     inst     inst_duplicate_entity_name_csbcs     e     Duplicate port @ in the	cse	csb	hid	enity_found_in_path_in_dsgn_csbcs	е					Entity @ found in path @
cse     csb     hid     hierarchical_id_path_contains_func_csb     e     Hierarchical_ID @ path contains a function at line @       cse     csb     init     assn_mem_in_init_blk_csbcs     e     Assign memory in initial block at line @       cse     csb     inst     inst_duplicate_mod_name_csbcs     e     Duplicate port @ in the port list for module @ at line @       cse     csb     inst     inst_duplicate_entity_name_csbcs     e     Duplicate port @ in the port list for module @ at line @	cse	csb	hid	unit_found_in_path_in_dsgn_csbcs	е					Unit @ found in path @
cse csb init assn_mem_in_init_blk_csbcs e Assign memory in initial block at line @  cse csb inst inst_duplicate_mod_name_csbcs e Duplicate port @ in the port list for module @ at line @  cse csb inst inst_duplicate_entity_name_csbcs e Duplicate port @ in the	cse	csb	hid	hierarchical_id_path_contains_func_csb	е					Hierarchical ID @ path
cse csb inst inst_duplicate_mod_name_csbcs e Duplicate port @ in the port list for module @ at line @  cse csb inst inst_duplicate_entity_name_csbcs e Duplicate port @ in the port list for module @ at line @  cse csb inst inst_duplicate_entity_name_csbcs e Duplicate port @ in the	000	och	in is	goon mam in this blue caboo						@
cse csb inst inst_duplicate_entity_name_csbcs e port list for module @ at line @  Duplicate port @ in the										block at line @
cse csb inst inst_duplicate_entity_name_csbcs e Duplicate port @ in the	cse	CSD	ınst	inst_aupilcate_mod_name_csbcs	е					port list for module @ at
	cse	csb	inst	inst_duplicate_entity_name_csbcs	е					

Cat	Phase	Туре	Name	W/E V19	95 V2001 Sys_ver	Csl Desc
cse	csb	inst	inst_duplicate_unit_name_csbcs	е		Duplicate port @ in the port list for unit @ at line @
cse	csb	inst	ill_mod_inst_name_csbcs	е		Illegal module instance @ at line @
cse	csb	inst	ill_entity_inst_name_csbcs	е		Illegal entity instance @ at line @
cse	csb	inst	ill_unit_inst_name_csbcs	е		Illegal unit instance @ at line @
cse	csb	inst	inst_name_defined_mod_csbc	е		Instance name @ already defined in this module at line @
cse	csb	inst	inst_name_defined_ent_csbc	е		Instance name @ already defined in this entity at line @
cse	csb	inst	inst_name_defined_unit_csbc	е		Instance name @ already defined in this unit at line @
cse	csb	inst	inst_too_many_bits_csbcs	е		Too many bits for port @ of instance array @, formal @, actual @ at
cse	csb	inst	inst_port_not_connected_var_csbcs	е		line @  Port 'port' of instance array 'array' is not connected to variable at line @
cse	csb	inst	inst_insufficient_bits_csbcs	е		Insufficient bits for port 'port' of instance array 'array ', formal number,
cse	csb	inst	inst_mod_name_not_defined_csbcs	е		actual number at line @ Module name not defined at line @
cse	csb	inst	inst_ent_name_not_defined_csbcs	е		Entity name not defined at line @
cse	csb	inst	inst_unit_name_not_defined_csbcs	е		Unit name not defined at line @
cse	csb	inst	many_mod_inst_param_assign_csbcs	е		Too many module instance parameter assignments (number >
cse	csb	inst	many_entity_inst_param_assign_csbcs	е		rrumber) at line @ Too many entity instance parameter assignments (number > rrumber) at line @
cse	csb	inst	many_unit_inst_param_assign_csbcs	е		Too many unit instance parameter assignments (number > rrumber) at line @
cse	csb	inst	complexexpr_cannot_mapped_inout_port_csbcs	е		Complex Expression @ cannot be mapped to inout port @ at line @
cse	csb	inst	complexexpr_cannot_mapped_unknown_port_csbcs	е		Complex Expression @ cannot be mapped to unknown type port @ at line @
cse	csb	inst	netdecl_contains_ill_prts_csbcs	е		Net Declaration [@: @] contains an illegal part select at line @
cse	csb	inst	regdecl_contains_ill_prts_csbcs	е		Reg Declaration [@ : @] contains an illegal part select at line @
cse	csb	inst	complex_expr_inst_parent_module_csbcs	е		Complex actual Expression associated with port @ of module @ instantiated in parent module at line @
cse	csb	inst	complex_expr_inst_entity_parent_module_csbcs	е		Complex actual Expression associated with port @ of entity @ instantiated in parent module at line @
cse	csb	inst	complex_expr_inst_unit_parent_module_csbcs	е		Complex actual Expression associated with port @ of unit @ instantiated in parent module at line @
cse	csb	inst	inst_mod_output_port_width_csbcs	е		Mod @ Output port @ width mismatch, actual-width ( port-width ) at line @
cse	csb	inst	inst_entity_output_port_width_csbcs	е		Entity @ Output port @ width mismatch, actual-width ( port-width ) at line @
cse	csb	inst	inst_unit_output_port_width_csbcs	е		Unit @ Output port @ width mismatch, actual-width ( port-width ) at line @
cse	csb	inst	inst_mod_input_port_width_csbcs	е		Mod @ Input port @ width mismatch,

see csb inst inst_entity_input_port_width_csbcs e	cse cse cse cse cse	csb	inst			V 1333	V2001	Cy3_VCI	031	actual-width ( port-width ) at line @
width mismate   cse   csb   inst   inst_unit_input_port_width_csbcs   e   Und @ input port_actual file @   Cse   csb   inst   inst_mod_not_define_csbcs   e   Module not define   csbcs   e   Entity not defined   csbcs   e   Entity e   csbc	cse cse cse cse	csb		inst_entity_input_port_width_csbcs	е					F 44 O 1
CSB   CSB   Inst   Inst_unit_input_port_width_csbcs   e   Unit @ Input_port_width (psbcs   unit @ Input_port_width (psbcs   e   unit @ Input_port_width (psbcs   csb   inst   inst_unit_input_port_width_csbcs   e   Module not define   Inst_unit_input_port_width_csbcs   e   Entity not defined_ins @ Inst_unit_inst_un	cse cse cse		inst							Entity @ Input port @
CSE   CSB   Inst   Inst_unit_input_port_width_csbcs   e     Unit @ Input port_statile width (part-statile width (part-statile)	cse cse cse		inst							actual-width ( port-width )
CSE   CSB   Inst   Inst_mod_not_define_csbcs   e   Module not define   CSE   CSE   Inst   Inst_entity_not_define_csbcs   e   Entity not defined   Entity not defined   CSE   CSE   Inst   Inst_unit_not_define_csbcs   e   Unit not defined   CSE   CSE   CSE   Inst   Inst_unit_not_define_csbcs   e   Unit not defined   CSE   CSE   CSE   Inst   Inst_unit_not_define_csbcs   w   Module @Instance   Pot   Width mism   Actual width @Instance   CSE   CSE   Inst   Entity @Instance   Width mismate   Entity @Instance   Width mismate   Entity @Instance   Width @Instance   Width mismate   Unit @Instance   Width @Instance   Width mismate   Unit @Instance   Width mismate   Unit @Instance   Width mismate   Unit @Instance   Width mismate   Unit @Instance   Width @Instance   Width mismate   Unit @Instance   Width @Instance	cse cse cse	csb		inst_unit_input_port_width_csbcs	е					Unit @ Input port @
cse csb inst inst_mod_not_define_csbcs e	cse cse cse	csb								width mismatch,
Ine @   Ine @   Entry not defined.csbcs   Entry not defined.csbc   Unit not defined at   Module @ Instance   Module @ Instan	cse cse cse	csb								at line @
CSe   CSb   Inst   Inst_unit_not_define_csbcs   e   Unit not defined   Module @ Instanctual width @ Inst	cse cse									
CSE   CSB   Inst   mifc_port_actual_formal_width_mismatch_csbcs   w	cse	csb	inst	inst_entity_not_define_csbcs	е					
cse csb inst ent_port_actual_formal_width_mismatch_csbcs w  cse csb inst ent_port_actual_formal_width_mismatch_csbcs w  cse csb inst unit_port_actual_formal_width_mismatch_csbcs w  cse csb inst unit_port_actual_formal_width_mismatch_csbcs w  cse csb inst unit_port_actual_formal_width_mismatch_csbcs w  cse csb inst inst_differs_in_case_from_mod_csbcs e  cse csb inst inst_differs_in_case_from_ent_csbcs e  cse csb inst inst_differs_in_case_from_sig_csbcs e  cse csb inst inst_differs_in_case_from_sig_csbcs e  cse csb loop undet_init_value_loop_csbcs e  cse csb loop loop_bounds_calculated_init_csbcs  cse csb loop loop_bounds_calculated_init_csbcs  cse csb loop loop_bounds_calculated_init_csbcs  cse csb loop loop_bounds_not_const_csbc w  cse csb loop loop_bounds_not_const_csbc w  cse csb loop loop_ctri_init_expr_not_const_csbc w  cse csb loop loop_term_expr_not_const_csbc w  cse csb loop loop_term_expr_not_const_csbcs w  cse csb loop loop_term_expr_not_const_csbcs w  cse csb loop loop_ctri_var_1_bit_wide_csbcs  cse csb loop loop_ctri_var_1_bit_wide_csbcs  cse csb mdb bad_mdb_port_csbcs e  cse csb mdb bad_mdb_signal_csbcs e  cse csb mdb bad_mdb_signal_csbcs  cse csb mdb bad_mdb_signal_csbcs  cse csb mdb bad_mdb_signal_csbcs  cse csb mdb bad_mdb_signal_csbcs  cse csb mdb called bad_mdb_met_csbcs  cse csb mdb called bad_mdb_met_										Unit not defined at line @
CSE	cse	CSD	inst	mirc_port_actual_formal_widtn_mismatcn_csbcs	W					port @ width mismatch, actual width @ formal
CSE   CSD   Inst   Unit_port_actual_formal_width_mismatch_csbcs   W   Unit_port_actual_formal_width_mismatch_csbcs   W   Unit_port_actual_formal_width_mismatch_csbcs   Unit_port_actual_formal_for	cse									width @ at line @
actual width @ for width @ altine @ width @ altine @ width @ altine @ width mismate.  CSE cSb inst inst_differs_in_case_from_mod_csbcs e inst_case_from_ent_csbcs e inst_case_from_ent_ent_csbcs e inst_case_from_ent_ent_csbcs e inst_case_from_ent_csbcs e inst_case_from_ent_csbcs e inst_case_from_ent_ent_csbcs e inst_case_from_ent_csbcs e inst_case_from_ent_csbcs e incase_from_ent_ent_csbcs e inst_case_from_ent_ent_csbcs e inst_case_from_ent_csbcs e inst_case_from_ent_ent_csbcs e incase_from_ent_ent_csbcs e inst_case_from_ent_ent_csbcs e inst_		CSD	inst	ent_port_actual_formal_width_mismatch_csbcs	W					@ width mismatch,
CSE										actual width @ formal
cse csb inst inst_differs_in_case_from_mod_csbcs e instance name @ at line @	cse	csb	inst	unit_port_actual_formal_width_mismatch_csbcs	W					Unit @ instance @ port
width @ at line   linstance name @ in case from mon name @ at line   linstance name @ in case from mon name @ at line @ in case from mon name @ at line @ in case from entity   @ in case from entity   @ in case from entity   @ at line @ in case from signal   @ at line @ at lin										@ width mismatch,
cse csb inst inst_differs_in_case_from_ent_csbcs e inst_case_from_ent_csbcs e inst_case_from_ent_csbcs e inst_case_from_ent_csbcs e inst_case_from_ent_csbcs e inst_case_from_ent_csbcs e inst_case_from_sig_csbcs e inst_case_from_sig_csbcs e inst_case_from_sig_csbcs e inst_case_from_sig_csbcs e inst_case_from_sig_csbcs e inst_case_from_sig_csbcs e inst_case_from_sig_a_le_case_from_sig_a_le_case_from_sig_a_le_case_from_sig_csbcs e inst_case_from_sig_a_le_case_from_sig_csbcs e inst_case_from_sig_a_le_case_from_sig_csbcs e inst_case_from_sig_csbcs in case_from_sig_csbcs										width @ at line @
name @ at line @ cse   csb   inst   inst_differs_in_case_from_ent_csbcs   e	cse	csb	inst	inst_differs_in_case_from_mod_csbcs	е					Instance name @ differs
cse csb inst inst_differs_in_case_from_sig_csbcs e linstance name @ in case from entity @ at line @ in case from signal @ at line @ in case from signal @ at line @ in case from signal @ at line @										name @ at line @
CSB   Inst   Inst_differs_in_case_from_sig_csbcs   e   Instance name @ in case from signal @ at line @ csb   Instance name @ in case from signal @ at line @ csb   Incase from signal @ at line @ csb   Incase from signal walue for loop at Instance name @ in case from signal @ at line @ csb   Incase from signal   Incase fro	cse	csb	inst	inst_differs_in_case_from_ent_csbcs	е					Instance name @ differs
cse   csb   loop   undet_init_value_loop_csbcs   e   Unable to determing value for loop at line @ cse   csb   loop   undet_limit_loop_csbcs   e   Unable to determing value for loop at line @ cse   csb   loop   loop_bounds_calculated_int_csbcs   w   Loop bounds a calculated to be in @, check that the correct at line   cse   csb   loop   expr_lhs_contains_var_bit_select_csbcs   w   Expression in Interpretation of the correct at line   cse   csb   loop   loop_bounds_not_const_csb   w   Loop bounds a signant contains_variable bit select.    cse   csb   loop   loop_bounds_not_const_csb   w   Loop bounds a non-constant at line constant Expression in Interpretation of the contains_variable initialization of the contains_variable at line   cse   csb   loop   loop_tri_var_1_bit_wide_csbcs   e   w   cs   csb   w   csb   csb   w										@ at line @
CSB	cse	csb	inst	inst_differs_in_case_from_sig_csbcs	е					Instance name @ differs
CSB										@ at line @
CSE	cse	csb	loop	undet_init_value_loop_csbcs	е					Unable to determine init
CSE	cse	csb	loop	undet_limit_loop_csbcs	е					Unable to determine limit
cse csb loop expr_lhs_contains_var_bit_select_csbcs w Expression in he assignment contains_var_abit_select_csbcs w Expression in he assignment contains_var_abit_select_csbcs w Expression in he assignment contains_var_abit_bit select is expression.  cse csb loop loop_bounds_not_const_csb w Loop bounds a non-constant at his condition to poor variable initializate. Expression is not constant Expression in he constant Expression is not constant Expression in expression could of evaluated to a cornic at his expression could of evaluated to a cornic at his expression rese variable at line. Cse csb loop loop_ctrl_var_1_bit_wide_csbcs w The loop control variable at line. Cse csb mdb bad_mdb_net_csbcs e Bad multi-driven New at line. Cse csb mdb bad_mdb_port_csbcs e Bad multi-driven Step at line. Cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Step at line. Cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Step at line. Cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Step at line. Cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Step at line. Cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Step at line. Cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Step at line. Cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Step at line. Cse csb mdb bad_mdb_signal_csbcs	CSE	csh	loon	loop bounds calculated int csbcs	w					for loop at line @
cse csb loop expr_lhs_contains_var_bit_select_csbcs w Expression in Ih assignment contains_variable bit select in assignment contains_variable bit select in assignment contains_variable bit select in a sasignment contains_variable at line a sasignment contains_variable at line a sasignment.  In a sasignment contains_variable at line a sasignment contains_variable at line a sasignment.  In a sasignment contains_variable at line a sasignment.  In a sasignment contains_		000	юор	loop_sounds_oundated_int_coses	"					calculated to be integer
CSE										
cse csb loop loop_bounds_not_const_csb w Loop bounds a non-constant at lin @ cse csb loop loop_ctrl_init_expr_not_const_csbcs w Non-constant to bound. Loop corvariable initializate Expression is not constant Expression is not constant Expression is not constant Expression is not constant Expression could nevaluated to a corvat line @ cse csb loop loop_ctrl_var_1_bit_wide_csbcs w Non-constant loop bound. loop terming Expression could nevaluated to a corvat line @ cse csb loop loop_ctrl_var_1_bit_wide_csbcs w Non-constant loop bound. loop terming Expression could nevaluated to a corvat line @ cse csb mdb bad_mdb_net_csbcs w Bad multi-driven S S B B Bad multi-driven S S B B B B B B B B B B B B B B B B B	cse	csb	loop	expr_lhs_contains_var_bit_select_csbcs	w					Expression in Ihs of
cse csb loop loop_bounds_not_const_csb w Loop bounds a non-constant at lit lit cse csb loop loop_ctrl_init_expr_not_const_csbcs w Non-constant til cbound. Loop cor variable initializate Expression is not constant Expression is not constant Expression is not constant Expression is not constant Expression in constant Expression is not constant Expression in constant Expression could revaluated to a correct at line @ cse csb loop init_expr_reset_by_var_csbcs e Non-constant Ic bound. Initializite Expression reservariable at line cse csb loop loop_ctrl_var_1_bit_wide_csbcs w The loop control var_display is one bit wide, the loop control var_display is one bit wide, the loop control var_display is one bit wide. See csb mdb bad_mdb_net_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Pat line @ cse csb mdb line pat line @ cse csb mdb line pat line @ cse csb mdb line p										assignment contains a variable bit select at line
cse csb loop loop_ctrl_init_expr_not_const_csbcs w loop_ctrl_init_expr_not_const_csbcs w loop constant at lince @ constant texpression is not constant texpression is not constant texpression is not constant Expression could repression could revaluated to a cornic at lince @ cse csb loop init_expr_reset_by_var_csbcs e loop loop_ctrl_var_1_bit_wide_csbcs w loop_ctrl_var_1_bit_wide_csbcs w loop_ctrl_var_1_bit_wide_csbcs w loop_control var_decorption is not constant texpression could revaluated to a cornic loop_control var_decorption in the loop control var_decorption is not constant texpression could revaluated to a cornic loop_control var_decorption in the loop control va				land have de not somet sole						@
bound. Loop cor variable initializa Expression is not constant Expression in each count. I loop terming Expression could revaluated to a cor at line @ cse csb loop init_expr_reset_by_var_csbcs e Non-constant in bound. Initializing Expression rese variable at line cse csb loop loop_ctrl_var_1_bit_wide_csbcs w The loop control var_0 is one bit wide. If the loop control var_1 is one bit wide. If the loop control var_1 is one cse csb mdb bad_mdb_net_csbcs e Bad multi-driven Pat line @ cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven Sad mu	cse	CSD	юор	loop_bounds_not_const_csb	W					non-constant at line @
cse csb loop loop_term_expr_not_const_csbcs w Non-constant Expression could in Expression could in evaluated to a cor at line @  cse csb loop init_expr_reset_by_var_csbcs e Non-constant lo bound. loop terming Expression could in evaluated to a cor at line @  cse csb loop init_expr_reset_by_var_csbcs e Non-constant lo bound. initializing Expression reservariable at line @  cse csb loop loop_ctrl_var_1_bit_wide_csbcs w The loop control var_@ is one bit wide. If the loop control var_derivar_ise in the loop control var_derivar_ise i	cse	csb	loop	loop_ctrl_init_expr_not_const_csbcs	W					Non-constant loop
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CSE										Expression is not a constant Expression at
bound. loop termir Expression could revaluated to a cor at line @  cse csb loop init_expr_reset_by_var_csbcs e  Some csb loop loop_ctrl_var_1_bit_wide_csbcs w  Cse csb loop loop_ctrl_var_1_bit_wide_csbcs w  Cse csb mdb bad_mdb_net_csbcs e  Cse csb mdb bad_mdb_port_csbcs e  Cse csb mdb bad_mdb_port_csbcs e  Cse csb mdb bad_mdb_port_csbcs e  Cse csb mdb bad_mdb_signal_csbcs e  Cse csb mdb bad_mdb_signal_csbcs e  Bad multi-driven N  at line @  Cse csb mdb bad_mdb_signal_csbcs e  Bad multi-driven S										line @
cse csb loop init_expr_reset_by_var_csbcs e Non-constant lo bound. initializi Expression rese variable at line  cse csb loop loop_ctrl_var_1_bit_wide_csbcs w The loop control var_displayed bad_mdb_net_csbcs e Bad multi-driven Nat line @  cse csb mdb bad_mdb_port_csbcs e Bad multi-driven Sad mul	cse	CSD	юор	loop_term_expr_not_const_csbcs	W					bound. loop terminating
cse csb loop init_expr_reset_by_var_csbcs e Non-constant lc bound. initializi Expression rese variable at line  cse csb loop loop_ctrl_var_1_bit_wide_csbcs w The loop control var_0 is one bit wide. If the loop control var_1 is one bit wide. If the loop control var_2 is one bit wide. If the loop control var_3 is one bit wide. If the loop control var_4 is one bit wide. If the loop control var_4 is one bit wide. If the loop control var_4 is one bit wide. If the loop control var_4 is one bit wide. If the loop control var_4 is one bit wide. If the loop control var_4 is one bit wide. If the loop control var_4 is one bit wide. If the loop control var_6 is one bit wide.										Expression could not be
bound. initializi Expression rese variable at line  cse csb loop loop_ctrl_var_1_bit_wide_csbcs w  The loop control va @ is one bit wide. the loop control va Declaration. at line  cse csb mdb bad_mdb_net_csbcs e  cse csb mdb bad_mdb_port_csbcs  Bad multi-driven N at line @ cse csb mdb bad_mdb_signal_csbcs e  Bad multi-driven S										at line @
Expression rese variable at line  CSE CSB loop loop_ctrl_var_1_bit_wide_csbcs W The loop control var @ is one bit wide. ( the loop control var Declaration. at line  CSE CSB mdb bad_mdb_net_csbcs e Bad multi-driven N at line @  CSE CSB mdb bad_mdb_port_csbcs e Bad multi-driven P at line @  CSE CSB mdb bad_mdb_signal_csbcs e Bad multi-driven S	cse	csb	loop	init_expr_reset_by_var_csbcs	е					Non-constant loop
cse     csb     loop     loop_ctrl_var_1_bit_wide_csbcs     w     The loop control vare @ is one bit wide. If the loop control vare with the loop control vare pectaration, at line one pectaration. The loop control vare with the loop control vare pectaration. The loop control vare with the loop control vare pectaration. The loop control vare with the loop control										Expression reset by
© is one bit wide. If the loop control vander of	cse	csb	loop	loop ctrl var 1 bit wide csbcs	w					variable at line @ The loop control variable
Declaration. at lin										@ is one bit wide. Check
cse         csb         mdb         bad_mdb_port_csbcs         e         Bad multi-driven P at line @           cse         csb         mdb         bad_mdb_signal_csbcs         e         Bad multi-driven S										Declaration. at line @
cse     csb     mdb     bad_mdb_port_csbcs     e     Bad multi-driven P at line @       cse     csb     mdb     bad_mdb_signal_csbcs     e     Bad multi-driven S	cse	csb	mdb	bad_mdb_net_csbcs	е					Bad multi-driven Net @
cse csb mdb bad_mdb_signal_csbcs e Bad multi-driven S	cse	csb	mdb	bad_mdb_port_csbcs	е					Bad multi-driven Port @
	cse	csb	mdb	bad_mdb_signal_csbcs	е					Bad multi-driven Signal
	cse	csb	mdb	unsupp_comp_mdb_net csbcs	е	?				@ at line @ Unsupported component
type @ driving				,, = , =						type @ driving in
multi-driven Net na										multi-driven Net name at line @
	cse	csb	mdb	unsupp_comp_mdb_port_csbcs	е	?				Unsupported component type @ driving in
multi-driven Port na										multi-driven Port name at
line @ cse csb mdb unsupp_comp_mdb_signal_csbcs e ? Unsupported comp	CSC	ceh	mdh	unsunn comn mah sianal cehes	6	2				line @ Unsupported component
type @ driving	use	CSD	mub	unsupp_comp_mab_signal_csbcs	е	,				type @ driving in
multi-driven Signal at line @										multi-driven Signal name at line @
cse csb mdb unsupp_comp_drive_mdb_csbcs e ? Unsupported comp	cse	csb	mdb	unsupp_comp_drive_mdb_csbcs	е	?				Unsupported component
	n									type @ driving multi-driven Net natne at
multi-driven Net na										line @

cse	Phase csb	Type mdb	Name unsupp_comp_drive_mdb_port_csbcs	W/E e	V1995	V2001	Sys_ver	Csl	Desc Unsupported component
000	000	mab	andapp_domp_anvo_mab_port_dobbd						type @ driving
									multi-driven Port natne at line @
cse	csb	mdb	unsupp_comp_drive_mdb_signal_csbcs	е	?				Unsupported component
									type @ driving
									multi-driven Signal natne at line @
cse	csb	mdb	mdb_net_driven_by_trns_csbcs	е					Multiply driven Net driven
			·						by transistor primitive
cse	csb	mdb	mdb_port_driven_by_trns_csbcs	е					type @ at line @ Multiply driven Port
000	000	mab	mas_port_anvort_sy_ana_cosses						driven by transistor
									primitive type @ at line @
cse	csb	mdb	mdb_sig_driven_by_trns_csbcs	е					Multiply driven Signal
									driven by transistor
									primitive type @ at line @
cse	csb	mdb	mdb_unsupp_comp_drvs_net_csbcs	е					Unsupported component
									type driving Net drives
									Net connected to multi-driven Net at line @
cse	csb	mdb	mdb_unsupp_comp_drvs_port_csbcs	е					Unsupported component
									type driving Port drives Port connected to
									multi-driven Port at line
									@
cse	csb	mdb	mdb_unsupp_comp_drvs_sig_csbcs	е					Unsupported component type driving Signal drives
									Signal connected to
									multi-driven Signal at line
cse	csb	mdb	mdb incompatible net drives multiple net csbcs	е					@ Incompatible driver
000	000		asespassee						driving tandem Net
									drives Net connected to
cse	csb	mdb	mdb_incompatible_port_drives_multiple_port_csbcs	е					multi-driven Net at line @ Incompatible driver
									driving tandem Port
									drives Port connected to multi-driven Port at line
									@
cse	csb	mdb	mdb_incompatible_sig_drives_multiple_sig_csbcs	е					Incompatible driver
									driving tandem Net drives Net connected to
									multi-driven Port at line
cse	csb	mdb	mdb_unsupp_LHS_concatenation_csbcs	е					@ Unsupported LHS
CSE	CSD	mub	mub_unsupp_tro_concatenation_csbcs	6					concatenation in
									multi-drive 'device at line
cse	csb	mdb	mdb_bus_has_too_many_drivers_csbcs	е					@ Bus has too many
									drivers. at line @
cse	csb	mdb	mdb_always_blk_drive_csbcs	W					Multiple always blocks drive name @ at line @
cse	csb	mdb	nontri_gate_drives_mdb_net_csbcs	W					non-tri-state gate drives
			and the second s						multi-driven Net at line @
cse	csb	mdb	nontri_gate_drives_mdb_port_csbcs	w					non-tri-state gate drives multi-driven Port at line
									@
cse	csb	mdb	nontri_gate_drives_mdb_sig_csbcs	W					non-tri-state gate drives multi-driven Signal at line
									@
cse	csb	mem	mem_ref_without_index_csbcs	е					Memory @ referenced
									without index through hierarchical ID @ at line
									@
cse	csb csb	mifc mifc	port_identifier_mifc_csbcs mod_output_wire_redecl_reg_csbcs	е					Port @ at line @ Module @ output port
cse	USD	HIIIC	mou_output_wire_redect_feg_cspcs	е					re-declared as type reg
									after use as implicitly
cse	csb	mifc	entity_output_wire_redecl_reg_csbcs	е					declared wire at line @ Entity @ output port
556	555		oning_odiput_wilo_rodool_reg_odbod	5					re-declared as type reg
									after use as implicitly
cse	csb	mifc	unit_output_wire_redecl_reg_csbcs	е					declared wire at line @ Unit @ output port
550	335		a53.pa5_,5000i_,10g_50000						re-declared as type reg
									after use as implicitly
cse	csb	mifc	output_port_is_mem_type_mifc_csbcs	е					declared wire at line @ Output port @ is memory
									type at line @
cse	csb	mifc	mifc_inout_port_is_mem_type_csbcs	е					Inout port @ is memory
cse	csb	mifc	mod_output_port_mismatch_actual_witdh_csbcs	w					type at line @ Module @ output port @
									formal to actual width
cse	csb	mifc	ent_output_port_mismatch_actual_witdh_csbcs	w					mismatch at line @ Entity @ output port @
USE	OOD		S.Ioutput_port_mismaton_actual_wituri_csbcs	VV					formal to actual width
		- "							mismatch at line @
cse	csb	mifc	unit_output_port_mismatch_actual_witdh_csb	W					Unit @ output port @

Cat	Phase	Туре	Name	W/E	V1995   V2001   Sys_ver	Csl Desc
Cat	riiase	Type	Name	VV/L	V1993 V2001 3ys_vei	formal to actual width
cse	csb	mifc	port_name_different_in_upper_lower_case_csbcs	е		mismatch at line @ Port name @ different in
030	CSD	TIME	port_name_dinerent_in_upper_lower_case_csbcs			upper lower case at line
cse	csb	mifc	port_not_def_in_iodecl_csbcs	е		@ Port @ not defined in
030			. – – – –	6		ioDeclaration at line @
cse	csb	mifc	port_not_def_in_portl_csbcs	е		Port @ not defined in port list at line @
cse	csb	mifc	port_wiredecl_mismatch_csbcs	е		Port @ wireDeclaration
cse	csb	mifc	pos_based_null_inst_port_csbcs	е		mismatch at line @ Position based null
030			. – – – –			instance port at line @
cse	csb	mifc	last_portdecl_contains_trailcomma_csbcs	е		Last portDeclaration contains a trailing
						comma at line @
cse	csb	mins	mins_expr_incompatible_type_csbcs	е		Expression @ has an incompatible argument
						type @ with the port at
cse	csb	mins	mins_mod_not_exist_csbcs	е		line @ Module @ does not exist
						at line @
cse	csb	mins	mins_entity_not_exist_csbcs	е		Entity @ does not exist at line @
cse	csb	mins	mins_unit_not_exist_csbcs	е		Unit @ does not exist at line @
cse	csb	mod	dup_declar_name_mod_csc	е		Duplicate Declaration of
			;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;			port @ at line @
cse	csb	mod	ill_mod_name_csbcs	е		Illegal module @ at line @
cse	csb	mod	ill_mod_entity_name_csbcs	е		Illegal entity @ at line @ Illegal unit @ at line @
cse	csb csb	mod mod	ill_mod_unit_name_csbcs mod_mult_decl_string_csbcs	e e		Multiple Declarations of
			<b>-</b>			string detected in module @ at line @
cse	csb	mod	mod_entity_mult_decl_string_csbcs	е		Multiple Declarations of
			-			string detected in entity @ at line @
cse	csb	mod	mod_unit_mult_decl_string_csbcs	е		Multiple Declarations of
						string detected in unit @ at line @
cse	csb	mod	mod_mult_def_csbcs	е		Module @ defined in
cse	csb	mod	mod_ent_mult_def_csbcs	е		multiple places at line @ Entity @ defined in
030						multiple places at line @
cse	csb	mod	mod_unit_mult_def_csbcs	е		unit @ defined in multiple places at line @
cse	csb	mod	mod_no_module_found_csbcs	е		No modules found at line
cse	csb	mod	mod_no_entity_found_csbcs	е		@ No entity found at line @
cse	csb	mod	mod_no_unit_found_csbcs	е		No unit found at line @
cse	csb	mod	failed_find_mod_csbcs	е		Failed to find module @ at line @
cse	csb	mod	failed_find_entity_csbcs	е		Failed to find entity @ at line @
cse	csb	mod	failed_find_unit_csbcs	е		Failed to find unit @ at
000	csb	mod	empty_mod_csbcs	е		line @ Empty module at line @
cse	csb	mod	empty_mod_csbcs empty_ent_csbcs	e		Empty entity at line @
cse	csb csb	mod net	empty_unit_csbcs net_implicit_wire_redecl_reg_csbcs	e e		Empty unit at line @ Implicitly declared as a
cse	CSD	net	net_iniplicit_wire_redeci_reg_csbcs	е		wire @ re-declared as a
cse	csb	net	undecl_net_in_mod_csbcs	е		reg @. at line @ Undeclared net @ in
						module @ at line @
cse	csb	net	undecl_port_in_mod_csbcs	е		Undeclared port @ in module @ at line @
cse	csb	net	undecl_sig_in_mod_csbcs	е		Undeclared signal @ in
cse	csb	net	undecl_net_in_ent_csbcs	е		module @ at line @ Undeclared net @ in
						entity @ at line @
cse	csb	net	undecl_port_in_ent_csbcs	е		Undeclared port @ in entity @ at line @
cse	csb	net	undecl_sig_in_ent_csbcs	е		Undeclared signal @ in
cse	csb	net	undecl_net_in_sig_csbcs	е		entity@ at line @ Undeclared net @ in
			💆			signal @ at line @
cse	csb	net	undecl_port_in_sig_csbcs	е		Undeclared port @ in signal @ at line @
cse	csb	net	undecl_sig_in_sig_csbcs	е		Undeclared signal @ in
cse	csb	net	port_used_prior_to_decl_csbcs	е		signal@ at line @ Port @ used prior
	och		. – – – –			toDeclaration at line @
cse	csb	net	1bit_with_prts_csbcs	е		1-bit with part select at line @
cse	csb	netd	ill_decl_vec_csbcs	е		Illegal Declaration of vector @ at line @
cse	csb	nett	nett_ill_reg_name_csbcs	е		Illegal register @ at line
CSO	csb	nett	nett_ill_net_name_csbcs	е		@ Illegal net @ at line @
cse	บอม	Hell	nett_iii_net_name_CSDCS	E		megarner @ ar ime @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	csb	nett	nett_ill_port_name_csbcs	е			- <b>,</b>		Illegal port @ at line @
cse	csb csb	nett	nett_ill_signal_name_csbcs net scalar vect nett csbcs	e					Illegal signal @ at line @ Net declared as both
CSE	CSD	Hell	riet_scalal_vect_riett_csbcs	6					scalar and vector at line
									@
cse	csb	nett	port_scalar_vect_nett_csbcs	е					Port declared as both scalar and vector at line
									@
cse	csb	nett	signal_scalar_vect_nett_csbcs	е					Signal declared as both scalar and vector at line
									@
cse	csb	nett	hot_mux_not_use_bus_connection_net_csbcs	е					One hot mux can not be
									used for bus connection between modules Net @
									at line @
cse	csb	nett	hot_mux_not_use_bus_connection_port_csbcs	е					One hot mux can not be used for bus connection
									between modules Port @
200	oob	nott	hat muy not use hus connection sig cohes						at line @ One hot mux can not be
cse	csb	nett	hot_mux_not_use_bus_connection_sig_csbcs	е					used for bus connection
									between modules Signal
cse	csb	num	not_allowed_width0_num_csbcs	е					@ at line @ Width 0 not allowed for
030	035	Halli	not_allowed_widtho_nam_cobbo						sized number at line @
cse	csb	num	real_num_not_allowed_csbcs	е					Real numbers not
cse	csb	num	found_x_z_in_num_literal_csbcs	е					allowed at line @ Found x and/or z value in
									number literal at line @
cse	csb	num	too_many_digits_in_sized_num_csbcs	W					Number of digits exceeds the width in a sized
									number at line @
cse	csb	num	divide_by_zero_num_csbcs	е					Divide by zero at line @
cse	csb	num	child_mod_inst_parent_mod_csbcs	е					Child module @ instantiates parent
									module @ at line @
cse	csb	num	child_ent_inst_parent_ent_csbcs	е					Child entity @
									instantiates entity module @ at line @
cse	csb	num	child_sig_inst_parent_sig_csbcs	е					Child signal @
									instantiates signal module @ at line @
cse	csb	num	int_decl_incorrect_csbcs	е					Integer Declaration
			int one independent						incorrect at line @
cse	csb	num	int_var_indexed_csbcs	е					Integer variable inedexed at line @
cse	csb	parm	ill_parm_identifier_csbcs	е					Illegal parameter @ at
cse	csb	parm	value_of_parm_OS_platform_dependent_csbcs	w					line @ Parameter select width >
030	035	paiiii	value_or_parm_oo_platform_dependent_esses						32. The value is OS and
									platform dependent at line @
cse	csb	parm	parm_redefined_csbcs	w					Parameter @ redefined
		·							at line @
cse	csb	port	ill_formal_port_name_csbcs	е					Illegal formal port @ at line @
cse	csb	рр	text_redefined_replaced_csbcs	W					Text macro redefined
									and replaced @. Previous definition
									filename, line number @
									New definition filename,
cse	csb	рр	endif_or_else_without_ifdef_csbcs	е					line number @ at line @ Endif-or-else-without
				Ů					ifdef at line @
cse	csb	prim	z_in_prim_inst_csbcs	е					z in primitive instantiation at line @
cse	csb	prts	prts_out_of_range_csbcs	е					Parameter @[@ : @]part
									select is out of range at
cse	csb	prts	ill_prts_inst_array_csbcs	е					line @ Illegal value for part
330	353	۵۰							select of instance array
000	cch	nrto	const arts contains non const coloctor ashes						'name' at line @ Constant part select @
cse	csb	prts	const_prts_contains_non_const_selector_csbcs	е					contains a non-constant
			hus index and f						selector @ at line @
cse	csb	prts	bus_index_prts_for_var_out_of_range_csbcs	е					Bus index @ integer of part select [@:@] for
									variable @ out of range
cse	csb	prts	bus_prts_for_var_out_of_range_csbcs	е					at line @ Bus part select [@:@] for
036	USD	Pito	buo_prio_ioi_vai_out_oi_tatige_conco	6					variable @ out of range
									at line @
cse	csb	prts	bus_prts_index_out_of_name_for_var_csbcs	е					Bus part select [@:@] index @ out of range for
								<u> </u>	variable @ at line @
cse	csb	prts	ill_token_in_prts_csbcs	е			-		Illegal token in part select @ at line @
cse	csb	prts	incomplete_prts_specification_csbcs	е					Incomplete part select
		·							specification @ at line @
cse	csb	prts	ill_index_in_prts_csbcs	е					Illegal index in part select @ at line @
L	1			_1	1	L		1	⊕ at mic ⊌

Cat	Phase	Typo	Name	W/E	V1005	V2001	Sys_ver	Csl Desc
cse	csb	prts	negative_index_in_prts_not_allowed_csbcs	e	V 1995	V2001	Sys_vei	Negative index in part select @ not allowed at
cse	csb	prts	prts_index_order_reversed_csbcs	е				line @ Part select index order reversed [@ : @] [@ : @] should be [@ : @] at line
cse	csb	prts	index_vec_over_max_size_csbcs	W				Vector index @ exceeds the size of the vector.
cse	csb	prts	x_or_z_in_vec_bit_select_index_csbcs	е				Index truncated at line @ x or z in vector bit select
cse	csb	sdir	ignored_synopsis_csdir_csstmt_csbcd	w				index at line @ Ignored a synopsis case directive which is not applied to a Case statement at line @
cse	csb	sdir	ignored_synopsis_csdir_miss_end_csbcd	W				Ignored a synopsis case directive which is missing the end <directive> at line</directive>
cse	csb	simr	inefficient_op_not_a_power_of_2_csbcs	е				@ Division/modulus by a number not a power of 2. Inefficient simulation operation. at line @
cse	csb	simr	simr_multiple_init_blk_force_csbcs	W				Multiple initial blocks force @. Unpredictable simulation result at line
cse	csb	snsl	incomplete_snsl_csbcs	W				Incomplete sensitivity list. @ is not in the sensitivity list. at line @
cse	csb	snsl	edge_sns_process_contains_data_pin_snsl_csbcs	е				Edge sensitive process contains a data pin @ in the sensitivity list at line @
cse	csb	snsl	unsupp_expr_in_snsl_csbcs	W				Unsupported Expression type @ in sensitivity list ' at line @
cse	csb	snsl	partial_bus_decl_width_csbcs	е	?			partial bus @ declared with width @ width @ at line @
cse	csb	snsl	contains_inst_name_csbcs	е				Contains instance name @ at line @
cse	csb	stmt	null_not_allowed_stmt_csbcs	е				Null statement is not allowed here at line @
cse	csb	stmt	stmt_ill_accept_only_net_reg_mem_csbcs	е				Illegal type @ can only accept net, reg, memory at line @
cse	csb	stmt	stmt_ill_accept_only_port_reg_mem_csbcs	е				Illegal type @ can only accept port, reg, memory at line @
cse	csb	stmt	stmt_ill_accept_only_signal_reg_mem_csbcs	е				Illegal type @ can only accept signal, reg, memory at line @
cse	csb	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_csbcs	е				Arithmetic operator RHS has one less bit than the LHS at line @
cse	csb	stmt	ar_op_unequal_lhs_rhs_csbcs	е				Arithmetic operator unequal width LHS and RHS at line @
cse	csb	stmt	ar_op_unequal_var_on_rhs_csb	е				Arithmetic operator unequal width variables @ on RHS at line @
cse	csb	stmt	empty_stmt_csb	е				Empty-statement at line @
cse	csb	syst	return_var_of_user_used_as_rhs_csbcs	W				Return variable of user system task is used as a RHS variable at line @
cse	csb	task	ask_var_not_decl_csbcs	е				Variable @ used but not declared at line @
cse	csb	task	too_few_arg_to_task_csbcs	е				Too few arguments passed to task @ at line @
cse	csb	tri	instance_not_tri_state_device_csbcs	е				Instance name is not a tri-state device at line @
cse	csb	tri	unsupp_gate_type_tristate_csbcs	е				Unsupported gate type @ used for tristate at line @
cse	csb	tri	tri_not_desgn_gate_contention_csbcs	е				Tristate not designed correctly gate @ can cause contention at line @
cse	csb	tri	unsupp_type_instance_tri_csbcs	е				Unsupported type instance type used for tristate @ at line @
cse	csb	tri	incorrect_cont_assign_stmt_tri_gate_csbcs	е				Incorrect continuous assign statement for tristate gate @ at line @
cse	csb	tri	const_assign_to_multidriven_net_csbcs	е				Constant (constiznt) assigned to multi-driven Net @ at line @

Cat	Phase	Tuno	Name	W/E	V4005	V2001	Cue ver	Csl	Desc
cse	csb	Type tri	const_assign_to_multidriven_port_csbcs	e	V 1995	V2001	Sys_ver	Cor	nstant (constiznt)
									ned to multi-driven ort @ at line @
cse	csb	tri	const_assign_to_multidriven_signal_csbcs	е				Cor	nstant (constiznt)
									ned to multi-driven and @ at line @
cse	csb	tri	unsupp_expr_for_tri_csbcs	е				Unsu	oported Expression
								type	@ for tristate at line @
cse	csb	vec	vec_invalid_csbcs	е				Vec	or @ is invalid. at line @
cse	csb	vec	vec_mod_not_exist_csbcs	е					or @ module name
cse	csb	vec	vec_ent_not_exist_csbcs	е					not exist at line @ for @ entity name
								does	not exist at line @
cse	csb	vec	vec_unit_not_exist_csbcs	е					r @ unit name does t exist at line @
cse	csb	vec	vec_not_contain_data_sig_csbcs	е					ctor @ does not in any data signals
									at line @
cse	csb	vec	vec_not_contain_clk_sig_csbcs	е					ctor @ does not in a clock signal at
cse	csb	vec	vec_not_contain_rst_sig_csbcs	е				\/o	line @ ctor @ does not
CSE	CSD	VEC	vec_not_contain_rst_sig_csucs						in a reset signal at
cse	csb	vec	vec_stim_not_contain_input_ports_csbcs	е				Ved	line @ ctor @ which is a
								stimu	lus vector does not
									n any input ports at line @
cse	csb	vec	vec_expect_not_contain_outputs_ports_csbcs	е					tor @ which is an
									in any output ports
cse	csb	vec	vec_is_missing_the_csbcs	е				Vecto	at line @ or @ is missing the
000	csb	vec	vec_dtsig_not_found_csbcs	е					@ at line @ r @ data signals @
cse			_ G	е				no	found at line @
cse	csb	vec	vec_clk_sig_not_found_csbcs	е					r @ clock signal @ tound at line @
cse	csb	vec	vec_rst_sig_not_found_csbcs	е				Vecto	r @ reset signal @
cse	csb	vec	vec_stim_input_port_not_found_csbcs	е					found at line @ r @ stimulus vector
			·					input	port @ not found at line @
cse	csb	vec	vec_output_port_not_found_csbcs	е					or @ output port @
cse	CSC	ase	arch_state_el_mod_not_exist_csccs	е					found at line @ chitectural state
									nent @ module @ not exist at line @
cse	CSC	ase	arch_state_el_ent_not_exist_csccs	е				Ar	chitectural state
									nt @ entity @ does t exist at line @
cse	CSC	ase	arch_state_el_unit_not_exist_csccs	е				Ar	chitectural state ent @ unit @ does
								no	t exist at line @
cse	CSC	ase	arch_state_el_missi_clk_name_csccs	е					chitectural state nt @ is missing the
			arab atata al misa mam nama assa					cloc	k name at line @ chitectural state
cse	CSC	ase	arch_state_el_miss_mem_name_csccs	е				eleme	nt @ is missing the
cse	CSC	ase	arch state el miss the csccs	е					ory name at line @ chitectural state
000	000	400	a.o.,_o.a.o_ooo						nt @ is missing the
cse	CSC	ase	arch_state_el_miss_rst_name_csccs	е				Ar	@ at line @ chitectural state
								eleme	nt @ is missing the et name at line @
cse	CSC	ase	arch_state_el_evtrigg_miss_ev_name_csccs	е				Ar	chitectural state
									ment @ is event ered and is missing
000	200	000	arch state of all name not found access					the ev	ent name at line @ chitectural state
cse	CSC	ase	arch_state_el_clk_name_not_found_csccs	е				elem	ent @ clock name
cse	CSC	ase	arch_state_el_mem_name_not_found_csccs	е					ot found at line @ chitectural state
330	300	400						ele	ment @ memory
L									@ not found at line @
cse	CSC	ase	arch_state_el_not_found_csccs	е				Ar	chitectural state element @
									state_name @ not
cse	CSC	assn	x_in_rhs_of_assihnment_cscc	е					ound at line @ as of assignment at
	csc		z_in_rhs_of_assn_default_csi_cscc						line @ hs of assignement
cse	USC	assn	Z_III_III3_UI_ASSII_UEIAUII_CSI_CSCC	е					efaultCase item at
cse	CSC	assn	z_in_rhs_of_assn_csccs	е				z in r	line @ hs of assignement
									at line @
cse	CSC	assn	unequal_length_lhs_rhs_csccs	е				Uneq	ual length LHS and

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_v	er Cs	
cse	CSC	assn	unequal_length_lhs_rhs_off_one_bit_csccs	е					RHS at line @ Unequal length LHS and RHS off by one bit at line @
cse	CSC	ccd	ccd_cdir_must_be_cst_expr_csccs	е				х	CSL directive size must be constant Expression
cse	CSC	ccd	clk_dir_not_applied_to_dsgn_csccs	w				х	at line @  CSL clock directive not applied to design. Could
cse	CSC	ccd	csl_filter_unused_csccs	W				х	not find clock at line @ CSL message filter @ not found. Filter @ is
cse	CSC	ccd	csl_mess_not_filtered_csccs	W				X	unused. at line @  CSL message @ can not be filtered. Filter @ is unused. at line @
cse	CSC	ccd	error_csdir_not_found_csccs	е				x	Error CSL directive @ not found. Error @ is unused. at line @
cse	CSC	chrs clk	ill_val_chrs_csc clk_name_not_found_cdir_csccs	e e				х	Illegal value @ at line @  Clock name not found in cslc directive at line @
cse	csc	clk	expr_sunj_to_different_clk_phases_csccs	е					Expression subject to different clock phases at line @
cse	CSC	csi	z_csi_not_in_casez_csc	е					z case item not in casez at line @
cse	CSC	csi	noncstn_rep_in_conc_csccs	е					Non-constant repeator in concatenation at line @
cse	csc	decl	decl_array_over_max_size_csccs	е					Array @ exceeds maximum size limit at line @
cse	CSC	dely	x_or_z_in_dely_csccs	е					x or z in delay at line @ Memory part select
cse	CSC	dmsn	mem_prts_index_out_of_range_for_mem_csccs	е					[@:@] index @ out range for memory @ at line @
cse	CSC	dmsn	dime_select_for_mem_missing_csccs	е					Select for memory @ missing at line @
cse	CSC	dmsn	dime_index_out_of_bounds_for_mem_csccs	е					Index <index> out of bounds for memory @. Range [@: @] at line @</index>
cse	csc	dmsn	dime_prts_out_of_bounds_for_net_csccs	е					Part select [@ : @] out of bounds for net @. Range [@ : @] at line @
cse	CSC	dmsn	dime_prts_out_of_bounds_for_port_csccs	е					Part select [@ : @] out of bounds for port @. Range [@ : @] at line @
cse	CSC	dmsn	dime_prts_out_of_bounds_for_sig_csccs	е					Part select [@ : @] out of bounds for signal @. Range [@ : @] at line @
cse	CSC	dmsn	dime_prts_reg_csccs	е					Part select [@ : @] reg @. Range [@ : @] at line @
cse	CSC	drvc	incompatible_drvc_for_net_csccs	е					Incompatible drivers for Net @ at line @
cse	CSC	drvc	incompatible_drvc_for_port_csccs	е					Incompatible drivers for Port @ at line @
cse	CSC	drvc	incompatible_drvc_for_sig_csccs	е					Incompatible drivers for Signal @ at line @
cse	CSC	drvc	drvc_multiple_drive_net_partially_overlap_csccs	е					Multiple drive Net partially overlap at line @
cse	CSC	drvc	drvc_multiple_drive_port_partially_overlap_csccs	е					Multiple drive Port partially overlap at line @
cse	CSC	drvc	drvc_multiple_drive_sig_partially_overlap_csccs	е					Multiple drive Signal partially overlap at line @
cse	CSC	dsgn	dsgn_top_mod_cannot_id_csccs	е					Top module @ cannot be identified at line @
cse	CSC	dsgn	dsgn_top_entity_cannot_id_csccs	е					Top entity @ cannot be identified at line @
cse	CSC	dsgn	dsgn_top_unit_cannot_id_csccs	е					Top unit @ cannot be identified at line @
cse	CSC	dsgn	unit_dsgn_cycle_not_spanning_tree_csccs	е					Unit design hierarchy contains a cycle. Hierarchy is not a
cse	CSC	dsgn	cse_csc_dsgn_has_parent	е					spanning tree. at line @ Parent already set at line
cse	csc	dsgn	cse_csc_dsgn_empty_list	W					@ at line @ List is empty, no signals added to unit at line @
cse	CSC	dsgn expr	cse_csc_dsgn_empty_group expr_prts_indices_1bit_var_csccs	w e					Group is empty at line @ Part select indices 1-bit variable at line @
cse	CSC	expr	expr_prts_must_be_cst_expr_csccs	е					Part select specifier Expression must be constant Expression at line @
cse	CSC	expr	not_const_expr_csccs	е					Repetition multiplier in concatenation is not a constant Expression at

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_	/er	Csl	Desc
cse	CSC	expr	ill_bit_select_expr_csccs	е						line @ Illegal bit select
cse	CSC	expr	repetition_multiplier_in_conc_not_const_expr_csccs	W						expression @ at line @ Repetition multiplier in
										concatenation is not a constant Expression at
cse	CSC	expr	int_operand_not_1_bit_csccs	W						line @ Logic operator has
										integer operands instead of 1-bit operands at line
cse	CSC	expr	unsupp_expr_csccs	W						@ Unsupported Expression
cse	CSC	expr	unsupp_operator_csccs	W						type @ at line @ Unsupported operator
cse	CSC	expr	use_of_sg_bit_const_csccs	W						type @ at line @ Use of single bit constant
cse	CSC	expr	unary_op_in_comparison_csccs	е						at line @ Unary op used in
cse	CSC	expr	x_or_z_in_cond_expr_csccs	е						comparison at line @ x or z in conditional
cse	CSC	expr	zero_in_rep_in_conc_csccs	е						expression at line @ Zero repeator in
cse	CSC	expr	expr_in_mod_port_dir_csccs	е						concatenation at line @ Expression @ in module
cse	CSC	expr	expr_in_ent_port_dir_csccs	е						port dir at line @ Expression @ in entity
cse	CSC	expr	expr_in_sig_port_dir_csccs	е						port dir at line @ Expression @ in unit port
cse	CSC	expr	expr in inst csccs	е						dir at line @ Expression @ in inst i@
cse	csc	expr	expr_operator_operands_unequal_lenght_csccs	е						at line @  Expression operator @
030	030	САРІ	expr_operator_operatios_unequa_tengin_esses							operands @ unequal length at line @
cse	CSC	file	cannot_open_filter_specification_file_csccs	е						Cannot open filter specification file @ at line
		£:1 -								. @
cse	CSC	file	filter_specification_file_missing_csccs	е						Filter specification file name @ is missing at
cse	CSC	file	mismatch_mod_file_name_csccs	е						line @ Mismatch between
										module name @ and file name @ at line @
cse	CSC	file	mismatch_ent_file_name_csccs	е						Mismatch between entity name @ and file name
cse	CSC	file	mismatch_sig_file_name_csccs	е						@ at line @ Mismatch between signal
										name @ and file name @ at line @
cse	CSC	func	port_not_output_func_csccs	е						Port @ direction cannot be output at line @
cse	CSC	func	too_many_arg_to_func_csccs	е						Too many arguments passed to function @ at
cse	CSC	func	too_few_arg_to_func_csccs	е						line @ Too few arguments
										passed to function @ at line @
cse	CSC	func	undefined_func_csccs	е						Undefined function @ at line @
cse	CSC	func	funct_expr_cannot_expnaded_csccs	е						Function expression @ cannot be expanded at
cse	CSC	func	funct_not_used_in_expr_csccs	W						line @ Function @ is not being
										used in an Expression at line @
cse	CSC	func	func_decl_csccs	W						Function Declaration @ already declared as
cse	CSC	func	cse csc func args	е						another type at line @ Invalid arguments at line
cse	CSC	func	cse_csc_func_illegal_state	е						@ Illegal state for this
cse	CSC	func	cse_csc_func_wrong_arg_nr	е						method @ call at line @ Wrong number of
cse	CSC	hid	cannot_locate_hier_id_hid_csccs	е						arguments at line @ Can't locate hierarchical
cse	csc	hid	ref_minst_found_in_expr_hid_cscs	е						identifier @ at line @ References a module
300	300		.cciodita_ii_oxpi_iita_cocc							instance @ found in an Expression hid at line @
cse	csc	hid	ref_entity_found_in_expr_hid_csccs	е						References a entity instance @ found in an
cse	csc	hid	ref_unit_found_in_expr_hid_csccs	е						Expression hid at line @  References a unit
USE	030	illu	roi_ariii_touriu_iii_expi_riiu_cocco	6						instance @ found in an Expression hid at line @
cse	CSC	hid	hid_reference_not_found_csccs	е						@ reference not found at line @ line @
cse	CSC	hid	mifc_in_hid_not_exist_csccs	е						Module instance @ in hid does not exist at line @
cse	CSC	hid	entity_instance_in_hid_not_exist_csccs	е						Entity instance @ in hid

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	CSC	hid	unit instance in hid not exist csccs	е			•		does not exist at line @ Unit instance @ in hid
cse	CSC	hid	mod_found_in_path_in_dsgn_csccs	е					does not exist at line @ Module @ found in path
cse	CSC	hid	enity_found_in_path_in_dsqn_csccs	е					@ in the design at line @ Entity @ found in path @
cse	csc	hid	unit_found_in_path_in_dsgn_csccs	е					in the design at line @ Unit @ found in path @
		hid	5 _						in the design at line @ Hierarchical ID @ path
cse	CSC	nia	hierarchical_id_path_contains_func_csc	е					contains a function at line
cse	CSC	hid	cse_csc_hid_illegal	е					@ Illegal hierarchical ID @
cse	CSC	id	cse_csc_id_illegal	е					at line @ Illegal identifier name @
cse	CSC	init	assn_mem_in_init_blk_csccs	е					at line @ Assign memory in initial
cse	CSC	inst	inst_duplicate_mod_name_csccs	е					block at line @ Duplicate port @ in the
									port list for module @ at line @
cse	CSC	inst	inst_duplicate_entity_name_csccs	е					Duplicate port @ in the port list for entity @ at
cse	CSC	inst	inst_duplicate_unit_name_csccs	е					line @ Duplicate port @ in the
			224, 3842, 2 8 32333						port list for unit @ at line @
cse	CSC	inst	ill_mod_inst_name_csccs	е					Illegal module instance @ at line @
cse	CSC	inst	ill_entity_inst_name_csccs	е					Illegal entity instance @ at line @
cse	csc	inst	ill_unit_inst_name_csccs	е					Illegal unit instance @ at line @
cse	CSC	inst	inst_name_defined_mod_cscc	е					Instance name @
									already defined in this module at line @
cse	CSC	inst	inst_name_defined_ent_cscc	е					Instance name @ already defined in this
cse	CSC	inst	inst_name_defined_unit_cscc	е					entity at line @ Instance name @
									already defined in this unit at line @
cse	CSC	inst	inst_too_many_bits_csccs	е					Too many bits for port @ of instance array @,
									formal @, actual @ at line @
cse	CSC	inst	inst_port_not_connected_var_csccs	е					Port 'port' of instance array 'array' is not
									connected to variable at line @
cse	CSC	inst	inst_insufficient_bits_csccs	е					Insufficient bits for port port of instance array
									'array ', formal number, actual number at line @
cse	CSC	inst	inst_mod_name_not_defined_csccs	е					Module name not defined at line @
cse	CSC	inst	inst_ent_name_not_defined_csccs	е					Entity name not defined at line @
cse	csc	inst	inst_unit_name_not_defined_csccs	е					Unit name not defined at
cse	CSC	inst	many_mod_inst_param_assign_csccs	е					line @ Too many module
									instance parameter assignments (number >
cse	CSC	inst	many_entity_inst_param_assign_csccs	е					rrumber) at line @ Too many entity instance
									parameter assignments (number > rrumber) at
cse	CSC	inst	many_unit_inst_param_assign_csccs	е					line @ Too many unit instance
			<u>-</u>						parameter assignments (number > rrumber) at
cse	CSC	inst	complexexpr_cannot_mapped_inout_port_csccs	е					line @ Complex Expression @
									cannot be mapped to inout port @ at line @
cse	CSC	inst	complexexpr_cannot_mapped_unknown_port_csccs	е					Complex Expression @ cannot be mapped to
									unknown type port @ at line @
cse	CSC	inst	netdecl_contains_ill_prts_csccs	е					Net Declaration [@: @] contains an illegal part
cse	csc	inst	regdecl_contains_ill_prts_csccs	е					select at line @  Reg Declaration [@ : @]
036	030	ıı ıəl	regacoi_contants_m_prts_csccs	6					contains an illegal part select at line @
cse	CSC	inst	complex_expr_inst_parent_module_csccs	е					Complex actual
									Expression associated with port @ of module @
	05-	in-4	sampley aver jest outity and a state						instantiated in parent module at line @
cse	CSC	inst	complex_expr_inst_entity_parent_module_csccs	е					Complex actual

Pisso   Type										
Complex_expt_inst_unit_parent_module_saccs   e	Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	with port @ of entity @ instantiated in parent
Expression associated with profit of units of profess of units of	020	CSC	inet	complex expr inst unit parent module cecce						
See	CSE	CSC	IIISt	complex_expl_inst_unit_parent_module_csccs	6					
module at line &   module at line &   module at line &   module at line &   width mismatch, at line &   module at line &   width mismatch, at line &   module at li										with port @ of unit @
See										
	cse	CSC	inst	inst_mod_output_port_width_csccs	е					
See   Case   Inst.   Inst., entity_output_port_width_cascos   e   Settly & Output port & width mismatch   Settly & Se										
Case										
See   CSC   Inst   Inst_unit_output_port_width_csccs   0   Unit of Cutput port   See   CSC   Inst   Inst_unit_output_port_width_csccs   0   Unit of Cutput port   See   CSC   Inst   Inst_unit_input_port_width_csccs   0   Word & Inst_unit_input_port_width_csccs   0   Word & Inst_unit_input_port_width_csccs   0   Word & Inst_unit_input_port_width_csccs   0   Word & Inst_unit_input_port_width_csccs   0   Unit of Coupt port of See   See   Inst   Inst_unit_input_port_width_csccs   0   Unit of Coupt port of See   See   Inst   Inst_unit_input_port_width_csccs   0   Unit of Coupt port of See   See   Inst   Inst_unit_input_port_width_csccs   0   Unit of Inst_unit_input_port_width_mismatch_csccs   0   Unit of Inst_unit_input_port_width_mismatch_csccs   0   Unit of Inst_unit_input_port_width_instant_cscc   0   Unit of Inst_unit_input_port_width_instant_csccs   0   Unit of In	cse	CSC	inst	inst_entity_output_port_width_csccs	е					
See   Sec   Inst										
CSC   Inst   Inst_mod_input_port_width_csccs   e										
cse csc inst inst_mod_input_port_width_csccs e csc inst inst_mod_input_port_width_csccs e csc inst inst_mod_input_port_width_csccs e csc inst inst_mod_input_port_width_csccs e csc inst inst_mod_not_define_csccs e csc inst_mod_not_defi	cse	csc	inst	inst_unit_output_port_width_csccs	е					Unit @ Output port @
See   Sec   Inst   Inst_mod_input_port_width_csccs   e										
width mismatch   struck   width mismatch   struck   width mismatch   struck   width mismatch   struck   width   port-width   port-width   struck   width   width   port-width   port-width   port-width   width   width   width   port-width   port-width   port-width   width   width   width   port-width   port-width   width   port-width   port-width   width   port-width   port-width   port-width   width   port-width   port-width   port-width   port-width   width   port-width   por										
CSE   CSC   Inst   Inst_entity_input_port_width_csccs   e	cse	CSC	inst	inst_mod_input_port_width_csccs	е					
see so inst inst_entity_input_port_width_csccs e lentity inst_entity_input_port_entity_input_port_width_csccs e lentity inst_entity_input_port_entity_input_										
width mismatch, actual-width (port-width (port-width (port-width (port-width) at line @ width mismatch, actual-width (port-width) at line @ width mismatch, actual-width (port-width) at line @ width mismatch, actual width mismatch, acces csc inst inst_entity_not_define_csccs e e										
CSE   CSC   Inst   Inst_unit_input_port_width_csccs   e	cse	csc	inst	inst_entity_input_port_width_csccs	е					
See   Sec   Inst   Inst_unit_input_port_width_csccs   e										
width mismatch, actual-width (port-width) at line @   Module on defined at line @   Entity not defined at line @   Unit not defined at line @   Entity width @ Instance good   Unit not defined at line @										at line @
CSE	cse	CSC	inst	inst_unit_input_port_width_csccs	е					
See   Sec   Inst   Inst_mod_not_define_csccs   e   Module not defined at line @ Cse   Sec   Inst   Inst_entity_not_define_csccs   e   Entity not defined at line @ Instance   Entity not defined at line @ Instance   Entity not defined at line @ Module   Instance										
International Cose										at line @
CSE   CSC   Inst   Inst_unit_not_define_csccs   e	cse	CSC	inst	inst_mod_not_define_csccs	е					
CSC   CSC   Inst   Inst.unit.not.define_CSCCS   e	cse	CSC	inst	inst_entity_not_define_csccs	е					
See				in the space of th						_
cse csc inst ent_port_actual_formal_width_mismatch_csccs w inst ent_formal_width_mismatch_csccs w instead ent_formal_width_mismatch_					_					
See   CSC   Inst   Inst_offers_in_case_from_end_csccs   W										
CSE										
actual width @ formal width @ at line @ width manatch_actual width @ formal width @ for loop at line @ formal width @ formal width or loop at line @ for	cse	CSC	inst	ent_port_actual_formal_width_mismatch_csccs	w					Entity @ instance @ port
See   CSC   Inst   Unit_port_actual_formal_width_mismatch_csccs   W   Unit_Dort_actual_formal_width_mismatch_actual width @ at line @ Unit_Dort_actual_width @ at line @ Instance name @ differs in case from module name @ at line @ Instance name @ differs in case from module name @ at line @ Instance name @ differs in case from entity name @ at line @ Q at line @ Instance name @ differs in case from entity name @ at line @ Instance name @ differs in case f										
CSE   CSC   Inst   Inst_differs_in_case_from_mod_csccs   e   Instance name @ differs in case from module name @ at line @ Instance name @ differs in case from module name @ at line @ Instance name @ differs in case from module name @ at line @ Instance name @ differs in case from module name @ at line @ Instance name @ differs in case from entity name @ at line @ at line @ Instance name @ differs in case from entity name @ at line @ Instance name at line @ Instance name @ at line @ Instance name at line @ I										
cse   csc   linst   inst_differs_in_case_from_mod_csccs   e     linstance name @ differs   in case from module   name @ at line @   linstance name @ differs   in case from module   name @ at line @   linstance name @ differs   in case from module   name @ at line @   linstance name @ differs   in case from mitty name @ at line @   linstance name @ differs   in case from signal name @ at line @   linstance name @ differs   in case from signal name @ at line @   linstance name @ differs   in case from signal name @ at line @   linstance name @ differs   in case from signal name @ at line @   linstance name @ differs   in case from signal name @ at line @   linstance name @ differs   in case from signal name @ at line @   l	cse	CSC	inst	unit_port_actual_formal_width_mismatch_csccs	W					
CSE   CSC   Inst   Inst_differs_in_case_from_mod_csccs   e   Instance name @ differs in case from module name @ at line @ line										
CSE   CSC   Inst   Inst_differs_in_case_from_ent_csccs   e   Instance name @ at line										width @ at line @
CSE   CSC   Inst   Inst_differs_in_case_from_ent_csccs   e   Instance name @ at line @   Instance name @ differs   Incase from entity name @ at line @   Instance name @ differs   Incase from entity name @ at line @   Instance name @ differs   Incase from entity name @ at line @   Instance name @ differs   Incase from signal name @ at line @   Instance name @ differs   Incase from signal name @ at line @   Instance name @ differs   Incase from signal name @ at line @   Instance name @ differs   Incase from signal name @ at line @   Unable to determine init value for loop at line @   Unable to determine linit for loop at line @   Unable to determine linit for loop at line @   Loop bounds are calculated to be integer @ check that this is correct at line @   Loop bounds are calculated to be integer @ check that this is correct at line @   Expression in lhs of assignment contains a variable bit select at line @   Expression in lhs of assignment contains a variable bit select at line @   Non-constant tine @   Non-constant tine @   Non-constant tine @   Non-constant toop bound. Loop control variable initialization Expression is not a constant Expression is not a constant Expression at at line @   Non-constant toop bound. Incop terminating Expression could not be evaluated to a constant at line @   Non-constant toop bound. Incop terminating Expression could not be evaluated to a constant at line @   Non-constant toop bound. Incop terminating Expression reset by variable at line @   Expression to the deconstant at line @   Expression to the deconstant at line @   Non-constant toop bound. Incop terminating Expression to the deconstant at line @   Non-constant toop bound. Incop terminating Expression to the deconstant at line @   Non-constant toop bound. Incop terminating Expression to the deconstant at line @   Non-constant toop bound. Incop terminating Expression to the deconstant at line @   Non-constant toop bound. Incop terminating Expression to the deconstant at line @   Non-constant toop bound. Incop terminating	cse	CSC	ınst	inst_differs_in_case_from_mod_csccs	е					
cse   csc   csc   loop   undet_limit_loop_csccs   e   Unable to determine init for loop at line @   cse   csc   loop   undet_limit_loop_csccs   e   Unable to determine init for loop at line @   cse   csc   loop   undet_limit_loop_csccs   e   Unable to determine limit   for loop at line @   cse   csc   loop   loop_bounds_calculated_int_csccs   w   Unable to determine limit   for loop at line @   cse   csc   loop   loop_bounds_calculated_int_csccs   w   Unable to determine limit   for loop at line @   correct at line @   correct at line @   expression in line of   assignment contains a variable bit select at line @   cse   csc   loop   loop_bounds_not_const_csc   w   Dop_bounds_are   non-constant to line @   csc   csc   loop   loop_ctrl_init_expr_not_const_cscs   w   Non-constant to line @   constant Expression is not a   constant Expression is not a   constant Expression could not be evaluated to a constant at line @   csc   csc   loop   loop_term_expr_not_const_cscs   e   Non-constant toop   bound. Loop terminating   cxpression could not be evaluated to a constant at line @   csc   csc   loop   loop_term_expr_not_const_cscs   e   Non-constant toop   bound. loop terminating   cxpression reset by variable at line @   ton-constant toop   bound. limitalizing   cxpression reset by variable at line @   ton-constant toop   ton-control variable tine @   ton-control variable   tine @   ton-control variable   tine @   ton-control variable   tine @   ton-control variable   tine @   ton-control variable   tine @   ton-control variable   tine @   ton-control variable   tine @   ton-control variable   tine @										name @ at line @
CSC   CSC   Inst   Inst_differs_in_case_from_sig_csccs   e   Instance name @ differs in case from signal name @ at line @ Instance name @ differs in case from signal name @ at line @ Unable to determine init value for loop at line @ Unable to determine init value for loop at line @ Unable to determine linit for loop at line @ Unable to determine linit for loop at line @ Unable to determine linit for loop at line @ Unable to determine linit for loop at line @ Loop bounds are calculated to be integer @, check that this is correct at line @ Expression in lhs of assignment contains a variable bit select at line @ Expression in lhs of assignment contains a variable bit select at line @ Sec   Ioop   Ioop_bounds_not_const_cscc   w   Unable to determine linit walue for loop at line @ Ioop_bounds are non-constant at line @ Non-constant toop bound. Loop bounds are non-constant at line @ Ioop_bound. Loop control variable initialization Expression is not a constant Expression is not a constant Expression at line @ Ioop_control variable initialization Expression could not be evaluated to a constant at line @ Ioop_control variable initializing Expression could not be evaluated to a constant at line @ Ioop_control variable initializing Expression could not be evaluated to a constant at line @ Ioop_control variable at line @ Ioop_cont	cse	CSC	inst	inst_differs_in_case_from_ent_csccs	е					
Instance name @ differs in case from signal name @ at line @ Unable to determine init case from signal name @ at line @ Unable to determine init value for loop at line @ Value for loop at line was loop at line @ Value for loop at line was loop at li										
CSC CSC IOOP Undet_init_value_loop_csccs	cse	csc	inst	inst_differs_in_case_from_sig_csccs	е					Instance name @ differs
CSE         CSC         loop         undet_init_value_loop_csccs         e         Unable to determine init value for loop at line @ value for loop at line @ Unable to determine limit for loop at line @ Unable to determine limit for loop at line @ Loop bounds are calculated to be integer @, check that this is correct at line @ check that this is sold that this is correct at line @ check that this is sold that this is sold that this is sold that the integer of the check that this is sold that the line is correct at line @ check that this is sold that the line is sold tha										
CSE         CSC         loop         undet_limit_loop_csccs         e         Unable to determine limit for loop at line @           CSE         CSC         loop         loop_bounds_calculated_int_csccs         w         Loop bounds are calculated to be integer @, check that this is correct at line @           CSE         CSC         loop         expr_lhs_contains_var_bit_select_csccs         w         Expression in hs of assignment contains a variable bit select at line @           CSE         CSC         loop         loop_bounds_not_const_cscc         w         Loop bounds are non-constant at line @           CSE         CSC         loop         loop_ctrl_init_expr_not_const_csccs         w         Non-constant loop bound. Loop control variable initialization Expression is not a constant Expression at line @           CSE         CSC         loop         loop_term_expr_not_const_csccs         w         Non-constant loop bound. loop terminating Expression could not be evaluated to a constant at line @           CSE         CSC         loop         init_expr_reset_by_var_csccs         e         Non-constant loop bound. initializing Expression reset by variable at line @           CSE         CSC         loop         loop_ctrl_var_1_bit_wide_csccs         w         The loop control variable @ is one bit wide. Check	cse	CSC	loop	undet_init_value_loop_csccs	е					Unable to determine init
CSE   CSC   Ioop   Ioop_bounds_calculated_int_csccs   W   Calculated to be integer @, check that this is correct at line @	CS A	CSC	loon	undet limit loop cecce						
calculated to be integer @, check that this is correct at line @  CSE CSC loop expr_lhs_contains_var_bit_select_csccs	030	030	юор	undet_imit_loop_cacca						for loop at line @
CSE CSC loop loop_term_expr_not_const_csccs w loop loop_term_expr_not_const_csccs loop loop_term_e	cse	CSC	loop	loop_bounds_calculated_int_csccs	W					
CSE CSC loop loop_trinit_expr_not_const_csccs										
assignment contains a variable bit select at line @  cse csc loop loop_bounds_not_const_csc w  Loop bounds are non-constant at line @  cse csc loop loop_ctrl_init_expr_not_const_csccs w  Non-constant loop bound. Loop control variable initialization Expression is not a constant Expression at line @  cse csc loop loop_term_expr_not_const_csccs w  Non-constant loop bound. loop terminating Expression could not be evaluated to a constant at line @  cse csc loop init_expr_reset_by_var_csccs e  csc csc loop loop_ctrl_var_1_bit_wide_csccs w  The loop control variable at line @  cse csc loop loop_ctrl_var_1_bit_wide_csccs w  The loop control variable @ is one bit wide. Check										correct at line @
CSE CSC loop loop_bounds_not_const_csc	cse	CSC	loop	expr_lhs_contains_var_bit_select_csccs	W					
CSE     CSC     loop     loop_bounds_not_const_cscc     W     Loop bounds are non-constant at line @       CSE     CSC     loop     loop_ctrl_init_expr_not_const_csccs     W     Non-constant loop bound. Loop control variable initialization Expression is not a constant Expression at line @       CSE     CSC     loop     loop_term_expr_not_const_csccs     W     Non-constant loop bound. loop terminating Expression could not be evaluated to a constant at line @       CSE     CSC     loop     init_expr_reset_by_var_csccs     e     Non-constant loop bound. initializing Expression reset by variable at line @       CSE     CSC     loop     loop_ctrl_var_1_bit_wide_csccs     W     The loop control variable @ is one bit wide. Check										
cse csc loop loop_ctrl_init_expr_not_const_csccs		605	les-	loop beyinds not soret						_
CSE     CSC     loop     loop_ctrl_init_expr_not_const_csccs     W     Non-constant loop bound. Loop control variable initialization Expression is not a constant Expression at line @         CSE       CSC       loop       loop_term_expr_not_const_csccs       W       Non-constant loop bound. loop terminating Expression could not be evaluated to a constant at line @         CSE       CSC       loop       init_expr_reset_by_var_csccs       e       Non-constant loop bound. initializing Expression reset by variable at line @         CSE       CSC       loop       loop_ctrl_var_1_bit_wide_csccs       W       The loop control variable @ is one bit wide. Check	use	USC	ioob	ioop_bourids_not_const_csc	W					
CSE   CSC   LOOP   LOOP_term_expr_not_const_csccs   W   W   Work   Wor	cse	CSC	loop	loop_ctrl_init_expr_not_const_csccs	W					Non-constant loop
Expression is not a constant Expression at line @  cse csc loop loop_term_expr_not_const_csccs										
cse csc loop loop_term_expr_not_const_csccs										Expression is not a
cse     csc     loop     loop_term_expr_not_const_csccs     w     Non-constant loop bound. loop terminating Expression could not be evaluated to a constant at line @       cse     csc     loop     init_expr_reset_by_var_csccs     e     Non-constant loop bound. initializing Expression reset by variable at line @       cse     csc     loop     loop_ctrl_var_1_bit_wide_csccs     w     The loop control variable @ is one bit wide. Check										
bound. loop terminating Expression could not be evaluated to a constant at line @    CSE	cse	CSC	loop	loop_term_expr_not_const_csccs	w					Non-constant loop
cse csc loop init_expr_reset_by_var_csccs e Non-constant loop bound. initializing Expression reset by variable at line @  cse csc loop loop_ctrl_var_1_bit_wide_csccs w The loop control variable @ is one bit wide. Check										
cse csc loop init_expr_reset_by_var_csccs e Non-constant loop bound. initalizing Expression reset by variable at line @  cse csc loop loop_ctrl_var_1_bit_wide_csccs w The loop control variable @ is one bit wide. Check										
bound. initializing Expression reset by variable at line @  cse csc loop loop_ctrl_var_1_bit_wide_csccs w The loop control variable @ is one bit wide. Check										at line @
Expression reset by variable at line @  cse csc loop loop_ctrl_var_1_bit_wide_csccs w The loop control variable @ is one bit wide. Check	cse	CSC	loop	init_expr_reset_by_var_csccs	е					
cse csc loop loop_ctrl_var_1_bit_wide_csccs w The loop control variable @ is one bit wide. Check										
@ is one bit wide. Check			le -	loop and were 4 his will						variable at line @
	cse	CSC	юор	ioop_ciii_var_i_bit_wide_csccs	W					

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	CSC	mdb	bad_mdb_net_csccs	е					Declaration. at line @ Bad multi-driven Net @ at line @
cse	CSC	mdb	bad_mdb_port_csccs	е					Bad multi-driven Port @ at line @
cse	CSC	mdb	bad_mdb_signal_csccs	е					Bad multi-driven Signal @ at line @
cse	CSC	mdb	unsupp_comp_mdb_net_csccs	е	?				Unsupported component type @ driving in multi-driven Net name at
cse	CSC	mdb	unsupp_comp_mdb_port_csccs	е	?				line @ Unsupported component type @ driving in multi-driven Port name at line @
cse	csc	mdb	unsupp_comp_mdb_signal_csccs	е	?				Unsupported component type @ driving in multi-driven Signal name at line @
cse	CSC	mdb	unsupp_comp_drive_mdb_csccs	е	?				Unsupported component type @ driving multi-driven Net natne at line @
cse	CSC	mdb	unsupp_comp_drive_mdb_port_csccs	е	?				Unsupported component type @ driving multi-driven Port natne at line @
cse	CSC	mdb	unsupp_comp_drive_mdb_signal_csccs	е	?				Unsupported component type @ driving multi-driven Signal natne at line @
cse	CSC	mdb	mdb_net_driven_by_trns_csccs	е					Multiply driven Net driven by transistor primitive type @ at line @
cse	CSC	mdb	mdb_port_driven_by_trns_csccs	е					Multiply driven Port driven by transistor primitive type @ at line @
cse	csc	mdb	mdb_sig_driven_by_trns_csccs	е					Multiply driven Signal driven by transistor primitive type @ at line
cse	CSC	mdb	mdb_unsupp_comp_drvs_net_csccs	е					Unsupported component type driving Net drives Net connected to multi-driven Net at line @
cse	CSC	mdb	mdb_unsupp_comp_drvs_port_csccs	е					Unsupported component type driving Port drives Port connected to multi-driven Port at line
cse	CSC	mdb	mdb_unsupp_comp_drvs_sig_csccs	е					Unsupported component type driving Signal drives Signal connected to multi-driven Signal at line
cse	CSC	mdb	mdb_incompatible_net_drives_multiple_net_csccs	е					Incompatible driver driving tandem Net drives Net connected to
cse	csc	mdb	mdb_incompatible_port_drives_multiple_port_csccs	е					multi-driven Net at line @ Incompatible driver driving tandem Port drives Port connected to multi-driven Port at line @
cse	CSC	mdb	mdb_incompatible_sig_drives_multiple_sig_csccs	е					Incompatible driver driving tandem Net drives Net connected to multi-driven Port at line
cse	CSC	mdb	mdb_unsupp_LHS_concatenation_csccs	е					Unsupported LHS concatenation in multi-drive 'device at line @
cse	CSC	mdb	mdb_bus_has_too_many_drivers_csccs	е					Bus has too many drivers. at line @
cse	CSC	mdb	mdb_always_blk_drive_csccs	W					Multiple always blocks drive name @ at line @
cse	CSC	mdb	nontri_gate_drives_mdb_net_csccs	W					non-tri-state gate drives multi-driven Net at line @
cse	CSC	mdb	nontri_gate_drives_mdb_port_csccs	w					non-tri-state gate drives multi-driven Port at line @
cse	csc	mdb	nontri_gate_drives_mdb_sig_csccs	W					non-tri-state gate drives multi-driven Signal at line @
cse	CSC	mem	mem_ref_without_index_csccs	е					Memory @ referenced without index through hierarchical ID @ at line @
cse	CSC	mifc	port_identifier_mifc_csccs	е					Port @ at line @

Cat	Phase	Туре	Name	W/E V1995	V2001   Sys_ver   Csl   Desc
cse	CSC	mifc	mod_output_wire_redecl_reg_csccs	е	Module @ output port
					re-declared as type reg
					after use as implicitly declared wire at line @
cse	CSC	mifc	entity_output_wire_redecl_reg_csccs	е	Entity @ output port
					re-declared as type reg
					after use as implicitly
		.,			declared wire at line @
cse	CSC	mifc	unit_output_wire_redecl_reg_csccs	е	Unit @ output port re-declared as type reg
					after use as implicitly
					declared wire at line @
cse	CSC	mifc	output_port_is_mem_type_mifc_csccs	е	Output port @ is memory
					type at line @
cse	CSC	mifc	mifc_inout_port_is_mem_type_csccs	е	Inout port @ is memory type at line @
cse	CSC	mifc	mod_output_port_mismatch_actual_witdh_csccs	W	Module @ output port @
000	000	111110	mod_odipat_port_monatori_dotdai_witari_ooooo	"	formal to actual width
					mismatch at line @
cse	CSC	mifc	ent_output_port_mismatch_actual_witdh_csccs	W	Entity @ output port @
					formal to actual width
000	000	mifc	unit output port mismetah actual witdh acc	147	mismatch at line @ Unit @ output port @
cse	CSC	mile	unit_output_port_mismatch_actual_witdh_csc	w	formal to actual width
					mismatch at line @
cse	CSC	mifc	port_name_different_in_upper_lower_case_csccs	е	Port name @ different in
					upper lower case at line
					@
cse	CSC	mifc	port_not_def_in_iodecl_csccs	е	Port @ not defined in
		ifa	nort not def in north coope		ioDeclaration at line @
cse	CSC	mifc	port_not_def_in_portl_csccs	е	Port @ not defined in port list at line @
cse	CSC	mifc	port_wiredecl_mismatch_csccs	е	Port @ wireDeclaration
			F		mismatch at line @
cse	CSC	mifc	pos_based_null_inst_port_csccs	е	Position based null
					instance port at line @
cse	CSC	mifc	last_portdecl_contains_trailcomma_csccs	е	Last portDeclaration
					contains a trailing comma at line @
cse	CSC	mins	mins_expr_incompatible_type_csccs	е	Expression @ has an
000	000		o_oxppab.o_xypo_ssess		incompatible argument
					type @ with the port at
					line @
cse	CSC	mins	mins_mod_not_exist_csccs	е	Module @ does not exist
cse	CSC	mins	mins_entity_not_exist_csccs	е	at line @ Entity @ does not exist
030	030	1111113	mins_entity_not_exist_csccs	6	at line @
cse	CSC	mins	mins_unit_not_exist_csccs	е	Unit @ does not exist at
					line @
cse	CSC	mod	dup_declar_name_mod_cscs	е	Duplicate Declaration of
000	000	mod	ill mod nome coope		port @ at line @  Illegal module @ at line
cse	CSC	mou	ill_mod_name_csccs	е	illegal module @ at life @
cse	CSC	mod	ill_mod_entity_name_csccs	е	Illegal entity @ at line @
cse	CSC	mod	ill_mod_unit_name_csccs	е	Illegal unit @ at line @
cse	CSC	mod	mod_mult_decl_string_csccs	е	Multiple Declarations of
					string detected in module
000	000	mad	mod entity mult decl string csccs	e	@ at line @ Multiple Declarations of
cse	CSC	mod	mod_entity_muit_deci_string_csccs	е	string detected in entity
					@ at line @
cse	CSC	mod	mod_unit_mult_decl_string_csccs	е	Multiple Declarations of
					string detected in unit @
					at line @
cse	csc	mod	mod_mult_def_cscsc	е	Module @ defined in multiple places at line @
cse	csc	mod	mod ent mult def csccs	е	Entity @ defined in
030	030	mou	mod_ent_mait_del_csccs	6	multiple places at line @
cse	CSC	mod	mod_unit_mult_def_csccs	е	Unit @ defined in
-				<u>                                     </u>	multiple places at line @
cse	CSC	mod	mod_no_module_found_csccs	е	No modules found at line
					@ N :: ( ) ( ) ( ) ( )
cse	CSC	mod mod	mod_no_entity_found_csccs mod_no_unit_found_csccs	e	No entity found at line @  No unit found at line @
cse	CSC	mod	failed_find_mod_csccs	e	Failed to find module @
	303		4 4 54_55555	_	at line @
cse	csc	mod	failed_find_entity_csccs	е	Failed to find entity @ at
			7 9 1 7 1		line @
cse	CSC	mod	failed_find_unit_csccs	е	Failed to find unit @ at
CSC	CCC	mod	empty_mod_csccs	Α	line @ Empty module at line @
cse	CSC	mod	empty_mod_csccs empty_ent_csccs	e	Empty module at line @  Empty entity at line @
cse	CSC	mod	empty_unit_csccs	e	Empty unit at line @
cse	CSC	net	net_implicit_wire_redecl_reg_csccs	e	Implicitly declared as a
					wire @ re-declared as a
					reg @. at line @
			undecl_net_in_mod_csccs	е	I Indeelered not @ in
cse	CSC	net	unded_net_in_mod_esees		Undeclared net @ in
cse	csc	net	undecl_port_in_mod_csccs	e	module @ at line @ Undeclared port @ in

CSE   CSC   net	Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
Cese   Cesc   net	cse	csc	net	undecl_sig_in_mod_csccs	е					Jndeclared signal @ in module @ at line @
CSS	cse	CSC	net	undecl_net_in_ent_csccs	е					Undeclared net @ in
See   CSC   net	cse	csc	net	undecl_port_in_ent_csccs	е					Undeclared port @ in
CSE   CSC   net	cse	CSC	net	undecl_sig_in_ent_csccs	е				ι	Jndeclared signal @ in
CSB   CSC   net	cse	CSC	net	undecl_net_in_sig_csccs	е					entity @ at line @ Undeclared net @ in
Signal @ at time   Signal @ at time   Signal @ at time   Port   Sign	CSE	CSC	net	unded nort in sig caces	6					signal @ at line @
See   CSC   net   port_used_prior_to_decl_csccs   e   port_used_										signal @ at line @
CSS	cse	csc	net	undeci_sig_in_sig_csccs	е				l	signal @ at line @
line @   l	cse	CSC	net	port_used_prior_to_decl_csccs	е				1	Port @ used prior to Declaration at line @
CSE   CSC   nett   netiii_reg_name_csccs   e	cse	CSC	net	1bit_with_prts_csccs	е					1-bit with part select at line @
CSC	cse	csc	netd	ill_decl_vec_csccs	е					Illegal Declaration of
	cse	CSC	nett	nett_ill_reg_name_csccs	е				I	llegal register @ at line
csc   csc   nett   nett.   port_name_csccs   e	cse	CSC	nett	nett ill net name csccs	е					@ Illegal net @ at line @
See   CSC   nett   net_scalar_vect_nett_csccs   e   Sec   Scalar and vector a   Gec   Sec   Sec   nett   port_scalar_vect_nett_csccs   e   Port declared as tala scalar and vector a   Gec   Gec   Signal_scalar_vect_nett_csccs   e   Signal_scalar and vector a   Gec   Signal_scalar_vect_nett_csccs   e   Signal_scalar_est_nett_csccs   e   Signal_scalar_est_est_est_est_est_est_est_est_est_est	cse	CSC	nett	nett_ill_port_name_csccs	е					Illegal port @ at line @
cse csc nett port_scalar_vect_nett_csccs e scalar and vector a scalar and vector and s									II	
CSE   CSC   nett   port_scalar_vect_nett_csccs   e   Signal and vector scalar and vector a scalar and vector and s	cse	CSC	neu	net_scalar_vect_nett_csccs	е				s	calar and vector at line
CSB   CSC   nett   Signal_Scalar_vect_nett_csccs   e   Signal_declared as Scalar and vector   One hor mux can   Declared hor modules   at line @ One hor mux can   at line @ On	cse	CSC	nett	port_scalar_vect_nett_csccs	е					Port declared as both
Signal scalar vect nett   Signal vec									s	calar and vector at line
CSS	cse	CSC	nett	signal_scalar_vect_nett_csccs	е				5	Signal declared as both
used for bus connection between modules is at line @ CSE CSC nett hot_mux_not_use_bus_connection_port_csccs e										@
at line @	cse	CSC	nett	hot_mux_not_use_bus_connection_net_csccs	е					One hot mux can not be used for bus connection
CSE									b	etween modules Net @
Detween modules   Set   Set   Nett   Not_mux_not_use_bus_connection_sig_csccs   e   One hot mux can rused for bus conne between modules set   One hot mux can rused for bus conne between modules set   One hot mux can rused for bus conne between modules set   One hot mux can rused for bus conne between modules set   One hot mux can rused for bus conne between modules set   One hot allowed can ruse the provided at line set   One hot allowed sized number at line set   One hot allowed at line set   One hot aline set   One hot allowed at line set   One hot allowed at line s	cse	CSC	nett	hot_mux_not_use_bus_connection_port_csccs	е					One hot mux can not be
CSE										ised for bus connection etween modules Port @
cse csc num real_num_not_allowed_csccs e	222	csc	nett	hat muy not use his connection sig secce						
CSE   CSC   Num   Not_allowed_width0_num_csccs   e   Width 0 not allowed sized number at line   CSE   CSC   Num   Feal_num_not_allowed_csccs   e   Real numbers at line   CSE   CSC   Num   found_x_in_num_literal_csccs   e   Found x and/or z v   Number of digits ex   the width in a sized number at line   CSE   CSC   Num   too_many_digits_in_sized_num_csccs   w   Number of digits ex   the width in a sized_num_csccs   e   Divide by zero at line   CSE   CSC   Num   Child_mod_inst_parent_mod_csccs   e   Divide by zero at line   CSE   CSC   Num   Child_mod_inst_parent_mod_csccs   e   Child module (instantiates pare module (instantiates at line (instantiates sign module (instantiates sign module (instantiates at line (instantiates sign module (instantiates sign	CSE	CSC	Hell	not_max_not_use_bus_connection_sig_csccs	6				u	ised for bus connection
Sized number at lift   CSE									b	
CSE	cse	csc	num	not_allowed_width0_num_csccs	е					Width 0 not allowed for sized number at line @
CSE	cse	csc	num	real_num_not_allowed_csccs	е					Real numbers not
CSE	cse	csc	num	found_x_z_in_num_literal_csccs	е					ound x and/or z value ir
cse   csc   num   divide_by_zero_num_csccs   e   Divide by_zero at lice   Cse   csc   num   child_mod_inst_parent_mod_csccs   e   Child module @ instantiates pare module @ at line @ instantiates pare module @ at line @   Child_entity @ at line @   Child_signate   csc   csc   num   child_sig_inst_parent_sig_csccs   e   Child signate @ instantiates sign module @ at line @   csc   csc   num   int_dect_incorrect_csccs   e   Child signate   csc   csc   num   int_var_indexed_csccs   e   Integer Declarate   incorrect at line   csc   csc   num   int_var_indexed_csccs   e   Integer variable ine @   csc   csc   parm   value_of_parm_os_platform_dependent_csccs   e   Illegal parameter   line @   csc   csc   parm   value_of_parm_os_platform_dependent_csccs   w   Parameter select w   32. The value is os_platform dependent   line @   csc   csc   parm   parm_redefined_csccs   e   Illegal formal port_line @   csc   csc   csc   parm   parm_redefined_csccs   e   Illegal formal port_line @   csc   csc   csc   parm   parm_redefined_csccs   e   Illegal formal port_line @   csc   csc   csc   parm   parm_redefined_csccs   e   Illegal formal port_line @   csc   csc   csc   parm   parm_redefined_csccs   e   Illegal formal port_line @   csc   csc   csc   parm   parm_redefined_csccs   e   Illegal formal port_line @   csc   csc   csc   csc   parm   parm_redefined_csccs   e   Illegal formal port_line @   csc	cse	CSC	num	too_many_digits_in_sized_num_csccs	w					umber of digits exceeds
CSE										the width in a sized number at line @
instantiates pare module @ at line @ Child_ent_inst_parent_ent_csccs e									[	Divide by zero at line @
cse         csc         num         child_ent_inst_parent_ent_csccs         e         Child entity @ instantiates entity m @ at line @ cse csc           cse         csc         num         child_sig_inst_parent_sig_csccs         e         Child signal @ instantiates sign module @ at line instantiates sign module @ at line @ instantiates entity module @ instantiates en	CSE	CSC	Hulli	ciliu_mou_mst_parent_mou_csccs	6					instantiates parent
Cse   Csc   num   Child_sig_inst_parent_sig_csccs   e   Child_signal @ at line @ Child_signal @ instantiates sig module @ at line   cse   csc   num   int_decl_incorrect_csccs   e   Integer Declarat incorrect at line   cse   csc   num   int_var_indexed_csccs   e   Integer variable ine   at line @ at line @   cse   csc   parm   ill_parm_identifier_csccs   e   Illegal parameter   line @   Parameter select w   32. The value is Ox   platform dependent   line @   cse   csc   parm   parm_redefined_csccs   w   Parameter @ rede   at line @   cse   csc   port   ill_formal_port_name_csccs   e   Illegal formal port   line @   cse   csc   pp   text_redefined_replaced_csccs   w   Text_macro redefined_csc   fill_ename, line numb   New definition filen   line number @ at line   line number @ at line number   line number @ at line   line number @ at line number   line	cse	CSC	num	child_ent_inst_parent_ent_csccs	е					Child entity @
CSE									in	stantiates entity module
cse   csc   num   int_decl_incorrect_csccs   e   Integer Declarat incorrect at line   cse   csc   num   int_var_indexed_csccs   e   Integer variable ine   at line @   cse   csc   parm   ill_parm_identifier_csccs   e   Illegal parameter   line @   cse   csc   parm   value_of_parm_OS_platform_dependent_csccs   w   Parameter select w   32. The value is Os   platform depende   line @   cse   csc   parm   parm_redefined_csccs   w   Parameter @ rede   at line @   cse   csc   port   ill_formal_port_name_csccs   e   Illegal formal port   line @   cse   csc   port   ill_formal_port_name_csccs   e   Illegal formal port   line @   cse   csc   port   ill_formal_port_name_csccs   e   illegal formal port   line @   cse   csc   port   csc	cse	CSC	num	child_sig_inst_parent_sig_csccs	е					Child signal @
cse csc num   int_var_indexed_csccs   e   linteger variable ine at line @										module @ at line @
cse         csc         num         int_var_indexed_csccs         e         Integer variable ine at line @ at line @ line with line with line line line line line line number @ at line line number @ at line line number @ at line line line line number @ at line number with number @ at line number w	cse	CSC	num	int_decl_incorrect_csccs	е					Integer Declaration
cse     csc     parm     ill_parm_identifier_csccs     e     Illegal parameter line @       cse     csc     parm     value_of_parm_OS_platform_dependent_csccs     w     Parameter select w       32. The value is OS platform dependent line @     scsc     csc     parm     parm_redefined_csccs     w     Parameter @ rede at line @       cse     csc     port     ill_formal_port_name_csccs     e     Illegal parameter line @       cse     csc     parm     parm_redefined_csccs     w     Parameter @ rede at line @       cse     csc     port     ill_formal_port_name_csccs     e     Illegal parameter select w       at line @     e     Illegal parameter select w     scr     parameter select w       scse     csc     parameter select w     scr     rede     at line @       cse     csc     port     ill_form_dependent_csccs     e     Illegal parameter select w     scr       cse     csc     parameter select w     scr     e     Illegal parameter select w     scr       cse     csc     port     illegal parameter select w     scr     e     Illegal parameter select w       cse     csc     port     illegal parameter select w     scr     e     Illegal parameter select w       cse     csc	cse	CSC	num	int_var_indexed_csccs	е				In	teger variable inedexed
CSE	cse	CSC	parm	ill_parm_identifier_csccs	е					at line @ Illegal parameter @ at
32. The value is Of platform depende line @	cse	CSC	parm	value of parm OS platform dependent csccs	w				P	line @ arameter select width >
cse csc parm parm_redefined_csccs w Parameter @ rede at line @ till_formal_port_name_csccs e Illegal formal port line @ cse csc ppr text_redefined_replaced_csccs w Text macro redefined and replaced @ Previous definition filen numb New definition filen line number @ at lilen number	000	000	paiiii	value_or_parm_oo_planerm_aspenderm_ssees					3	2. The value is OS and
cse csc port ill_formal_port_name_csccs e Illegal formal port line @ cse csc pp text_redefined_replaced_csccs w Text macro redefi and replaced @ Previous definiti filename, line numb New definition filen line number @ at li										line @
cse     csc     port     ill_formal_port_name_csccs     e     Illegal formal port line @       cse     csc     pp     text_redefined_replaced_csccs     w     Text macro redefinant replaced @       Previous definition filen numb     Previous definition filen line number @ at line number @ at line number with line number w	cse	CSC	parm	parm_redefined_csccs	W				F	Parameter @ redefined at line @
cse csc pp text_redefined_replaced_csccs w  Text macro redefined eplaced  Previous definition filen numb New definition filen line number @ at li	cse	CSC	port	ill_formal_port_name_csccs	е					Illegal formal port @ at
Previous definiti filename, line numb New definition filen line number @ at li	cse	CSC	pp	text_redefined_replaced_csccs	w					Text macro redefined
filename, line numb New definition filen line number @ at li										and replaced @. Previous definition
line number @ at li										lename, line number @
cse csc pp endit or else without ifdef csccs e Fndif-or-else-with										ne number @ at line @
	cse	CSC	pp	endit_or_else_without_ifdef_csccs	е					Endif-or-else-without ifdef at line @
	cse	CSC	prim	z_in_prim_inst_csccs	е				Z	in primitive instantiation
	cse	CSC	prts	prts_out_of_range_csccs	е				Р	arameter @[@ : @]par

C-+	Dha	T	Nama	\A//=	V400F	V2024	Cura ···	Cal	Daga
Cat	Phase	Туре	Name	W/E	v 1995	V2001	Sys_ver	Csl	Desc select is out of range at line @
cse	CSC	prts	ill_prts_inst_array_csccs	е					Illegal value for part select of instance array
cse	CSC	prts	const_prts_contains_non_const_selector_csccs	е					'name' at line @ Constant part select @ contains a non-constant
000	200	nrto	hus index pris for year out of range cases						selector @ at line @ Bus index @ integer of
cse	CSC	prts	bus_index_prts_for_var_out_of_range_csccs	е					part select [@:@] for
									variable @ out of range at line @
cse	CSC	prts	bus_prts_for_var_out_of_range_csccs	е					Bus part select [@:@] for variable @ out of range
									at line @
cse	CSC	prts	bus_prts_index_out_of_name_for_var_csccs	е					Bus part select [@:@] index @ out of range for variable @ at line @
cse	CSC	prts	ill_token_in_prts_csccs	е					Illegal token in part select
cse	CSC	prts	incomplete_prts_specification_csccs	е					@ at line @ Incomplete part select
cse	CSC	prts	ill_index_in_prts_csccs	е					specification @ at line @ Illegal index in part select
cse	CSC	prts	negative_index_in_prts_not_allowed_csccs	е					@ at line @  Negative index in part
030	030	pito	megauve_meex_m_pns_not_anowed_cocco						select @ not allowed at line @
cse	CSC	prts	prts_index_order_reversed_csccs	е					Part select index order reversed [@ : @] [@ : @] should be [@ : @] at line
		n rin	index yes aver may aim asses						@  Vector index @ exceeds
cse	csc	prts	index_vec_over_max_size_csccs	W					the size of the vector.
cse	CSC	prts	x_or_z_in_vec_bit_select_index_csccs	е					Index truncated at line @ x or z in vector bit select
cse	CSC	scop	cse_csc_not_scope_holder	е					index at line @  @ cannot be a scope
cse	csc	scop	cse_csc_scop_id_already_defined	е					holder at line @ Id @ already defined in
			,_ ,_						scope @ at line @
cse	CSC	sdir	ignored_synopsis_csdir_csstmt_csccd	W					Ignored a synopsis case directive which is not
									applied to a Case statement at line @
cse	CSC	sdir	ignored_synopsis_csdir_miss_end_csccd	W					Ignored a synopsis case directive which is missing
									the end <directive> at line</directive>
cse	CSC	simr	inefficient_op_not_a_power_of_2_csccs	е					@ Division/modulus by a
									number not a power of 2. Inefficient simulation
cse	CSC	simr	simr_multiple_init_blk_force_csccs	W					operation. at line @ Multiple initial blocks
030	030	SIIII	3IIII_IIIuliipie_IIII_DIK_IOICe_c3cc3						force @. Unpredictable
									simulation result at line @
cse	CSC	snsl	incomplete_snsl_csccs	W					Incomplete sensitivity list.  @ is not in the sensitivity
cse	CSC	snsl	edge_sns_process_contains_data_pin_snsl_csccs	е					list. at line @ Edge sensitive process
									contains a data pin @ in the sensitivity list at line
cse	CSC	snsl	unsupp_expr_in_snsl_csccs	w					@ Unsupported Expression
									type @ in sensitivity list ' at line @
cse	CSC	snsl	partial_bus_decl_width_csccs	е	?				partial bus @ declared with width @ width @ at line @
cse	CSC	snsl	contains_inst_name_csccs	е					Contains instance name
cse	CSC	stmt	illegal_LHS	е					@ at line @ LHS expression is illegal at line @
cse	csc	stmt	null_not_allowed_stmt_csccs	е					Null statement is not allowed here at line @
cse	csc	stmt	stmt_ill_accept_only_net_reg_mem_csccs	е					Illegal type @ can only accept net, reg, memory
000	200	otmt	etmt ill gegent only port reg mem egge						at line @ Illegal type @ can only
cse	CSC	stmt	stmt_ill_accept_only_port_reg_mem_csccs	е					accept port, reg, memory at line @
cse	CSC	stmt	stmt_ill_accept_only_signal_reg_mem_csccs	е					Illegal type @ can only accept signal, reg,
cse	CSC	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_csccs	е					memory at line @ Arithmetic operator RHS
									has one less bit than the LHS at line @
cse	CSC	stmt	ar_op_unequal_lhs_rhs_csccs	е					Arithmetic operator unequal width LHS and
									RHS at line @
cse	CSC	stmt	ar_op_unequal_var_on_rhs_csc	е					Arithmetic operator

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									unequal width variables @ on RHS at line @
cse	CSC	stmt	empty_stmt_csc	е					Empty-statement at line
cse	CSC	syst	return_var_of_user_used_as_rhs_csccs	w					Return variable of user system task is used as a
cse	CSC	task	ask_var_not_decl_csccs	е					RHS variable at line @ Variable @ used but not
cse	CSC	task	too_few_arg_to_task_csccs	е					declared at line @ Too few arguments
cse	CSC	tri	instance_not_tri_state_device_csccs	е					passed to task @ at line @ Instance name is not a
cse	CSC	tri	unsupp_gate_type_tristate_csccs	е					Unsupported gate type
		tri	tri not doorn goto contention space						@ used for tristate at line @
cse	CSC	ui	tri_not_desgn_gate_contention_csccs	е					Tristate not designed correctly gate @ can cause contention at line @
cse	CSC	tri	unsupp_type_instance_tri_csccs	е					Unsupported type instance type used for tristate @ at line @
cse	csc	tri	incorrect_cont_assign_stmt_tri_gate_csccs	е					Incorrect continuous assign statement for tristate gate @ at line @
cse	csc	tri	const_assign_to_multidriven_net_csccs	е					Constant (constiznt) assigned to multi-driven
cse	csc	tri	const_assign_to_multidriven_port_csccs	е					Net @ at line @ Constant (constiznt) assigned to multi-driven
cse	CSC	tri	const_assign_to_multidriven_signal_csccs	е					Port @ at line @ Constant (constiznt) assigned to multi-driven
cse	CSC	tri	unsupp_expr_for_tri_csccs	е					Signal @ at line @ Unsupported Expression type @ for tristate at line
cse	csc	vec	vec_invalid_csccs	е					@ Vector @ is invalid. at line @
cse	CSC	vec	vec_mod_not_exist_csccs	е					Vector @ module name does not exist at line @
cse	csc	vec	vec_ent_not_exist_csccs	е					Vector @ entity name does not exist at line @
cse	CSC	vec	vec_unit_not_exist_csccs	е					Vector @ unit name does not exist at line @
cse	CSC	vec	vec_not_contain_data_sig_csccs	е					Vector @ does not contain any data signals at line @
cse	CSC	vec	vec_not_contain_clk_sig_csccs	е					Vector @ does not contain a clock signal at line @
cse	CSC	vec	vec_not_contain_rst_sig_csccs	е					Vector @ does not contain a reset signal at line @
cse	CSC	vec	vec_stim_not_contain_input_ports_csccs	е					Vector @ which is a stimulus vector does not contain any input ports at
cse	CSC	vec	vec_expect_not_contain_outputs_ports_csccs	е					line @ Vector @ which is an expect vector does not contain any output ports
cse	CSC	vec	vec_is_missing_the_csccs	е					at line @  Vector @ is missing the @ at line @
cse	csc	vec	vec_dtsig_not_found_csccs	е					Vector @ data signals @ not found at line @
cse	CSC	vec	vec_clk_sig_not_found_csccs	е					Vector @ clock signal @ not found at line @
cse	CSC	vec	vec_rst_sig_not_found_csccs	е					Vector @ reset signal @ not found at line @
cse	CSC	vec	vec_stim_input_port_not_found_csccs	е					Vector @ stimulus vector input port @ not found at line @
cse	csc	vec	vec_output_port_not_found_csccs	е					Vector @ output port @ not found at line @
cse	csp	ccd	CSL_out_ccd	е				х	CSL directive outside of module at line @
cse	csp	ccd	ill_pos_CSLC_ccd_mod_csc	е				х	Illegal position for CSLC directive in module name
cse	csp	ccd	ill_pos_CSLC_ccd_ent_csc	е				Х	at line @ Illegal position for CSLC directive in entity name at line @
cse	csp	ccd	ill_pos_CSLC_ccd_unit_csc	е				х	Illegal position for CSLC directive in unit name at line @
cse	csp	ccd	misplaced_csdir_ignored_cscs	е				Х	Lower case directive in wrong location. Ignored at line @

Cat	Phase	Туре	Name	W/E	V1995   V2001   Sys_ver   Csl   Desc
cse	csp	clk	clk_file_cannot_open_cscs	е	Clock file @ cannot be
cse	csp	clk	no_clk_source_specified_clk_cscs	е	opened at line @ No clock source
					specified clock @ at line
cse	csp	cmdl	ill_cmdl_uselib_dir_path_cscs	е	Illegal 'uselib directory
					path @ no such directory at line @
cse	csp	cmnt	cse_csp_cmnt_miss_closing_cscs	е	/* comment missing
cse	csp	csi	miss_char_case_cscs	е	closing */ at line @ Missing character @ at
					line @
cse	csp	expr	malformed_unary_expr_ccsp	е	Malformed unary Expression @ at line @
cse	csp	expr	malformed_binary_expr_ccsp	е	Malformed binary Expression @ at line @
cse	csp	expr	malformed_ternary_expr_ccsp	е	Malformed ternary
cse	csp	expr	expr_s_cse	е	Expression @ at line @ Expression S at line @
cse	csp	expr	expr_found_reserved_word_cscs	е	Expected identifier but
					found reserved word @ at line @
cse	csp	expr	expr_concatenation_empty_cscs	е	Concatenation empty at line @
cse	csp	expr	ill_operator_expr_cscs	е	Illegal operator @ at line
cse	csp	expr	ill operand expr cscs	е	@ Illegal operand @ at line
		·	_, _,_		@
cse	csp	file	cannot_open_file_cscs	е	Cannot open file @ at line @
cse	csp	file	line_lenght_overflow_cscs	е	Line length overflow line_length @ at line @
cse	csp	file	environ_var_in_filel_cscs	е	Environ variable in file list
cse	csp	func	fct_non_block	е	at line @ Function definition
030	СОР	Turic	loc_non_block		contains non-blocking
cse	csp	func	undefined_func_cscs	е	assignment at line @ Undefined function @ at
					line @ Illegal module instance
cse	csp	inst	ill_mod_inst_name_cscs	е	@ at line @
cse	csp	inst	ill_entity_inst_name_cscs	е	Illegal entity instance @ at line @
cse	csp	inst	ill_unit_inst_name_cscs	е	Illegal unit instance @ at
cse	csp	lib	not_open_lib_file_csc	е	line @ Cannot open library file
cse	csp	list	trail_comma_list_css	е	@ at line @ Trailing comma in
036	СЭР	list	tran_comma_nst_css	6	parentheses enclosed list
cse	csp	list	list_miising_comma_cscs	w	at line @  Missing comma between
			3		@ and name at line @
cse	csp	mem	unknown_latch_in_latch_array_decl_	е	Unknown latch type in latch-array declaration at
cse	csp	mifc	mifc port type unsupported cscs	е	line @ Port type @ unsupported
	-				at line @
cse	csp	mmod	mult_css_arg_div	е	Macro @ contains too many actual arguments
000	200	mmod	mice are div		at line @  Macro @ is missing
cse	csp	mmou	miss_css_arg_div	е	some actual arguments
cse	csp	mmod	not else css div	е	at line @ Unmatched 'else
					directive at line @
cse	csp	mmod	not_endif_css_div	е	Unmatched 'endif directive at line @
cse	csp	mmod	not_include_css_div	е	Missing filename for
					'include directive at line @
cse	csp	mmod	bad_include_css_div	е	Badly formed include directive at line @
cse	csp	mmod	fmis_include_css_div	е	Filename missing in
					#include directive at line @
cse	csp	mod	mod_miss_endmodule_cscs	е	Missing endmodule at line @
cse	csp	mod	mod_no_module_found_cscs	е	No modules found at line
cse	csp	mod	mod_no_entity_found_cscs	е	@ No entity found at line @
cse	csp	mod	mod_no_unit_found_cscs	е	No unit found at line @
cse	csp	nett	nett_unsupported_reg_cscs	е	Unsupported register type @ at line @
cse	csp	num	radix_h_num_css	ew	Illegal number radix, 'h expected at line @
cse	csp	num	radix_b_num_css	ew	Illegal number radix, 'b
cse	csp	num	radix_d_num_css	ew	expected at line @ Illegal number radix, 'd
	·				expected at line @
cse	csp	num	radix_o_num_css	ew	Illegal number radix; 'o

See   Gisp   Daris	Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
Gel Gsp pp pp_cannot_open_file_not_have_read_perm_cscs	cse	csp	pars	S_stmt_pars_cs	е					expected at line @ Statement S at line @
Case	cse	csp	port	ill_formal_port_name_cscs	е					Illegal formal port @ at line @
Camord open included   Fine   Camord open included   Camord open included   Fine   Fin	cse	csp	pp	pp_cannot_open_file_not_exist_csc	е					Cannot open include file @, file does not exist at
See   CSP   PP	cse	csp	pp	pp_cannot_open_file_not_have_read_perm_cscs	е					Cannot open include file @, file does not have
CSP   DPTS   Define_III_Prist_CSC   E   Silegal part select   Spocifier, doften emissing, at time (iii)   Spocifier, and time (iii)   Spocif	cse	csp	pp	include_filne	е					
ce csp prts prts_part_select_cass e all and prompted part select_cass e sit me get at the get at th	cse	csp	prts	define_ill_prts_csc	е					
See   Cap   Stimt   miss_comma_stimt_cas   e   Missing_somm_a aline (6   Cap   Cap   Stimt   miss_comma_stimt_cas   e   Missing_somm_a aline (6   Cap   Cap   Stimt   miss_comma_stimt_cas   e   Missing_somm_a aline (6   Cap   C		200	n. w4.0	pute pout extent acce						
CSS   CSS   SIMT		•	•	. – –						at line @
Case   Casp   Simit   miss_char_stmt_cas   e   Missing dist line (@ Case   Casp   Simit   missing_atiline (Se   Cannot be pared at line (@ Cannot be	_									Missing semi colon at
CSP   SIMIT	_				_					Missing @ at line @
cse csp simt unparasible e Cse csp simt null_not_allowed_simt_cscs e Cse csc csp simt null_not_allowed_simt_cscs e Cse csc csc csc csc csc csc csc csc csc c		-			_					Equal sign missing at line
cse csp stmt unparsable e Cannot be parsed at line @ cse csp stmt null_not_allowed_stmt_cscs e Multistatement is not allowed better at line @ cse csp stmt of the color of the	cse	csp	stmt	illegal_semi_colon	е					Null (semi colon) found in
csp stmt null_not_allowed_stmt_cscs	cse	csp	stmt	unparsable	е					Cannot be parsed at line
CSP   Stf   III_Stf_Char_found_cscs   e   allegal character @ found cscs   csp   udir   other_cdir_cscs   w   found other compiler backslash at line @ cse   prp   file   not_dir_name_file_csp   e   Directory@ does not   exist at line @ cse   prp   file   cannot_open_file_ppcs   e   Directory@ does not   exist at line @ cse   prp   prp   not_ind_directive_pp_ppcs   e   Empty lifename for   include directive at line @ include directive at line include directive directive include directive include direct	cse	csp	stmt	null_not_allowed_stmt_cscs	е					Null statement is not
CSP   Udir   Other_cdif_cscs   W   Found offer compiler	cse	csp	str	ill_str_char_found_cscs	е					Illegal character @ found
CSE   PTP   File   Cannot_open_file_csp   e   Directory @ dees not exist at line @ Cannot_open_file_ppcs   e   Cannot_open_file @ Cannot_open_file_file_ppcs   e   Missing macro name at line @ Cannot_open_file_file_ppcs   e   Missing macro name @ Compress open_file @ Cannot_open_file_file_ppcs   e   Missing macro name @ Compress_file @ Cannot_open_file_file_ppcs   e   Cannot_open_file_file_file_file_file_file_file_file	cse	csp	udir	other_cdir_cscs	w					Found other compiler
Cannot open file   Cannot open	cse	prp	file	not_dir_name_file_csp	е					Directory @ does not
See   prp   pp   pp   not_incl_directive_pp_ppcs   e	cse	prp	file	cannot_open_file_ppcs	е					
See   prp   pp   pp_miss_macroname_cs   e	cse		DD	not incl directive pp ppcs	е					
CSE   Prp   Pp   Pp_miss_macroname_cs   e		P.P	PP							'include directive at line
CSE   PTP	cse	prp	pp	pp_miss_macroname_cs	е					Missing macro name at
CSE   PTP   PP   PP   PP_CANTO_OPEN_IBBITE_PDCS   E   Cannot open_IBBITE_PTE_CAS   E   PTP   PP   PP   PP_CANTO_OPEN_IBBITE_PDCS   E   CANTO OPEN_IBBITE_PTE_CAS   E   CANTO OPEN_IBBITE_CAS   E   CANTO OPE	cse	prp	pp	ill_macroname_pp_cs	е					Illegal macro name @ at
CSE   PTP   PP   PP_IENT_MACTONAME_NOT_CHANNED.   CSE   PTP   PP   PP_IENT_MACTONAME_NOT_CHANNED.   CSE   PTP   PP   PP   PP_IENT_MACTONAME_NOT_CHANNED.   CSE   PTP   PP   PP   PP_IENT_MACTONAME_PDCS   PTP   PP   PP   PP   PP   PP   PP	cse	prp	pp	pp_text_macro_rec_cs	е					Text macro string used recursively at line @
cse prp pp pp_ifdef_miss_macroname_ppcs e	cse	prp	pp	pp_cannot_open_libfile_ppcs	е					
cse         prp         pp         pp_lfdef_miss_macroname_ppcs         e         "ifdef missing macroname at line @           cse         prp         pp         pp_undef_miss_macroname_ppcs         e         undef missing macroname at line @           cse         prp         pp         pp_undef_miss_macroname_ppcs         e         Missing endif directive a line @           cse         prp         pp         pp_miss_endif_directive_ppcs         e         Missing endif directive a line @           cse         prp         pp         pp_rec_include_file_ppcs         e         Recursive INCLUDE file @ at line @           cse         prp         pp         cmdl_arg_used_in_def_ppcs         e         Command line argumen used in define at line @           cse         prp         pp         pp_undef_macro_ppcs         e         Undef @ not defined macro at line @           cse         prp         pp         pp_undef_macro_ppcs         e         Include file @ not found at line @           cse         vep         ccd         ill_pos_CSLC_ccd_mod_vec         e         x         Illegal position for CSLC directive in module name at line @           cse         vep         ccd         ill_pos_CSLC_ccd_ent_vec         e         x         Illegal position for CSLC directive in module name at line @ <td>cse</td> <td>prp</td> <td>pp</td> <td>pp_text_macroname_not_defined_ppcs</td> <td>е</td> <td></td> <td></td> <td></td> <td></td> <td>Text macro (name) not defined at line @</td>	cse	prp	pp	pp_text_macroname_not_defined_ppcs	е					Text macro (name) not defined at line @
cse         prp         pp         pp_undef_miss_macroname_ppcs         e         'undef missing macroname at line @ name at line @ name at line @ Missing endif directive a line @ line @ line @ at line @ case prp         pp         pp_miss_endif_directive_ppcs         e         Missing endif directive a line @ line @ at line @ line @ at line @ line @ case prp         pp         pp_miss_endif_directive ppcs         e         Recursive INCLUDE file @ at line @ line @ case prp         pp         pp_miss_end_in_def_ppcs         e         Recursive INCLUDE file @ at line @ case prp         command line argumen used in define at line @ macro at line @ line @ to line @ at line @ at line @ case vep         Undef @ not defined macro at line @ to line @ to line @ to line @ at line @ case vep         x         Illegal position for CSLC directive in module nam at line @ at	cse	prp	pp	pp_ifdef_miss_macroname_ppcs	е					'ifdef missing macro
cse         prp         pp         pp_miss_endif_directive_ppcs         e         Missing 'endif directive e line @ line @ line @ at line @ command line argument           cse         prp         pp         cmdl_arg_used_in_def_ppcs         e         Command line argument used in define at line @ command line argument used in define at line @ used in defined macro at line @ macro at line @ macro at line @ include file @ not defined macro at line @ line @ to line	cse	prp	pp	pp_undef_miss_macroname_ppcs	е					'undef missing macro
cse         prp         pp         pp_rec_include_file_ppcs         e         Recursive INCLUDE file @ at line @           cse         prp         pp         cmdl_arg_used_in_def_ppcs         e         Command line argumen used in define at line @           cse         prp         pp         pp_undef_macro_ppcs         e         Undef @ not defined macro at line @           cse         prp         pp         include_file         e         Include file @ not founce at line @           cse         vep         ccd         ill_pos_CSLC_ccd_mod_vec         e         x         Illegal position for CSLC directive in module name at line @           cse         vep         ccd         ill_pos_CSLC_ccd_ent_vec         e         x         Illegal position for CSLC directive in unit name at line @           cse         vep         ccd         ill_pos_CSLC_ccd_unit_vec         e         x         Illegal position for CSLC directive in unit name at line @           cse         vep         ccd         misplaced_csdir_ignored_vecs         e         x         Lower case directive in unit name a line @           cse         vep         clk         clk_file_cannot_open_vecs         e         x         Lower case directive in module name at line @           cse         vep         clk         clk_file_cannot_op	cse	prp	pp	pp_miss_endif_directive_ppcs	е					Missing 'endif directive at
cse prp pp pp cmdl_arg_used_in_def_ppcs e	cse	prp	pp	pp_rec_include_file_ppcs	е					Recursive INCLUDE file
CSE   Prp   Pp   Pp   Pp_undef_macro_ppcs   e   Undef @ not defined macro at line @ cse   Prp   Pp   include_filne   e   Include file @ not found at line @ cse   Vep   Ccd   ill_pos_CSLC_ccd_mod_vec   e   X   Illegal position for CSLC directive in module nam at line @ cse   Vep   Ccd   ill_pos_CSLC_ccd_ent_vec   e   X   Illegal position for CSLC directive in entity name at line @ cse   Vep   Ccd   ill_pos_CSLC_ccd_unit_vec   e   X   Illegal position for CSLC directive in unit name a line @ cse   Vep   Ccd   misplaced_csdir_ignored_vecs   e   X   Lower case directive in wrong location. Ignored at line @ cse   Vep   Clk   Clk_file_cannot_open_vecs   e   Clock file @ cannot be opened at line @ cse   Vep   Clk   no_clk_source_specified_clk_vecs   e   No clock source specified clock @ at line @ cse   Vep   Cmdl   ill_cmdl_uselib_dir_path_vecs   e   Illegal 'uselib directory path @ no such directory path @ no such directory at line @ cse   Vep   Cmnt   cse_vep_cmnt_miss_closing_vecs   e   Missing character @ at line @ cse   Vep   Csi   miss_char_case_vecs   e   Missing character @ at line @ cse   Vep   Csi   miss_char_case_vecs   e   Missing character @ at line @ cse   Vep   Csi   miss_char_case_vecs   E   Missing character @ at line @ cse   Vep   Csi   Missing character @ at line @ cse   Vep   Csi   Missing character @ at line @ cse   Vep   Csi   Missing character @ at line @ cse   Vep   Csi   Missing character @ at line @ cse   Vep   Csi   Vep   Cs	cse	prp	pp	cmdl_arg_used_in_def_ppcs	е					Command line argument
CSE	cse	prp	pp	pp_undef_macro_ppcs	е					Undef @ not defined
CSE	cse	prp	pp	include_filne	е					Include file @ not found
cse vep ccd ill_pos_CSLC_ccd_ent_vec e	cse	vep	ccd	ill_pos_CSLC_ccd_mod_vec	е				Х	Illegal position for CSLC
directive in entity name at line @   x   Illegal position for CSLC   directive in unit name at line @   x   Lower case directive in unit name at line @   x   Lower case directive in unit name at line @   x   Lower case directive in wrong location. Ignored at line @   x   Lower case directive in wrong location. Ignored at line @   cse   vep   clk   clk_file_cannot_open_vecs   e   Clock file @ cannot be opened at line @   No clock source specified_clk_vecs   e   No clock source specified_clk_vecs   e   Illegal 'uselib directory path @ no such directory path @ no such directory path @ no such directory at line @   cse   vep   cmnt   cse_vep_cmnt_miss_closing_vecs   e   /* comment missing closing */ at line @   cse   vep   csi   miss_char_case_vecs   e   Missing character @ at   cse   miss_char_case_vecs   cse   Missing character @ at   cse										
cse   vep   ccd   ill_pos_CSLC_ccd_unit_vec   e   x   Illegal position for CSLC directive in unit name a line @   cse   vep   ccd   misplaced_csdir_ignored_vecs   e   x   Lower case directive in wrong location. Ignored at line @   cse   vep   clk   clk_file_cannot_open_vecs   e   Clock file @ cannot be opened at line @   cse   vep   clk   no_clk_source_specified_clk_vecs   e   No clock source specified clock @ at line @   cse   vep   cmd  ill_cmdl_uselib_dir_path_vecs   e   Illegal 'uselib directory path @ no such directory path @ no such director at line @   cse   vep   cmnt   cse_vep_cmnt_miss_closing_vecs   e   /* comment missing closing */ at line @   cse   vep   csi   miss_char_case_vecs   e   Missing character @ at   miss_character @ at   miss_characte	cse	vep	ccd	ill_pos_CSLC_ccd_ent_vec	е				Х	Illegal position for CSLC directive in entity name
cse         vep         ccd         misplaced_csdir_ignored_vecs         e         x         Lower case directive in wrong location. Ignored at line @           cse         vep         clk         clk_file_cannot_open_vecs         e         Clock file @ cannot be opened at line @           cse         vep         clk         no_clk_source_specified_clk_vecs         e         No clock source specified clock @ at line @           cse         vep         cmdl         ill_cmdl_uselib_dir_path_vecs         e         Illegal 'uselib directory path @ no such directory path @ no such directory path @ no such director at line @           cse         vep         cmnt         cse_vep_cmnt_miss_closing_vecs         e         /* comment missing closing */ at line @           cse         vep         csi         miss_char_case_vecs         e         Missing character @ at	cse	vep	ccd	ill_pos_CSLC_ccd_unit_vec	е				Х	Illegal position for CSLC directive in unit name at
cse vep clk clk_file_cannot_open_vecs e Clock file @ cannot be opened at line @ cse vep clk no_clk_source_specified_clk_vecs e No clock source specified clock @ at line @ No clock source specified clock @ at line @ at line @ cse vep cmd ill_cmdl_uselib_dir_path_vecs e Illegal 'uselib directory path @ no such director at line @ cse vep cmnt cse_vep_cmnt_miss_closing_vecs e /* comment missing closing */ at line @ cse_vep_csi miss_char_case_vecs e Missing character @ at line @ cse_vep_csi miss_char_case_vecs e Missing character @ at line @ cse_vep_csi miss_char_case_vecs e Missing character @ at line @ cse_vep_csi miss_char_case_vecs e Missing character @ at line @ cse_vep_csi miss_char_case_vecs e Missing character @ at line @ cse_vep_csi miss_char_case_vecs e Missing character @ at line @ cse_vep_csi miss_char_case_vecs	cse	vep	ccd	misplaced_csdir_ignored_vecs	е				х	
cse vep clk no_clk_source_specified_clk_vecs e				· · · · · · ·						wrong location. Ignored at line @
cse     vep     clk     no_clk_source_specified_clk_vecs     e     No clock source specified clock @ at line @       cse     vep     cmdl     ill_cmdl_uselib_dir_path_vecs     e     Illegal 'uselib directory path @ no such directory path @ no such director at line @       cse     vep     cmnt     cse_vep_cmnt_miss_closing_vecs     e     /* comment missing closing */ at line @       cse     vep     csi     miss_char_case_vecs     e     Missing character @ at	cse	vep	clk	clk_file_cannot_open_vecs	е					Clock file @ cannot be opened at line @
cse     vep     cmdl     ill_cmdl_uselib_dir_path_vecs     e     Illegal 'uselib directory path @ no such directory path @ no such director at line @       cse     vep     cmnt     cse_vep_cmnt_miss_closing_vecs     e     /* comment missing closing */ at line @       cse     vep     csi     miss_char_case_vecs     e     Missing character @ at	cse	vep	clk	no_clk_source_specified_clk_vecs	е					No clock source specified clock @ at line
cse vep cmnt cse_vep_cmnt_miss_closing_vecs e /* comment missing closing */ at line @  cse vep csi miss_char_case_vecs e Missing character @ at	cse	vep	cmdl	ill_cmdl_uselib_dir_path_vecs	е					Illegal 'uselib directory
closing */ at line @ cse vep csi miss_char_case_vecs e Missing character @ at										
cse vep csi miss_char_case_vecs e Missing character @ at	cse	vep	cmnt	cse_vep_cmnt_miss_closing_vecs	е					closing */ at line @
	cse	vep	csi	miss_char_case_vecs	е					Missing character @ at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	vep	expr	malformed_unary_expr_cvep	е					Malformed unary Expression @ at line @
cse	vep	expr	malformed_binary_expr_cvep	е					Malformed binary Expression @ at line @
cse	vep	expr	malformed_ternary_expr_cvep	е					Malformed ternary
cse	vep	expr	expr_found_reserved_word_vecs	е					Expression @ at line @ Expected identifier but
									found reserved word @ at line @
cse	vep	expr	expr_concatenation_empty_vecs	е					Concatenation empty at line @
cse	vep	expr	ill_operator_expr_vecs	е					Illegal operator @ at line
cse	vep	expr	ill_operand_expr_vecs	е					@ Illegal operand @ at line
cse	vep	file	cannot_open_file_vecs	е					Cannot open file @ at
cse	vep	file	line_lenght_overflow_vecs	е					line @ Line length overflow
cse	vep	file	environ_var_in_filel_vecs	е					line_length @ at line @ Environ variable in file list
cse	vep	func	undefined_func_vecs	е					at line @ Undefined function @ at
cse	vep	inst	ill_mod_inst_name_vecs	е					line @ Illegal module instance
	•								@ at line @
cse	vep	inst	ill_entity_inst_name_vecs	е					Illegal entity instance @ at line @
cse	vep	inst	ill_unit_inst_name_vecs	е					Illegal unit instance @ at line @
cse	vep	lib	not_open_lib_file_vec	е					Cannot open library file @ at line @
cse	vep	list	trail_comma_list_csc	е					Trailing comma in parentheses enclosed list
000	VOD	list	liet mileing commo vece	14/					at line @ Missing comma between
cse	vep		list_miising_comma_vecs	W					@ and name at line @
cse	vep	mem	latch_type_miss_in_latch_array_decl_	е					Latch type missing ' in latch-array declaration at
cse	vep	mifc	mifc_port_type_unsupported_vecs	е					line @ Port type @ unsupported
cse	vep	mmod	mult_csc_arg_div	е					at line @ Macro @ contains too
									many actual arguments at line @
cse	vep	mmod	miss_csc_arg_div	е					Macro @ is missing some actual arguments
			and also are div						at line @
cse	vep	mmod	not_else_csc_div	е					Unmatched 'else directive at line @
cse	vep	mmod	not_endif_csc_div	е					Unmatched 'endif directive at line @
cse	vep	mmod	not_include_csc_div	е					Missing filename for 'include directive at line
cse	vep	mmod	bad include csc div	е					@ Badly formed include
cse	vep	mmod	fmis include csc div	е					directive at line @ Filename missing in
000									#include directive at line
cse	vep	mod	mod_miss_endmodule_vecs	е					Missing endmodule at
cse	vep	mod	mod_no_module_found_vecs	е					line @ No modules found at line
cse	vep	mod	mod_no_entity_found_vecs	е					@ No entity found at line @
cse	vep	mod nett	mod_no_unit_found_vecs nett_unsupported_reg_vecs	e e					No unit found at line @ Unsupported register
	•								type @ at line @  Illegal number radix, 'h
cse	vep	num	radix_h_num_csc	ew					expected at line @
cse	vep	num	radix_b_num_csc	ew					Illegal number radix, 'b expected at line @
cse	vep	num	radix_d_num_csc	ew				L	Illegal number radix, 'd expected at line @
cse	vep	num	radix_o_num_csc	ew					Illegal number radix; 'o expected at line @
cse	vep	port	ill_formal_port_name_vecs	е					Illegal formal port @ at line @
cse	vep	pp	pp_cannot_open_file_not_exist_vecs	е					Cannot open include file @, file does not exist at
000	1/67	n=	pp connet onen file net begg read never						line @
cse	vep	pp	pp_cannot_open_file_not_have_read_perm_vecs	е					Cannot open include file @, file does not have
									read permission at line @
cse	vep	prts	define_ill_prts_vec	е					Illegal part select specifier, define missing
cse	vep	prts	prts_part_select_vecs	е					at line @ Badly formed part select
cse	vep	stmt	miss_comma_stmt_csc	е					at line @ Missing comma at line @
036	4eh	JUIIL	111100_00111111a_3t111t_030		L	L	l .	1	imosing comma at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
cse	vep	stmt	miss_semicolon_stmt_csc	е			-		Missing semi colon at line @
cse	vep	stmt	miss_char_stmt_csc	е					Missing @ at line @
cse	vep vep	stmt stmt	wait_kword_stmt_csc null_not_allowed_stmt_vecs	e e					@ expected at line @ Null statement is not
CSE	veb			6					allowed here at line @
cse	vep	str	ill_str_char_found_vecs	е					Illegal character @ found after backslash at line @
cse	vep	udir	other_cdir_vecs	W					Found other compiler
cse	vhp	ccd	ill_pos_CSLC_ccd_mod_vhc	е				Х	directive at line @ Illegal position for CSLC
	'								directive in module name
cse	vhp	ccd	ill_pos_CSLC_ccd_ent_vhc	е				х	at line @ Illegal position for CSLC
									directive in entity name at line @
cse	vhp	ccd	ill_pos_CSLC_ccd_unit_vhc	е				х	Illegal position for CSLC
									directive in unit name at line @
cse	vhp	ccd	misplaced_csdir_ignored_vhcs	е				х	Lower case directive in
									wrong location. Ignored at line @
cse	vhp	clk	clk_file_cannot_open_vhcs	е					Clock file @ cannot be opened at line @
cse	vhp	clk	no_clk_source_specified_clk_vhcs	е					No clock source
									specified clock @ at line @
cse	vhp	cmdl	ill_cmdl_uselib_dir_path_vhcs	е					Illegal 'uselib directory
									path @ no such directory at line @
cse	vhp	cmnt	cse_vhp_cmnt_miss_closing_vhcs	е					/* comment missing
cse	vhp	csi	miss_char_case_vhcs	е					closing */ at line @ Missing character @ at
									line @ Malformed unary
cse	vhp	expr	malformed_unary_expr_cvhp	е					Expression @ at line @
cse	vhp	expr	malformed_binary_expr_cvhp	е					Malformed binary Expression @ at line @
cse	vhp	expr	malformed_ternary_expr_cvhp	е					Malformed ternary
cse	vhp	expr	expr_found_reserved_word_vhcs	е					Expression @ at line @ Expected identifier but
000	VIIP	ОДР	CAPI_IOUNG_IOSOTVOG_WOIG_VIIOS						found reserved word @
cse	vhp	expr	expr_concatenation_empty_vhcs	е					at line @ Concatenation empty at
		-	, -						line @
cse	vhp	expr	ill_operator_expr_vhcs	е					Illegal operator @ at line @
cse	vhp	expr	ill_operand_expr_vhcs	е					Illegal operand @ at line @
cse	vhp	file	cannot_open_file_vhcs	е					Cannot open file @ at
cse	vhp	file	line_lenght_overflow_vhcs	е					line @ Line length overflow
	•								line_length @ at line @
cse	vhp	file	environ_var_in_filel_vhcs	е					Environ variable in file list at line @
cse	vhp	func	undefined_func_vhcs	е					Undefined function @ at line @
cse	vhp	inst	ill_mod_inst_name_vhcs	е					Illegal module instance
cse	vhp	inst	ill_entity_inst_name_vhsc	е					@ at line @ Illegal entity instance @
			_ ,						at line @
cse	vhp	inst	ill_unit_inst_name_vhcs	е					Illegal unit instance @ at line @
cse	vhp	lib	not_open_lib_file_vhc	е					Cannot open library file @ at line @
cse	vhp	list	trail_comma_list_csh	е					Trailing comma in
									parentheses enclosed list at line @
cse	vhp	list	list_miising_comma_vhcs	W					Missing comma between
cse	vhp	mem	clk_name_miss_in_latch_array_decl_	е					@ and name at line @ Clock name missing in
	٩								latch-array directive
cse	vhp	mifc	mifc_port_type_unsupported_vhcs	е					declaration at line @ Port type @ unsupported
cse	vhp	mmod	mult_csh_arg_div	е					at line @ Macro @ contains too
CSE	νιιρ	minou	muit_csn_aig_uiv	6					many actual arguments
cse	vhp	mmod	miss_csh_arg_div	е					at line @ Macro @ is missing
	٩		55_5555_517						some actual arguments
cse	vhp	mmod	not_else_csh_div	е					at line @ Unmatched 'else
	•								directive at line @
cse	vhp	mmod	not_endif_csh_div	е	L				Unmatched 'endif directive at line @
cse	vhp	mmod	not_include_csh_div	е					Missing filename for 'include directive at line
									@
cse	vhp	mmod	bad_include_csh_div	е					Badly formed include directive at line @
	l		l .		1		1	L	

Cat	Phase vhp	Type mmod	Name fmis_include_csh_div	W/E	V1995	V2001	Sys_ver	Csl	Desc Filename missing in #include directive at line
cse	vhp	mod	mod_miss_endmodule_vhcs	е					@ Missing endmodule at line @
cse	vhp	mod	mod_no_module_found_vhcs	е					No modules found at line
cse	vhp vhp	mod mod	mod_no_entity_found_vhcs mod_no_unit_found_vhcs	e e					No entity found at line @ No unit found at line @
cse	vhp	nett	nett_unsupported_reg_vhcs	е					Unsupported register type @ at line @
cse	vhp	num	radix_h_num_csh	ew					Illegal number radix, 'h expected at line @
cse	vhp	num	radix_b_num_csh	ew					Illegal number radix, 'b expected at line @
cse	vhp	num	radix_d_num_csh	ew					Illegal number radix, 'd expected at line @
cse	vhp	num	radix_o_num_csh	ew					Illegal number radix; 'o expected at line @
cse	vhp	port	ill_formal_port_name_vhcs	е					Illegal formal port @ at line @
cse	vhp	рр	pp_cannot_open_file_not_exist_vhcs	е					Cannot open include file @, file does not exist at line @
cse	vhp	pp	pp_cannot_open_file_not_have_read_perm_vhcs	е					Cannot open include file @, file does not have read permission at line @
cse	vhp	prts	define_ill_prts_vhc	е					Illegal part select specifier, define missing at line @
cse	vhp	prts	prts_part_select_vhcs	е					Badly formed part select at line @
cse	vhp	stmt	miss_comma_stmt_csh	е					Missing comma at line @
cse	vhp	stmt	miss_semicolon_stmt_csh	е					Missing semi colon at line @
cse	vhp vhp	stmt stmt	miss_char_stmt_csh wait_kword_stmt_csh	e					Missing @ at line @ @ expected at line @
cse	vhp	stmt	null_not_allowed_stmt_vhcs	е					Null statement is not allowed here at line @
cse	vhp	str	ill_str_char_found_vhcs	е					Illegal character @ found after backslash at line @
cse	vhp	udir	other_cdir_vhcs	W					Found other compiler directive at line @
CSW	csp	stmt	long_line	W				х	Line too long, maximum line size is @ characters at line @
dee	cda	ccd	dupl_filter_dir_cdde	W				Х	Duplicated filter directive @ at line @
dee	cda	ccd	unused_filter_dir_cdde	W				х	Unused filter directive @ at line @
dee	cda	ccd	ill_filter_dir_cdde	W				Х	Illegal filter directive @ at line @
dee	cda	clk	clk_array_latches_cannot_mix_latch_types	е					Array-latches which use multiple clocks cannot mix latch types at line @
dee	cda	clk	latch_not_connected_clk_cdde	е					Latch not connected to a clock pin. at line @
dee	cda	clk	FF_not_connected_clk_cdde	е					FF not connected to a clock pin. at line @
dee	cda	clk	clk_source_not_vec_bit_cdde	е					Clock source @ cannot be a vector bit at line @
dee	cda	clk	clk_driven_by_net_cdde	е					The clock source @ is not driven by a clock and is driven by net @. Inferring a net type instead of clock per the clock directive. at line @
dee	cda	clk	clk_driven_by_port_cdde	е					The clock source @ is not driven by a clock and is driven by port @. Inferring a port type instead of clock per the clock directive. at line @
dee	cda	clk	clk_driven_by_signal_cdde	е					The clock source @ is not driven by a clock and is driven by signal @. Inferring a signal type instead of clock per the clock directive. at line @
dee	cda	clk	clk_should_drive_clk_cdde	е					A clock should drive clock @. at line @
dee	cda	clk	clk_source_def_contains_clk_cdde	е					Clock source definition contains a clock at line @
dee	cda	clk	cannot_open_clk_filename_cdde	е					Cannot open the clock file filename at line @
dee	cda	clk	clk_source_specification_error_cdde	е					Clock source

Cat	Phase cda	<b>Type</b> clk	Name clck_assign_const_value_cdde	W/E e	V1995	V2001	Sys_ver	Csl	Desc Clock @ assigned to
dee	cda	clk	clk_assign_mux_clk_glitch_cdde	е					constant value. at line @ Clock @ assigned to
			- 0						multiplexed clock gate with glitch. at line @
dee	cda	clk	clk_assign_phase_shifted_clk_cdde	е					Clock @ assigned to phase shifted clock. at
dee	cda	clk	generated_clk_not_driven_by_FF_cdde	е					line @ Generated clock @ is not
dee	cda	clk	clk_source_driven_by_clk_cdde	е					driven by FF. at line @ The clock source clock is driven by another clock
									(reword this msg) at line
dee	cda	clk	unsupp_logic_op_during_tree_clk_anls_cdde	W					Found unsupported logic operation type @ during
									clock tree analysis. at line @
dee	cda	clk	unsupp_gated_clk_logic_during_clk_tree_anls_cdde	W					Found unsupported gated clock logic type @
									during clock tree analysis. at line @
dee	cda	clk	unsupp_logic_expr_during_clk_tree_anls_cdde	W					Found unsupported logic Expression type @
dee	cda	clk	unsupp_gated_clk_comp_during_clk_tree_anls_cdde	W					during clock tree analysis. at line @ Found unsupported
uee	cua	OIK	unsupp_gated_cik_comp_duming_dik_tree_ams_code	VV					gated clock component type @ during clock tree
dee	cda	clk	logic comp clk pin driven unsupp 1 gate cdde	w					analysis. 1 at line @  A logic component clock
			-5 -2 - 1 - 2 - 2 - 2 - 3 - 3 - 3 - 3 - 3 - 3 - 3						pin is driven by unsupported clock 1 logic
dee	cda	clk	mux_select_input_driven_gated_clk_cdde	W					gate. at line @ Multiplexer both the
									select @ and input @ are driven by gated
									clock This warning now reports the path from the
									path from the clock source to the input pin and the dock source to
									the mux select pin. at line  @
dee	cda	clk	one_input_pin_driven_gated_clk_other_not_cdde	W					Multiplexer has one data input @ driven by gated
									clock @ and the other data pin @ not driven by
									gated clock. Output @ may be undefined. at line
dee	cda	clk	unsupp_gated_clk_cdde	w					@ Unsupported gated clock
dee	cda	clk	unsupp_logic_inst_clk_tree_cdde	w					type @ at line @ Unsupported logic instance @ in clock tree
dee	cda	clk	unsupp_gated_clk_type_cdde	w					logic at line @  Use of unsupported
			2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2						gated clock type @ at line @
dee	cda	clk	enable_asserted_clk_sig_inactive_cdde	W					The enable signal of a gated clock logic may be
									asserted when the clock signal is inactive. at line
dee	cda	clk	unsupp_gated_clk_comp_cdde	w					@ Unsupported gated clock
dee	cda	clk	unsupp_logic_gate_comp_clk_pin_cdde	W					component type @. at line @  By unsupported clock
uee	cua	OIK	unsupp_logic_gate_comp_cik_piii_cude	VV					logic gate a logic component clock pin @
dee	cda	clk	complex_gated_clk_cdde	w					at line @ Found complex gated
dee	cda	clk	mux_select_or_input_pin_drvn_gate_clk_cdde	W					clock @ at line @ The mux select pin and
									one or more mux input pins are driven by gated
dee	cda	clk	one_data_pin_driven_gated_clk_other_not_cdde	W					clocks at line @ Mux has one data pin
									driven by gated clock @ and the other data pin @
dee	cda	clk	cannot_anls_gated_clk_cdde	W					not driven by gated clock @ at line @ Cannot analyze gated
dee	cda	clk	gated_clk_more_than_1pin_output_cdde	w					clock type @ at line @ Gated clock has more
200	344	J\	3	"					than 1 output pin at line
dee	cda	clk	no_clknet_in_always_blk_edge_stmt_cdde	w					No clockNet found in always block with edge
dee	cda	clk	no_clkport_in_always_blk_edge_stmt_cdde	w					statement at line @ No clockPort found in

									_
Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc always block with edge statement at line @
dee	cda	clk	no_clksig_in_always_blk_edge_stmt_cdde	W					No clockSignal found in always block with edge
doo	cda	clk	no alknot in always blk on latch adds	14/					statement at line @ No clockNet found in
dee	cua	CIK	no_clknet_in_always_blk_as_latch_cdde	W					always block which can
									be inferred as a latch at
dee	cda	clk	no_clkport_in_always_blk_as_latch_cdde	w					line @ No clockPort found in
									always block which can
									be inferred as a latch at line @
dee	cda	clk	no_clksig_in_always_blk_as_latch_cdde	W					No clockSignal found in
									always block which can be inferred as a latch at
									line @
dee	cda	clk	merged_clk_latch_point_cdde	W					Merged clock @ with latching point at line @
dee	cda	clk	merged_clk_doamins_cdde	W					Merged clock domains
dee	cda	clk	clk_domains_mergednet_unknown_cdde	w					clocks @ at line @ Clock domains
									mergedNets unknown
dee	cda	clk	clk_domains_mergedport_unknown_cdde	W					at line @ Clock domains
									mergedPorts unknown
dee	cda	clk	clk_domains_mergedsig_unknown_cdde	W					at line @ Clock domains
									mergedSignals
dee	cda	clk	merged_clk_phases_cdde	W					unknown at line @ Merged clock phases
			<b>5</b> – – – –						clock @ phase phase @
									clock @ phase @ at line @
dee	cda	clk	clk_tree_outputs_more_max_fanout_cdde	W					Clock tree logic has @ outputs which exceeds
									the maximimum
									threshold for gated clock
dee	cda	clk	scan_latch_no_domain_cdde	W					fan out at line @  Driver of scan latch clock
									'clock' has no domain. at
dee	cda	clk	clk_dupl_multi_dirs_cdde	W					line @ Clock @ duplicated in
									multiple clock directives at line @
dee	cda	clk	cannot_locate_clknet_dsgn_cdde	W					Cannot locate the
									clockNet @ in design at line @
dee	cda	clk	cannot_locate_clkport_dsgn_cdde	W					Cannot locate the
									clockPortt @ in design at line @
dee	cda	clk	cannot_locate_clksig_dsgn_cdde	W					Cannot locate the
									clockSignal @ in design at line @
dee	cda	cmpl	comp_loop_split_auto_cdde	W					Component with
									component loop has been automatically split
									at line @
dee	cda	comb	comb_level_exceeds_num_cdde	W					Combinational logic cone depth. Level exceeds
									maximum specified
dee	cda	CSS	css_coded_as_ternary_expr_cdde	W					depth @ at line @ Case statement could be
									coded as a ternaryExpression at line
									. @
dee	cda	drvc	tri_nontri_drives_net_cdde	W					tristate @ and non-tristate @ drivers
									onNet at line @
dee	cda	drvc	tri_nontri_drives_port_cdde	W					tristate @ and non-tristate @ drivers
									onPort at line @
dee	cda	drvc	tri_nontri_drives_sig_cdde	W					tristate @ and non-tristate @ drivers
									onSignal at line @
dee	cda	func	unm_type_func_task_param_cdde	е		1			Unmatched type in function/task @
									parameter @ at line @
dee	cda	func	unused_func_cdde	е					Unused function @ at line @
dee	cda	inhw	inhw_latch_not_connected_clk_cde	е					Scan latch not connected
dee	cda	inhw	inhw_latch_not_connected_data_in_cdde	е					to clock at line @ Scan latch not connected
									to data in at line @
dee	cda	inhw	inhw_latch_not_connected_output_cdde	е					Scan latch not connected to output at line @
dee	cda	init	init_time_domain_invalid_comp_cdde	W					Initialization time domain
									contains an Invalid component type @ at
al-	e -1	le	umana protrondon in 1 1 1						line @
dee	cda	inst	wrong_port_order_in_inst_cdde	е			1		Wrong port order in

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc instantiation @ at line @
dee	cda	inst	unparam_inst_to_param_cdde	е					Unparameterized instantiation to parameter
dee	cda	mdb	mdb contention cdde	w					@ at line @ Bus contention. at line @
dee	cda	mdb	mdb_connected_to_pull_up_down_cdde	W					Wired bus connected to pull up(s) and pull
dee	cda	mdb	mdb_net_driven_by_different_driver_cdde	w					down(s) at line @ Multi-driven Net driven
									by different driver types at line @
dee	cda	mdb	mdb_port_driven_by_different_driver_cdde	W					Multi-driven Port driven by different driver types
dee	cda	mdb	mdb sig driven by different driver cdde	w					at line @ Multi-driven Signal driven
doo	odd	mab	ab_sig_anvon_by_anionan_anvon_cado	"					by different driver types at line @
dee	cda	mdb	single_mod_net_with_mult_drvtri_cdde	w					Single module drives same multi driven Net
									with multiple tri-state drivers at line @
dee	cda	mdb	single_mod_port_with_mult_drvtri_cdde	w					Single module drives same multi driven Port
									with multiple tri-state
dee	cda	mdb	single_mod_sig_with_mult_drvtri_cdde	w					drivers at line @ Single module drives
									same multi driven Signal with multiple tri-state
dee	cda	mdb	single_ent_net_with_mult_drvtri_cdde	W					drivers at line @ Single entity drives same
			-						multi driven Net with multiple tri-state drivers
dee	cda	mdb	single_ent_port_with_mult_drvtri_cdde	w					at line @ Single entity drives same
			<b>g</b> <u>-</u>						multi driven Port with multiple tri-state drivers
dee	cda	mdb	single_ent_sig_with_mult_drvtri_cdde	w					at line @ Single entity drives same
uee	cua	mub	single_ent_sig_with_mult_arvith_cade	W					multi driven Signal with
									multiple tri-state drivers at line @
dee	cda	mdb	singlee_unit_with_mult_drvtri_cdde	W					Single unit drives same multi driven Net with
									multiple tri-state drivers at line @
dee	cda	mdb	single_unitt_with_mult_drvtri_cdde	W					Single unit drives same multi driven Port with
									multiple tri-state drivers at line @
dee	cda	mdb	single_unit_with_mult_drvtri_cdde	W					Single unit drives same multi driven Signal with
									multiple tri-state drivers at line @
dee	cda	mdb	expr_on_lhs_mdb_net_cdde	W					Expression type @ on LHS in multi-drivenNet at
doo	odo	an alla	expr on lhs mdb port cdde						line @  Expression type @ on
dee	cda	mdb	expr_on_ins_mab_port_cade	W					LHS in multi-drivenPort at line @
dee	cda	mdb	wired_net_only_connected_one_drvr_cdde	е					Wired net type only
									connected to one driver @ at line @
dee	cda	mdb	wired_port_only_connected_one_drvr_cdde	е					Wired port type only connected to one driver
dee	cda	mdb	wired_sig_only_connected_one_drvr_cdde	е					@ at line @ Wired signal type only
									connected to one driver @ at line @
dee	cda	mdb	wired_net_cdde	е					Wired net type @ found at line @
dee	cda	mdb	wired_port_cde	е					Wired port type @ found at line @
dee	cda	mdb	wired_sig_cde	е					Wired signal type @ found at line @
dee	cda	mifc	empty_list_port_module_port_cdde	е					Empty list port at top module port @ at line @
dee	cda	mifc	empty_list_port_entity_port_cdde	е					Empty list port at top entity port @ at line @
dee	cda	mifc	empty_list_port_unit_port_cdde	е					Empty list port at top unit port @ at line @
dee	cda	mifc	mod_csl_max_num_ports_cdde	w				х	Module @ exceeds the
									maximum number of ports. (trumber read /
									trumber write ports in use.). Specify the port
									number threshold with the cslc directive
									csl_max_num_ports. at line @
dee	cda	mifc	entity_csl_max_num_ports_cdde	W			<u></u>	Х	Entity @ exceeds the maximum number of

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
Cat	Filase	Туре	Name	VV/E	V1995	V2001	oys_ver	CSI	ports. (trumber read / trumber write ports in use.). Specify the port number threshold with the cslc directive csl_max_num_ports. at line @
dee	cda	mifc	unit_csl_max_num_ports_cdde	W				х	Unit @ exceeds the maximum number of ports. (trumber read / trumber write ports in use.). Specify the port number threshold with the cslc directive csl_max_num_ports. at
dee	cda	mod	wrong_order_in_port_decl_cdde	е					line @ Wrong order in port
dee	cda	net	net_not_decalred_and_used_in_stmt_cdde	w					declaration at line @ Inferred Net @ used in statement.Net not
dee	cda	net	port_not_decalred_and_used_in_stmt_cdde	w					Inferred Port @ used in statement.Port not declared at line @
dee	cda	net	sig_not_decalred_and_used_in_stmt_csde	w					Inferred Signal @ used in statement.Signal not declared at line @
dee	cda	net	sig_not_decalred_and_used_in_stmt_cdde	W					Inferred Signal @ used in statement.Signal not declared at line @
dee	cda	rst	FF_without_rst_cdde	е					FF without reset at line @
dee	cda	rst	FF_with_rst_cdde	е					FF with reset. Low power designs reduce the load on the reset line by eliminating reset on FFs at line @
dee	cda	sdir	unmatched_syns_transl_on_off_cdde	е					unmatched synopsys translate off on at line @
dee	cda	seq	unconventional_always_blk_cdde	W					Found unconventional always block at line @
dee	cda	seq	always_blk_cannot_infer_all_outputs_cdde	w					Always block cannot infer all outputs as latches not all outputs can be
dee	cda	seq	irregular_latch_detected_cdde	w	?				inferred at line @ Irregular latch detected. Latch may be transparent for longer than one cvcle. at line @
dee	cda	seq	detected_latching_point_cdde	w					Detected a latching point at line @
dee	cda	seq	latch_driven_both_phases_cdde	w					Latch driven by both phases at line @
dee	cda	seq	latch_driven_clk_logic_cdde	w					Latch driven by clock
dee	cda	sig	sig_not_exist_in_dsgn_cdde	W					logic at line @ Signal @ does not exist
dee	cda	simr	mixed_edge_type_cdde	е					in the design at line @ Mixed edge types at line
dee	cda	snsl	edge_clk_not_specifiect_cdde	W					@ Edge type of clock @ is
dee	cda	snsl	edge_incorrect_clk_cdde	W					not specified at line @ Edge type of clock @ is
dee	cda	snsl	expr_type_cdde	w					incorrect at line @ Expression type @ at line @
dee	cda	sply	nonlib_el_defi_as_sply_cdde	е					Non-library element define name used as supply at line @
dee	cda cda	task topo	unused_task_cdde topo_sort_graph_cdde	e w					Unused task @ at line @ The topological sort of
dee	cda	unsy	unsy_case_op_cdde	е					the graph. at line @ Un-synthesizable case equality operator = = at
dee	cda	unsy	unsy_deassn_stmt_cdde	е					line @ Un-synthesizable deassign statement at line @
dee	cda	unsy	unsy_defparam_cdde	е					Un-synthesizable
dee	cda	unsy	unsy_dely_ctrl_cdde	е					defparam at line @ Un-synthesizable delay
dee	cda	unsy	unsy_evctrl_cdde	е					control at line @ Un-synthesizable event control at line @
dee	cda	unsy	unsy_evdecl_cdde	е					Un-synthesizable event declaration at line @
dee	cda	unsy	unsy_forc_stmt_cdde	е					Un-synthesizable force statement at line @
dee	cda cda	unsy	unsy_fok_stmt_cdde  unsy_init_cdde	e e					Un-synthesizable fork statement at line @ Un-synthesizable initial
			,						at line @

Cat	Phase	Туре	Name	W/E V1995	V2001 S	ys_ver Csl	Desc
dee	cda	unsy	unsy_prim_def_cdde	е	1200.		Un-synthesizable orimitive definition at line
dee	cda	unsy	unsy_rel_stmt_cdde	е		U	@ In-synthesizable release statement at line @
dee	cda	unsy	unsy_rep_stmt_cdde	е		l	Jn-synthesizable repeat statement at line @
dee	cda	unsy	unsy_time_decl_cdde	е		ti	Un-synthesizable meDeclaration at line @
dee	cda	unsy	unsy_trns_cdde	е			Un-synthesizable transistor at line @
dee	cda	unsy	unsy_wait_stmt_cdde	е			Un-synthesizable wait statement at line @
dee	cdc	blk	blk_cont_assign_not_allowed_cdcde	е			Procedural continuous assignment is not allowed at line @
dee	cdc	cyb	cyb_stmt_repeat_evc_in_blocking_assign_cdcde	е			Statement intra-assignment repeat
						(	event control in blocking assignment detected at line @
dee	cdc	cyb	cyb_stmt_evc_in_blocking_assign_cdcde	е			Statement intra-assignment event control in blocking
							assignment detected at line @
dee	cdc	cyb	cyb_stmt_repeat_evc_in_non_blk_assign_cdcde	е			Statement intra-assignment repeat event control in ion-blocking assignment
dee	cdc	cyb	cyb_stmt_evc_in_non_blk_assign_cdcde	e			detected at line @ Statement
		-					intra-assignment event control in non-blocking assignment detected at line @
dee	cdc	cyb	cyb_deassign_stmt_not_stimul_cdcde	е		c	De-assign statement can't be simulated at line
dee	cdc	cyb	cyb_forever_loop_not_stimul_cdcde	е			Forever-loop is can't be simulated at line @
dee	cdc	dely	inappropriate_form_intra_assign_dely_cdcde	е			Intra-assignmentDelay control in blocking assignment not of form
dee	cdc	forc	cannot_forc_prts_net_cdcde	е			#O or #1 at line @ Cannot force a partially elected Net name at line @
dee	cdc	forc	cannot_forc_prts_port_cdcde	е			Cannot force a partially selected Port name at line @
dee	cdc	forc	cannot_forc_prts_signal_cdcde	е		5	Cannot force a partially selected Signal name at line @
dee	cdc	inst	inst_mult_connections_port_cdcde	е			Port 'port' has multiple connections specified at line @
dee	cdc	inst	inst_unknown_port_name_cdcde	е			Inknown port name @ in amed port connection at line @
dee	cdc	inst	too_many_port_connections_inst_cdcde	е		c	Too many port connections specified for instance @ at line @
dee	cdc	inst	inst_port_mod_width_cdcde	е			Input port @ in module @ width mismatch, actual-width (port-width)
dee	cdc	inst	inst_port_entity_width_cdcde	е			at line @ Input port @ in entity @ width mismatch, actual-width (port-width)
dee	cdc	inst	inst_port_unit_width_cdcde	e			at line @ Input port @ in unit @
uee	ouc	ii i o l	moc_port_unit_widit1_cucue				width mismatch, actual-width (port-width)
dee	cdc	inst	inst_output_mod_port_width_cdcde	е			at line @  Output port @ in module width mismatch,
							actual-width (port-width) at line @
dee	cdc	inst	inst_output_entity_port_width_cdcde	е			Output port @ in entity width mismatch, actual-width (port-width)
dee	cdc	inst	inst_output_unit_port_width_cdcde	e			at line @  Output port @ in unit
406	500		oc_oapat_unit_port_mutit_outde				width mismatch, actual-width (port-width) at line @
dee	cdc	inst	inst_mod_not_contain_port_cdcde	е			Module @ does not contain Port @ at line @
dee	cdc	inst	inst_entity_not_contain_port_cdcde	е			Entity @ does not

Cat		Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
dee	cdc	inst	inst_unit_not_contain_port_cdcde	е				L	Unit @ does not contain Port @ at line @
dee	cdc	inst	inout_port_mod_width_cdcde	е					Inout port @ in module width mismatch, actual width (port-width) at line
dee	cdc	inst	inout_port_entity_width_cdcde	е					@ Inout port @ in entity
									width mismatch, actual width (port-width) at line
dee	cdc	inst	inout_port_unit_width_cdcde	е					Inout port @ in unit width mismatch, actual width
-1			and annual by found adads						(port-width) at line @
dee	cdc	mdn	mdn_cannot_be_forced_cdcde	е					Multiple drive Net 'name' cannot be forced. at line @
dee	cdc	mdn	mdn_port_cannot_be_forced_cdcde	е					Multiple drive Port 'name' cannot be forced. at line @
dee	cdc	mdn	mdn_signal_cannot_be_forced_cdcde	е					Multiple drive Signal 'name' cannot be forced. at line @
dee	cdc	mifc	mifc_complex_port_decl_not_supported_cdcde	е					Complex port Declaration port of module @ is not
doo	ada	ifa	mile antity compley part deal not appointed adala						supported at line @
dee	cdc	mifc	mifc_entity_complex_port_decl_not_supported_cdcde	е					Complex port Declaration port of entity @ is not supported at line @
dee	cdc	mifc	mifc_unit_complex_port_decl_not_supported_cdcde	е					Complex port Declaration port of unit @ is not supported at line @
dee	cdc	mifc	mifc_unknown_port_direction_cdcde	е					Unknown port direction @ (port) at line @
dee	cdc	mifc	mifc_input_port_is_mem_type_cdcde	е					Input port @ is memory
dee	cdc	num	num_division_by_zero_cdcde	е					type at line @  Division by zero at line @
dee	cdc	rel	cannot_rel_prts_net_cdcde	е					Cannot release a partially selected Net name at line @
dee	cdc	rel	cannot_rel_prts_port_cdcde	е					Cannot release a partially selected Port
dee	cdc	rel	cannot_rel_prts_signal_cdcde	е					name at line @ Cannot release a partially selected Signal
dee	cdc	trns	trns_inst_not_allowed_cdcde	е					name at line @ Transistor-level instantiations @ not
dee	csa	ccd	dupl_filter_dir_csde	w				х	allowed at line @ Duplicated filter directive @ at line @
dee	csa	ccd	unused_filter_dir_csde	W				Х	Unused filter directive @
dee	csa	ccd	ill_filter_dir_csde	W				Х	at line @ Illegal filter directive @ at line @
dee	csa	clk	latch_not_connected_clk_csde	е					Latch not connected to a clock pin. at line @
dee	csa	clk	FF_not_connected_clk_csde	е					FF not connected to a clock pin. at line @
dee	csa	clk	clk_source_not_vec_bit_csde	е					Clock source @ cannot be a vector bit at line @
dee	csa	clk	clk_driven_by_net_csde	е					The clock source @ is
									not driven by a clock and is driven by net @.
									Inferring a net type instead of clock per the
dee	csa	clk	clk_driven_by_port_csde	е					clock directive. at line @ The clock source @ is
	000	0	S.Ia.i.io.i5y_poi55345						not driven by a clock and is driven by port @.
									Inferring a port type
									instead of clock per the clock directive. at line @
dee	csa	clk	clk_driven_by_signal_csde	е					The clock source @ is not driven by a clock and
									is driven by signal @. Inferring a signal type
									instead of clock per the
dee	csa	clk	clk_should_drive_clk_csde	е					clock directive. at line @ A clock should drive
dee	csa	clk	clk_source_def_contains_clk_csde	е					clock @. at line @ Clock source definition
									contains a clock at line @
dee	csa	clk	cannot_open_clk_filename_csde	е					Cannot open the clock file filename at line @
dee	csa	clk	clk_source_specification_error_csde	е					Clock source specification error at line @
dee	csa	clk	clck_assign_const_value_csde	е					Clock @ assigned to constant value. at line @
dee	csa	clk	clk_assign_mux_clk_glitch_csde	е					Clock @ assigned to

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									multiplexed clock gate
dee	csa	clk	clk_assign_phase_shifted_clk_csde	е			<del>                                     </del>		with glitch. at line @ Clock @ assigned to
	-	•				l n			phase shifted clock. at
dee	csa	clk	generated_clk_not_driven_by_FF_csde	е					line @ Generated clock @ is not
uee	USa	CIK	generated_cik_not_dilven_by_i i _csde	6		l I			driven by FF. at line @
dee	csa	clk	clk_source_driven_by_clk_csde	е					The clock source clock is
						l I			driven by another clock (reword this msg) at line
									@
dee	csa	clk	unsupp_logic_op_during_tree_clk_anls_csde	W		l n			Found unsupported logic operation type @ during
						l I			clock tree analysis. at
						,			line @
dee	csa	clk	unsupp_gated_clk_logic_during_clk_tree_anls_csde	W		l n			Found unsupported gated clock logic type @
						l I			during clock tree
dee	csa	clk	unsupp_logic_expr_during_clk_tree_anls_csde	w					analysis. at line @ Found unsupported logic
acc	osa	OIIX	unsupp_logic_cxpi_ddinig_cik_ucc_dinis_csdc	**		l I			Expression type @
						l I			during clock tree
dee	csa	clk	unsupp_gated_clk_comp_during_clk_tree_anls_csde	w					analysis. at line @ Found unsupported
						l n			gated clock component
						l I			type @ during clock tree analysis. 1 at line @
dee	csa	clk	logic_comp_clk_pin_driven_unsupp_1_gate_csde	w					A logic component clock
						l n			pin is driven by
						l n			unsupported clock 1 logic gate. at line @
dee	csa	clk	cslc_primitive_during_clk_tree_anls_csde	w				Х	Found complex gated
						l I			clock CSLC primitive 'primitive' during clock
						l n			tree analysis. at line @
dee	csa	clk	cslc_primitive_during_clk_tree_anls_cdde	W				Х	Found complex gated
						l n			clock CSLC primitive 'primitive' during clock
							<u> </u>		tree analysis. at line @
dee	csa	clk	mux_select_input_driven_gated_clk_csde	W		l I			Multiplexer both the select @ and input @
						l I			are driven by gated
						l n			clock This warning now
						l I			reports the path from the path from the clock
						l I			source to the input pin
						l n			and the dock source to the mux select pin. at line
							<u> </u>		@ .
dee	csa	clk	one_input_pin_driven_gated_clk_other_not_csde	w		l n			Multiplexer has one data input @ driven by gated
						l I			clock @ and the other
						l I			data pin @ not driven by
						l n			gated clock. Output @ may be undefined. at line
							<u> </u>		@
dee	csa	clk	unsupp_gated_clk_csde	w		l n			Unsupported gated clock type @ at line @
dee	csa	clk	unsupp_logic_inst_clk_tree_csde	w					Unsupported logic
						l I			instance @ in clock tree logic at line @
dee	csa	clk	unsupp gated clk type csde	w					Use of unsupported
			11-5 71 -			l n			gated clock type @ at
dee	csa	clk	enable_asserted_clk_sig_inactive_csde	w					line @ The enable signal of a
doo	oou	One	onabio_accontoa_ont_org_macrivo_code	"		l n			gated clock logic may be
						l I			asserted when the clock signal is inactive. at line
						l n			@
dee	csa	clk	unsupp_gated_clk_comp_csde	W					Unsupported gated clock
						l n			component type @. at line @
dee	csa	clk	unsupp_logic_gate_comp_clk_pin_csde	w					By unsupported clock
						l I			logic gate a logic component clock pin @
						l I			at line @
dee	csa	clk	complex_gated_clk_csde	w		-			Found complex gated
dee	csa	clk	mux_select_or_input_pin_drvn_gate_clk_csde	w			<del></del>		clock @ at line @ The mux select pin and
230	554	- Ont	55.655psipiii_di 111_gdio_oii6506	"		  -			one or more mux input
						  -			pins are driven by gated
dee	csa	clk	one_data_pin_driven_gated_clk_other_not_csde	w					clocks at line @ Mux has one data pin
			,			  -			driven by gated clock @
						ļ			and the other data pin @ not driven by gated clock
						ļ			@ at line @
dee	csa	clk	cannot_anls_gated_clk_csde	w					Cannot analyze gated clock type @ at line @
uoo							1	1	
dee	csa	clk	gated_clk_more_than_1pin_output_csde	w					Gated clock has more

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
dee	csa	clk	no_clknet_in_always_blk_edge_stmt_csde	W					@ No clockNet found in always block with edge statement at line @
dee	csa	clk	no_clkport_in_always_blk_edge_stmt_csde	W					No clockPort found in always block with edge statement at line @
dee	csa	clk	no_clksig_in_always_blk_edge_stmt_csde	W					No clockSignal found in always block with edge statement at line @
dee	csa	clk	no_clknet_in_always_blk_as_latch_csde	W					No clockNet found in always block which can be inferred as a latch at line @
dee	csa	clk	no_clkport_in_always_blk_as_latch_csde	W					No clockPort found in always block which can be inferred as a latch at line @
dee	csa	clk	no_clksig_in_always_blk_as_latch_csde	w					No clockSignal found in always block which can be inferred as a latch at
dee	csa	clk	merged_clk_latch_point_csde	w					line @ Merged clock @ with
dee	csa	clk	merged_clk_doamins_csde	W					latching point at line @ Merged clock domains
dee	csa	clk	clk_domains_mergednet_unknown_csde	w					clocks @ at line @ Clock domains mergedNets unknown
dee	csa	clk	clk_domains_mergedport_unknown_csde	w					at line @ Clock domains mergedPorts unknown at line @
dee	csa	clk	clk_domains_mergedsig_unknown_csde	w					Clock domains mergedSignals unknown at line @
dee	csa	clk	merged_clk_phases_csde	W					Merged clock phases clock @ phase phase @ clock @ phase @ at line @
dee	csa	clk	clk_tree_outputs_more_max_fanout_csde	w					Clock tree logic has @ outputs which exceeds the maximimum threshold for gated clock fan out at line @
dee	csa	clk	scan_latch_no_domain_csde	W					Driver of scan latch clock 'clock' has no domain. at line @
dee	csa	clk	clk_dupl_multi_dirs_csde	w					Clock @ duplicated in multiple clock directives at line @
dee	csa	clk	cannot_locate_clknet_dsgn_csde	W					Cannot locate the clockNet @ in design at line @
dee	csa	clk	cannot_locate_clkport_dsgn_csde	W					Cannot locate the clockPortt @ in design at line @
dee	csa	clk	cannot_locate_clksig_dsgn_csde	W					Cannot locate the clockSignal @ in design at line @
dee	csa	cmpl	comp_loop_split_auto_csde	W					Component with component loop has been automatically split at line @
dee	csa	comb	comb_level_exceeds_num_csde	W					Combinational logic cone depth. Level exceeds maximum specified depth @ at line @
dee	csa	CSS	css_coded_as_ternary_expr_csde	W					Case statement could be coded as a ternaryExpression at line
dee	csa	drvc	tri_nontri_drives_net_csde	W					tristate @ and non-tristate @ drivers onNet at line @
dee	csa	drvc	tri_nontri_drives_port_csde	w					tristate @ and non-tristate @ drivers onPort at line @
dee	csa	drvc	tri_nontri_drives_sig_csde	w					tristate @ and non-tristate @ drivers onSignal at line @
dee	csa	func	unm_type_func_task_param_csde	е					Unmatched type in function/task @ parameter @ at line @
dee	csa	func	unused_func_csde	е					Unused function @ at line @
dee	csa	inhw	inhw_latch_not_connected_clk_csde inhw latch not connected data in csde	e e					Scan latch not connected to clock at line @ Scan latch not connected
dee	csa	inhw	inhw_latch_not_connected_output_csde	е					to data in at line @ Scan latch not connected to output at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
dee	csa	init	init_time_domain_invalid_comp_csde	W			-,		Initialization time domain contains an Invalid component type @ at
dee	csa	inst	wrong_port_order_in_inst_csde	е					line @ Wrong port order in
			<b>5</b> – – – –						instantiation @ at line @
dee	csa	inst	unparam_inst_to_param_csde	е					Unparameterized instantiation to parameter
									@ at line @
dee dee	csa	mdb mdb	mdb_contention_csde mdb_connected_to_pull_up_down_csde	W					Bus contention. at line @ Wired bus connected to
ucc	osa								pull up(s) and pull down(s) at line @
dee	csa	mdb	mdb_net_driven_by_different_driver_csde	W					Multi-driven Net driven by different driver types at line @
dee	csa	mdb	mdb_port_driven_by_different_driver_csde	W					Multi-driven Port driven by different driver types
dee	csa	mdb	mdb_sig_driven_by_different_driver_csde	W					at line @ Multi-driven Signal driver by different driver types at line @
dee	csa	mdb	single_mod_net_with_mult_drvtri_csde	W					Single module drives same multi driven Net with multiple tri-state
dee	csa	mdb	single_mod_port_with_mult_drvtri_csde	w					drivers at line @  Single module drives same multi driven Port with multiple tri-state drivers at line @
dee	csa	mdb	single_mod_sig_with_mult_drvtri_csde	w					Single module drives same multi driven Signal with multiple tri-state
dee	csa	mdb	single_ent_net_with_mult_drvtri_csde	w					drivers at line @ Single entity drives same multi driven Net with multiple tri-state drivers
dee	csa	mdb	single_ent_port_with_mult_drvtri_csde	W					at line @ Single entity drives same multi driven Port with multiple tri-state drivers
dee	csa	mdb	single_ent_sig_with_mult_drvtri_csde	W					at line @ Single entity drives same multi driven Signal with multiple tri-state drivers
dee	csa	mdb	singlee_unit_with_mult_drvtri_csde	W					at line @ Single unit drives same multi driven Net with multiple tri-state drivers at line @
dee	csa	mdb	single_unitt_with_mult_drvtri_csde	W					Single unit drives same multi driven Port with multiple tri-state drivers
dee	csa	mdb	single_unit_with_mult_drvtri_csde	w					at line @ Single unit drives same multi driven Signal with multiple tri-state drivers at line @
dee	csa	mdb	expr_on_lhs_mdb_port_csde	W					Expression type @ on LHS in multi-drivenPort at line @
dee	csa	mdb	expr_on_lhs_mdb_sig_csde	w					Expression type @ on LHS in multi-drivenSigna at line @
dee	csa	mdb	wired_net_only_connected_one_drvr_csde	е					Wired net type only connected to one driver @ at line @
dee	csa	mdb	wired_port_only_connected_one_drvr_csde	е					Wired port type only connected to one driver @ at line @
dee	csa	mdb	wired_sig_only_connected_one_drvr_csde	е					Wired signal type only connected to one driver @ at line @
dee	csa	mdb	wired_net_csde	е					Wired net type @ found at line @
dee	csa	mdb	wired_port_cde	е					Wired port type @ found at line @
dee	csa	mdb	wired_sig_cde	е					Wired signal type @
dee	csa	mifc	empty_list_port_module_port_csde	е					found at line @ Empty list port at top
			.,						module port @ at line @
dee	csa	mifc	empty_list_port_entity_port_csde	е					Empty list port at top entity port @ at line @
dee	csa	mifc	empty_list_port_unit_port_csde	е					Empty list port at top unit
dee	csa	mifc	mod_csl_max_num_ports_csde	w				x	port @ at line @  Module @ exceeds the maximum number of ports. (trumber read / trumber write ports in use.). Specify the port

Company	Cat	Phase	Туре	Name	W/F	V1995	V2001	Sys_ver	Csl	Desc
de csa mot mote de mitty_csl_max_num_ports_csde w	Jui	T Huoo	. , , ,	Hamo	11,2	71000	72001	Cyc_rc.	00.	the cslc directive
Section										
Description	dee	csa	mifc	entity_csl_max_num_ports_csde	W				Х	Entity @ exceeds the
dee										
										number threshold with
See										
maximum number of protects or instruments with protect (number read) trumber with protest or in number threshold in the class of colors or instruments or with protect or instruments	doo		mile.	unit cal may num narta and					.,	line @
dee csa mod wrong_order_in_port_deel_csde e	uee	USa	IIIIC	unit_csi_max_num_ports_csue	vv				Χ	maximum number of
dee csa met met_not_decaired_and_used_in_stmt_csde w interest control to the cities of incline cont										
dee Csa met net net net net net net net net net n										use.). Specify the port
Inc.										the cslc directive
Dec   Cas										
dee ca pp   net_not_decaired_and_used_in_stmt_cade   w   laferred Net @ used_in_decared_ain_used_in_stmt_cade   w   laferred Net @ used_in_decared_ain_used_in_stmt_cade   w   laferred Net @ used_in_def_and_used_in_stmt_cade   w   laferred Net @ used_in_def_and_param_name_cade   e   laferred Net @	dee	csa	mod	wrong_order_in_port_decl_csde	е					Wrong order in port
dee esa net port_not_decalred_and_used_in_stmt_csde w lateracter port @ used in statement.Port of @ used in statement.Port of declared_at line @ lateracter port of used in statement.Port of declared_at line @ lateracter port of used in define and parame.Pode esa pp used_in_def_and_param_name_cdde e lateracter port of used in define and parameter name at line @ lateracter parameter name at line @ lateracter parameter parame	dee	csa	net	net_not_decalred_and_used_in_stmt_csde	w					Inferred Net @ used in
Inferred Port @ used in stemment.Port not declared and _used in_stimt_code   w   Inferred Port @ used in statement.Port not declared at line @										
dee csa pp used_in_del_and_param_name_csde e	dee	csa	net	port_not_decalred_and_used_in_stmt_csde	w					
dee csa sqr unconventional_always_bik_cannot_infer_all_outputs_csde w from the control all outputs can be inferred at line @ and parameter name at line @ and parameter at line @ and parameter name at line @ and parameter at line @ and parameter at line @ and parameter attransparameter for internstitute and parameter attransparameter and parameter attransparameter and parameter attransparame										declared at line @
dee   csa	dee	csa	pp	used_in_def_and_param_name_csde	е					
dee csa sdir unmatched_syns_transl_on_off_csde e	dee	csa	nn	used in def and naram name cdde	Α					
dee csa rst FF_without_rst_csde e e FF without_rsst_csde e e FF without_rsst_csde e e FF without_rsst_csde e e FF with reset Low power est line by company the company of t	ucc	034	PP	used_in_der_and_param_name_edde						and parameter name at
dee csa seq irregular_latch_detected_csde w ?  dee csa seq irregular_latch_detected_csde w ?  dee csa seq irregular_latch_detected_csde w ?  dee csa seq detected_latching_point_csde w ?  dee csa seq irregular_latch_detected_csde w ?  dee csa seq irregular_latch_detected_csde w ?  dee csa seq detected_latching_point_csde w ?  dee csa seq irregular_latch_detected_csde w ?  dee csa seq detected_latching_point_csde w ?  dee csa seq detected_latching_point_csde w Detected a latching point at line @ Detected a latching point at line @ Detected a latching point at line @ Detected a latch property control to latch detected. Latch may be transparent to longer than one cvole. At line @ Detected a latch property control to latch detected. Latch detected w Detected a latch detected. Latch driven_both_phases_csde w Detected a latch driven by both phases at line @ Detected a latch driven by both phases at line @ Detected a latch driven by clock logic at line @ Detecte	dee	csa	rst	FF_without_rst_csde	е					FF without reset at line
dee csa seq detected_latching_point_csde w latch_driven_obth_phases_csde w latch_driven_obth_obth_phases_csde w latch_driven_obth_obth_phases_csde w latch_driven_obth_obth_phases_csde w latch_driven_obth_obth_obth_obth_obth_obth_obth_obth	dee	csa	rst	FF with rst csde	е					
dee csa sdir unmatched_syns_transl_on_off_csde e unmatched_syns_transl_on_off_csde e unmatched_syns_translate_off on at line @ translate off on at line @ unmatched_syns_blk_csde w										designs reduce the load
dee csa sdir unmatched_syns_transl_on_off_csde e unmatched_syns_translate of_on_at line @ csa seq unconventional_always_blk_csde w										eliminating reset on FFs
Gee   Csa   seq	dee	csa	sdir	unmatched_syns_transl_on_off_csde	е					
dee csa seq always_blk_cannot_infer_all_outputs_csde	dee	csa	sea	unconventional always blk csde	w					
dee csa seq detected_latching_point_csde w ? latch_driven_both_phases_csde w Detected a latching point dec csa seq latch_driven_both_phases_csde w Latch driven by both phases at line @ Detected a latching point at line @ Latch driven by both phases at line @ Latch driven by clock logic at line @ Latch driven by clock logic at line @ Signal @ does not exist in the design at line @ Signal @ does not exist in the design at line @ Wixed edge_type_csde e Mixed edge_type_csde e Mixed edge_type_csde e Mixed edge_type_csde w ledge_lock_csa sinsl edge_clk_not_specifiect_csde w ledge_type_csde w ledge_type_csde w ledge_type_csde ledge_type_csde w ledge_type_csde w ledge_toto specified_tine @ Ledge_type_of clock_cs_since tine @ Ledge_type_of_type_of_type_of_cs_de e Un-synthesizable_cde_type_of_type_of_type_of_type_of_type			·	•						always block at line @
dee csa seq detected_latching_point_csde w ? Irregular latch_detected_csde w ? Irregular latch detected. Latch may be transparent for longer than one cvcle. at line @ transparent for longer than one cvcle. at line @ Detected a latching point at line @ Latch driven_both_phases_csde w Detected a latching point at line @ Latch driven by both phases at line @ Latch driven by both phases at line @ Latch driven by both phases at line @ Latch driven by clock logic at line @ Signal @ does not exist in the design at line @ Signal @ does not exist in the design at line @ Mixed edge_type at line @ Mixed edge_types at line @ Mixed edge_types at line @ Mixed edge_types at line @ Bedge_toth_csde w Bedge_incorrect_clk_csde w Bedge_incorrect_clk_csde w Bedge_incorrect_clk_csde w Bedge_incorrect_clk_csde w Bedge_toth_csde at line @ Bedge_toth_csde at line @ Bedge_toth_csde at line @ Bedge_toth_csde w Bedge_toth_csde at line @ Bedge_toth_csde_toth_csde at line @ Bedge_toth_csde_tot	uee	USa	seq	aiways_bik_caiiilot_iiilet_aii_outputs_csue	vv					all outputs as latches not
dee csa seq detected_latching_point_csde										
dee csa seq detected_latching_point_csde w Detected a latching point at line @ Detected a latching point at line @ Latch driven by both phases at line @ Latch driven by clock logic at line @ Signal @ does not exist in the design at line @ Signal @ does not exist in the design at line @ Mixed edge_type_csde e Mixed edge_type_csde e Mixed edge_type_st line @ Mixed edge_type_st line @ Mixed edge_type_st line @ Mixed edge_type_st line @ Edge_type_of-lock @ is not specified at line @ Is not specifi	dee	csa	seq	irregular_latch_detected_csde	W	?				
dee         csa         seq         detected_latching_point_csde         w         Detected a latching point at line @ tat line @										transparent for longer
dee   csa   seq   latch_driven_both_phases_csde   w   phases at line @   Latch driven by both   phases at line @   Latch driven by clock   logic at line @   Signal @ does not exist   in the design at line @   Mixed edge_type_csde   e   Mixed edge_type_st line @   Edge_type_of_clock @ is   not specified at line @   Edg_type_of_clock @ is   not specified at line @   Unusynthesizable design_to_the manused as   supply_at line @   Unusynthesizable design_to_the manused as   supply_at line @   Unusynthesizable design_to_the manused as   supply_at line @   Unusynthesizable design_to_the manused as   unusy_defparam_csde   e   Unusynthesizable defiguram_tine @	dee	csa	seq	detected_latching_point_csde	w					Detected a latching point
dee   csa   seq   latch_driven_cik_logic_csde   w     Latch driven by clock logic at line @   Signal @ does not exist in the design at line @   Mixed edge types at line @   Mixed edge types at line @   Mixed edge type of clock @ is not specified at line @   edge_cik_not_specifiect_csde   w   Edge type of clock @ is not specified at line @   edge_cik_not_specifiect_csde   w   Edge type of clock @ is not specified at line @   expr_type_csde   w   Edge type of clock @ is not specified at line @   Expression type @ at line @   Unused task @ at line @   Unused task @ at line @   Unusynthesizable case equality operator = at line @   Unusynthesizable deasign statement at line @   Unusynthesizable deasign statement at line @   Unusynthesizable deasign statement at line @   Unusynthesizable deasynthesizable deavnthesizable deavnthesizable deavnthesizable deavnthesizable deavnthesizable deavnthesizable deavnthesizable deavnthesizable deventhesizable deventhesizable declaration at line @   Unusynthesizable deventhesizable dev	dee	csa	seq	latch_driven_both_phases_csde	w					
dee   csa   sig   sig_not_exist_in_dsgn_csde   w   Signal @ does not exist in the design at line @	dee	csa	Seu .	latch driven clk logic csde	\ <b>\</b> \					
dee   csa   simr   mixed_edge_type_csde   e     Mixed edge type at line @     Edge type of clock @ is   not specified at line @   Edge type of clock @ is   not specified at line @   Edge type of clock @ is   not specified at line @   Edge type of clock @ is   not specified at line @   Edge type of clock @ is   not specified at line @   Edge type of clock @ is   not specified at line @   Edge type of clock @ is   not specified at line @   Edge type of clock @ is   not specified at line @   Edge type of clock @ is   not specified at line @   Edge type of clock @ is   not specified at line @   Edge type of clock @ is   not specified at line @   Edge type of clock @ is   not specified at line @   Edge type of clock @ is   not specified at line @   Edge type of clock @ is   not specified at line @   Edge type of clock @ is   not specified at line @   Edge type of clock @ is   not specified at line @   Edge type of clock @ is   not specified at line @   Non-library element   Edge type of clock @ is   not specified at line @   Inserting element   Edge type of clock @ is   not specified at line @   Inserting element   Edge type of clock @ is   not specified at line @   Inserting element   Edge type of clock @ is   not specified at line @   Inserting element   Edge type of clock @ is   not specified at line @   Inserting element   Inserting element   Edge type of clock @ is   not specified at line @   Inserting element   Insertin			·							logic at line @
dee csa snsl edge_clk_not_specifiect_csde w Edge type of clock @ is not specified at line @ Edge type of clock @ is not specified at line @ Edge type of clock @ is incorrect at line @ Edge type of clock @ is incorrect at line @ Edge type of clock @ is incorrect at line @ Edge type of clock @ is incorrect at line @ Edge type of clock @ is incorrect at line @ Expression type @ at line @ Incorrect at line	dee	csa	sig	<b>3</b> = = = <b>3</b> =	W					in the design at line @
dee csa snsl edge_incorrect_clk_csde w Edge_type of clock @ is incorrect at line @ Edge type of clock @ is incorrect at line @ Expression type @ at line @ Expression type @ at line @ Expression type @ at line @ Mon-library element define name used as supply at line @ Mon-library element define name used as supply at line @ Unused task @ at line @ Unused task @ at line @ The topological sort of the graph. at line @ Un-synthesizable case equality operator = at line @ Un-synthesizable case equality operator = at line @ Un-synthesizable deassign statement at line @ Un-synthesizable defapram at line @ Un-synthesizable deforator at line @ Un-synthesizable devent control at line @ Un-synthesizable event declaration at	dee	csa	simr	mixed_edge_type_csde	е					Mixed edge types at line @
dee       csa       snsl       edge_incorrect_clk_csde       w       Edge type of clock @ is incorrect at line @         dee       csa       snsl       expr_type_csde       w       Expression type @ at line @         dee       csa       sply       nonlib_el_defi_as_sply_csde       e       Non-library element define name used as supply at line @         dee       csa       task       unused_task_csde       e       Unused task @ at line @         dee       csa       topo       topo_sort_graph_csde       w       The topological sort of the graph. at line @         dee       csa       unsy       unsy_case_op_csde       e       Un-synthesizable case equality operator = at line @         dee       csa       unsy       unsy_deassn_stmt_csde       e       Un-synthesizable deassign statement at line @         dee       csa       unsy       unsy_defparam_csde       e       Un-synthesizable delay control at line @         dee       csa       unsy       unsy_dely_ctrl_csde       e       Un-synthesizable event control at line @         dee       csa       unsy       unsy_evctrl_csde       e       Un-synthesizable event control at line @         dee       csa       unsy       unsy_evdecl_csde       e       Un-synthesizable event declaration at line @ <td>dee</td> <td>csa</td> <td>snsl</td> <td>edge_clk_not_specifiect_csde</td> <td>w</td> <td></td> <td></td> <td></td> <td></td> <td></td>	dee	csa	snsl	edge_clk_not_specifiect_csde	w					
dee       csa       snsl       expr_type_csde       w       Expression type @ at line @         dee       csa       sply       nonlib_el_defi_as_sply_csde       e       Non-library element define name used as supply at line @         dee       csa       task       unused_task_csde       e       Unused task @ at line @         dee       csa       topo       topo_sort_graph_csde       w       The topological sort of the graph. at line @         dee       csa       unsy       unsy_case_op_csde       e       Un-synthesizable case equality operator = at line @         dee       csa       unsy       unsy_deassn_stmt_csde       e       Un-synthesizable deassign statement at line @         dee       csa       unsy       unsy_defparam_csde       e       Un-synthesizable delay control at line @         dee       csa       unsy       unsy_evterl_csde       e       Un-synthesizable delay control at line @         dee       csa       unsy       unsy_evterl_csde       e       Un-synthesizable event control at line @         dee       csa       unsy       unsy_evterl_csde       e       Un-synthesizable event declaration at line @	dee	csa	snsl	edge_incorrect_clk_csde	w					Edge type of clock @ is
dee       csa       sply       nonlib_el_defi_as_sply_csde       e       Non-library element define name used as supply at line @ supply at line @         dee       csa       task       unused_task_csde       e       Unused task @ at line @         dee       csa       topo       topo_sort_graph_csde       w       The topological sort of the graph. at line @         dee       csa       unsy       unsy_case_op_csde       e       Un-synthesizable case equality operator = = at line @         dee       csa       unsy       unsy_deassn_stmt_csde       e       Un-synthesizable deassign statement at line @         dee       csa       unsy       unsy_defparam_csde       e       Un-synthesizable delay control at line @         dee       csa       unsy       unsy_evctrl_csde       e       Un-synthesizable event control at line @         dee       csa       unsy       unsy_evdecl_csde       e       Un-synthesizable event declaration at line @	dee	csa	snsl	expr_type_csde	w					
dee csa task unused_task_csde e Unused task @ at line @ the graph. at line @ dee csa unsy unsy_defsparam_csde e unsy unsy_evctrl_csde e unsy unsy_evctrl_				,						line @
dee       csa       task       unused_task_csde       e       Unused task @ at line @         dee       csa       topo       topo_sort_graph_csde       w       The topological sort of the graph. at line @         dee       csa       unsy       unsy_case_op_csde       e       Un-synthesizable case equality operator = = at line @         dee       csa       unsy       unsy_deassn_stmt_csde       e       Un-synthesizable deassign statement at line @         dee       csa       unsy       unsy_defparam_csde       e       Un-synthesizable defparam at line @         dee       csa       unsy       unsy_dely_ctrl_csde       e       Un-synthesizable delay control at line @         dee       csa       unsy       unsy_evctrl_csde       e       Un-synthesizable event control at line @         dee       csa       unsy       unsy_evdecl_csde       e       Un-synthesizable event declaration at line @	ucc	034	Зріу	normb_cr_den_ds_spry_csdc						define name used as
the graph. at line @  dee csa unsy unsy_case_op_csde e  dee csa unsy unsy_deassn_stmt_csde e  dee csa unsy unsy_defparam_csde e  dee csa unsy unsy_dely_ctrl_csde e  dee csa unsy unsy_dely_ctrl_csde e  dee csa unsy unsy_evctrl_csde e	dee	csa	task	unused_task_csde	е					
dee       csa       unsy       unsy_case_op_csde       e       Un-synthesizable case equality operator = at line @         dee       csa       unsy       unsy_deassn_stmt_csde       e       Un-synthesizable deassign statement at line @         dee       csa       unsy       unsy_defparam_csde       e       Un-synthesizable defparam at line @         dee       csa       unsy       unsy_dely_ctrl_csde       e       Un-synthesizable delay control at line @         dee       csa       unsy       unsy_evctrl_csde       e       Un-synthesizable event control at line @         dee       csa       unsy       unsy_evdecl_csde       e       Un-synthesizable event declaration at line @	dee	csa	topo	topo_sort_graph_csde	W					
dee csa unsy unsy_deassn_stmt_csde e Un-synthesizable deassign statement at line @  dee csa unsy unsy_defparam_csde e Un-synthesizable defparam at line @  dee csa unsy unsy_dely_ctrl_csde e Un-synthesizable delay control at line @  dee csa unsy unsy_evctrl_csde e Un-synthesizable event control at line @  dee csa unsy unsy_evctrl_csde e Un-synthesizable event declaration at line @	dee	csa	unsy	unsy_case_op_csde	е					Un-synthesizable case
dee csa unsy unsy_defparam_csde e Un-synthesizable defparam at line @  dee csa unsy unsy_dely_ctrl_csde e Un-synthesizable delay control at line @  dee csa unsy unsy_evctrl_csde e Un-synthesizable event control at line @  dee csa unsy unsy_evctrl_csde e Un-synthesizable event control at line @  dee csa unsy unsy_evdecl_csde e Un-synthesizable event declaration at line @				·						line @
dee csa unsy unsy_defparam_csde e Un-synthesizable defparam at line @  dee csa unsy unsy_dely_ctrl_csde e Un-synthesizable delay control at line @  dee csa unsy unsy_evctrl_csde e Un-synthesizable event control at line @  dee csa unsy unsy_evctrl_csde e Un-synthesizable event control at line @  dee csa unsy unsy_evdecl_csde e Un-synthesizable event declaration at line @	dee	csa	unsy	unsy_deassn_stmt_csde	е					
dee csa unsy unsy_dely_ctrl_csde e Un-synthesizable delay control at line @  dee csa unsy unsy_evctrl_csde e Un-synthesizable event control at line @  dee csa unsy unsy_evctrl_csde e Un-synthesizable event control at line @  dee csa unsy unsy_evdecl_csde e Un-synthesizable event declaration at line @	dee	csa	unev	unsv defnaram csde	6					line @
dee csa unsy unsy_evctrl_csde e Un-synthesizable event control at line @  dee csa unsy unsy_evdecl_csde e Un-synthesizable event control at line @  dee csa unsy unsy_evdecl_csde e Un-synthesizable event declaration at line @			-	•						defparam at line @
dee csa unsy unsy_evdecl_csde e Un-synthesizable event declaration at line @				•- •						control at line @
dee csa unsy unsy_evdecl_csde e Un-synthesizable event declaration at line @	dee	csa	unsy	unsy_evctrl_csde	е					
	dee	csa	unsy	unsy_evdecl_csde	е					Un-synthesizable event
	dee	csa	unsy	unsy_forc_stmt_csde	е					

Cat	Phase	Туре	Name	W/E V199	5 V2001	Sys_ver Csl	Desc
dee	csa	unsy	unsy_fok_stmt_csde	е			statement at line @ Un-synthesizable fork statement at line @
dee	csa	unsy	unsy_init_csde	е			Un-synthesizable initial at line @
dee	csa	unsy	unsy_prim_def_csde	е			Un-synthesizable primitive definition at line
dee	csa	unsy	unsy_rel_stmt_csde	е			@ Un-synthesizable release statement at line @
dee	csa	unsy	unsy_rep_stmt_csde	е			Un-synthesizable repeat statement at line @
dee	csa	unsy	unsy_time_decl_csde	е		t	Un-synthesizable timeDeclaration at line @
dee	csa	unsy	unsy_trns_csde	е			Un-synthesizable transistor at line @
dee	csa	unsy	unsy_wait_stmt_csde	е			Un-synthesizable wait statement at line @
dee	csb	blk	blk_cont_assign_not_allowed_csbde	е			Procedural continuous assignment is not
dee	csb	cyb	cyb_stmt_repeat_evc_in_blocking_assign_csbde	е			allowed at line @ Statement intra-assignment repeat event control in blocking assignment detected at line @
dee	csb	cyb	cyb_stmt_evc_in_blocking_assign_csbde	е			Statement
							intra-assignment event control in blocking assignment detected at line @
dee	csb	cyb	cyb_stmt_repeat_evc_in_non_blk_assign_csbde	е			Statement intra-assignment repeat
dee	csb	cyb	cyb_stmt_evc_in_non_blk_assign_csbde	e			event control in non-blocking assignment detected at line @ Statement intra-assignment event control in non-blocking assignment detected at line @
dee	csb	cyb	cyb_deassign_stmt_not_stimul_csbde	е			De-assign statement can't be simulated at line
dee	csb	cyb	cyb_forever_loop_not_stimul_csbde	е			Forever-loop is can't be simulated at line @
dee	csb	dely	inappropriate_form_intra_assign_dely_csbde	е			Intra-assignmentDelay control in blocking assignment not of form #O or #1 at line @
dee	csb	forc	cannot_forc_prts_net_csbde	е		8	Cannot force a partially selected Net name at line
dee	csb	forc	cannot_forc_prts_port_csbde	е			Cannot force a partially selected Port name at line @
dee	csb	forc	cannot_forc_prts_signal_csbde	е			Cannot force a partially selected Signal name at line @
dee	csb	inst	inst_mult_connections_port_csbde	е			Port 'port' has multiple connections specified at
dee	csb	inst	inst_unknown_port_name_csbde	е			line @ Unknown port name @ in named port connection at line @
dee	csb	inst	too_many_port_connections_inst_csbde	е			Too many port connections specified for
dee	csb	inst	inst_port_mod_width_csbde	е			instance @ at line @ Input port @ in module @ width mismatch, actual-width (port-width) at line @
dee	csb	inst	inst_port_entity_width_csbde	е			Input port @ in entity @ width mismatch,
dee	csb	inst	inst_port_unit_width_csbde	е			actual-width (port-width) at line @ Input port @ in unit @ width mismatch, actual-width (port-width) at line @
dee	csb	inst	inst_output_mod_port_width_csbde	е			Output port @ in module width mismatch, actual-width (port-width)
dee	csb	inst	inst_output_entity_port_width_csbde	e			at line @ Output port @ in entity width mismatch, actual-width (port-width) at line @
dee	csb	inst	inst_output_unit_port_width_csbde	е			Output port @ in unit width mismatch, actual-width (port-width)

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
dee	csb	inst	inst_mod_not_contain_port_csbde	е					at line @ Module @ does not
dee	csb	inst	inst_entity_not_contain_port_csbde	е					contain Port @ at line @ Entity @ does not
dee	csb	inst	inst_unit_not_contain_port_csbde	е					contain Port @ at line @ Unit @ does not contain
			<del>_</del> _						Port @ at line @
dee	csb	inst	inout_port_mod_width_csbde	е					Inout port @ in module width mismatch, actual width (port-width) at line
dee	csb	inst	inout_port_entity_width_csbde	е					Inout port @ in entity width mismatch, actual width (port-width) at line @
dee	csb	inst	inout_port_unit_width_csbde	е					Inout port @ in unit width mismatch, actual width (port-width) at line @
dee	csb	mdn	mdn_cannot_be_forced_csbde	е					Multiple drive Net 'name' cannot be forced. at line
dee	csb	mdn	mdn_port_cannot_be_forced_csbde	е					Multiple drive Port 'name' cannot be forced. at line
dee	csb	mdn	mdn_signal_cannot_be_forced_csbde	е					Multiple drive Signal 'name' cannot be forced. at line @
dee	csb	mifc	mifc_complex_port_decl_not_supported_csbde	е					Complex port Declaration port of module @ is not supported at line @
dee	csb	mifc	mifc_entity_complex_port_decl_not_supported_csbde	е					Complex port Declaration port of entity @ is not supported at line @
dee	csb	mifc	mifc_unit_complex_port_decl_not_supported_csbde	е					Complex port Declaration port of unit @ is not supported at line @
dee	csb	mifc	mifc_unknown_port_direction_csbde	е					Unknown port direction @ (port) at line @
dee	csb	mifc	mifc_input_port_is_mem_type_csbde	е					Input port @ is memory type at line @
dee	csb csb	num rel	num_division_by_zero_csbde cannot_rel_prts_net_csbde	e e					Division by zero at line @ Cannot release a
dee	csb	rel	cannot_rel_prts_port_csbde	е					partially selected Net name at line @ Cannot release a partially selected Port
dee	csb	rel	cannot_rel_prts_signal_csbde	е					name at line @ Cannot release a partially selected Signal
dee	csb	trns	trns_inst_not_allowed_csbde	е					name at line @ Transistor-level instantiations @ not
dee	CSC	blk	blk_cont_assign_not_allowed_cscde	е					allowed at line @ Procedural continuous assignment is not allowed at line @
dee	CSC	cyb	cyb_stmt_repeat_evc_in_blocking_assign_cscde	е					Statement intra-assignment repeat event control in blocking assignment detected at
dee	CSC	cyb	cyb_stmt_evc_in_blocking_assign_cscde	е					line @ Statement intra-assignment event control in blocking assignment detected at line @
dee	csc	cyb	cyb_stmt_repeat_evc_in_non_blk_assign_cscde	е					Statement intra-assignment repeat event control in non-blocking assignment
dee	CSC	cyb	cyb_stmt_evc_in_non_blk_assign_cscde	е					detected at line @ Statement intra-assignment event control in non-blocking assignment detected at line @
dee	CSC	cyb	cyb_deassign_stmt_not_stimul_cscde	е					De-assign statement can't be simulated at line
dee	CSC	cyb	cyb_forever_loop_not_stimul_cscde	е					@ Forever-loop is can't be
dee	CSC	dely	inappropriate_form_intra_assign_dely_cscde	е					simulated at line @ Intra-assignmentDelay control in blocking assignment not of form
dee	CSC	dmsn	dee_csc_dmsn_already_set_dim	е					#O or #1 at line @ Number of dimensions
dee	CSC	dmsn	dee_csc_dmsn_0dim	е					already set at line @ Number of dimensions can not be 0 at line @
dee	CSC	dmsn	dee_csc_dmsn_dim_not_set	е					Number of dimensions not set at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl Desc	
dee	CSC	dmsn	dee_csc_dmsn_illegal_dim	е			_	Illegal dimens number at lin	
dee	CSC	dmsn	dee_csc_dmsn_multidim_object	е				Multi-dimensiona	al object
dee	CSC	dsgn	dee_csc_dsgn_illegal	е				at line @ Parent should	be the
dee	CSC	dsgn	dee_csc_dsgn_illegal_parent	е				design at line Parent should b	
dee	CSC	dsgn	dee_csc_dsgn_illegal_parent1	е				declaration at Parent should	
								instance at lir	ne @
dee	CSC	dsgn	dee_csc_dsgn_already_set_width	е				Width or range set at line	@
dee	CSC	forc	cannot_forc_prts_net_cscde	е				Cannot force a page selected Net name	
dee	CSC	forc	cannot_forc_prts_port_cscde	е				Cannot force a page selected Port name line @	
dee	CSC	forc	cannot_forc_prts_signal_cscde	е				Cannot force a selected Signal line @	
dee	CSC	id	dee_csc_id_name_exists	е				Name @ alread	
dee	CSC	id	dee_csc_scop_undefined_scope	е				at line @ Undefined scop	
dee	CSC	inst	inst_mult_connections_port_cscde	е				Port 'port' has r connections spe	
dee	CSC	inst	inst_unknown_port_name_cscde	е				line @ Unknown port na	me @ in
								named port conn line @	ection at
dee	CSC	inst	too_many_port_connections_inst_cscde	е				Too many p connections spe- instance @ at	cified for
dee	CSC	inst	inst_port_mod_width_cscde	е				Input port @ in @ width mism actual-width (po	natch, rt-width)
dee	CSC	inst	inst_port_entity_width_cscde	е				at line @ Input port @ in e width misma actual-width (po	entity @ itch, rt-width)
dee	CSC	inst	inst_port_unit_width_cscde	е				at line @ Input port @ in width misma actual-width (po	unit @ itch,
dee	CSC	inst	inst_output_mod_port_width_cscde	е				at line @ Output port @ in width misma actual-width (po	module itch, rt-width)
dee	CSC	inst	inst_output_entity_port_width_cscde	е				at line @ i Output port @ i width misma actual-width (po	n entity itch, rt-width)
dee	csc	inst	inst_output_unit_port_width_cscde	е				at line @ Output port @ width misma actual-width (pol at line @	in unit itch, rt-width)
dee	CSC	inst	inst_mod_not_contain_port_cscde	е				Module @ doe	es not
dee	CSC	inst	inst_entity_not_contain_port_cscde	е				contain Port @ a Entity @ doe	s not
dee	CSC	inst	inst_unit_not_contain_port_cscde	е				contain Port @ a Unit @ does not	
dee	CSC	inst	inout port mod width cscde	е				Port @ at lin Inout port @ in	
ucc	000	11100	mod_por_mod_man_occdo					width mismatch width (port-width @	, actual
dee	CSC	inst	inout_port_entity_width_cscde	е				Inout port @ in width mismatch width (port-width	, actual
dee	CSC	inst	inout_port_unit_width_cscde	е				Inout port @ in u	al width
dee	CSC	mdn	mdn_cannot_be_forced_cscde	е				(port-width) at Multiple drive Ne	et 'name'
dee	CSC	mdn	mdn_port_cannot_be_forced_cscde	е				cannot be forced @ Multiple drive Po	
								cannot be forced	d. at line
dee	csc	mdn	mdn_signal_cannot_be_forced_cscde	е				Multiple drive iname' cannot be at line @	e forced.
dee	CSC	mifc	mifc_complex_port_decl_not_supported_cscde	е		-		Complex port De port of module ( supported at li	@ is not
dee	CSC	mifc	mifc_entity_complex_port_decl_not_supported_cscde	е				Complex port De port of entity @ supported at li	claration is not
dee	CSC	mifc	mifc_unit_complex_port_decl_not_supported_cscde	е				Complex port De	

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									port of unit @ is not supported at line @
dee	CSC	mifc	mifc_unknown_port_direction_cscde	е					Unknown port direction
dee	CSC	mifc	mifc_input_port_is_mem_type_cscde	е					@ (port) at line @ Input port @ is memory
dee	CSC	num	num_division_by_zero_cscde	е					type at line @ Division by zero at line @
dee	CSC	rel	cannot_rel_prts_net_cscde	е					Cannot release a partially selected Net
dee	CSC	rel	cannot_rel_prts_port_cscde						name at line @ Cannot release a
uee	CSC	rei	cannot_rei_pris_port_cscde	е					partially selected Port
dee	CSC	rel	cannot_rel_prts_signal_cscde	е					name at line @ Cannot release a
									partially selected Signal name at line @
dee	CSC	scop	dee_csc_scop_cannot_find_object	е					Cannot find object in scope at line @
dee	CSC	stmt	dee_csc_stmt_type_expected	е					Illegal type at line @ Transistor-level
dee	CSC	trns	trns_inst_not_allowed_cscde	е					instantiations @ not
dee	csp	mifc	mifc_unknown_port_direction_csde	е					allowed at line @ Unknown port direction
dee	csp	netd	net_decl_no_range_csde	е					for port @ at line @ Net declared with no
	· ·								range specification used with bit/part select at line
doo	200	natal	noted post no rouge and						@
dee	csp	netd	netd_port_no_range_csde	е					Port declared with no range specification used
									with bit/part select at line @
dee	csp	netd	netd_signal_no_range_csde	е					Signal declared with no range specification used
									with bit/part select at line @
dee	csp	port	port_decl_no_range_csde	е					Port declared with no
									range specification used with bit/part select at line
dee	vep	mifc	mifc_unknown_port_direction_vede	е					@ Unknown port direction
dee	vep	netd	net_decl_no_range_vede	е					for port @ at line @ Net declared with no
			<u></u>						range specification used with bit/part select at line
doo		natal	noted port no rooms years						. @
dee	vep	netd	netd_port_no_range_vede	е					Port declared with no range specification used
									with bit/part select at line @
dee	vep	netd	netd_signal_no_range_vede	е					Signal declared with no range specification used
									with bit/part select at line @
dee	vep	port	port_decl_no_range_vede	е					Port declared with no range specification used
									with bit/part select at line
dee	vhp	mifc	mifc_unknown_port_direction_vhde	е					@ Unknown port direction
dee	vhp	netd	net_decl_no_range_vhde	е					for port @ at line @ Net declared with no
	·								range specification used with bit/part select at line
dee	vhp	netd	netd_port_no_range_vhde	е					@ Port declared with no
uee	viip	neta	netd_port_no_range_vnde	е					range specification used
									with bit/part select at line @
dee	vhp	netd	netd_signal_no_range_vhde	е					Signal declared with no range specification used
									with bit/part select at line
dee	vhp	port	port_decl_no_range_vhde	е					Port declared with no range specification used
									with bit/part select at line
ne	csp	num	sillnum_hex	е					@ Illegal character @ at line
ne	vep	num	cillnum_hex	е					@ Illegal character @ at line
ne	vhp	num	hillnum_hex	е					@ Illegal character @ at line
res	csa	file	cannot_open_statistic_file_	w					@ Cannot open statistics
			-·						file @ at line @
vee	cda	assn	unequal_length_lhs_rhs_cdve	е					Unequal length LHS and RHS at line @
vee	cda	assn	unequal_length_lhs_rhs_off_one_bit_cdve	е					Unequal length LHS and RHS off by one bit at line
vee	cda	blk	repeat_in_nonblk_assn_cdve	е					@ Repeat in non-blocking
	Juu	~ii\	. op out_m_nonbm_udon_ouve						assignment at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	cda	blk	empty_blk_cdve	е			, -		Empty-block at line @
vee	cda	clk	unsupp_logic_operation_cdve	W					Unsupported logic operation type @. at line
vee	cda	clk	unsupp_cl_gated_logic_cdve	w					@ Unsupported gated clock logic type. at line @
vee	cda	clk	unsupp_logic_expr_clk_cdve	w					Unsupported logicExpression type @
vee	cda	csi	duplicate_csi_cdve	е					at line @ Duplicate Case item @
vee	cda	csi	case_sel_contains_real_num_const_cdve	е					at line @ Case selector contains a constant real number at
vee	cda	csi	csi_contains_real_num_const_cdve	е					line @  Case item contains a
									constant real number at line @
vee	cda cda	csi	real_in_csi_cdve noncnst_in_iclude_file_cdve	e					Real @ in case item at line @  Non-constant in include
vee	cda	csi	csi_width_mismatch_cdve	e					file @ at line @  Case item @ width
									mismatch at line @
vee	cda cda	csi	efault_missing_cdve not_all_csi_specified_cdve	e					Default missing at line @ Not allCase items are
100	ouu	000	not_an_ool_opoomoa_oavo						specified @ at line @
vee	cda	defd	mod_def_within_mod_not_in_include_cdde	е					Module define within module but not in include at line @
vee	cda	defd	ent_def_within_ent_not_in_include_cdde	е					Entity define within entity but not in include at line @
vee	cda	defd	unit_def_within_unit_not_in_include_cdde	е					Unit define within unit but
vee	cda	dely	comb_blk_contains_dely_assn_cdve	е					not in include at line @ Combinational block
									contains delay assignement at line @
vee	cda	dely	seq_blk_contains_dely_assn_cdde	е					Sequential block contains delay
vee	cda	dely	comb_blk_dely_between_stms_cdve	е					assignement at line @ Combinational block contains delay between
vee	cda	dely	seq_blk_dely_between_stmt_cdve	е					statements at line @ Sequential block
		,							contains delay between statements at line @
vee	cda	dely	dely_in_nonblk_assn_comb_cdve	е					Delay in nonblocking assignement in combinational at line @
vee	cda	dely	dely_in_nonblk_assn_seq_cdve	е					Delay in nonblocking assignement in sequential at line @
vee	cda	drst	drvs_not_in_lib_cdve	е					Drive strength @ not in library at line @
vee	cda	drvc	output_arg_appers_rhs_cdve	W					Output argument @ of user system task appears in RHS and is driven elsewhere at line @
vee	cda	drvc	multiple_init_blk_drvc_cdve	w					Multiple initial blocks force 'narne' at line @
vee	cda	drvc	net_multiple_always_blk_cdve	W					Net @ multiple always blocks at line @
vee	cda	drvc	port_multiple_always_blk_cdve	w					Port @ multiple always blocks at line @
vee	cda	drvc	sig_multiple_always_blk_cdve	w					Signal @ multiple always
vee	cda	drvc	net_multiple_stmt_cdve	w					blocks at line @ Net @ multiple statements with in the
vee	cda	drvc	port_multiple_stmt_cdve	w					same always at line @ Port @ multiple statements with in the
vee	cda	drvc	sig_multiple_stmt_cdve	w					same always at line @ Signal @ multiple statements with in the
vee	cda	drvc	multiply_drvn_net_nontri_gate_cdve	w					same always at line @ Multiply drivenNet driven
			, , , , , , , , , , , , , , , , , , , ,						by a non-tristate gate at line @
vee	cda	drvc	multiply_drvn_port_nontri_gate_cdve	W					Multiply drivenPort driven by a non-tristate gate at line @
vee	cda	drvc	multiply_drvn_sig_nontri_gate_cdve	w					Multiply drivenSignal driven by a non-tristate gate at line @
vee	cda	drvc	incompatible_driver_net_cdve	W					Incompatible driver of type @ drivingNet_@ multi drivenNet of type @
vee	cda	drvc	incompatible_driver_port_cdve	W					name @ at line @ Incompatible driver of

Cat	Phase	Туре	Name	W/F	V1995	V2001	Sys_ver	Csl Desc
Out	Tilasc	турс	Hame	***/_	V 1333	12001	Oy3_VCI	type @ drivingPort_@
								multi drivenPort of type @ name @ at line @
vee	cda	drvc	incompatible_driver_sig_cdve	w				Incompatible driver of
								type @ drivingSignal_@ multi drivenSignal of type
								@ name @ at line @
vee	cda	dsbl	dsbl_used_cdve	е				Disable used at line @
vee	cda	evc	embedded_ectl_cdve	е				Embedded-event-control at line @
vee	cda	expr	unary_op_in_comparison_cdve	е				Unary op used in
vee	cda	expr	shift by non constcdve	е				comparison at line @ Shift by non constant @
VCC	cua	СХРІ	Shirt_by_hon_constauve_					at line @
vee	cda	expr	miss_parenthesis_cdve	е				Unary op @ with
								comparison op @ missing precedence
		,						parenthesis at line @
vee	cda	forc	no_release_stmt_in_init_blk_cdve	W				Force @ statement in the initial block and there is
								no release statement.for
vee	cda	forc	no_force_stmt_in_init_blk_cdve	w	?			@ at line @ Release @ statement in
100	odd	1010	110_10100_04111_11111_0411_0410	"				the and there is no force
								statement.for @ at line @
vee	cda	forc	forcing_input_port_cdve	е				Forcing input port @ at
1/00	ada	func	return value not at and of fune adve					line @  Return value not at end
vee	cda	Tunc	return_value_not_at_end_of_func_cdve	е				of function at line @
vee	cda	func	time_and_evctrl_in_func_cdve	е				Time and event control in
vee	cda	func	func_call_itself_rec_cdve	е				function at line @ Function @ calling itself
								recursively at line @
vee	cda	gate	error_output_terminal_cdve	W			х	IEEE 1364-1995 error output terminal @. This
								will compile and simulate
								correctly on commercial
								verilog simulators at line @
vee	cda	init	assn_mem_in_init_blk_cdve	е				Assign memory in initial
vee	cda	inst	input_port_drvn_from_inside_mod_cdve	е				block at line @ Input port @ being driven
	0 3.0.							from inside of module @
vee	cda	inst	input_port_drvn_from_inside_entity_cdve	е				at line @ Input port @ being driven
VCC	cua	IIISt	input_port_drvn_nom_mside_entity_cdve					from inside of entity @ at
1/00	cda	inst	input port drvn from inside signal cdve					line @ Input port @ being driven
vee	cua	11151	input_port_drvit_from_friside_signal_cdve	е				from inside of signal @ at
	ada	inat	input part not connected in parent mad adua					line @
vee	cda	inst	input_port_not_connected_in_parent_mod_cdve	е				Input port @ not connected in parent
								module at line @
vee	cda	inst	input_port_not_connected_in_parent_entity_cdve	е				Input port @ not connected in parent
								entity at line @
vee	cda	inst	input_port_not_connected_in_parent_signal_cdve	е				Input port @ not connected in parent
								signal at line @
vee	cda	mdb	single_comp_contains_multiple_tri_drv_cdve	W				A single component contains multiple tristate
								drivers at line @
vee	cda	mdb	unsuppexpr_on_lhs_net_drv_stmt_cdve	W				Unsupported Expression type type on LHS of Net
								driver statement at line
								@
vee	cda	mdb	unsuppexpr_on_lhs_port_drv_stmt_cdve	W				Unsupported Expression type type on LHS ofPort
								driver statement at line
vee	cda	mdb	unsuppexpr_on_lhs_sig_drv_stmt_cdve	w				@ Unsupported Expression
706	Jua	mub	anoupponpi_ori_ino_org_urv_orrit_ouve	**				type type on LHS
								ofSignal driver statement at line @
vee	cda	mdb	tri_not_in_top_mod_cdve	е				Tristate not in top module
V00	cdo	mdh	tri not in ton ont odyo	_				at line @
vee	cda	mdb	tri_not_in_top_ent_cdve	е				Tristate not in top entity at line @
vee	cda	mdb	tri_not_in_top_sig_cdve	е				Tristate not in top signal
vee	cda	mdb	tri_primitive_inst_cdve	е				at line @ Tristate primitive
								instantiation at line @
vee	cda	mdb	tri_net_only_one_drvr_cdve	е				Tri Net has only one driver at line @
vee	cda	mdb	tri_port_only_one_drvr_cdve	е				Tri Port has only one
vee	cda	mdb	tri_sig_only_one_drvr_cdve	е				driver at line @ Tri Signal has only one
			_ 5_					driver at line @
vee	cda	mem	single_bit_mem_cdve	е				Single bit memory @ at line @
				1	1	l		iiile @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_v	er Csl	
vee	cda	mod	redef_mod_cdve	е					Redefined module @ at line @
vee	cda	mod	redef_ent_cdve	е					Redefined entity @ at line @
vee	cda	mod	redef_signal_cdve	е					Redefined signal @ at line @
vee	cda	net	tri_and_net_only_one_driver_cdve	е	?				triandNet @ has only one driver at line @
vee	cda	net	tri_and_port_only_one_driver_cdve	е	?				triandPort @ has only one driver at line @
vee	cda	net	tri_and_sig_only_one_driver_cdve	е	?				triandSignal @ has only one driver at line @
vee	cda	net	var_assn_but_never_ref_cdve	е					Variable @ assigned but never referenced at line
vee	cda	net	var never assn cdve	е					@ Variable @ never
vee	cda	net	var_net_assn_in_all_paths_cdve	е					assigned at line @  Variable @ not being
VCC	cua	net	vai_not_assii_m_aii_pairis_cuve	6					assigned in all paths at line @
vee	cda	net	var_not_in_snsl_cdve	е					Variable @ not in
vee	cda	net	reg_connected_to_inout_in_inst_cdve	е					sensitivity list at line @ Reg @ connected to
									inout @ in instantiation @ at line @
vee	cda	net	reg_connectede_to_output_in_inst_cdve	е					Reg @ connected to output in instantiation at
vee	cda	net	reg_used_as_output_of_cont_assn_cdve	е					line @ Reg @ used as output of
									continuous assign at line @
vee	cda	net	port_used_prior_to_decl_cdve	е					Port @ used prior toDeclaration at line @
vee	cda	net	dupl_sig_in_snsl_cdve	е					Duplicate signal @ in sensitivity list at line @
vee	cda	netd	var_never_assigned_cdve	е					Variable @ never assigned at line @
vee	cda	num	assignment_contains_real_num_const_cdve	е					Assignment contains a real number constant at
vee	cda	parm	unused_parm_cdve	е					line @ Unused parameter @ at
vee	cda	parm	redef_param_cdve	e					line @  Redefined parameter @
vee	cda		redef_macro_cdve	е					at line @  Redefined macro @ at
vee	cda	pp	prts_on_vec_net_not_allowed_cdve	w					line @ Part select @ on a
vee	cua	pris	pris_on_vec_net_not_anoweu_cuve	VV					vectored Net may not be allowed according to
									IEEE 1364-1995 at line
vee	cda	prts	prts_on_vec_port_not_allowed_cdve	W					Part select @ on a
									vectored Port may not be allowed according to
									IEEE 1364-1995 at line
vee	cda	prts	prts_on_vec_sig_not_allowed_cdve	W					Part select @ on a vectored Signal may not
									be allowed according to IEEE 1364-1995 at line
vee	cda	prts	out_of_range_bit_ref_cdve	е					@ Out of range bus bit
vee	cda	prts	vec_index_order_incorrect_cdve	е					referenced at line @ Vector index @ order
vee	cda	prts	vec_index_truncated_cdve	е					incorrect at line @ Vector index @ truncated
vee	cda	sdir	sdir_compiler_cdve	е					at line @ Found synopsys
			•						compiler directive at line @
vee	cda	seq	blk_not_in_lib_cdve	е					Block @ not in library at line @
vee	cda	sig	sig_will_float_when_rel_cdve	е					Signal @ will float when it is released at line @
vee	cda	snsl	var_modified_in_snsl_cdve	е					Variable @ modified in sense list at line @
vee	cda	snsl	var_in_snsl_unsused_in_blk_cdve	е					Variable @ in sensitivity list not used in block at
vee	cda	snsl	rhs_var_noi_in_snsl_cdve	е					line @  RHS variable not in
vee	cda	spec	spec_blk_found_cdve	е					sensitivity list at line @ Specify block found at
vee	cda	•	sply_being_driven_cdve	e					line @ Supply being driven at
		sply							line @ Supply not defined with
vee	cda	sply	sply_not_def_user_keyword_cdve	е					user defined keyword at
vee	cda	sply	sply_not_in_lib_cdve	е					line @ Supply not in library at
					L				line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	cda	sply	output_conncet_to_sply_	е					Output @ connect to supply at line @
vee	cda	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_cdve	е					Arithmetic operator RHS has one less bit than the
1/00	odo	otmt	or on unaqual lba the adva						LHS at line @
vee	cda	stmt	ar_op_unequal_lhs_rhs_cdve	е					Arithmetic operator unequal width LHS and
vee	cda	stmt	ar_op_unequal_var_on_rhs_cdve	е					RHS at line @ Arithmetic operator
									unequal width variables @ on RHS at line @
vee	cda	task	task_call_iteslf_rec_cdve	е					Task @ calling itself recursively at line @
vee	cda	time	time_var_bit_used_cdde	е					Time variable bit used at line @
vee	cda	tri	tri_not_in_top_mod_cdve	е					Tristate @ not in top
vee	cda	tri	tri_not_in_top_entity_cdve	е					module at line @ Tristate @ not in top
vee	cda	tri	tri_not_in_top_signal_cdve	е					entity at line @ Tristate @ not in top
vee	cda	tri	tri_prim_ist_cdve	е					signal at line @ Tristate primitive
vee	cda	udp	upd_not_supported_cdve	е					instantiation @ at line @ UDPs are not supported
vee	cdc	assn	x_in_rhs_of_assihnment_cdcve	е					at line @  x in rhs of assignment at
									line @
vee	cdc	assn	z_in_rhs_of_assn_default_csi_cdcve	е					x in rhs of assignement in defaultCase item at
vee	cdc	assn	z_in_rhs_of_assn_cdcve	е					line @ z in rhs of assignement
vee	cdc	assn	unequal_length_lhs_rhs_cdcve	е					at line @ Unequal length LHS and
vee	cdc	assn	unequal_length_lhs_rhs_off_one_bit_cdcve	е					RHS at line @ Unequal length LHS and
									RHS off by one bit at line
vee	cdc	blk	blk_ill_block_id_cdv	е					Illegal block @ at line @
vee	cdc	blk	nonblocking_assign_in_comb_always_blk_cdcve	е					Non blocking aasignment in combinational always
vee	cdc	blk	seq_blk_contains_blk_assn_cdcve	е					block at line @ Sequential block
									contains blocking assignement at line @
vee	cdc	casn	LHS_not_reg_casn_vhve	е					LHS cannot be a register @ at line @
vee	cdc	ccd	ccd_cdir_must_be_cst_expr_cdcve	е				Х	CSL directive size must be constant Expression
1400	ada	alle	ally pages pat found adir adous					.,	at line @  Clock name not found in
vee	cdc	clk	clk_name_not_found_cdir_cdcve	е				х	cslc directive at line @
vee	cdc	clk	expr_sunj_to_different_clk_phases_cdcve	е					Expression subject to different clock phases at
vee	cdc	cmdl	cannot_use_librescan_with_liborder_specified_cdcve	е					line @ Cannot use +librescan
									when +liborder has already been specified at
vee	cdc	cmdl	cannot_use_liborder_with_librescan_specified_cdcve	е					line @ Cannot use +liborder
									when +librescan has already been specified at
1/00	cdc	oond	if case question cond cdcve						line @
vee	cac	cond	ii_case_questioii_cond_cdcve	е					expression expr syntax
vee	cdc	cond	if_no_else_in_comb_blk_cdcve	е					error at line @ If no else in
									combinational block at line @
vee	cdc	cond	if_no_else_in_comb_blk_cdcvh	е					If no else in combinational block at
vee	cdc	csi	xcsi not in casex cdcve	е					line @ xCase item not in casex
vee	cdc	csi	noncnst_csi_cdcve	е					at line @  Non-constantCase item
									@ at line @
vee	cdc	csi	noncnst_dely_cdcve	е					Non-constant delay @ at line @
vee	cdc	csi	noncstn_rep_in_conc_cdcve	е					Non-constant repeator in concatenation at line @
vee	cdc	CSS	sns_pragma_full_case_cdcve	е				[	Assume a full case, missing default or
									synopsys pragma full case. at line @
vee	cdc	cyb	repeat_in_delay_cyb_cdv	е					Repeat clause in delay not supported at line @
vee	cdc	cyb	repeat_in_event_control_cyb_cdv	е					Repeat clause in event control not supported at
1/0-	مطء	-اد ده	ovent id not supported at a dis-						line @
vee	cdc	cyb	event_id_not_supported_cyb_cdv	е					@ event id is not supported at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ve	r Csl	Desc
vee	cdc	cyb	ill_proc_assign_cyb_cdv	е		1 - 0 0 1	- J		Illegal procedural continuous assignment
									statement at line @
vee	cdc	cyb	ill_deassign_cyb_cdv	е					Illegal de-assign statement at line @
vee	cdc	cyb	ill_force_cyb_cdv	е					Illegal force statement at line @
vee	cdc	cyb	ill_release_cyb_cdv	е					Illegal release statement at line @
vee	cdc	cyb	repeat_as_delay_cyb_cdv	е					Repeat as delay not
vee	cdc	cyb	repeat_as_event_control_cyb_cdv	е					supported at line @ Repeat as event control
vee	cdc	cyb	wait_statement_not_cyb_cdv	е					not supported at line @ Wait statement is not
vee	cdc	cyb	disable_statement_not_cyb_cdv	е					supported at line @ Disable statement is not
		-							supported at line @
vee	cdc	cyb	events_not_supported_cyb_cdv	е					Events are not supported at line @
vee	cdc	cyb	fork_join_blocks_not_supported_cyb_cdv	е					Fork/join blocks are not supported at line @
vee	cdc	cyb	unsupp_function_return_time_cyb_cdv	е					Unsupported function return time at line @
vee	cdc	cyb	not_supp_events_cyb_cdv	е					Events are not supported at line @
vee	cdc	cyb	repeat_in_delay_or_event_cyb_cdv	е					Repeat clause in delay or
vee	cdc	cyb	ill_proc_cont_assign_stmt_cyb_cdv	е					Event control at line @ Illegal procedural
									continuous assignment statement at line @
vee	cdc	cyb	ill_deassign_cyb_stmt_cdc	е					Illegal de-assign statement at line @
vee	cdc	cyb	ill_force_stmt_cyb_cdv	е					Illegal force statement at
vee	cdc	cyb	ill_release_stmt_cyb_cdv	е					line @ Illegal release statement
vee	cdc	cyb	repeat_not_supp_as_delay_or_event_cyb_cdv	е					at line @ Repeat as delay or event
		,	,,, - ,, - ,, -						control not supported at line @
vee	cdc	cyb	not_supp_wait_stmt_cyb_cdv	е					Wait statement is not supported at line @
vee	cdc	cyb	not_supp_disable_stmt_cyb_cdv	е					Disable statement is not
vee	cdc	cyb	supp_not_events_cyb_cdv	е					supported at line @ Events are not supported
vee	cdc	cyb	not_supp_fork_join_blocks_cyb_cdv	е					at line @ Fork/join blocks are not
vee	cdc	cyb	not_supp_UDP_cyb_cdv	е					supported at line @ UDPs are not supported
vee	cdc		not_supp_defparam_cyb_cdv	е					at line @ Defparam is not
		cyb							supported at line @
vee	cdc	cyb	specify_blk_not_supported_cdcve	е					Specify blocks are not supported at line @
vee	cdc	cyb	mintypmax_expr_not_supp_cdcve	W					mintypmax Expressions are not supported at line
vee	cdc	decl	decl array over max size cdcve	е					@ Array @ exceeds
									maximum size limit at line @
vee	cdc	dely	max_val_dly_cdv	е					Too many delay values,
vee	cdc	dely	found_gate_dely_not_allowed_cdcve	е					max @ at line @ Found gate delay which
vee	cdc	dely	found_dely_in_casn_not_allowed_cdcve	е					are not allowed at line @ Found delay in
			_ ,						continuous assignment which are not allowed at
1/00	odo	doly	dely ignoring dely specification cdcve						line @
vee	cdc	dely	dery_ignoring_dery_specification_cdcve	е					Delay Ignoring delay specification in Net
vee	cdc	dely	dely_ignoring_dely_specification_port_cdcve	е					Declaration at line @ Delay Ignoring delay
									specification in Port Declaration at line @
vee	cdc	dely	dely_ignoring_dely_specification_sig_cdcve	е					Delay Ignoring delay specification in Signal
		4-1.							Declaration at line @
vee	cdc	dely	dely_ignoring_dely_before_stmt_cdcve	е					Delay Ignoring delay before statement at line
vee	cdc	dely	x_or_z_in_dely_cdcve	е					@ x or z in delay at line @
vee	cdc	dely	non_int_dely_cdcve	е					Non integer delay at line @
vee	cdc	dmsn	mem_prts_index_out_of_range_for_mem_cdcve	е					Memory part select [@:@] index @ out
									range for memory @ at
vee	cdc	dmsn	dime_select_for_mem_missing_cdcve	е					line @ Select for memory @
vee	cdc	dmsn	dime_index_out_of_bounds_for_mem_cdcve	е					missing at line @ Index <index> out of</index>
									bounds for memory @.

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	cdc	dmsn	dime_prts_out_of_bounds_for_net_cdcve	е					Range [@: @] at line @ Part select [@: @] out of bounds for net @. Range
vee	cdc	dmsn	dime_prts_out_of_bounds_for_port_cdcve	е					[@ : @] at line @ Part select [@ : @] out of bounds for port @.
vee	cdc	dmsn	dime_prts_out_of_bounds_for_sig_cdcve	е					Range [@ : @] at line @ Part select [@ : @] out of bounds for signal @.
vee	cdc	dmsn	dime_prts_reg_cdcve	е					Range [@ : @] at line @ Part select [@ : @] reg @. Range [@ : @] at line
vee	cdc	drvc	incompatible_drvc_for_net_cdcve	е					@ Incompatible drivers for
vee	cdc	drvc	incompatible_drvc_for_port_cdcve	е					Net @ at line @ Incompatible drivers for
vee	cdc	drvc	incompatible_drvc_for_sig_cdcve	е					Port @ at line @ Incompatible drivers for
vee	cdc	drvc	drvc_multiple_drive_net_partially_overlap_cdcve	е					Signal @ at line @ Multiple drive Net partially overlap at line @
vee	cdc	drvc	drvc_multiple_drive_port_partially_overlap_cdcve	е					Multiple drive Port
vee	cdc	drvc	drvc_multiple_drive_sig_partially_overlap_cdcve	е					partially overlap at line @ Multiple drive Signal partially overlap at line @
vee	cdc	dsgn	dsgn_top_mod_cannot_id_cdcve	е					Top module @ cannot be identified at line @
vee	cdc	dsgn	dsgn_top_entity_cannot_id_cdcve	е					Top entity @ cannot be identified at line @
vee	cdc	dsgn	dsgn_top_unit_cannot_id_cdcve	е					Top unit @ cannot be
vee	cdc	dsgn	unit_dsgn_cycle_not_spanning_tree_cdcve	е					identified at line @ Unit design hierarchy
									contains a cycle. Hierarchy is not a
vee	cdc	evc	not_allowed_edge_trigger_cdcve	е					spanning tree. at line @ Edge trigger is not
									allowed in this location at line @
vee	cdc	evc	ectl_in_assn_cdcve	е					Event control in assignement at line @
vee	cdc	expr	expr_prts_indices_1bit_var_cdcve	е					Part select indices 1-bit variable at line @
vee	cdc	expr	expr_prts_must_be_cst_expr_cdcve	е					Part select specifier Expression must be
									constant Expression at line @
vee	cdc	expr	not_const_expr_cdcve	е					Repetition multiplier in concatenation is not a
									constant Expression at line @
vee	cdc	expr	ill_bit_select_expr_cdcve	е					Illegal bit select expression @ at line @
vee	cdc	expr	equality_operator_detected_cdcve	е					Use of operator === detected at line @
vee	cdc	expr	notequal_operator_detected_cdcve	е					Use of operator !== detected at line @
vee	cdc	expr	ill_parm_value_cdcve	е					Illegal parameter value at line @
vee	cdc	expr	repetition_multiplier_in_conc_not_const_expr_cdcve	W					Repetition multiplier in concatenation is not a
									constant Expression at line @
vee	cdc	expr	int_operand_not_1_bit_cdcve	W					Logic operator has integer operands instead
									of 1-bit operands at line
vee	cdc	expr	unsupp_expr_cdcve	W					Unsupported Expression type @ at line @
vee	cdc	expr	unsupp_operator_cdcve	W					Unsupported operator type @ at line @
vee	cdc	expr	use_of_sg_bit_const_cdcve	W					Use of single bit constant at line @
vee	cdc	expr	unary_op_in_comparison_cdcve	е					Unary op used in comparison at line @
vee	cdc	expr	nonconst_repeator_in_conc_cdcve	е					Non constant repeator in
vee	cdc	expr	x_or_z_in_cond_expr_cdcve	е					x or z in conditional
vee	cdc	expr	zero_in_rep_in_conc_cdcve	е					expression at line @  Zero repeator in
vee	cdc	expr	expr_in_mod_port_dir_cdcve	е					concatenation at line @ Expression @ in module
vee	cdc	expr	expr_in_ent_port_dir_cdcve	е					port dir at line @ Expression @ in entity
vee	cdc	expr	expr_in_sig_port_dir_cdcve	е					port dir at line @ Expression @ in unit port
vee	cdc	expr	expr_in_inst_cdcve	е					dir at line @ Expression @ in inst i@
vee	cdc	expr	expr_operator_operands_unequal_lenght_cdcve	е					at line @ Expression operator @
			. – 3 –						operands @ unequal

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc length at line @
vee	cdc	file	cannot_open_filter_specification_file_cdcve	е					Cannot open filter specification file @ at line
vee	cdc	file	filter_specification_file_missing_cdcve	е					@ Filter specification file
vee	cdc	file	mismatch_mod_file_name_cdcve	е					name @ is missing at line @  Mismatch between module name @ and file
vee	cdc	file	mismatch ent file name cdcve	е					name @ at line @  Mismatch between entity
vee	cdc	file	mismatch_siq_file_name_cdcve	е					name @ and file name @ at line @ Mismatch between signa
VCC	cuc	IIIC	mismatch_sig_me_name_cucve						name @ and file name @ at line @
vee	cdc	forc	ill_forc_obj_type_cdcve	е					Illegal force object type @ at line @
vee	cdc	func	ill_func_return_type_cdv	е					Illegal function return type at line @
vee	cdc	func	ill_func_cdv	е					Illegal function @ at line @
vee	cdc	func	port_not_output_func_cdve	е					Port @ direction cannot be output at line @
vee	cdc	func	ill_use_func_cdcve	е					Illegal use of function @ at line @
vee	cdc	func	func_not_define_cdcve	е					Function @ not defined at line @
vee	cdc	func	too_many_arg_to_func_cdcve	е					Too many arguments passed to function @ at line @
vee	cdc	func	too_few_arg_to_func_cdcve	е					Too few arguments passed to function @ at line @
vee	cdc	func	undefined_func_cdcve	е					Undefined function @ at line @
vee	cdc	func	funct_expr_cannot_expnaded_cdcve	е					Function expression @ cannot be expanded at line @
vee	cdc	func	funct_not_used_in_expr_cdcve	w					Function @ is not being used in an Expression a line @
vee	cdc	func	func_decl_cdcve	w					Function Declaration @ already declared as another type at line @
vee	cdc	func	func_param_cdc	е					Found function parameter @ at line @
vee	cdc	func	unmatched_funct_param_cdcve	е					Unmatched function parameter @ at line @
vee	cdc	gate	ill_output_pin_name_gate_cdv	е					Illegal output terminal Expression pin @ at line
vee	cdc	hid	cannot_locate_hier_id_hid_cdcve	е					Can't locate hierarchical identifier @ at line @
vee	cdc	hid	ref_minst_found_in_expr_hid_cdcve	е					References a module instance @ found in an Expression hid at line @
vee	cdc	hid	ref_entity_found_in_expr_hid_cdcve	е					References a entity instance @ found in an Expression hid at line @
vee	cdc	hid	ref_unit_found_in_expr_hid_cdcve	е					References a unit instance @ found in an
vee	cdc	hid	ref_in_eexpr_hid_cdcve	е					Expression hid at line @  References a module instance @ passed as
									argument to PLI task cal is also found in an Expression @ at line @
vee	cdc	hid	ref_in_expr_hid_cdcve	е					References a entity instance @ passed as argument to PLI task cal is also found in an
vee	cdc	hid	reff_in_expr_hid_cdcve	е					Expression @ at line @ References a unit
			,						instance @ passed as argument to PLI task cal is also found in an
vee	cdc	hid	hid_name_traverses_into_func	е					Expression @ at line @ Hid @ name traverses into a function @ at line @
vee	cdc	hid	hid_ref_mod_out_arg_sytk_cdcve	е					Hid @ referencing a module instance passed as 'out' type argument to a system task @ at line @
vee	cdc	hid	hid_ref_entity_out_arg_sytk_cdcve	е					Hid @ referencing a entity instance passed a 'out' type argument to a
vee	cdc	hid	hid_ref_unit_out_arg_sytk_cdcve	е					system task @ at line @ Hid @ referencing a unit

Cat	Phase	Typo	Name	W/E	V/1005	V2001	Sys_ver	Csl	Desc
Cal	Filase	Type	Name	VV/E	V 1995	V2001	Sys_ver	CSI	instance passed as 'out' type argument to a system task @ at line @
vee	cdc	hid	hid_reference_not_found_cdcve	е					@ reference not found at
vee	cdc	hid	mifc_in_hid_not_exist_cdcve	е					line @ Module instance @ in hid
vee	cdc	hid	entity_instance_in_hid_not_exist_cdcve	е					does not exist at line @ Entity instance @ in hid
		hid	,						does not exist at line @ Unit instance @ in hid
vee	cdc	,	unit_instance_in_hid_not_exist_cdcve	е					does not exist at line @
vee	cdc	hid	mod_found_in_path_in_dsgn_cdcve	е					Module @ found in path @ in the design at line @
vee	cdc	hid	enity_found_in_path_in_dsgn_cdcve	е					Entity @ found in path @ in the design at line @
vee	cdc	hid	unit_found_in_path_in_dsgn_cdcve	е					Unit @ found in path @ in the design at line @
vee	cdc	hid	hierarchical_id_path_contains_func_cdc	е					Hierarchical ID @ path
									contains a function at line @
vee	cdc	id	ill_terminal_id_cdv	е					Illegal terminal identifier at line @
vee	cdc	init	assn_mem_in_init_blk_cdcve	е					Assign memory in initial block at line @
vee	cdc	inst	inst_duplicate_mod_name_cdcve	е					Duplicate port @ in the
									port list for module @ at line @
vee	cdc	inst	inst_duplicate_entity_name_cdcve	е					Duplicate port @ in the port list for entity @ at
				_					line @
vee	cdc	inst	inst_duplicate_unit_name_cdcve	е					Duplicate port @ in the port list for unit @ at line
vee	cdc	inst	miss declparam inst cdv	е					@ Parameter Declaration
vee	cdc	inst	ill_mod_inst_name_cdcve	е					missing value at line @ Illegal module instance
									@ at line @
vee	cdc	inst	ill_entity_inst_name_cdcve	е					Illegal entity instance @ at line @
vee	cdc	inst	ill_unit_inst_name_cdcve	е					Illegal unit instance @ at line @
vee	cdc	inst	inst_name_defined_mod_cdv	е					Instance name @ already defined in this
1/00	ada	inat	ingt name defined ant ody						module at line @
vee	cdc	inst	inst_name_defined_ent_cdv	е					Instance name @ already defined in this
vee	cdc	inst	inst_name_defined_unit_cdv	е					entity at line @ Instance name @
									already defined in this unit at line @
vee	cdc	inst	inst_too_many_bits_cdcve	е					Too many bits for port @ of instance array @.
									formal @, actual @ at
vee	cdc	inst	inst_port_not_connected_var_cdcve	е					line @ Port 'port' of instance
									array 'array' is not connected to variable at
vee	cdc	inst	inst_insufficient_bits_cdcve	е					line @ Insufficient bits for port
VCC	cuc	11130	mst_msumoiont_bits_cuove						'port' of instance array
									'array', formal number, actual number at line @
vee	cdc	inst	inst_mod_name_not_defined_cdcve	е					Module name not defined at line @
vee	cdc	inst	inst_ent_name_not_defined_cdcve	е					Entity name not defined at line @
vee	cdc	inst	inst_unit_name_not_defined_cdcve	е					Unit name not defined at
vee	cdc	inst	many_mod_inst_param_assign_cdcve	е					line @ Too many module
									instance parameter assignments (number >
vee	cdc	inst	many_entity_inst_param_assign_cdcve	е					rrumber) at line @ Too many entity instance
VCC	cuc	iiist	many_entity_inst_param_assign_cucve						parameter assignments
									(number > rrumber) at line @
vee	cdc	inst	many_unit_inst_param_assign_cdcve	е					Too many unit instance parameter assignments
									(number > rrumber) at line @
vee	cdc	inst	complexexpr_cannot_mapped_inout_port_cdcve	е					Complex Expression @
									cannot be mapped to inout port @ at line @
vee	cdc	inst	complexexpr_cannot_mapped_unknown_port_cdcve	е					Complex Expression @ cannot be mapped to
									unknown type port @ at line @
vee	cdc	inst	netdecl_contains_ill_prts_cdcve	е					Net Declaration [@: @]
									contains an illegal part select at line @
vee	cdc	inst	regdecl_contains_ill_prts_cdcve	е					Reg Declaration [@ : @]

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
		-71	7.00.10						contains an illegal part select at line @
vee	cdc	inst	complex_expr_inst_parent_module_cdcve	е					Complex actual
									Expression associated with port @ of module @
									instantiated in parent
1/00	ada	inat	compley ever inst entity parent module edeve						module at line @ Complex actual
vee	cdc	inst	complex_expr_inst_entity_parent_module_cdcve	е					Expression associated
									with port @ of entity @
									instantiated in parent module at line @
vee	cdc	inst	complex_expr_inst_unit_parent_module_cdcve	е					Complex actual Expression associated
									with port @ of unit @
									instantiated in parent module at line @
vee	cdc	inst	inst_mod_output_port_width_cdcve	е					Mod @ Output port @
									width mismatch, actual-width ( port-width )
									at line @
vee	cdc	inst	inst_entity_output_port_width_cdcve	е					Entity @ Output port @ width mismatch,
									actual-width ( port-width )
vee	cdc	inst	inst_unit_output_port_width_cdcve	е					at line @ Unit @ Output port @
100	ouo		moc_umc_oupuc_pon_man_ouovo						width mismatch,
									actual-width ( port-width ) at line @
vee	cdc	inst	inst_mod_input_port_width_cdcve	е					Mod @ Input port @
									width mismatch, actual-width ( port-width )
									at line @
vee	cdc	inst	inst_entity_input_port_width_cdcve	е					Entity @ Input port @ width mismatch,
									actual-width ( port-width )
vee	cdc	inst	inst_unit_input_port_width_cdcve	е					at line @ Unit @ Input port @
	000		o_apac_portaaoaoro						width mismatch,
									actual-width ( port-width ) at line @
vee	cdc	inst	inst_mod_not_define_cdcve	е					Module not defined at
vee	cdc	inst	inst_entity_not_define_cdcve	е					line @ Entity not defined at line
			_ <b>,</b>						@
vee	cdc cdc	inst inst	inst_unit_not_define_cdcve miss_mifc_name_cdcve	e w			Х		Unit not defined at line @ Missing module instance
									name. This syntax is an
									error according to IEEE 1364-1995 but is allowed
									by commercial Verilog compilers at line @
vee	cdc	inst	miss_ent_instance_name_cdcve	w			Х		Missing entity instance
									name. This syntax is an error according to IEEE
									1364-1995 but is allowed
									by commercial Verilog compilers at line @
vee	cdc	inst	miss_unit_instance_name_cdcve	w			Х		Missing unit instance
									name. This syntax is an error according to IEEE
									1364-1995 but is allowed
									by commercial Verilog compilers at line @
vee	cdc	inst	mifc_port_actual_formal_width_mismatch_cdcve	W					Module @ instance @
									port @ width mismatch, actual width @ formal
V00	cdc	inst	ant part actual formal width mismatch edges	w					width @ at line @ Entity @ instance @ port
vee	cuc	ıııəl	ent_port_actual_formal_width_mismatch_cdcve	vv					@ width mismatch,
									actual width @ formal width @ at line @
vee	cdc	inst	unit_port_actual_formal_width_mismatch_cdcve	W					Unit @ instance @ port
									@ width mismatch, actual width @ formal
									width @ at line @
vee	cdc	inst	unmatched_port_connect_in_inst_cdcve	е					Unmatched port @ connect in instance @ at
									line @
vee	cdc	inst	inst_differs_in_case_from_mod_cdcev	е					Instance name @ differs in case from module
		to a	ings different to the second						name @ at line @
vee	cdc	inst	inst_differs_in_case_from_ent_cdcve	е					Instance name @ differs in case from entity name
	e -1 -	le = '	ingt differe in and from						@ at line @
vee	cdc	inst	inst_differs_in_case_from_sig_cdcve	е					Instance name @ differs in case from signal name
110-	مطء	l:h	lib name not mad deal						@ at line @
vee	cdc	lib	lib_name_not_mod_declaration_cdv	е					Library file @ doesn't contain a module
									Declaration at line @

vee cdc iib lib_name_not_unit_declaration_cdv e Cuchan a native declaration_cdv e Cuchan a native declaratio									
vee dot lib lib_name_not_wind_declaration_cdv e	Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver Csl	Desc
Vee   cdc   lib   lib_name_not_unit_declaration_cdv   e	vee	cuc	IID	lib_name_not_entity_declaration_cdv	6				
vee ddc lib lib_not_contain_supply_cdove									Declaration at line @
veo cdc loop initial_value_unknown_loop_cdove e Lbrary-does not cont supply @ at line & vanable @ unassign initial_value_unknown_loop_cdove e vanable @ unassign initial_value_loop_cdove e vanable @ unassign initial_value_loop_cdove e vanable @ unassign initial_value_loop_cdove e value de loop undet_limit_loop_cdove e Unable to determine value vanable @ unassign initial_value_loop_cdove e Unable to determine value val	vee	cdc	lib	lib_name_not_unit_declaration_cdv	е				
Vee         doc         loop         Initial_value_unknown_loop_odove         e         supply 8 at time 8           Vee         doc         loop         while_loop_not_assign_stmt_controlvar_cdove         e         While loop body does control and seight in the loop_cdove         e         While loop body does control and assign_stmt_not_loat_while_loop_cdove         e         Control wanted 8         While loop body does control and assign_stmt_not_loat_while_loop_cdove         e         Assignment and the loop_cdove and loop_cdove         e         Assignment and loop_cdove         e         Assignment and loop_cdove         e         Assignment and loop_cdove         e         Unable to determine to control wanted for control wanted for loop and loop_bounds_calculated_ind_cdove         e         Unable to determine to control wanted for loop bounds_calculated_ind_cdove         e         Unable to determine to calculated to be intered.         d. check that this is calculated to be intered.         d. check that this is calculated to be intered.         d. check that this is calculated to be intered.         d. check that this is calculated to be intered.         d. check that this is calculated to be intered.         d. check that this is calculated to be intered.         d. check that this is calculated to be intered.         d. check that this is calculated to be intered.         d. check that this is calculated to be intered.         d. check that this is calculated to be intered.         d. check that this is calculated to be intered.         d. check that this is calculated to be intered. <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>									
Vee   Cold   C	vee	cdc	lib	lib_not_contain_supply_cdcve	е				Library does not contain
vealed @ unasign infinial value under the control variable of the contain a single of the contain a single contain an assignm statement for contain an assignment statement for contain an assignment statement for contain an assignment statement for contain and the contain assignment statement in who statement in who sop at first @ Unable to determine the contain assignment contains contain assignment contain									supply @ at line @
Veb   Coc   Coop   while_loop_not_assign_stmt_controlvar_colove   o   While_loop_not_assign_stmt_controlvar_colove   o   While_loop_colovby does   Satement for control variable @1 at line @1   Satement for control variable @1 at line @2   Satement for control variable @3 at line @3   Satement for control variable @3 at line @4   Satement for control variable @3   Satement for control variable @3   Satement for control variable @4   Satement for control variable &4	vee	cac	юор	initiai_value_unknown_loop_cdcve	е				
Web   Code   C									Initial value unknown at
vee ddc loop assign_stmt_not_liset_while_loop_cdove e									
Vee   cdc   loop   assign_stmt_not_last_while_loop_cdove   e   Assignment stateler & Assignment stateler & Assignment stateler & I cop at time & View   cdc   loop   undet_init_value_loop_cdove   e   Unable to determine value for loop at time & View   cdc   loop   undet_init_loop_cdove   e   Unable to determine value for loop at time & View   cdc   loop   loop_bounds_calculated_init_odove   w   Caccadated to be intered & Caccadated	vee	cdc	loop	while_loop_not_assign_stmt_controlvar_cdcve	е				
vee         dc         loop         assign_stmt_not_last_while_loop_cdove         e         Assignment statemer for control variable & Assignment statemer for control variable & Isal statement in virule for loop at line & Isal statement in line									statement for control
vee   cdc									variable @ at line @
Vec   cdc   loop   undet_init_value_loop_cdove   e   Unable to determine   value to to loop at time @ Value to the value to a constant Expression cand and value to a constant Expression cand to value to a constant expression expression expression expression expression expression expression expression expression	vee	cdc	loop	assign_stmt_not_last_while_loop_cdcve	е				Assignment statement
ve         doc         loop at line §           ve         cdc         loop         undet_limit_loop_cdcve         e         Unable to determine value for loop at line §           ve         cdc         loop         loop_bounds_calculated_int_cdcve         w         Loop bounds are actualised to be integed. In color to the loop at line §         loop bounds are actualised to be integed. In color to the loop actual line §         loop bounds are actualised to be integed. In color to the loop actual line §         loop bounds are actualised to be integed. In color to the loop actual line §         loop bounds are actualised to be integed. In color to the loop actual line §         loop bounds are actualised to be integed. In color to the loop actual line §         loop bounds are non-constant of line §         loop bounds are non-constant loop bound. Loop contregate for line §         loop bounds are non-constant loop bound. Loop contregate for line §         loop bounds.								i i	
vee   cdc   loop   undet_limit_loop_cdove   e   Unable to determine   Unable to determ									
vee         cdc         loop         underLimit_loop_cdove         e         Unable to determine Indicated at Indication of the post at the Good at the Go	vee	cdc	loop	undet_init_value_loop_cdcve	е				Unable to determine init
vee         cdc         loop         bloop_bounds_calculated_int_cdcve         w         Loop bounds are calculated to be integer. Q, check that this is calculated to the integer. Q, check that this is correct at line @ assignment contains variable bit select at line @ assignment at line	1/00	odo	loop	undet limit loop, edevo					
Vee         cdc         loop         loop_bounds_calculated_int_cdcve         w         Loop bounds are calculated to be integened accorded to be integened. In the calculated to be integened and integened accorded to be integened and integened accorded to be integened and integened accorded to the integened accorded to the integened accorded and integers accorded an	vee	cuc	ююр	under_iimir_loop_cacve	е				
vee         cdc         loop         expr_lhs_contains_var_bit_select_odove         w         Expression in list a correct at line @ stepression in list a select at line @ stepression in line a select at line @ stepression in line a select at line @ stepression is not a select manual variable initialization assignment or variable initialization are selected bound. Loop control variable initialization in line initialization in the properties of the loop control variable initialization in the loop control variable initialization are selected to a constant expression could not evaluated to a constant in line @ stepression could not evaluated to a constant in line @ stepression could not evaluate at line @ ste	vee	cdc	loop	loop_bounds_calculated_int_cdcve	w				Loop bounds are
vee         cdc         loop         expr_lhs_contains_var_bit_select_cdcve         w         Expression in lhs casingment contains variable to select at line @ sasingment contains variable initializations.           vee         cdc         loop         loop_ctrl_inil_expr_not_const_cdcve         w         non-constant contains not not contain to provide a pression is not constant Expression line @ not constant Expression l									calculated to be integer
Vee   CdC   loop   expr_lhs_contains_var_bit_select_cdcve   w   assignment contains variable bit select at language   loop_ctrl_init_expr_not_const_cdc   w   Loop bounds are non-constant at line   loop   loop_ctrl_init_expr_not_const_cdcve   w   Non-constant at line   loop   loop_ctrl_init_expr_not_const_cdcve   w   Non-constant loop   loop_ctrl_init_expr_not_const_cdcve   w   Non-constant loop   loop_ctrl_init_expr_not_const_cdcve   w   Non-constant loop   loop_ctrl_init_expr_not_const_cdcve   w   Non-constant loop   loop_ctrl_init_expr_rot_const_cdcve   w   Non-constant loop   loop_ctrl_init_expr_rot_const_cdcve   w   Non-constant loop   loop_ctrl_init_expr_reset_by_var_cdcve   e   Non-constant loop   loop_ctrl_init_expr_reset_by_var_cdcve   e   Mon-constant loop   loop_ctrl_init_expr_reset_by_var_cdcve   e   Bad_minit_expr_sion_ctrl_init_expr_sion_ctrl_init_expr_reset_by_var_cdcve   e   Mon-constant loop_ctrl_init_expr_reset_by_var_cdcve   e   Mon-constant loop_ctrl_init_expr_reset_by_var_cdcve   e   Mon-constant_expr_sion_ctrl_init_expr_reset_by_var_cdcve   e   Mon-constant_expr_sion_ctrl_init_expr_reset_by_var_cdcve   e   Mon-constant_expr_sion_ctrl_init_expr_reset_by_var_cdc									
vee         cdc         loop         loop_bounds_not_const_cdc         w         Loop bounds are non-constant at line @ loop_ctrl_init_expr_not_const_cdcve         w         Loop bounds are non-constant constructions.           vee         cdc         loop         loop_ctrl_init_expr_not_const_cdcve         w         Non-constant loop bound. Loop contru variable initialization of constant Expression is not of expression or constant loop bound. Ioop leminate Expression could not explain the properties of the properties or constant loop bound. Ioop leminate Expression could not explain the properties or constant loop bound. Ioop leminate Expression could not explain the properties or constant loop bound. Initializing Expression reset be a string. In the properties or constant loop bound. Initializing Expression reset be a string. In the properties or loop or loop_ctrl_var_1_bit_wide_cdcve         w         Non-constant loop bound. Initializing Expression reset be a string. In the properties or loop or loop_ctrl_var_1_bit_wide_cdcve         w         The loop control variable Expression reset be a string. In the properties or loop or loop_ctrl_var_1_bit_wide_cdcve         e         Bad multi-divers Net a string. In the loop control variable at line. In the loop control variable at line	vee	cdc	loop	expr_lhs_contains_var_bit_select_cdcve	w				Expression in lhs of
vee         cdc         loop         bloop_bounds are non-constant at line non-constant non-c				, – – – – –					assignment contains a
Vee   cdc   loop   loop_tornds_not_const_cdc   w     Loop bounds at at line   Vee   cdc   loop   loop_trir_init_expr_not_const_cdcve   w     Non-constant at line   Non-constant cop   Non-constant loop   Non-const									variable bit select at line
Nee   cdc   loop   loop_ctrl_init_expr_not_const_cdcve   w   Non-constant at line   more than the loop control variable initialization   Expression is not or variable initialization   Expression is not or variable initialization   Expression   Expres	vee	cdc	loop	loop bounds not const cdc	w				
bound, Loop control variable initialization   Expression is not constant Expression is not constant Expression   Express			•						non-constant at line @
vee cdc loop loop_term_expr_not_const_cdcve w loop_term_expr_not_const_cdcve w loop_term_expr_not_const_cdcve w loop_term_expr_not_const_cdcve w loop_term_expr_not_const_cdcve loop loop_term_expr_not_const_cdcve w loop_term_expr_reset_by_var_cdcve loop_term_expr_reset_by_var_c	vee	cdc	loop	loop_ctrl_init_expr_not_const_cdcve	W				Non-constant loop
Expression is not a constant Expression constant Expression could not explain the @ Non-constant loop bound. Icop terminate Expression could not evaluated to a constant loop bound. Initializing Expression reset by variable at line @ Non-constant loop bound. Initializing Expression reset by variable at line @ The loop control varia expression could not evaluated by a constant loop bound. Initializing Expression reset by variable at line @ Iso not be twide. Oh the loop control varia expression reset by variable at line @ Iso not by twide. Oh the loop control varia beclaration. At line is a more control varia by the development of the properties of the propertie									
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Vee   cdc   mdb   mdb_incompatible_net_drives_multiple_net_cdove   e     Unsupported with Signal connected to multi-driven Signal drives   Signal connected to multi-driven Signal drives   Signal connected to multi-driven Signal drives   Incompatible   Incompa									
vee cdc mdb mdb_incompatible_net_drives_multiple_net_cdove e diverses to connected to multi-driven Signal at time signal at ti	Vee	cdc	mdh	mdh unsunn comn drys sig cdcye	6				_
vee   cdc   mdb   mdb_incompatible_net_drives_multiple_net_cdove   e   mdb_incompatible_net_drives_multiple_port_cdove   e   mdb_incompatible_port_drives_multiple_port_cdove   e   mdb_incompatible_sig_drives_multiple_port_cdove   e   mdb_incompatible_sig_drives_multiple_sig_cdove   e   mdb_incompatible_sig_drives_multiple_multiple_sig_cdove   e   mdb_incompatible_drives_multiple		000		as_aeapp_cop_ae_s.g_cas-re					type driving Signal drive
vee         cdc         mbb         mdb_incompatible_net_drives_multiple_net_cdove         e         discompatible drivers driving tandem Net drives Net connected to multi-driven Net connected to multi-driven Net connected to driving tandem Port at the drives Net connected to multi-driven Port at the drives Net connected to multi-driven Port at the second of the port of the port of the multi-driven Port at the drives Net connected to Multiple advance Net Connected Net Connected Net Connected Net Connected									multi-driven Signal at lir
Vee   cdc   mdb   mdb_incompatible_port_drives_multiple_port_cdove   e   multi-driven Net at tine 6   multi-driven Port at tine 6   multi-drive Net connected to 1   multi-drive Net Net Net Net Net Net Net Net Net Ne	vee	cdc	mdb	mdb_incompatible_net_drives_multiple_net_cdcve	е				Incompatible driver
vee   cdc   mdb   mdb_incompatible_port_drives_multiple_sig_odove   e   mlc.mompatible driver Port ornected to multi-driven Port at time   formation Port at time   formation Port at time   formation Port at time   formation   format									
divining tandem Port of this port connected to multi-driven Port at the multi-driven Signal at this multi-driven Port at the multi-driven Port at	vee	cdc	mdb	mdb incompatible port drives multiple port cdcve	е				
vee   cdc   mdb   mdb_incompatible_sig_drives_multiple_sig_cdcve   e   mdb   mdb_incompatible_sig_drives_multiple_sig_cdcve   e   mdb   mdb_incompatible_sig_drives_multiple_sig_cdcve   e   mdb   mdb_incompatible_sig_drives_motion_read line   mdb_incompatible_sig_drives_motion_read_sig_drives_motion_read_sig_drives_motion_read_sig_drives_motion_read_s		000		asespase_peaesap.speesaste					driving tandem Port
vee   cdc   mdb   mdb_incompatible_sig_drives_multiple_sig_cdove   e   mdb   mdb_incompatible_sig_drives_multiple_sig_cdove   e   mdb   mdb_unsupp_LHS_concatenation_cdove   e   Ursupport_HS_concatenation_cdove   e   Ursupport_HS_concatenation_multi-drive fevice at line @ @ @ @ @ @ @ @ @ @ @ @ @ @ @ @ @ @ @									multi-driven Port at line
vee cdc mdb mdb_unsupp_LHS_concatenation_cdcve e Unsupported LHS concatenation in multi-drive Port at fail in multi-drive Port at fail in multi-drive device at fail in multi-drive sol time in multi-driven in multi-driven bet at fail in multi-driven Port at fail in multi	vee	cdc	mdb	mdb_incompatible_sig_drives_multiple_sig_cdcve	е				Incompatible driver
vee cdc mdb mdb_unsupp_LHS_concatenation_cdove e Unsupported LHS concatenation in multi-drive (active) at interest of the concatenation in multi-drive (active) and interest of the concatenation i									
vee cdc mdb mdb_bus_has_too_many_drivers_cdcve e Bus has too many drivers_at line @ will_tid-rive 'device at line @ will_tid-rive 'device at line @ will_tid-rive 'device at line @ will_tidevice of the will_tidevice of t									
vee cdc mdb mdb_bus_has_too_many_drivers_odcve e during device at line @ durivers, at line @ during durivers, at line @ during dur	vee	cdc	mdb	mdb_unsupp_LHS_concatenation_cdcve	е				
vee         cdc         mdb         mdb_bus_has_too_many_drivers_cdcve         e         Bus has too many drivers. at line @ Multiple allways blocks five name @ at line @ non-tri-state gate drives multi-driven Next at line @ non-tri-state gate drives multi-driven Next at line @ non-tri-state gate drives multi-driven Next at line @ non-tri-state gate drives multi-driven Port at line @ non-tri-state gate drives multi-driven Signal at line @ non-tri-state gate drives driven driven driven driven driven driven driven driv									multi-drive 'device at lir
vee         cdc         mdb         mdb_always_bloks_of view and early shocks of view name @ at line @ nontri_gate_drives_mdb_net_cdove         w         Multiple always_bloks_of view name @ at line @ non-tri-state gate drives_multi-driven Net at line @ non-tri-state gate drives_multi-driven Port at line @ non-tri-state gate drives_multi-driven Port at line @ non-tri-state gate drives_multi-driven Signal at	vee	cdc	mdb	mdb_bus_has_too_many_drivers_cdcve	е				Bus has too many
vee         cdc         mdb         nontri_gate_drives_mdb_net_cdcve         w         non-tri-state gate drives multi-driven Net at line @ non-tri-state gate drives multi-driven Port at line @ non-tri-state gate drives multi-driven Signal at line @ non-tri-state gate drives at line @ non-tri-state gate frives multi-driven Signal at line @ non-tri-state gate line	vee	cdc	mdb	mdb_always_blk_drive_cdcve	W				Multiple always blocks
vee         cdc         mdb         nontri_gate_drives_mdb_port_cdcve         w         non-tri-state gate drives multi-driven Port at line @ nulti-driven Port at line @ nulti-driven Port at line @ nulti-driven Signal at line @ nulti-driven Signal at line @ nulti-driven Signal at line @ nulti-driven Port at line @ nulti-driven Signal at line @ nulti-driven Port at line @ nulti-driven Port as line @ nulti-driven Port nulti-driven line @ nulti-driven Port nulti-driven Port nulti-driven Port nulti-nulti-driven Port as line @ nulti-driven Port as l	vee	cdc	mdb	nontri_gate_drives_mdb_net_cdcve	W				non-tri-state gate drive
vee   cdc   mdb   nontri_gate_drives_mdb_sig_cdcve   w   non-tri-state gate drives   multi-driven Signal at line @	vee	cdc	mdb	nontri_gate_drives_mdb_port_cdcve	W				non-tri-state gate drive
vee   cdc   mem   mem_prts_cdve   e   mem_prts_cdve   e   mem_prts_cdve   mem_prts_cdve   e   mem_prts_cdve   mifc   mifc_not_array_cdve   mem_prts_cdve   mifc_cdcd   mifc_cdcdd   mifc_cdcddd   mifc_cdcddd   mifc_cdcddd   mifc_cdcddd   mifc_cdcddd   mifc_cdcddd   mifc_cdcd									
vee   cdc   mem   mem_prts_cdve   e     Memories do not suppor part select specifier at line @ lillegal hid reference to memory (name) at line @ lillegal hid reference to memory (name) at line @ mem_ref_without_index_cdcve   e   mem   mem_ref_without_index_cdcve   e   Memory @ referenced without index through hierarchical ID @ at line @ without index through hierarchical ID @ at line @ wee   cdc   mifc   mifc_not_array_cdve   e   Port @ at line @ marray at line @ new   Port @ at line @ wee   cdc   mifc   mifc_mod_input_port_decl_as_reg_cdcve   e   Port @ at line @ wee   Module @ input port @ declared as type reg at line @ wee   cdc   mifc   mifc_mod_input_port_decl_as_reg_cdcve   e   Entity @ input port @ declared as type reg at line @ wee   cdc   mifc   mifc_unit_input_port_decl_as_reg_cdcve   e   Unit @ input port @ declared as type reg at line @ wee   cdc   mifc   mifc_unit_input_port_decl_as_reg_cdcve   e   Module @ output port re-declared as type reg at line @ wee   cdc   mifc   mod_output_wire_redecl_reg_cdcve   e   Module @ output port re-declared as type reg at line @ wee   cdc   mifc   mod_output_wire_redecl_reg_cdcve   e   Entity @ output port re-declared as type reg at line @ wee   cdc   mifc   unit_output_wire_redecl_reg_cdcve   e   Entity @ output port re-declared as type reg at line @ wee   cdc   mifc   unit_output_wire_redecl_reg_cdcve   e   Unit @ output port re-declared as type reg at line @ wee   cdc   mifc   unit_output_wire_redecl_reg_cdcve   e   Unit @ output port re-declared as type reg at line @ wee   cdc   mifc   output_port_is_mem_type_mifc_cdcve   e   Unit @ output port re-declared as type reg at line @ wee   cdc   mifc   output_port_is_mem_type_mifc_cdcve   e   unit_output_wire_redecl_reg_cdcve   lnoutport @ is memory   type at line @ wee   cdc   mifc   mod_output_port_mismatch_actual_witdh_cdcve   lnoutput_port_mismatch_actual_witdh_cdcve   lnoutput_port_wire_town   town	vee	cdc	mdb	nontri_gate_drives_mdb_sig_cdcve	W				multi-driven Signal at lir
vee         cdc         mem         illegal hid reference to memony (name) at line @ memory (name) at line @ without index through hierarchical ID @ at line @ without index through hierarchical ID @ at line @ without index through hierarchical ID @ at line @ without index through hierarchical ID @ at line @ without index through hierarchical ID @ at line @ Ports may not be an array at line @ Port @ Index @ Index @ Port @ Index @ Port @ Index @	vee	cdc	mem	mem_prts_cdve	е				Memories do not suppo
vee         cdc         mem         mem_ref_without_index_cdcve         e         Memory @ referenced without index through hierarchical ID @ at line @ without index through hierarchical ID @ at line @ Ports may not be an array at line @ array at line @ Ports may not be an array at line @ Port @ at line @ Index @ I									line @
vee         cdc         mifc         mifc_not_array_cdve         e         Ports may not be an array at line @ array at li	vee	cdc	mem	ill_ref_mem_name_cdv	е				memory (name) at line
vee         cdc         mifc         mifc_not_array_cdve         e         Ports may not be an array at line @ array at line @ Port @ at line @ Module @ input port @ declared as type reg at line @ Inou @ Inou port @ declared as type reg at line @ Inou @ Inou port @ declared as type reg at line @ Inou @ Inou port @ declared as type reg at line @ Inou @ Inou port @ declared as type reg at line @ Inou @ Inou port @ declared as type reg at line @ Inou @ Inou port @ declared as type reg at line @ Inou @ Inou port @ declared as type reg at line @ Inou port @ declared wire at line @ Inou port @ is memory type at line @ Inou port @ is memory type at line @ Inou port @ is memory type at line @ Inou port @ is memory type at line @ Inou port @ is memory type at line @ Inou port @ is memory type at line @ Inou port @ is memory type at line @ Inou port @ is memory type at line @ Inou port @ is memory type at line @ Inou port @ is memory type at line @ Inou port @ is memory type at line @ Inou port @ is memory type at line @ Inou port @ is memory type at line @ Inou port @ is memory type at line @ Inou port @ is memory type at line @ Inou port @ is memory type at line @ Inou port @ is memory type at line @ Inou port @ is memory type at line @ Inou port @ inou p	vee	cdc	mem	mem_ref_without_index_cdcve	е				
vee         cdc         mifc         mifc_not_array_cdve         e         Ports may not be an array at line @ 1 array at li									
vee         cdc         mifc         port_identifier_mifc_cdcve         e         Port @ at line @           vee         cdc         mifc         mifc_mod_input_port_decl_as_reg_cdcve         e         Module @ input port @ declared as type reg at line @           vee         cdc         mifc         mifc_entity_input_port_decl_as_reg_cdcve         e         Entity @ input port @ declared as type reg at line @           vee         cdc         mifc         mifc_unit_input_port_decl_as_reg_cdcve         e         Unit @ input port @ declared as type reg at line @           vee         cdc         mifc         mod_output_wire_redecl_reg_cdcve         e         Module @ output port re-declared as type reg at line @           vee         cdc         mifc         entity_output_wire_redecl_reg_cdcve         e         Entity @ output port re-declared wire at line @           vee         cdc         mifc         unit_output_wire_redecl_reg_cdcve         e         Unit @ output port re-declared as type reg after use as implicitly declared wire at line @           vee         cdc         mifc         unit_output_wire_redecl_reg_cdcve         e         Unit @ output port re-declared as type reg after use as implicitly declared wire at line @           vee         cdc         mifc         output_port_is_mem_type_mifc_cdcve         e         Output port @ is_memor type at line @ <t< td=""><td>vee</td><td>cdc</td><td>mifc</td><td>mifc_not_array_cdve</td><td>е</td><td></td><td></td><td></td><td>Ports may not be an</td></t<>	vee	cdc	mifc	mifc_not_array_cdve	е				Ports may not be an
vee         cdc         mifc         mifc_entity_input_port_decl_as_reg_cdcve         e         Entity @ input port @ declared as type reg at line @           vee         cdc         mifc         mifc_unit_input_port_decl_as_reg_cdcve         e         Unit @ input port @ declared as type reg at line @           vee         cdc         mifc         mod_output_wire_redecl_reg_cdcve         e         Module @ output port re-declared as type reg after use as implicitly declared wire at line @           vee         cdc         mifc         entity_output_wire_redecl_reg_cdcve         e         Entity @ output port re-declared as type reg after use as implicitly declared wire at line @           vee         cdc         mifc         unit_output_wire_redecl_reg_cdcve         e         Unit @ output port re-declared as type reg after use as implicitly declared wire at line @           vee         cdc         mifc         unit_output_wire_redecl_reg_cdcve         e         Unit @ output port re-declared as type reg after use as implicitly declared wire at line @           vee         cdc         mifc         output_port_is_mem_type_mifc_cdcve         e         Output port @ is memor type at line @           vee         cdc         mifc         mifc_inout_port_is_mem_type_cdcve         e         Inout port @ is memory type at line @           vee         cdc         mifc         mod_output_port_mismatch_actual_witdh									Port @ at line @
vee         cdc         mifc         mifc_entity_input_port_decl_as_reg_cdcve         e         Entity @ input port @ declared as type reg at line @           vee         cdc         mifc         mifc_unit_input_port_decl_as_reg_cdcve         e         Unit @ input port @ declared as type reg at line @           vee         cdc         mifc         mod_output_wire_redecl_reg_cdcve         e         Module @ output port re-declared as type reg after use as implicitly declared wire at line @           vee         cdc         mifc         entity_output_wire_redecl_reg_cdcve         e         Entity @ output port re-declared as type reg after use as implicitly declared wire at line @           vee         cdc         mifc         unit_output_wire_redecl_reg_cdcve         e         Unit @ output port re-declared as type reg after use as implicitly declared wire at line @           vee         cdc         mifc         unit_output_wire_redecl_reg_cdcve         e         Unit @ output port re-declared as type reg after use as implicitly declared wire at line @           vee         cdc         mifc         output_port_is_mem_type_mifc_cdcve         e         Output port @ is memory type at line @           vee         cdc         mifc         mifc_inout_port_is_mem_type_cdcve         e         Inout port @ is memory type at line @           vee         cdc         mifc         mod_output_port_mismatch_actual_witd	vee	cuc	IIIIC	milic_mod_input_port_deci_as_reg_cdcve	6				declared as type reg a
vee         cdc         mifc         mifc_unit_input_port_decl_as_reg_cdcve         e         Unit @ input port @ declared as type reg at line @           vee         cdc         mifc         mod_output_wire_redecl_reg_cdcve         e         Module @ output port re-declared as type reg after use as implicitly declared wire at line @           vee         cdc         mifc         entity_output_wire_redecl_reg_cdcve         e         Entity @ output port re-declared as type reg after use as implicitly declared wire at line @           vee         cdc         mifc         unit_output_wire_redecl_reg_cdcve         e         Unit @ output port re-declared as type reg after use as implicitly declared wire at line @           vee         cdc         mifc         output_port_is_mem_type_mifc_cdcve         e         Output port @ is memor type at line @           vee         cdc         mifc         mifc_inout_port_is_mem_type_cdcve         e         Inout port @ is memor type at line @           vee         cdc         mifc         mod_output_port_mismatch_actual_witdh_cdcve         w         Module @ output port @ formal to actual width mismatch at line @           vee         cdc         mifc         ent_output_port_mismatch_actual_witdh_cdcve         w         Entity @ output port @ formal to actual width	vee	cdc	mifc	mifc_entity_input_port_decl_as_reg_cdcve	е				Entity @ input port @
vee       cdc       mifc       mod_output_wire_redecl_reg_cdcve       e       Module @ output port re-declared as type reg after use as implicitly declared wire at line @         vee       cdc       mifc       entity_output_wire_redecl_reg_cdcve       e       Entity @ output port re-declared as type reg after use as implicitly declared wire at line @         vee       cdc       mifc       unit_output_wire_redecl_reg_cdcve       e       Unit @ output port re-declared as type reg after use as implicitly declared as type reg after use as implicitly declared wire at line @         vee       cdc       mifc       output_port_is_mem_type_mifc_cdcve       e       Output port @ is memor type at line @         vee       cdc       mifc       mifc_inout_port_is_mem_type_cdcve       e       Inout port @ is memory type at line @         vee       cdc       mifc       mod_output_port_mismatch_actual_witdh_cdcve       w       Module @ output port @ formal to actual width mismatch at line @         vee       cdc       mifc       ent_output_port_mismatch_actual_witdh_cdcve       w       Entity @ output port @ formal to actual width									
vee         cdc         mifc         mod_output_wire_redecl_reg_cdcve         e         Module @ output port re-declared as type reg after use as implicitly declared wire at line @ Entity @ output port re-declared as type reg after use as implicitly declared wire at line @ after use as implicitly declared wire at line @ Unit @ output port re-declared as type reg after use as implicitly declared wire at line @ Unit @ output port re-declared as type reg after use as implicitly declared wire at line @ Output port_is_mem_type_mifc_cdcve         e         Output port_is_memory type at line @ Inout port @ is memory type at line @ Inout port @ is memory type at line @         Output port @ is memory type at line @ Inout port @ is memory type at line @         Module @ output port @ is memory type at line @ Inout port @ is memory type at line @         Module @ output port @ is memory type at line @ Inout port @ is memory type at line @ In	vee	cdc	mifc	mifc_unit_input_port_decl_as_reg_cdcve	е				
re-declared as type reg after use as implicitly declared wire at line @ Entity @ output port re-declared as type reg after use as implicitly declared wire at line @ Entity @ output port re-declared as type reg after use as implicitly declared wire at line @ Unit @ output_wire_redecl_reg_cdcve e Unit @ output port @ is memory type at line @ Output port @ is memory type at line @ Unit @ output port @ is memory type at line @ Unit @ output port @ is memory type at line @ Unit @ output port @ is memory type at line @ Unit @ output port @ is memory type at line @ Unit @ output port @ is memory type at line @ Unit @ output port @ is memory type at line @ Unit @ output port @ is memory type at line @ Unit @ output port @ is memory type at line @ Unit @ output port @ is memory type at line @ Unit @ output port @ is memory type at line @ Unit @ output port @ is memory type at line @ Unit @ Output Dort @ is memory type at line @ Unit @ Output Dort @ is memory type at line @ Unit @ Ou	vee	cdc	mifc	mod output wire redect rea cacve	е				
vee cdc mifc entity_output_wire_redecl_reg_cdcve e									re-declared as type re-
re-declared as type reg after use as implicitly declared wire at line @ Unit @ output_wire_redecl_reg_cdcve e			!6-						declared wire at line @
vee       cdc       mifc       unit_output_wire_redecl_reg_cdcve       e       Unit @ output port re-declared as type reg after use as implicitly declared wire at line @ after use as implicitly declared wire at line @ output port @ is memor type at line @ output port @ is memor type at line @ output port @ is memory type at line @ output port @ is memory type at line @ output port @ is memory output port @ is memor	vee	cac	mile	entity_output_wire_redect_reg_cdcve	е				re-declared as type re-
re-declared as type reg after use as implicitly declared wire at line @ Output port_is_mem_type_mifc_cdcve e Output port @ is memor type at line @ Inout port @ is memory type at line @ Inout port @ inout									declared wire at line @
vee cdc mifc output_port_is_mem_type_mifc_cdcve e Output port @ is memor type at line @ Inout port @ is memor type at line @ Inout port @ is memory type at line @ Inout port @ ino	vee	cdc	mifc	unit_output_wire_redecl_reg_cdcve	е				
vee         cdc         mifc         output_port_is_mem_type_mifc_cdcve         e         Output port @ is memor type at line @ Inout port @ is memory type at line @           vee         cdc         mifc         mifc_inout_port_is_mem_type_cdcve         e         Inout port @ is memory type at line @           vee         cdc         mifc         mod_output_port_mismatch_actual_witdh_cdcve         w         Module @ output port @ formal to actual width mismatch at line @           vee         cdc         mifc         ent_output_port_mismatch_actual_witdh_cdcve         w         Entity @ output port @ formal to actual width									after use as implicitly declared wire at line @
vee         cdc         mifc         mifc_inout_port_is_mem_type_cdcve         e         Inout port @ is memory type at line @           vee         cdc         mifc         mod_output_port_mismatch_actual_witdh_cdcve         w         Module @ output port @ is memory type at line @           vee         cdc         mifc         ent_output_port_mismatch_actual_witdh_cdcve         w         Entity @ output port @ is memory type at line @           vee         cdc         mifc         ent_output_port_mismatch_actual_witdh_cdcve         w         Entity @ output port @ is memory type at line @	vee	cdc	mifc	output_port_is_mem_type_mifc_cdcve	е				Output port @ is memo
vee     cdc     mifc     mod_output_port_mismatch_actual_witdh_cdcve     w     Module @ output port @ formal to actual width mismatch at line @       vee     cdc     mifc     ent_output_port_mismatch_actual_witdh_cdcve     w     Entity @ output port @ formal to actual width	vee	cdc	mifc	mifc_inout_port_is_mem_type_cdcve	е				Inout port @ is memor
vee cdc mifc ent_output_port_mismatch_actual_witdh_cdcve w Entity @ output port @ formal to actual width	vee	cdc	mifc	mod_output_port_mismatch_actual_witdh_cdcve	W				Module @ output port (
formal to actual width									mismatch at line @
mismatch at line @	vee	cac	mitc	enc_output_port_mismatcn_actual_witdh_cdcve	W				formal to actual width
vee         cdc         mifc         unit_output_port_mismatch_actual_witdh_cdc         w         Unit @ output port @	vee	cdc	mifc	unit_output_port_mismatch_actual_witdh_cdc	W				

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
Out	Tilasc	турс	Name	***,_	V 1333	72001	Oy3_vci	031	formal to actual width
		.,							mismatch at line @
vee	cdc	mifc	port_name_different_in_upper_lower_case_cdcve	е					Port name @ different in upper lower case at line
									@
vee	cdc	mifc	port_not_def_in_iodecl_cdcve	е					Port @ not defined in ioDeclaration at line @
vee	cdc	mifc	port_not_def_in_portl_cdcve	е					Port @ not defined in
									port list at line @
vee	cdc	mifc	port_wiredecl_mismatch_cdcve	е					Port @ wireDeclaration mismatch at line @
vee	cdc	mifc	pos_based_null_inst_port_cdcve	е					Position based null
		'.							instance port at line @
vee	cdc	mifc	last_portdecl_contains_trailcomma_cdcve	е					Last portDeclaration contains a trailing
									comma at line @
vee	cdc	mins	mins_expr_incompatible_type_cdcve	е					Expression @ has an incompatible argument
									type @ with the port at
vee	cdc	mins	mins_mod_not_exist_cdcve	е					line @ Module @ does not exist
VCC	cuc	1111113	mins_mod_not_exist_cdcve						at line @
vee	cdc	mins	mins_entity_not_exist_cdcve	е					Entity @ does not exist
vee	cdc	mins	mins_unit_not_exist_cdcve	е					at line @ Unit @ does not exist at
									line @
vee	cdc	mins	undefined_instance_cdcve	е					Undefined instance @ at line @
vee	cdc	mod	mod_param_bad_number_cdv	е					Module name @
			•						parameter list contains
									an Incorrect number of parameter overrides at
									line @
vee	cdc	mod	mod_entity_param_bad_number_cdv	е					Entity name @ parameter list contains
									an Incorrect number of
									parameter overrides at
vee	cdc	mod	mod_unit_param_bad_number_cdv	е					line @ Unit name @ parameter
			····						list contains an Incorrect
									number of parameter overrides at line @
vee	cdc	mod	ill_mod_name_cdcve	е					Illegal module @ at line
			31 1 6						@
vee	cdc cdc	mod mod	ill_mod_entity_name_cdcve ill_mod_unit_name_cdcve	e					Illegal entity @ at line @ Illegal unit @ at line @
vee	cdc	mod	mod_mult_decl_string_cdcve	е					Multiple Declarations of
									string detected in module @ at line @
vee	cdc	mod	mod_entity_mult_decl_string_cdcve	е					Multiple Declarations of
									string detected in entity @ at line @
vee	cdc	mod	mod_unit_mult_decl_string_cdcve	е					Multiple Declarations of
									string detected in unit @
vee	cdc	mod	mod_mult_def_cdcve	е					at line @ Module @ defined in
									multiple places at line @
vee	cdc	mod	mod_ent_mult_def_cdcve	е					Entity @ defined in multiple places at line @
vee	cdc	mod	mod_unit_mult_def_cdcve	е					Unit @ defined in
			and an anadala formal adams						multiple places at line @
vee	cdc	mod	mod_no_module_found_cdcve	е					No modules found at line @
vee	cdc	mod	mod_no_entity_found_cdcve	е					No entity found at line @
vee	cdc cdc	mod mod	mod_no_unit_found_cdcve failed_find_mod_cdcve	e					No unit found at line @ Failed to find module @
vee				-					at line @
vee	cdc	mod	failed_find_entity_cdcve	е					Failed to find entity @ at
vee	cdc	mod	failed_find_unit_cdcve	е					line @ Failed to find unit @ at
									line @
vee	cdc	mod	undefined_mod_cdcve	е					Undefined module @ at line @
vee	cdc	mod	undefined_ent_cdcve	е					Undefined entity @ at
V/00	cdc	mod	undefined unit edeve	_					line @ Undefined unit @ at line
vee	cuc	mou	undefined_unit_cdcve	е					@ at line
vee	cdc	mod	unexpandable_macromodule_cdcve	е					Unexpandable
									macromodule @ at line @
vee	cdc	mod	non_interconnect_in_hierarchical_mod_cdcve	е					Non interconnect in
									hierarchical module @ at
vee	cdc	mod	non_interconnect_in_hierarchical_ent_cdcve	е					line @ Non interconnect in
									hierarchical entity @ at
vee	cdc	mod	non_interconnect_in_hierarchical_sig_cdcve	е					line @ Non interconnect in
¥00	500	mou		9					hierarchical signal @ at
V/00	cdo	med	ampty mad adaya	_					line @
vee	cdc	mod	empty_mod_cdcve	е				l	Empty module at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	cdc	mod	empty_ent_cdcve	e		12001	<b> </b>		Empty entity at line @
vee	cdc cdc	mod net	empty_unit_cdcve namereq not on LHS stmt net cdv	e					Empty unit at line @ Register @ cannot be
vee	cuc	net	namereg_not_on_Lno_sum_net_cuv						used on LHS of this assignment statement at
vee	cdc	net	net_implicit_wire_redecl_reg_cdcve	е					line @ Implicitly declared as a wire @ re-declared as a
vee	cdc	net	time_var_decl_cdcve	е					reg @. at line @ Time variable @ declared at line @
vee	cdc	net	time_var_bit_used_cdcve	е					Time variable @ bit used at line @
vee	cdc	net	undecl_net_in_mod_cdcve	е					Undeclared net @ in module @ at line @
vee	cdc	net	undecl_port_in_mod_cdcve	е					Undeclared port @ in module @ at line @
vee	cdc	net	undecl_sig_in_mod_cdcve	е					Undeclared signal @ in module @ at line @
vee	cdc	net	undecl_net_in_ent_cdcve	е					Undeclared net @ in entity @ at line @
vee	cdc	net	undecl_port_in_ent_cdcve	е					Undeclared port @ in entity @ at line @
vee	cdc	net	undecl_sig_in_ent_cdcve	е					Undeclared signal @ in entity @ at line @
vee	cdc	net	undecl_net_in_sig_cdcve	е					Undeclared net @ in signal @ at line @
vee	cdc	net	undecl_port_in_sig_cdcve	е					Undeclared port @ in signal @ at line @
vee	cdc	net	undecl_sig_in_sig_cdcve	е					Undeclared signal @ in signal @ at line @
vee	cdc	net	port_used_prior_to_decl_cdcve	е					Port @ used prior toDeclaration at line @
vee	cdc	net	1bit_with_prts_cdcve	е					1-bit with part select at line @
vee	cdc	netd	ill_decl_vec_cdcve	е					Illegal Declaration of vector @ at line @
vee	cdc	nett	nett_ill_reg_name_cdcve	е					Illegal register @ at line @
vee	cdc cdc	nett	nett_ill_net_name_cdcve nett_ill_port_name_cdcve	e e					Illegal net @ at line @ Illegal port @ at line @
vee	cdc	nett	nett_ill_signal_name_cdcve	е					Illegal signal @ at line @
vee	cdc	nett	net_scalar_vect_nett_cdcve	е					Net declared as both scalar and vector at line @
vee	cdc	nett	port_scalar_vect_nett_cdcve	е					port declared as both scalar and vector at line @
vee	cdc	nett	signal_scalar_vect_nett_cdcve	е					Signal declared as both scalar and vector at line @
vee	cdc	nett	hot_mux_not_use_bus_connection_net_cdcve	е					One hot mux can not be used for bus connection between modules Net @ at line @
vee	cdc	nett	hot_mux_not_use_bus_connection_port_cdcve	е					One hot mux can not be used for bus connection between modules Port @ at line @
vee	cdc	nett	hot_mux_not_use_bus_connection_sig_cdcve	е					One hot mux can not be used for bus connection between modules Signal @ at line @
vee	cdc	nett	reg_connected_inst_inout_cdcve	е					Reg @ connnected to instantiation @ inout @ at line @
vee	cdc	nett	ill_net_in_proc_assn_cdcve	е					Illegal net type type in procedural assignement at line @
vee	cdc	nett	ill_port_in_proc_assn_cdcve	е					Illegal port type type in procedural assignement at line @
vee	cdc	nett	ill_sig_in_proc_assn_cdcve	е					Illegal signal type type in procedural assignement at line @
vee	cdc	num	not_allowed_width0_num_cdcve	е					Width 0 not allowed for sized number at line @
vee	cdc	num	real_num_not_allowed_cdcve	е					Real numbers not allowed at line @
vee	cdc	num	found_x_z_in_num_literal_cdcve	е					Found x and/or z value in number literal at line @
vee	cdc	num	too_many_digits_in_sized_num_cdcve	w					Number of digits exceeds the width in a sized number at line @
vee	cdc cdc	num	divide_by_zero_num_cdcve child mod inst parent mod cdcve	e e					Divide by zero at line @ Child module @
vee	cuc	null	Gillia_Hou_litst_parefit_Hlou_cucve	е					instantiates parent module @ at line @
vee	cdc	num	child_ent_inst_parent_ent_cdcve	е					Child entity @ instantiates entity module

Cat	Phase	Туре	Name	W/E \	/1995   V2001   Sys_ve	
vee	cdc	num	child_sig_inst_parent_sig_cdcve	е		@ at line @ Child signal @ instantiates signal module @ at line @
vee	cdc	num	int_decl_incorrect_cdcve	е		Integer Declaration
vee	cdc	num	int_var_indexed_cdcve	е		incorrect at line @ Integer variable inedexed at line @
vee	cdc	parm	parm_redecl_as_reg_name_cdv	е		Parameter re-declared
vee	cdc	parm	parm_redecl_as_port_port_cdv	е		as reg @ at line @ Parameter re-declared
vee	cdc	parm	parm_redecl_as_net_name_cdv	е		as port @ at line @ Parameter re-declared
vee	cdc	parm	parm_redecl_as_port_name_cdv	е		as Net @ at line @ Parameter re-declared as Port @ at line @
vee	cdc	parm	parm_redecl_as_signal_name_cdv	е		Parameter re-declared as Signal @ at line @
vee	cdc	parm	duplicate_decl_parm_name_cdv	е		Duplicate declaration of parameter name @ at line @
vee	cdc	parm	ill_parm_identifier_cdcve	е		Illegal parameter @ at
vee	cdc	parm	value_of_parm_OS_platform_dependent_cdcve	W		line @ Parameter select width > 32. The value is OS and platform dependent at line @
vee	cdc	parm	parm_redefined_cdcve	w		Parameter @ redefined at line @
vee	cdc	pars	endfunction_miss_cyb_cdv	е		Endfunction missing at
vee	cdc	pars	endtask_miss_pars_cdv	е		line @ Endtask missing at line @
vee	cdc	pars	endmodule_miss_pars_cdc	е		Endmodule missing at line @
vee	cdc	pars	miss_cont_assign_pars_cdc	е		Missing = sign for continuous assignment at line @
vee	cdc	pli	user_syst_not_listed_in_pli_table_cdcve	е		User system task @ is not listed in PLI table at line @
vee	cdc	port	ill_formal_port_name_cdcve	е		Illegal formal port @ at line @
vee	cdc	pp	text_redefined_replaced_cdcve	w		Text macro redefined and replaced @. Previous definition filename, line number @ New definition filename, line number @ at line @
vee	cdc	pp	undefined_macro_cdcve	е		Undefined macro @ at line @
vee	cdc	pp	include_file_contains_nonconst_cdcve	е		Include file contains non
vee	cdc	pp	endif_or_else_without_ifdef_cdcve	е		constant @ at line @ Endif-or-else-without ifdef at line @
vee	cdc	prim	z_in_prim_inst_cdcve	е		z in primitive instantiation at line @
vee	cdc	prim	prim_instan_cdcve	е		Primitive instantiation @ at line @
vee	cdc	proc	proc_blk_missing_evc_cdcve	е		Always block missing event control at line @
vee	cdc	prts	type_prts_cdve	е		Type @ does not support part select specifier at line @
vee	cdc	prts	prts_out_of_range_cdcve	е		Parameter @[@ : @]part select is out of range at line @
vee	cdc	prts	ill_prts_inst_array_cdcve	е		Illegal value for part select of instance array
vee	cdc	prts	const_prts_contains_non_const_selector_cdcve	е		'name' at line @ Constant part select @ contains a non-constant
vee	cdc	prts	bus_index_prts_for_var_out_of_range_cdcve	е		selector @ at line @  Bus index @ integer of part select [@:@] for variable @ out of range
vee	cdc	prts	bus_prts_for_var_out_of_range_cdcve	е		at line @ Bus part select [@:@] for variable @ out of range
vee	cdc	prts	bus_prts_index_out_of_name_for_var_cdcve	е		at line @  Bus part select [@:@] index @ out of range for variable @ at line @
vee	cdc	prts	ill_token_in_prts_cdcve	е		Illegal token in part select @ at line @
vee	cdc	prts	incomplete_prts_specification_cdcve	е		Incomplete part select specification @ at line @
vee	cdc	prts	ill_index_in_prts_cdcve	е		Illegal index in part select @ at line @
vee	cdc	prts	negative_index_in_prts_not_allowed_cdcve	е		Negative index in part

Vee   odc   prts	Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
Part saled inflact coder   Part saled inflact   Part saled inflact coder   Part saled   Part sale		1 11.000	.,,,,,			11000	12001	cycc.		select @ not allowed at
Vee   Cot   Same   Infection   Same	vee	cdc	prts	prts index order reversed cdcve	е					Part select index order
Veg			μ	F107-1101-211-21-21-21-21-21-21-21-21-21-21-21-2						reversed [@ : @] [@ : @]
the size of the vector, interference of the second of the										
	vee	cdc	prts	index_vec_over_max_size_cdcve	w					Vector index @ exceeds
Vec										Index truncated at line @
Vee   Cod   Feel	vee	cdc	prts	x_or_z_in_vec_bit_select_index_cdcve	е					x or z in vector bit select
Veb   Odd   Feal	vee	cdc	real	real cdcve	е					
Veo	vee	cdc	real	real_in_assn_cdcve	е					Real @ in assignement
vee         cdc         real         real_in_comparatison_cdove         e         Real 8 in comparation at line 8           vee         cdc         real_in_comparatison_cdove         e         Illegal release object by a legal	vee	cdc	real	real_in_csi_cdcve	е					Real @ inCase item at
vee cdc simr incomplete_snst_cdove e coc snst incomplete_snst_cdove e coc sts incomplete_snst_cdove e coc st	1/00	odo	rool	roal in comparaigon adove						
vee dc simi inefficient_op_not_a_power_of_2_cdove e	vee			real_in_comparaison_cucve	6					at line @
vee         cdc         scop         Var_end_in_scope_cdove         e         Variable of redirect in scope of scop	vee	cdc	rel	ill_rel_obj_type_cdcve	е					
vee   cdc   simr   inefficient_op_not_a_power_of_2_cdove   e	vee	cdc	scop	var_erd_in_scope_cdcve	е					Variable @ redfined in
vee cdc snsl contains_inst_name_cdcve e cdc stmt lill_register_assign_cdv e lill_register_assign_cdv e lill_register_assign_cdv e lill_register_assign_cdv e lill_register_assign_cdv e lill_register_assign_cdv e lill_register_assign_redv e	vee	cdc	simr	inefficient op not a power of 2 cdcve	е					
vee odd sinir simir_multiple_init_bik_force_odove w										number not a power of 2.
vee cdc snsl incomplete_snsl_cdcve w incomplete_snsl_cdccve w incomplete_snsl_cdccve w incomplete_snsl_cdccve w incomplete_snsl_cdccve w incomplete_sn										
vee cdc snsl incomplete_snsl_cdcve w incomplete_snsl_cdcve w incomplete snsl_cdcve we cdc snsl edge_sns_process_contains_data_pin_snsl_cdcve e Edge_snssibly process contains_data_pin_snsl_cdcve e Edge_snslive process contains_data_pin_snsl_cdcve e Edge_snslive process contains_data_pin_snsl_cdcve w incomplete_snslive process contains_data_pin_snsl_cdcve e Cdc snsl unsupp_expr_in_snsl_cdcve w incomplete_snslive process contains_data_pin_snsl_cdcve w incomplete_snslive process contains_data_pin_snsl_cdcve e Cdc snsl always_bik_is_miss_snsl_cdcve e Always_bik_is_miss_snsl_cdcve e Always_bik_is_miss_snsl_cdcve e Always_bik_is_miss_snsl_cdcve e Personal District incomplete e Per	vee	cdc	simr	simr_multiple_init_blk_force_cdcve	W					
Incomplete_snsl_cdove   W										
Vee   CdC   Sinst   edge_sns_process_contains_data_pin_snst_cdcve   e	1/00	odo	onal	incomplete and adoug	147					_
vee         cdc         snsl         edge_sns_process_contains_data_pin_snsl_cdcve         e         Edge sensitive process contains a data pin @ in the sensitivity list at line @ in line	vee	cac	SHSI	incomplete_snsi_cacve	W					@ is not in the sensitivity
vee cdc snsl unsupp_expr_in_snsl_cdcve w Unsupp_expr_in_snsl_cdcve w Unsupported Expression type @ in sensitivity list at line @	VOO	cdc	enel	adda ene procese containe data nin enel cdove						
vee cdc snsl unsupp_expr_in_snsl_cdcve w Unsupp_expr_in_snsl_cdcve ve cdc snsl always_blk_is_miss_snsl_cdcve e Always_blck is_miss_snsl_cdcve e Always_blck is_miss_snsl_cdcve e Always_blck_is_miss_snsl_cdcve e P?  vee cdc snsl not_all_bits_snsvar_used_cdc e P?  vee cdc snsl partial bus_decl_width_cdcve e P?  partial bus_declared in process at line @ Sused in process at line @ Always_blck_is_miss_snsl_miss_snsl_cdcve e P.  cdc snsl contains_inst_name_cdcve e Contains_inst_name_cdcve e Bus_@ intereated with width @ w	VCC	cuc	31131	euge_sns_process_contains_uata_pm_snsi_cucve						contains a data pin @ in
Vee   CdC   SnSl										
ve cdc snsl always_bik_is_miss_snsl_cdove e	vee	cdc	snsl	unsupp_expr_in_snsl_cdcve	w					Unsupported Expression
vee         cdc         snsl         always_blk_is_miss_snsl_cdove         e         Always block is missing sensitury list at line general sensitury list at line general sensitury list at line general sensitury variable gar au used in process at line (and the partial bus general sensitury) variable gar au used in process at line (and partial bus general sensitury) variable gar au used in process at line (and partial bus general sensitury) variable gar au used in process at line (and partial bus general sensitury) variable gar au used in process at line (and partial bus general sensitury) variable gar au used in process at line (and partial bus general sensitury) variable gar au used in process at line (and partial bus general sensitury) variable gar au used in process at line (and partial bus general sensitury) in the partial bus general sensitury list at line (and partial bus general sensity) is at line (and partial bus general										
vee         cdc         snsl         not_all_bits_snsvar_used_cdc         e         snstitity variable @a used in process at line @ sensitivity variable @a used in process at line @ partial bus @ declared with width @a width W	vee	cdc	snsl	always_blk_is_miss_snsl_cdcve	е					Always block is missing
vee   cdc   snsl   partial_bus_decl_width_cdcve   e   ?   partial_bus @ declared with width @ width width @ wi	vee	cdc	snsl	not_all_bits_snsvar_used_cdc	е					
vee         cdc         snsl         partial_bus_decl_width_cdcve         e         ?           vee         cdc         snsl         contains_inst_name_cdcve         e         Contains instance name at line @           vee         cdc         snsl         bus_indexed_in_snsl_cdcve         e         Bus @ indexed in sensitivity list at line @           vee         cdc         stmt         iil_register_assign_cdv         e         Bus @ indexed in sensitivity list at line @           vee         cdc         stmt         iil_register_assign_cdv         e         Null statement is not allowed here at line @           vee         cdc         stmt         null_not_allowed_stmt_cdcve         e         Null statement is not allowed here at line @           vee         cdc         stmt         id_expected_FHSexpr_force_stmt_cdcve         e         Simple identifier expected for LHS Expression in force-statement at line @           vee         cdc         stmt         id_expected_FHSexpr_ferce_stmt_cdcve         e         Illegal type @ can only accept instruction in release-statement at line @           vee         cdc         stmt         stmt_iil_accept_only_not_reg_mem_cdcve         e         Illegal type @ can only accept instruction in release-statement at line @           vee         cdc         stmt         stmt_iil_accept_only_signal_re										sensitivity variable @ are
vee   cdc   snsl   contains_inst_name_cdcve   e     Contains instance name	vee	cdc	snsl	partial_bus_decl_width_cdcve	е	?				partial bus @ declared
vee         cdc         snsl         contains_inst_name_cdcve         e         Contains_instance name @ at tine @           vee         cdc         snsl         bus_indexed_in_snsl_cdcve         e         Bus @ indexed in @ at tine @           vee         cdc         stmt         iil_register_assign_cdv         e         Illegal register assignment statement a line @           vee         cdc         stmt         null_not_allowed_stmt_cdcve         e         Null statement is not allowed here at line @           vee         cdc         stmt         id_expected_FHSexpr_force_stmt_cdcve         e         Simple identifier expected for LHS Expression in force-statement at line @           vee         cdc         stmt         id_expected_FHSexpr_release_stmt_cdcve         e         Simple identifier expected for LHS Expression in force-statement at line @           vee         cdc         stmt         stmt_iil_accept_only_net_reg_mem_cdcve         e         Illegal type @ can only accept net_reg, memory at line @           vee         cdc         stmt         stmt_iil_accept_only_port_reg_mem_cdcve         e         Illegal type @ can only accept net_reg, memory at line @           vee         cdc         stmt         while_stmt_usage_disc_cdcve         w         Willestatement as line @           vee         cdc         stmt         whil										
vee         cdc         snsl         bus_indexed_in_snsl_cdcve         e         Bus @ indexed in sensitivity list at line @ lilegal register assignment statement a sign ment statement a sign ment statement a sign ment statement a sign ment statement a line @           vee         cdc         stmt         null_not_allowed_stmt_cdcve         e         Null statement is not allowed here at line @ sexpected for LHS Expression in force-statement at line @           vee         cdc         stmt         id_expected_FHSexpr_release_stmt_cdcve         e         Simple identifier expected for LHS Expression in release-statement at line @           vee         cdc         stmt         stmt_ill_accept_only_net_reg_mem_cdcve         e         Illegal type @ can only accept net, reg, memon at line @           vee         cdc         stmt         stmt_ill_accept_only_port_reg_mem_cdcve         e         Illegal type @ can only accept net, reg, memon at line @           vee         cdc         stmt         stmt_ill_accept_only_signal_reg_mem_cdcve         e         Illegal type @ can only accept port, reg, memon at line @           vee         cdc         stmt         while_stmt_usage_disc_cdcve         w         Whilesstatement usage discouraged at line @           vee         cdc         stmt         arithmetic_op_rhs_one_less_bit_than_lhs_cdcve         e         Arithmetic operator nthe lane @           vee         cdc <t< td=""><td>vee</td><td>cdc</td><td>snsl</td><td>contains_inst_name_cdcve</td><td>е</td><td></td><td></td><td></td><td></td><td>Contains instance name</td></t<>	vee	cdc	snsl	contains_inst_name_cdcve	е					Contains instance name
vee         cdc         stmt         ill_register_assign_cdv         e         lllegal register assignment statement a sing ment statement a line @           vee         cdc         stmt         null_not_allowed_stmt_cdove         e         Null statement is not allowed here at line @           vee         cdc         stmt         id_expected_FHSexpr_force_stmt_cdove         e         Simple identifier expected for LHS Expression in force-statement at line @           vee         cdc         stmt         id_expected_FHSexpr_release_stmt_odove         e         Simple identifier expected for LHS Expression in force-statement at line @           vee         cdc         stmt         stmt_ill_accept_only_net_reg_mem_cdove         e         lllegal type @ can only accept net, reg, memor at line @           vee         cdc         stmt         stmt_ill_accept_only_signal_reg_mem_cdove         e         lllegal type @ can only accept port, reg, memor at line @           vee         cdc         stmt         stmt_ill_accept_only_signal_reg_mem_cdove         e         lllegal type @ can only accept signal, reg, memory at line @           vee         cdc         stmt         while_statement usage disc_cdove         w         While statement usage discouraged at line @           vee         cdc         stmt         arithmetic_operator RRS has one less bit than the LHS at line @         Arithmetic operator un	vee	cdc	snsl	bus indexed in spsl cdcve	е					
vee       cdc       stmt       null_not_allowed_stmt_cdcve       e       Null statement is not allowed here at line @         vee       cdc       stmt       id_expected_FHSexpr_force_stmt_cdcve       e       Simple identifier expected for LHS Expression in force-statement at line @         vee       cdc       stmt       id_expected_FHSexpr_release_stmt_cdcve       e       Simple identifier expected for LHS Expression in force-statement at line @         vee       cdc       stmt       stmt_ill_accept_only_net_reg_mem_cdcve       e       Illegal type @ can only accept net, reg, memon at line @         vee       cdc       stmt       stmt_ill_accept_only_port_reg_mem_cdcve       e       Illegal type @ can only accept port, reg, memon at line @         vee       cdc       stmt       stmt_ill_accept_only_signal_reg_mem_cdcve       e       Illegal type @ can only accept signal, reg, memon at line @         vee       cdc       stmt       while_stmt_usage_disc_cdcve       w       While statement usage discouraged at line @         vee       cdc       stmt       arithmetic_op_rhs_one_less_bit_than_lhs_cdcve       e       Arithmetic operator RHS has one less bit than the LHS at line @         vee       cdc       stmt       ar_op_unequal_var_on_rhs_cdc       e       Arithmetic operator cunequal width variables @ on RHS at line @         vee       cdc										sensitivity list at line @
vee         cdc         stmt         null_not_allowed_stmt_cdcve         e         Null statement is not allowed here at line @ Simple identifier expected for LHS Expression in force-statement at line @ Simple identifier expected for LHS Expression in force-statement at line @ Simple identifier expected for LHS Expression in release-statement at line @ stmt_ill_accept_only_net_reg_mem_cdcve         e         Simple identifier expected for LHS Expression in release-statement at line @ stmt_ill_accept_only_net_reg_mem_cdcve         e         Illegal type @ can only accept net, reg, memory at line @ stmt_ill_accept_only_port_reg_mem_cdcve         e         Illegal type @ can only accept net, reg, memory at line @ scept port, reg, memory at line @ scept signal, reg,	vee	cac	stmt	iii_register_assign_cdv	е					assignment statement at
vee       cdc       stmt       id_expected_FHSexpr_force_stmt_cdcve       e       Simple identifier expected for LHS Expression in force-statement at line @ Simple identifier expected for LHS Expression in release-statement at line @ Simple identifier expected for LHS Expression in release-statement at line @ Simple identifier expected for LHS Expression in release-statement at line @ Illegal type @ can only accept net, reg, memory at line @ Illegal type @ c	1/00	odo	otmt	null not allowed atmt adays						
vee cdc stmt stmt_iil_accept_only_net_reg_mem_cdcve e cdc stmt stmt_iil_accept_only_net_reg_mem_cdcve e cdc stmt stmt_iil_accept_only_signal_reg_mem_cdcve e cdc stmt arithmetic_op_rhs_one_less_bit_than_lhs_cdcve e cdc stmt arithmetic_op_rhs_one_less_bit_than_lhs_cdcve e cdc stmt arithmetic_op_rhs_one_less_bit_than_lhs_cdcve e cdc stmt ar_op_unequal_lhs_rhs_cdcve e cdc stmt ar_op_unequal_var_on_rhs_cdc e cdc stmt ar_op_unequal_var_on_rhs_cdc e stmt ar_op_unequal_var_on_rhs_cdc e cdc stmt empty_stmt_cdc e stmt empty_stmt_cdc e stmt empty_stmt_cdc e stmt empty_stmt_cdc e legal system task @ Argument @ at line @ Argument	vee		Sum		е					allowed here at line @
Expression in force-statement at line @ Simple identifier expected for LHS Expression in release-statement at line @ Simple identifier expected for LHS Expression in release-statement at line @ Illegal type @ can only accept net, reg, memory at line @ Illegal type @ can only accept net, reg, memory at line @ Illegal type @ can only accept net, reg, memory at line @ Illegal type @ can only accept port, reg, memory at line @ Illegal type @ can only accept port, reg, memory at line @ Illegal type @ can only accept port, reg, memory at line @ Illegal type @ can only accept signal, reg, memory at line @ While statement usage discouraged at line @ While statement usage discouraged at line @ Arithmetic operator RHS at line @ Arithmetic operator RHS at line @ Arithmetic operator unequal width LHS and RHS at line @ Arithmetic operator unequal width variables @ on RHS at line @ Arithmetic operator unequal width variables @ on RHS at line @ Arithmetic operator unequal width variables @ on RHS at line @ Arithmetic operator unequal width variables @ on RHS at line @ Arithmetic operator unequal width variables @ on RHS at line @ Arithmetic operator unequal width variables @ on RHS at line @ Arithmetic operator unequal width variables @ on RHS at line @ Arithmetic operator unequal width variables @ on RHS at line @ On RHS a	vee	cdc	stmt	id_expected_FHSexpr_force_stmt_cdcve	е					
vee         cdc         stmt         id_expected_FHSexpr_release_stmt_cdcve         e         Simple identifier expected for LHS Expression in release-statement at line @           vee         cdc         stmt         stmt_ill_accept_only_net_reg_mem_cdcve         e         Illegal type @ can only accept net, reg, memory at line @           vee         cdc         stmt         stmt_ill_accept_only_port_reg_mem_cdcve         e         Illegal type @ can only accept signal, reg, memory at line @           vee         cdc         stmt         while_stmt_usage_disc_cdcve         w         While statement usage discouraged at line @           vee         cdc         stmt         arithmetic_op_rhs_one_less_bit_than_lhs_cdcve         e         Arithmetic operator RHS has one less bit than the LHS at line @           vee         cdc         stmt         ar_op_unequal_lhs_rhs_cdcve         e         Arithmetic operator unequal width LHS and RHS at line @           vee         cdc         stmt         ar_op_unequal_var_on_rhs_cdc         e         Arithmetic operator unequal width variables @ on RHS at line @           vee         cdc         stmt         empty_statement at line @         Empty_statement at line @           vee         cdc         stmt         empty_statement at line @         Empty_statement at line @										Expression in
expected for LHS Expression in release-statement at line  vee cdc stmt stmt_ill_accept_only_net_reg_mem_cdcve e  cdc stmt stmt_ill_accept_only_port_reg_mem_cdcve e  cdc stmt stmt_ill_accept_only_port_reg_mem_cdcve e  cdc stmt stmt_ill_accept_only_signal_reg_mem_cdcve e  cdc stmt stmt_ill_accept_only_signal_reg_mem_cdcve e  cdc stmt while_stmt_usage_disc_cdcve w  vee cdc stmt while_stmt_usage_disc_cdcve w  vee cdc stmt arithmetic_op_rhs_one_less_bit_than_lhs_cdcve e  cdc stmt arithmetic_op_rhs_one_less_bit_than_lhs_cdcve e  cdc stmt ar_op_unequal_lhs_rhs_cdcve e  Arithmetic operator RHS has one less bit than the LHS at line @  vee cdc stmt ar_op_unequal_var_on_rhs_cdc e  Arithmetic_operator unequal width LHS and RHS at line @  vee cdc stmt ar_op_unequal_var_on_rhs_cdc e  Empty-statement at line @  vee cdc stmt empty_stmt_cdc e  Empty-statement at line @  vee cdc stmt empty_stmt_cdc e  Illegal type @ can only accept port, reg, memory at line e  e  accept sqn reg, memory at line e  Arithmetic operator unequal width LHS and RHS at line @  on RHS at line @  vee cdc stmt empty_stmt_cdc e  Empty-statement at line @  vee cdc syst ill_syst_task_arg_cdcve e  Illegal system task @  Argument @ at line @  Illegal system task @  Argument @ at line @  Illegal system task @  Argument @ at line @	vee	cdc	stmt	id expected FHSexpr release stmt cdcve	е					
release-statement at line @ lillegal type @ can only accept net, reg, memory at line @ lillegal type @ can only accept net, reg, memory at line @ lillegal type @ can only accept net, reg, memory at line @ lillegal type @ can only accept port, reg, memory at line @ lillegal type @ can only accept port, reg, memory at line @ lillegal type @ can only accept signal, reg, memory at line @ lillegal type @ can only accept signal, reg, memory at line @ lillegal type @ can only accept signal, reg, memory at line @ lillegal type @ can only accept signal, reg, memory at line @ lillegal type @ can only accept signal, reg, memory at line @ lillegal type @ can only accept signal, reg, memory at line @ lillegal type @ can only accept signal, reg, memory at line @ lillegal type @ can only accept signal, reg, memory at line @ lillegal type @ can only accept port, reg, memory at line @ lillegal type @ can only		000	0	та_өлрөөтөа_т т. <b>с</b> өлрт_төгөөөө_өтт_өөөтө						expected for LHS
vee         cdc         stmt         stmt_ill_accept_only_net_reg_mem_cdcve         e         Illegal type @ can only accept net, reg, memory at line @           vee         cdc         stmt         stmt_ill_accept_only_port_reg_mem_cdcve         e         Illegal type @ can only accept port, reg, memory at line @           vee         cdc         stmt         stmt_ill_accept_only_signal_reg_mem_cdcve         e         Illegal type @ can only accept port, reg, memory at line @           vee         cdc         stmt         while_stmt_usage_disc_cdcve         w         While statement usage discouraged at line @           vee         cdc         stmt         arithmetic_op_rhs_one_less_bit_than_lhs_cdcve         e         Arithmetic operator RHS has one less bit than the LHS at line @           vee         cdc         stmt         ar_op_unequal_lhs_rhs_cdcve         e         Arithmetic operator unequal width LHS and RHS at line @           vee         cdc         stmt         ar_op_unequal_var_on_rhs_cdc         e         Arithmetic operator unequal width variables @ on RHS at line @           vee         cdc         stmt         empty_statement at line @         e         Empty-statement at line @           vee         cdc         stmt         empty_state, eq, memory at line @         e         Empty-statement at line @										release-statement at line
vee       cdc       stmt       stmt_ill_accept_only_port_reg_mem_cdcve       e       Illegal type @ can only accept port, reg, memor at line @         vee       cdc       stmt       stmt_ill_accept_only_signal_reg_mem_cdcve       e       Illegal type @ can only accept signal, reg, memory at line @         vee       cdc       stmt       while_stmt_usage_disc_cdcve       w       While statement usage discouraged at line @         vee       cdc       stmt       arithmetic_op_rhs_one_less_bit_than_lhs_cdcve       e       Arithmetic operator RHS has one less bit than the LHS at line @         vee       cdc       stmt       ar_op_unequal_lhs_rhs_cdcve       e       Arithmetic operator unequal width LHS and RHS at line @         vee       cdc       stmt       ar_op_unequal_var_on_rhs_cdc       e       Arithmetic operator unequal width variables @ on RHS at line @         vee       cdc       stmt       empty_statement at line @       e       Empty-statement at line @         vee       cdc       syst       ill_syst_task_arg_cdcve       e       Illegal system task @ Argument @ at line @	1/00	odo	otmt	atmt ill accept only not rea mem adays						
vee         cdc         stmt         stmt_ill_accept_only_port_reg_mem_cdcve         e         Illegal type @ can only accept port, reg, memor at line @           vee         cdc         stmt         stmt_ill_accept_only_signal_reg_mem_cdcve         e         Illegal type @ can only accept signal, reg, memory at line @           vee         cdc         stmt         while_stmt_usage_disc_cdcve         w         While statement usage discouraged at line @           vee         cdc         stmt         arithmetic_op_rhs_one_less_bit_than_lhs_cdcve         e         Arithmetic operator RHS has one less bit than the LHS at line @           vee         cdc         stmt         ar_op_unequal_lhs_rhs_cdcve         e         Arithmetic operator unequal width LHS and RHS at line @           vee         cdc         stmt         ar_op_unequal_var_on_rhs_cdc         e         Arithmetic operator unequal width variables @ on RHS at line @           vee         cdc         stmt         empty_stmt_cdc         e         Empty-statement at line @           vee         cdc         stmt         empty_state_arg_cdcve         e         Illegal system task @           vee         cdc         syst         ill_syst_task_arg_cdcve         e         Argument @ at line @	vee	cac	Simi	stmt_iii_accept_only_net_reg_mem_cacve	е					accept net, reg, memory
vee       cdc       stmt       stmt_ill_accept_only_signal_reg_mem_cdcve       e       Illegal type @ can only accept signal, reg, memory at line @ while_stmt_usage_disc_cdcve         vee       cdc       stmt       while_stmt_usage_disc_cdcve       w       While statement usage discouraged at line @ while_stmt_usage_discouraged at line @ Arithmetic operator RHS has one less bit than the LHS at line @ Arithmetic operator runequal width LHS and RHS at line @ Arithmetic operator unequal width LHS and RHS at line @ Arithmetic operator unequal width variables @ on RHS at line @ Arithmetic operator unequal width variables @ on RHS at line @ Empty-statement at line @ are cdc         vee       cdc       stmt       empty_stmt_cdc       e       Empty-statement at line @ are cdc         vee       cdc       stmt       empty_statesk_arg_cdcve       e       Illegal system task @ Argument @ at line	VAA	cdc	stmt	stmt ill accent only nort reg mem cdcve	Δ.					
vee         cdc         stmt         stmt_ill_accept_only_signal_reg_mem_cdcve         e         Illegal type @ can only accept signal, reg, memory at line @ memory at line @ while statement usage discouraged at line @ discouraged at line @ discouraged at line @ Arithmetic_op_rhs_one_less_bit_than_lhs_cdcve         w         Arithmetic operator RHS has one less bit than the LHS at line @ Arithmetic operator unequal width LHS and RHS at line @ Arithmetic operator unequal width LHS and RHS at line @ Arithmetic operator unequal width variables @ on RHS at line @ on RHS at line @ encylear at line @ on RHS at line @ and RHS a	VCC	cuc	Sum	stini_iii_accept_oniy_port_reg_mem_cacve						accept port, reg, memory
vee       cdc       stmt       while_stmt_usage_disc_cdcve       w       While statement usage discouraged at line @ Arithmetic operator RHS has one less bit than the LHS at line @ Arithmetic operator unequal width LHS and RHS at line @ Arithmetic operator unequal width LHS and RHS at line @ Arithmetic operator unequal width LHS and RHS at line @ Arithmetic operator unequal width variables @ on RHS at line @ Empty-statement at line @ Use Cdc         vee       cdc       stmt       empty_stmt_cdc       e       Empty-statement at line @ Use Cdc         vee       cdc       stmt       empty_statement at line @ Use Cdc       e       Illegal system task @ Argument @ at line @ Argument @ a	Vee	cdc	stmt	stmt ill accent only signal reg mem cdcye	6					
vee         cdc         stmt         while_stmt_usage_disc_cdcve         w         While statement usage discouraged at line @ discouraged at line @ Arithmetic operator RM has one less bit than the LHS at line @ Arithmetic operator runequal width LHS and RMS at line @ Arithmetic operator unequal width LHS and RMS at line @ Arithmetic operator unequal width variables @ on RMS at line @ On RMS at line @ Arithmetic operator unequal width variables @ on RMS at line @ Empty-statement at line @ Wee cdc         stmt         empty_stmt_cdc         e         Empty-statement at line @ Argument @ at line @	100	000	Othit	o.mm_accopt_cmy_o.gnat_reg_mem_cacve						accept signal, reg,
vee       cdc       stmt       arithmetic_op_rhs_one_less_bit_than_lhs_cdcve       e       Arithmetic operator RHS has one less bit than than one lest bit than than one less bit than than one less bit than than one less bi	vee	cdc	stmt	while stmt usage disc cdcve	W					
vee     cdc     stmt     ar_op_unequal_lhs_rhs_cdcve     e     Arithmetic operator unequal width LHS and RHS at line @       vee     cdc     stmt     ar_op_unequal_var_on_rhs_cdc     e     Arithmetic operator unequal width variables @ on RHS at line @       vee     cdc     stmt     empty_stmt_cdc     e     Empty-statement at line @       vee     cdc     syst     ill_syst_task_arg_cdcve     e     Illegal system task @ Argument @ at line @										discouraged at line @
vee     cdc     stmt     ar_op_unequal_lhs_rhs_cdcve     e     Arithmetic operator unequal width LHS and RHS at line @       vee     cdc     stmt     ar_op_unequal_var_on_rhs_cdc     e     Arithmetic operator unequal width variables @ on RHS at line @       vee     cdc     stmt     empty_stmt_cdc     e     Empty-statement at line @       vee     cdc     syst     ill_syst_task_arg_cdcve     e     Illegal system task @       Argument @ at line @	vee	cac	smt	andmetic_op_ms_one_less_bit_than_ins_cdcve	е					has one less bit than the
vee     cdc     stmt     ar_op_unequal_var_on_rhs_cdc     e     Arithmetic operator unequal width variables @ on RHS at line @       vee     cdc     stmt     empty_stmt_cdc     e     Empty-statement at line @       vee     cdc     syst     ill_syst_task_arg_cdcve     e     Illegal system task @       Argument @ at line @	VAA	cdc	stmt	ar on unequal the the edoug	6					
vee     cdc     stmt     ar_op_unequal_var_on_rhs_cdc     e     Arithmetic operator unequal width variables @ on RHS at line @       vee     cdc     stmt     empty_stmt_cdc     e     Empty-statement at line @       vee     cdc     syst     ill_syst_task_arg_cdcve     e     Illegal system task @ Argument @ at line @	vee	cuc	ount	ar_op_uriequar_iris_tris_cucve	6					unequal width LHS and
vee     cdc     stmt     empty_stmt_cdc     e     Empty-statement at line @       vee     cdc     syst     ill_syst_task_arg_cdcve     e     Illegal system task @       Argument @ at line @	VAA	cdc	stmt	ar on linearial var on the ede	6					
vee     cdc     stmt     empty_stmt_cdc     e     Empty-statement at line @       vee     cdc     syst     ill_syst_task_arg_cdcve     e     Illegal system task @       Argument @ at line @	,,,,	500	Carit	ai_op_ailoquai_vai_oii_iiib_ouo						unequal width variables
vee cdc syst ill_syst_task_arg_cdcve e Illegal system task @ Argument @ at line @	vee	cdc	stmt	emptv stmt cdc	е					
Argument @ at line @				. ,						@
	vee	cac	syst	iii_syst_task_arg_cdcve	е					
	vee	cdc	syst	csdir_converts_syts_cdcve	W				Х	Lower case converts the

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
-		.,,,,,				12001	<b>- - - - - - - - - -</b>		system task \$realtime
									return value to an integer at line @
vee	cdc	syst	return_var_of_user_used_as_rhs_cdcve	W					Return variable of user
		,							system task is used as a
vee	cdc	task	miss_task_name_stmst_body_cdv	е					RHS variable at line @ Task @ body statement
****		taok		Ŭ					missing at line @
vee	cdc cdc	task task	ill_task_cdv ill_use_task_cdcve	e					Illegal task @ at line @ Illegal use of task @ at
vee	cuc	lask	III_use_task_cucve	6					line @
vee	cdc	task	ask_var_not_decl_cdcve	е					Variable @ used but not
vee	cdc	task	task not defined cdcve	е					declared at line @ Task @ not defined at
									line @
vee	cdc	task	too_few_arg_to_task_cdcve	е					Too few arguments passed to task @ at line
									@
vee	cdc	task	undefined_task_cdcve	е					Undefined task @ at line @
vee	cdc	task	syts_output_port_drvs_nonsqs_logic_comp_cdcve	W					User system task output
			, - , , - 3 - , -						port drives
									non-sequential logic component at line @
vee	cdc	task	undefioned_task_	е					Undefined task @ at line
vee	cdc	task	task_decl_error_vhve	е					@ Task declaration error at
VCC	cuc	lask	task_deci_entil_viive	6					line @
vee	cdc	task	func_task_parm_cdcve	е					Found function
vee	cdc	task	unmatched task param cdcve	е					parameter @ at line @ Unmatched task
			Ī						parameter @ at line @
vee	cdc cdc	tbcd tbcd	found_forever_tbcd_cdcve behavioral_code_mod_cdcve	e					Found forever at line @ Behavioral code in
VCC	ouc	ibca	benavioral_code_mod_cdeve						module @ at line @
vee	cdc	tbcd	behavioral_code_ent_cdcve	е					Behavioral code in entity
vee	cdc	tbcd	behavioral_code_unit_cdcve	е					@ at line @ Behavioral code in unit
									@ at line @
vee	cdc	tri	instance_not_tri_state_device_cdcve	е					Instance name is not a tri-state device at line @
vee	cdc	tri	unsupp_gate_type_tristate_cdcve	е					Unsupported gate type
									@ used for tristate at line @
vee	cdc	tri	tri_not_desgn_gate_contention_cdcve	е					Tristate not designed
									correctly gate @ can cause contention at line
									@
vee	cdc	tri	unsupp_type_instance_tri_cdcve	е					Unsupported type
									instance type used for tristate @ at line @
vee	cdc	tri	incorrect_cont_assign_stmt_tri_gate_cdcve	е					Incorrect continuous
									assign statement for tristate gate @ at line @
vee	cdc	tri	const_assign_to_multidriven_net_cdcve	е					Constant (constiznt)
									assigned to multi-driven Net @ at line @
vee	cdc	tri	const_assign_to_multidriven_port_cdcve	е					Constant (constiznt)
									assigned to multi-driven
vee	cdc	tri	const_assign_to_multidriven_signal_cdcve	е					Port @ at line @ Constant (constiznt)
									assigned to multi-driven
vee	cdc	tri	unsupp_expr_for_tri_cdcve	е					Signal @ at line @ Unsupported Expression
100	ouo		unoupp_0xp1_101_u1_0u010						type @ for tristate at line
vee	cdc	unov	cs equality op cdcve						@ Case equality operator
vee	cuc	unsy	cs_equality_op_cdcve	е					== at line @
vee	cdc	unsy	deassign_stmt_cdcve	е					Deassign statement at
vee	cdc	unsy	defparam_cdcve	е					line @ Defparam at line @
vee	cdc	unsy	dely_ctrl_cdcve	е					Delay control at line @
vee	cdc cdc	unsy	ev_ctrl_cdcve time_decl_cdcve	e e					Event control at line @ Time Declaration at line
V06		,			L			L	@
vee	cdc	unsy	wait_stmt_unsy_cdcve	е					Wait statement at line @
vee	csa	assn	unequal_length_lhs_rhs_csve	е					Unequal length LHS and RHS at line @
vee	csa	assn	unequal_length_lhs_rhs_off_one_bit_csve	е					Unequal length LHS and
									RHS off by one bit at line @
vee	csa	blk	repeat_in_nonblk_assn_csve	е					Repeat in non-blocking
1/00	000	blk	empty blk eave	_					assignment at line @ Empty-block at line @
vee	csa	clk	empty_blk_csve unsupp_logic_operation_csve	e w					Unsupported logic
			5 3						operation type @. at line
vee	csa	clk	unsupp_cl_gated_logic_csve	W					@ Unsupported gated clock
			5 - 5 -						logic type. at line @
vee	csa	clk	unsupp_logic_expr_clk_csve	W					Unsupported

Cat	Phase	Туре	Name	W/F	V1995	V2001	Sys_ver	Csl Desc
Out	Tilasc	Type	Nume	***	V 1333	12001	Oy3_VCI	logicExpression type @
vee	csa	csi	duplicate_csi_csve	е				at line @ Duplicate Case item @ at line @
vee	csa	csi	case_sel_contains_real_num_const_csve	е				Case selector contains a constant real number at line @
vee	csa	csi	csi_contains_real_num_const_csve	е				Case item contains a constant real number at
vee	csa	csi	real_in_csi_csve	е				line @  Real @ in case item at line @
vee	csa	csi	noncnst_in_iclude_file_csve	е				Non-constant in include
vee	csa	csi	csi_width_mismatch_csve	е				file @ at line @  Case item @ width
vee	csa	csi	efault_missing_csve	е				mismatch at line @ Default missing at line @
vee	csa	CSS	not_all_csi_specified_csve	е				Not allCase items are specified @ at line @
vee	csa	defd	mod_def_within_mod_not_in_include_csde	е				Module define within module but not in include
vee	csa	defd	ent_def_within_ent_not_in_include_csde	е				at line @ Entity define within entity but not in include at line @
vee	csa	defd	unit_def_within_unit_not_in_include_csde	е				Unit define within unit but not in include at line @
vee	csa	dely	comb_blk_contains_dely_assn_csve	е				Combinational block contains delay
vee	csa	dely	seq_blk_contains_dely_assn_csde	е				assignement at line @ Sequential block contains delay
vee	csa	dely	comb_blk_dely_between_stms_csve	е				assignement at line @ Combinational block contains delay between statements at line @
vee	csa	dely	seq_blk_dely_between_stmt_csve	е				Sequential block contains delay between
vee	csa	dely	dely_in_nonblk_assn_comb_cscve	е				statements at line @ Delay in nonblocking assignement in
vee	csa	dely	dely_in_nonblk_assn_seq_csve	е				combinational at line @ Delay in nonblocking assignement in
vee	csa	drst	drvs_not_in_lib_csve	е				sequential at line @ Drive strength @ not in
vee	csa	drvc	output_arg_appers_rhs_csve	w				library at line @ Output argument @ of user system task
								appears in RHS and is driven elsewhere at line
vee	csa	drvc	multiple_init_blk_drvc_csve	W				Multiple initial blocks force 'narne' at line @
vee	csa	drvc	net_multiple_always_blk_csve	w				Net @ multiple always blocks at line @
vee	csa	drvc	port_multiple_always_blk_csve	W				Port @ multiple always blocks at line @
vee	csa	drvc	sig_multiple_always_blk_csve	W				Signal @ multiple always blocks at line @
vee	csa	drvc	net_multiple_stmt_csve	w				Net @ multiple statements with in the
vee	csa	drvc	port_multiple_stmt_csve	w				same always at line @ Port @ multiple statements with in the
vee	csa	drvc	sig_multiple_stmt_csve	W				same always at line @ Signal @ multiple statements with in the
								same always at line @
vee	csa	drvc	multiply_drvn_net_nontri_gate_csve	W				Multiply drivenNet driven by a non-tristate gate at line @
vee	csa	drvc	multiply_drvn_port_nontri_gate_csve	W				Multiply drivenPort driven by a non-tristate gate at line @
vee	csa	drvc	multiply_drvn_sig_nontri_gate_csve	W				Multiply drivenSignal driven by a non-tristate gate at line @
vee	csa	drvc	incompatible_driver_net_csve	w				Incompatible driver of type @ drivingNet_@ multi drivenNet of type @ name @ at line @
vee	csa	drvc	incompatible_driver_port_csve	W				Incompatible driver of type @ drivingPort_@ multi drivenPort of type @ name @ at line @
vee	csa	drvc	incompatible_driver_sig_csve	W				Incompatible driver of type @ drivingSignal_@ multi drivenSignal of type @ name @ at line @
vee	csa	dsbl	dsbl_used_csev	е				Disable used at line @

Cat   Phase   Type   Name   WE   V1995   V2001   Sys_ver   Csl   Desc
vee csa expr shift_by_non_const_csve e shift_by_non_const_csve e shift_by_non_constant at line @ ver csa expr miss_parenthesis_csve e Unary op @ Wiff_comparison op @ Wiff_compar
vee         csa         expr         shift by non constant in the B           vee         csa         expr         miss_parenthesis_csve         e         Shift by non constant in the B           vee         csa         forc         no_release_stmt_in_init_blk_csve         w         Force & statement initial block and there no release statemen on release statement on release statement in initial block and there no release statement on release
Vee   CSB   Force   CSB   Force   CSB   Force   CSB
vec   csa   forc   no_release_stmt_in_init_bik_csve   w   Proce@statement in initial block and ther no release statement in ore locks and ther no release statement in initial block and ther no release statement in ore locks and the normal statements or @ in the lock and the normal statements or @ in the lock and the normal statements or @ in the lock and the normal statements or @ in the lock and the normal statements or @ in the lock and the normal statements or @ in the lock and the normal statements or @ in the lock and the normal statements or @ in the lock and the normal statements or which and the lock and the normal statements or which and the lock and
vee csa forc no_release_stmt_in_init_blk_csve w
vee   csa   forc   no_force_stmt_in_init_blk_csve   w   ?   Release \$\text{statement.or } \text{elase } \$\text{\$\
Wee   csa   forc   no_force_stmt_in_init_blk_csve   w   ?   Release @ statement.for @ at I
Vee
vee csa forc forcing_input_port_csve e
Vee         csa         forc         forcing_input_port_csve         e         Forcing_input_port_esve           Vee         csa         func         return_value_not_at_end_of_func_csve         e         Return value not at ine of function at line of function and function at line of function and function at line of function tops in the function of function at line of function tops in the function tops in the function of function tops in the function of function tops in the function tops in the function tops in the functi
vee         csa         func         return_value_not_at_end_of_func_csve         e         Return value not at infunction at line of function at line of func
vee   csa   func   time_and_evclrt_in_func_csve   e   function at line   vee   csa   func   func_all_itself_rec_csve   e   function at line   vee   vee   vee   vee   function at line   vee   vee   vee   vee   vee   vee   vee   function at line   vee   v
Vee   csa   func   func_call_itself_rec_csve   e   function at line @
recursively at line   recursively at line   x   liEET 1364-1995 E 1364-1995
Vee
vee   csa   inist   input_port_drvn_from_inside_entity_csve   e   input_port @ hort connected in pare not entity of input_port @ not connected in pare not entity at line @ entity ent
vee         csa         init         assn_mem_in_init_blk_csve         e         Assign memory in in block at line @ linput port @ being di from inside of moduli at line @ linput port @ being di from inside of entity in line @ linput port @ being di from inside of entity in line @ linput port @ being di from inside of entity in line @ linput port @ being di from inside of entity in line @ linput port @ being di from inside of entity in line @ line @ linput port @ being di from inside of signal line @ linput port @ being di from inside of signal line @ linput port @ being di from inside of signal line @ linput port @ not connected in pare module at line @ linput port @ not connected in pare module at line @ linput port @ not connected in pare module at line @ linput port @ not connected in pare entity at line @ linput port @ not connected in pare entity at line @ linput port @ not connected in pare entity at line @ linput port @ not connected in pare signal at line @ A single compone with a line @ linput port @ not connected in pare signal at line @ A single compone with line with line with linput port @ not connected in pare signal at line @ A single compone with line with line with linput port @ not connected in pare signal at line @ A single compone with line with l
vee         csa         init         assn_mem_in_init_blk_csve         e         Assign memory in inblock at line @ Input port @ being di from inside of moduli at line @ Input port @ being di from inside of moduli at line @ Input port @ being di from inside of entity in line @ Input port @ being di from inside of entity in line @ Input port @ being di from inside of signal line @ Input port @ being di from inside of signal line @ Input port @ being di from inside of signal line @ Input port @ being di from inside of signal line @ Input port @ being di from inside of signal line @ Input port @ being di from inside of signal line @ Input port @ being di from inside of signal line @ Input port @ not connected in pare module at line @ Input port @ not connected in pare module at line @ Input port @ not connected in pare entity at line @ Input port @ not connected in pare entity at line @ Input port @ not connected in pare entity at line @ Input port @ not connected in pare entity at line @ Input port @ not connected in pare entity at line @ Input port @ not connected in pare signal at line @ Input port @ not entity at line @ Input port @ Input port @ not entity at line @ Input port @ Input port @ Input port @ not entity at line @ Input port @ not entity entity at line @ Input port @ not entity enti
vee         csa         inst         input_port_drvn_from_inside_mod_csve         e         Input port @ being difrom inside of modul at line @ from inside of modul at line @ linput port @ being difform inside of entity of line @ linput port @ being difform inside of entity of line @ linput port @ being difform inside of entity of line @ linput port @ being difform inside of signal line @ linput port @ being difform inside of signal line @ linput port @ being difform inside of signal line @ linput port @ not connected in pare module at line @ linput port @ not connected in pare module at line @ linput port @ not connected in pare module at line @ linput port @ not connected in pare entity at line @ linput port @ not connected in pare entity at line @ linput port @ not connected in pare entity at line @ linput port @ not connected in pare signal at line
vee csa inst input_port_not_connected_in_parent_entity_csve e input_port_entity in input_port_entity_csve e inst input_port_not_connected_in_parent_mod_csve e inst input_port_not_connected_in_parent_entity_csve e inst input_port_not_connected_in_parent_signal_csve e input_port_entity_tailine_entity_tailin
vee         csa         inst         input_port_drvn_from_inside_entity_csve         e         Input port @ being differentisted entity line @ input_port @ being different inside of signal line @ input_port input_port @ being different inside of signal line @ input_port @ not connected in pare module at line @ input_port @ not connected in pare module at line @ input_port @ not connected in pare module at line @ input_port @ not connected in pare entity at line @ input_port @ not connected in pare entity at line @ input_port @ not connected in pare signal at line @ input_port @ not connected in pare signal at line @ input_port @ not connected in pare input_port @ not connected input_port @ not connected inpare input_port @ not connected inpare input_port @ not connected inpare input_port @ not connected input_port @ not connected inpare input_port @ not connected inpare input_port @ not connected inpare input_port @ not connected input_port @ not @ not connected input_port @ not entity in @
vee         csa         inst         input_port_drvn_from_inside_signal_csve         e         Input port @ being diffrom inside of signal line @ from inside signal line signal li
vee         csa         inst         input_port_drvn_from_inside_signal_csve         e         Input port         linput port         lint line         linput port         lint lint lint         lint lint         lint lint         lint lint         lint lint         lint lint         lint lint         lint lint         lint lint lint         lint lint         lint lint         lint lint lint         lint lint lint         lint lint         lint lint         lint lint         lint lint         lint lint         lint lint         lint lint         lint lint         lint lint         lint lint         lint lint         lint lint         li
vee         csa         inst         input_port_not_connected_in_parent_mod_csve         e         Input_port@ not connected in pare module at line @ connected in pare module at line @ linput_port.           vee         csa         inst         input_port_not_connected_in_parent_entity_csve         e         Input_port @ not connected in pare entity at line @ linput_port @ not connected in pare entity at line @ linput_port @ not connected in pare entity at line @ linput_port @ not connected in pare entity at line @ linput_port @ not connected in pare signal at line @ linput_port @ not connected in pare signal at line @ linput_port @ not connected in pare signal at line @ linput_port @ not connected in pare signal at line @ linput_port @ not connected in pare signal at line @ linput_port @ not connected in pare signal at line @ linput_port @ not linput
vee       csa       inst       input_port_not_connected_in_parent_entity_csve       e       Input port @ not connected in pare module at line @ vee         vee       csa       inst       input_port_not_connected_in_parent_signal_csve       e       Input port @ not connected in pare entity at line @ vee         vee       csa       mdb       single_comp_contains_multiple_tri_drv_cdve       w       A single compone contains multiple tris drivers at line @ vee         vee       csa       mdb       unsuppexpr_on_lhs_net_drv_stmt_csve       w       Unsupported Expres type type on LHS of driver statement at line @ vee         vee       csa       mdb       unsuppexpr_on_lhs_port_drv_stmt_csve       w       Unsupported Expres type type on LHS of driver statement at line @ vee         vee       csa       mdb       unsuppexpr_on_lhs_sig_drv_stmt_csve       w       Unsupported Expres type type on LHS of driver statement at line @ vee         vee       csa       mdb       unsuppexpr_on_lhs_sig_drv_stmt_csve       w       Unsupported Expres type type on LHS of signaldriver statement at line @ Tristate not in top modet in the person of
vee         csa         inst         input_port_not_connected_in_parent_entity_csve         e         Input port @ not connected in pare entity at line @ entity at line @           vee         csa         inst         input_port_not_connected_in_parent_signal_csve         e         Input port @ not connected in pare entity at line @           vee         csa         mdb         single_comp_contains_multiple_tri_drv_cdve         w         A single compone contains multiple tris drivers at line @           vee         csa         mdb         unsuppexpr_on_lhs_net_drv_stmt_csve         w         Unsupported Expres type type on LHS of driver statement at line @           vee         csa         mdb         unsuppexpr_on_lhs_port_drv_stmt_csve         w         Unsupported Expres type type on LHS of driver statement at line @           vee         csa         mdb         unsuppexpr_on_lhs_sig_drv_stmt_csve         w         Unsupported Expres type type on LHS of Signaldriver statement at line @           vee         csa         mdb         tri_not_in_top_mod_csve         e         Tristate not in top on at line @           vee         csa         mdb         tri_not_in_top_ent_csve         e         Tristate not in top sig_time.           vee         csa         mdb         tri_not_in_top_sig_csve         e         Tristate not in top sig_time.
vee       csa       inst       input_port_not_connected_in_parent_signal_csve       e       Input port @ not connected in pare signal at line @ linput port @ not connected in pare signal at line @ signal at line @ A single comp_contains_multiple_tri_drv_cdve         vee       csa       mdb       single_comp_contains_multiple_tri_drv_cdve       w       A single component contains multiple tri driver at line @ contains multiple tris drivers at line @ type type on LHS of driver statement at line @ type type on LHS of driver statement at line @ type type on LHS of driver statement at line @ type type on LHS of driver statement at line @ tri_not_in_top_mod_csve         vee       csa       mdb       unsuppexpr_on_lhs_sig_drv_stmt_csve       w       Unsupported Expres type type on LHS of driver statement at line @ type type on LHS of Signaldriver statem at line @ type type on LHS of Signaldriver statem at line @ tri_not_in_top_mod_csve         vee       csa       mdb       tri_not_in_top_mod_csve       e       Tristate not in top mod at line @ tristate not in top er at line @ tristate not in top sig_csve
vee         csa         inst         input_port_not_connected_in_parent_signal_csve         e         Input_port @ not connected in pare signal at line @ signal at line @           vee         csa         mdb         single_comp_contains_multiple_tri_drv_cdve         w         A single compone contains multiple tris drivers at line @           vee         csa         mdb         unsuppexpr_on_lhs_net_drv_stmt_csve         w         Unsupported Expres type type on LHS of driver statement at line @           vee         csa         mdb         unsuppexpr_on_lhs_port_drv_stmt_csve         w         Unsupported Expres type type on LHS of driver statement at line @           vee         csa         mdb         unsuppexpr_on_lhs_sig_drv_stmt_csve         w         Unsupported Expres type type on LHS of signaldriver statement at line @           vee         csa         mdb         tri_not_in_top_mod_csve         e         Tristate not in top mod_at line @           vee         csa         mdb         tri_not_in_top_ent_csve         e         Tristate not in top sig_at line @           vee         csa         mdb         tri_not_in_top_sig_csve         e         Tristate not in top sig_at line @
vee       csa       mdb       single_comp_contains_multiple_tri_drv_cdve       w       A single compone contains multiple tris drivers at line @         vee       csa       mdb       unsuppexpr_on_lhs_net_drv_stmt_csve       w       Unsupported Expres type type on LHS of driver statement at line @         vee       csa       mdb       unsuppexpr_on_lhs_port_drv_stmt_csve       w       Unsupported Expres type type on LHS of driver statement at line @         vee       csa       mdb       unsuppexpr_on_lhs_sig_drv_stmt_csve       w       Unsupported Expres type type on LHS of Signaldriver statement at line @         vee       csa       mdb       tri_not_in_top_mod_csve       e       Tristate not in top mod at line @         vee       csa       mdb       tri_not_in_top_ent_csve       e       Tristate not in top sig at line @         vee       csa       mdb       tri_not_in_top_sig_csve       e       Tristate not in top sig at line @
vee         csa         mdb         single_comp_contains_multiple_tri_drv_cdve         w         A single compone contains multiple tris drivers at line @           vee         csa         mdb         unsuppexpr_on_lhs_net_drv_stmt_csve         w         Unsupported Expres type type on LHS of driver statement at leg.           vee         csa         mdb         unsuppexpr_on_lhs_port_drv_stmt_csve         w         Unsupported Expres type type on LHS of driver statement at leg.           vee         csa         mdb         unsuppexpr_on_lhs_sig_drv_stmt_csve         w         Unsupported Expres type type on LHS of Signaldriver statement at leg.           vee         csa         mdb         tri_not_in_top_mod_csve         e         Tristate not in top mod at line @           vee         csa         mdb         tri_not_in_top_ent_csve         e         Tristate not in top sig at line @           vee         csa         mdb         tri_not_in_top_ent_csve         e         Tristate not in top sig at line @
vee csa mdb unsuppexpr_on_lhs_net_drv_stmt_csve w Unsupported Expres type type on LHS of driver statement at line @  vee csa mdb unsuppexpr_on_lhs_port_drv_stmt_csve w Unsupported Expres type type on LHS ofl driver statement at line @  vee csa mdb unsuppexpr_on_lhs_sig_drv_stmt_csve w Unsupported Expres type type on LHS ofl driver statement at line @  vee csa mdb tri_not_in_top_mod_csve e Tristate not in top mod at line @  vee csa mdb tri_not_in_top_ent_csve e Tristate not in top end at line @  vee csa mdb tri_not_in_top_sig_csve e Tristate not in top sig
type type on LHS of driver statement at I @  vee csa mdb unsuppexpr_on_lhs_port_drv_stmt_csve w Unsupported Expres type type on LHS of driver statement at I @  vee csa mdb unsuppexpr_on_lhs_sig_drv_stmt_csve w Unsupported Expres type type on LHS of Signaldriver statement at I @  vee csa mdb tri_not_in_top_mod_csve e Tristate not in top mode at line @  vee csa mdb tri_not_in_top_ent_csve e Tristate not in top end at line @  vee csa mdb tri_not_in_top_sig_csve e Tristate not in top sig
vee       csa       mdb       unsuppexpr_on_lhs_port_drv_stmt_csve       w       Unsupported Expres type type on LHS off driver statement at learning with the learning of type type on LHS off driver statement at learning with the learning of the learning with
vee     csa     mdb     unsuppexpr_on_lhs_port_drv_stmt_csve     w     Unsupported Expres type type on LHS of driver statement at legent with the legent control of type type on LHS of stype type on LHS of signal driver statement at line graph.       vee     csa     mdb     tri_not_in_top_mod_csve     e     Tristate not in top mode at line graph.       vee     csa     mdb     tri_not_in_top_ent_csve     e     Tristate not in top ender at line graph.       vee     csa     mdb     tri_not_in_top_est_csve     e     Tristate not in top sight line graph.       vee     csa     mdb     tri_not_in_top_sig_csve     e     Tristate not in top sight line graph.
vee       csa       mdb       unsuppexpr_on_lhs_sig_drv_stmt_csve       w       Unsupported Expres type type on LHS of Signaldriver statem at line @         vee       csa       mdb       tri_not_in_top_mod_csve       e       Tristate not in top mode at line @         vee       csa       mdb       tri_not_in_top_ent_csve       e       Tristate not in top ender at line @         vee       csa       mdb       tri_not_in_top_sig_csve       e       Tristate not in top sig_csve
vee     csa     mdb     unsuppexpr_on_lhs_sig_drv_stmt_csve     w     Unsupported Expres type type on LHS of Signaldriver staten at line @       vee     csa     mdb     tri_not_in_top_mod_csve     e     Tristate not in top mod at line @       vee     csa     mdb     tri_not_in_top_ent_csve     e     Tristate not in top end at line @       vee     csa     mdb     tri_not_in_top_sig_csve     e     Tristate not in top sig_csve
type type on LHS of Signaldriver staten at line @  vee csa mdb tri_not_in_top_mod_csve e Tristate not in top mo at line @  vee csa mdb tri_not_in_top_ent_csve e Tristate not in top en at line @  vee csa mdb tri_not_in_top_est_csve e Tristate not in top sig_csve e Tristate not in top sig_csve type on LHS of Signaldriver staten at line @  tri_not_in_top_mod_csve e Tristate not in top sig_csve e Tristate not in top sig_csve type on LHS of Signaldriver staten at line @
vee     csa     mdb     tri_not_in_top_mod_csve     e     Tristate not in top mo at line @       vee     csa     mdb     tri_not_in_top_ent_csve     e     Tristate not in top en at line @       vee     csa     mdb     tri_not_in_top_sig_csve     e     Tristate not in top sig
vee     csa     mdb     tri_not_in_top_ent_csve     e     Tristate not in top er at line @       vee     csa     mdb     tri_not_in_top_sig_csve     e     Tristate not in top sig_csve
vee     csa     mdb     tri_not_in_top_sig_csve     e     Tristate not in top sig_sig_sig_sig_sig_sig_sig_sig_sig_sig_
vee csa mdb tri_not_in_top_sig_csve e Tristate not in top sig
vee     csa     mdb     tri_primitive_inst_csve     e     Tristate primitive
vee csa mdb tri_net_only_one_drvr_csve e instantiation at line  Tri Net has only or
driver at line @  vee csa mdb tri_port_only_one_drvr_csve e Tri Port has only or
driver at line @
vee     csa     mdb     tri_sig_only_one_drvr_csve     e     Tri Signal has only of driver at line @
vee     csa     mem     single_bit_mem_csve     e     Single bit memory @       line @
vee     csa     mod     redef_mod_csve     e     Redefined module @ line @
vee csa mod redef_ent_csve e Redefined entity @
vee csa mod redef_signal_csve e Redefined signal @
line @ ´

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_v	/er Cs	
vee	csa	net	tri_and_port_only_one_driver_csve	е	?				triandPort @ has only one driver at line @
vee	csa	net	tri_and_sig_only_one_driver_csve	е	?				triandSignal @ has only one driver at line @
vee	csa	net	var_assn_but_never_ref_csve	е					Variable @ assigned but never referenced at line @
vee	csa	net	var_never_assn_csve	е					Variable @ never assigned at line @
vee	csa	net	var_not_assn_in_all_paths_csve	е					Variable @ not being assigned in all paths at
vee	csa	net	var_not_in_snsl_csve	е					line @ Variable @ not in
vee	csa	net	reg_connected_to_inout_in_inst_csve	е					sensitivity list at line @  Reg @ connected to inout @ in instantiation
vee	csa	net	reg_connectede_to_output_in_inst_csve	е					@ at line @  Reg @ connected to output in instantiation at
vee	csa	net	reg_used_as_output_of_cont_assn_csve	е					line @ Reg @ used as output of continuous assign at line @
vee	csa	net	port_used_prior_to_decl_csve	е					Port @ used prior
vee	csa	net	dupl_sig_in_snsl_csve	е					toDeclaration at line @ Duplicate signal @ in
vee	csa	netd	var_never_assigned_csve	е					Variable @ never assigned at line @
vee	csa	num	assignment_contains_real_num_const_csve	е					Assignment contains a real number constant at
vee	csa	parm	unused_parm_csve	е					line @ Unused parameter @ at line @
vee	csa	parm	redef_param_csve	е					Redefined parameter @ at line @
vee	csa	pp	redef_macro_csve	е					Redefined macro @ at line @
vee	csa	prts	prts_on_vec_net_not_allowed_csve	W					Part select @ on a vectored Net may not be allowed according to IEEE 1364-1995 at line @
vee	csa	prts	prts_on_vec_port_not_allowed_csve	W					Part select @ on a vectored Port may not be allowed according to IEEE 1364-1995 at line @
vee	csa	prts	prts_on_vec_sig_not_allowed_csve	W					Part select @ on a vectored Signal may not be allowed according to IEEE 1364-1995 at line @
vee	csa	prts	out_of_range_bit_ref_csve	е					Out of range bus bit referenced at line @
vee	csa	prts	vec_index_order_incorrect_csve	е					Vector index @ order incorrect at line @
vee	csa	prts	vec_index_truncated_csve	е					Vector index @ truncated at line @
vee	csa	sdir	sdir_compiler_csve	е					Found synopsys compiler directive at line @
vee	csa	seq	blk_not_in_lib_csve	е					Block @ not in library at line @
vee	csa	sig	sig_will_float_when_rel_csve	е					Signal @ will float when it is released at line @
vee	csa	snsl	var_modified_in_snsl_csve	е					Variable @ modified in sense list at line @
vee	csa	snsl	var_in_snsl_unsused_in_blk_csve	е					Variable @ in sensitivity list not used in block at line @
vee	csa	snsl	rhs_var_noi_in_snsl_csve	е					RHS variable not in sensitivity list at line @
vee	csa	spec	spec_blk_found_csev	е					Specify block found at line @
vee	csa	sply	sply_being_driven_csve	е					Supply being driven at line @
vee	csa	sply	sply_not_def_user_keyword_csve	е					Supply not defined with user defined keyword at line @
vee	csa	sply	sply_not_in_lib_csve	е					Supply not in library at line @
vee	csa	sply	output_conncet_to_sply_	е					Output @ connect to supply at line @
vee	csa	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_csve	е		-			Arithmetic operator RHS has one less bit than the LHS at line @
vee	csa	stmt	ar_op_unequal_lhs_rhs_csve	е					Arithmetic operator unequal width LHS and RHS at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	csa	stmt	ar_op_unequal_var_on_rhs_csve	е					Arithmetic operator unequal width variables
									@ on RHS at line @
vee	csa	task	task_call_iteslf_rec_csve	е					Task @ calling itself recursively at line @
vee	csa	time	time_var_bit_used_csde	е					Time variable bit used at line @
vee	csa	tri	tri_not_in_top_mod_csve	е					Tristate @ not in top
vee	csa	tri	tri_not_in_top_entity_csve	е					module at line @ Tristate @ not in top
vee	csa	tri	tri_not_in_top_signal_csve	е					entity at line @ Tristate @ not in top
									signal at line @
vee	csa	tri	tri_prim_ist_csve	е					Tristate primitive instantiation @ at line @
vee	csa	udp	upd_not_supported_csve	е					UDPs are not supported at line @
vee	csb	assn	x_in_rhs_of_assihnment_csbve	е					x in rhs of assignment at line @
vee	csb	assn	z_in_rhs_of_assn_default_csi_csbve	е					x in rhs of assignement
									in defaultCase item at line @
vee	csb	assn	z_in_rhs_of_assn_csbve	е					z in rhs of assignement at line @
vee	csb	assn	unequal_length_lhs_rhs_csbve	е					Unequal length LHS and
vee	csb	assn	unequal_length_lhs_rhs_off_one_bit_csbve	е					RHS at line @ Unequal length LHS and
			6						RHS off by one bit at line
vee	csb	blk	blk_ill_block_id_csv	е					Illegal block @ at line @
vee	csb	blk	nonblocking_assign_in_comb_always_blk_csbve	е					Non blocking aasignment in combinational always
vee	csb	blk	seq_blk_contains_blk_assn_csbve	е					block at line @ Sequential block
VCC	030	DIK	304_DIK_00/Hall/13_DIK_d33/1_030V0						contains blocking
vee	csb	casn	LHS_not_reg_casn_veve	е					assignement at line @ LHS cannot be a register
vee	csb	ccd	ccd_cdir_must_be_cst_expr_csbve	е				Х	@ at line @ CSL directive size must
VCC	CSD	ccu	ccu_cuii_must_be_cst_expt_csbve					^	be constant Expression
vee	csb	clk	clk_name_not_found_cdir_csbve	е				Х	at line @ Clock name not found in
vee	csb	clk	expr_sunj_to_different_clk_phases_csbve	е					cslc directive at line @ Expression subject to
100	000	Oiit	oxpr_ourry_to_amoronic_on_priagog_copye						different clock phases at
vee	csb	cmdl	cannot_use_librescan_with_liborder_specified_csbve	е					line @ Cannot use +librescan
									when +liborder has already been specified at
vee	csb	cmdl	cannot_use_liborder_with_librescan_specified_csbve	е					line @ Cannot use +liborder
vee	CSD	Ciliai	cannot_use_iiborder_witir_iibrescari_specified_csbve	е					when +librescan has
									already been specified at line @
vee	csb	cond	if_case_question_cond_csbve	е					If/case conditional expression expr syntax
									error at line @
vee	csb	cond	if_no_else_in_comb_blk_csbve	е					If no else in combinational block at
vee	csb	cond	if_no_else_in_comb_blk_csbvh	е					line @ If no else in
100	000	oona	11_110_0100_111_001110_011(_0000411						combinational block at
vee	csb	csi	xcsi_not_in_casex_csbve	е					line @ xCase item not in casex
vee	csb	csi	noncnst_csi_csbve	е					at line @ Non-constantCase item
vee	csb	csi	noncnst_dely_csbve	е					@ at line @ Non-constant delay @ at
			_ ,_						line @
vee	csb	csi	noncstn_rep_in_conc_csbve	е					Non-constant repeator in concatenation at line @
vee	csb	css	sns_pragma_full_case_csbve	е					Assume a full case, missing default or
									synopsys pragma full
vee	csb	cyb	repeat_in_delay_cyb_csv	е					case. at line @ Repeat clause in delay
vee	csb	cyb	repeat_in_event_control_cyb_csv	е					not supported at line @ Repeat clause in event
,,,,	300	٠,5							control not supported at
vee	csb	cyb	event_id_not_supported_cyb_csv	е					line @ @ event id is not
vee	csb	cyb	ill_proc_assign_cyb_csv	е					supported at line @ Illegal procedural
	- 52	-,~	p						continuous assignment statement at line @
vee	csb	cyb	ill_deassign_cyb_csv	е					Illegal de-assign
vee	csb	cyb	ill_force_cyb_csv	е					statement at line @ Illegal force statement at
	csb		•						line @
vee	CSD	cyb	ill_release_cyb_csv	е	1				megai release statement

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	csb	cyb	repeat_as_delay_cyb_csv	е					at line @  Repeat as delay not
vee	csb	cyb	repeat_as_event_control_cyb_csv	е					supported at line @ Repeat as event control
vee	csb	cyb	wait_statement_not_cyb_csv	е					not supported at line @ Wait statement is not
vee	csb	cyb	disable_statement_not_cyb_csv	е					supported at line @  Disable statement is not
		,							supported at line @
vee	csb	cyb	events_not_supported_cyb_csv	е					Events are not supported at line @
vee	csb	cyb	fork_join_blocks_not_supported_cyb_csv	е					Fork/join blocks are not supported at line @
vee	csb	cyb	unsupp_function_return_time_cyb_csv	е					Unsupported function return time at line @
vee	csb	cyb	not_supp_events_cyb_csv	е					Events are not supported at line @
vee	csb	cyb	repeat_in_delay_or_event_cyb_csv	е					Repeat clause in delay or Event control at line @
vee	csb	cyb	ill_proc_cont_assign_stmt_cyb_csv	е					Illegal procedural continuous assignment
			ill dans in a state and						statement at line @
vee	csb	cyb	ill_deassign_cyb_stmt_csv	е					Illegal de-assign statement at line @
vee	csb	cyb	ill_force_stmt_cyb_csv	е					Illegal force statement at line @
vee	csb	cyb	ill_release_stmt_cyb_csv	е					Illegal release statement at line @
vee	csb	cyb	repeat_not_supp_as_delay_or_event_cyb_csv	е					Repeat as delay or event control not supported at
vee	csb	cyb	not_supp_wait_stmt_cyb_csv	е					line @ Wait statement is not
		-							supported at line @
vee	csb	cyb	not_supp_disable_stmt_cyb_csv	е					Disable statement is not supported at line @
vee	csb	cyb	supp_not_events_cyb_csv	е					Events are not supported at line @
vee	csb	cyb	not_supp_fork_join_blocks_cyb_csv	е					Fork/join blocks are not supported at line @
vee	csb	cyb	not_supp_UDP_cyb_csv	е					UDPs are not supported at line @
vee	csb	cyb	not_supp_defparam_cyb_csv	е					Defparam is not supported at line @
vee	csb	cyb	specify_blk_not_supported_csbve	е					Specify blocks are not
vee	csb	cyb	mintypmax_expr_not_supp_csbve	w					supported at line @ mintypmax Expressions
									are not supported at line @
vee	csb	decl	decl_array_over_max_size_csbve	е					Array @ exceeds maximum size limit at
vee	csb	dely	max_val_dly_csv	е					line @ Too many delay values,
vee	csb	dely	found_gate_dely_not_allowed_csbve	е					max @ at line @ Found gate delay which
vee	csb	dely	found dely in casn not allowed csbve	е					are not allowed at line @ Found delay in
VCC	035	doly	lound_dely_in_odsh_not_allowed_dsbvc						continuous assignment which are not allowed at
									line @
vee	csb	dely	dely_ignoring_dely_specification_csbve	е					Delay Ignoring delay specification in Net
vee	csb	dely	dely_ignoring_dely_specification_port_csbve	е					Declaration at line @ Delay Ignoring delay
									specification in Port Declaration at line @
vee	csb	dely	dely_ignoring_dely_specification_sig_csbve	е					Delay Ignoring delay specification in Signal
vee	csb	dely	dely ignoring dely before stmt csbve	е					Declaration at line @  Delay Ignoring delay
vee	CSD	uely	dely_ignornig_dely_belore_strit_csbve	6					before statement at line
vee	csb	dely	x_or_z_in_dely_csbve	е					@ x or z in delay at line @
vee	csb	dely	non_int_dely_csbve	е					Non integer delay at line @
vee	csb	dmsn	mem_prts_index_out_of_range_for_mem_csbve	е					Memory part select [@:@] index @ out
									range for memory @ at line @
vee	csb	dmsn	dime_select_for_mem_missing_csbve	е					Select for memory @ missing at line @
vee	csb	dmsn	dime_index_out_of_bounds_for_mem_csbve	е					Index <index> out of bounds for memory @.</index>
1/0-	cak	dms:-	dimo arta out of hounds for and only	_					Range [@: @] at line @
vee	csb	dmsn	dime_prts_out_of_bounds_for_net_csbve	е					Part select [@ : @] out of bounds for net @. Range
vee	csb	dmsn	dime_prts_out_of_bounds_for_port_csbve	е					[@:@] at line @ Part select [@:@] out of
									bounds for port @. Range [@ : @] at line @
vee	csb	dmsn	dime_prts_out_of_bounds_for_sig_csbve	е					Part select [@ : @] out of

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									bounds for signal @. Range [@ : @] at line @
vee	csb	dmsn	dime_prts_reg_csbve	е					Part select [@ : @] reg @. Range [@ : @] at line
									@
vee	csb	drvc	incompatible_drvc_for_net_csbve	е					Incompatible drivers for Net @ at line @
vee	csb	drvc	incompatible_drvc_for_port_csbve	е					Incompatible drivers for Port @ at line @
vee	csb	drvc	incompatible_drvc_for_sig_csbve	е					Incompatible drivers for Signal @ at line @
vee	csb	drvc	drvc_multiple_drive_net_partially_overlap_csbve	е					Multiple drive Net partially overlap at line @
vee	csb	drvc	drvc_multiple_drive_port_partially_overlap_csbve	е					Multiple drive Port partially overlap at line @
vee	csb	drvc	drvc_multiple_drive_sig_partially_overlap_csbve	е					Multiple drive Signal
vee	csb	dsgn	dsgn_top_mod_cannot_id_csbve	е					partially overlap at line @ Top module @ cannot be
vee	csb	dsgn	dsgn_top_entity_cannot_id_csbve	е					identified at line @ Top entity @ cannot be
vee	csb	dsgn	dsgn_top_unit_cannot_id_csbve	е					identified at line @ Top unit @ cannot be
vee	csb	dsgn	unit dsgn cycle not spanning tree csbve	е					identified at line @ Unit design hierarchy
			g						contains a cycle. Hierarchy is not a
	aab	0110	not allowed adapting or solve						spanning tree. at line @
vee	csb	evc	not_allowed_edge_trigger_csbve	е					Edge trigger is not allowed in this location at
vee	csb	evc	ectl_in_assn_csbve	е					line @ Event control in
vee	csb	expr	expr_prts_indices_1bit_var_csbve	е					assignement at line @ Part select indices 1-bit
vee	csb	expr	expr prts must be cst expr csbve	е					variable at line @ Part select specifier
		·							Expression must be constant Expression at
vee	csb	expr	not_const_expr_csbve	е					line @ Repetition multiplier in
Vec	CSD	СХРІ	not_const_expt_conve						concatenation is not a
									constant Expression at line @
vee	csb	expr	ill_bit_select_expr_csbve	е					Illegal bit select expression @ at line @
vee	csb	expr	equality_operator_detected_csbve	е					Use of operator === detected at line @
vee	csb	expr	notequal_operator_detected_csbve	е					Use of operator !== detected at line @
vee	csb	expr	ill_parm_value_csbve	е					Illegal parameter value at line @
vee	csb	expr	repetition_multiplier_in_conc_not_const_expr_csbve	w					Repetition multiplier in concatenation is not a
									constant Expression at line @
vee	csb	expr	int_operand_not_1_bit_csbve	W					Logic operator has
									of 1-bit operands at line
vee	csb	expr	unsupp_expr_csbve	w					Unsupported Expression
vee	csb	expr	unsupp_operator_csbve	w					type @ at line @ Unsupported operator
vee	csb	expr	use_of_sq_bit_const_csbve	w					type @ at line @ Use of single bit constant
vee	csb	expr	unary_op_in_comparison_csbve	е					at line @ Unary op used in
vee	csb	expr	nonconst_repeator_in_conc_csbve	е					comparison at line @  Non constant repeator in
		-	_ ·						concatention at line @
vee	csb	expr	x_or_z_in_cond_expr_csbve	е					expression at line @
vee	csb	expr	zero_in_rep_in_conc_csbve	е					Zero repeator in concatenation at line @
vee	csb	expr	expr_in_mod_port_dir_csbve	е					Expression @ in module port dir at line @
vee	csb	expr	expr_in_ent_port_dir_csbve	е					Expression @ in entity port dir at line @
vee	csb	expr	expr_in_sig_port_dir_csbve	е					Expression @ in unit port dir at line @
vee	csb	expr	expr_in_inst_csbve	е					Expression @ in inst i@ at line @
vee	csb	expr	expr_operator_operands_unequal_lenght_csbve	е					Expression operator @ operands @ unequal
	cak	file	connet onen filter enceification file och						length at line @
vee	csb	file	cannot_open_filter_specification_file_csbve	е					Cannot open filter specification file @ at line
vee	csb	file	filter_specification_file_missing_csbve	е					@ Filter specification file
									name @ is missing at line @
vee	csb	file	mismatch_mod_file_name_csbve	е					Mismatch between

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									module name @ and file name @ at line @
vee	csb	file	mismatch_ent_file_name_csbve	е					Mismatch between entity
									name @ and file name @ at line @
vee	csb	file	mismatch_sig_file_name_csbve	е					Mismatch between signal name @ and file name
		<i>t</i>	ill from this time and the						@ at line @
vee	csb	forc	ill_forc_obj_type_csbve	е					Illegal force object type @ at line @
vee	csb	func	ill_func_return_type_csv	е					Illegal function return type at line @
vee	csb	func	ill_func_csv	е					Illegal function @ at line @
vee	csb	func	port_not_output_func_csbve	е					Port @ direction cannot
vee	csb	func	ill_use_func_csbve	е					be output at line @ Illegal use of function @
vee	csb	func	func_not_define_csbve	е					at line @ Function @ not defined
vee	csb	func	too_many_arg_to_func_csbve	е					at line @ Too many arguments
VCC	030	Tario	too_many_arg_to_rane_coove						passed to function @ at line @
vee	csb	func	too_few_arg_to_func_csbve	е					Too few arguments
									passed to function @ at line @
vee	csb	func	undefined_func_csbve	е					Undefined function @ at line @
vee	csb	func	funct_expr_cannot_expnaded_csbve	е					Function expression @
									cannot be expanded at line @
vee	csb	func	funct_not_used_in_expr_csbve	W					Function @ is not being used in an Expression at
vee	csb	func	func_decl_csbve	w					line @ Function Declaration @
vee	CSD	Turic	Turio_deci_csbve	VV					already declared as
vee	csb	func	func_param_csb	е					another type at line @ Found function
vee	csb	func	unmatched_funct_param_csbve	е					parameter @ at line @ Unmatched function
									parameter @ at line @
vee	csb	gate	ill_output_pin_name_gate_csv	е					Illegal output terminal Expression pin @ at line
vee	csb	hid	cannot_locate_hier_id_hid_csbve	е					@ Can't locate hierarchical
vee	csb	hid	ref_minst_found_in_expr_hid_csbve	е					identifier @ at line @ References a module
VCC	CSD	Tild	rei_minst_round_in_expi_ma_csbve						instance @ found in an
vee	csb	hid	ref_entity_found_in_expr_hid_csbve	е					Expression hid at line @ References a entity
									instance @ found in an Expression hid at line @
vee	csb	hid	ref_unit_found_in_expr_hid_csbve	е					References a unit instance @ found in an
									Expression hid at line @
vee	csb	hid	ref_in_eexpr_hid_csbve	е					References a module instance @ passed as
									argument to PLI task call is also found in an
	200	hid	ref in ever hid cobve						Expression @ at line @ References a entity
vee	csb	nia	ref_in_expr_hid_csbve	е					instance @ passed as
									argument to PLI task call is also found in an
vee	csb	hid	reff_in_expr_hid_csbve	е					Expression @ at line @ References a unit
VCC	CSD	Tild	ren_in_expi_ind_cabve						instance @ passed as
									argument to PLI task call is also found in an
vee	csb	hid	hid_name_traverses_into_func	е					Expression @ at line @ Hid @ name traverses
									into a function @ at line @
vee	csb	hid	hid_ref_mod_out_arg_sytk_csbve	е					Hid @ referencing a
									module instance passed as 'out' type argument to
									a system task @ at line @
vee	csb	hid	hid_ref_entity_out_arg_sytk_csbve	е					Hid @ referencing a entity instance passed as
									'out' type argument to a
vee	csb	hid	hid_ref_unit_out_arg_sytk_csbve	е					system task @ at line @ Hid @ referencing a unit
									instance passed as 'out' type argument to a
1/00	och	Pi-4	hid reference not found cohus	1					system task @ at line @
vee	csb	hid	hid_reference_not_found_csbve	е					@ reference not found at line @
vee	csb	hid	mifc_in_hid_not_exist_csbve	е					Module instance @ in hid does not exist at line @
vee	csb	hid	entity_instance_in_hid_not_exist_csbve	е					Entity instance @ in hid

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vee	csb	hid	unit_instance_in_hid_not_exist_csbve	е					does not exist at line @ Unit instance @ in hid
vee	csb	hid	mod_found_in_path_in_dsgn_csbve	е					does not exist at line @ Module @ found in path
vee	csb	hid	enity_found_in_path_in_dsgn_csbve	е					@ in the design at line @ Entity @ found in path @
vee	csb	hid	unit_found_in_path_in_dsgn_csbve	е					in the design at line @ Unit @ found in path @
		,							in the design at line @
vee	csb	hid	hierarchical_id_path_contains_func_csb	е					Hierarchical ID @ path contains a function at line
vee	csb	id	ill_terminal_id_csv	е					@ Illegal terminal identifier
vee	csb	init	assn mem in init blk csbve	е					at line @ Assign memory in initial
	csb	inst							block at line @  Duplicate port @ in the
vee	CSD	IIISt	inst_duplicate_mod_name_csbve	е					port list for module @ at
vee	csb	inst	inst_duplicate_entity_name_csbve	е					line @ Duplicate port @ in the
									port list for entity @ at line @
vee	csb	inst	inst_duplicate_unit_name_csbve	е					Duplicate port @ in the port list for unit @ at line
									. @
vee	csb	inst	miss_declparam_inst_csv	е					Parameter Declaration missing value at line @
vee	csb	inst	ill_mod_inst_name_csbve	е					Illegal module instance @ at line @
vee	csb	inst	ill_entity_inst_name_csbve	е					Illegal entity instance @ at line @
vee	csb	inst	ill_unit_inst_name_csbve	е					Illegal unit instance @ at line @
vee	csb	inst	inst_name_defined_mod_csv	е					Instance name @
									already defined in this module at line @
vee	csb	inst	inst_name_defined_ent_csv	е					Instance name @ already defined in this
vee	csb	inst	inst_name_defined_unit_csv	е					entity at line @ Instance name @
vee	CSD	11151	inst_name_defined_drift_csv	6					already defined in this
vee	csb	inst	inst_too_many_bits_csbve	е					unit at line @ Too many bits for port @
									of instance array @, formal @, actual @ at
vee	csb	inst	inst_port_not_connected_var_csbve	е					line @ Port 'port' of instance
	002								array 'array' is not connected to variable at
									line @
vee	csb	inst	inst_insufficient_bits_csbve	е					Insufficient bits for port 'port' of instance array
									'array', formal number, actual number at line @
vee	csb	inst	inst_mod_name_not_defined_cssbve	е					Module name not defined at line @
vee	csb	inst	inst_ent_name_not_defined_csbve	е					Entity name not defined at line @
vee	csb	inst	inst_unit_name_not_defined_csbve	е					Unit name not defined at
vee	csb	inst	many_mod_inst_param_assign_csbve	е					line @ Too many module
									instance parameter assignments (number >
vee	csb	inst	many entity inst param assign csbve	е					rrumber) at line @ Too many entity instance
			a.,,						parameter assignments (number > rrumber) at
									ine @
vee	csb	inst	many_unit_inst_param_assign_csbve	е					Too many unit instance parameter assignments
									(number > rrumber) at line @
vee	csb	inst	complexexpr_cannot_mapped_inout_port_csbve	е					Complex Expression @ cannot be mapped to
vee	csb	inst	complexexpr_cannot_mapped_unknown_port_csbve	е					inout port @ at line @ Complex Expression @
vee	เอม	IIIƏL	- complexexpi_calinot_mapped_unknown_port_csbve	6					cannot be mapped to
									unknown type port @ at line @
vee	csb	inst	netdecl_contains_ill_prts_csbve	е					Net Declaration [@: @] contains an illegal part
vee	csb	inst	regdecl_contains_ill_prts_csbve	е					select at line @ Reg Declaration [@ : @]
100	555		10g0001_0011tdii10_111_p1tb_000ve						contains an illegal part
vee	csb	inst	complex_expr_inst_parent_module_csbve	е					select at line @ Complex actual
									Expression associated with port @ of module @
									instantiated in parent module at line @
vee	csb	inst	complex_expr_inst_entity_parent_module_csbve	е					Complex actual

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vee	csb	inst	complex_expr_inst_unit_parent_module_csbve	е			-	Expression associated with port @ of entity @ instantiated in parent module at line @ Complex actual
								Expression associated with port @ of unit @ instantiated in parent module at line @
vee	csb	inst	inst_mod_output_port_width_csbve	е				Mod @ Output port @ width mismatch, actual-width ( port-width ) at line @
vee	csb	inst	inst_entity_output_port_width_csbve	е				Entity @ Output port @ width mismatch, actual-width ( port-width ) at line @
vee	csb	inst	inst_unit_output_port_width_csbve	е				Unit @ Output port @ width mismatch, actual-width ( port-width )
vee	csb	inst	inst_mod_input_port_width_csbve	е				at line @  Mod @ Input port @  width mismatch, actual-width ( port-width )  at line @
vee	csb	inst	inst_entity_input_port_width_csbve	е				Entity @ Input port @ width mismatch, actual-width ( port-width ) at line @
vee	csb	inst	inst_unit_input_port_width_csbve	е				Unit @ Input port @ width mismatch, actual-width ( port-width ) at line @
vee	csb	inst	inst_mod_not_define_csbve	е				Module not defined at line @
vee	csb	inst	inst_entity_not_define_csbve	е				Entity not defined at line @
vee	csb csb	inst inst	inst_unit_not_define_csbve miss_mifc_name_csbve	e W			X	Unit not defined at line @ Missing module instance name. This syntax is an error according to IEEE 1364-1995 but is allowed by commercial Verilog compilers at line @
vee	csb	inst	miss_ent_instance_name_csbve	w			X	Missing entity instance name. This syntax is an error according to IEEE 1364-1995 but is allowed by commercial Verilog compilers at line @
vee	csb	inst	miss_unit_instance_name_csbve  mifc_port_actual_formal_width_mismatch_csbve	W			х	Missing unit instance name. This syntax is an error according to IEEE 1364-1995 but is allowed by commercial Verilog compilers at line @ Module @ instance @
								port @ width mismatch, actual width @ formal width @ at line @
vee	csb	inst	ent_port_actual_formal_width_mismatch_csbve	W				Entity @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vee	csb	inst	unit_port_actual_formal_width_mismatch_csbve	W				Unit @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vee	csb	inst	unmatched_port_connect_in_inst_csbve	е				Unmatched port @ connect in instance @ at line @
vee	csb	inst	inst_differs_in_case_from_mod_csbve	е				Instance name @ differs in case from module name @ at line @
vee	csb	inst	inst_differs_in_case_from_ent_csbve	е				Instance name @ differs in case from entity name @ at line @
vee	csb	inst	inst_differs_in_case_from_sig_csbve lib_name_not_mod_declaration_csv	e				Instance name @ differs in case from signal name @ at line @ Library file @ doesn't
vee	csb	lib	lib_name_not_entity_declaration_csv	е				contain a module Declaration at line @ Library file @ doesn't
vee	csb	lib	lib_name_not_unit_declaration_csv	е				contain a entity Declaration at line @ Library file @ doesn't contain a unit Declaration
vee	csb	lib	lib_not_contain_supply_csbve	е				at line @ Library does not contain supply @ at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl Desc
vee	csb	loop	initial_value_unknown_loop_csbve	е				While control initial variable @ unassigned.
vee	csb	loop	while_loop_not_assign_stmt_controlvar_csbve	е				Initial value unknown at line @ While loop body does no
								contain an assignment statement for control variable @ at line @
vee	csb	loop	assign_stmt_not_last_while_loop_csbve	е				Assignment statement for control variable @ no last statement in while
vee	csb	loop	undet_init_value_loop_csbve	е				loop at line @ Unable to determine init
vee	csb	loop	undet_limit_loop_csbve	е				value for loop at line @ Unable to determine limi
vee	csb	loop	loop_bounds_calculated_int_csbve	w				for loop at line @  Loop bounds are calculated to be integer
								@, check that this is correct at line @
vee	csb	loop	expr_lhs_contains_var_bit_select_csbve	W				Expression in lhs of assignment contains a variable bit select at line
vee	csb	loop	loop_bounds_not_const_csb	w				@ Loop bounds are non-constant at line @
vee	csb	loop	loop_ctrl_init_expr_not_const_csbve	W				Non-constant loop bound. Loop control
								variable initialization Expression is not a constant Expression at line @
vee	csb	loop	loop_term_expr_not_const_csbve	w				Non-constant loop bound. loop terminating
								Expression could not be evaluated to a constant at line @
vee	csb	loop	init_expr_reset_by_var_csbve	е				Non-constant loop bound. initializing Expression reset by
vee	csb	loop	loop_ctrl_var_1_bit_wide_csbve	w				variable at line @ The loop control variable @ is one bit wide. Check the loop control variable Declaration. at line @
vee	csb	mdb	bad_mdb_net_csbve	е				Bad multi-driven Net @ at line @
vee	csb	mdb	bad_mdb_port_csbve	е				Bad multi-driven Port @ at line @
vee	csb	mdb	bad_mdb_signal_csbve	е				Bad multi-driven Signal @ at line @
vee	csb	mdb	unsupp_comp_mdb_net_csbve	е	?			Unsupported component type @ driving in multi-driven Net name at line @
vee	csb	mdb	unsupp_comp_mdb_port_csbve	е	?			Unsupported component type @ driving in multi-driven Port name a
vee	csb	mdb	unsupp_comp_mdb_signal_csbve	е	?			line @ Unsupported component type @ driving in
								multi-driven Signal name at line @
vee	csb	mdb	unsupp_comp_drive_mdb_csbve	е	?			Unsupported component type @ driving multi-driven Net natne at
vee	csb	mdb	unsupp_comp_drive_mdb_port_csbve	е	?			line @ Unsupported component
								type @ driving multi-driven Port natne at line @
vee	csb	mdb	unsupp_comp_drive_mdb_signal_csbve	е	?			Unsupported component type @ driving
								multi-driven Signal natne at line @
vee	csb	mdb	mdb_net_driven_by_trns_csbve	е				Multiply driven Net driver by transistor primitive type @ at line @
vee	csb	mdb	mdb_port_driven_by_trns_csbve	е				Multiply driven Port driven by transistor primitive type @ at line
vee	csb	mdb	mdb_sig_driven_by_trns_csbve	е				Multiply driven Signal driven by transistor primitive type @ at line @
vee	csb	mdb	mdb_unsupp_comp_drvs_net_csbve	е				Unsupported component type driving Net drives  Net connected to
vee	csb	mdb	mdb_unsupp_comp_drvs_port_csbve	е				multi-driven Net at line @ Unsupported component

Cat	Phase	Typo	Name	W/E	V100F	V2001	Sve vor	Csl	Desc
Cat	гнаѕе	Туре	Name	44/E	v 1993	V Z U U I	Sys_ver	USI	type driving Port drives Port connected to multi-driven Port at line
vee	csb	mdb	mdb_unsupp_comp_drvs_sig_csbve	е					Unsupported component
									type driving Signal drives
									Signal connected to multi-driven Signal at line
									@
vee	csb	mdb	mdb_incompatible_net_drives_multiple_net_csbve	е					Incompatible driver driving tandem Net
									drives Net connected to
vee	csb	mdb	mdb_incompatible_port_drives_multiple_port_csbve	е					multi-driven Net at line @ Incompatible driver
									driving tandem Port drives Port connected to
									multi-driven Port at line
vee	csb	mdb	mdb_incompatible_sig_drives_multiple_sig_csbve	е					@ Incompatible driver
VCC	COD	mab	mab_moompatible_sig_anves_mattple_sig_essive						driving tandem Net
									drives Net connected to multi-driven Port at line
									@
vee	csb	mdb	mdb_unsupp_LHS_concatenation_csbve	е					Unsupported LHS concatenation in
									multi-drive 'device at line
vee	csb	mdb	mdb_bus_has_too_many_drivers_csbve	е					@ Bus has too many
	aah	ماله مد	made always bill drive askyo						drivers. at line @
vee	csb	mdb	mdb_always_blk_drive_csbve	W					Multiple always blocks drive name @ at line @
vee	csb	mdb	nontri_gate_drives_mdb_net_csbve	W					non-tri-state gate drives multi-driven Net at line @
vee	csb	mdb	nontri_gate_drives_mdb_port_csbve	W					non-tri-state gate drives
									multi-driven Port at line @
vee	csb	mdb	nontri_gate_drives_mdb_sig_csbve	w					non-tri-state gate drives
									multi-driven Signal at line @
vee	csb	mem	mem_prts_csve	е					Memories do not support
									part select specifier at line @
vee	csb	mem	ill_ref_mem_name_csv	е					Illegal hid reference to
vee	csb	mem	mem_ref_without_index_csbve	е					memory (name) at line @ Memory @ referenced
									without index through hierarchical ID @ at line
									@
vee	csb	mifc	mifc_not_array_csve	е					Ports may not be an array at line @
vee	csb	mifc	port_identifier_mifc_csbve	е					Port @ at line @
vee	csb	mifc	mifc_mod_input_port_decl_as_reg_csbve	е					Module @ input port @ declared as type reg at
1/00	ooh	mifo	mife enity input part deal on reg cabyo						line @ Entity @ input port @
vee	csb	mifc	mifc_enity_input_port_decl_as_reg_csbve	е					declared as type reg at
vee	csb	mifc	mifc_unit_input_port_decl_as_reg_csbve	е					line @ Unit @ input port @
VCC	COD	111110	milo_dim_input_port_deoi_as_reg_essive						declared as type reg at
vee	csb	mifc	mod_output_wire_redecl_reg_csbve	е					line @ Module @ output port
100	000	111110							re-declared as type reg
									after use as implicitly declared wire at line @
vee	csb	mifc	entity_output_wire_redecl_reg_csbve	е					Entity @ output port
									re-declared as type reg after use as implicitly
vee	csb	mifc	unit_output_wire_redecl_reg_csbve	е					declared wire at line @ Unit @ output port
VCC	CSD	111110	unit_output_wire_redeci_reg_cabve						re-declared as type reg
									after use as implicitly declared wire at line @
vee	csb	mifc	output_port_is_mem_type_mifc_csbve	е					Output port @ is memory
vee	csb	mifc	mifc_inout_port_is_mem_type_csbve	е					type at line @ Inout port @ is memory
									type at line @
vee	csb	mifc	mod_output_port_mismatch_actual_witdh_csbve	W					Module @ output port @ formal to actual width
vee	csb	mifc	ent_output_port_mismatch_actual_witdh_csbve	W					mismatch at line @ Entity @ output port @
vee	CSD	IIIIC	enc_output_port_mismatch_actual_witun_csbve	VV					formal to actual width
vee	csb	mifc	unit_output_port_mismatch_actual_witdh_csb	W					mismatch at line @ Unit @ output port @
	300		os.psps.t_momaton_dotddi_witdii_osb						formal to actual width
vee	csb	mifc	port_name_different_in_upper_lower_case_csbve	е					mismatch at line @ Port name @ different in
	300								upper lower case at line
vee	csb	mifc	port_not_def_in_iodecl_csbve	е					@ Port @ not defined in
vee	csb	mifc	port_not_def_in_portl_csbve	е					ioDeclaration at line @ Port @ not defined in
vee	บอม	TITLE	port_not_uer_in_porti_csbve	₽	1	1	1	1	. Or a not defined it

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	csb	mifc	port_wiredecl_mismatch_csbve	е					port list at line @ Port @ wireDeclaration
			. – – –						mismatch at line @
vee	csb	mifc	pos_based_null_inst_port_csbve	е					Position based null instance port at line @
vee	csb	mifc	last_portdecl_contains_trailcomma_csbve	е					Last portDeclaration contains a trailing
									comma at line @
vee	csb	mins	mins_expr_incompatible_type_csbve	е					Expression @ has an incompatible argument
									type @ with the port at line @
vee	csb	mins	mins_mod_not_exist_csbve	е					Module @ does not exist
vee	csb	mins	mins_entity_not_exist_csbve	е					at line @ Entity @ does not exist
vee	csb	mins	mins_unit_not_exist_csbve	е					at line @ Unit @ does not exist at
									line @
vee	csb	mins	undefined_instance_csbve	е					Undefined instance @ at line @
vee	csb	mod	mod_param_bad_number_csv	е					Module name @ parameter list contains
									an Incorrect number of
									parameter overrides at line @
vee	csb	mod	mod_entity_param_bad_number_csv	е					Entity name @ parameter list contains
									an Incorrect number of
									parameter overrides at line @
vee	csb	mod	mod_unit_param_bad_number_csv	е					Unit name @ parameter list contains an Incorrect
									number of parameter
vee	csb	mod	ill_mod_name_csbve	е					overrides at line @ Illegal module @ at line
									@
vee	csb csb	mod mod	ill_mod_entity_name_csbve ill_mod_unit_name_csbve	e					Illegal entity @ at line @ Illegal unit @ at line @
vee	csb	mod	mod_mult_decl_string_csbve	е					Multiple Declarations of string detected in module
									@ at line @
vee	csb	mod	mod_entity_mult_decl_string_csbve	е					Multiple Declarations of string detected in entity
vee	csb	mod	mod_unit_mult_decl_string_csbve	е					@ at line @ Multiple Declarations of
VCC	CSD	illou	mod_driit_mait_deci_striitg_csbve						string detected in unit @
vee	csb	mod	mod_mult_def_csbve	е					at line @ Module @ defined in
vee	csb	mod	mod_ent_mult_def_csbve	е					multiple places at line @ Entity @ defined in
									multiple places at line @
vee	csb	mod	mod_unit_mult_def_csbve	е					Unit @ defined in multiple places at line @
vee	csb	mod	mod_no_module_found_csbve	е					No modules found at line @
vee	csb	mod	mod_no_entity_found_csbve	е					No entity found at line @
vee	csb csb	mod mod	mod_no_unit_found_csbve failed find mod csbve	e					No unit found at line @ Failed to find module @
vee	csb	mod	failed_find_entity_csbve	е					at line @ Failed to find entity @ at
									line @
vee	csb	mod	failed_find_unit_csbve	е					Failed to find unit @ at line @
vee	csb	mod	undefined_mod_csbve	е					Undefined module @ at line @
vee	csb	mod	undefined_ent_csbve	е					Undefined entity @ at
vee	csb	mod	undefined unit csbve	е					line @ Undefined unit @ at line
									@
vee	csb	mod	unexpandable_macromodule_csbve	е					Unexpandable macromodule @ at line
vee	csb	mod	non_interconnect_in_hierarchical_mod_csbve	е					@ Non interconnect in
	300								hierarchical module @ at
vee	csb	mod	non_interconnect_in_hierarchical_ent_csbve	е					line @ Non interconnect in
									hierarchical entity @ at line @
vee	csb	mod	non_interconnect_in_hierarchical_sig_csbve	е					Non interconnect in
L								L	hierarchical signal @ at line @
vee	csb csb	mod mod	empty_mod_csbve empty_ent_csbve	e e					Empty module at line @ Empty entity at line @
vee	csb	mod	empty_unit_csbve	е					Empty unit at line @
vee	csb	net	namereg_not_on_LHS_stmt_net_csv	е					Register @ cannot be used on LHS of this
									assignment statement at line @
vee	csb	net	net_implicit_wire_redecl_reg_csbve	е					Implicitly declared as a
									wire @ re-declared as a

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	csb	net	time var decl csbve	е					reg @. at line @ Time variable @
									declared at line @
vee	csb	net	time_var_bit_used_csbve	е					Time variable @ bit used at line @
vee	csb	net	undecl_net_in_mod_csbve	е					Undeclared net @ in module @ at line @
vee	csb	net	undecl_port_in_mod_csbve	е					Undeclared port @ in module @ at line @
vee	csb	net	undecl_sig_in_mod_csbve	е					Undeclared signal @ in
vee	csb	net	undecl_net_in_ent_csbve	е					module @ at line @ Undeclared net @ in
vee	csb	net	undecl_port_in_ent_csbve	е					entity @ at line @ Undeclared port @ in
vee	csb	net	undecl_sig_in_ent_csbve	e					entity @ at line @ Undeclared signal @ in
									entity @ at line @
vee	csb	net	undecl_net_in_sig_csbve	е					Undeclared net @ in signal @ at line @
vee	csb	net	undecl_port_in_sig_csbve	е					Undeclared port @ in signal @ at line @
vee	csb	net	undecl_sig_in_sig_csbve	е					Undeclared signal @ in signal @ at line @
vee	csb	net	port_used_prior_to_decl_csbve	е					Port @ used prior toDeclaration at line @
vee	csb	net	1bit_with_prts_csbve	е					1-bit with part select at
vee	csb	netd	ill_decl_vec_csbve	е					line @ Illegal Declaration of
vee	csb	nett	nett_ill_reg_name_csbve	е					vector @ at line @ Illegal register @ at line
vee	csb	nett	nett_ill_net_name_csbve	е					@ Illegal net @ at line @
vee	csb	nett	nett_ill_port_name_csbve	е					Illegal port @ at line @
vee	csb csb	nett	nett_ill_signal_name_csbve net_scalar_vect_nett_csbve	e					Illegal signal @ at line @ Net declared as both
									scalar and vector at line @
vee	csb	nett	port_scalar_vect_nett_csbve	е					Port declared as both scalar and vector at line
									@
vee	csb	nett	signal_scalar_vect_nett_csbve	е					Signal declared as both scalar and vector at line
vee	csb	nett	hot_mux_not_use_bus_connection_net_csbve	е					@ One hot mux can not be
									used for bus connection between modules Net @
1/00	aab	2044	hot mux not use bus connection port csbve						at line @ One hot mux can not be
vee	csb	nett	not_max_not_use_bus_connection_port_csbve	е					used for bus connection
									between modules Port @ at line @
vee	csb	nett	hot_mux_not_use_bus_connection_sig_csbve	е					One hot mux can not be used for bus connection
									between modules Signal @ at line @
vee	csb	nett	reg_connected_inst_inout_csbve	е					Reg @ connnected to instantiation @ inout @
									at line @
vee	csb	nett	ill_net_in_proc_assn_csbve	е					Illegal net type type in procedural assignement
vee	csb	nett	ill_port_in_proc_assn_csbve	е					at line @ Illegal port type type in
									procedural assignement at line @
vee	csb	nett	ill_sig_in_proc_assn_csbve	е					Illegal signal type type in procedural assignement
									at line @
vee	csb	num	not_allowed_width0_num_csbve	е					Width 0 not allowed for sized number at line @
vee	csb	num	real_num_not_allowed_csbve	е					Real numbers not allowed at line @
vee	csb	num	found_x_z_in_num_literal_csbve	е					Found x and/or z value in number literal at line @
vee	csb	num	too_many_digits_in_sized_num_csbve	w					Number of digits exceeds the width in a sized
									number at line @
vee	csb csb	num num	divide_by_zero_num_csbve child_mod_inst_parent_mod_csbve	e e					Divide by zero at line @ Child module @
									instantiates parent module @ at line @
vee	csb	num	child_ent_inst_parent_ent_csbve	е					Child entity @ instantiates entity module
1/0-	cak	D	shild sig inst perset -i	-					@ at line @ Child signal @
vee	csb	num	child_sig_inst_parent_sig_csbve	е					instantiates signal
vee	csb	num	int_decl_incorrect_csbve	е					module @ at line @ Integer Declaration
vee	csb	num	int_var_indexed_csbve	е					incorrect at line @ Integer variable inedexed
	300								at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	csb	parm	parm_redecl_as_reg_name_csv	е					Parameter re-declared as reg @ at line @
vee	csb	parm	parm_redecl_as_port_port_csv	е					Parameter re-declared as port @ at line @
vee	csb	parm	parm_redecl_as_net_name_csv	е					Parameter re-declared as Net @ at line @
vee	csb	parm	parm_redecl_as_port_name_csv	е					Parameter re-declared
vee	csb	parm	parm_redecl_as_signal_name_csv	е					as Port @ at line @ Parameter re-declared
vee	csb	parm	duplicate_decl_parm_name_csv	е					as Signal @ at line @ Duplicate declaration of
		·							parameter name @ at line @
vee	csb	parm	ill_parm_identifier_csbve	е					Illegal parameter @ at line @
vee	csb	parm	value_of_parm_OS_platform_dependent_csbve	w					Parameter select width >
									32. The value is OS and platform dependent at
vee	csb	parm	parm_redefined_csbve	W					line @ Parameter @ redefined
vee	csb	pars	endfunction_miss_cyb_csv	е					at line @ Endfunction missing at
		•							line @
vee	csb	pars	endtask_miss_pars_csv	е					Endtask missing at line @
vee	csb	pars	endmodule_miss_pars_csv	е					Endmodule missing at line @
vee	csb	pars	miss_cont_assign_pars_csv	е					Missing = sign for continuous assignment
vee	csb	pli	user_syst_not_listed_in_pli_table_csbve	е					at line @ User system task @ is
VCC	CSD	Pii	user_syst_not_nsteu_m_pn_table_csbve						not listed in PLI table at
vee	csb	port	ill_formal_port_name_csbve	е					line @ Illegal formal port @ at
vee	csb	pp	text_redefined_replaced_csbve	W					line @ Text macro redefined
									and replaced @. Previous definition
									filename, line number @ New definition filename,
									line number @ at line @
vee	csb	pp	undefined_macro_csbve	е					Undefined macro @ at line @
vee	csb	pp	include_file_contains_nonconst_csbve	е					Include file contains non constant @ at line @
vee	csb	pp	endif_or_else_without_ifdef_csbve	е					Endif-or-else-without ifdef at line @
vee	csb	prim	z_in_prim_inst_csbve	е					z in primitive instantiation at line @
vee	csb	prim	prim_instan_csbve	е					Primitive instantiation @
vee	csb	proc	proc_blk_missing_evc_csbve	е					at line @ Always block missing
vee	csb	prts	prts_out_of_range_csbve	е					event control at line @ Parameter @[@ : @]part
									select is out of range at line @
vee	csb	prts	ill_prts_inst_array_csbve	е					Illegal value for part select of instance array
									'name' at line @
vee	csb	prts	const_prts_contains_non_const_selector_csbve	е					Constant part select @ contains a non-constant
vee	csb	prts	bus_index_prts_for_var_out_of_range_csbve	е					selector @ at line @ Bus index @ integer of
									part select [@:@] for variable @ out of range
vee	csb	prts	bus_prts_for_var_out_of_range_csbve	е					at line @ Bus part select [@:@] for
100	000	pito	546_p16_161_vai_64t_61_14t1g6_66546						variable @ out of range at line @
vee	csb	prts	bus_prts_index_out_of_name_for_var_csbve	е					Bus part select [@:@]
									index @ out of range for variable @ at line @
vee	csb	prts	ill_token_in_prts_csbve	е					Illegal token in part select @ at line @
vee	csb	prts	incomplete_prts_specification_csbve	е					Incomplete part select specification @ at line @
vee	csb	prts	ill_index_in_prts_csbve	е					Illegal index in part select @ at line @
vee	csb	prts	negative_index_in_prts_not_allowed_csbve	е					Negative index in part
									select @ not allowed at line @
vee	csb	prts	prts_index_order_reversed_csbve	е					Part select index order reversed [@ : @] [@ : @]
									should be [@ : @] at line @
vee	csb	prts	index_vec_over_max_size_csbve	w					Vector index @ exceeds the size of the vector.
V00	cch	nrto	v or z in voc hit coloct index cohve						Index truncated at line @
vee	csb	prts	x_or_z_in_vec_bit_select_index_csbve	е					index at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	csb csb	real real	real_csbve real_in_assn_csbve	e e			•		Real @ at line @ Real @ in assignement
vee	CSD	icai	real_iii_assii_csbve	6					at line @
vee	csb	real	real_in_csi_csbve	е					Real @ inCase item at line @
vee	csb	real	real_in_comparaison_csbve	е					Real @ in comparaison
vee	csb	rel	ill_rel_obj_type_csbve	е					at line @ Illegal release object type
			<i>,</i> _ · · · _						type at line @
vee	csb	scop	var_erd_in_scope_csbve	е					Variable @ redfined in scope @ at line @
vee	csb	simr	inefficient_op_not_a_power_of_2_csbve	е					Division/modulus by a number not a power of 2.
									Inefficient simulation
vee	csb	simr	simr_multiple_init_blk_force_csbve	w					operation. at line @ Multiple initial blocks
	002	<b></b>	5	"					force @. Unpredictable
									simulation result at line @
vee	csb	snsl	incomplete_snsl_csbve	W					Incomplete sensitivity list.  @ is not in the sensitivity
									list. at line @
vee	csb	snsl	edge_sns_process_contains_data_pin_snsl_csbve	е					Edge sensitive process contains a data pin @ in
									the sensitivity list at line
vee	csb	snsl	unsupp_expr_in_snsl_csbve	W					@ Unsupported Expression
									type @ in sensitivity list '
vee	csb	snsl	always_blk_is_miss_snsl_csbve	е					at line @ Always block is missing
vee	csb	snsl	not all bits snsvar used csb	е					sensitivity list at line @ Not all bus bits of
VCC	CSD	31131	Hot_all_bits_shsval_useu_csb						sensitivity variable @ are
vee	csb	snsl	partial bus decl width csbve	е	?				used in process at line @ partial bus @ declared
			F						with width @ width @ at
vee	csb	snsl	contains_inst_name_csbve	е					line @ Contains instance name
vee	csb	snsl	bus_indexed_in_snsl_csbve	е					@ at line @ Bus @ indexed in
vee	CSD	51151	bus_indexed_in_shsi_csbve	е					sensitivity list at line @
vee	csb	stmt	ill_register_assign_csv	е					Illegal register assignment statement at
									line @
vee	csb	stmt	null_not_allowed_stmt_csbve	е					Null statement is not allowed here at line @
vee	csb	stmt	id_expected_FHSexpr_force_stmt_csbve	е					Simple identifier expected for LHS
									Expression in
vee	csb	stmt	id_expected_FHSexpr_release_stmt_csbve	е					force-statement at line @ Simple identifier
100	000	Ottill	id_oxposiod_i i ioxxpi_iologoo_otiiit_oobvo						expected for LHS
									Expression in release-statement at line
V00	cch	stmt	stmt ill accept only net reg mem csbve	0					@ Illegal type @ can only
vee	csb	Still	stint_iii_accept_only_net_reg_mem_csbve	е					accept net, reg, memory
vee	csb	stmt	stmt ill accept only port reg mem csbve	е					at line @ Illegal type @ can only
100	000	Ottill	ouni_iii_dosopi_oniy_pori_rog_iiioiii_cosvo						accept port, reg, memory
vee	csb	stmt	stmt_ill_accept_only_signal_reg_mem_csbve	е					at line @ Illegal type @ can only
									accept signal, reg, memory at line @
vee	csb	stmt	while_stmt_usage_disc_csbve	W					While statement usage
vee	csb	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_csbve	е					discouraged at line @ Arithmetic operator RHS
VCC	CSD	Stillt	antimetto_op_ms_one_less_bit_than_ms_csbvc						has one less bit than the
vee	csb	stmt	ar_op_unequal_lhs_rhs_csbve	е					LHS at line @ Arithmetic operator
									unequal width LHS and
vee	csb	stmt	ar_op_unequal_var_on_rhs_csb	е					RHS at line @ Arithmetic operator
									unequal width variables @ on RHS at line @
vee	csb	stmt	empty_stmt_csb	е					Empty-statement at line
vee	csb	syst	ill_syst_task_arg_csbve	е					@ Illegal system task @
			_; <del>5</del> _					.,	Argument @ at line @
vee	csb	syst	csdir_converts_syts_csbve	W				Х	Lower case converts the system task \$realtime
									return value to an integer at line @
vee	csb	syst	return_var_of_user_used_as_rhs_csbve	w					Return variable of user
									system task is used as a RHS variable at line @
vee	csb	task	miss_task_name_stmst_body_csv	е					Task @ body statement
vee	csb	task	ill_task_csv	е					missing at line @ Illegal task @ at line @
vee	csb	task	ill_use_task_csbve	е					Illegal use of task @ at
					1				line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ve	er Csl	Desc
vee	csb	task	ask_var_not_decl_csbve	е					Variable @ used but not
vee	csb	task	task_not_defined_csbve	е					declared at line @ Task @ not defined at line @
vee	csb	task	too_few_arg_to_task_csbve	е					Too few arguments passed to task @ at line
vee	csb	task	undefined_task_csbve	е					@ Undefined task @ at line @
vee	csb	task	syts_output_port_drvs_nonsqs_logic_comp_csbve	w					User system task output port drives
vee	csb	task	undefioned_task_	е					non-sequential logic component at line @ Undefined task @ at line
vee	csb	task	task_decl_error_veve	е					@ Task declaration error at
vee	csb	task	func_task_parm_csbve	е					line @ Found function
vee	csb	task	unmatched_task_param_csbve	е					parameter @ at line @ Unmatched task parameter @ at line @
vee	csb	tbcd	found_forever_tbcd_csbve	е					Found forever at line @
vee	csb	tbcd	behavioral_code_mod_csbve	е					Behavioral code in
vee	csb	tbcd	behavioral_code_ent_csbve	е					module @ at line @  Behavioral code in entity @ at line @
vee	csb	tbcd	behavioral_code_unit_csbve	е					Behavioral code in unit @ at line @
vee	csb	tri	instance_not_tri_state_device_csbve	е					Instance name is not a tri-state device at line @
vee	csb	tri	unsupp_gate_type_tristate_csbve	е					Unsupported gate type @ used for tristate at line @
vee	csb	tri	tri_not_desgn_gate_contention_csbve	е					Tristate not designed correctly gate @ can cause contention at line @
vee	csb	tri	unsupp_type_instance_tri_csbve	е					Unsupported type instance type used for tristate @ at line @
vee	csb	tri	incorrect_cont_assign_stmt_tri_gate_csbve	е					Incorrect continuous assign statement for tristate gate @ at line @
vee	csb	tri	const_assign_to_multidriven_net_csbve	е					Constant (constiznt) assigned to multi-driven Net @ at line @
vee	csb	tri	const_assign_to_multidriven_port_csbve	е					Constant (constiznt) assigned to multi-driven
vee	csb	tri	const_assign_to_multidriven_signal_csbve	е					Port @ at line @ Constant (constiznt) assigned to multi-driven Signal @ at line @
vee	csb	tri	unsupp_expr_for_tri_csbve	е					Unsupported Expression type @ for tristate at line @
vee	csb	unsy	cs_equality_op_csbve	е					Case equality operator == at line @
vee	csb	unsy	deassign_stmt_csbve	е					Deassign statement at line @
vee	csb csb	unsy	defparam_csbve dely_ctrl_csbve	e					Defparam at line @ Delay control at line @
vee	csb csb	unsy	ev_ctrl_csbve time_decl_csbve	e e					Event control at line @ Time Declaration at line
VCC	CSD	unsy	time_deci_csbve	-					@
vee	csb csc	unsy assn	wait_stmt_unsy_csbve x_in_rhs_of_assihnment_cscve	e e					Wait statement at line @ x in rhs of assignment at
vee	CSC	assn	z_in_rhs_of_assn_default_csi_cscve	е					line @ x in rhs of assignement in defaultCase item at
vee	CSC	assn	z_in_rhs_of_assn_cscve	е					line @ z in rhs of assignement at line @
vee	csc	assn	unequal_length_lhs_rhs_cscve	е					Unequal length LHS and RHS at line @
vee	csc	assn	unequal_length_lhs_rhs_off_one_bit_cscve	е					Unequal length LHS and RHS off by one bit at line
vee	CSC	blk	blk_ill_block_id_csve	е					Illegal block @ at line @
vee	CSC	blk	nonblocking_assign_in_comb_always_blk_cscve	е					Non blocking aasignment
vee	CSC	blk	seq_blk_contains_blk_assn_cscve	е					in combinational always block at line @ Sequential block
vee	csc	casn	LHS_not_reg_casn_csve	е					contains blocking assignement at line @ LHS cannot be a register
vee	csc	ccd	ccd_cdir_must_be_cst_expr_cscve	е				х	@ at line @  CSL directive size must be constant Expression
vee	CSC	clk	clk_name_not_found_cdir_cscve	е				Х	at line @ Clock name not found in
									· · · · · · · · · · · · · · · · · · ·

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_v	er Csl	
vee	CSC	clk	expr_sunj_to_different_clk_phases_cscve	е					cslc directive at line @ Expression subject to different clock phases at line @
vee	CSC	cmdl	cannot_use_librescan_with_liborder_specified_cscve	е					Cannot use +librescan when +liborder has already been specified at line @
vee	CSC	cmdl	cannot_use_liborder_with_librescan_specified_cscve	е					Cannot use +liborder when +librescan has already been specified at line @
vee	csc	cond	if_case_question_cond_cscve	е					If/case conditional expression expr syntax error at line @
vee	csc	cond	if_no_else_in_comb_blk_cscve	е					If no else in combinational block at line @
vee	CSC	csi	xcsi_not_in_casex_cscve	е					xCase item not in casex at line @
vee	CSC	csi	noncnst_csi_cscve	е					Non-constantCase item @ at line @
vee	CSC	csi	noncnst_dely_cscve	е					Non-constant delay @ at line @
vee	CSC	csi	noncstn_rep_in_conc_cscve	е					Non-constant repeator in concatenation at line @
vee	CSC	CSS	sns_pragma_full_case_cscve	е					Assume a full case, missing default or synopsys pragma full case, at line @
vee	CSC	cyb	repeat_in_delay_cyb_csve	е					Repeat clause in delay not supported at line @
vee	csc	cyb	repeat_in_event_control_cyb_csve	е					Repeat clause in event control not supported at line @
vee	csc	cyb	event_id_not_supportedcyb_csve ill_proc_assign_cyb_csve	e					@ event id is not supported at line @ Illegal procedural
vee	csc	cyb							continuous assignment statement at line @
vee	CSC	cyb	ill_deassign_cyb_csve	е					Illegal de-assign statement at line @
vee	CSC	cyb	ill_force_cyb_csve	е					Illegal force statement at line @
vee	CSC	cyb	ill_release_cyb_csve	е					Illegal release statement at line @
vee	CSC	cyb	repeat_as_delay_cyb_csve	е					Repeat as delay not supported at line @
vee	CSC	cyb	repeat_as_event_control_cyb_csve	е					Repeat as event control not supported at line @
vee	CSC	cyb	wait_statement_not_cyb_csve	е					Wait statement is not supported at line @
vee	CSC	cyb	disable_statement_not_cyb_csve	е					Disable statement is not supported at line @
vee	CSC	cyb	events_not_supported_cyb_csve	е					Events are not supported at line @
vee	CSC	cyb	fork_join_blocks_not_supported_cyb_csve	е					Fork/join blocks are not supported at line @
vee	CSC	cyb	unsupp_function_return_time_cyb_csve	е					Unsupported function return time at line @
vee	CSC	cyb	not_supp_events_cyb_csve	е					Events are not supported at line @
vee	CSC	cyb	repeat_in_delay_or_event_cyb_csve	е					Repeat clause in delay or Event control at line @
vee	CSC	cyb	ill_proc_cont_assign_stmt_cyb_csve	е					Illegal procedural continuous assignment statement at line @
vee	CSC	cyb	ill_deassign_cyb_stmt_csve	е					Illegal de-assign statement at line @
vee	CSC	cyb	ill_force_stmt_cyb_csve	е					Illegal force statement at line @
vee	CSC	cyb	ill_release_stmt_cyb_csve	е					Illegal release statement at line @
vee	CSC	cyb	repeat_not_supp_as_delay_or_event_cyb_csve	е					Repeat as delay or event control not supported at line @
vee	CSC	cyb	not_supp_wait_stmt_cyb_csve	е					Wait statement is not supported at line @
vee	CSC	cyb	not_supp_disable_stmt_cyb_csve	е					Disable statement is not supported at line @
vee	csc	cyb	supp_not_events_cyb_csve	е					Events are not supported at line @
vee	csc	cyb	not_supp_fork_join_blocks_cyb_csve	е					Fork/join blocks are not supported at line @
vee	CSC	cyb	not_supp_UDP_cyb_csve	е					UDPs are not supported at line @
vee	CSC	cyb	not_supp_defparam_cyb_csve	е					Defparam is not supported at line @
vee	CSC	cyb	specify_blk_not_supported_cscve	е					Specify blocks are not supported at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	CSC	cyb	mintypmax_expr_not_supp_cscve	W					mintypmax Expressions are not supported at line @
vee	csc	decl	decl_array_over_max_size_cscve	е					Array @ exceeds maximum size limit at line @
vee	CSC	dely	max_val_dly_csve	е					Too many delay values, max @ at line @
vee	CSC	dely	found_gate_dely_not_allowed_cscve	е					Found gate delay which
vee	CSC	dely	found_dely_in_casn_not_allowed_cscve	е					are not allowed at line @ Found delay in
									continuous assignment which are not allowed at line @
vee	CSC	dely	dely_ignoring_dely_specification_cscve	е					Delay Ignoring delay specification in Net Declaration at line @
vee	CSC	dely	dely_ignoring_dely_specification_port_cscve	е					Delay Ignoring delay specification in Port
vee	CSC	dely	dely_ignoring_dely_specification_sig_cscve	е					Declaration at line @  Delay Ignoring delay specification in Signal
vee	CSC	dely	dely_ignoring_dely_before_stmt_cscve	е					Declaration at line @ Delay Ignoring delay before statement at line @
vee	CSC	dely dely	x_or_z_in_dely_cscve non_int_dely_cscve	e e					x or z in delay at line @ Non integer delay at line @
vee	CSC	dmsn	mem_prts_index_out_of_range_for_mem_cscve	е					Memory part select [@:@] index @ out range for memory @ at line @
vee	csc	dmsn	dime_select_for_mem_missing_cscve	е					Select for memory @
vee	CSC	dmsn	dime_index_out_of_bounds_for_mem_cscve	е					missing at line @ Index <index> out of</index>
vee	csc	dmsn	dime_prts_out_of_bounds_for_net_cscve	е					bounds for memory @. Range [@: @] at line @ Part select [@: @] out of bounds for net @. Range
vee	csc	dmsn	dime_prts_out_of_bounds_for_port_cscve	е					[@ : @] at line @ Part select [@ : @] out of bounds for port @.
vee	CSC	dmsn	dime_prts_out_of_bounds_for_sig_cscve	е					Range [@ : @] at line @ Part select [@ : @] out of
									bounds for signal @. Range [@ : @] at line @
vee	csc	dmsn	dime_prts_reg_cscve	е					Part select [@ : @] reg @. Range [@ : @] at line @
vee	csc	drvc	incompatible_drvc_for_net_cscve	е					Incompatible drivers for Net @ at line @
vee	csc	drvc	incompatible_drvc_for_port_cscve	е					Incompatible drivers for Port @ at line @
vee	csc	drvc	incompatible_drvc_for_sig_cscve	е					Incompatible drivers for Signal @ at line @
vee	CSC	drvc	drvc_multiple_drive_net_partially_overlap_cscve	е					Multiple drive Net partially overlap at line @
vee	CSC	drvc	drvc_multiple_drive_port_partially_overlap_cscve	е					Multiple drive Port partially overlap at line @
vee	CSC	drvc	drvc_multiple_drive_sig_partially_overlap_cscve	е					Multiple drive Signal partially overlap at line @
vee	CSC	dsgn	dsgn_top_mod_cannot_id_cscve	е					Top module @ cannot be
vee	CSC	dsgn	dsgn_top_entity_cannot_id_cscve	е					Top entity @ cannot be
vee	CSC	dsgn	dsgn_top_unit_cannot_id_cscve	е					identified at line @ Top unit @ cannot be
vee	CSC	dsgn	unit_dsgn_cycle_not_spanning_tree_cscve	е					identified at line @ Unit design hierarchy
									contains a cycle. Hierarchy is not a spanning tree. at line @
vee	CSC	evc	not_allowed_edge_trigger_cscve	е					Edge trigger is not allowed in this location at line @
vee	csc	evc	ectl_in_assn_cscve	е					Event control in assignement at line @
vee	csc	expr	const_expr_nm_var_vecsc	е					Constant Expression contains variable @ at line @
vee	csc	expr	const_expr_usage_vecsc	е					Constant Expression usage at line @
vee	CSC	expr	expr_prts_indices_1bit_var_cscve	е					Part select indices 1-bit variable at line @
vee	CSC	expr	expr_prts_must_be_cst_expr_cscve	е					Part select specifier Expression must be constant Expression at
vee	CSC	expr	not_const_expr_cscve	е					line @ Repetition multiplier in
									concatenation is not a

Page	Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
ve csc expr equality operator, detected, desire e descriptions and the second control of								, _		
Vec   GSC   Sept	vee	CSC	expr	ill_bit_select_expr_cscve	е					
Vee         GSC         expr         notequal_operator_lesched_closeve         e         ductor_lesched_closer_lesched_closeve           Vee         GC         expr         III_parm_value_closeve         e         decleted_at late in expending_closeve           Vee         GC         expr         int_operand_not_t_bill_closeve         v         Reposition multiplier in concatenation is not a constant Expression at concatenation is not a constant Expression at concatenation is not a constant Expression at concatenation is not a concatenation in the concatenation is not at late expression at the concatenation is not at late expression at the concatenation is not at late expression at the concatenation at late expression at l	vee	CSC	expr	equality_operator_detected_cscve	е					Use of operator ===
Vee         CSC         expr         III. parm. value, assore         e         III. parameter value at line 0 inc.	vee	CSC	expr	notequal_operator_detected_cscve	е					Use of operator !==
vee         csc         expr         repetition_multiplier_int_conc_nut_const_expr_csove         w         Repetition multiplier in not a constant fagterssion at the constant fagterssion at the constant fagterssion at the constant fagterssion at the constant fagters and an integer operands instead of 1-bit operands instead operands instead operands instead operand	vee	CSC	expr	ill_parm_value_cscve	е					Illegal parameter value at
Vale         CSC         expr         Int_operand_not_1_bit_csove         w         constant Expression at land sine @ network of she will all sine @ network of she will be she w	vee	CSC	expr	repetition_multiplier_in_conc_not_const_expr_cscve	w					Repetition multiplier in
Vee         SSC         expr         Int_operand_not_1_bit_csove         W         Logic operator has integer operands instead of 1-bit operands integer operands instead of 1-bit operands instead of 1-bit operands integer operands in 1-bit operands in 1-bit operands integer operands in 1-bit opera										constant Expression at
vee   csc   expr	vee	CSC	expr	int_operand_not_1_bit_cscve	w					Logic operator has
vee         cac         expr         unsupp_oxpc_cscve         w         Unsupported Expression speed at line @ Unsupported operator speed of the word of any and any and any any and any any and any										of 1-bit operands at line
Vee         csc         expr         unsupp.operator_csove         w         Unsupported operator type & at line 8           vee         csc         expr         use_of_sg_bit_const_csove         w         Use of single bit constant type & at line 8           vee         csc         expr         unary_op_in_comparison_csove         e         unary_op_in_comparison_csove           vee         csc         expr         nonconst_repeator_in_conc_csove         e         Non-constant repeator in concatention at line 9           vee         csc         expr         X_OT_z_in_cond_expr_csove         e         X_OT_z in_conditional expression at line 9           vee         csc         expr         expr_in_end_port_dir_csove         e         Expression at line 9           vee         csc         expr         expr_in_ent_port_dir_csove         e         Expression at line 9           vee         csc         expr         expr_in_ent_port_dir_csove         e         Expression at line 9           vee         csc         expr         expr_in_ent_port_dir_csove         e         Expression at line 9           vee         csc         expr         expr_in_ent_port_dir_csove         e         Expression at line 9           vee         csc         expr         expr_in_ent_port_dir_c	vee	CSC	expr	unsupp_expr_cscve	W					Unsupported Expression
vec         csc         expr         use_of_sqb_bit_const_cseve         w         Use of single bit const           vec         csc         expr         unany_op_in_comparison_cseve         e         Unary op used in comparison at line @ Non constant repeator in comparison at line @ Non constant repeator in comparison at line @ Non constant repeator in concatenation at line @ Non constant repeator in concatenation at line @ Yee         e         xor constant repeator in comparison at line @ Yee         xor constant repeator in concatenation at line @ Yee         xor concatenation at line @	vee	CSC	expr	unsupp_operator_cscve	w					Unsupported operator
Vee         csc         expr         unay_op_in_comparison.cscve         e         Unary op used in comparison at line @ concatent at line	vee	CSC	expr	use_of_sg_bit_const_cscve	w					Use of single bit constant
Vee         csc         expr         nonconstrapeator_in_conc_escve         e         Non constant repeator in concentration at line @ concentration at line @ systems and a system and a sys	vee	CSC	expr	unary_op_in_comparison_cscve	е					Unary op used in
Vec   CSC   Expr   X_0r_Z_in_cond_expr_cscve   e   X or z in conditional expression at line @ Xero_in_rep_in_conc_cscve   e   Zero repeator in concatenation at line @ Xero_in_rep_in_conc_cscve   e   Zero repeator in concatenation at line @ Xero_in_rep_in_en_rep_in_cscve   e   Zero repeator in concatenation at line @ Xero_in_rep_in_en_rep_in_cscve   e   Zero repeator in concatenation at line @ Xero_in_rep_in_en_rep_in_en_rep_in_expr_cscve   e   Zero_in_rep_in_en_rep_in_en_rep_in_expr_en_rep_in_e	vee	CSC	expr	nonconst_repeator_in_conc_cscve	е					Non constant repeator in
vee         csc         expr         zero_in_rep_in_conc_cseve         e         Zero repeator in concentation at line @ concentation at line @ Expression @ in module wee         concentation at line @ Expression @ in module in ite @ Expression @ in ord ord in at line @ Expression @ in ord ord in at line @ Expression @ in ord ord in at line @ Expression @ in ord ord in at line @ Expression @ in ord ord in at line @ Expression @ in ord ord in at line @ Expression @ in ord ord in at line @ Expression @ in inst to well at line @ Expression @ in inst to well expression @ in inst to well at line @ Expression @ in inst to well at line @ Institute @ Institu	vee	CSC	expr	x_or_z_in_cond_expr_cscve	е					
vee         csc         expr         expr.in.mod.port.dir_cscve         e         Expression @ in module port dir at line @ Expression @ in module port dir at line @ Expression @ in entity port dir at line @ Expression @ in entity port dir at line @ Expression @ in entity port dir at line @ Expression @ in entity port dir at line @ Expression @ in entity port dir at line @ Expression @ in insi il @ Expression & Exp	vee	CSC	expr	zero in rep in conc cscve	е					
ve         csc         expr         expr.in_ent_port_dir_cscve         e         Expression @ in entity port dir at line @ Expression @ in unit port dir at line @ Expression @ in unit port dir at line @ Expression @ in unit port dir at line @ Expression @ in unit port dir at line @ Expression @ in insi ti @ at line @ Expression @ in insi ti @ at line @ Expression @ in insi ti @ at line @ Expression @ in insi ti @ at line @ Expression @ in insi ti @ at line @ Expression @ in insi ti @ at line @ Expression @ in insi ti @ at line @ Expression gine in insi ti @ at line @ Expression gine in insi ti @ at line @ Expression gine in insi ti @ at line @ Expression gine in insi ti @ at line @ Expression gine in insi ti @ at line @ Expression gine in insi ti @ at line @ Expression gine in insi ti @ at line @ Expression gine in insi ti @ at line @ Expression gine in insi ti @ at line @ Expression gine in insi ti @ at line @ Expression gine in insi ti @ at line @ Expression gine in insi ti @ at line @ Expression gine in insi ti @ at line @ Expression gine in insi ti @ at line @ Expression gine in insi ti @ at line @ Expression gine in insi ti @ at line @ Expression gine in insi ti @ at line @ Expression gine in insi ti @ Expression gine in insi ti @ at line @ Is at line	vee	CSC			е					concatenation at line @
vee   csc   expr   expr_in_sig_port_dir_cscve   e   Expression @ to instit or dir at tine @ to instit or dir at tine @ to instit or at tine @ to perands @ unequal length at tine @ to perands @ tine @				. – – – –						port dir at line @
vee         csc         expr         expr.in_inst_cscve         e         Expression @ st. pression operator           vee         csc         expr         expr_operator_operands_unequal_length_cscve         e         Expression operator @ operands @ unequal length at line @ toperands @ unequal length at line @ unequ			·							port dir at line @
At line @ Expression operator @ operands @ unequal lenght_cscve e	vee	CSC	-	. – – 5–	е					dir at line @
vee csc file mismatch_ent_file_name_cscve e Mismatch between nignal name @ at line @ vee csc func func_arg_miss_vecsc e e mill_func_cscve e lill_func_cscve e lill_func_ine dilline @ at line @ vee csc func func_not_define_cscve e lill_func_cscve e lill_func_cscve e lill_func_name e lill_func_name e lill_func_cscve e lill_func_name e lill_func_ine e lill_func_name e lill_func_ine e lill_func_ine e lill_func_name e lill_func_ine e lill_func_ine e lill_func_ine e lill_func_name e lill_func_ine e lill_func_name e li	vee	CSC	expr	expr_in_inst_cscve	е					at line @
vee         csc         file         cannot_open_filter_specification_file_escve         e         Cannot_open filter specification file at line ged ged at line ged ged at line ged ged at line ged ged ged ged ged ged ged ged ged ge	vee	CSC	expr	expr_operator_operands_unequal_lenght_cscve	е					operands @ unequal
vee   csc   file   filter_specification_file_missing_cscve   e     Filter specification file   name @ is missing at line @	vee	CSC	file	cannot_open_filter_specification_file_cscve	е					Cannot open filter
vee csc file mismatch_mod_file_name_cscve e Mismatch_between module name @ and file name @ at line @ mismatch_ent_file_name_cscve e Mismatch between module name @ and file name @ at line @ Mismatch between entity name @ at line @ Mismatch between signal name @ at line @ Mismatch between signal name @ at line @ Mismatch between signal name @ and file name @ at line										. @
vee         csc         file         mismatch_mod_file_name_cscve         e         Mismatch between mondule name @ and file name @ at line @ name @ at line @ name @ at line @ name @ and file name @ at line @ at line @ at line @ name @ and file name @ at line @ name @ and file name @ at line @ name @ and file name @ at line @ name @ name @ at line @ name at line @ n	vee	csc	file	filter_specification_file_missing_cscve	е					name @ is missing at
vee         csc         file         mismatch_ent_file_name_cscve         e         Mismatch between entity name @ and file name @ at line @           vee         csc         file         mismatch_sig_file_name_cscve         e         Mismatch between signal name @ and file name @ at line @           vee         csc         forc         ill_forc_obj_type_cscve         e         Illegal force object type @ at line @           vee         csc         func         func_arg_miss_vecsc         e         Function call missing argument(s) at line @           vee         csc         func         ill_func_return_type_csve         e         Illegal function return type at line @           vee         csc         func         ill_func_csve         e         Illegal function return type at line @           vee         csc         func         port_not_output_func_csve         e         Illegal function return type at line @           vee         csc         func         port_not_output_func_csve         e         Illegal function return type at line @           vee         csc         func         port_not_output_func_csve         e         Illegal function cannot be output at line @           vee         csc         func         func_not_ocsve         e         Illegal vse of function @ at line @	vee	CSC	file	mismatch_mod_file_name_cscve	е					Mismatch between
vee       csc       file       mismatch_sig_file_name_cscve       e       Mismatch between signal name @ and file name @ are made and file and @ are made and file name was and file name										
vee         csc         file         mismatch_sig_file_name_cscve         e         Mismatch between signal name @ and file name @ at line @           vee         csc         forc         ill_forc_obj_type_cscve         e         Illegal force object type @ at line @           vee         csc         func         func_arg_miss_vecsc         e         Function call missing argument(s) at line @           vee         csc         func         ill_func_return_type_csve         e         Illegal function return type at line @           vee         csc         func         ill_func_csve         e         Illegal function @ at line @           vee         csc         func         port_not_output_func_cscve         e         lllegal use of function @ at line @           vee         csc         func         ill_use_func_cscve         e         Illegal use of function @ at line @           vee         csc         func         func_not_define_cscve         e         Function @ not defined at line @           vee         csc         func         too_many_arg_to_func_cscve         e         Too many arguments passed to function @ at line @           vee         csc         func         too_few_arg_to_func_cscve         e         Undefined function @ at line @           vee         csc	vee	CSC	file	mismatch_ent_file_name_cscve	е					
vee csc func ill_forc_obj_type_cscve e lill_forc_obj_type_cscve e lill_forc_obj_type_cscve e lill_forc_obj_type_cscve e lill_forc_obj_type_cscve e lill_forc_obj_type_cscve e lill_forc_obj_type_cscve e lill_func_recoll_func_obj_type_cscve e lill_func_recoll_func_obj_type_cscve e lill_func_recoll_func_obj_type_cscve e lill_func_recoll_func_obj_type_daragument(s) at line @ lill_func_recoll_func_obj_type_daragument(s) at line @ lill_func_obj_type_daragument(s) at lill_func_obj_t	VAA	CSC	file	mismatch sig file name cscve	Δ					@ at line @
vee         csc         forc         ill_forc_obj_type_cscve         e         Illegal force object type @ at line @           vee         csc         func         func_arg_miss_vecsc         e         Function call missing argument(s) at line @           vee         csc         func         ill_func_return_type_csve         e         Illegal function return type at line @           vee         csc         func         ill_func_csve         e         Illegal function @ at line @           vee         csc         func         port_not_output_func_cscve         e         Port @ direction cannot be output at line @           vee         csc         func         ill_use_func_cscve         e         Illegal use of function @ at line @           vee         csc         func         func_not_define_cscve         e         Function @ not defined at line @           vee         csc         func         too_many_arg_to_func_cscve         e         Too many arguments passed to function @ at line @           vee         csc         func         too_few_arg_to_func_cscve         e         Too few arguments passed to function @ at line @           vee         csc         func         undefined_func_cscve         e         Undefined function @ at line @           vee         csc         fu	VCC	030	IIIC	mismatori_sig_ine_name_eseve						name @ and file name
vee         csc         func         func_arg_miss_vecsc         e         Function call missing argument(s) at line @ argument(s) at line @ lillegal function return type at line @ vee         csc         func         ill_func_csve         e         Illegal function return type at line @ lillegal function return type at line @ lillegal function @ at line @ wee         e         Port @ direction cannot be output at line @ lillegal use of function @ at line @ wee         e         Port @ direction cannot be output at line @ wee         e         Illegal use of function @ at line @ wee         e         Illegal use of function @ at line @ wee         e         Illegal use of function @ at line @ wee         e         Illegal use of function @ at line @ wee         e         Illegal use of function @ at line @ wee         e         Illegal use of function @ at line @ wee         e         Illegal use of function @ at line @ wee         e         Illegal use of function @ at line @ wee         e         Illegal use of function @ at line @ wee         e         Illegal use of function @ at line @ wee         e         Illegal use of function @ at line @ wee         e         e         Illegal use of function @ at line @ wee         e <th< td=""><td>vee</td><td>CSC</td><td>forc</td><td>ill_forc_obj_type_cscve</td><td>е</td><td></td><td></td><td></td><td></td><td>Illegal force object type</td></th<>	vee	CSC	forc	ill_forc_obj_type_cscve	е					Illegal force object type
vee         csc         func         ill_func_return_type_csve         e         Illegal function return type at line @           vee         csc         func         ill_func_csve         e         Illegal function @ at line @           vee         csc         func         port_not_output_func_cscve         e         Port @ direction cannot be output at line @           vee         csc         func         ill_use_func_cscve         e         Illegal use of function @ at line @           vee         csc         func         func_not_define_cscve         e         Function @ not defined at line @           vee         csc         func         too_many_arg_to_func_cscve         e         Too many arguments passed to function @ at line @           vee         csc         func         too_few_arg_to_func_cscve         e         Undefined function @ at line @           vee         csc         func         undefined_func_cscve         e         Undefined function @ at line @           vee         csc         func         funct_expr_cannot_expnaded_cscve         e         Function expression @ cannot be expanded at line @           vee         csc         func         funct_not_used_in_expr_cscve         w         Function @ at line @           vee         csc         func	vee	CSC	func	func_arg_miss_vecsc	е					Function call missing
vee         csc         func         ill_func_csve         e         Illegal function @ at line @           vee         csc         func         port_not_output_func_cscve         e         Port @ direction cannot be output at line @           vee         csc         func         ill_use_func_cscve         e         Illegal use of function @ at line @           vee         csc         func         func_not_define_cscve         e         Function @ not defined at line @           vee         csc         func         too_many_arg_to_func_cscve         e         Too many arguments passed to function @ at line @           vee         csc         func         too_few_arg_to_func_cscve         e         Undefined function @ at line @           vee         csc         func         undefined_func_cscve         e         Undefined function @ at line @           vee         csc         func         funct_expr_cannot_expnaded_cscve         e         Function expression @ cannot be expanded at line @           vee         csc         func         funct_not_used_in_expr_cscve         w         Function Declaration @ already declared as another type at line @	vee	CSC	func	ill_func_return_type_csve	е					Illegal function return
vee         csc         func         port_not_output_func_cscve         e         Port @ direction cannot be output at line @           vee         csc         func         func_not_define_cscve         e         Function @ not defined at line @ Too many arguments passed to function @ at line @           vee         csc         func         too_many_arg_to_func_cscve         e         Too few arguments passed to function @ at line @           vee         csc         func         undefined_func_cscve         e         Undefined function @ at line @           vee         csc         func         undefined_func_cscve         e         Undefined function @ at line @           vee         csc         func         funct_expr_cannot_expnaded_cscve         e         Function expression @ cannot be expanded at line @           vee         csc         func         funct_not_used_in_expr_cscve         w         Function @ is not being used in an Expression at line @           vee         csc         func         func_decl_cscve         w         Function Declaration @ already declared as another type at line @	vee	CSC	func	ill_func_csve	е					type at line @ Illegal function @ at line
vee         csc         func         ill_use_func_cscve         e         Illegal use of function @ at line @           vee         csc         func         func_not_define_cscve         e         Function @ not defined at line @           vee         csc         func         too_many_arg_to_func_cscve         e         Too many arguments passed to function @ at line @           vee         csc         func         undefined_func_cscve         e         Undefined function @ at line @           vee         csc         func         undefined_func_cscve         e         Undefined function @ at line @           vee         csc         func         funct_expr_cannot_expnaded_cscve         e         Function expression @ cannot be expanded at line @           vee         csc         func         funct_not_used_in_expr_cscve         w         Function @ is not being used in an Expression at line @           vee         csc         func         func_decl_cscve         w         function Declaration @ already declared as another type at line @	vee	CSC	func	port_not_output_func_cscve	е					
vee csc func func_not_define_cscve e Function @ not defined at line @  vee csc func too_many_arg_to_func_cscve e Too many arguments passed to function @ at line @  vee csc func too_few_arg_to_func_cscve e Too few arguments passed to function @ at line @  vee csc func undefined_func_cscve e Undefined function @ at line @  vee csc func funct_expr_cannot_expnaded_cscve e Function expression @ cannot be expanded at line @  vee csc func funct_not_used_in_expr_cscve w Function @ is not being used in an Expression at line @  vee csc func func_decl_cscve w Function @ is not being used in an Expression at line @  vee csc func func_decl_cscve w Function @ is not being used in an Expression at line @  vee csc func func_decl_cscve w Function @ is not being used in an Expression at line @  vee csc func func_decl_cscve w Function @ is not being used in an Expression at line @  vee csc func func_decl_cscve w Function @ already declared as another type at line @	vee	CSC	func	ill use func cscve	е					
vee     csc     func     too_many_arg_to_func_cscve     e     Too many arguments passed to function @ at line @       vee     csc     func     too_few_arg_to_func_cscve     e     Too few arguments passed to function @ at line @       vee     csc     func     undefined_func_cscve     e     Undefined function @ at line @       vee     csc     func     funct_expr_cannot_expnaded_cscve     e     Function expression @ cannot be expanded at line @       vee     csc     func     funct_not_used_in_expr_cscve     w     Function @ is not being used in an Expression at line @       vee     csc     func     func_decl_cscve     w     Function Declaration @ already declared as another type at line @										at line @
vee csc func too_few_arg_to_func_cscve e Too few arguments passed to function @ at line @  vee csc func undefined_func_cscve e Undefined function @ at line @  vee csc func funct_expr_cannot_expnaded_cscve e Function expression @ cannot be expanded at line @  vee csc func funct_not_used_in_expr_cscve w Function @ is not being used in an Expression at line @  vee csc func funct_not_used_in_expr_cscve w Function @ is not being used in an Expression at line @  vee csc func func_decl_cscve w Function Declaration @ already declared as another type at line @										at line @
vee         csc         func         too_few_arg_to_func_cscve         e         Too few arguments passed to function @ at line @           vee         csc         func         undefined_func_cscve         e         Undefined function @ at line @           vee         csc         func         funct_expr_cannot_expnaded_cscve         e         Function expression @ cannot be expanded at line @           vee         csc         func         funct_not_used_in_expr_cscve         w         Function @ is not being used in an Expression at line @           vee         csc         func         func_decl_cscve         w         Function Declaration @ already declared as another type at line @	vee	CSC	Turic	too_many_arg_to_tune_cscve	е					passed to function @ at
vee     csc     func     undefined_func_cscve     e     Undefined function @ at line @       vee     csc     func     funct_expr_cannot_expnaded_cscve     e     Function expression @ cannot be expanded at line @       vee     csc     func     funct_not_used_in_expr_cscve     w     Function @ is not being used in an Expression at line @       vee     csc     func     func_decl_cscve     w     Function Declaration @ already declared as another type at line @	vee	CSC	func	too_few_arg_to_func_cscve	е					Too few arguments
vee csc func funct_expr_cannot_expnaded_cscve e Function expression @ cannot be expanded at line @  vee csc func funct_not_used_in_expr_cscve w Function @ is not being used in an Expression at line @  vee csc func func_decl_cscve w Function Declaration @ already declared as another type at line @	1/00	000	funo	undefined tune engue						line @
vee csc func funct_not_used_in_expr_cscve w Function @ is not being used in an Expression at line @  vee csc func func_decl_cscve w Function Declaration @ already declared as another type at line @										line @
vee     csc     func     funct_not_used_in_expr_cscve     w     Function @ is not being used in an Expression at line @       vee     csc     func     func_decl_cscve     w     Function Declaration @ already declared as another type at line @	vee	CSC	TUNC	runct_expr_cannot_expnaded_cscve	e					cannot be expanded at
vee csc func func_decl_cscve w Function Declaration @ already declared as another type at line @	vee	CSC	func	funct_not_used_in_expr_cscve	w					Function @ is not being
already declared as another type at line @										line @
	vee	CSC	tunc	tunc_decl_cscve	W					already declared as
	vee	CSC	func	func_param_csc	е					

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	CSC	func	unmatched_funct_param_cscve	е					parameter @ at line @ Unmatched function
									parameter @ at line @
vee	CSC	gate	ill_output_pin_name_gate_csve	е				ı	Illegal output terminal Expression pin @ at line @
vee	csc	hid	cannot_locate_hier_id_hid_cscve	е					Can't locate hierarchical identifier @ at line @
vee	CSC	hid	ref_minst_found_in_expr_hid_cscve	е					References a module
									instance @ found in an Expression hid at line @
vee	CSC	hid	ref_entity_found_in_expr_hid_cscve	е					References a entity instance @ found in an
									Expression hid at line @
vee	CSC	hid	ref_unit_found_in_expr_hid_cscve	е					References a unit instance @ found in an
vee	CSC	hid	ref_in_eexpr_hid_cscve	е					Expression hid at line @ References a module
			,						instance @ passed as argument to PLI task call
									is also found in an
vee	CSC	hid	ref_in_expr_hid_cscve	е					Expression @ at line @ References a entity
								a	instance @ passed as argument to PLI task call
									is also found in an Expression @ at line @
vee	CSC	hid	reff_in_expr_hid_cscve	е					References a unit
								a	instance @ passed as argument to PLI task call
									is also found in an Expression @ at line @
vee	csc	hid	hid_name_traverses_into_func	е					Hid @ name traverses
									into a function @ at line @
vee	CSC	hid	hid_ref_mod_out_arg_sytk_cscve	е					Hid @ referencing a module instance passed
								a	as 'out' type argument to a system task @ at line
									@
vee	CSC	hid	hid_ref_entity_out_arg_sytk_cscve	е				e	Hid @ referencing a entity instance passed as
									out' type argument to a system task @ at line @
vee	CSC	hid	hid_ref_unit_out_arg_sytk_cscve	е					Hid @ referencing a unit instance passed as 'out'
									type argument to a
vee	CSC	hid	hid_reference_not_found_cscve	е					system task @ at line @ @ reference not found at
vee	CSC	hid	mifc_in_hid_not_exist_cscve	е				N	line @ Module instance @ in hid
vee	CSC	hid	entity_instance_in_hid_not_exist_cscve						does not exist at line @ Entity instance @ in hid
			•	е					does not exist at line @
vee	CSC	hid	unit_instance_in_hid_not_exist_cscve	е					Unit instance @ in hid does not exist at line @
vee	CSC	hid	mod_found_in_path_in_dsgn_cscve	е					Module @ found in path @ in the design at line @
vee	CSC	hid	enity_found_in_path_in_dsgn_cscve	е					in the design at line @
vee	CSC	hid	unit_found_in_path_in_dsgn_cscve	е					Unit @ found in path @
vee	CSC	hid	hierarchical_id_path_contains_func_csc	е					in the design at line @ Hierarchical ID @ path
								C	ontains a function at line @
vee	CSC	id	ill_terminal_id_csve	е					Illegal terminal identifier at line @
vee	CSC	init	assn_mem_in_init_blk_cscve	е					Assign memory in initial
vee	CSC	inst	inst_duplicate_mod_name_cscve	е					block at line @ Duplicate port @ in the
									port list for module @ at line @
vee	CSC	inst	inst_duplicate_entity_name_cscve	е					Duplicate port @ in the port list for entity @ at
									line @
vee	CSC	inst	inst_duplicate_unit_name_cscve	е					Duplicate port @ in the port list for unit @ at line
vee	CSC	inst	miss_declparam_inst_csve	е					@ Parameter Declaration
	csc	inst	ill_mod_inst_name_cscve	е					missing value at line @ Illegal module instance
vee									@ at line @
vee	CSC	inst	ill_entity_inst_name_cscve	е					Illegal entity instance @ at line @
vee	CSC	inst	ill_unit_inst_name_cscve	е				l	llegal unit instance @ at line @
vee	CSC	inst	inst_name_defined_mod_csve	е					Instance name @ already defined in this
									module at line @
vee	CSC	inst	inst_name_defined_ent_csve	е	1	1			Instance name @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl Desc entity at line @
vee	CSC	inst	inst_name_defined_unit_csve	е				Instance name @
								already defined in this unit at line @
vee	CSC	inst	inst_too_many_bits_cscve	е				Too many bits for port @ of instance array @,
								formal @, actual @ at line @
vee	CSC	inst	inst_port_not_connected_var_cscve	е				Port 'port' of instance
								array 'array' is not connected to variable at
vee	CSC	inst	inst_insufficient_bits_cscve	е				line @ Insufficient bits for port
•00	000		mot_modmoiont_one_ocovo					'port' of instance array
								'array ', formal number, actual number at line @
vee	CSC	inst	inst_mod_name_not_defined_cscve	е				Module name not defined at line @
vee	CSC	inst	inst_ent_name_not_defined_cscve	е				Entity name not defined at line @
vee	CSC	inst	inst_unit_name_not_defined_cscve	е				Unit name not defined at
vee	CSC	inst	many_mod_inst_param_assign_cscve	е				line @ Too many module
								instance parameter assignments (number >
1/00	200	inst	many entity inst param assign cscve					rrumber) at line @ Too many entity instance
vee	CSC	IIISt	many_enuty_inst_param_assign_cscve	е				parameter assignments
								(number > rrumber) at line @
vee	CSC	inst	many_unit_inst_param_assign_cscve	е				Too many unit instance parameter assignments
								(number > rrumber) at
vee	CSC	inst	complexexpr_cannot_mapped_inout_port_cscve	е				line @ Complex Expression @
								cannot be mapped to inout port @ at line @
vee	CSC	inst	complexexpr_cannot_mapped_unknown_port_cscve	е				Complex Expression @ cannot be mapped to
								unknown type port @ at
vee	CSC	inst	netdecl_contains_ill_prts_cscve	е				line @ Net Declaration [@: @]
			·					contains an illegal part select at line @
vee	CSC	inst	regdecl_contains_ill_prts_cscve	е				Reg Declaration [@ : @]
								contains an illegal part select at line @
vee	CSC	inst	complex_expr_inst_parent_module_cscve	е				Complex actual Expression associated
								with port @ of module @ instantiated in parent
			in the state of th					module at line @
vee	CSC	inst	complex_expr_inst_entity_parent_module_cscve	е				Complex actual Expression associated
								with port @ of entity @ instantiated in parent
vee	CSC	inst	complex_expr_inst_unit_parent_module_cscve	е				module at line @ Complex actual
VCC	030	iiist	complex_expl_inst_unit_parent_module_cscve	6				Expression associated
								with port @ of unit @ instantiated in parent
vee	CSC	inst	inst_mod_output_port_width_cscve	е				module at line @ Mod @ Output port @
	555							width mismatch, actual-width ( port-width )
								at line @
vee	CSC	inst	inst_entity_output_port_width_cscve	е				Entity @ Output port @ width mismatch,
								actual-width ( port-width ) at line @
vee	CSC	inst	inst_unit_output_port_width_cscve	е				Unit @ Output port @
								width mismatch, actual-width ( port-width )
vee	CSC	inst	inst_mod_input_port_width_cscve	е				at line @ Mod @ Input port @
			- ·					width mismatch, actual-width ( port-width )
								at line @
vee	CSC	inst	inst_entity_input_port_width_cscve	е				Entity @ Input port @ width mismatch,
								actual-width ( port-width ) at line @
vee	CSC	inst	inst_unit_input_port_width_cscve	е				Unit @ Input port @ width mismatch,
								actual-width ( port-width )
vee	CSC	inst	inst_mod_not_define_cscve	е				at line @  Module not defined at
vee	CSC	inst	inst_entity_not_define_cscve	е				line @ Entity not defined at line
			_ ,					@
vee	CSC	inst	inst_unit_not_define_cscve	е				Unit not defined at line @

•	ь		No	\.	1/4005	1/0004			
Vee	Phase	Type inst	Name miss_mifc_name_cscve	W/E w	V1995	V2001	Sys_ver x	Csl	Desc Missing module instance
	000								name. This syntax is an
									error according to IEEE
									1364-1995 but is allowed by commercial Verilog
									compilers at line @
vee	CSC	inst	miss_ent_instance_name_cscve	w			Х		Missing entity instance
									name. This syntax is an
									error according to IEEE
									1364-1995 but is allowed
									by commercial Verilog compilers at line @
vee	CSC	inst	miss_unit_instance_name_cscve	w			Х		Missing unit instance
									name. This syntax is an
									error according to IEEE
									1364-1995 but is allowed by commercial Verilog
									compilers at line @
vee	CSC	inst	mifc_port_actual_formal_width_mismatch_cscve	w					Module @ instance @
									port @ width mismatch,
									actual width @ formal width @ at line @
vee	CSC	inst	mifc_port_actual_formal_width_mismatch_cscvh	w					Module @ instance @
									port @ width mismatch,
									actual width @ formal
vee	CSC	inst	ent_port_actual_formal_width_mismatch_cscve	w					width @ at line @ Entity @ instance @ port
vee	CSC	IIISt	ent_port_actual_formal_width_fillsfillation_cscve	VV					@ width mismatch.
									actual width @ formal
									width @ at line @
vee	CSC	inst	unit_port_actual_formal_width_mismatch_cscve	W					Unit @ instance @ port @ width mismatch.
									actual width @ formal
									width @ at line @
vee	CSC	inst	unmatched_port_connect_in_inst_cscve	е					Unmatched port @
									connect in instance @ at
vee	CSC	inst	inst_differs_in_case_from_mod_cscve	е					line @ Instance name @ differs
VCC	030	iiist	inst_diners_in_case_noin_mod_cscve						in case from module
									name @ at line @
vee	CSC	inst	inst_differs_in_case_from_ent_cscve	е					Instance name @ differs
									in case from entity name @ at line @
vee	CSC	inst	inst_differs_in_case_from_sig_cscve	е					Instance name @ differs
									in case from signal name
									@ at line @
vee	CSC	lib	lib_name_not_mod_declaration_csve	е					Library file @ doesn't contain a module
									Declaration at line @
vee	CSC	lib	lib_name_not_entity_declaration_csve	е					Library file @ doesn't
									contain a entity
vee	CSC	lib	lib_name_not_unit_declaration_csve	е					Declaration at line @ Library file @ doesn't
vee	CSC	IID	lib_name_not_unit_declaration_csve	6					contain a unit Declaration
									at line @
vee	CSC	lib	lib_not_contain_supply_cscve	е					Library does not contain
1/00	000	loon	while_initial_value_unknown_loop_cscve	е					supply @ at line @ While control initial
vee	CSC	loop	writte_trittial_value_urikriowri_loop_cscve	е					variable @ unassigned.
									Initial value unknown at
		_							line @
vee	CSC	loop	while_loop_not_assign_stmt_controlvar_cscve	е					While loop body does not contain an assignment
									statement for control
									variable @ at line @
vee	CSC	loop	assign_stmt_not_last_while_loop_cscve	е					Assignment statement
									for control variable @ not last statement in while
									loop at line @
vee	CSC	loop	undet_init_value_loop_cscve	е					Unable to determine init
		•	,						value for loop at line @
vee	CSC	loop	undet_limit_loop_cscve	е					Unable to determine limit
vee	CSC	loop	loop_bounds_calculated_int_cscve	w	1	1			for loop at line @ Loop bounds are
1.55	300	.50p		"					calculated to be integer
									@, check that this is
1/00	000	loo-	over the contains yer hit salest seems	100	-	-			correct at line @
vee	CSC	loop	expr_lhs_contains_var_bit_select_cscve	w					Expression in lhs of assignment contains a
					1	1			variable bit select at line
									@
vee	csc	loop	loop_bounds_not_const_csc	W					Loop bounds are
vee	CSC	loop	loop_ctrl_init_expr_not_const_cscve	W		-			non-constant at line @ Non-constant loop
100	030	ююр	100P_0ttl_ttllt_exbt_ttot_cottst_cscve	VV	1	1			bound. Loop control
					1	1			variable initialization
									Expression is not a
									constant Expression at line @
vee	CSC	loop	loop_term_expr_not_const_cscve	w					Non-constant loop
	300	.500		"	1	1			bound. loop terminating
			•						

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
Jul	11100	.,,,,	Hamo		71000	72001		00.	Expression could not be evaluated to a constant at line @
vee	CSC	loop	init_expr_reset_by_var_cscve	е					Non-constant loop bound. initializing Expression reset by
vee	csc	loop	loop_ctrl_var_1_bit_wide_cscve	w					variable at line @ The loop control variable @ is one bit wide. Check the loop control variable
vee	CSC	mdb	bad_mdb_net_cscve	е					Declaration. at line @ Bad multi-driven Net @
vee	CSC	mdb	bad_mdb_port_cscve	е					at line @ Bad multi-driven Port @ at line @
vee	CSC	mdb	bad_mdb_signal_cscve	е					Bad multi-driven Signal @ at line @
vee	CSC	mdb	unsupp_comp_mdb_net_cscve	е	?				Unsupported component type @ driving in multi-driven Net name at line @
vee	CSC	mdb	unsupp_comp_mdb_port_cscve	е	?				Unsupported component type @ driving in multi-driven Port name at
vee	csc	mdb	unsupp_comp_mdb_signal_cscve	е	?				line @ Unsupported component type @ driving in multi-driven Signal name at line @
vee	CSC	mdb	unsupp_comp_drive_mdb_cscve	е	?				Unsupported component type @ driving multi-driven Net natne at
vee	CSC	mdb	unsupp_comp_drive_mdb_port_cscve	е	?				line @ Unsupported component type @ driving multi-driven Port natne at line @
vee	CSC	mdb	unsupp_comp_drive_mdb_signal_cscve	е	?				Unsupported component type @ driving multi-driven Signal natne at line @
vee	CSC	mdb	mdb_net_driven_by_trns_cscve	е					Multiply driven Net driven by transistor primitive type @ at line @
vee	CSC	mdb	mdb_port_driven_by_trns_cscve	е					Multiply driven Port driven by transistor primitive type @ at line
vee	CSC	mdb	mdb_sig_driven_by_trns_cscve	е					@ Multiply driven Signal driven by transistor primitive type @ at line @
vee	csc	mdb	mdb_unsupp_comp_drvs_net_cscve	е					Unsupported component type driving Net drives Net connected to multi-driven Net at line @
vee	CSC	mdb	mdb_unsupp_comp_drvs_port_cscve	е					Unsupported component type driving Port drives Port connected to multi-driven Port at line
vee	CSC	mdb	mdb_unsupp_comp_drvs_sig_cscve	е					@ Unsupported component type driving Signal drives Signal connected to multi-driven Signal at line
vee	CSC	mdb	mdb_incompatible_net_drives_multiple_net_cscve	е					@ Incompatible driver driving tandem Net drives Net connected to multi-driven Net at line @
vee	CSC	mdb	mdb_incompatible_port_drives_multiple_port_cscve	е					Incompatible driver driving tandem Port drives Port connected to multi-driven Port at line @
vee	CSC	mdb	mdb_incompatible_sig_drives_multiple_sig_cscve	е					Incompatible driver driving tandem Net drives Net connected to multi-driven Port at line @
vee	CSC	mdb	mdb_unsupp_LHS_concatenation_cscve	е					Unsupported LHS concatenation in multi-drive 'device at line @
vee	CSC	mdb	mdb_bus_has_too_many_drivers_cscve	е					Bus has too many drivers. at line @
vee	csc	mdb mdb	mdb_always_blk_drive_cscve nontri_gate_drives_mdb_net_cscve	W					Multiple always blocks drive name @ at line @ non-tri-state gate drives
vee	CSC	mdb	nontri_gate_drives_mdb_port_cscve	w					multi-driven Net at line @ non-tri-state gate drives
<u> </u>				<u> </u>	1	i	1	1	J J

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc multi-driven Port at line @
vee	CSC	mdb	nontri_gate_drives_mdb_sig_cscve	w					non-tri-state gate drives multi-driven Signal at line
vee	csc	mem	mem_prts_csvee	е					@ Memories do not support part select specifier at
vee	CSC	mem	ill_ref_mem_name_csve	е					line @ Illegal hid reference to
vee	CSC	mem	mem_ref_without_index_cscve	е					memory (name) at line @ Memory @ referenced
									without index through hierarchical ID @ at line @
vee	CSC	mifc	mifc_not_array_csvee	е					Ports may not be an array at line @
vee	CSC	mifc mifc	port_identifier_mifc_cscve mifc_mod_input_port_decl_as_reg_cscve	e					Port @ at line @ Module @ input port @
			,						declared as type reg at line @
vee	CSC	mifc	mifc_entity_input_port_decl_as_reg_cscve	е					Entity @ input port @ declared as type reg at line @
vee	CSC	mifc	mifc_unit_input_port_decl_as_reg_cscve	е					Unit @ input port @ declared as type reg at line @
vee	CSC	mifc	mod_output_wire_redecl_reg_cscve	е					Module @ output port re-declared as type reg after use as implicitly declared wire at line @
vee	CSC	mifc	enity_output_wire_redecl_reg_cscve	е					Entity @ output port re-declared as type reg
									after use as implicitly declared wire at line @
vee	CSC	mifc	unit_output_wire_redecl_reg_cscve	е					Unit @ output port re-declared as type reg
									after use as implicitly declared wire at line @
vee	CSC	mifc	output_port_is_mem_type_mifc_cscve	е					Output port @ is memory type at line @
vee	CSC	mifc	mifc_inout_port_is_mem_type_cscve	е					Inout port @ is memory type at line @
vee	CSC	mifc	mod_output_port_mismatch_actual_witdh_cscve	w					Module @ output port @ formal to actual width
vee	CSC	mifc	ent_output_port_mismatch_actual_witdh_cscve	w					mismatch at line @ Entity @ output port @ formal to actual width mismatch at line @
vee	CSC	mifc	unit_output_port_mismatch_actual_witdh_csc	W					Unit @ output port @ formal to actual width mismatch at line @
vee	csc	mifc	port_name_different_in_upper_lower_case_cscve	е					Port name @ different in upper lower case at line @
vee	CSC	mifc	port_not_def_in_iodecl_cscve	е					Port @ not defined in ioDeclaration at line @
vee	CSC	mifc	port_not_def_in_portl_cscve	е					Port @ not defined in port list at line @
vee	csc	mifc	port_wiredecl_mismatch_cscve	е					Port @ wireDeclaration mismatch at line @
vee	csc	mifc	pos_based_null_inst_port_cscve	е					Position based null instance port at line @
vee	CSC	mifc	last_portdecl_contains_trailcomma_cscve	е					Last portDeclaration contains a trailing comma at line @
vee	CSC	mins	mins_expr_incompatible_type_cscve	е					Expression @ has an incompatible argument type @ with the port at
vee	CSC	mins	mins_mod_not_exist_cscve	е					line @ Module @ does not exist
vee	CSC	mins	mins_entity_not_exist_cscve	е					at line @ Entity @ does not exist
vee	CSC	mins	mins_unit_not_exist_cscve	е					at line @ Unit @ does not exist at
vee	CSC	mins	undefined_instance_cscve	е					line @ Undefined instance @ at
vee	CSC	mod	mod_param_bad_number_csve	е					line @ Module name @
									parameter list contains an Incorrect number of parameter overrides at line @
vee	CSC	mod	mod_entity_param_bad_number_csve	е					Entity name @ parameter list contains an Incorrect number of parameter overrides at line @
vee	CSC	mod	mod_unit_param_bad_number_csve	е					Unit name @ parameter list contains an Incorrect
									number of parameter overrides at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	CSC	mod	ill_mod_name_cscve	е					Illegal module @ at line
vee	CSC	mod	ill_mod_entity_name_cscve	е					@ Illegal entity @ at line @
vee	csc	mod	ill_mod_unit_name_cscve	е					Illegal unit @ at line @
vee	csc	mod	mod_mult_decl_string_cscve	е					Multiple Declarations of string detected in module
									@ at line @
vee	csc	mod	mod_entity_mult_decl_string_cscve	е					Multiple Declarations of
									string detected in entity @ at line @
vee	CSC	mod	mod_unit_mult_decl_string_cscve	е					Multiple Declarations of
									string detected in unit @ at line @
vee	CSC	mod	mod_mult_def_cscve	е					Module @ defined in
1/00		d	mad ant mult dat aggre						multiple places at line @
vee	CSC	mod	mod_ent_mult_def_cscve	е					Entity @ defined in multiple places at line @
vee	csc	mod	mod_unit_mult_def_cscve	е					Unit @ defined in
vee	CSC	mod	mod_no_module_found_cscve	е					multiple places at line @ No modules found at line
100	000	11100		ŭ					@
vee	CSC	mod	mod_no_entity_found_cscve mod_no_unit_found_cscve	е					No entity found at line @ No unit found at line @
vee	CSC	mod mod	failed_find_mod_cscve	e					Failed to find module @
									at line @
vee	CSC	mod	failed_find_entity_cscve	е					Failed to find entity @ at line @
vee	CSC	mod	failed_find_unit_cscve	е					Failed to find unit @ at
V00	CSC	mod	undefined_mod_cscve						line @ Undefined module @ at
vee	CSC	mou	undenned_mod_cscve	е					line @
vee	csc	mod	undefined_ent_cscve	е					Undefined entity @ at
vee	CSC	mod	undefined_unit_cscve	е					line @ Undefined unit @ at line
				ŭ					@
vee	csc	mod	unexpandable_macromodule_cscve	е					Unexpandable macromodule @ at line
									@
vee	csc	mod	non_interconnect_in_hierarchical_mod_cscve	е					Non interconnect in
									hierarchical module @ at line @
vee	csc	mod	non_interconnect_in_hierarchical_ent_cscve	е					Non interconnect in
									hierarchical entity @ at line @
vee	CSC	mod	non_interconnect_in_hierarchical_sig_cscve	е					Non interconnect in
									hierarchical signal @ at line @
vee	CSC	mod	empty_mod_cscve	е					Empty module at line @
vee	CSC	mod	empty_ent_cscve	е					Empty entity at line @
vee	CSC	mod net	empty_unit_cscve namereg_not_on_LHS_stmt_net_csve	e					Empty unit at line @ Register @ cannot be
									used on LHS of this
									assignment statement at line @
vee	CSC	net	net_implicit_wire_redecl_reg_cscve	е					Implicitly declared as a
									wire @ re-declared as a req @. at line @
vee	csc	net	time var decl cscve	е					Time variable @
									declared at line @
vee	CSC	net	time_var_bit_used_cscve	е					Time variable @ bit used at line @
vee	csc	net	undecl_net_in_mod_cscve	е					Undeclared net @ in
vee	CSC	net	undecl port in mod cscve	е					module @ at line @ Undeclared port @ in
466	030	Het		6					module @ at line @
vee	CSC	net	undecl_sig_in_mod_cscve	е					Undeclared signal @ in
vee	CSC	net	undecl_net_in_ent_cscve	е					module @ at line @ Undeclared net @ in
									entity @ at line @
vee	CSC	net	undecl_port_in_ent_cscve	е					Undeclared port @ in entity @ at line @
vee	CSC	net	undecl_sig_in_ent_cscve	е					Undeclared signal @ in
V00	000	net	unded not in sig seeve						entity @ at line @ Undeclared net @ in
vee	CSC	net	undecl_net_in_sig_cscve	е					signal@ at line @
vee	CSC	net	undecl_port_in_sig_cscve	е					Undeclared port @ in
vee	CSC	net	undecl_sig_in_sig_cscve	е					signal @ at line @ Undeclared signal @ in
									signal @ at line @
vee	CSC	net	port_used_prior_to_decl_cscve	е					Port @ used prior toDeclaration at line @
vee	CSC	net	1bit_with_prts_cscve	е					1-bit with part select at
1/00	000	notal	ill dod voo ossys	-					line @
vee	CSC	netd	ill_decl_vec_cscve	е					Illegal Declaration of vector @ at line @
vee	CSC	nett	nett_ill_reg_name_cscve	е					Illegal register @ at line
vee	CSC	nett	nett_ill_net_name_cscve	е					@ Illegal net @ at line @
vee	CSC	nett	nett_ill_port_name_cscve	е					Illegal port @ at line @
vee	CSC	nett	nett_ill_signal_name_cscve	е					Illegal signal @ at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	CSC	nett	net_scalar_vect_nett_cscve	е			- J · · ·		Net declared as both scalar and vector at line
vee	CSC	nett	port_scalar_vect_nett_cscve	е					@ Port declared as both scalar and vector at line
vee	CSC	nett	signal_scalar_vect_nett_cscve	е					@ Signal declared as both scalar and vector at line
vee	CSC	nett	hot_mux_not_use_bus_connection_net_cscve	е					@ One hot mux can not be used for bus connection between modules Net @
vee	csc	nett	hot_mux_not_use_bus_connection_port_cscve	е					at line @ One hot mux can not be used for bus connection between modules Port @ at line @
vee	CSC	nett	hot_mux_not_use_bus_connection_sig_cscve	е					One hot mux can not be used for bus connection between modules Signal
vee	CSC	nett	reg_connected_inst_inout_cscve	е					@ at line @  Reg @ connnected to instantiation @ inout @
vee	CSC	nett	ill_net_in_proc_assn_cscve	е					at line @ Illegal net type type in procedural assignement
vee	CSC	nett	ill_port_in_proc_assn_cscve	е					at line @ Illegal port type type in procedural assignement
vee	csc	nett	ill_sig_in_proc_assn_cscve	е					at line @ Illegal signal type type in procedural assignement
vee	CSC	num	not_allowed_width0_num_cscve	е					at line @ Width 0 not allowed for
vee	CSC	num	real_num_not_allowed_cscve	е					Real numbers not allowed at line @
vee	CSC	num	found_x_z_in_num_literal_cscve	е					Found x and/or z value in
vee	CSC	num	too_many_digits_in_sized_num_cscve	w					number literal at line @ Number of digits exceeds the width in a sized
vee	CSC	num	divide_by_zero_num_cscve	е					number at line @ Divide by zero at line @
vee	CSC	num	child_mod_inst_parent_mod_cscve	е					Child module @ instantiates parent
vee	CSC	num	child_ent_inst_parent_ent_cscve	е					module @ at line @ Child entity @ instantiates entity module
vee	CSC	num	child_sig_inst_parent_sig_cscve	е					@ at line @ Child signal @ instantiates signal
vee	CSC	num	int_decl_incorrect_cscve	е					module @ at line @ Integer Declaration
vee	csc	num	int_var_indexed_cscve	е					incorrect at line @ Integer variable inedexed
vee	CSC	parm	parm_redecl_as_reg_name_csve	е					at line @ Parameter re-declared
vee	CSC	parm	parm_redecl_as_port_port_csve	е					as reg @ at line @ Parameter re-declared
vee	csc	parm	parm_redecl_as_net_name_csve	е					as port @ at line @ Parameter re-declared
vee	CSC	parm	parm redect as port name csve	е					as Net @ at line @ Parameter re-declared
vee	CSC	parm	parm_redecl_as_signal_name_csve	е					as Port @ at line @ Parameter re-declared as Signal @ at line @
vee	CSC	parm	duplicate_decl_parm_name_csve	е					Duplicate declaration of parameter name @ at
vee	CSC	parm	ill_parm_identifier_cscve	е					line @ Illegal parameter @ at
vee	csc	parm	value_of_parm_OS_platform_dependent_cscve	W					line @ Parameter select width > 32. The value is OS and
vee	csc	parm	parm_redefined_cscve	w					platform dependent at line @ Parameter @ redefined
vee	CSC	pars	endfunction_miss_pars_csve	е					at line @ Endfunction missing at
vee	csc	pars	endtask_miss_pars_csve	е					line @ Endtask missing at line
vee	CSC	pars	endmodule_miss_pars_csve	е					@ Endmodule missing at
vee	CSC	pars	miss_cont_assign_pars_csve	е					line @ Missing = sign for
vee	csc	pli	user_syst_not_listed_in_pli_table_cscve	е					continuous assignment at line @
		•	_,						not listed in PLI table at line @
vee	CSC	port	ill_formal_port_name_cscve	е	L				Illegal formal port @ at

Text macro resolar and replaced   Pervision solar and replac	Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
Vee csc pris	vee	CSC	pp	text_redefined_replaced_cscve	W					line @ Text macro redefined
Vec   Cac										and replaced @. Previous definition
veo csc pp undefined_macro_cscve o Undefined macro of Undefined Macro										filename, line number @
vee csc pp include_file_contains_nonconst_cscve e include_file_contains_contant @ sit line @ vee csc pp endif_or_else_without_iddef_cscve e										line number @ at line @
	vee	CSC	pp		е					line @
Veo   CSC   prim   Z.In_prim_inst_Cscve   e   Z in_prim_inst instantials	vee	CSC	pp	include_file_contains_nonconst_cscve	е					Include file contains non constant @ at line @
vee         cso         prim         z.in.phin_inst_csove         e         zin primitive instantial and in the @instantial and in the @in	vee	CSC	pp	endif_or_else_without_ifdef_cscve	е					Endif-or-else-without ifdef at line @
Vee         csc         prim         prim.Instan_cscve         9         Prim.Invernistant in eilie           vee         csc         proc         proc_blk_missing_evc_cscve         e         Always block miss           vee         csc         pris         type_pris_csve         e         Type_ged does not supprised typecrife line in eilie eilie in eilie eil	vee	CSC	prim	z_in_prim_inst_cscve	е					z in primitive instantiation
vee         csc         proc         proc, bilk, missing, evc_scve         e         Always block miss event control at line.           vee         csc         prfs         type_prfs_csvee         e         Type @ does not suppart select specifie inc. @           vee         csc         prfs         type_prfs_csve         e         Type @ foreign suppart select specifie inc. @           vee         csc         prfs         prfs_out_of_range_cscve         e         Parameter @ @ @           vee         csc         prfs         constant_aray_cscve         e         Illegal value for prescriber inc. @           vee         csc         prfs         constant_aray_cscve         e         Constant prescriber inc. @           vee         csc         prfs         const_arts_contains_non_const_selector_cscve         e         Constant prescriber inc. @           vee         csc         prfs         bus_index_prts_for_var_out_of_range_cscve         e         Bus index @ index out for an one-const select (@ : @           vee         csc         prfs         bus_prts_index_out_of_name_for_var_cscve         e         Bus_part select (@ : @           vee         csc         prfs         bus_prts_index_out_of_name_for_var_cscve         e         Bus_part select (@ : @           vee	vee	CSC	prim	prim_instan_cscve	е					Primitive instantiation @
Vee   CSC   prits   type_prits_csve   e   prits_csve_prits_csve   e   prits_csve_prits_csve   e   type_prits_csve   e   type_prits_csve   e   type_prits_csve   e   type_prits_csve_	vee	CSC	proc	proc_blk_missing_evc_cscve	е					Always block missing
Inine @   Type @ Gos not suppart select specifies   Type @ Gos	vee	CSC	prts	type_prts_csvee	е					event control at line @ Type @ does not support
vee   csc   prts   type_prts_csve   e   prts   type @ does not suppressed specifie line @   parts elect specifie line @   select specifie line &										part select specifier at line @
Vee   CSC   prts   prts_out_of_range_osove   e   Parameter @(@: @ select is out of rang ine @ select of instance a select of instance a select of prts   const_prts_contains_non_const_selector_csove   e   Constaint_part_selector_csove   e   Constain	vee	CSC	prts	type_prts_csve	е					Type @ does not support
vec   csc   prts   ill_prts_inst_array_cscve   e   select is out of rang ine @   lllegal value for presentation   select of instance										line @
Vee   CSC   prts   Ill_prts_inst_array_cscve   e   sellect of instance   name at time @ Constamp part select of instance   constamp part select of instanc	vee	CSC	prts	prts_out_of_range_cscve	е					select is out of range at
vee   csc   prits   const_prits_contains_non_const_selector_cscve   e   Constant part selec contains a non-const selector   gat line   Bus index   integer   part select   gat   gat   part select   gat   p	vee	CSC	prts	ill_prts_inst_array_cscve	е					line @ Illegal value for part
Vee   CSC   prts   Dus_Index_prts_for_var_out_of_range_cscve   e   Constant part select (@ constant										select of instance array 'name' at line @
selector @ at lime @ surprise out of a lime surprise out of a lime guitable surprise out of a lime @ surprise out of a lime guitable surprise out of a lime surprise out out of a lime surprise out out o	vee	CSC	prts	const_prts_contains_non_const_selector_cscve	е					Constant part select @
part select (@:@) variable @ out of ra at line @ Sus part select (@:@) variable @ out of ra at line @ Sus part select (@:@) variable @ out of range at line @ Use or select (@:@) variable @ out of range variable @ out of range variable @ at line @ lines @ out of range variable @ at line @ variable @ at line @ lines @ out of range variable @ at line @ lines lines incomplete_prts_specification_cscve e lillegat locken in part select (@:@) at line @ lines lincomplete part select @ out of range variable @ at line @ lines lincomplete part select @ out of range variable @ at line @ lines lines lines lines lines lines in lines lines in lines e lines @ lines										selector @ at line @
vee csc prts bus_prts_for_var_out_of_range_cscve e Bus part select @ variable @ out of ra at line @ leve csc prts bus_prts_index_out_of_name_for_var_cscve e Bus_part select [@ index @ out of ray variable @ at line index @ out of ray variable @ at line index @ out of ray variable @ at line index @ out of ray variable @ at line index @ out of ray variable @ at line index @ out of ray variable @ at line index @ out of ray variable @ at line index @ out of ray variable @ at line index @ out of ray variable @ at line @ lilegal index index in gat line @ specification death index in parts_cscve e incomplete parts especification death index index in parts_out lilegal index in parts gat line @ at line @ select @ not allowed were csc prts index_order_reversed_cscve e Bus_order_reversed_index_order_index_order_in	vee	CSC	prts	bus_index_prts_for_var_out_or_range_cscve	е					part select [@:@] for
vee         csc         prts         bus_prts_index_out_of_name_for_var_cscve         e         Bus_part select [@ index @ out of rang variable @ at line @ variable @ at line @ variable @ at line index @ out of rang variable @ at line @ lilegal token in parts @ at line @ incomplete_prts_specification_cscve         e         Illegal token in parts @ at line @ incomplete part sel specification @ at line @ incomplete index_in_prts_not_allowed_cscve         e         Illegal index in part sel index in part select index in part select index in part select index or reversed [@ : index_in_prts_not_allowed_cscve         e         Negative index in part select index in part select index in part select index or reversed [@ : index_in_allowed_cscve         e         Part select index or reversed [@ : index_in_prts_not_allowed_cscve         e         Part select index or reversed [@ : index_in_prts_not_allowed_cscve         e         Part select index or reversed [@ : index_in_prts_not_allowed_cscve         e         Part select index or reversed [@ : index_in_allowed_cscve         e         Part select index or reversed [@ : index_in_prts_not_allowed_cscve         e         Part select index_in_allowed_cscve         e         Part select index_in_prts_not_allowed_cscve         e         Part select index_in_allowed_cscve         e         Part select index_in_allowed_cscve         e         Part select index_in_allowed_cscve         e         Part select index_in_allowed_cscve										at line @
vee csc prts index_out_of_name_for_var_cscve e Bus part select [@ index @ out of tang variable @ at line @	vee	CSC	prts	bus_prts_for_var_out_of_range_cscve	е					Bus part select [@:@] for variable @ out of range
vee csc prts ill_token_in_prts_cscve e lllegal token in part est incomplete_prts_specification_cscve e lncomplete_prts_specification_cscve e lncomplete_prts_specification_cscve e lncomplete_prts_specification_cscve e lncomplete_prts_specification_cscve e lncomplete_prts_specification_cscve e lnlegal index in part select csc prts ill_index_in_prts_cscve e lnlegal index in part select index in part select csc prts negative_index_in_prts_not_allowed_cscve e lnlegal index in part select csc not allowed in e lncomplete_specification est in part select csc not allowed in e lncomplete_specification est in part select index or reversed [sc :0] [e should be [e]	VEE	CSC	nrts	hus nots index out of name for var oscye	P					
Vee         CSC         pfts         ill_token_in_prts_cscve         e         Illiggal token in parts @ at line @ at line @ incomplete part sel specification at line incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete part select index or select @ not allowed incomplete gate incomplete part select @ not allowed incomplete part se	100	000	prio	545_p165_ind5X_641_61_indino_161_v4i1_66646						index @ out of range for
vee         csc         prts         incomplete_prts_specification_cscve         e         Incomplete_part set specification @ at line get incomplete part set specification @ at line @ specification @ at line @ at line @ the part set specification provided in the part set specification of at line with the part set specification of at line @ at line @ the part set specification of at line with specification of at line with specification of at line part set specification of a line get specification of the part set specification of a line get specification of the part set specificatio	vee	CSC	prts	ill_token_in_prts_cscve	е					Illegal token in part select
Vee         csc         prts         ill_index_in_prts_cscve         e         lliegal index in parts @ at line @ at line @ select @ not allowe line @ should be [@ : @] at @ should be [@ : @] at @ wee csc prts         prts_index_order_reversed_cscve         e         Part select index or reversed @ : @] (@ should be [@ : @] at @ should be [@ : @] at line @ should be	vee	CSC	prts	incomplete_prts_specification_cscve	е					Incomplete part select
vee         csc         prts         negative_index_in_prts_not_allowed_cscve         e         Negative index in pselect @ not allowed line @ line with line @ line @ line with line @ line with line @ line @ line with line @ lin	vee	CSC	prts	ill_index_in_prts_cscve	е					Illegal index in part select
vee   csc   prts   prts_index_order_reversed_cscve   e   Part select index or reversed [@ : @] [@ : @] a   @	vee	CSC	prts	negative index in prts not allowed cscve	е					Negative index in part
vee         csc         prts         prts_index_order_reversed_cscve         e         Part select index or reversed [@ : @] [@ should be [@ : @] and well and well are should be [@ : @] and well are should be [well are sho										select @ not allowed at
vee       csc       prts       index_vec_over_max_size_cscve       w       Vector index @ excetthe size of the vector the size of the vector lindex truncated at lire vector bit section index at line @         vee       csc       prts       x_or_zin_vec_bit_select_index_cscve       e       x_or_zin_vector bit section index_at line @         vee       csc       real       real_cscve       e       Real @ at line @         vee       csc       real       real_in_assn_cscve       e       Real @ in assignen at line @         vee       csc       real       real_in_csi_cscve       e       Real @ in comparain at line @         vee       csc       real       real_in_comparaison_cscve       e       Real @ in comparain at line @         vee       csc       rel       ill_rel_obj_type_cscve       e       lllegal release object type at line @         vee       csc       scop       var_erd_in_scope_cscve       e       Variable @ redirine scope @ at line @         vee       csc       simr       inefficient_op_not_a_power_of_2_cscve       e       Division/modulus be not a power linefficient simulation operation. at line @         vee       csc       simr       simr_multiple_init_blk_force_cscve       w       Multiple initial bloc force @ .Unpredicte simulation result at @ .incomplete sensitivity orce	vee	CSC	prts	prts_index_order_reversed_cscve	е					Part select index order
vee         csc         prts         index_vec_over_max_size_cscve         w         Vector index @ exception index truncated at life size of the vector index truncated at life with extended at life with extended at life index truncated at life index truncated at life index at line @           vee         csc         real         real_cscve         e         Real @ in assigner at line @           vee         csc         real         real_in_assn_cscve         e         Real @ in cassigner at line @           vee         csc         real         real_in_csi_cscve         e         Real @ in cassigner at line @           vee         csc         real         real_in_csi_cscve         e         Real @ in cassigner at line @           vee         csc         real         real_in_csi_cscve         e         Real @ in cassigner at line @           vee         csc         real         real_in_csi_cscve         e         Real @ in cassigner at line @           vee         csc         real         real_in_csi_cscve         e         Real @ in cassigner at line @           vee         csc         real         real_in_csi_cscve         e         Illegal relaase object           vee         csc         simr         vee         csc         vee         vee         vee         vee         vee										should be [@ : @] at line
Index truncated at lir   vee	vee	CSC	prts	index_vec_over_max_size_cscve	w					Vector index @ exceeds
vee         csc         real         real_cscve         e         Real @ at line @           vee         csc         real         real_in_assn_cscve         e         Real @ in assignem at line @           vee         csc         real         real_in_csi_cscve         e         Real @ in Case iten line @           vee         csc         real         real_in_comparaison_cscve         e         Real @ in comparaison at line @           vee         csc         rel         ill_rel_obj_type_cscve         e         lllegal release object type at line @           vee         csc         scop         var_erd_in_scope_cscve         e         Variable @ redfine scope @ at line @           vee         csc         simr         inefficient_op_not_a_power_of_2_cscve         e         Division/modulus b number not a power lnefficient simulation operation. at line @           vee         csc         simr         simr_multiple_init_blk_force_cscve         w         Multiple initial bloc force @. Unpredicts simulation result at @           vee         csc         snsl         incomplete_snsl_cscve         w         Incomplete sensitivity @ is not in the sensitist. at line @           vee         csc         snsl         edge_sns_process_contains_data_pin_snsl_cscve         e         Edge sensitive process_contains_data_pin_snsl_cscve<										Index truncated at line @
vee         csc         real         real_in_assn_cscve         e         Real @ in assignem at line @ real_in_csi_cscve           vee         csc         real         real_in_csi_cscve         e         Real @ in comparaison_cscve line @ real_in_comparaison_cscve           vee         csc         real         real_in_comparaison_cscve         e         Real @ in comparaison_cscve line @ real_in_comparaison_cscve           vee         csc         real         ill_rel_obj_type_cscve         e         Illegal release object type at line @ real_in_cscope_cscve           vee         csc         scop         var_erd_in_scope_cscve         e         Variable @ redfinered scope at line @ redfi	vee	CSC	prts	x_or_z_in_vec_bit_select_index_cscve	е					x or z in vector bit select index at line @
vee       csc       real       real_in_csi_cscve       e       Real @ inCase iten line @ line										Real @ at line @
line @										at line @
vee csc rel ill_rel_obj_type_cscve e lllegal release object type at line @ lllegal release object type at line @ vee csc scop var_erd_in_scope_cscve e Variable @ redfine scope @ at line @ scope @ at line @ scope @ at line @ obvision/modulus be number not a power Inefficient simulation operation. at line wee csc simr simr_multiple_init_blk_force_cscve w Multiple initial block force @ . Unpredicts simulation result at @ line obvision/modulus be number not a power Inefficient simulation operation. at line wee csc snsl incomplete_snsl_cscve w line obvision/modulus be number not a power Inefficient simulation operation. at line wee csc snsl incomplete_snsl_cscve w line obvision/modulus be number not a power Inefficient simulation operation. At line weel csc snsl incomplete_snsl_cscve w line obvision/modulus be number not a power Inefficient simulation operation. At line weel csc snsl incomplete_snsl_cscve w line obvision/modulus be number not a power Inefficient simulation operation. At line weel csc snsl incomplete_snsl_cscve w line obvision/modulus be number not a power Inefficient simulation operation. At line weel csc snsl incomplete_snsl_cscve w line obvision/modulus be number not a power Inefficient simulation operation. At line weel csc snsl incomplete_snsl_cscve w line obvision/modulus be number not a power Inefficient simulation operation. At line weel csc snsl incomplete_snsl_cscve w line obvision/modulus be number not a power Inefficient simulation operation. At line weel csc snsl incomplete_snsl_cscve w line obvision/modulus be number not a power line obvision/modulus be n										line @
vee     csc     scop     var_erd_in_scope_cscve     e     Variable @ redfinered redfinered redfinered red red red red red red red red red										at line @
vee csc simr inefficient_op_not_a_power_of_2_cscve e Division/modulus b number not a power Inefficient simulation operation. at line vee csc simr simr_multiple_init_blk_force_cscve w Multiple initial block force @. Unpredicts simulation result at @ is not in the sensitist. at line @ vee csc snsl edge_sns_process_contains_data_pin_snsl_cscve e Edge sensitive process.	vee	csc	rel	ill_rel_obj_type_cscve	е				L	
vee         csc         simr         inefficient_op_not_a_power_of_2_cscve         e         Division/modulus be number not a power Inefficient simulation operation. at line           vee         csc         simr         simr_multiple_init_blk_force_cscve         w         Multiple initial block force @. Unpredicts simulation result at @.           vee         csc         snsl         incomplete_snsl_cscve         w         Incomplete sensitivity @ is not in the sensitist. at line @.           vee         csc         snsl         edge_sns_process_contains_data_pin_snsl_cscve         e         Edge sensitive procestive proces	vee	CSC	scop	var_erd_in_scope_cscve	е					Variable @ redfined in scope @ at line @
vee csc simr simr_multiple_init_blk_force_cscve w Multiple_initial bloc force @. Unpredict simulation result at @  vee csc snsl incomplete_snsl_cscve w Incomplete sensitivity @ is not in the sensitist. at line w list. at line w list. at line w ledge_sns_process_contains_data_pin_snsl_cscve e Edge sensitive procontains a data pin w list. at line w list at line w ledge sns_process_contains_data_pin_snsl_cscve list. at line w ledge_sns_process_contains_data_pin_snsl_cscve list. At line w ledge_sns_process_contains_data_pin_snsl_csc	vee	csc	simr	inefficient_op_not_a_power_of_2_cscve	е					Division/modulus by a
vee     csc     simr     simr_multiple_init_blk_force_cscve     w     Multiple initial block force @. Unpredicts simulation result at @.       vee     csc     snsl     incomplete_snsl_cscve     w     Incomplete sensitivity @ is not in the sensitist. at line @.       vee     csc     snsl     edge_sns_process_contains_data_pin_snsl_cscve     e     Edge sensitive procest contains a data pin of contains a data pin.										Inefficient simulation
vee csc snsl incomplete_snsl_cscve w Incomplete sensitivitt @ is not in the sensit list. at line @ ledge_sns_process_contains_data_pin_snsl_cscve e Edge sensitive procest.	vee	CSC	simr	simr_multiple_init_blk_force_cscve	w					Multiple initial blocks
vee     csc     snsl     incomplete_snsl_cscve     w     Incomplete sensitivity       @ is not in the sensitist. at line @       vee     csc     snsl     edge_sns_process_contains_data_pin_snsl_cscve     e     Edge sensitive procest contains a data pin of contai										simulation result at line
vee csc snsl edge_sns_process_contains_data_pin_snsl_cscve e	vee	CSC	snsl	incomplete_snsl_cscve	W					Incomplete sensitivity list.
vee         csc         snsl         edge_sns_process_contains_data_pin_snsl_cscve         e         Edge sensitive procest contains a data pin or contains.										@ is not in the sensitivity
the sensitivity list at	vee	csc	snsl	edge_sns_process_contains_data_pin_snsl_cscve	е					Edge sensitive process
										the sensitivity list at line
vee         csc         snsl         unsupp_expr_in_snsl_cscve         w         Unsupported Expres	vee	CSC	snsl	unsupp_expr_in_snsl_cscve	W					Unsupported Expression
type @ in sensitivity at line @										type @ in sensitivity list ' at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	CSC	snsl	always_blk_is_miss_snsl_cscve	е					Always block is missing sensitivity list at line @
vee	CSC	snsl	not_all_bits_snsvar_used_csc	е					Not all bus bits of sensitivity variable @ are
vee	CSC	snsl	partial bus decl width cscve	е	?				used in process at line @ partial bus @ declared
	333	00.	paina_505_000_maii_50075						with width @ width @ at line @
vee	CSC	snsl	contains_inst_name_cscve	е					Contains instance name
vee	CSC	snsl	bus_indexed_in_snsl_cscve	е					@ at line @ Bus @ indexed in
vee	CSC	stmt	ill_register_assign_csve	е					sensitivity list at line @ Illegal register
									assignment statement at line @
vee	csc	stmt	null_not_allowed_stmt_cscve	е					Null statement is not allowed here at line @
vee	CSC	stmt	id_expected_FHSexpr_force_stmt_cscve	е					Simple identifier expected for LHS
									Expression in force-statement at line @
vee	CSC	stmt	id_expected_FHSexpr_release_stmt_cscve	е					Simple identifier
									expected for LHS Expression in
									release-statement at line @
vee	CSC	stmt	stmt_ill_accept_only_net_reg_mem_cscve	е					Illegal type @ can only accept net, reg, memory
vee	CSC	stmt	stmt_ill_accept_only_port_reg_mem_cscve	е					at line @ Illegal type @ can only
			<u></u>						accept port, reg, memory at line @
vee	csc	stmt	stmt_ill_accept_only_signal_reg_mem_cscve	е					Illegal type @ can only
									accept signal, reg, memory at line @
vee	CSC	stmt	while_stmt_usage_disc_cscve	W					While statement usage discouraged at line @
vee	CSC	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_cscve	е					Arithmetic operator RHS has one less bit than the
vee	CSC	stmt	ar_op_unequal_lhs_rhs_cscve	е					LHS at line @ Arithmetic operator
									unequal width LHS and RHS at line @
vee	CSC	stmt	ar_op_unequal_var_on_rhs_csc	е					Arithmetic operator unequal width variables
									@ on RHS at line @
vee	CSC	stmt	empty_stmt_csc	е					Empty-statement at line @
vee	CSC	syst	ill_syst_task_arg_cscve	е					Illegal system task @ Argument @ at line @
vee	CSC	syst	csdir_converts_syts_cscve	W				Х	Lower case converts the system task \$realtime
									return value to an integer at line @
vee	CSC	syst	return_var_of_user_used_as_rhs_cscve	w					Return variable of user system task is used as a
V00	csc	task	miss_task_name_stmst_body_csve	е					RHS variable at line @ Task @ body statement
vee			,_						missing at line @
vee	CSC	task task	ill_task_csve ill_use_task_cscve	e					Illegal task @ at line @ Illegal use of task @ at
vee	CSC	task	ask_var_not_decl_cscve	е					line @ Variable @ used but not
vee	CSC	task	task_not_defined_cscve	е					declared at line @ Task @ not defined at
vee	CSC	task	too_few_arg_to_task_cscve	е					line @ Too few arguments
									passed to task @ at line @
vee	csc	task	undefined_task_cscve	е					Undefined task @ at line
vee	CSC	task	syts_output_port_drvs_nonsqs_logic_comp_cscve	w					@ User system task output
									port drives non-sequential logic
vee	CSC	task	undefioned_task_	е					component at line @ Undefined task @ at line
vee	CSC	task	task_decl_error_csve	е					@ Task declaration error at
vee	CSC	task	func_task_parm_cscve	е					line @ Found function
vee	csc	task	unmatched_task_param_cscve	е					parameter @ at line @ Unmatched task
									parameter @ at line @
vee	CSC	tbcd tbcd	found_forever_tbcd_cscve behavioral_code_mod_cscve	e					Found forever at line @ Behavioral code in
vee	CSC	tbcd	behavioral_code_ebt_cscve	е					module @ at line @ Behavioral code in entity
vee	CSC	tbcd	behavioral_code_unit_cscve	е					@ at line @ Behavioral code in unit
									@ at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_v	er Csl	
vee	CSC	tri	instance_not_tri_state_device_cscve	е					Instance name is not a
vee	csc	tri	unsupp_gate_type_tristate_cscve	е					tri-state device at line @ Unsupported gate type @ used for tristate at line @
vee	CSC	tri	tri_not_desgn_gate_contention_cscve	е					Tristate not designed correctly gate @ can cause contention at line @
vee	CSC	tri	unsupp_type_instance_tri_cscve	е					Unsupported type instance type used for tristate @ at line @
vee	CSC	tri	incorrect_cont_assign_stmt_tri_gate_cscve	е					Incorrect continuous assign statement for tristate gate @ at line @
vee	csc	tri	const_assign_to_multidriven_net_cscve	е					Constant (constiznt) assigned to multi-driven Net @ at line @
vee	CSC	tri	const_assign_to_multidriven_port_cscve	е					Constant (constiznt) assigned to multi-driven Port @ at line @
vee	csc	tri	const_assign_to_multidriven_signal_cscve	е					Constant (constiznt) assigned to multi-driven Signal @ at line @
vee	csc	tri	unsupp_expr_for_tri_cscve	е					Unsupported Expression type @ for tristate at line @
vee	CSC	unsy	cs_equality_op_cscve	е					Case equality operator
vee	CSC	unsy	deassign_stmt_cscve	е					== at line @ Deassign statement at line @
vee	csc	unsy	defparam_cscve	е					Defparam at line @
vee	CSC	unsy	dely_ctrl_cscve ev_ctrl_cscve	e					Delay control at line @  Event control at line @
vee	CSC	unsy	time_decl_cscve	е					Time Declaration at line @
vee	csc	unsy	wait_stmt_unsy_cscve misplaced_csdir_ignored_csve	e				Х	Wait statement at line @ Lower case directive in
		cmdl	ill_incdir_path_dir_cmdl_csve						wrong location. Ignored at line @  Illegal +incdir+ path @
vee	csp			е					directory does not exist at line @
vee	csp	cmdl	ill_path_cmdl_csve	е					Illegal -y path @ directory does not exist at line @
vee	csp	cmdl	cmdl_bad_uselib_libtext_csve	е					Bad 'uselib syntax expected dir, file, 'libext or clear , got character-string at line @
vee	csp	cmdl	ill_cmdl_uselib_dir_path_csve	е					Illegal 'uselib directory path @ no such directory at line @
vee	csp	cmnt	vee_csp_cmnt_miss_closing_csve miss_char_case_csve	e					/* comment missing closing */ at line @ Missing character @ at
	-								line @
vee	csp	csi	colon_for_case_csi_csp	е					Colon expected for Case item at line @
vee	csp	cyb	mintypmax_expr_cyb_vcsp	е					Mintypmax Expressions are not supported at line
vee	csp	cyb	found_id_cyb_csv	е					Found event id syntax in the design at line @
vee	csp	cyb	cyb_ev_var_not_supp_csve	е					Event variables are not supported at line @
vee	csp	evc	not_evc_stmt_csve	е					Cannot use event control statement in this position at line @
vee	csp	expr	expr_found_reserved_word_csve	е					Expected identifier but found reserved word @
vee	csp	expr	expr_concatenation_empty_csve	е					at line @ Concatenation empty at line @
vee	csp	expr	ill_operator_expr_csve	е					Illegal operator @ at line
vee	csp	expr	ill_operand_expr_csve	е				+	Illegal operand @ at line
vee	csp	file	cannot_open_file_csve	е					Cannot open file @ at line @
vee	csp	file	line_lenght_overflow_csve	е					Line length overflow line_length @ at line @
vee	csp	file	environ_var_in_filel_csve	е					Environ variable in file list at line @
vee	csp	func	var_redecl_func_csve	е					Variable re-declared as a function @ at line @
vee	csp	func	func_def_multiple_csve	е					Function @ defined in multiple places (list all places it is defined here)

Cat	<b>Phase</b> csp	<b>Type</b> func	Name ill_use_func_csve	W/E	V1995	V2001	Sys_ver	Csl	Desc Illegal use of function @
vee	csp	func	undefined_func_csve	е					at line @ Undefined function @ at
									line @
vee	csp	gate	gate_inst_miss_input_csve	е					Gate instance @ is missing input
vee	csp	inst	inst_both_formal_order_csv	е					connections at line @ Port list cannot contain
VCC	СЭР	IIISt	inst_bottl_tormal_order_csv						both formal to actual
									mappings and ordered port connections at line
vee	csp	inst	ill_mod_inst_name_csve	е					@ Illegal module instance
									@ at line @
vee	csp	inst	ill_entity_inst_name_csve	е					Illegal entity instance @ at line @
vee	csp	inst	ill_unit_inst_name_csve	е					Illegal unit instance @ at line @
vee	csp	inst	empty_parm_mod_inst_csve	е					Empty parameter list for module instantiation @ at
		. ,							line @
vee	csp	inst	empty_parm_ent_inst_csve	е					Empty parameter list for entity instantiation @ at
vee	csp	inst	empty_parm_unit_inst_csve	е					line @ Empty parameter list for
VCC	СОР	iiiot	empty_parm_umc_mst_csvc						unit instantiation @ at
vee	csp	lib	not_open_lib_file_csve	е					line @ Cannot open library file
vee	csp	list	trail comma list vcs	е					@ at line @ Trailing comma in
	334								parentheses enclosed list at line @
vee	csp	list	list_miising_comma_csve	w					Missing comma between
vee	csp	mifc	mifc_port_type_unsupported_csve	е					@ and name at line @ Port type @ unsupported
vee		mmod	mult_vcs_arg_div	е					at line @ Macro @ contains too
vee	csp	minou	muit_vcs_arg_urv	6					many actual arguments
vee	csp	mmod	miss_vcs_arg_div	е					at line @ Macro @ is missing
									some actual arguments at line @
vee	csp	mmod	not_else_vcs_div	е					Unmatched 'else
vee	csp	mmod	not_endif_vcs_div	е					directive at line @ Unmatched 'endif
vee	csp	mmod	not_include_vcs_div	е					directive at line @ Missing filename for
									'include directive at line @
vee	csp	mmod	bad_include_vcs_div	е					Badly formed include
vee	csp	mmod	fmis_include_vcs_div	е					directive at line @ Filename missing in
									#include directive at line @
vee	csp	mod	not_mod_item_csv	е					Not a module item @ at line @
vee	csp	mod	not_mod_entity_item_csv	е					Not a entity item @ at
vee	csp	mod	not_mod_unit_item_csv	е					line @ Not a unit item @ at line
vee	csp	mod	mod miss endmodule csve	е					@ Missing endmodule at
									line @
vee	csp	mod	mod_no_module_found_csve	е					No modules found at line @
vee	csp	mod mod	mod_no_entity_found_csve mod_no_unit_found_csve	e e					No entity found at line @ No unit found at line @
vee	csp	nett	nett_unsupported_reg_csve	e					Unsupported register type @ at line @
vee	csp	num	radix_h_num_vcs	ew					Illegal number radix, 'h
vee	csp	num	radix b num vcs	ew					expected at line @ Illegal number radix, 'b
vee		num	radix_d_num_vcs	ew					expected at line @ Illegal number radix, 'd
	csp								expected at line @
vee	csp	num	radix_o_num_vcs	ew					Illegal number radix; 'o expected at line @
vee	csp	port	ill_formal_port_name_csve	е					Illegal formal port @ at line @
vee	csp	port	implicitly_decl_net_bit_part_select_csve	е					Implicitly declared Net (inferred 1-bit width)
									used with bit/part select
vee	csp	port	implicitly_decl_port_bit_part_select_csve	е					at line @ Implicitly declared Port
									(inferred 1-bit width) used with bit/part select
1/	95-	nc-t	implicitly deal signed bit west select	_					at line @
vee	csp	port	implicitly_decl_signal_bit_part_select_csve	е					Implicitly declared Signal (inferred 1-bit width)
									used with bit/part select at line @
			<u> </u>						

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vee	csp	pp	ill_macronm_match_pp_csve	е		12001	<b>- - - - - - - - - -</b>		Illegal macro name @
									matches existing compiler directive - illegal
									according to IEEE
1/00			nn connet onen file net eviet enve						1364-1995 S at line @
vee	csp	pp	pp_cannot_open_file_not_exist_csve	е					Cannot open include file @, file does not exist at
									line @
vee	csp	pp	pp_cannot_open_file_not_have_read_perm_csve	е					Cannot open include file @, file does not have
									read permission at line
vee	csp	prts	prts_part_select_csve	е					@ Badly formed part select
	ООР	•		Ů					at line @
vee	csp	sdir	synopsys_cdir_csve	W					Found Synopsys compiler directive at line
									. @
vee	csp	sig stmt	not_define_wire_type_csv miss_comma_stmt_vcs	е					Wire type @ at line @ Missing comma at line @
vee	csp	stmt	miss_semicolon_stmt_vcs	e					Missing semi colon at
		-44							line @
vee	csp	stmt stmt	miss_char_stmt_vcs wait_kword_stmt_vcs	e					Missing @ at line @ @ expected at line @
vee	csp	stmt	null_not_allowed_stmt_csve	е					Null statement is not
vee	csp	str	ill str char found csve	е					allowed here at line @ Illegal character @ found
	-								after backslash at line @
vee	csp	sysc	system_call_csve	W					Found system call @ at line @
vee	csp	task	redeclared_var_task_csve	е					Variable re-declared as a
vee	000	task	task def multiple csve						task @ at line @ Task @ defined in
vee	csp	lask	task_del_muttiple_csve	е					multiple places (list all
									places it is defined here)
vee	csp	task	ill_use_task_csve	е					at line @ Illegal use of task @ at
	·								line @
vee	csp	task	cannot_redefine_ve_sytk_csve	е			Х		Cannot redefine Verilog system task @ at line @
vee	csp	task	task_decl_error_csvh	е					Task declaration error at
vee	csp	udir	other_cdir_csve	w					line @ Found other compiler
	-								directive at line @
vee	prp	file	not_dir_name_file_vep	е					Directory @ does not exist at line @
vee	prp	file	cannot_open_file_ppve	е					Cannot open file @ at
vee	prp	pp	not_incl_directive_pp_ppve	е					line @ Empty filename for
100	PiP	PP	110C_1110C_41100011V0_pp_ppV0						'include directive at line
vee	prp	pp	pp_miss_macroname_ve	е					@ Missing macro name at
****	PiP	PP	ppooao	Ů					line @
vee	prp	pp	ill_macroname_pp_ve	е					Illegal macro name @ at line @
vee	prp	pp	pp_text_macro_rec_ve	е					Text macro string used
vee	prp	pp	pp cannot open libfile ppve	е					recursively at line @ Cannot open library file
VCC	PiP	PP							@ at line @
vee	prp	pp	pp_text_macroname_not_defined_ppve	е					Text macro (name) not defined at line @
vee	prp	pp	pp_ifdef_miss_macroname_ppve	е					'ifdef missing macro
1/00	nrn	nn	nn undet miss maeranama nnva						name at line @ 'undef missing macro
vee	prp	pp	pp_undef_miss_macroname_ppve	е					name at line @
vee	prp	pp	pp_miss_endif_directive_ppve	е					Missing 'endif directive at
vee	prp	pp	pp rec include file ppve	е					line @ Recursive INCLUDE file
									@ at line @
vee	prp	pp	cannot_undef_nonexistent_macro	е					Attempt to 'undef a nonexistent macro @ at
									line @
vee	prp	pp	cmdl_arg_used_in_def_ppve	е					Command line argument used in define at line @
vee	prp	pp	pp_undef_macro_ppve	е					Undef @ not defined
vee	vep	blk	multiple_declaration_blk	е					macro at line @ Named block register
		Jt	pio_accia:alidii_biit						@ame declared in
									multiple locations at line @
vee	vep	ccd	misplaced_csdir_ignored_veve	е				х	Lower case directive in
									wrong location. Ignored at line @
vee	vep	cmdl	ill_incdir_path_dir_cmdl_veve	е					Illegal +incdir+ path @
			. –						directory does not exist
vee	vep	cmdl	ill_path_cmdl_veve	е					at line @ Illegal -y path @
									directory does not exist
vee	vep	cmdl	cmdl_bad_uselib_libtext_veve	е					at line @ Bad 'uselib syntax
1	1			1			1		expected dir, file, 'libext

Cat	Phase	Туре	Name	W/E	V1995   V2001   Sys_ver	Csl Desc
		.,,,,			3,0_10	or clear, got
vee	vep	cmdl	ill_cmdl_uselib_dir_path_veve	е		character-string at line @ Illegal 'uselib directory
						path @ no such directory at line @
vee	vep	cmnt	vee_vep_cmnt_miss_closing_veve	е		/* comment missing
vee	vep	csi	miss_char_case_veve	е		closing */ at line @ Missing character @ at
						line @
vee	vep	csi	colon_for_case_csi_vev	е		Colon expected for Case item at line @
vee	vep	cyb	mintypmax_expr_cyb_vvep	е		Mintypmax Expressions
						are not supported at line @
vee	vep	cyb	found_id_cyb_vev	е		Found event id syntax in the design at line @
vee	vep	cyb	cyb_ev_var_not_supp_veve	е		Event variables are not
vee	vep	evc	not_evc_stmt_veve	е		supported at line @ Cannot use event control
						statement in this position at line @
vee	vep	expr	expr_s_vee	е		Expression S at line @
vee	vep	expr	expr_found_reserved_word_veve	е		Expected identifier but found reserved word @
						at line @
vee	vep	expr	expr_concatenation_empty_veve	е		Concatenation empty at line @
vee	vep	expr	ill_operator_expr_veve	е		Illegal operator @ at line
vee	vep	expr	ill_operand_expr_veve	е		@ Illegal operand @ at line
vee	vep	file	cannot open file veve	е		@ Cannot open file @ at
vee	νep			е		line @
vee	vep	file	line_lenght_overflow_veve	е		Line length overflow line_length @ at line @
vee	vep	file	environ_var_in_filel_veve	е		Environ variable in file list
vee	vep	func	var_redecl_func_veve	е		at line @ Variable re-declared as a
		func	func_def_multiple_veve			function @ at line @ Function @ defined in
vee	vep	Turic	runc_der_munipie_veve	е		multiple places (list all
						places it is defined here) at line @
vee	vep	func	ill_use_func_veve	е		Illegal use of function @
vee	vep	func	undefined_func_veve	е		at line @ Undefined function @ at
vee		anto	gate inst miss input veve			line @ Gate instance @ is
vee	vep	gate	gate_inst_miss_input_veve	е		missing input
vee	vep	inst	inst both formal order vev	е		connections at line @ Port list cannot contain
						both formal to actual
						mappings and ordered port connections at line
vee	vep	inst	ill mod inst name veve	е		@ Illegal module instance
						@ at line @
vee	vep	inst	ill_entity_inst_name_veve	е		Illegal entity instance @ at line @
vee	vep	inst	ill_unit_inst_name_veve	е		Illegal unit instance @ at
vee	vep	inst	empty_parm_mod_inst_veve	е		line @ Empty parameter list for
						module instantiation @ at line @
vee	vep	inst	empty_parm_ent_inst_veve	е		Empty parameter list for
						entity instantiation @ at line @
vee	vep	inst	empty_parm_unit_inst_veve	е		Empty parameter list for
						unit instantiation @ at line @
vee	vep	lib	not_open_lib_file_veve	е		Cannot open library file @ at line @
vee	vep	list	trail_comma_list_vcc	е		Trailing comma in
						parentheses enclosed list at line @
vee	vep	list	list_miising_comma_veve	W		Missing comma between
vee	vep	mifc	mifc_port_type_unsupported_veve	е		@ and name at line @ Port type @ unsupported
vee	vep	mmod	mult_vcc_arg_div	е		at line @ Macro @ contains too
			man_voo_arg_arv			many actual arguments
vee	vep	mmod	miss_vcc_arg_div	е		at line @ Macro @ is missing
	- F					some actual arguments
vee	vep	mmod	not_else_vcc_div	е		at line @ Unmatched 'else
vee	vep	mmod	not_endif_vcc_div	е		directive at line @ Unmatched 'endif
	·					directive at line @
vee	vep	mmod	not_include_vcc_div	е		Missing filename for

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
Jui	Tiluoo	1,700	Hamo	1.,_	11000	72001	oyo_ro.	00.	'include directive at line @
vee	vep	mmod	bad_include_vcc_div	е					Badly formed include
vee	vep	mmod	fmis_include_vcc_div	е					directive at line @ Filename missing in
vee	vep	minou	imis_mciade_vcc_div	6					#include directive at line
vee	vep	mod	not_mod_item_vev	е					Not a module item @ at
vee	vep	mod	not_mod_entity_item_vev	е					line @ Not a entity item @ at
vee	vep	mod	not_mod_unit_item_vev	е					line @ Not a unit item @ at line
vee	vep	mod	mod_miss_endmodule_veve	е					@ Missing endmodule at
vee	vep	mod	mod_no_module_found_veve	е					line @ No modules found at line
vee	vep	mod	mod_no_entity_found_veve	е					@ No entity found at line @
vee	vep	mod	mod_no_unit_found_veve	е					No unit found at line @
vee	vep	nett	nett_unsupported_reg_veve	е					Unsupported register type @ at line @
vee	vep	num	radix_h_num_vcc	ew					Illegal number radix, 'h expected at line @
vee	vep	num	radix_b_num_vcc	ew					Illegal number radix, 'b expected at line @
vee	vep	num	radix_d_num_vcc	ew					Illegal number radix, 'd expected at line @
vee	vep	num	radix_o_num_vcc	ew					Illegal number radix; 'o expected at line @
vee	vep	pars	S_stmt_pars_ve	е					Statement S at line @
vee	vep	port	ill_formal_port_name_veev	е					Illegal formal port @ at line @
vee	vep	port	implicitly decl net bit part select veve	е					Implicitly declared Net
			, ,						(inferred 1-bit width) used with bit/part select
									at line @
vee	vep	port	implicitly_decl_port_bit_part_select_veve	е					Implicitly declared Port
									(inferred 1-bit width) used with bit/part select
									at line @
vee	vep	port	implicitly_decl_signal_bit_part_select_veve	е					Implicitly declared Signal
									(inferred 1-bit width) used with bit/part select
									at line @
vee	vep	pp	ill_macronm_match_pp_veve	е					Illegal macro name @ matches existing
									compiler directive - illegal
									according to IEEE 1364-1995 S at line @
vee	vep	pp	pp_cannot_open_file_not_exist_veve	е					Cannot open include file
									@, file does not exist at line @
vee	vep	pp	pp_cannot_open_file_not_have_read_perm_veve	е					Cannot open include file
									@, file does not have
									read permission at line @
vee	vep	pp	include_filne	е					Include file @ not found
vee	vep	prts	prts_part_select_veve	е					at line @ Badly formed part select
		•	. – –						at line @
vee	vep	sdir	synopsys_cdir_veve	w					Found Synopsys compiler directive at line
									@
vee	vep	sig	not_define_wire_type_vev	е					Wire type @ at line @
vee	vep	stmt stmt	miss_comma_stmt_vcc miss_semicolon_stmt_vcc	e					Missing comma at line @ Missing semi colon at
									line @
vee	vep	stmt stmt	miss_char_stmt_vcc wait_kword_stmt_vcc	e e					Missing @ at line @ @ expected at line @
vee	vep	stmt	null_not_allowed_stmt_veve	e					Null statement is not
vee	vep	str	ill_str_char_found_veve	е					allowed here at line @ Illegal character @ found
vee	vep	sysc	system_call_veve	W					after backslash at line @ Found system call @ at
vee	vep	task	redeclared_var_task_veve	е					line @ Variable re-declared as a
	-								task @ at line @
vee	vep	task	task_def_multiple_veve	е					Task @ defined in multiple places (list all
									places it is defined here)
,	,	45 - 1	III 41						at line @
vee	vep	task	ill_use_task_veve	е					Illegal use of task @ at line @
vee	vep	task	cannot_redefine_ve_sytk_veve	е			Х		Cannot redefine Verilog
vee	vep	task	task_decl_error_vevh	е					system task @ at line @ Task declaration error at
vee	vep	udir	other_cdir_veve	w					line @ Found other compiler
									directive at line @
vee	vhp	ccd	misplaced_csdir_ignored_vhve	е	1			Х	Lower case directive in

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
		-71					<b>0</b> ,0		wrong location. Ignored at line @
vee	vhp	cmdl	ill_incdir_path_dir_cmdl_vhve	е					Illegal +incdir+ path @ directory does not exist at line @
vee	vhp	cmdl	ill_path_cmdl_vhve	е					Illegal -y path @ directory does not exist at line @
vee	vhp	cmdl	cmdl_bad_uselib_libtext_vhve	е					Bad 'uselib syntax expected dir, file, 'libext or clear, got
vee	vhp	cmdl	ill_cmdl_uselib_dir_path_vhve	е					character-string at line @ Illegal 'uselib directory path @ no such directory
vee	vhp	cmnt	vee_vhp_cmnt_miss_closing_vhve	е					at line @ /* comment missing
vee	vhp	csi	miss_char_case_vhve	е					closing */ at line @ Missing character @ at
vee	vhp	csi	colon_for_case_csi_vhv	е					line @ Colon expected for Case item at line @
vee	vhp	cyb	mintypmax_expr_cyb_vvhp	е					Mintypmax Expressions are not supported at line
vee	vhp	cyb	found_id_cyb_vhv	е					Found event id syntax in the design at line @
vee	vhp	cyb	cyb_ev_var_not_supp_vhve	е					Event variables are not supported at line @
vee	vhp	evc	not_evc_stmt_vhve	е					Cannot use event control statement in this position at line @
vee	vhp	expr	expr_found_reserved_word_vhve	е					Expected identifier but found reserved word @ at line @
vee	vhp	expr	expr_concatenation_empty_vhve	е					Concatenation empty at line @
vee	vhp	expr	ill_operator_expr_vhve	е					Illegal operator @ at line @
vee	vhp	expr	ill_operand_expr_vhve	е					Illegal operand @ at line @
vee	vhp	file	cannot_open_file_vhve	е					Cannot open file @ at line @
vee	vhp	file	line_lenght_overflow_vhve	е					Line length overflow line_length @ at line @
vee	vhp	file	environ_var_in_filel_vhve	е					Environ variable in file list at line @
vee	vhp	func	var_redecl_func_vhve func_def_multiple_vhve	e e					Variable re-declared as a function @ at line @ Function @ defined in multiple places (list all
vee	vhp	func	ill_use_func_vhve	е					places it is defined here) at line @ Illegal use of function @ at line @
vee	vhp	func	undefined_func_vhve	е					Undefined function @ at line @
vee	vhp	gate	gate_inst_miss_input_vhve	е					Gate instance @ is missing input
vee	vhp	inst	inst_both_formal_order_vhv	е					connections at line @ Port list cannot contain both formal to actual mappings and ordered port connections at line @
vee	vhp	inst	ill_mod_inst_name_vhve	е					Illegal module instance @ at line @
vee	vhp	inst	ill_entity_inst_name_vhve	е					Illegal entity instance @ at line @
vee	vhp	inst	ill_unit_inst_name_vhve	е					Illegal unit instance @ at line @
vee	vhp	inst	empty_parm_mod_inst_vhve	е					Empty parameter list for module instantiation @ at line @
vee	vhp	inst	empty_parm_ent_inst_vhve	е					Empty parameter list for entity instantiation @ at line @
vee	vhp	inst	empty_parm_unit_inst_vhve	е					Empty parameter list for unit instantiation @ at line @
vee	vhp	lib	not_open_lib_file_vhve	е					Cannot open library file @ at line @
vee	vhp	list	trail_comma_list_vch	е					Trailing comma in parentheses enclosed list at line @
vee	vhp	list	list_miising_comma_vhve	w					Missing comma between @ and name at line @
vee	vhp	mifc	mifc_port_type_unsupported_vhve	е					Port type @ unsupported at line @
vee	vhp	mmod	mult_vch_arg_div	е					Macro @ contains too many actual arguments

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc at line @
vee	vhp	mmod	miss_vch_arg_div	е					Macro @ is missing
									some actual arguments at line @
vee	vhp	mmod	not_else_vch_div	е					Unmatched 'else
vee	vhp	mmod	not_endif_vch_div	е					directive at line @ Unmatched 'endif
VCC									directive at line @
vee	vhp	mmod	not_include_vch_div	е					Missing filename for 'include directive at line
									@
vee	vhp	mmod	bad_include_vch_div	е					Badly formed include directive at line @
vee	vhp	mmod	fmis_include_vch_div	е					Filename missing in
									#include directive at line @
vee	vhp	mod	not_mod_item_vhv	е					Not a module item @ at line @
vee	vhp	mod	not_mod_entity_item_vhv	е					Not a entity item @ at line @
vee	vhp	mod	not_mod_unit_item_vhv	е					Not a unit item @ at line
vee	vhp	mod	mod_miss_endmodule_vhve	е					@ Missing endmodule at
vee	vhp	mod	mod_no_module_found_vhve	е					line @ No modules found at line
VCC	•			6					@
vee	vhp vhp	mod mod	mod_no_entity_found_vhve mod_no_unit_found_vhve	е					No entity found at line @ No unit found at line @
vee	vhp	nett	nett_unsupported_reg_vhve	e					Unsupported register
									type @ at line @
vee	vhp	num	radix_h_num_vch	ew					Illegal number radix, 'h expected at line @
vee	vhp	num	radix_b_num_vch	ew					Illegal number radix, 'b
vee	vhp	num	radix_d_num_vch	ew					expected at line @ Illegal number radix, 'd
VCC				CVV					expected at line @
vee	vhp	num	radix_o_num_vch	ew					Illegal number radix; 'o expected at line @
vee	vhp	port	ill_formal_port_name_vhve	е					Illegal formal port @ at
vee	vhp	port	implicitly_decl_net_bit_part_select_vhve	е					line @ Implicitly declared Net
		-							(inferred 1-bit width) used with bit/part select
									at line @
vee	vhp	port	implicitly_decl_port_bit_part_select_vhve	е					Implicitly declared Port (inferred 1-bit width)
									used with bit/part select
vee	vhp	port	implicitly_decl_signal_bit_part_select_vhve	е					at line @ Implicitly declared Signal
VEE	VIIP	port	implicitly_deci_signal_bit_part_select_virve	6					(inferred 1-bit width)
									used with bit/part select at line @
vee	vhp	pp	ill_macronm_match_pp_vhve	е					Illegal macro name @
									matches existing compiler directive - illegal
									according to IEEE
vee	vhp	pp	pp_cannot_open_file_not_exist_vhve	е					1364-1995 S at line @ Cannot open include file
VCC	VIIP	PP	pp_caimot_open_ine_not_exist_vrive						@, file does not exist at
vee	vhp	pp	pp_cannot_open_file_not_have_read_perm_vhve	е					line @ Cannot open include file
VCC	VIIP	PP	pp_caimot_open_me_not_nave_read_peni_viive						@, file does not have
									read permission at line @
vee	vhp	prts	prts_part_select_vhve	е					Badly formed part select
vee	vhp	sdir	synopsys_cdir_vhve	w					at line @ Found Synopsys
	'		· 7 · 1 · 3 · 2 · · · ·						compiler directive at line
vee	vhp	sig	not_define_wire_type_vhv	е					@ Wire type @ at line @
vee	vhp	stmt	miss_comma_stmt_vch	е					Missing comma at line @
vee	vhp	stmt	miss_semicolon_stmt_vch	е					Missing semi colon at line @
vee	vhp	stmt	miss_char_stmt_vch	е					Missing @ at line @
vee	vhp vhp	stmt	wait_kword_stmt_vch null_not_allowed_stmt_vhve	e e					@ expected at line @ Null statement is not
	•								allowed here at line @
vee	vhp	str	ill_str_char_found_vhve	е					Illegal character @ found after backslash at line @
vee	vhp	sysc	system_call_vhve	w					Found system call @ at line @
vee	vhp	task	redeclared_var_task_vhve	е					Variable re-declared as a
vee	vhp	task	task_def_multiple_vhve						task @ at line @ Task @ defined in
vee	νιιρ	ıask	task_uei_multiple_vnve	е					multiple places (list all
									places it is defined here) at line @
vee	vhp	task	ill_use_task_vhve	е					Illegal use of task @ at
vee	vhp	task	cannot_redefine_ve_sytk_vhve	е			Х		line @ Cannot redefine Verilog
	۲۲	-551			I	L	•	1	voinog

Cat	Phase	Туре	Name	W/E	V1995   V2001	Sys ver Csl	Desc
vee	vhp	task	task_decl_error_vhvh	e	1100 12001	oye_rer oe.	system task @ at line @ Task declaration error at
vee	vhp	udir	other_cdir_vhve	W			line @ Found other compiler
vhe	cda	assn	unequal_length_lhs_rhs_cdvh	е			directive at line @ Unequal length LHS and
vhe	cda	assn	unequal_length_lhs_rhs_off_one_bit_cdvh	е			RHS at line @ Unequal length LHS and
							RHS off by one bit at line
vhe	cda	blk	var_not_assigned_in_all_branches_cdve	е			Variable @ not assigned in all branches at line @
vhe	cda	clk	unsupp_logic_operation_cdvh	W			Unsupported logic operation type @. at line
vhe	cda	clk	unsupp_cl_gated_logic_cdvh	w			@ Unsupported gated clock
vhe	cda	clk	unsupp_logic_expr_clk_cdvh	W			logic type. at line @ Unsupported
vho	cda	csi	popopot in injude file adult				logicExpression type @ at line @ Non-constant in include
vhe			noncnst_in_iclude_file_cdvh	е			file @ at line @
vhe	cda	drvc	multiply_drvn_net_nontri_gate_cdvh	W			Multiply drivenNet driven by a non-tristate gate at line @
vhe	cda	drvc	multiply_drvn_port_nontri_gate_cdvh	W			Multiply drivenPort driven by a non-tristate gate at line @
vhe	cda	drvc	multiply_drvn_sig_nontri_gate_cdvh	W			Multiply drivenSignal driven by a non-tristate gate at line @
vhe	cda	drvc	incompatible_driver_net_cdvh	W			Incompatible driver of type @ drivingNet_@
							multi drivenNet of type @ name @ at line @
vhe	cda	drvc	incompatible_driver_port_cdvh	W			Incompatible driver of type @ drivingPort_@
							multi drivenPort of type @ name @ at line @
vhe	cda	drvc	incompatible_driver_sig_cdvh	W			Incompatible driver of type @ drivingSignal_@
							multi drivenSignal of type @ name @ at line @
vhe	cda	expr	unary_op_in_comparison_cdvh	е			Unary op used in comparison at line @
vhe	cda	expr	miss_parenthesis_cdvh	е			Unary op @ with comparison op @
							missing precedence parenthesis at line @
vhe	cda	init	assn_mem_in_init_blk_cdvh	е			Assign memory in initial block at line @
vhe	cda	inst	input_port_drvn_from_inside_mod_cdvh	е			Input port @ being driven from inside of module @
vhe	cda	inst	input_port_drvn_from_inside_entity_cdvh	е			at line @ Input port @ being driven
							from inside of entity @ at line @ Input port @ being driven
vhe	cda	inst	input_port_drvn_from_inside_signal_cdvh	е			from inside of signal @ at line @
vhe	cda	inst	input_port_not_connected_in_parent_mod_cdvh	е			Input port @ not connected in parent
vhe	cda	inst	input_port_not_connected_in_parent_entity_cdvh	е			module at line @ Input port @ not
	044						connected in parent entity at line @
vhe	cda	inst	input_port_not_connected_in_parent_signal_cdvh	е			Input port @ not connected in parent
vhe	cda	mdb	single_comp_contains_multiple_tri_drv_cdvh	W			signal at line @ A single component
							contains multiple tristate drivers at line @
vhe	cda	mdb	unsuppexpr_on_lhs_net_drv_stmt_cdvh	W			Unsupported Expression type type on LHS ofNet driver statement at line
vhe	cda	mdb	unsuppexpr_on_lhs_port_drv_stmt_cdvh	W			@ Unsupported Expression
			,, , , , , , , , , , , , , , , , , , , ,				type type on LHS ofPort driver statement at line
vhe	cda	mdb	unsuppexpr_on_lhs_sig_drv_stmt_cdvh	w			Unsupported Expression type type on LHS
							ofSignal driver statement at line @
vhe	cda	mdb	tri_not_in_top_mod_cdvh	е			Tristate not in top module at line @
vhe	cda	mdb	tri_not_in_top_ent_cdvh	е			Tristate not in top entity at line @
vhe	cda	mdb	tri_not_in_top_sig_cdvh	е			Tristate not in top signal at line @
vhe	cda	mdb	tri_primitive_inst_cdvh	е			Tristate primitive

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_v	er C	sl Desc
vhe	cda	mdb	tri_net_only_one_drvr_cdvh	е					instantiation at line @ Tri Net has only one driver at line @
vhe	cda	mdb	tri_port_only_one_drvr_cdvh	е					Tri Port has only one
vhe	cda	mdb	tri_sig_only_one_drvr_cdvh	е					driver at line @ Tri Signal has only one
vhe	cda	mod	redef_mod_cdvh	е					driver at line @ Redefined module @ at
vhe	cda	mod	redef_ent_cdvh	е					line @ Redefined entity @ at
vhe	cda	mod	redef_signal_cdvh	е					line @ Redefined signal @ at
vhe	cda	net	tri_and_net_only_one_driver_cdvh	е	?				line @ triandNet @ has only one
vhe	cda	net	tri_and_port_only_one_driver_cdvh	е	?				driver at line @ triandPort @ has only
vhe	cda	net	tri_and_sig_only_one_driver_cdvh	е	?				one driver at line @ triandSignal @ has only
vhe	cda	net	var_assn_but_never_ref_cdvh	е					one driver at line @ Variable @ assigned but
									never referenced at line @
vhe	cda	net	var_never_assn_cdvh	е					Variable @ never assigned at line @
vhe	cda	net	var_not_assn_in_all_paths_cdvh	е					Variable @ not being assigned in all paths at
vhe	cda	net	var_not_in_snsl_cdvh	е					line @ Variable @ not in
vhe	cda	net	reg connected to inout in inst cdvh	е					sensitivity list at line @ Reg @ connected to
****	ouu								inout @ in instantiation @ at line @
vhe	cda	net	reg_connectede_to_output_in_inst_cdvh	е					Reg @ connected to output in instantiation at
vhe	cda	net	reg_used_as_output_of_cont_assn_cdvh	е					line @  Reg @ used as output of
VIIC	cua	Het	reg_useu_as_output_or_cont_assir_cuvii	6					continuous assign at line
vhe	cda	net	port_used_prior_to_decl_cdvh	е					Port @ used prior toDeclaration at line @
vhe	cda	num	var_modulus_by_0_cdve	е					Variable @ modulus by zero at line @
vhe	cda	parm	redef_param_cdvh	е					Redefined parameter @ at line @
vhe	cda	рр	redef_macro_cdvh	е					Redefined macro @ at line @
vhe	cda	prts	vec_index_order_incorrect_cdvh	е					Vector index @ order incorrect at line @
vhe	cda	prts	vec_index_truncated_cdvh	е					Vector index @ truncated at line @
vhe	cda	sig	sig_will_float_when_rel_cdvh	е					Signal @ will float when
vhe	cda	sply	output_conncet_to_sply_	е					it is released at line @ Output @ connect to
vhe	cda	stmt	miss_else_stmt_cdvh	е					supply at line @ Missing else statement at
vhe	cda	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_cdvh	е					line @ Arithmetic operator RHS
									has one less bit than the LHS at line @
vhe	cda	stmt	ar_op_unequal_lhs_rhs_cdvh	е					Arithmetic operator unequal width LHS and
vhe	cda	tri	tri_not_in_top_mod_cdvh	е					RHS at line @ Tristate @ not in top
vhe	cda	tri	tri_not_in_top_entity_cdvh	е					module at line @ Tristate @ not in top
vhe	cda	tri	tri_not_in_top_signal_cdvh	е					entity at line @ Tristate @ not in top
vhe	cda	tri	tri_prim_ist_cdvh	е					signal at line @ Tristate primitive
vhe	cdc	assn	x_in_rhs_of_assihnment_cdcvh	е					x in rhs of assignment at
vhe	cdc	assn	z_in_rhs_of_assn_default_csi_cdcvh	е					line @ x in rhs of assignement
									in defaultCase item at line @
vhe	cdc	assn	z_in_rhs_of_assn_cdcvh	е					z in rhs of assignement at line @
vhe	cdc	assn	unequal_length_lhs_rhs_cdcvh	е					Unequal length LHS and RHS at line @
vhe	cdc	assn	unequal_length_lhs_rhs_off_one_bit_cdcvh	е					Unequal length LHS and RHS off by one bit at line
vhe	cdc	ccd	ccd_cdir_must_be_cst_expr_cdcvh	е				>	© CSL directive size must
			· · -						be constant Expression at line @
vhe	cdc	clk	clk_name_not_found_cdir_cdcvh	е				>	
vhe	cdc	clk	expr_sunj_to_different_clk_phases_cdcvh	е					Expression subject to different clock phases at
									line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	cdc	cond	if_case_cond_expr_cdcve	е			-		If/case conditional
									expression @ syntax error at line @
vhe	cdc	cond	if_no_else_cdcve	е					If no else at line @
vhe	cdc	csi	xcsi_not_in_casex_cdcvh	е					xCase item not in casex at line @
vhe	cdc	csi	noncstn_rep_in_conc_cdcvh	е					Non-constant repeator in
vhe	cdc	csi	cond_expr_in_csi_cdcvh	е					concatenation at line @ Conditional Expression
			_ •						inCase item at line @
vhe	cdc	csi	full_case_has_default_cdcvh	е					Full case has default at line @
vhe	cdc	CSS	sns_pragma_full_case_cdcvh	е					Assume a full case, missing default or
									synopsys pragma full
vhe	cdc	decl	decl_array_over_max_size_cdcvh	е					case. at line @ Array @ exceeds
VIIC	cuc	ueci	deci_array_over_max_size_cdcviii						maximum size limit at
vhe	cdc	dely	x_or_z_in_dely_cdcvh	е					line @ x or z in delay at line @
vhe	cdc	dmsn	mem_prts_index_out_of_range_for_mem_cdcvh	е					Memory part select
									[@:@] index @ out range for memory @ at
									line @
vhe	cdc	dmsn	dime_select_for_mem_missing_cdcvh	е					Select for memory @ missing at line @
vhe	cdc	dmsn	dime_index_out_of_bounds_for_mem_cdcvh	е					Index <index> out of</index>
									bounds for memory @. Range [@: @] at line @
vhe	cdc	dmsn	dime_prts_out_of_bounds_for_net_cdcvh	е					Part select [@ : @] out of
									bounds for net @. Range [@:@] at line @
vhe	cdc	dmsn	dime_prts_out_of_bounds_for_port_cdcvh	е					Part select [@ : @] out of bounds for port @.
									Range [@:@] at line @
vhe	cdc	dmsn	dime_prts_out_of_bounds_for_sig_cdcvh	е					Part select [@ : @] out of bounds for signal @.
									Range [@ : @] at line @
vhe	cdc	dmsn	dime_prts_reg_cdcvh	е					Part select [@ : @] reg @. Range [@ : @] at line
									@
vhe	cdc	drvc	incompatible_drvc_for_net_cdcvh	е					Incompatible drivers for Net @ at line @
vhe	cdc	drvc	incompatible_drvc_for_port_cdcvh	е					Incompatible drivers for Port @ at line @
vhe	cdc	drvc	incompatible_drvc_for_sig_cdcvh	е					Incompatible drivers for
vhe	cdc	drvc	drvc_multiple_drive_net_partially_overlap_cdcvh	е					Signal @ at line @ Multiple drive Net
			, ,						partially overlap at line @
vhe	cdc	drvc	drvc_multiple_drive_port_partially_overlap_cdcvh	е					Multiple drive Port partially overlap at line @
vhe	cdc	drvc	drvc_multiple_drive_sig_partially_overlap_cdcvh	е					Multiple drive Signal partially overlap at line @
vhe	cdc	dsgn	dsgn_top_mod_cannot_id_cdcvh	е					Top module @ cannot be
vhe	cdc	dsgn	dsgn_top_entity_cannot_id_cdcvh	е					identified at line @ Top entity @ cannot be
		_	<b>3</b> – 1 – 7 – 1						identified at line @
vhe	cdc	dsgn	dsgn_top_unit_cannot_id_cdcvh	е					Top unit @ cannot be identified at line @
vhe	cdc	dsgn	unit_dsgn_cycle_not_spanning_tree_cdcvh	е					Unit design hierarchy contains a cycle.
									Hierarchy is not a
vhe	cdc	expr	const_expr_nm_var_vhcdc	е					spanning tree. at line @ Constant Expression
V110	000	ОХРІ	oonot_oxpr_mi_vai_vilodo						contains variable @ at
vhe	cdc	expr	const_expr_usage_vhcdc	е					line @ Constant Expression
	ada	-							usage at line @ Part select indices 1-bit
vhe	cdc	expr	expr_prts_indices_1bit_var_cdcvh	е					variable at line @
vhe	cdc	expr	expr_prts_must_be_cst_expr_cdcvh	е					Part select specifier Expression must be
									constant Expression at
vhe	cdc	expr	not_const_expr_cdcvh	е					line @ Repetition multiplier in
									concatenation is not a
									constant Expression at line @
vhe	cdc	expr	ill_bit_select_expr_cdcvh	е					Illegal bit select expression @ at line @
vhe	cdc	expr	repetition_multiplier_in_conc_not_const_expr_cdcvh	W					Repetition multiplier in
									concatenation is not a constant Expression at
									line @
vhe	cdc	expr	int_operand_not_1_bit_cdcvh	w					Logic operator has integer operands instead
									of 1-bit operands at line
vhe	cdc	expr	unsupp_expr_cdcvh	w					@ Unsupported Expression
									type @ at line @

Vision   Code	Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
Main	vhe	cdc	expr	unsupp_operator_cdcvh	w					Unsupported operator type @ at line @
Vie	vhe	cdc	expr	use_of_sg_bit_const_cdcvh	W					
vivo         Odd         Bayor         X_O_Z_In_Cood_code_pep_cdowh         0           vivo         Cod         Bayor         Zero_in_rep_in_coor_cdodowh         0         A zor in conditional serpension of a line of a zoro in_rep_in_coor_cdowh         2         Zoro repeator in of a zoro in_rep_in_coor_cdowh         2         Zoro repeator in of a zoro in_rep_in_coor_cdowh         2         Zoro repeator in of a zoro in_rep_in_coor_cdowh         2         Expression © in relative in_coor_cdowh         3         Expression © in_relative in_coor_cdown         4         Description of a zoro in_coor_cdown         4         Descript	vhe	cdc	expr	unary_op_in_comparison_cdcvh	е					
vivo         Odd         oxpr         2ero_li_ep_li_corec_cdowh         0         Zero repeator in module         Zero repea	vhe	cdc	expr	x_or_z_in_cond_expr_cdcvh	е					x or z in conditional
Veh         Odd         expr         expr_in_mat_port_dir_dodoh         e         Expression 8 in module port dir a time port dire a time	vhe	cdc	expr	zero_in_rep_in_conc_cdcvh	е					Zero repeator in
Separation   Sep	vhe	cdc	expr	expr_in_mod_port_dir_cdcvh	е					Expression @ in module
Vhe         Odd         expr         expr_ins_port_dic_odo/h         e         Expression 8 in unit in 6 in the 6 in of at all the 8 in the 8	vhe	cdc	expr	expr_in_ent_port_dir_cdcvh	е					Expression @ in entity
vho         cdc         expr         expr_im_inst_cochh         0         Expression @ in inst is grant in e@ is grant in e	vhe	cdc	expr	expr_in_sig_port_dir_cdcvh	е					Expression @ in unit port
vhe         cdc         expr         expr_operator_operator_unequal_length_cdown         e         Expression operator of coperands unequal_length at line @ coperands of unequal length at line @ operators of unequal length at line @ coperands of unequal length at line	vhe	cdc	expr	expr_in_inst_cdcvh	е					
vhe         ode         file         cannot_open_filter_specification_file_odown         e         Cannot_open filter_specification_file_odown           vhe         ode         file         Cannot_open_filter_specification_file_odown         e         Cannot_open_filter_specification_file_odown           vhe         ode         file         lifer_specification_file_odown         e         Filter_specification_file_name_cled.           vhe         ode         file         mismatch_end_file_name_cdown         e         Mismatch_end_mame_6_ad_ine_file_name_6_ad_wn           vhe         ode         file         mismatch_end_file_name_cdown         e         Mismatch_end_mame_6_ad_wn           vhe         ode         file         mismatch_end_file_name_cdown         e         Proction_call mismatch_end_mame_6_ad_wn           vhe         ode         file         mismatch_end_file_cdown         e         Prof @ direction_call mismatch_end_mame_6_ad_wn      <	vhe	cdc	expr	expr operator operands unequal lenght cdcvh	е					
vhe         cdc         file         cannot_open_filter_specification_file_cidovh         e         Cannot_open_filter specification_file @ at Inte @ specification file @ starter specification file @ starter specification file of the properties of th			•							operands @ unequal
whe odd file mismatch_mod_file_massing_odcvh e   Filter specification_file_masse_dcovh e   Filter specification_file_name_cdovh e   Filter specification_file_name_cdovh e   Mismatch_between file_name_dcovh e   Mismatch_between file_name_cdovh e   Mismatch_between file_name_dcovh e   Mismatch_between file_name_dcovh e   Mismatch_between file_name_dcovh e   Mismatch_between file_name_dcovh masse_dcovh e   Mismatch_between signal name dcover file_name_dcovh e   Mismatch_between signal name dcover file_name_dcover file_name_dcove	vhe	cdc	file	cannot_open_filter_specification_file_cdcvh	е					Cannot open filter
vhe         cdc         file         mismatch_mod_file_name_cdcvh         e         Mismatch_mod_file_name_cdcvh           vhe         cdc         file         mismatch_end_file_name_cdcvh         e         Mismatch between module name @ and file name module name @ and file	vho	odo	filo	filter enceification file missing adoub						. @
whe         cdc         file         mismatch_mod_file_name_cdcvh         e         Mismatch_mod_file_name @ and file of name @ and file name @ a	vne	cac	ille	iliter_specification_file_missing_cdcvn	е					name @ is missing at
name @ at line @   name @ at line @   name @ at line @   mismatch_ent_file_name_cdcvh   e	vhe	cdc	file	mismatch_mod_file_name_cdcvh	е					Mismatch between
vhe cdc file mismatch_sig_file_name_cdcvh e Mismatch between signal ename @ and file name @ an										
vhe         cdc         file         mismatch_sig_file_name_cdovh         e         Alismatch between signal name @ and file name passed to function @ at file name @ and file name passed to function @ at file name @ and file name passed on function @ at file name @ and file name passed for function @ at file name @ and file name passed for function @ at file name passe	vhe	cdc	file	mismatch_ent_file_name_cdcvh	е					
vhe cdc func too_many_arg_to_func_cdcvh e Port @ disction @ at line @ argument(s) at line @ argument(s) at line @ argument(s) at line @ bottoo_many_arg_to_func_cdcvh e Port @ disction cannot be output at line @ argument(s) at line	vhe	cdc	file	mismatch sig file name cdcvh	е					
whe         cdc         func         func_arg_miss_whodo         e         Prunction call missing argument(s) at line @ argument(s) at line @ argument(s) at line @ vinction cannot be output at line @ vinction @ at line @ vinction expression winction expression expression winction expression expr	*****	040	0							name @ and file name
whe         cdc         func         port_not_output_func_cdvh         e         Port @ direction cannot be output at line @ 1 so boutput at line @ 2 spassed to function @ at line @ 2 spassed to function @ 2 spassed to functio	vhe	cdc	func	func_arg_miss_vhcdc	е					Function call missing
whe         cdc         func         too_many_arg_to_func_cdcvh         e         Too many arguments passed to function @ at line @ store of the function of the store of the store of the function of the store of the function of the store of	vhe	cdc	func	port_not_output_func_cdvh	е					Port @ direction cannot
vhe         cdc         func         too_few_arg_to_func_cdcvh         e         Too few arguments passed to function @ at line @ 10 for few arguments passed to function @ at line @ 10 few arguments passed to function @ at line @ 10 few arguments passed to function @ at line @ 10 few arguments passed to function @ at line @ 10 few arguments passed to function @ at line @ 10 few arguments passed to function @ at line @ 10 few arguments passed to function @ at line @ 10 few arguments passed to function @ at line @ 10 few arguments passed for function @ at line @ 10 few arguments passed for function @ at line @ 10 few arguments passed for function @ at line @ 10 few arguments passed for function @ at line @ 10 few arguments passed for function @ at line @ 10 few arguments passed for function @ at line @ 10 few arguments passed for function @ at line @ 10 few arguments passed for function @ at line @ 10 few arguments passed for function @ at line @ 10 few arguments passed for function @ at line @ 10 few arguments passed for function @ at line @ 10 few arguments passed for function @ at line @ 10 few arguments passed for function @ at line @ 10 few arguments passed for function @ at line @ 10 few arguments passed for function @ at line @ 10 few arguments passed for function @ at line @ 10 few arguments passed for function @ 10 few argume	vhe	cdc	func	too_many_arg_to_func_cdcvh	е					Too many arguments
vhe         cdc         func         undefined_func_cscvh         e         Undefined function @ at line @           vhe         cdc         func         undefined_func_cscvh         e         Undefined function @ at line @           vhe         cdc         func         undefined_func_cdcvh         e         Undefined function @ at line @           vhe         cdc         func         funct_expr_cannot_expnaded_cdcvh         e         Function @ spression @ cannot be expanded at line @           vhe         cdc         func         funct_not_used_in_expr_cdcvh         w         Function @ spression @ cannot be expanded at line @           vhe         cdc         func         func_decl_cdcvh         w         Function @ spression at line @           vhe         cdc         func         func_decl_cdcvh         w         Function @ spression at line @           vhe         cdc         func         func_decl_cdcvh         w         Function @ spression at line @           vhe         cdc         func         func_decl_cdcvh         w         Function @ spression at line @           vhe         cdc         hid         cannot_locate_hier_id_hid_cdcvh         e         Can't locate hier_action @           vhe         cdc         hid         ref_entity_found_in_expr_hid_cdc										line @
vhe         cdc         func         undefined_func_cscvh         e         Undefined function @ at line @ line line line @ line line @ line line line @ line line line line line line @ line line line @ line line line line line line line line	vhe	cdc	func	too_few_arg_to_func_cdcvh	е					
vhe         cdc         func         undefined func_cdcvh         e         Undefined function @ at line @ line @ cannot be expanded at line @ sused in an Expression at line @ cannot be expanded at line @ cannot can	vhe	cdc	func	undefined func cscvh	е					
Vhe         cdc         func         funct_expr_cannot_expnaded_cdcvh         e         Function expression @ cannot be expanded at line @ cannot be expanded at line @ cannot be expanded at line @ sed in an Expression at line @ used in an Expression at line @ used in an Expression at line @ sed in an Expression at line @ line @ the color of the color	vhe	cdc	func		е					
vhe         cdc         func         funct_not_used_in_expr_cdcvh         w         Function @ is not being used in an Expression at line @ sanother type at line @ already declared as another type at line @ already declared as another type at line @ can't locate hierarchical identifier @ at line @ locate hiera										line @
Vhe         cdc         func         funct_not_used_in_expr_cdcvh         w         Function @ is not being used in an Expression at line @ safready declared as another type at line @ already declared as another type at line @ already declared as another type at line @ cannot_locate_hier_id_hid_cdcvh         e         Can't locate hierarchical identifier @ at line @ References a module instance @ found in an Expression hid at line @ References a module instance @ found in an Expression hid at line @ References a unit instance @ found in an expression hid at line @ References a unit instance @ found in an expression hid at line @ References a unit instance @ found in an expression hid at line @ References a unit instance @ found in an expression hid at line @ References a unit instance @ found in an expression hid at line @ References a unit instance @ found in an expression hid at line @ References a unit instance @ found in an expression hid at line @ References a unit instance @ found in an expression hid at line @ References a unit instance @ found in an expression hid at line @ References a unit instance @ found in an expression hid at line @ References a unit instance @ found in an expression hid at line @ References a unit instance @ found in an expression hid at line @ References a unit instance @ found in found line @ References a unit instance @ found in expression hid at line @ References a unit instance @ found in expression hid at line @ References a unit instance @ found in an expression hid at line @ References a unit instance @ found in an expression hid at line @ References a unit instance @ found in an expression hid at line @ In hid does not exist at line @ References and tine @ In hid does not exist at line @ In the design at line @ In the des	*****	000	rano	Tallot_oxp1_sallilot_oxp1laasa_cacv11						cannot be expanded at
Inle @   Function Declaration @ already declared as another type at line @   Function Declaration @ already declared as another type at line @   Can't locate hierarchical identifier @ at line @   References a module instance @ found in an   Expression hid at line @   References a module instance @ found in an   Expression hid at line @   References a unit instance @ found in an   Expression hid at line @   References a unit instance @ found in an   Expression hid at line @   References a unit instance @ found in an   Expression hid at line @   References a unit instance @ found in an   Expression hid at line @   References a unit instance @ found in an   Expression hid at line @   References a unit instance @ found in an   Expression hid at line @   Reference a unit instance @ found in an   Expression hid at line @   Reference a unit instance @ found in an   Expression hid at line @   Reference a unit instance @ found in an   Expression hid at line @   Reference a unit instance @ found in an   Expression hid at line @   Reference a unit instance @ found in an   Expression hid at line @   Reference a unit instance @ found in e   Reference a unit instance @   Instance @ found in e   Reference a unit instance @ found in e   Reference a unit instance @ found in e   Reference a unit instance @   Inst	vhe	cdc	func	funct_not_used_in_expr_cdcvh	w					Function @ is not being
vhe         cdc         hid         cannot_locate_hier_id_hid_cdcvh         e         Can't locate hier anchical inle @ Can't locate hier archical identifier @ at line @ References a module instance @ found in an Expression hid at line @ References a module instance @ found in an Expression hid at line @ References a entity instance @ found in an Expression hid at line @ References a unit instance @ found in an Expression hid at line @ References a unit instance @ found in an Expression hid at line @ References a unit instance @ found in an Expression hid at line @ References a unit instance @ found in an Expression hid at line @ References a unit instance @ found in an Expression hid at line @ References a unit instance @ in hid does not exist at line @ References a unit instance @ in hid does not exist at line @ References a unit instance @ in hid does not exist at line @ Reference not found at line @ Reference not found at line @ Reference not found at line @ References a unit instance @ in hid does not exist at line @ References a unit instance @ in hid does not exist at line @ References a unit instance @ in hid does not exist at line @ Interest at line @ I			,							line @
Vhe         Cdc         hid         cannot_locate_hier_id_hid_cdcvh         e         Can't locate hierarchical identifier @ at line @ ref_minst_found_in_expr_hid_cdcvh         e         Can't locate hierarchical identifier @ at line @ References a module instance @ found in an Expression hid at line @ References a entity instance @ found in an Expression hid at line @ References a entity instance @ found in an Expression hid at line @ References a unit instance @ found in an Expression hid at line @ Reference and in an Expression hid at line @ Reference and instance @ found in an Expression hid at line @ Reference not found in path @ In the design at line @ Reference not found at line @ In the design at line	vhe	cdc	func	func_decl_cdcvh	W					already declared as
vhe         cdc         hid         ref_minst_found_in_expr_hid_cdcvh         e         References a module instance @ found in an Expression hid at line @ References a entity instance @ found in an Expression hid at line @ References a entity instance @ found in an Expression hid at line @ References a unit instance @ found in an Expression hid at line @ References a unit instance @ found in an Expression hid at line @ Reference not found at line @ Reference a unit instance @ found at line @ References a unit instance @ found at line @ References a entity instance @ found at line @ References a entity instance @ found at line @ References a entity instance @ found at line @ References a entity instance @ found at line @ Info does not exist at line @ Unit instance @ in hid does not exist at line @ Unit instance @ in hid does not exist at line @ Unit instance @ in hid does not exist at line @ Info does not exist at	vhe	cdc	hid	cannot_locate_hier_id_hid_cdcvh	е					Can't locate hierarchical
vhe         cdc         hid         ref_entity_found_in_expr_hid_cdcvh         e         References a entity instance @ found in an Expression hid at line @ References a unit instance @ found in an Expression hid at line @ References a unit instance @ found in an Expression hid at line @ Reference a unit instance @ found in an Expression hid at line @ Reference not found at line @ References a unit instance @ found in line @ References a unit line @ Module instance @ found at line @ References a unit line @ References a line @ References a entity line and Expression hid at line @ References a line in hid does not exist at line @ References a unit line @ References a line @ References a line in hid does not exist at line @ References a unit line @ References a line @ References a unit line @ References a line @ Reference line and line and line @ Reference line and line @ Reference line and	vhe	cdc	hid	ref_minst_found_in_expr_hid_cdcvh	е					
vhe         cdc         hid         ref_entity_found_in_expr_hid_cdcvh         e         References a entity instance @ found in an Expression hid at line @ References a unit instance @ found in an Expression hid at line @ References a unit instance @ found in an Expression hid at line @ Reference not found at line @ Reference not found at line @ Reference not found in an Expression hid at line @ Reference not found in an Expression hid at line @ Reference not found in an Expression hid at line @ Reference not found in an Expression hid at line @ Reference not found in an Expression hid at line @ Reference not found in an Expression hid at line @ Reference not found in an Expression hid at line @ References a entity instance @ found in a Expression hid at line @ References a entity instance @ found in a Expression hid at line @ References a entity instance @ found in a Expression hid at line @ References a entity instance @ found in a Expression hid at line @ References a entity instance @ found in expression hid at line @ References a entity instance @ found in expression hid at line @ References a entity instance @ found in expression hid at line @ Unit instance @ in hid does not exist at line @ Unit instance @ in hid does not exist at line @ Unit instance @ in hid does not exist at line @ References a unit in hid does not exist at line @ In the design a										
vhe         cdc         hid         ref_unit_found_in_expr_hid_cdcvh         e         Expression hid at line @ References a unit instance @ found in an Expression hid at line @ expression hid at line @ whe         References a unit instance @ found in an Expression hid at line @ whe cdc         @ reference not found at line @ whe cdc         @ reference not found at line @ whe cdc         Module instance @ in hid does not exist at line @ whe cdc         Module instance @ in hid does not exist at line @ whe cdc         Init instance @ in hid does not exist at line @ whe cdc         Unit instance @ in hid does not exist at line @ whe cdc         Whe cdc         hid mod_found_in_path_in_dsgn_cdcvh         e         Unit instance @ in hid does not exist at line @ whe cdc         Whe cdc will hid does not exist at line @ whe will hid does not exist at line @ whe cdc         Whe cdc will hid does not exist at line @ will hid does not	vhe	cdc	hid	ref_entity_found_in_expr_hid_cdcvh	е					References a entity
instance @ found in an Expression hid at line @  vhe cdc hid hid_reference_not_found_cdcvh e @ reference not found at line @  vhe cdc hid mifc_in_hid_not_exist_cdcvh e Module instance @ in hid does not exist at line @  vhe cdc hid entity_instance_in_hid_not_exist_cdcvh e Entity instance @ in hid does not exist at line @  vhe cdc hid unit_instance_in_hid_not_exist_cdcvh e Unit instance @ in hid does not exist at line @  vhe cdc hid mod_found_in_path_in_dsgn_cdcvh e Module @ found in path @  in the design at line @  vhe cdc hid enity_found_in_path_in_dsgn_cdcvh e Entity @ found in path @  in the design at line @  vhe cdc hid unit_found_in_path_in_dsgn_cdcvh e Hierarchical_id_path_contains_func_cdc e Hierarchical_ID @ path  contains a function at line @  vhe cdc init assn_mem_in_init_blk_cdcvh e Assign memory in initial block at line @	vhe	cdc	hid	ref unit found in ever hid edeath						Expression hid at line @
vhe         cdc         hid         hid_reference_not_found_cdcvh         e         @ reference not found at line @           vhe         cdc         hid         mifc_in_hid_not_exist_cdcvh         e         Module instance @ in hid does not exist at line @           vhe         cdc         hid         entity_instance_in_hid_not_exist_cdcvh         e         Entity instance @ in hid does not exist at line @           vhe         cdc         hid         unit_instance_in_hid_not_exist_cdcvh         e         Unit instance @ in hid does not exist at line @           vhe         cdc         hid         mod_found_in_exist_cdcvh         e         Module @ found in path @ in the design at line @           vhe         cdc         hid         enity_found_in_path_in_dsgn_cdcvh         e         Entity @ found in path @ in the design at line @           vhe         cdc         hid         unit_found_in_path_in_dsgn_cdcvh         e         Unit @ found in path @ in the design at line @ in the design at line @           vhe         cdc         hid         hierarchical_id_path_contains_func_cdc         e         Hierarchical_ID @ path contains a function at line @           vhe         cdc         init         assn_mem_in_init_blk_cdcvh         e         Assign memory in initial block at line @	VIIC	cuc	IIIG	rei_unit_lound_in_expi_nid_cdcvii						instance @ found in an
vhe         cdc         hid         mifc_in_hid_not_exist_cdcvh         e         Module instance @ in hid does not exist at line @           vhe         cdc         hid         entity_instance_in_hid_not_exist_cdcvh         e         Entity instance @ in hid does not exist at line @           vhe         cdc         hid         unit_instance_in_hid_not_exist_cdcvh         e         Unit instance @ in hid does not exist at line @           vhe         cdc         hid         mod_found_in_path_in_dsgn_cdcvh         e         Module @ found in path @ in the design at line @           vhe         cdc         hid         enity_found_in_path_in_dsgn_cdcvh         e         Entity @ found in path @ in the design at line @           vhe         cdc         hid         unit_found_in_path_in_dsgn_cdcvh         e         Unit @ found in path @ in the design at line @           vhe         cdc         hid         hierarchical_id_path_contains_func_cdc         e         Hierarchical ID @ path contains a function at line @           vhe         cdc         init         assn_mem_in_init_blk_cdcvh         e         Assign memory in initial block at line @	vhe	cdc	hid	hid_reference_not_found_cdcvh	е					@ reference not found at
vhe         cdc         hid         entity_instance_in_hid_not_exist_cdcvh         e         Entity instance @ in hid does not exist at line @           vhe         cdc         hid         unit_instance_in_hid_not_exist_cdcvh         e         Unit instance @ in hid does not exist at line @           vhe         cdc         hid         mod_found_in_path_in_dsgn_cdcvh         e         Module @ found in path @ in the design at line @           vhe         cdc         hid         enity_found_in_path_in_dsgn_cdcvh         e         Entity @ found in path @ in the design at line @           vhe         cdc         hid         unit_found_in_path_in_dsgn_cdcvh         e         Unit @ found in path @ in the design at line @           vhe         cdc         hid         hierarchical_id_path_contains_func_cdc         e         Hierarchical ID @ path contains a function at line @           vhe         cdc         init         assn_mem_in_init_blk_cdcvh         e         Assign memory in initial block at line @	vhe	cdc	hid	mifc_in_hid_not_exist_cdcvh	е					Module instance @ in hid
vhe     cdc     hid     unit_instance_in_hid_not_exist_cdcvh     e     Unit instance @ in hid does not exist at line @ Module @ found in path in the design at line @ in the design at l	vhe	cdc	hid	entity_instance_in_hid_not_exist_cdcvh	е					Entity instance @ in hid
vhe       cdc       hid       mod_found_in_path_in_dsgn_cdcvh       e       Module @ found in path @ in the design at line @         vhe       cdc       hid       enity_found_in_path_in_dsgn_cdcvh       e       Entity @ found in path @ in the design at line @ in the design at line @         vhe       cdc       hid       unit_found_in_path_in_dsgn_cdcvh       e       Unit @ found in path @ in the design at line @ in the design at line @ in the design at line @         vhe       cdc       hid       hierarchical_id_path_contains_func_cdc       e       Hierarchical ID @ path contains a function at line @         vhe       cdc       init       assn_mem_in_init_blk_cdcvh       e       Assign memory in initial block at line @	vhe	cdc	hid	unit_instance_in_hid_not_exist_cdcvh	е					
whe cdc hid enity_found_in_path_in_dsgn_cdcvh e Entity @ found in path @  vhe cdc hid unit_found_in_path_in_dsgn_cdcvh e  vhe cdc hid unit_found_in_path_in_dsgn_cdcvh e  vhe cdc hid hierarchical_id_path_contains_func_cdc  vhe cdc hid hierarchical_id_path_contains_func_cdc  vhe cdc init assn_mem_in_init_blk_cdcvh e  whe cdc init assn_mem_in_init_blk_cdcvh e  @ Assign memory in initial block at line @	vhe	cdc	hid		е					
in the design at line @  vhe cdc hid unit_found_in_path_in_dsgn_cdcvh e Unit @ found in path @ in the design at line @  vhe cdc hid hierarchical_id_path_contains_func_cdc e Hierarchical ID @ path contains a function at line @  vhe cdc init assn_mem_in_init_blk_cdcvh e Assign memory in initial block at line @										@ in the design at line @
vhe cdc init assn_mem_in_init_blk_cdcvh e in the design at line @  vhe cdc init assn_mem_in_init_blk_cdcvh e in the design at line @  vhe cdc init assn_mem_in_init_blk_cdcvh e Assign memory in initial block at line @										in the design at line @
vhe     cdc     init     assn_mem_in_init_blk_cdcvh     e     Assign memory in initial block at line @										in the design at line @
vhe     cdc     init     assn_mem_in_init_blk_cdcvh     e     Assign memory in initial block at line @	viie	cuc	HIU	meraromoai_iu_pam_comains_iunc_cuc	е					contains a function at line
	vhe	cdc	init	assn_mem_in_init_blk_cdcvh	е					Assign memory in initial
	vhe	cdc	inst	inst_duplicate_mod_name_cdcvh	е					

Cat	Phase	Туре	Name	W/E V1995	V2001	Sys_ver   Csl	Desc
						port lis	t for module @ at line @
vhe	cdc	inst	inst_duplicate_entity_name_cdcvh	е			ate port @ in the st for entity @ at line @
vhe	cdc	inst	inst_duplicate_unit_name_cdcvh	е			ate port @ in the t for unit @ at line @
vhe	cdc	inst	ill_mod_inst_name_cdcvh	е			module instance @ at line @
vhe	cdc	inst	ill_entity_inst_name_cdcvh	е			entity instance @ at line @
vhe	cdc	inst	ill_unit_inst_name_cdcvh	е		Illegal u	unit instance @ at line @
vhe	cdc	inst	inst_name_defined_mod_cdcvh	е			ance name @
vhe	cdc	inst	inst_name_defined_ent_cdcvh	е		mo Inst alread	dy defined in this dule at line @ ance name @ dy defined in this utity at line @
vhe	cdc	inst	inst_name_defined_unit_cdcvh	е		Inst	ance name @ dy defined in this
vhe	cdc	inst	inst_too_many_bits_cdcvh	е		u Too ma of ins	nit at line @ any bits for port @ stance array @, I @, actual @ at line @
vhe	cdc	inst	inst_port_not_connected_var_cdcvh	е		arra	port' of instance ay 'array' is not cted to variable at
vhe	cdc	inst	inst_insufficient_bits_cdcvh	е		'port' ( 'array	line @ cient bits for port of instance array ', formal number, number at line @
vhe	cdc	inst	inst_mod_name_not_defined_cdcvh	е			name not defined at line @
vhe	cdc	inst	inst_ent_name_not_defined_cdcvh	е		Entity	name not defined at line @
vhe	cdc	inst	inst_unit_name_not_defined_cdcvh	е		Unit na	me not defined at
vhe	cdc	inst	many_mod_inst_param_assign_cdcvh	е		insta assign	line @ many module nce parameter ments (number > nber) at line @
vhe	cdc	inst	many_entity_inst_param_assign_cdcvh	е		Too ma param	any entity instance eter assignments per > rrumber) at line @
vhe	cdc	inst	many_unit_inst_param_assign_cdcvh	е		param	any unit instance eter assignments per > rrumber) at line @
vhe	cdc	inst	complexexpr_cannot_mapped_inout_port_cdcvh	е			ex Expression @ ot be mapped to
vhe	cdc	inst	complexexpr_cannot_mapped_unknown_port_cdcvh	е		inout Compl canno	port @ at line @ ex Expression @ ot be mapped to wn type port @ at line @
vhe	cdc	inst	netdecl_contains_ill_prts_cdcvh	е		contai	eclaration [@: @] ns an illegal part lect at line @
vhe	cdc	inst	regdecl_contains_ill_prts_cdcvh	е		Reg De contai se	eclaration [@ : @] ns an illegal part lect at line @
vhe	cdc	inst	complex_expr_inst_parent_module_cdcvh	е		Expre with po instar	omplex actual ssion associated rt @ of module @ ntiated in parent dule at line @
vhe	cdc	inst	complex_expr_inst_entity_parent_module_cdcvh	е		Co Expre with po instal mo	omplex actual ssion associated ort @ of entity @ ntiated in parent dule at line @
vhe	cdc	inst	complex_expr_inst_unit_parent_module_cdcvh	е		Expre with prinstal	omplex actual ssion associated port @ of unit @ ntiated in parent dule at line @
vhe	cdc	inst	inst_mod_output_port_width_cdcvh	е		Mod @	Output port @ Output port @ Output port width, width ( port-width ) at line @
vhe	cdc	inst	inst_entity_output_port_width_cdcvh	е		wic	@ Output port @ dth mismatch, width ( port-width ) at line @
vhe	cdc	inst	inst_unit_output_port_width_cdcvh	е			© Output port @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl Desc
							-	actual-width ( port-width ) at line @
vhe	cdc	inst	inst_mod_input_port_width_cdcvh	е				Mod @ Input port @
								width mismatch, actual-width ( port-width )
								at line @
vhe	cdc	inst	inst_entity_input_port_width_cdcvh	е				Entity @ Input port @ width mismatch,
								actual-width ( port-width )
vhe	cdc	inst	inst_unit_input_port_width_cdcvh	е				at line @ Unit @ Input port @
								width mismatch,
								actual-width ( port-width ) at line @
vhe	cdc	inst	inst_mod_not_define_cdcvh	е				Module not defined at line @
vhe	cdc	inst	inst_entity_not_define_cdcvh	е				Entity not defined at line
vhe	cdc	inst	inst_unit_not_define_cdcvh	е				@ Unit not defined at line @
vhe	cdc	inst	mifc_port_actual_formal_width_mismatch_cdcvh	w				Module @ instance @
								port @ width mismatch, actual width @ formal
v do o	cdc	inat	ant nort actual formal width mismatch adoub					width @ at line @ Entity @ instance @ port
vhe	cac	inst	ent_port_actual_formal_width_mismatch_cdcvh	W				@ width mismatch,
								actual width @ formal width @ at line @
vhe	cdc	inst	unit_port_actual_formal_width_mismatch_cdcvh	w				Unit @ instance @ port
								@ width mismatch, actual width @ formal
								width @ at line @
vhe	cdc	inst	inst_differs_in_case_from_mod_cdcvh	е				Instance name @ differs in case from module
								name @ at line @
vhe	cdc	inst	inst_differs_in_case_from_ent_cdcvh	е				Instance name @ differs in case from entity name
								@ at line @
vhe	cdc	inst	inst_differs_in_case_from_sig_cdcvh	е				Instance name @ differs in case from signal name
vhe	cdc	loop	undet_init_value_loop_cdcvh	е				@ at line @ Unable to determine init
		•						value for loop at line @
vhe	cdc	loop	undet_limit_loop_cdcvh	е				Unable to determine limit for loop at line @
vhe	cdc	loop	loop_bounds_calculated_int_cdcvh	w				Loop bounds are
								calculated to be integer @, check that this is
			and the section was left as least admit					correct at line @
vhe	cdc	loop	expr_lhs_contains_var_bit_select_cdcvh	W				Expression in lhs of assignment contains a
								variable bit select at line
vhe	cdc	loop	loop_bounds_not_const_cdc	w				Loop bounds are
vhe	cdc	loop	loop ctrl init expr not const cdcvh	w				non-constant at line @  Non-constant loop
				-				bound. Loop control
								variable initialization Expression is not a
								constant Expression at line @
vhe	cdc	loop	loop_term_expr_not_const_cdcve	w				Non-constant loop
								bound. loop terminating Expression could not be
								evaluated to a constant
vhe	cdc	loop	init_expr_reset_by_var_cdcvh	е				at line @ Non-constant loop
VIIIO	odo	юор	:::::_oxp:_:oso(_b)_vai_odovii					bound. initializing
								Expression reset by variable at line @
vhe	cdc	loop	loop_ctrl_var_1_bit_wide_cdcvh	w				The loop control variable
								@ is one bit wide. Check the loop control variable
vhe	cdc	mdb	bad_mdb_net_cdcvh	е				Declaration. at line @ Bad multi-driven Net @
					L			at line @
vhe	cdc	mdb	bad_mdb_port_cdcvh	е				Bad multi-driven Port @ at line @
vhe	cdc	mdb	bad_mdb_signal_cdcvh	е				Bad multi-driven Signal
vhe	cdc	mdb	unsupp_comp_mdb_net_cdcvh	е	?			@ at line @ Unsupported component
								type @ driving in
								multi-driven Net name at line @
vhe	cdc	mdb	unsupp_comp_mdb_port_cdcvh	е	?			Unsupported component
								type @ driving in multi-driven Port name at
- مارر	c d c	m dl-	unquing come made along to devit		2			line @
vhe	cdc	mdb	unsupp_comp_mdb_signal_cdcvh	е	?			Unsupported component type @ driving in
								multi-driven Signal name
								at line @

Cat	Phase	Туре	Name	W/E		V2001	Sys_ver	Csl	Desc
vhe	cdc	mdb	unsupp_comp_drive_mdb_cdcvh	е	?				Unsupported component type @ driving
									multi-driven Net natne at
vhe	cdc	mdb	unsupp_comp_drive_mdb_port_cdcvh	е	?				line @ Unsupported component
VIIC	ouc	mab	unsupp_comp_anve_mab_port_caevii		•				type @ driving
									multi-driven Port natne at line @
vhe	cdc	mdb	unsupp_comp_drive_mdb_signal_cdcvh	е	?				Unsupported component
									type @ driving multi-driven Signal natne
									at line @
vhe	cdc	mdb	mdb_net_driven_by_trns_cdcvh	е					Multiply driven Net driven by transistor primitive
									type @ at line @
vhe	cdc	mdb	mdb_port_driven_by_trns_cdcvh	е					Multiply driven Port driven by transistor
									primitive type @ at line
vhe	cdc	mdb	mdb_sig_driven_by_trns_cdcvh	е					Multiply driven Signal
			_ 6 ,						driven by transistor primitive type @ at line
									@
vhe	cdc	mdb	mdb_unsupp_comp_drvs_net_cdcvh	е					Unsupported component type driving Net drives
									Net connected to
vhe	cdc	mdb	mdb_unsupp_comp_drvs_port_cdcvh	е					multi-driven Net at line @ Unsupported component
****	odo	mab	mas_andapp_domp_arvo_port_dadvii						type driving Port drives
									Port connected to multi-driven Port at line
									@
vhe	cdc	mdb	mdb_unsupp_comp_drvs_sig_cdcvh	е					Unsupported component type driving Signal drives
									Signal connected to multi-driven Signal at line
									@
vhe	cdc	mdb	mdb_incompatible_net_drives_multiple_net_cdcvh	е					Incompatible driver driving tandem Net
									drives Net connected to
vhe	cdc	mdb	mdb_incompatible_port_drives_multiple_port_cdcvh	е					multi-driven Net at line @ Incompatible driver
	000		aspanse_pon_anveeanipre_pon_eacon						driving tandem Port
									drives Port connected to multi-driven Port at line
v h a	292	no alla	madle in a supposible aig drives multiple aig adayte						@ Incompatible driver
vhe	cdc	mdb	mdb_incompatible_sig_drives_multiple_sig_cdcvh	е					driving tandem Net
									drives Net connected to multi-driven Port at line
									@
vhe	cdc	mdb	mdb_unsupp_LHS_concatenation_cdcvh	е					Unsupported LHS concatenation in
									multi-drive 'device at line
vhe	cdc	mdb	mdb_bus_has_too_many_drivers_cdcvh	е					@ Bus has too many
uha	ada	مالہ مم							drivers. at line @
vhe	cdc	mdb	mdb_always_blk_drive_cdcvh	W					Multiple always blocks drive name @ at line @
vhe	cdc	mdb	nontri_gate_drives_mdb_net_cdcvh	W					non-tri-state gate drives multi-driven Net at line @
vhe	cdc	mdb	nontri_gate_drives_mdb_port_cdcvh	W					non-tri-state gate drives
									multi-driven Port at line @
vhe	cdc	mdb	nontri_gate_drives_mdb_sig_cdcvh	w					non-tri-state gate drives
									multi-driven Signal at line
vhe	cdc	mem	mem_prts_cdv	е					Memories do not support
									part select specifier at line @
vhe	cdc	mem	mem_ref_without_index_cdcvh	е					Memory @ referenced
									without index through hierarchical ID @ at line
vho	odo	mom	ill mom adayb						@
vhe	cdc	mem	ill_mem_cdcvh	е					Illegal memory @ at line @
vhe	cdc	mifc	mifc_not_array_cdv	е					Ports may not be an array at line @
vhe	cdc	mifc	port_identifier_mifc_cdcvh	е					Port @ at line @
vhe	cdc	mifc	mod_output_wire_redecl_reg_cdcvh	е					Module @ output port re-declared as type reg
									after use as implicitly
vhe	cdc	mifc	entity_output_wire_redecl_reg_cdcvh	е					declared wire at line @ Entity @ output port
0	545	0	5y_53pai_mio_154551_15g_545711						re-declared as type reg
									after use as implicitly declared wire at line @
vhe	cdc	mifc	unit_output_wire_redecl_reg_cdcvh	е					Unit @ output port
									re-declared as type reg after use as implicitly
							i		

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	cdc	mifc	output_port_is_mem_type_mifc_cdcvh	е					Output port @ is memory type at line @
vhe	cdc	mifc	mifc_inout_port_is_mem_type_cdcvh	е					Inout port @ is memory
vhe	cdc	mifc	mod_output_port_mismatch_actual_witdh_cdcvh	W					type at line @ Module @ output port @
									formal to actual width mismatch at line @
vhe	cdc	mifc	ent_output_port_mismatch_actual_witdh_cdcvh	w					Entity @ output port @
									formal to actual width mismatch at line @
vhe	cdc	mifc	unit_output_port_mismatch_actual_witdh_cdc	W					Unit @ output port @ formal to actual width
		16							mismatch at line @ Port name @ different in
vhe	cdc	mifc	port_name_different_in_upper_lower_case_cdcvh	е					upper lower case at line
vhe	cdc	mifc	port_not_def_in_iodecl_cdcvh	е					@ Port @ not defined in
vhe	cdc	mifc	port_not_def_in_portl_cdcvh	е					ioDeclaration at line @ Port @ not defined in
									port list at line @
vhe	cdc	mifc	port_wiredecl_mismatch_cdcvh	е					Port @ wireDeclaration mismatch at line @
vhe	cdc	mifc	pos_based_null_inst_port_cdcvh	е					Position based null instance port at line @
vhe	cdc	mifc	last_portdecl_contains_trailcomma_cdcvh	е					Last portDeclaration contains a trailing
									comma at line @
vhe	cdc	mins	mins_expr_incompatible_type_cdcvh	е					Expression @ has an incompatible argument
									type @ with the port at line @
vhe	cdc	mins	mins_mod_not_exist_cdcvh	е					Module @ does not exist
vhe	cdc	mins	mins_entity_not_exist_cdcvh	е					at line @ Entity @ does not exist
vhe	cdc	mins	mins_unit_not_exist_cdcvh	е					at line @ Unit @ does not exist at
vhe	cdc	mod	dup_declar_name_mod_cdv	е					line @ Duplicate Declaration of
	cdc								port @ at line @ Illegal module @ at line
vhe		mod	ill_mod_name_cdcvh	е					@
vhe vhe	cdc cdc	mod mod	ill_mod_entity_name_cdcvh ill_mod_unit_name_cdcvh	e					Illegal entity @ at line @ Illegal unit @ at line @
vhe	cdc	mod	mod_mult_decl_string_cdcvh	е					Multiple Declarations of string detected in module
									@ at line @
vhe	cdc	mod	mod_entity_mult_decl_string_cdcvh	е					Multiple Declarations of string detected in entity
vhe	cdc	mod	mod_unit_mult_decl_string_cdcvh	е					@ at line @ Multiple Declarations of
									string detected in unit @ at line @
vhe	cdc	mod	mod_mult_def_cdcvh	е					Module @ defined in multiple places at line @
vhe	cdc	mod	mod_ent_mult_def_cdcvh	е					Entity @ defined in
vhe	cdc	mod	mod_unit_mult_def_cdcvh	е					multiple places at line @ Unit @ defined in
vhe	cdc	mod	mod no module found cdcvh	е					multiple places at line @ No modules found at line
	cdc								@ No entity found at line @
vhe vhe	cdc	mod mod	mod_no_entity_found_cdcvh mod_no_unit_found_cdcvh	e					No unit found at line @
vhe	cdc	mod	failed_find_mod_cdcvh	е					Failed to find module @ at line @
vhe	cdc	mod	failed_find_entity_cdcvh	е					Failed to find entity @ at line @
vhe	cdc	mod	failed_find_unit_cdcvh	е					Failed to find unit @ at
vhe	cdc	mod	empty_mod_cdcvh	е					line @ Empty module at line @
vhe vhe	cdc cdc	mod mod	empty_ent_cdcvh empty_unit_cdcvh	e					Empty entity at line @ Empty unit at line @
vhe	cdc	net	net_implicit_wire_redecl_reg_cdcvh	е					Implicitly declared as a wire @ re-declared as a
		4	and all get in good adout						reg @. at line @
vhe	cdc	net	undecl_net_in_mod_cdcvh	е					Undeclared net @ in module @ at line @
vhe	cdc	net	undecl_port_in_mod_cdcvh	е					Undeclared port @ in module @ at line @
vhe	cdc	net	undecl_sig_in_mod_cdcvh	е					Undeclared signal @ in module @ at line @
vhe	cdc	net	undecl_net_in_ent_cdcvh	е					Undeclared net @ in
vhe	cdc	net	undecl_port_in_ent_cdcvh	е					entity @ at line @ Undeclared port @ in
vhe	cdc	net	undecl_sig_in_ent_cdcvh	е					entity @ at line @ Undeclared signal @ in
vhe	cdc	net	undecl_net_in_sig_cdcvh	е					entity @ at line @ Undeclared net @ in
									signal @ at line @ Undeclared port @ in
vhe	cdc	net	undecl_port_in_sig_cdcvh	е					signal @ at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_v	er Cs	sl Desc
vhe	cdc	net	undecl_sig_in_sig_cdcvh	е		12001	- Ju-		Undeclared signal @ in
vhe	cdc	net	port_used_prior_to_decl_cdcvh	е					signal @ at line @ Port @ used prior
vhe	cdc	net	1bit_with_prts_cdcvh	е					toDeclaration at line @ 1-bit with part select at
vhe	cdc	netd	ill_decl_vec_cdcvh	е					line @ Illegal Declaration of
vhe	cdc	nett	nett_ill_reg_name_cdcvh	е					vector @ at line @ Illegal register @ at line
vhe	cdc	nett	nett_ill_net_name_cdcvh	е					@ Illegal net @ at line @
vhe	cdc	nett	nett_ill_port_name_cdcvh	е					Illegal port @ at line @
vhe	cdc	nett	nett_ill_signal_name_cdcvh	е					Illegal signal @ at line @
vhe	cdc	nett	net_scalar_vect_nett_cdcvh	е					Net declared as both scalar and vector at line
vhe	cdc	nett	port_scalar_vect_nett_cdcvh	е					Port declared as both scalar and vector at line
vhe	cdc	nett	signal_scalar_vect_nett_cdcvh	е					Signal declared as both scalar and vector at line @
vhe	cdc	nett	hot_mux_not_use_bus_connection_net_cdcvh	е					One hot mux can not be used for bus connection between modules Net @ at line @
vhe	cdc	nett	hot_mux_not_use_bus_connection_port_cdcvh	е					One hot mux can not be used for bus connection between modules Port @ at line @
vhe	cdc	nett	hot_mux_not_use_bus_connection_sig_cdcvh	е					One hot mux can not be used for bus connection between modules Signal @ at line @
vhe	cdc	num	not_allowed_width0_num_cdcvh	е					Width 0 not allowed for sized number at line @
vhe	cdc	num	real_num_not_allowed_cdcvh	е					Real numbers not allowed at line @
vhe	cdc	num	found_x_z_in_num_literal_cdcvh	е					Found x and/or z value in number literal at line @
vhe	cdc	num	too_many_digits_in_sized_num_cdcvh	W					Number of digits exceeds the width in a sized number at line @
vhe	cdc	num	divide_by_zero_num_cdcvh	е					Divide by zero at line @
vhe	cdc	num	child_mod_inst_parent_mod_cdcvh	e					Child module @ instantiates parent module @ at line @
vhe	cdc	num	child_ent_inst_parent_ent_cdcvh	е					Child entity @ instantiates entity module @ at line @
vhe	cdc	num	child_sig_inst_parent_sig_cdcvh	е					Child signal @ instantiates signal
vhe	cdc	num	int_decl_incorrect_cdcvh	е					module @ at line @ Integer Declaration incorrect at line @
vhe	cdc	num	int_var_indexed_cdcvh	е					Integer variable inedexed at line @
vhe	cdc	parm	ill_parm_identifier_cdcvh	е					Illegal parameter @ at line @
vhe	cdc	parm	value_of_parm_OS_platform_dependent_cdcvh	W					Parameter select width > 32. The value is OS and platform dependent at line @
vhe	cdc	parm	parm_redefined_cdcvh	W					Parameter @ redefined at line @
vhe	cdc	port	ill_formal_port_name_cdcvh	е					Illegal formal port @ at line @
vhe	cdc	pp	text_redefined_replaced_cdcvh	w					Text macro redefined and replaced @. Previous definition filename, line number @
yda -	64-		andif or also without if the stands	-					New definition filename, line number @ at line @
vhe	cdc	pp	endif_or_else_without_ifdef_cdcvh	е					Endif-or-else-without ifdef at line @
vhe	cdc	prim	z_in_prim_inst_cdcvh type_prts_cdv	e					z in primitive instantiation at line @ Type @ does not support
		•	<i>,</i> – –						part select specifier at line @
vhe	cdc	prts	prts_out_of_range_cdcvh	е					Parameter @[@ : @]part select is out of range at line @
vhe	cdc	prts	ill_prts_inst_array_cdcvh	е					Illegal value for part select of instance array 'name' at line @
vhe	cdc	prts	const_prts_contains_non_const_selector_cdcvh	е					Constant part select @ contains a non-constant selector @ at line @
vhe	cdc	prts	bus_index_prts_for_var_out_of_range_cdcvh	е					Bus index @ integer of

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
		- 7   -							part select [@:@] for variable @ out of range at line @
vhe	cdc	prts	bus_prts_for_var_out_of_range_cdcvh	е					Bus part select [@:@] for variable @ out of range
vhe	cdc	prts	bus_prts_index_out_of_name_for_var_cdcvh	е					at line @ Bus part select [@:@] index @ out of range for
vhe	cdc	prts	ill_token_in_prts_cdcvh	е					variable @ at line @ Illegal token in part select
vhe	cdc	prts	incomplete_prts_specification_cdcvh	е					@ at line @ Incomplete part select
vhe	cdc	prts	ill_index_in_prts_cdcvh	е					specification @ at line @ Illegal index in part select
vhe	cdc	prts	negative_index_in_prts_not_allowed_cdcvh	е					@ at line @  Negative index in part select @ not allowed at
vhe	cdc	prts	prts_index_order_reversed_cdcvh	е					line @ Part select index order reversed [@ : @] [@ : @] should be [@ : @] at line
vhe	cdc	prts	index_vec_over_max_size_cdcvh	W					Vector index @ exceeds the size of the vector.
vhe	cdc	prts	x_or_z_in_vec_bit_select_index_cdcvh	е					Index truncated at line @ x or z in vector bit select
vhe	cdc	simr	inefficient_op_not_a_power_of_2_cdcvh	е					index at line @ Division/modulus by a number not a power of 2. Inefficient simulation operation, at line @
vhe	cdc	simr	simr_multiple_init_blk_force_cdcvh	W					Multiple initial blocks force @. Unpredictable simulation result at line @
vhe	cdc	snsl	incomplete_snsl_cdcvh	w					Incomplete sensitivity list.  @ is not in the sensitivity
vhe	cdc	snsl	edge_sns_process_contains_data_pin_snsl_cdcvh	е					list. at line @ Edge sensitive process contains a data pin @ in the sensitivity list at line @
vhe	cdc	snsl	unsupp_expr_in_snsl_cdcvh	W					Unsupported Expression type @ in sensitivity list ' at line @
vhe	cdc	snsl	partial_bus_decl_width_cdcvh	е	?				partial bus @ declared with width @ width @ at line @
vhe	cdc	snsl	contains_inst_name_cdcvh	е					Contains instance name @ at line @
vhe	cdc	stmt	null_not_allowed_stmt_cdcvh	е					Null statement is not allowed here at line @
vhe	cdc	stmt	stmt_ill_accept_only_net_reg_mem_cdcvh	е					Illegal type @ can only accept net, reg, memory at line @
vhe	cdc	stmt	stmt_ill_accept_only_port_reg_mem_cdcvh	е					Illegal type @ can only accept port, reg, memory
vhe	cdc	stmt	stmt_ill_accept_only_signal_reg_mem_cdcvh	е					at line @ Illegal type @ can only accept signal, reg, memory at line @
vhe	cdc	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_cdcvh	е					Arithmetic operator RHS has one less bit than the LHS at line @
vhe	cdc	stmt	ar_op_unequal_lhs_rhs_cdcvh	е					Arithmetic operator unequal width LHS and RHS at line @
vhe	cdc	stmt	ar_op_unequal_var_on_rhs_cdc	е					Arithmetic operator unequal width variables @ on RHS at line @
vhe	cdc	stmt	empty_stmt_cdc	е					Empty-statement at line
vhe	cdc	syst	return_var_of_user_used_as_rhs_cdcvh	W					Return variable of user system task is used as a RHS variable at line @
vhe	cdc	task	ask_var_not_decl_cdcvh	е					Variable @ used but not declared at line @
vhe	cdc	task	too_many_arg_to_task_cdcve	е					Too many arguments passed to task @ at line @
vhe	cdc	task	too_few_arg_to_task_cdcvh	е					Too few arguments passed to task @ at line
vhe	cdc	tri	instance_not_tri_state_device_cdcvh	е					@ Instance name is not a tri-state device at line @
vhe	cdc	tri	unsupp_gate_type_tristate_cdcvh	е					Unsupported gate type @ used for tristate at line @
vhe	cdc	tri	tri_not_desgn_gate_contention_cdcvh	е					Tristate not designed correctly gate @ can cause contention at line

Cat	Phase	Туре	Name	W/E V	1995 V2001	Sys_ver Csl	Desc
vhe	cdc	tri	unsupp_type_instance_tri_cdcvh	е			Unsupported type instance type used for tristate @ at line @
vhe	cdc	tri	incorrect_cont_assign_stmt_tri_gate_cdcvh	е			Incorrect continuous assign statement for tristate gate @ at line @
vhe	cdc	tri	const_assign_to_multidriven_net_cdcvh	е			Constant (constiznt) assigned to multi-driven Net @ at line @
vhe	cdc	tri	const_assign_to_multidriven_port_cdcvh	е			Constant (constiznt) assigned to multi-driven Port @ at line @
vhe	cdc	tri	const_assign_to_multidriven_signal_cdcvh	е			Constant (constiznt) assigned to multi-driven Signal @ at line @
vhe	cdc	tri	unsupp_expr_for_tri_cdcvh	е			Unsupported Expression type @ for tristate at line @
vhe	csa	assn	unequal_length_lhs_rhs_csvh	е			Unequal length LHS and RHS at line @
vhe	csa	assn	unequal_length_lhs_rhs_off_one_bit_csvh	е			Unequal length LHS and RHS off by one bit at line
vhe	csa	blk	var_not_assigned_in_all_branches_csve	е			Variable @ not assigned in all branches at line @
vhe	csa	clk	unsupp_logic_operation_csvh	w			Unsupported logic operation type @. at line
vhe	csa	clk	unsupp_cl_gated_logic_csvh	w			@ Unsupported gated clock logic type. at line @
vhe	csa	clk	unsupp_logic_expr_clk_csvh	w			Unsupported logicExpression type @
vhe	csa	csi	noncnst_in_iclude_file_csvh	е			at line @ Non-constant in include
vhe	csa	drvc	multiply_drvn_net_nontri_gate_csvh	W			file @ at line @  Multiply drivenNet driven by a non-tristate gate at line @
vhe	csa	drvc	multiply_drvn_port_nontri_gate_csvh	w			Multiply drivenPort driven by a non-tristate gate at
vhe	csa	drvc	multiply_drvn_sig_nontri_gate_csvh	w			line @ Multiply drivenSignal driven by a non-tristate gate at line @
vhe	csa	drvc	incompatible_driver_net_csvh	w			Incompatible driver of type @ drivingNet_@
							multi drivenNet of type @
vhe	csa	drvc	incompatible_driver_port_csvh	w			name @ at line @ Incompatible driver of type @ drivingPort_@
							multi drivenPort of type @ name @ at line @
vhe	csa	drvc	incompatible_driver_sig_csvh	w			Incompatible driver of type @ drivingSignal_@ multi drivenSignal of type
vhe	csa	expr	unary_op_in_comparison_csvh	е			@ name @ at line @ Unary op used in
vhe	csa	expr	miss_parenthesis_csvh	е			comparison at line @ Unary op @ with
							comparison op @ missing precedence parenthesis at line @
vhe	csa	init	assn_mem_in_init_blk_csvh	е			Assign memory in initial block at line @
vhe	csa	inst	input_port_drvn_from_inside_mod_csvh	е			Input port @ being driven from inside of module @ at line @
vhe	csa	inst	input_port_drvn_from_inside_entity_csvh	е			Input port @ being driven from inside of entity @ at line @
vhe	csa	inst	input_port_drvn_from_inside_signal_csvh	е			Input port @ being driven from inside of signal @ at line @
vhe	csa	inst	input_port_not_connected_in_parent_mod_csvh	е			Input port @ not connected in parent module at line @
vhe	csa	inst	input_port_not_connected_in_parent_entitycsvh	е			Input port @ not connected in parent entity at line @
vhe	csa	inst	input_port_not_connected_in_parent_signal_csvh	е			Input port @ not connected in parent signal at line @
vhe	csa	mdb	single_comp_contains_multiple_tri_drv_csvh	w			A single component contains multiple tristate
vhe	csa	mdb	unsuppexpr_on_lhs_net_drv_stmt_csvh	w			drivers at line @ Unsupported Expression type type on LHS ofNet driver statement at line
vhe	csa	mdb	unsuppexpr_on_lhs_port_drv_stmt_csvh	W			@ Unsupported Expression

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									type type on LHS ofPort driver statement at line @
vhe	csa	mdb	unsuppexpr_on_lhs_sig_drv_stmt_csvh	w					Unsupported Expression type type on LHS
									ofSignal driver statement at line @
vhe	csa	mdb	tri_not_in_top_mod_csvh	е					Tristate not in top module at line @
vhe	csa	mdb	tri_not_in_top_ent_csvh	е					Tristate not in top entity at line @
vhe	csa	mdb	tri_not_in_top_sig_csvh	е					Tristate not in top signal at line @
vhe	csa	mdb	tri_primitive_inst_csvh	е					Tristate primitive instantiation at line @
vhe	csa	mdb	tri_net_only_one_drvr_csvh	е					Tri Net has only one driver at line @
vhe	csa	mdb	tri_port_only_one_drvr_csvh	е					Tri Port has only one driver at line @
vhe	csa	mdb	tri_sig_only_one_drvr_csvh	е					Tri Signal has only one driver at line @
vhe	csa	mod	redef_mod_csvh	е					Redefined module @ at line @
vhe	csa	mod	redef_ent_csvh	е					Redefined entity @ at line @
vhe	csa	mod	redef_signal_csvh	е					Redefined signal @ at line @
vhe	csa	net	tri_and_net_only_one_driver_csvh	е	?				triandNet @ has only one driver at line @
vhe	csa	net	tri_and_port_only_one_driver_csvh	е	?				triandPort @ has only
vhe	csa	net	tri_and_sig_only_one_driver_csvh	е	?				one driver at line @ triandSignal @ has only
vhe	csa	net	var_assn_but_never_ref_csvh	е					one driver at line @ Variable @ assigned but never referenced at line
vhe	csa	net	var_never_assn_csvh	е					@ Variable @ never
vhe	csa	net	var_not_assn_in_all_paths_csvh	е					assigned at line @ Variable @ not being assigned in all paths at
vhe	csa	net	var_not_in_snsl_csvh	е					line @ Variable @ not in
vhe	csa	net	reg_connected_to_inout_in_inst_csvh	е					sensitivity list at line @ Reg @ connected to
									inout @ in instantiation @ at line @
vhe	csa	net	reg_connectede_to_output_in_inst_csvh	е					Reg @ connected to output in instantiation at line @
vhe	csa	net	reg_used_as_output_of_cont_assn_csvh	е					Reg @ used as output of continuous assign at line @
vhe	csa	net	port_used_prior_to_decl_csvh	е					Port @ used prior toDeclaration at line @
vhe	csa	num	var_modulus_by_0_csve	е					Variable @ modulus by zero at line @
vhe	csa	parm	redef_param_csvh	е					Redefined parameter @ at line @
vhe	csa	pp	redef_macro_csvh	е					Redefined macro @ at line @
vhe	csa	prts	vec_index_order_incorrect_csvh	е					Vector index @ order incorrect at line @
vhe	csa	prts	vec_index_truncated_csvh	е					Vector index @ truncated at line @
vhe	csa	sig	sig_will_float_when_rel_csvh	е					Signal @ will float when it is released at line @
vhe	csa	sply	output_conncet_to_sply_	е					Output @ connect to
vhe	csa	stmt	miss_else_stmt_csvh	е					supply at line @ Missing else statement at
vhe	csa	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_csvh	е					line @ Arithmetic operator RHS has one less bit than the
vhe	csa	stmt	ar_op_unequal_lhs_rhs_scvh	е					LHS at line @ Arithmetic operator unequal width LHS and
vhe	csa	stmt	ar_op_unequal_var_on_rhs_csvh	е					RHS at line @ Arithmetic operator unequal width variables @ on RHS at line @
vhe	csa	stmt	ar_op_unequal_var_on_rhs_cdvh	е					Arithmetic operator unequal width variables
vhe	csa	tri	tri_not_in_top_mod_csvh	е					@ on RHS at line @ Tristate @ not in top
vhe	csa	tri	tri_not_in_top_entity_csvh	е					module at line @ Tristate @ not in top
vhe	csa	tri	tri_not_in_top_signal_csvh	е					entity at line @  Tristate @ not in top
vhe	csa	tri	tri_prim_ist_csvh	е					signal at line @ Tristate primitive instantiation @ at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	csb	assn	x_in_rhs_of_assihnment_csbvh	е					x in rhs of assignment at line @
vhe	csb	assn	z_in_rhs_of_assn_default_csi_csbvh	е					x in rhs of assignement in defaultCase item at line @
vhe	csb	assn	z_in_rhs_of_assn_csbvh	е					z in rhs of assignement
vhe	csb	assn	unequal_length_lhs_rhs_csbvh	е					at line @ Unequal length LHS and
vhe	csb	assn	unequal_length_lhs_rhs_off_one_bit_csbvh	е					RHS at line @ Unequal length LHS and RHS off by one bit at line
vhe	csb	ccd	ccd_cdir_must_be_cst_expr_csbvh	е				х	@ CSL directive size must be constant Expression
vhe	csb	clk	clk_name_not_found_cdir_csbvh	е				х	at line @ Clock name not found in cslc directive at line @
vhe	csb	clk	expr_sunj_to_different_clk_phases_csbvh	е					Expression subject to different clock phases at
vhe	csb	cond	if_case_cond_expr_csbve	е					line @  If/case conditional expression @ syntax
vhe	csb	cond	if_no_else_csbve	е					error at line @  If no else at line @
vhe	csb	csi	xcsi_not_in_casex_csbvh	е					xCase item not in casex at line @
vhe	csb	csi	noncstn_rep_in_conc_csbvh	е					Non-constant repeator in concatenation at line @
vhe	csb	csi	cond_expr_in_csi_csbvh	е					Conditional Expression inCase item at line @
vhe	csb	csi	full_case_has_default_csbvh	е					Full case has default at line @
vhe	csb	CSS	sns_pragma_full_case_csbvh	е					Assume a full case, missing default or synopsys pragma full case. at line @
vhe	csb	decl	decl_array_over_max_size_csbvh	е					Array @ exceeds maximum size limit at line @
vhe	csb	dely	x_or_z_in_dely_csbvh	е					x or z in delay at line @
vhe	csb	dmsn	mem_prts_index_out_of_range_for_mem_csbvh	е					Memory part select [@:@] index @ out range for memory @ at line @
vhe	csb	dmsn	dime_select_for_mem_missing_csbvh	е					Select for memory @ missing at line @
vhe	csb	dmsn	dime_index_out_of_bounds_for_mem_csbvh	е					Index <index> out of bounds for memory @. Range [@: @] at line @</index>
vhe	csb	dmsn	dime_prts_out_of_bounds_for_net_csbvh	е					Part select [@ : @] out of bounds for net @. Range [@ : @] at line @
vhe	csb	dmsn	dime_prts_out_of_bounds_for_port_csbvh	е					Part select [@ : @] out of bounds for port @. Range [@ : @] at line @
vhe	csb	dmsn	dime_prts_out_of_bounds_for_sig_csbvh	е					Part select [@ : @] out of bounds for signal @. Range [@ : @] at line @
vhe	csb	dmsn	dime_prts_reg_csbvh	е					Part select [@ : @] reg @. Range [@ : @] at line
vhe	csb	drvc	incompatible_drvc_for_net_csbvh	е					Incompatible drivers for Net @ at line @
vhe	csb	drvc	incompatible_drvc_for_port_csbvh	е					Incompatible drivers for Port @ at line @
vhe	csb	drvc	incompatible_drvc_for_sig_csbvh	е					Incompatible drivers for
vhe	csb	drvc	drvc_multiple_drive_net_partially_overlap_csbvh	е					Signal @ at line @ Multiple drive Net partially overlap at line @
vhe	csb	drvc	drvc_multiple_drive_port_partially_overlap_csbvh	е					Multiple drive Port partially overlap at line @
vhe	csb	drvc	drvc_multiple_drive_sig_partially_overlap_csbvh	е					Multiple drive Signal partially overlap at line @
vhe	csb	dsgn	dsgn_top_mod_cannot_id_csbvh	е					Top module @ cannot be identified at line @
vhe	csb	dsgn	dsgn_top_entity_cannot_id_csbvh	е					Top entity @ cannot be identified at line @
vhe	csb	dsgn	dsgn_top_unit_cannot_id_csbvh	е					Top unit @ cannot be identified at line @
vhe	csb	dsgn	unit_dsgn_cycle_not_spanning_tree_csbvh	е					Unit design hierarchy contains a cycle. Hierarchy is not a
vhe	csb	expr	expr_prts_indices_1bit_var_csbvh	е					spanning tree. at line @ Part select indices 1-bit
vhe	csb	expr	expr_prts_must_be_cst_expr_csbvh	е					variable at line @ Part select specifier Expression must be constant Expression at
vhe	csb	expr	not_const_expr_csbvh	е					line @ Repetition multiplier in

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									concatenation is not a constant Expression at line @
vhe	csb	expr	ill_bit_select_expr_csbvh	е					Illegal bit select expression @ at line @
vhe	csb	expr	repetition_multiplier_in_conc_not_const_expr_csbvh	w					Repetition multiplier in
									concatenation is not a constant Expression at
vhe	csb	expr	int_operand_not_1_bit_csbvh	w					line @ Logic operator has
*****	000	одрі	in_oporana_no_ :_bi_obbvii						integer operands instead
									of 1-bit operands at line @
vhe	csb	expr	unsupp_expr_csbvh	W					Unsupported Expression type @ at line @
vhe	csb	expr	unsupp_operator_csbvh	W					Unsupported operator type @ at line @
vhe	csb	expr	use_of_sg_bit_const_csbvh	w					Use of single bit constant at line @
vhe	csb	expr	unary_op_in_comparison_csbvh	е					Unary op used in comparison at line @
vhe	csb	expr	x_or_z_in_cond_expr_csbvh	е					x or z in conditional
vhe	csb	expr	zero_in_rep_in_conc_csbvh	е					expression at line @ Zero repeator in
vhe	csb	expr	expr_in_mod_port_dir_csbvh	е					concatenation at line @ Expression @ in module
vhe	csb	expr	expr_in_ent_port_dir_csbvh	е					port dir at line @ Expression @ in entity
		·							port dir at line @  Expression @ in unit port
vhe	csb	expr	expr_in_sig_port_dir_csbvh	е					dir at line @
vhe	csb	expr	expr_in_inst_csbvh	е					Expression @ in inst i@ at line @
vhe	csb	expr	expr_operator_operands_unequal_lenght_csbvh	е					Expression operator @ operands @ unequal
vhe	csb	file	cannot_open_filter_specification_file_csbvh	е					length at line @ Cannot open filter
VIIC	035	1110	cannot_open_inter_specification_ine_cssviii						specification file @ at line @
vhe	csb	file	filter_specification_file_missing_csbvh	е					Filter specification file
									name @ is missing at line @
vhe	csb	file	mismatch_mod_file_name_csbvh	е					Mismatch between module name @ and file
vhe	csb	file	mismatch_ent_file_name_csbvh	е					name @ at line @ Mismatch between entity
*****	000	0	mionidion_on_mo_namo_ooovii						name @ and file name @ at line @
vhe	csb	file	mismatch_sig_file_name_csbvh	е					Mismatch between signal
									name @ and file name @ at line @
vhe	csb	func	port_not_output_func_csbvh	е					Port @ direction cannot be output at line @
vhe	csb	func	too_many_arg_to_func_csbvh	е					Too many arguments passed to function @ at
vhe	csb	func	too few arg to func csbvh	е					line @ Too few arguments
VIIE	CSD	Turic	too_iew_aig_to_idilc_csbvii	6					passed to function @ at
vhe	csb	func	undefined_func_csbvh	е					line @ Undefined function @ at
vhe	csb	func	funct_expr_cannot_expnaded_csbvh	е					line @ Function expression @
									cannot be expanded at line @
vhe	csb	func	funct_not_used_in_expr_csbvh	w					Function @ is not being used in an Expression at
		t	form deal cabula						line @ Function Declaration @
vhe	csb	func	func_decl_csbvh	W					already declared as
vhe	csb	hid	cannot_locate_hier_id_hid_csbvh	е					another type at line @ Can't locate hierarchical
vhe	csb	hid	ref_minst_found_in_expr_hid_csbvh	е					identifier @ at line @ References a module
									instance @ found in an Expression hid at line @
vhe	csb	hid	ref_entity_found_in_expr_hid_csbvh	е					References a entity instance @ found in an
									Expression hid at line @
vhe	csb	hid	ref_unit_found_in_expr_hid_csbch	е					References a unit instance @ found in an
vhe	csb	hid	hid_reference_not_found_csbvh	е					Expression hid at line @ @ reference not found at
vhe	csb	hid	mifc_in_hid_not_exist_csbvh	е					line @ Module instance @ in hid
									does not exist at line @
vhe	csb	hid	entity_instance_in_hid_not_exist_csbvh	е					Entity instance @ in hid does not exist at line @
vhe	csb	hid	unit_instance_in_hid_not_exist_csbvh	е					Unit instance @ in hid does not exist at line @
vhe	csb	hid	mod_found_in_path_in_dsgn_csbvh	е					Module @ found in path

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc @ in the design at line @
vhe	csb	hid	enity_found_in_path_in_dsgn_csbvh	е					Entity @ found in path @ in the design at line @
vhe	csb	hid	unit_found_in_path_in_dsgn_csbvh	е					Unit @ found in path @
vhe	csb	hid	hierarchical_id_path_contains_func_csb	е					in the design at line @ Hierarchical ID @ path contains a function at line @
vhe	csb	init	assn_mem_in_init_blk_csbvh	е					Assign memory in initial
vhe	csb	inst	inst_duplicate_mod_name_csbvh	е					block at line @ Duplicate port @ in the port list for module @ at
vhe	csb	inst	inst_duplicate_entity_name_csbvh	е					line @ Duplicate port @ in the port list for entity @ at
vhe	csb	inst	inst_duplicate_unit_name_csbvh	е					line @ Duplicate port @ in the port list for unit @ at line @
vhe	csb	inst	ill_mod_inst_name_csbvh	е					Illegal module instance
vhe	csb	inst	ill_entity_inst_name_csbvh	е					@ at line @ Illegal entity instance @
vhe	csb	inst	ill_unit_inst_name_csbvh	е					at line @ Illegal unit instance @ at
vhe	csb	inst	inst_name_defined_mod_csbvh	е					line @ Instance name @ already defined in this
vhe	csb	inst	inst_name_defined_ent_csbvh	е					module at line @ Instance name @ already defined in this
vhe	csb	inst	inst_name_defined_unit_csbvh	е					entity at line @ Instance name @ already defined in this unit at line @
vhe	csb	inst	inst_too_many_bits_csbvh	е					Too many bits for port @ of instance array @, formal @, actual @ at line @
vhe	csb	inst	inst_port_not_connected_var_csbvh	е					Port 'port' of instance array 'array' is not connected to variable at
vhe	csb	inst	inst_insufficient_bits_csbvh	е					line @ Insufficient bits for port 'port' of instance array 'array ', formal number, actual number at line @
vhe	csb	inst	inst_mod_name_not_defined_csbvh	е					Module name not defined at line @
vhe	csb	inst	inst_ent_name_not_defined_csbvh	е					Entity name not defined at line @
vhe	csb	inst	inst_unit_name_not_defined_csbvh	е					Unit name not defined at line @
vhe	csb	inst	many_mod_inst_param_assign_csbvh	е					Too many module instance parameter assignments (number > rrumber) at line @
vhe	csb	inst	many_entity_inst_param_assign_csbvh	е					Too many entity instance parameter assignments (number > rrumber) at line @
vhe	csb	inst	many_unit_inst_param_assign_csbvh	е					Too many unit instance parameter assignments (number > rrumber) at
vhe	csb	inst	complexexpr_cannot_mapped_inout_port_csbvh	е					line @ Complex Expression @ cannot be mapped to inout port @ at line @
vhe	csb	inst	complexexpr_cannot_mapped_unknown_port_csbvh	е					Complex Expression @ cannot be mapped to unknown type port @ at
vhe	csb	inst	netdecl_contains_ill_prts_csbvh	е					line @  Net Declaration [@: @] contains an illegal part select at line @
vhe	csb	inst	regdecl_contains_ill_prts_csbvh	е					Reg Declaration [@ : @] contains an illegal part select at line @
vhe	csb	inst	complex_expr_inst_parent_module_csbvh	е					Complex actual Expression associated with port @ of module @ instantiated in parent module at line @
vhe	csb	inst	complex_expr_inst_entity_parent_module_csbvh	е					Complex actual Expression associated with port @ of entity @ instantiated in parent module at line @
vhe	csb	inst	complex_expr_inst_unit_parent_module_csbvh	е					Complex actual Expression associated with port @ of unit @ instantiated in parent

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc module at line @
vhe	csb	inst	inst_mod_output_port_width_csbvh	е					Mod @ Output port @ width mismatch,
									actual-width ( port-width ) at line @
vhe	csb	inst	inst_entity_output_port_width_csbvh	е					Entity @ Output port @ width mismatch,
									actual-width ( port-width ) at line @
vhe	csb	inst	inst_unit_output_port_width_csbvh	е					Unit @ Output port @ width mismatch,
vhe	csb	inst	inst_mod_input_port_width_csbvh	е					actual-width ( port-width ) at line @ Mod @ Input port @
VIIC	CSD	IIISt	ilist_iliou_iliput_port_widtil_csbvii	6					width mismatch, actual-width ( port-width )
vhe	csb	inst	inst_entity_input_port_width_csbvh	е					at line @ Entity @ Input port @
	002		o_oypapoausos						width mismatch, actual-width ( port-width )
vhe	csb	inst	inst_unit_input_port_width_csbvh	е					at line @ Unit @ Input port @
									width mismatch, actual-width ( port-width )
vhe	csb	inst	inst_mod_not_define_csbvh	е					at line @ Module not defined at
vhe	csb	inst	inst_entity_not_define_csbvh	е					line @ Entity not defined at line
vhe	csb	inst	inst_unit_not_define_csbvh	е					@ Unit not defined at line @
vhe	csb	inst	mifc_port_actual_formal_width_mismatch_csbvh	W					Module @ instance @ port @ width mismatch,
									actual width @ formal width @ at line @
vhe	csb	inst	ent_port_actual_formal_width_mismatch_csbvh	W					Entity @ instance @ port @ width mismatch,
									actual width @ formal width @ at line @
vhe	csb	inst	unit_port_actual_formal_width_mismatch_csbvh	W					Unit @ instance @ port @ width mismatch,
									actual width @ formal width @ at line @
vhe	csb	inst	inst_differs_in_case_from_mod_csbvh	е					Instance name @ differs in case from module
vhe	csb	inst	inst_differs_in_case_from_ent_csbvh	е					name @ at line @ Instance name @ differs in case from entity name
vhe	csb	inst	inst differs in case from sig csbvh	е					@ at line @ Instance name @ differs
VIIC	CSD	IIISt	ilist_ulliers_iii_case_iiUiii_sig_csbvii	6					in case from signal name @ at line @
vhe	csb	loop	undet_init_value_loop_csbvh	е					Unable to determine init value for loop at line @
vhe	csb	loop	undet_limit_loop_csbvh	е					Unable to determine limit for loop at line @
vhe	csb	loop	loop_bounds_calculated_int_csbvh	W					Loop bounds are calculated to be integer
									@, check that this is correct at line @
vhe	csb	loop	expr_lhs_contains_var_bit_select_csbvh	W					Expression in lhs of assignment contains a
									variable bit select at line
vhe	csb	loop	loop_bounds_not_const_csb	W					Loop bounds are non-constant at line @
vhe	csb	loop	loop_ctrl_init_expr_not_const_csbvh	w					Non-constant loop bound. Loop control variable initialization
									Expression is not a constant Expression at
vhe	csb	loop	loop_term_expr_not_const_csbve	w					line @  Non-constant loop
VIIC	CSD	юор	loop_term_expr_not_const_cabve	٧٧					bound. loop terminating Expression could not be
									evaluated to a constant at line @
vhe	csb	loop	init_expr_reset_by_var_csbvh	е					Non-constant loop bound. initializing
L									Expression reset by variable at line @
vhe	csb	loop	loop_ctrl_var_1_bit_wide_csbvh	w					The loop control variable @ is one bit wide. Check
									the loop control variable Declaration. at line @
vhe	csb	mdb	bad_mdb_net_csbvh	е					Bad multi-driven Net @ at line @
vhe	csb	mdb	bad_mdb_port_csbvh	е					Bad multi-driven Port @ at line @
vhe	csb	mdb	bad_mdb_signal_csbvh	е					Bad multi-driven Signal @ at line @
vhe	csb	mdb	unsupp_comp_mdb_net_csbvh	е	?				Unsupported component

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl Desc
							•	type @ driving in multi-driven Net name at
vhe	csb	mdb	unsupp_comp_mdb_port_csbvh	е	?			line @ Unsupported component type @ driving in
								multi-driven Port name at line @
vhe	csb	mdb	unsupp_comp_mdb_signal_csbvh	е	?			Unsupported component
								type @ driving in multi-driven Signal name at line @
vhe	csb	mdb	unsupp_comp_drive_mdb_csbvh	е	?			Unsupported component
								type @ driving multi-driven Net natne at line @
vhe	csb	mdb	unsupp_comp_drive_mdb_port_csbvh	е	?			Unsupported component
								type @ driving multi-driven Port natne at line @
vhe	csb	mdb	unsupp_comp_drive_mdb_signal_csbvh	е	?			Unsupported component type @ driving
								multi-driven Signal natne at line @
vhe	csb	mdb	mdb_net_driven_by_trns_csbvh	е				Multiply driven Net driven
								by transistor primitive type @ at line @
vhe	csb	mdb	mdb_port_driven_by_trns_csbvh	е				Multiply driven Port driven by transistor
								primitive type @ at line @
vhe	csb	mdb	mdb_sig_driven_by_trns_csbvh	е				Multiply driven Signal driven by transistor
								primitive type @ at line @
vhe	csb	mdb	mdb_unsupp_comp_drvs_net_csbvh	е				Unsupported component type driving Net drives
								Net connected to multi-driven Net at line @
vhe	csb	mdb	mdb_unsupp_comp_drvs_port_csbvh	е				Unsupported component type driving Port drives
								Port connected to multi-driven Port at line
vhe	csb	mdb	mdb_unsupp_comp_drvs_sig_csbvh	е				Unsupported component type driving Signal drives
								Signal connected to multi-driven Signal at line
vhe	csb	mdb	mdb_incompatible_net_drives_multiple_net_csbvh	е				@ Incompatible driver
								driving tandem Net
vhe	csb	mdb	mdb_incompatible_port_drives_multiple_port_csbvh	е				multi-driven Net at line @ Incompatible driver driving tandem Port
								drives Port connected to multi-driven Port at line
vhe	csb	mdb	mdb_incompatible_sig_drives_multiple_sig_csbvh	е				@ Incompatible driver
								driving tandem Net drives Net connected to
								multi-driven Port at line @
vhe	csb	mdb	mdb_unsupp_LHS_concatenation_csbvh	е				Unsupported LHS concatenation in
								multi-drive 'device at line @
vhe	csb	mdb	mdb_bus_has_too_many_drivers_csbvh	е				Bus has too many drivers. at line @
vhe	csb	mdb	mdb_always_blk_drive_csbvh	W				Multiple always blocks drive name @ at line @
vhe	csb	mdb	nontri_gate_drives_mdb_net_csbvh	W				non-tri-state gate drives multi-driven Net at line @
vhe	csb	mdb	nontri_gate_drives_mdb_port_csbvh	w				non-tri-state gate drives multi-driven Port at line
vhe	csb	mdb	nontri_gate_drives_mdb_sig_csbvh	W				@ non-tri-state gate drives
								multi-driven Signal at line @
vhe	csb	mem	mem_prts_csv	е				Memories do not support part select specifier at line @
vhe	csb	mem	mem_ref_without_index_csbvh	е				Memory @ referenced without index through
								hierarchical ID @ at line @
vhe	csb	mem	ill_mem_csbvh	е				Illegal memory @ at line @
vhe	csb	mifc	mifc_not_array_csv	е				Ports may not be an array at line @
vhe vhe	csb csb	mifc mifc	port_identifier_mifc_cssbvh mod_output_wire_redecl_reg_csbvh	e e				Port @ at line @ Module @ output port

Cat	Phase	Туре	Name	W/F	V1995   V2001   S	ys_ver   Csl   Desc
Jui	Tildoo	1,700	Numo	****	11000 12001 0	re-declared as type reg
						after use as implicitly declared wire at line @
vhe	csb	mifc	entity_output_wire_redecl_reg_csbvh	е		Entity @ output port
						re-declared as type reg
						after use as implicitly declared wire at line @
vhe	csb	mifc	unit_output_wire_redecl_reg_csbvh	е		Unit @ output port
						re-declared as type reg after use as implicitly
						declared wire at line @
vhe	csb	mifc	output_port_is_mem_type_mifc_csbvh	е		Output port @ is memory
vhe	csb	mifc	mifc_inout_port_is_mem_type_csbvh	е		type at line @ Inout port @ is memory
						type at line @
vhe	csb	mifc	mod_output_port_mismatch_actual_witdh_csbvh	W		Module @ output port @ formal to actual width
						mismatch at line @
vhe	csb	mifc	ent_output_port_mismatch_actual_witdh_csbvh	W		Entity @ output port @ formal to actual width
						mismatch at line @
vhe	csb	mifc	unit_output_port_mismatch_actual_witdh_csb	W		Unit @ output port @
						formal to actual width mismatch at line @
vhe	csb	mifc	port_name_different_in_upper_lower_case_csbvh	е		Port name @ different in
						upper lower case at line @
vhe	csb	mifc	port_not_def_in_iodecl_csbvh	е		Port @ not defined in
						ioDeclaration at line @
vhe	csb	mifc	port_not_def_in_portl_csbvh	е		Port @ not defined in port list at line @
vhe	csb	mifc	port_wiredecl_mismatch_csbvh	е		Port @ wireDeclaration
v do o	aab	mifa	nee beend mult inst next cabula			mismatch at line @ Position based null
vhe	csb	mifc	pos_based_null_inst_port_csbvh	е		instance port at line @
vhe	csb	mifc	last_portdecl_contains_trailcomma_csbvh	е		Last portDeclaration
						contains a trailing comma at line @
vhe	csb	mins	mins_expr_incompatible_type_csbvh	е		Expression @ has an
						incompatible argument type @ with the port at
						line @
vhe	csb	mins	mins_mod_not_exist_csbvh	е		Module @ does not exist
vhe	csb	mins	mins_entity_not_exist_csbvh	е		at line @ Entity @ does not exist
*****			- <b>,</b>			at line @
vhe	csb	mins	mins_unit_not_exist_csbvh	е		Unit @ does not exist at line @
vhe	csb	mod	dup_declar_name_mod_csv	е		Duplicate Declaration of
vho	csb	mad	ill mod name csbvh			port @ at line @  Illegal module @ at line
vhe	CSD	mod	III_IIIOd_Hairie_csbvii	е		@ @
vhe	csb	mod	ill_mod_entity_name_csbvh	е		Illegal entity @ at line @
vhe vhe	csb csb	mod mod	ill_mod_unit_name_csbvh mod_mult_decl_string_csbvh	e		Illegal unit @ at line @ Multiple Declarations of
						string detected in module
vhe	csb	mod	mod_entity_mult_decl_string_csbvh	е		@ at line @ Multiple Declarations of
VIIC	CSD	mou	mod_entity_muit_deci_string_csbvii	6		string detected in entity
			and with most deal attitue and the			@ at line @
vhe	csb	mod	mod_unit_mult_decl_string_csbvh	е		Multiple Declarations of string detected in unit @
						at line @
vhe	csb	mod	mod_mult_def_csbvh	е		Module @ defined in multiple places at line @
vhe	csb	mod	mod_ent_mult_def_csbvh	е		Entity @ defined in
			mand with mouth slot and the			multiple places at line @
vhe	csb	mod	mod_unit_mult_def_csbvh	е		Unit @ defined in multiple places at line @
vhe	csb	mod	mod_no_module_found_csbvh	е		No modules found at line
vhe	csb	mod	mod_no_entity_found_csbvh	е		@ No entity found at line @
vhe	csb	mod	mod_no_unit_found_csbvh	е		No unit found at line @
vhe	csb	mod	failed_find_mod_csbvh	е		Failed to find module @
vhe	csb	mod	failed_find_entity_csbvh	е		at line @ Failed to find entity @ at
			,_			line @
vhe	csb	mod	failed_find_unit_csbvh	е		Failed to find unit @ at line @
vhe	csb	mod	empty_mod_csbvh	е		Empty module at line @
vhe	csb	mod mod	empty_ent_csbvh	е		Empty entity at line @ Empty unit at line @
vhe vhe	csb csb	net	empty_unit_csbvh net_implicit_wire_redecl_reg_csbvh	e		Implicitly declared as a
						wire @ re-declared as a
	ļ			1	1 1 1	reg @. at line @
	ceh	net	unded net in mod cehyh	Δ		
vhe	csb	net	undecl_net_in_mod_csbvh	е		Undeclared net @ in module @ at line @
	csb	net net	undecl_net_in_mod_csbvh undecl_port_in_mod_csbvh	e e		Undeclared net @ in

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	csb	net	undecl_net_in_ent_csbvh	е					module @ at line @ Undeclared net @ in
vhe	csb	net	undecl_port_in_ent_csbvh	е					entity @ at line @ Undeclared port @ in
vhe	csb	net	undecl sig in ent csbvh	е					entity @ at line @ Undeclared signal @ in
vhe	csb	net	undecl net in sig csbvh	е					entity @ at line @ Undeclared net @ in
	csb								signal @ at line @ Undeclared port @ in
vhe		net	undecl_port_in_sig_csbvh	е					signal @ at line @
vhe	csb	net	undecl_sig_in_sig_csbvh	е					Undeclared signal @ in signal @ at line @
vhe	csb	net	port_used_prior_to_decl_csbvh	е					Port @ used prior toDeclaration at line @
vhe	csb	net	1bit_with_prts_csbvh	е					1-bit with part select at line @
vhe	csb	netd	ill_decl_vec_csbvh	е					Illegal Declaration of vector @ at line @
vhe	csb	nett	nett_ill_reg_name_csbvh	е					Illegal register @ at line @
vhe	csb	nett	nett_ill_net_name_csbvh	е					Illegal net @ at line @
vhe	csb	nett	nett_ill_port_name_csbvh	е					Illegal port @ at line @
vhe	csb	nett	nett_ill_signal_name_csbvh	е					Illegal signal @ at line @
vhe	csb	nett	net_scalar_vect_nett_csbvh	е					Net declared as both scalar and vector at line @
vhe	csb	nett	port_scalar_vect_nett_csbvh	е					Port declared as both scalar and vector at line @
vhe	csb	nett	signal_scalar_vect_nett_csbvh	е					Signal declared as both scalar and vector at line @
vhe	csb	nett	hot_mux_not_use_bus_connection_net_csbvh	е					One hot mux can not be used for bus connection between modules Net @
vhe	csb	nett	hot_mux_not_use_bus_connection_port_csbvh	е					at line @ One hot mux can not be used for bus connection between modules Port @ at line @
vhe	csb	nett	hot_mux_not_use_bus_connection_sig_csbvh	е					One hot mux can not be
									used for bus connection between modules Signal @ at line @
vhe	csb	num	not_allowed_width0_num_csbvh	е					Width 0 not allowed for sized number at line @
vhe	csb	num	real_num_not_allowed_csbvh	е					Real numbers not allowed at line @
vhe	csb	num	found_x_z_in_num_literal_csbvh	е					Found x and/or z value in number literal at line @
vhe	csb	num	too_many_digits_in_sized_num_csbvh	W					Number of digits exceeds the width in a sized number at line @
vhe vhe	csb csb	num num	divide_by_zero_num_csbvh child_mod_inst_parent_mod_csbvh	e e					Divide by zero at line @ Child module @ instantiates parent
vhe	csb	num	child_ent_inst_parent_ent_csbvh	е					module @ at line @ Child entity @ instantiates entity module
vhe	csb	num	child_sig_inst_parent_sig_csbvh	е					@ at line @ Child signal @
									instantiates signal module @ at line @
vhe	csb	num	int_decl_incorrect_csbvh	е					Integer Declaration incorrect at line @
vhe	csb	num	int_var_indexed_csbvh	е					Integer variable inedexed at line @
vhe	csb	parm	ill_parm_identifier_cssbvh	е					Illegal parameter @ at line @
vhe	csb	parm	value_of_parm_OS_platform_dependent_csbvh	w					Parameter select width >
									32. The value is OS and platform dependent at line @
vhe	csb	parm	parm_redefined_csbvh	W					Parameter @ redefined at line @
vhe	csb	port	ill_formal_port_name_csbvh	е					Illegal formal port @ at line @
vhe	csb	pp	text_redefined_replaced_csbvh	w					Text macro redefined and replaced @.
									Previous definition filename, line number @
									New definition filename, line number @ at line @
vhe	csb	pp	endif_or_else_without_ifdef_csbvh	е				L	Endif-or-else-without ifdef at line @
vhe	csb	prim	z_in_prim_inst_csbvh	е				L	z in primitive instantiation at line @
vhe	csb	prts	type_prts_csv	е					Type @ does not support part select specifier at

vhe vhe	csb	prts	Name  prts_out_of_range_csbvh		V1995 V2001 S	line @
			p.to_out_or_rungo_osbvii	е		Parameter @[@ : @]part select is out of range at line @
vhe	csb	prts	ill_prts_inst_array_csbvh	е		Illegal value for part select of instance array
	csb	prts	const_prts_contains_non_const_selector_csbvh	е		'name' at line @ Constant part select @ contains a non-constant selector @ at line @
vhe	csb	prts	bus_index_prts_for_var_out_of_range_csbvh	е		Bus index @ integer of part select [@:@] for variable @ out of range
vhe	csb	prts	bus_prts_for_var_out_of_range_csbvh	е		at line @  Bus part select [@:@] for  variable @ out of range  at line @
vhe	csb	prts	bus_prts_index_out_of_name_for_var_csbvh	е		Bus part select [@:@] index @ out of range for variable @ at line @
vhe	csb	prts	ill_token_in_prts_csbvh	е		Illegal token in part select
vhe	csb	prts	incomplete_prts_specification_csbvh	е		@ at line @ Incomplete part select specification @ at line @
vhe	csb	prts	ill_index_in_prts_csbvh	е		Illegal index in part select
vhe	csb	prts	negative_index_in_prts_not_allowed_csbvh	е		@ at line @  Negative index in part select @ not allowed at
vhe	csb	prts	prts_index_order_reversed_csbvh	е		line @ Part select index order reversed [@ : @] [@ : @] should be [@ : @] at line
vhe	csb	prts	index_vec_over_max_size_csbvh	W		Vector index @ exceeds the size of the vector. Index truncated at line @
vhe	csb	prts	x_or_z_in_vec_bit_select_index_csbvh	е		x or z in vector bit select index at line @
vhe	csb	simr	inefficient_op_not_a_power_of_2_csbvh	е		Division/modulus by a number not a power of 2. Inefficient simulation operation. at line @
vhe	csb	simr	simr_multiple_init_blk_force_csbvh	W		Multiple initial blocks force @. Unpredictable simulation result at line @
vhe	csb	snsl	incomplete_snsl_csbvh	W		Incomplete sensitivity list. @ is not in the sensitivity list. at line @
vhe	csb	snsl	edge_sns_process_contains_data_pin_snsl_csbvh	е		Edge sensitive process contains a data pin @ in the sensitivity list at line @
vhe	csb	snsl	unsupp_expr_in_snsl_csbvh	W		Unsupported Expression type @ in sensitivity list ' at line @
vhe	csb	snsl	partial_bus_decl_width_csbvh	е	?	partial bus @ declared with width @ width @ at line @
vhe	csb	snsl	contains_inst_name_csbvh	е		Contains instance name  @ at line @
vhe	csb	stmt	null_not_allowed_stmt_csbvh	е		Null statement is not
vhe	csb	stmt	stmt_ill_accept_only_net_reg_mem_csbvh	е		allowed here at line @ Illegal type @ can only accept net, reg, memory at line @
vhe	csb	stmt	stmt_ill_accept_only_port_reg_mem_csbvh	е		Illegal type @ can only accept port, reg, memory at line @
vhe	csb	stmt	stmt_ill_accept_only_signal_reg_mem_csbvh	е		Illegal type @ can only accept signal, reg, memory at line @
vhe	csb	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_csbvh	е		Arithmetic operator RHS has one less bit than the
vhe	csb	stmt	ar_op_unequal_lhs_rhs_csbvh	е		LHS at line @  Arithmetic operator unequal the land
vhe	csb	stmt	ar_op_unequal_var_on_rhs_csb	е		RHS at line @ Arithmetic operator unequal width variables
vhe	csb	stmt	empty_stmt_csb	е		@ on RHS at line @ Empty-statement at line @
vhe	csb	syst	return_var_of_user_used_as_rhs_csbvh	W		Return variable of user system task is used as a RHS variable at line @
vhe	csb	task	ask_var_not_decl_csbvh	е		Variable @ used but not declared at line @
vhe	csb	task	too_many_arg_to_task_csbve	Ф		Too many arguments passed to task @ at line @

									_
vhe	csb	task	<b>Name</b> too_few_arg_to_task_csbvh	e e	V1995	V2001	Sys_ver	Csl	Too few arguments passed to task @ at line @
vhe	csb	tri	instance_not_tri_state_device_csbvh	е					Instance name is not a
vhe	csb	tri	unsupp_gate_type_tristate_csbvh	е					tri-state device at line @ Unsupported gate type @ used for tristate at line
vhe	csb	tri	tri_not_desgn_gate_contention_csbvh	е					@ Tristate not designed correctly gate @ can cause contention at line
									@
vhe	csb	tri	unsupp_type_instance_tri_csbvh	е					Unsupported type instance type used for tristate @ at line @
vhe	csb	tri	incorrect_cont_assign_stmt_tri_gate_csbvh	е					Incorrect continuous assign statement for tristate gate @ at line @
vhe	csb	tri	const_assign_to_multidriven_net_csbvh	е					Constant (constiznt) assigned to multi-driven Net @ at line @
vhe	csb	tri	const_assign_to_multidriven_port_csbvh	е					Constant (constiznt) assigned to multi-driven Port @ at line @
vhe	csb	tri	const_assign_to_multidriven_signal_csbvh	е					Constant (constiznt) assigned to multi-driven
vhe	csb	tri	unsupp_expr_for_tri_csbvh	е					Signal @ at line @ Unsupported Expression type @ for tristate at line
vhe	CSC	assn	x_in_rhs_of_assihnment_cscvh	е					@ x in rhs of assignment at
vhe	CSC	assn	z_in_rhs_of_assn_default_csi_cscvh	е					line @ x in rhs of assignement in defaultCase item at
vhe	CSC	assn	z_in_rhs_of_assn_cscvh	е					line @ z in rhs of assignement
									at line @
vhe	CSC	assn	unequal_length_lhs_rhs_cscvh	е					Unequal length LHS and RHS at line @
vhe	CSC	assn	unequal_length_lhs_rhs_off_one_bit_cscvh	е					Unequal length LHS and RHS off by one bit at line @
vhe	CSC	ccd	ccd_cdir_must_be_cst_expr_cscvh	е				Х	CSL directive size must be constant Expression at line @
vhe	csc	clk	clk_name_not_found_cdir_cscvh	е				х	Clock name not found in cslc directive at line @
vhe	csc	clk	expr_sunj_to_different_clk_phases_cscvh	е					Expression subject to different clock phases at line @
vhe	CSC	cond	if_case_cond_expr_cscve	е					If/case conditional expression @ syntax error at line @
vhe	CSC	cond	if_no_else_cscve	е					If no else at line @
vne	CSC	CSI	xcsi_not_in_casex_cscvn	е					at line @
vhe	CSC	csi	noncstn_rep_in_conc_cscvh	е					Non-constant repeator in concatenation at line @
vhe	CSC	csi	cond_expr_in_csi_cscvh	е					Conditional Expression inCase item at line @
vhe	CSC	csi	full_case_has_default_cscvh	е					Full case has default at line @
vhe	csc	CSS	sns_pragma_full_case_cscvh	е					Assume a full case, missing default or synopsys pragma full
vhe	CSC	decl	decl_array_over_max_size_cscvh	е					case. at line @ Array @ exceeds maximum size limit at
vhe vhe	CSC	dely dmsn	x_or_z_in_dely_cscvh mem prts index out of range for mem cscvh	e					line @ x or z in delay at line @ Memory part select
VIIC	030	uman	mem_pris_index_out_or_range_ior_mem_cscvii	6					[@:@] index @ out range for memory @ at
vhe	CSC	dmsn	dime_select_for_mem_missing_cscvh	е					line @ Select for memory @
vhe	CSC	dmsn	dime_index_out_of_bounds_for_mem_cscvh	е					missing at line @ Index <index> out of bounds for memory @.</index>
vhe	CSC	dmsn	dime_prts_out_of_bounds_for_net_cscvh	е					Range [@: @] at line @ Part select [@: @] out of bounds for net @. Range
vhe	CSC	dmsn	dime_prts_out_of_bounds_for_port_cscvh	е					[@ : @] at line @ Part select [@ : @] out of bounds for port @.
vhe	CSC	dmsn	dime_prts_out_of_bounds_for_sig_cscvh	е					Range [@ : @] at line @ Part select [@ : @] out of
vhe	CSC	dmsn	dime_prts_reg_cscvh	е					bounds for signal @. Range [@ : @] at line @ Part select [@ : @] reg
			<b>~</b> _						@. Range [@ : @] at line @

Vite   GSC   drice   Incompatible_drice_for_port_cschh   e	Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vho         csc         dive         incompatible_drive_for_sig_cachh         o         Fortil & at line @ 1   Engaged & 2   Engaged & at line @ 1   Engag	vhe	CSC	drvc	incompatible_drvc_for_net_cscvh	е					
Vine         Cost         droz         droz multiple_drive_net_partially_overlap_cso/h         a         Skipriol 6 at Inc 8 (Mildiple drive Net Mildiple	vhe	CSC	drvc	incompatible_drvc_for_port_cscvh	е					
vihe         csc         drov         Chem, multiple_drive_port_partially_overlag, cscivh         e         Multiple_drive_port_partially_overlag, cscivh           vhe         csc         drov         drov_multiple_drive_sile_partially_overlag, cscivh         e         purtially voorlage at line 6           vhe         csc         drov_multiple_drive_sile_partially_overlag_cscivh         e         Multiple_drive_sile_partially_overlag_cscivh           vhe         csc         dsgn_lop_mod_cannot_ld_cscvh         e         Top minty 6 cannot be learned be le	vhe	CSC	drvc	incompatible_drvc_for_sig_cscvh	е					
whe         csc         droc         drive_multiple_drive_part_partially_coverlap_csoch         e         Multiple_drive_part         Amount partially overlap at lain of sour partially coverlap at lain of sour partially overlap at lain	vhe	csc	drvc	drvc_multiple_drive_net_partially_overlap_cscvh	е					Multiple drive Net
Vine         SSS         drivor         divorce, multiple, divive, sill, partially, overlap, p.cschh         e         Multiple divive pat line (8) artially overlap at line (8) artially overlap at line (8) artially overlap at line (8) for promoted (8) cannot be dentified of tine (8) artially overlap at line (8) for portified (2) artially overlap at line (8) for portified (2) artially overlap at line (8) for portified (2) artially be obtained (8) artially overlap at line (8) for portified (2) artially overlap at line	vhe	CSC	drvc	drvc_multiple_drive_port_partially_overlap_cscvh	е					Multiple drive Port
vhe         csc         dsgn         dsgn_top_mot_dc_ennot_id_cscwh         e         Top motide 8 cannot be identified at 10 cannot be identi	vhe	CSC	drvc	drvc_multiple_drive_sig_partially_overlap_cscvh	е					Multiple drive Signal
whe         css         dsgn         dsgn_top_unit_cannot_id_csowh         e         Top entity @ cannot be definited at line @ to definite a contain a cycle.         Top unit @ cannot be definited at line @ to definite a contain a cycle.         Unit design hierarchy contains a cycle.         Hierarchy is not a spanning tree. at line @ to definite a cycle.         Hierarchy is not a spanning tree. at line @ to definite a cycle.         Hierarchy is not a spanning tree. at line @ to definite a cycle.         Hierarchy is not a spanning tree. at line @ to definite a cycle.         Hierarchy is not a spanning tree. at line @ to definite a cycle.         Hierarchy is not a spanning tree. at line @ to definite a cycle.         Hierarchy is not a spanning tree. at line @ to definite a cycle.         Hierarchy is not a spanning tree. at line @ to definite a cycle.         Hierarchy is not a spanning tree. at line @ to definite a cycle.         Hierarchy is not a spanning tree. at line @ to definite a cycle.         Hierarchy is not a spanning tree. at line @ to definite a cycle.         Hierarchy is not a spanning tree. at line @ to cycle.         Hierarchy is not a spanning tree. at line @ to cycle.         Hierarchy is not a spanning tree. at line @ to cycle.         Hierarchy is not a spanning tree. at line @ to cycle.         Hier	vhe	CSC	dsgn	dsgn_top_mod_cannot_id_cscvh	е					Top module @ cannot be
vhe         csc         dsgn         dsgn_up_unit_cannot_id_cscvh         6         Top unit @ cannot be identified at line @ iden	vhe	CSC	dsgn	dsgn_top_entity_cannot_id_cscvh	е					Top entity @ cannot be
whe         csc         dsgn         unit_dsgn_cycle_not_spanning_tree_cscvh         e         Unit design hierarchy contains a cycle. Hierarchy is not a spanning tree.         Available at line.         With cost of the contains the con	vhe	CSC	dsgn	dsgn_top_unit_cannot_id_cscvh	е					Top unit @ cannot be
vhe         csc         expr         expr_pris_indices_1bit_var_cscvh         e         Part select indices a planning rise at a la apanning rise of a la panning rise of a	vhe	CSC	dsgn	unit_dsgn_cycle_not_spanning_tree_cscvh	е					
whe         csc         expr         expr_prts_must_be_cst_expr_cscvh         e         Part select indices the life in variable at line in the in variable at line in the interest of the part select specification. He is a constant such as the constant such										
whe         sc         expr         expr_prts_must_be_cst_expr_csovh         e         Part select specifier Expression must fine @ Expression @ at line @ Axio & at line @	vhe	CSC	expr	expr prts indices 1bit var cscvh	е					
type csc expr unsupp_cerator_cscvh w lil_bit_select_expr_cscvh w constant Expression at line @ line	vhe	CSC			е					
whe         csc         expr         not_const_expr_cscvh         e         Repetition multiplier in concatenation is not a constant Expression at line @ included in the included included included in the included		000	oxp.	олррнеаооо_ооолрооо						Expression must be
vhe         csc         expr         lil_bit_select_expr_cscvh         e         constant Expression at line @ line	vho	200	over	not const over each						line @
whe         csc         expr         ill_bit_select_expr_cscvh         e         lilegal bit select expression & at line @ lilegal bit select expression & at line @ lilegal bit select expression at line @ lilegal bit select on concatenation is not a constant Expression at line @ lilegal bit select expression at lilegal bit select expression exp	vne	CSC	expi	not_const_expt_cscvn	е					concatenation is not a
whe csc expr repetition_multiplier_in_conc_not_const_expr_cscvh w Repetition multiplier in concatenation is not a constant Expression at line @ Logic operator has integer operands instead of the properands at line @ Logic operator has integer operands instead of the properands at line @ Logic operator has integer operands at line @ Unsupported Expression at line @ Unsupported Operator has not been at line @ Expression @ In ontity port dir at line @ Expression @ In ontity port dir at line @ Expression @ In ontity port dir at line @ Expression @ In ontity port dir at line @ Expression @ In ontity port dir at line @ Expression @ In ontity port dir at line @ Expression @ In ontity port dir at line @ Expression @ In ontity port dir at line @ Expression @ In ontity port dir at line @ In ontity port dir at line @ Expression @ In ontity port dir at line @ Expression @ In ontity port dir at line @ In o										line @
vhe         csc         expr         int_operand_not_1_bit_cscvh         w         Logic operator has integer operands instead of 1-bit operands at line @ 0           vhe         csc         expr         unsupp_expr_cscvh         w         Unsupported Expression of 1-bit operands at line @ 0           vhe         csc         expr         unsupp_expr_cscvh         w         Unsupported Expression flype @ at line @ 10           vhe         csc         expr         unsupp_operator_cscvh         w         Unsupported Expression flype @ at line @ 10           vhe         csc         expr         unsupp_operator_cscvh         w         Use of single bit constant at line @ 10           vhe         csc         expr         unary_op_in_comparison_cscvh         e         Unary op used in comparison at line @ 10           vhe         csc         expr         x_or_zin_cond_expr_cscvh         e         comparison at line @ 2           vhe         csc         expr         zero_in_rep_in_conc_cscvh         e         concatenation at line @ 2           vhe         csc         expr         zero_in_rep_in_conc_cscvh         e         e         concatenation at line @ 2           vhe         csc         expr         zero_in_expr_cscvh         e         e         expression @ in module port dir cscvh         e<		CSC	expr		е					expression @ at line @
Inine @   Logic operator has integer operands instead of 1-bit operands at line @   Unsupported Expression (ype @ at line @   Expression @   Ininity   yort dir at line @     Expression @   Ininity   yort dir at line @     Yort   yort	vhe	CSC	expr	repetition_multiplier_in_conc_not_const_expr_cscvh	W					
Integer operands instead of 1-bit operands at line @   Integer operands										
vhe         csc         expr         unsupp_expr_cscvh         w         Unsupported Expression 1ype @ at line @ vhe           vhe         csc         expr         unsupp_operator_cscvh         w         Unsupported operator 1ype @ at line @ vhe           vhe         csc         expr         use_of_sg_bit_const_cscvh         w         Use of single bit constan at line @ vhe           vhe         csc         expr         unary_op_in_comparison_cscvh         e         Use of single bit constan at line @ vhe           vhe         csc         expr         unary_op_in_comparison_cscvh         e         Unary op used in comparison at line @ xpression @ in module xpression @ in unit port dir at line @ xpression @ in unit port xpression @ in unit port xpression @ in unit port xpression @ xpression @ in intitie xpression @ xpression & xpres	vhe	CSC	expr	int_operand_not_1_bit_cscvh	W					
type @ at line @ Unsuppoperator_cscvh w Unsuppoperator_type @ at line @ Unsupported operator type @ at line @ Unary op used in comparison at line @ Unary op used in comparison at line @ X or z in conditional expression at line @ X or z in conditional expression at line @ X or z in conditional expression at line @ X or z in conditional expression at line @ X or z in conditional expression at line @ X or z in conditional expression at line @ X or z in conditional expression at line @ X or z in conditional expression at line @ X or z in conditional expression at line @ X or z in conditional expression at line @ X or z in conditional expression at line @ X or z in conditional expression at line @ X or z in conditional expression at line @ X or z in conditional expression at line @ X or z in conditional expression at line @ X or z in conditional expression at line @ X or z in conditional expression at line @ X or z in conditional expression @ in morbid in at line @ X or z in conditional expression @ in unit port dir at line @ X or z in conditional expression @ in unit port dir at line @ X or z in conditional expression @ in unit port dir at line @ X or z in conditional expression & X or z in conditional expression										of 1-bit operands at line
Whe         CSC         expr         unsupp_operator_cscvh         W         Unsupported operator type @ at line @ tine @ t	vhe	CSC	expr	unsupp_expr_cscvh	W					
Whe         csc         expr         use_ol_sg_bit_const_cscvh         w         Use of single bit constant at line @ tain the at line	vhe	CSC	expr	unsupp_operator_cscvh	w					Unsupported operator
vhe         csc         expr         unary_op_in_comparison_cscvh         e         Unary op used in comparison at line @ x or z in conditional expression at line @ x or z in condition at line @	vhe	CSC	expr	use_of_sg_bit_const_cscvh	W					Use of single bit constant
Vhe         csc         expr         x_or_z_in_cond_expr_cscvh         e         x or z in conditional expression at line @ expression at line @ cxpression at line @ cxpression at line @ cxpression dillocate and the cxpression operator dillocate and the cxpression dillocate and tx or z in tx or z	vhe	CSC	expr	unary_op_in_comparison_cscvh	е					Unary op used in
Vhe         csc         expr         zero_in_rep_in_conc_cscvh         e         Zero repeator in concatenation at line @ expression @ in module port dir at line @ expression @ in module port dir at line @ expr_in_ent_port_dir_cscvh         e         Expression @ in entity port dir at line @ expr_sion @ in entity port dir at line @ expr_sion @ in unit port dir at line @ expr_sion @ in unit port dir at line @ expr_sion @ in unit port dir at line @ at line @ at line @ at line @ expr_sion @ in unit port dir at line @ expr_sion @ in inst ident in expression in expression in expression @ in inst ident in exp	vhe	CSC	expr	x_or_z_in_cond_expr_cscvh	е					x or z in conditional
vhe         csc         expr         expr_in_mod_port_dir_cscvh         e         Expression @ in module port dir at line @ port dir at line @ Expression @ in entity port dir at line @ Expression @ in entity port dir at line @ Expression @ in unit port dir at line @ Expression @ in unit port dir at line @ Expression @ in unit port dir at line @ Expression @ in unit port dir at line @ Expression @ in unit port dir at line @ Expression @ in unit port dir at line @ Expression @ in unit port dir at line @ Expression @ in unit port dir at line @ Expression @ in unit port dir at line @ Expression @ in unit port dir at line @ Expression @ in unit port dir at line @ Expression @ in unit port dir at line @ Expression @ in expression in exp	vhe	CSC	expr	zero_in_rep_in_conc_cscvh	е					Zero repeator in
Vhe         csc         expr         expr_in_ent_port_dir_cscvh         e         Expression @ in entity port dir at line @ Expression @ in unit port dir at line @ dir at line @ expr_operator_operands_unequal_lenght_cscvh         e         Expression @ in entity port dir at line @ at line @ at line @ at line @ cannot_operator @ operands @ unequal_length at line @ cannot_open_filter_specification_file_cscvh         e         Expression operator @ operands @ unequal_length at line @ cannot_open_filter_specification_file_cscvh         e         Cannot_open filter specification file_cscvh         e         Cannot_open filter specification file @ at line @ cannot_open filter_specification_file_cscvh         e         Filter specification file @ at line @ cannot_open filter_specification_file_cscvh         e         Filter specification file @ at line @ cannot_open filter_specification_file_cscvh         e         Filter specification file @ at line @ cannot_open filter_specification_file_cscvh         e         Filter specification_file_ant line @ cannot_open filter_specification_file_cscvh         e         Filter specification_file_cscvh         e         Filter specification_file_ant line @ cannot_open filter_specification_file_cscvh         e         Mismatch between end and file ant line @ at line @	vhe	CSC	expr	expr_in_mod_port_dir_cscvh	е					Expression @ in module
vhe         csc         expr         expr_in_sig_port_dir_cscvh         e         Expression @ in unit por dir at line @ Expression @ in inst iow at line @ at line @ start line @ at line @ start li	vhe	CSC	expr	expr_in_ent_port_dir_cscvh	е					Expression @ in entity
vhe         csc         expr         expr_in_inst_cscvh         e         Expression @ in inst i@ at line @ at line @ operands @ unequal length cscvh         e         Expression operator @ operands @ unequal length at line @ operands @ unequal length at line @ operands @ unequal length at line @ Cannot open filter specification file @ at line @ at line @ operands @ unequal length at line @ Cannot open filter specification file @ at line @ operands @ unequal length at line @ operands in line @ operands in line @ operands line @ operands length at line @ operands length at line operands length at line operands lengthat line operands length at line operands length at line operands	vhe	CSC	expr	expr_in_sig_port_dir_cscvh	е					Expression @ in unit port
vhe         csc         expr         expr_operator_operands_unequal_lenght_cscvh         e         Expression operator @ operands @ unequal length at line @           vhe         csc         file         cannot_open_filter_specification_file_cscvh         e         Cannot open filter specification file @ at line @           vhe         csc         file         filter_specification_file_missing_cscvh         e         Filter specification file name @ is missing at line @           vhe         csc         file         mismatch_mod_file_name_cscvh         e         Mismatch between module name @ and file name @ and file name @ and file name @ and file name @ at line @           vhe         csc         file         mismatch_ent_file_name_cscvh         e         Mismatch between entity name @ and file name @ at line @           vhe         csc         file         mismatch_sig_file_name_cscvh         e         Mismatch between signa name @ and file name @ at line @           vhe         csc         func         port_not_output_func_cscvh         e         Port @ direction cannot be output at line @           vhe         csc         func         too_many_arg_to_func_cscvh         e         Too many arguments passed to function @ at line @           vhe         csc         func         too_few_arg_to_func_cscvh         e         Too few arguments passed to function @ at line @ </td <td>vhe</td> <td>CSC</td> <td>expr</td> <td>expr_in_inst_cscvh</td> <td>е</td> <td></td> <td></td> <td></td> <td></td> <td></td>	vhe	CSC	expr	expr_in_inst_cscvh	е					
vhe         csc         file         cannot_open_filter_specification_file_cscvh         e         Cannot open filter specification file @ at line @ cannot open filter specification file @ at line @ to specification file @ at line @ smissing at line @ to smismatch_mod_file_name_cscvh         e         Filter specification file mame @ is missing at line @ to smissing at line @ to smismatch between module name @ and file name @ at line @ to smismatch_sig_file_name_cscvh         e         Mismatch between signa name @ and file name @ at line @ to smismatch_sig_file_name_cscvh         e         Port @ direction cannot be output at line @ to many arguments passed to function @ at line @ to func	vhe	CSC	expr	expr_operator_operands_unequal_lenght_cscvh	е					
vhe         csc         file         cannot_open_filter_specification_file_cscvh         e         Cannot open filter specification file @ at line @ @           vhe         csc         file         filter_specification_file_missing_cscvh         e         Filter specification file name @ is missing at line @           vhe         csc         file         mismatch_mod_file_name_cscvh         e         Mismatch between module name @ and file name @ at line @           vhe         csc         file         mismatch_ent_file_name_cscvh         e         Mismatch between entry name @ and file name @ at line @           vhe         csc         file         mismatch_sig_file_name_cscvh         e         Mismatch between signa name @ and file name @ at line @           vhe         csc         func         port_not_output_func_cscvh         e         Port @ direction cannot be output at line @           vhe         csc         func         too_many_arg_to_func_cscvh         e         Too many arguments passed to function @ at line @           vhe         csc         func         too_few_arg_to_func_cscvh         e         Too few arguments passed to function @ at line @           vhe         csc         func         funct_expr_cannot_expnaded_cscvh         e         Function expression @										
vhe         csc         file         filter_specification_file_missing_cscvh         e         Filter specification file name @ is missing at line @           vhe         csc         file         mismatch_mod_file_name_cscvh         e         Mismatch between module name @ and file name @ at line @           vhe         csc         file         mismatch_sig_file_name_cscvh         e         Mismatch between entity name @ and file name @ and	vhe	CSC	file	cannot_open_filter_specification_file_cscvh	е					Cannot open filter
vhe       csc       file       mismatch_mod_file_name_cscvh       e       Mismatch between module name @ and file name @ at line @         vhe       csc       file       mismatch_sig_file_name_cscvh       e       Mismatch between entity name @ and file name @ at line @         vhe       csc       file       port_not_output_func_cscvh       e       Port @ direction cannot be output at line @         vhe       csc       func       too_many_arg_to_func_cscvh       e       Too many arguments passed to function @ at line @         vhe       csc       func       too_few_arg_to_func_cscvh       e       Too few arguments passed to function @ at line @         vhe       csc       func       function expression @       Function expression @	vhe	CSC	file	filter specification file missing cscvh	е					@
vhe         csc         file         mismatch_mod_file_name_cscvh         e         Mismatch between module name @ and file name @ at line @           vhe         csc         file         mismatch_ent_file_name_cscvh         e         Mismatch between entity name @ and file name @ at line @           vhe         csc         file         mismatch_sig_file_name_cscvh         e         Mismatch between signa name @ and file name @ at line @           vhe         csc         func         port_not_output_func_cscvh         e         Port @ direction cannot be output at line @           vhe         csc         func         too_many_arg_to_func_cscvh         e         Too many arguments passed to function @ at line @           vhe         csc         func         too_few_arg_to_func_cscvh         e         Too few arguments passed to function @ at line @           vhe         csc         func         function expression @         Function expression @		000	0							name @ is missing at
rame @ at line @  vhe csc file mismatch_ent_file_name_cscvh e  vhe csc file mismatch_sig_file_name_cscvh  vhe csc file mismatch_sig_file_name_cscvh  vhe csc func port_not_output_func_cscvh  vhe csc func too_many_arg_to_func_cscvh  vhe csc func too_many_arg_to_func_cscvh  vhe csc func too_many_arg_to_func_cscvh  vhe csc func too_few_arg_to_func_cscvh  vhe csc func function @ at line @  vhe csc func funct_expr_cannot_expnaded_cscvh	vhe	CSC	file	mismatch_mod_file_name_cscvh	е					Mismatch between
vhe     csc     file     mismatch_sig_file_name_cscvh     e     Mismatch between signa name @ and file name @ at line @       vhe     csc     func     port_not_output_func_cscvh     e     Port @ direction cannot be output at line @       vhe     csc     func     too_many_arg_to_func_cscvh     e     Too many arguments passed to function @ at line @       vhe     csc     func     too_few_arg_to_func_cscvh     e     Too few arguments passed to function @ at line @       vhe     csc     func     function expression @			£:1 -	rian tale and Clauran and						name @ at line @
vhe     csc     file     mismatch_sig_file_name_cscvh     e     Mismatch between signa name @ and file name @ at line @       vhe     csc     func     port_not_output_func_cscvh     e     Port @ direction cannot be output at line @       vhe     csc     func     too_many_arg_to_func_cscvh     e     Too many arguments passed to function @ at line @       vhe     csc     func     too_few_arg_to_func_cscvh     e     Too few arguments passed to function @ at line @       vhe     csc     func     function expression @	vne	CSC	ille	mismatch_ent_nie_name_cscvn	е					name @ and file name
vhe     csc     func     port_not_output_func_cscvh     e     Port @ direction cannot be output at line @       vhe     csc     func     too_many_arg_to_func_cscvh     e     Too many arguments passed to function @ at line @       vhe     csc     func     too_few_arg_to_func_cscvh     e     Too few arguments passed to function @ at line @       vhe     csc     func     function expression @ at line @	vhe	CSC	file	mismatch_sig_file_name_cscvh	е					Mismatch between signal
be output at line @  vhe csc func too_many_arg_to_func_cscvh e  vhe csc func too_few_arg_to_func_cscvh  vhe csc func too_few_arg_to_func_cscvh  vhe csc func funct_expr_cannot_expnaded_cscvh  vhe csc func funct_expr_cannot_expnaded_cscvh  be output at line @  Too many arguments passed to function @ at line @  vhe csc func funct_expr_cannot_expnaded_cscvh  e Function expression @			,							@ at line @
vhe csc func too_few_arg_to_func_cscvh e passed to function @ at line @  Too few arguments passed to function @ at line @  vhe csc func funct_expr_cannot_expnaded_cscvh e Function expression @				. – – . – –	е				L	be output at line @
vhe     csc     func     too_few_arg_to_func_cscvh     e     Too few arguments passed to function @ at line @       vhe     csc     func     funct_expr_cannot_expnaded_cscvh     e     Function expression @	vhe	csc	func	too_many_arg_to_func_cscvh	е					
passed to function @ at line @  vhe csc func funct_expr_cannot_expnaded_cscvh e Function expression @	vhe	CSC	func	too_few_arg_to_func cscvh	е					line @
vhe         csc         func         funct_expr_cannot_expnaded_cscvh         e         Function expression @				_ <b>_ _</b> _ <b>_</b>						passed to function @ at
	vhe	CSC	func	funct_expr_cannot_expnaded_cscvh	е					Function expression @ cannot be expanded at

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	CSC	func	funct_not_used_in_expr_cscvh	w					line @ Function @ is not being used in an Expression at line @
vhe	CSC	func	func_decl_cscvh	W					Function Declaration @ already declared as
vhe	CSC	func	undefined_func_cscvh	е					another type at line @ Undefined function @ at line @
vhe	CSC	hid	cannot_locate_hier_id_hid_cscvh	е					Can't locate hierarchical identifier @ at line @
vhe	csc	hid	ref_minst_found_in_expr_hid_cscvh	е					References a module instance @ found in an
vhe	CSC	hid	ref_entity_found_in_expr_hid_cscvh	е					References a entity instance @ found in an
vhe	CSC	hid	ref_unit_found_in_expr_hid_cscvh	е					Expression hid at line @ References a unit instance @ found in an
vhe	CSC	hid	hid_reference_not_found_cscvh	е					© reference not found a line © line ©
vhe	CSC	hid	mifc_in_hid_not_exist_cscvh	е					Module instance @ in hid
vhe	CSC	hid	entity_instance_in_hid_not_exist_cscvh	е					does not exist at line @ Entity instance @ in hid does not exist at line @
vhe	CSC	hid	unit_instance_in_hid_not_exist_cscvh	е					Unit instance @ in hid does not exist at line @
vhe	CSC	hid	mod_found_in_path_in_dsgn_cscvh	е					Module @ found in path @ in the design at line @
vhe	CSC	hid	enity_found_in_path_in_dsgn_cscvh	е					Entity @ found in path @ in the design at line @
vhe	csc	hid	unit_found_in_path_in_dsgn_cscvh	е					Unit @ found in path @ in the design at line @
vhe	csc	hid	hierarchical_id_path_contains_func_csc	е					Hierarchical ID @ path contains a function at line
vhe	CSC	init	assn_mem_in_init_blk_cscvh	е					Assign memory in initial block at line @
vhe	CSC	inst	inst_duplicate_mod_name_cscvh	е					Duplicate port @ in the port list for module @ at
vhe	CSC	inst	inst_duplicate_entity_name_cscvh	е					line @  Duplicate port @ in the port list for entity @ at line @
vhe	CSC	inst	inst_duplicate_unit_name_cscvh	е					Duplicate port @ in the port list for unit @ at line @
vhe	CSC	inst	ill_mod_inst_name_cscvh	е					Illegal module instance @ at line @
vhe	CSC	inst	ill_entity_inst_name_cscvh	е					Illegal entity instance @ at line @
vhe	csc	inst	ill_unit_inst_name_cscvh	е					Illegal unit instance @ at line @
vhe	csc	inst	inst_name_defined_mod_cscvh	е					Instance name @ already defined in this module at line @
vhe	CSC	inst	inst_name_defined_ent_cscvh	е					Instance name @ already defined in this
vhe	CSC	inst	inst_name_defined_unit_cscvh	е					entity at line @ Instance name @ already defined in this
vhe	CSC	inst	inst_too_many_bits_cscvh	е					unit at line @ Too many bits for port @ of instance array @, formal @, actual @ at
vhe	CSC	inst	inst_port_not_connected_var_cscvh	е					line @ Port 'port' of instance array 'array' is not connected to variable at
vhe	CSC	inst	inst_insufficient_bits_cscvh	е					line @ Insufficient bits for port 'port' of instance array 'array ', formal number, actual number at line @
vhe	CSC	inst	inst_mod_name_not_defined_cscvh	е					Module name not defined at line @
vhe	CSC	inst	inst_ent_name_not_defined_cscvh	е					Entity name not defined
vhe	CSC	inst	inst_unit_name_not_defined_cscvh	е					at line @ Unit name not defined at line @
vhe	CSC	inst	many_mod_inst_param_assign_cscvh	е					Too many module instance parameter
vhe	CSC	inst	many_entity_inst_param_assign_cscvh	е					assignments (number > rrumber) at line @ Too many entity instance parameter assignments (number > rrumber) at
vhe	CSC	inst	many_unit_inst_param_assign_cscvh	е					line @ Too many unit instance

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
									parameter assignments (number > rrumber) at line @
vhe	csc	inst	complexexpr_cannot_mapped_inout_port_cscvh	е					Complex Expression @ cannot be mapped to inout port @ at line @
vhe	CSC	inst	complexexpr_cannot_mapped_unknown_port_cscvh	е					Complex Expression @ cannot be mapped to unknown type port @ at
vhe	CSC	inst	netdecl_contains_ill_prts_cscvh	е					line @ Net Declaration [@: @] contains an illegal part
vhe	CSC	inst	regdecl_contains_ill_prts_cscvh	е					select at line @ Reg Declaration [@ : @] contains an illegal part select at line @
vhe	CSC	inst	complex_expr_inst_parent_module_cscvh	е				,	Complex actual Expression associated with port @ of module @ instantiated in parent
vhe	CSC	inst	complex_expr_inst_entity_parent_module_cscvh	е					module at line @ Complex actual Expression associated with port @ of entity @ instantiated in parent module at line @
vhe	csc	inst	complex_expr_inst_unit_parent_module_cscvh	е					Complex actual Expression associated with port @ of unit @ instantiated in parent module at line @
vhe	CSC	inst	inst_mod_output_port_width_cscvh	е				á	Mod @ Output port @ width mismatch, actual-width ( port-width ) at line @
vhe	CSC	inst	inst_entity_output_port_width_cscvh	е					Entity @ Output port @ width mismatch, actual-width ( port-width ) at line @
vhe	csc	inst	inst_unit_output_port_width_cscvh	е					Unit @ Output port @ width mismatch, actual-width ( port-width ) at line @
vhe	CSC	inst	inst_mod_input_port_width_cscvh	е				á	Mod @ Input port @ width mismatch, actual-width ( port-width ) at line @
vhe	CSC	inst	inst_entity_input_port_width_cscvh	е				á	Entity @ Input port @ width mismatch, actual-width ( port-width ) at line @
vhe	CSC	inst	inst_unit_input_port_width_cscvh	е				á	Unit @ Input port @ width mismatch, actual-width ( port-width ) at line @
vhe	CSC	inst	inst_mod_not_define_cscvh	е					Module not defined at line @
vhe	CSC	inst	inst_entity_not_define_cscvh	е					Entity not defined at line @
vhe	CSC	inst inst	inst_unit_not_define_cscvh ent_port_actual_formal_width_mismatch_cscvh	e W					Unit not defined at line @ Entity @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vhe	CSC	inst	unit_port_actual_formal_width_mismatch_cscvh	W					Unit @ instance @ port @ width mismatch, actual width @ formal width @ at line @
vhe	CSC	inst	inst_differs_in_case_from_mod_cscvh	е					Instance name @ differs in case from module name @ at line @
vhe	CSC	inst	inst_differs_in_case_from_ent_cscvh	е					Instance name @ differs in case from entity name @ at line @
vhe	csc	inst	inst_differs_in_case_from_sig_cscvh	е					Instance name @ differs in case from signal name @ at line @
vhe	CSC	loop	undet_init_value_loop_cscvh	е					Unable to determine init value for loop at line @
vhe	csc	loop	undet_limit_loop_cscvh	е					Unable to determine limit for loop at line @
vhe	CSC	loop	loop_bounds_calculated_int_cscvh	W					Loop bounds are calculated to be integer @, check that this is correct at line @
vhe	csc	loop	expr_lhs_contains_var_bit_select_cscvh	W					expression in lhs of assignment contains a variable bit select at line
vhe	csc	loop	loop_bounds_not_const_csc	W					Loop bounds are non-constant at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	CSC	loop	loop_ctrl_init_expr_not_const_cscvh	w					Non-constant loop bound. Loop control
									variable initialization
									Expression is not a constant Expression at
									line @
vhe	CSC	loop	loop_term_expr_not_const_cscve	W					Non-constant loop bound. loop terminating
									Expression could not be
									evaluated to a constant at line @
vhe	csc	loop	init_expr_reset_by_var_cscvh	е					Non-constant loop
									bound. initializing
									Expression reset by variable at line @
vhe	csc	loop	loop_ctrl_var_1_bit_wide_cscvh	w					The loop control variable
									@ is one bit wide. Check the loop control variable
									Declaration. at line @
vhe	CSC	mdb	bad_mdb_net_cscvh	е					Bad multi-driven Net @ at line @
vhe	CSC	mdb	bad_mdb_port_cscvh	е					Bad multi-driven Port @
vhe	CSC	mdb	bad mdb signal cscvh	е					at line @ Bad multi-driven Signal
VIIC	030	mub	bad_mdb_signal_cscvii	6					@ at line @
vhe	CSC	mdb	unsupp_comp_mdb_net_cscvh	е	?				Unsupported component type @ driving in
									multi-driven Net name at
									line @
vhe	CSC	mdb	unsupp_comp_mdb_port_cscvh	е	?				Unsupported component type @ driving in
									multi-driven Port name at
vhe	CSC	mdb	unsupp comp mdb signal cscvh	е	?				line @ Unsupported component
	000		aapp_compas_s.gacoo						type @ driving in
									multi-driven Signal name at line @
vhe	CSC	mdb	unsupp_comp_drive_mdb_cscvh	е	?				Unsupported component
									type @ driving multi-driven Net natne at
									line @
vhe	CSC	mdb	unsupp_comp_drive_mdb_port_cscvh	е	?				Unsupported component type @ driving
									multi-driven Port natne at
مطيد		ماله معا	unauna agen driva media aignal aggub		?				line @
vhe	CSC	mdb	unsupp_comp_drive_mdb_signal_cscvh	е	?				Unsupported component type @ driving
									multi-driven Signal natne
vhe	CSC	mdb	mdb net driven by trns cscvh	е					at line @ Multiply driven Net driven
			······						by transistor primitive
vhe	CSC	mdb	mdb_port_driven_by_trns_cscvh	е					type @ at line @ Multiply driven Port
									driven by transistor
									primitive type @ at line @
vhe	CSC	mdb	mdb_sig_driven_by_trns_cscvh	е					Multiply driven Signal
									driven by transistor primitive type @ at line
									@
vhe	CSC	mdb	mdb_unsupp_comp_drvs_net_cscvh	е					Unsupported component type driving Net drives
									Net connected to
vhe	CSC	mdb	mdb_unsupp_comp_drvs_port_cscvh	е					multi-driven Net at line @ Unsupported component
VIIC	030	mub	mab_unsupp_comp_urvs_port_cscvn						type driving Port drives
									Port connected to
									multi-driven Port at line @
vhe	CSC	mdb	mdb_unsupp_comp_drvs_sig_cscvh	е					Unsupported component
									type driving Signal drives Signal connected to
									multi-driven Signal at line
vhe	CSC	mdb	mdb_incompatible_net_drives_multiple_net_cscvh	е				1	@ Incompatible driver
-									driving tandem Net
									drives Net connected to multi-driven Net at line @
vhe	CSC	mdb	mdb_incompatible_port_drives_multiple_port_cscvh	е					Incompatible driver
									driving tandem Port drives Port connected to
									multi-driven Port at line
vhe	CSC	mdb	mdb_incompatible_sig_drives_multiple_sig_cscvh	е				1	@ Incompatible driver
	300								driving tandem Net
									drives Net connected to multi-driven Port at line
		<u>L</u>		L				L	@
vhe	CSC	mdb	mdb_unsupp_LHS_concatenation_cscvh	е					Unsupported LHS concatenation in
					1	1	il .	1	CONCARCHARON IN

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	CSC	mdb	mdb_bus_has_too_many_drivers_cscvh	е					@ Bus has too many drivers. at line @
vhe	CSC	mdb	mdb_always_blk_drive_cscvh	w					Multiple always blocks drive name @ at line @
vhe	CSC	mdb	nontri_gate_drives_mdb_net_cscvh	w					non-tri-state gate drives
vhe	CSC	mdb	nontri_gate_drives_mdb_port_cscvh	w					multi-driven Net at line @ non-tri-state gate drives
									multi-driven Port at line @
vhe	CSC	mdb	nontri_gate_drives_mdb_sig_cscvh	W					non-tri-state gate drives multi-driven Signal at line @
vhe	CSC	mem	mem_prts_csvh	е					Memories do not support part select specifier at
vhe	CSC	mem	mem_ref_without_index_cscvh	е					line @ Memory @ referenced without index through hierarchical ID @ at line @
vhe	CSC	mem	ill_mem_cscvh	е					Illegal memory @ at line
vhe	CSC	mifc	mifc_not_array_csvh	е					@ Ports may not be an
vhe	CSC	mifc	port_identifier_mifc_cscvh	е					array at line @ Port @ at line @
vhe	CSC	mifc	mod_output_wire_redecl_reg_cscvh	е					Module @ output port re-declared as type reg after use as implicitly declared wire at line @
vhe	CSC	mifc	entity_output_wire_redecl_reg_cscvh	е					Entity @ output port re-declared as type reg after use as implicitly declared wire at line @
vhe	CSC	mifc	unit_output_wire_redecl_reg_cscvh	е					Unit @ output port re-declared as type reg after use as implicitly declared wire at line @
vhe	CSC	mifc	output_port_is_mem_type_mifc_cscvh	е					Output port @ is memory type at line @
vhe	CSC	mifc	mifc_inout_port_is_mem_type_cscvh	е					Inout port @ is memory type at line @
vhe	CSC	mifc	mod_output_port_mismatch_actual_witdh_cscvh	W					Module @ output port @ formal to actual width mismatch at line @
vhe	CSC	mifc	ent_output_port_mismatch_actual_witdh_cscvh	W					Entity @ output port @ formal to actual width mismatch at line @
vhe	CSC	mifc	unit_output_port_mismatch_actual_witdh_csc	W					Unit @ output port @ formal to actual width mismatch at line @
vhe	CSC	mifc	port_name_different_in_upper_lower_case_cscvh	е					Port name @ different in upper lower case at line @
vhe	CSC	mifc	port_not_def_in_iodecl_cscvh	е					Port @ not defined in ioDeclaration at line @
vhe	CSC	mifc	port_not_def_in_portl_cscvh	е					Port @ not defined in
vhe	CSC	mifc	port_wiredecl_mismatch_cscvh	е					port list at line @ Port @ wireDeclaration
vhe	CSC	mifc	pos_based_null_inst_port_cscvh	е					mismatch at line @ Position based null
vhe	CSC	mifc	last portdecl contains trailcomma cscvh	е					instance port at line @ Last portDeclaration
vhe	CSC	mins	mins_expr_incompatible_type_cscvh	е					contains a trailing comma at line @ Expression @ has an incompatible argument type @ with the port at
vhe	csc	mins	mins_mod_not_exist_cscvh	е					line @  Module @ does not exist
									at line @
vhe	CSC	mins	mins_entity_not_exist_cscvh	е					Entity @ does not exist at line @
vhe	CSC	mins	mins_unit_not_exist_cscvh	е					Unit @ does not exist at line @
vhe	CSC	mod	dup_declar_name_mod_csvh	е					Duplicate Declaration of port @ at line @
vhe	CSC	mod	ill_mod_name_cscvh	е					Illegal module @ at line
vhe vhe	CSC	mod mod	ill_mod_entity_name_cscvh ill mod unit name cscvh	е					Illegal entity @ at line @ Illegal unit @ at line @
vhe	CSC	mod	mod_mult_decl_string_cscvh	e					Multiple Declarations of string detected in module @ at line @
vhe	CSC	mod	mod_entity_mult_decl_string_cscvh	е					Multiple Declarations of string detected in entity  @ at line @
vhe	CSC	mod	mod_unit_mult_decl_string_cscvh	е					Multiple Declarations of string detected in unit @ at line @
vhe	CSC	mod	mod_mult_def_cscvh	е					Module @ defined in

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	CSC	mod	mod_ent_mult_def_cscvh	е			-		multiple places at line @ Entity @ defined in
viie	CSC	mou	mod_ent_muit_dei_cscvii	е					multiple places at line @
vhe	CSC	mod	mod_unit_mult_def_cscvh	е					Unit @ defined in multiple places at line @
vhe	csc	mod	mod_no_module_found_cscvh	е					No modules found at line @
vhe	CSC	mod	mod_no_entity_found_cscvh	е					No entity found at line @
vhe vhe	CSC	mod mod	mod_no_unit_found_cscvh failed_find_mod_cscvh	e					No unit found at line @ Failed to find module @
									at line @
vhe	CSC	mod	failed_find_entity_cscvh	е					Failed to find entity @ at line @
vhe	CSC	mod	failed_find_unit_cscvh	е					Failed to find unit @ at line @
vhe vhe	CSC	mod mod	empty_mod_cscvh empty_ent_cscvh	e					Empty module at line @ Empty entity at line @
vhe	CSC	mod	empty_unit_cscvh	e					Empty unit at line @
vhe	CSC	net	net_implicit_wire_redecl_reg_cscvh	е					Implicitly declared as a
vhe	CSC	net	undecl_net_in_mod_cscvh	е					wire @ re-declared as a reg @. at line @ Undeclared net @ in
vhe	csc	net	undecl_net_in_mod_cscvh	e					module @ at line @ Undeclared port @ in
vhe	csc	net	undecl_sig_in_mod_cscvh	е					module @ at line @ Undeclared signal @ in
vhe	CSC	net	undecl net in ent cscvh	е					module @ at line @ Undeclared net @ in
									entity @ at line @
vhe	CSC	net	undecl_port_in_ent_cscvh	е					Undeclared port @ in entity @ at line @
vhe	CSC	net	undecl_sig_in_ent_cscvh	е					Undeclared signal @ in entity @ at line @
vhe	CSC	net	undecl_net_in_sig_cscvh	е					Undeclared net @ in
vhe	CSC	net	undecl_port_in_sig_cscvh	е					signal @ at line @ Undeclared port @ in
vhe	CSC	net	undecl_sig_in_sig_cscvh	е					signal @ at line @ Undeclared signal @ in
vhe	CSC	net	port_used_prior_to_decl_cscvh	е					signal @ at line @ Port @ used prior
vhe	CSC	net	1bit_with_prts_cscvh	е					toDeclaration at line @ 1-bit with part select at
vhe	CSC	netd	ill_decl_vec_cscvh	е					line @
vhe	CSC	nett	nett_ill_reg_name_cscvh	е					vector @ at line @ Illegal register @ at line
vhe	CSC	nett	nett_ill_net_name_cscvh	е					@ Illegal net @ at line @
vhe	CSC	nett	nett_ill_port_name_cscvh	е					Illegal port @ at line @
vhe vhe	CSC	nett nett	nett_ill_signal_name_cscvh net_scalar_vect_nett_cscvh	e					Illegal signal @ at line @ Net declared as both
VIIC	030	neu	rie_scalar_vect_riet_cscvii						scalar and vector at line
vhe	CSC	nett	port_scalar_vect_nett_cscvh	е					Port declared as both scalar and vector at line
vhe	CSC	nett	signal_scalar_vect_nett_cscvh	е					@ Signal declared as both
									scalar and vector at line @
vhe	CSC	nett	hot_mux_not_use_bus_connection_net_cscvh	е					One hot mux can not be used for bus connection
									between modules Net @
vhe	CSC	nett	hot_mux_not_use_bus_connection_port_cscvh	е					at line @ One hot mux can not be
VIIC	030	nou	not_max_not_use_bus_connection_port_escent						used for bus connection between modules Port @
		44	h-t						at line @
vhe	CSC	nett	hot_mux_not_use_bus_connection_sig_cscvh	е					One hot mux can not be used for bus connection
									between modules Signal
vhe	CSC	num	not_allowed_width0_num_cscvh	е					@ at line @ Width 0 not allowed for
									sized number at line @
vhe	CSC	num	real_num_not_allowed_cscvh	е					Real numbers not allowed at line @
vhe	CSC	num	found_x_z_in_num_literal_cscvh	е					Found x and/or z value in number literal at line @
vhe	csc	num	too_many_digits_in_sized_num_cscvh	W					Number of digits exceeds the width in a sized
vhe	CSC	num	divide_by_zero_num_cscvh	е					number at line @ Divide by zero at line @
vhe	CSC	num	unknown_num_base_cscvh	e					Unkown number base @ at line @
vhe	CSC	num	child_mod_inst_parent_mod_cscvh	е					Child module @
									instantiates parent module @ at line @
vhe	CSC	num	child_ent_inst_parent_ent_cscvh	е					Child entity @ instantiates entity module
									@ at line @
vhe	CSC	num	child_sig_inst_parent_sig_cscvh	е					Child signal @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl Desc
								instantiates signal module @ at line @
vhe	CSC	num	int_decl_incorrect_cscvh	е				Integer Declaration incorrect at line @
vhe	CSC	num	int_var_indexed_cscvh	е				Integer variable inedexed at line @
vhe	CSC	parm	ill_parm_identifier_cscvh	е				Illegal parameter @ at line @
vhe	CSC	parm	value_of_parm_OS_platform_dependent_cscvh	w				Parameter select width >
								<ol><li>The value is OS and platform dependent at</li></ol>
vhe	CSC	parm	parm_redefined_cscvh	w				line @ Parameter @ redefined
vhe	CSC	port	ill formal port name cscvh	е				at line @ Illegal formal port @ at
vhe	csc	·	text_redefined_replaced_cscvh	w				line @  Text macro redefined
VIIC	030	pp	text_redefined_replaced_cscviii	v				and replaced @. Previous definition filename, line number @ New definition filename, line number @ at line @
vhe	CSC	pp	endif_or_else_without_ifdef_cscvh	е				Endif-or-else-without
vhe	CSC	prim	z_in_prim_inst_cscvh	е				ifdef at line @ z in primitive instantiation
vhe	CSC	prts	type_prts_csvh	е				at line @ Type @ does not support
vhe	csc	prts	prts out of range cscvh	е				part select specifier at line @ Parameter @[@:@]part
	030		0 -					select is out of range at line @
vhe	CSC	prts	ill_prts_inst_array_cscvh	е				Illegal value for part select of instance array 'name' at line @
vhe	CSC	prts	const_prts_contains_non_const_selector_cscvh	е				Constant part select @ contains a non-constant selector @ at line @
vhe	CSC	prts	bus_index_prts_for_var_out_of_range_cscvh	е				Bus index @ integer of part select [@:@] for variable @ out of range at line @
vhe	CSC	prts	bus_prts_for_var_out_of_range_cscvh	е				Bus part select [@:@] for variable @ out of range at line @
vhe	csc	prts	bus_prts_index_out_of_name_for_var_cscvh	е				Bus part select [@:@] index @ out of range for variable @ at line @
vhe	CSC	prts	ill_token_in_prts_cscvh	е				Illegal token in part select @ at line @
vhe	CSC	prts	incomplete_prts_specification_cscvh	е				Incomplete part select specification @ at line @
vhe	CSC	prts	ill_index_in_prts_cscvh	е				Illegal index in part select @ at line @
vhe	csc	prts	negative_index_in_prts_not_allowed_cscvh	е				Negative index in part select @ not allowed at line @
vhe	CSC	prts	prts_index_order_reversed_cscvh	е				Part select index order reversed [@ : @] [@ : @] should be [@ : @] at line
vhe	CSC	prts	index_vec_over_max_size_cscvh	w				Vector index @ exceeds the size of the vector. Index truncated at line @
vhe	CSC	prts	x_or_z_in_vec_bit_select_index_cscvh	е				x or z in vector bit select
vhe	CSC	simr	inefficient_op_not_a_power_of_2_cscvh	е				index at line @ Division/modulus by a number not a power of 2. Inefficient simulation
vhe	CSC	simr	simr_multiple_init_blk_force_cscvh	w				operation. at line @ Multiple initial blocks force @. Unpredictable simulation result at line @
vhe	csc	snsl	incomplete_snsl_cscvh	w				Incomplete sensitivity list.  @ is not in the sensitivity
vhe	csc	snsl	edge_sns_process_contains_data_pin_snsl_cscvh	е				list. at line @ Edge sensitive process contains a data pin @ in the sensitivity list at line
vhe	CSC	snsl	unsupp_expr_in_snsl_cscvh	W				@ Unsupported Expression type @ in sensitivity list ' at line @
vhe	csc	snsl	partial_bus_decl_width_cscvh	е	?			partial bus @ declared with width @ width @ at line @
vhe	CSC	snsl	contains_inst_name_cscvh	е				Contains instance name @ at line @
vhe	CSC	stmt	null_not_allowed_stmt_cscvh	е				Null statement is not allowed here at line @

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_v	er Cs	I Desc
vhe	CSC	stmt	stmt_ill_accept_only_net_reg_mem_cscvh	е					Illegal type @ can only accept net, reg, memory at line @
vhe	CSC	stmt	stmt_ill_accept_only_port_reg_mem_cscvh	е					Illegal type @ can only accept port, reg, memory at line @
vhe	CSC	stmt	stmt_ill_accept_only_signal_reg_mem_cscvh	е					Illegal type @ can only accept signal, reg,
vhe	csc	stmt	arithmetic_op_rhs_one_less_bit_than_lhs_cscvh	е					memory at line @ Arithmetic operator RHS has one less bit than the
vhe	CSC	stmt	ar_op_unequal_lhs_rhs_cscvh	е					LHS at line @ Arithmetic operator unequal width LHS and
vhe	csc	stmt	ar_op_unequal_var_on_rhs_csc	е					RHS at line @ Arithmetic operator unequal width variables
vhe	CSC	stmt	empty_stmt_csc	е					@ on RHS at line @ Empty-statement at line @
vhe	csc	syst	return_var_of_user_used_as_rhs_cscvh	W					Return variable of user system task is used as a RHS variable at line @
vhe	CSC	task	ask_var_not_decl_cscvh	е					Variable @ used but not declared at line @
vhe	csc	task	too_many_arg_to_task_cscve	е					Too many arguments passed to task @ at line @
vhe	csc	task	too_few_arg_to_task_cscvh	е					Too few arguments passed to task @ at line @
vhe	CSC	tri	instance_not_tri_state_device_cscvh	е					Instance name is not a tri-state device at line @
vhe	csc	tri	unsupp_gate_type_tristate_cscvh	е					Unsupported gate type @ used for tristate at line @
vhe	CSC	tri	tri_not_desgn_gate_contention_cscvh	е					Tristate not designed correctly gate @ can cause contention at line
vhe	csc	tri	unsupp_type_instance_tri_cscvh	е					Unsupported type instance type used for tristate @ at line @
vhe	CSC	tri	incorrect_cont_assign_stmt_tri_gate_cscvh	е					Incorrect continuous assign statement for
vhe	CSC	tri	const_assign_to_multidriven_net_cscvh	е					tristate gate @ at line @ Constant (constiznt) assigned to multi-driven Net @ at line @
vhe	CSC	tri	const_assign_to_multidriven_port_cscvh	е					Constant (constiznt) assigned to multi-driven
vhe	csc	tri	const_assign_to_multidriven_signal_cscvh	е					Port @ at line @ Constant (constiznt) assigned to multi-driven Signal @ at line @
vhe	csc	tri	unsupp_expr_for_tri_cscvh	е					Unsupported Expression type @ for tristate at line
vhe	csp	ccd	misplaced_csdir_ignored_csvh	е				X	Lower case directive in wrong location. Ignored at line @
vhe	csp	cmdl	ill_cmdl_uselib_dir_path_csvh	е					Illegal 'uselib directory path @ no such directory at line @
vhe	csp	cmnt	vhe_csp_cmnt_miss_closing_csvh	е					/* comment missing closing */ at line @
vhe	csp	csi	miss_char_case_csvh	е					Missing character @ at line @
vhe	csp	expr	malformed_unary_expr_vcsp	е					Malformed unary
vhe	csp	expr	malformed_binary_expr_vcsp	е					Expression @ at line @ Malformed binary
vhe	csp	expr	malformed_ternary_expr_vcsp	е					Expression @ at line @  Malformed ternary Expression @ at line @
vhe	csp	expr	expr_found_reserved_word_csvh	е					Expected identifier but found reserved word @
vhe	csp	expr	expr_concatenation_empty_csvh	е					at line @ Concatenation empty at
vhe	csp	expr	ill_operator_expr_csvh	е					line @ Illegal operator @ at line
vhe	csp	expr	ill_operand_expr_csvh	е					@ Illegal operand @ at line
vhe	csp	file	cannot_open_file_csvh	е					@ Cannot open file @ at
vhe	csp	file	line_lenght_overflow_csvh	е					line @ Line length overflow
vhe	csp	file	environ_var_in_filel_csvh	е					line_length @ at line @ Environ variable in file list
vhe	csp	func	undefined_func_csvh	е					at line @ Undefined function @ at

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	csp	inst	ill_mod_inst_name_csvh	е					line @
vhe	csp	inst	ill_entity_inst_name_csvh	е					@ at line @ Illegal entity instance @
vhe	csp	inst	ill_unit_inst_name_csvh	е					at line @ Illegal unit instance @ at
vhe	csp	lib	not_open_lib_file_csvh	е					line @ Cannot open library file
vhe	csp	list	trail_comma_list_vhs	е					@ at line @ Trailing comma in
	•								parentheses enclosed list at line @
vhe	csp	list	list_miising_comma_csvh	W					Missing comma between @ and name at line @
vhe	csp	mifc	mifc_port_type_unsupported_csvh	е					Port type @ unsupported at line @
vhe	csp	mmod	mult_vhs_arg_div	е					Macro @ contains too many actual arguments
vhe	csp	mmod	miss_vhs_arg_div	е					at line @  Macro @ is missing
VIIC	СЗР	minod	IIII35_VII5_aIg_uiV						some actual arguments at line @
vhe	csp	mmod	not_else_vhs_div	е					Unmatched 'else directive at line @
vhe	csp	mmod	not_endif_vhs_div	е					Unmatched 'endif
vhe	csp	mmod	not_include_vhs_div	е					directive at line @ Missing filename for
									'include directive at line @
vhe	csp	mmod	bad_include_vhs_div	е					Badly formed include directive at line @
vhe	csp	mmod	fmis_include_vhs_div	е					Filename missing in #include directive at line
vhe	csp	mod	mod_miss_endmodule_csvh	е					@ Missing endmodule at
vhe	csp	mod	mod_no_module_found_csvh	е					line @ No modules found at line
vhe	csp	mod	mod_no_entity_found_csvh	е					@  No entity found at line @
vhe	csp	mod	mod_no_entity_found_csvh	e					No unit found at line @
vhe	csp	nett	nett_unsupported_reg_csvh	е					Unsupported register
vhe	csp	num	radix_h_num_vhs	ew					type @ at line @ Illegal number radix, 'h
vhe	csp	num	radix_b_num_vhs	ew					expected at line @ Illegal number radix, 'b
vhe	csp	num	radix_d_num_vhs	ew					expected at line @ Illegal number radix, 'd
vhe	csp	num	radix_o_num_vhs	ew					expected at line @ Illegal number radix; 'o
vhe	csp	parm	mod_parm_miss_csv	е					expected at line @ Module @ parameter
									declaration missing value at line @
vhe	csp	parm	entity_parm_miss_csv	е					Module @ parameter declaration missing value at line @
vhe	csp	parm	unit_parm_miss_csv	е					Module @ parameter declaration missing value
vhe	csp	port	ill_formal_port_name_csvh	е					at line @ Illegal formal port @ at
vhe	csp	pp	pp_cannot_open_file_not_exist_csvh	е					line @ Cannot open include file
									@, file does not exist at line @
vhe	csp	pp	pp_cannot_open_file_not_have_read_perm_csvh	е					Cannot open include file @, file does not have
									read permission at line @
vhe	csp	prts	define_ill_prts_csv	е					Illegal part select specifier, define missing
vhe	csp	prts	prts_part_select_csvh	е					at line @ Badly formed part select
vhe	csp	sdir	synopsys_cdir_csvh	W					at line @ Found Synopsys
									compiler directive at line @
vhe vhe	csp	stmt stmt	miss_comma_stmt_vhs miss_semicolon_stmt_vhs	e e					Missing comma at line @ Missing semi colon at
vhe	•	stmt	miss_char_stmt_vhs						line @ Missing @ at line @
vhe	csp csp	stmt	wait_kword_stmt_vhs	e					@ expected at line @
vhe	csp	stmt	null_not_allowed_stmt_csvh	е					Null statement is not allowed here at line @
vhe	csp	str	ill_str_char_found_csvh	е					Illegal character @ found after backslash at line @
vhe	csp	sysc	system_call_csvh	w					Found system call @ at line @
vhe	csp	udir	other_cdir_csvh	W					Found other compiler directive at line @
vhe	prp	file	not_dir_name_file_vhp	е					Directory @ does not

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	prp	file	cannot_open_file_ppvh	е					exist at line @ Cannot open file @ at line @
vhe	prp	pp	not_incl_directive_pp_ppvh	е					Empty filename for 'include directive at line
vhe	prp	pp	pp_miss_macroname_vh	е					@ Missing macro name at
vhe	prp	pp	ill_macroname_pp_vh	е					line @ Illegal macro name @ at line @
vhe	prp	pp	pp_text_macro_rec_vh	е					Text macro string used recursively at line @
vhe	prp	pp	pp_cannot_open_libfile_ppvh	е					Cannot open library file  @ at line @
vhe	prp	pp	pp_text_macroname_not_defined_ppvh	е					Text macro (name) not defined at line @
vhe	prp	pp	pp_ifdef_miss_macroname_ppvh	е					'ifdef missing macro
vhe	prp	pp	pp_undef_miss_macroname_ppvh	е					name at line @ 'undef missing macro name at line @
vhe	prp	pp	pp_miss_endif_directive_ppvh	е					Missing 'endif directive at line @
vhe	prp	pp	pp_rec_include_file_ppvh	е					Recursive INCLUDE file @ at line @
vhe	prp	pp	cmdl_arg_used_in_def_ppvh	е					Command line argument
vhe	prp	pp	pp_undef_macro_ppvh	е					used in define at line @ Undef @ not defined macro at line @
vhe	vep	ccd	misplaced_csdir_ignored_vevh	е				х	Lower case directive in wrong location. Ignored
vhe	vep	cmdl	ill_cmdl_uselib_dir_path_vhve	е					at line @ Illegal 'uselib directory path @ no such directory
									at line @
vhe	vep	cmnt	vhe_vep_cmnt_miss_closing_vevh	е					/* comment missing closing */ at line @ Missing character @ at
vhe	vep	csi	miss_char_case_vevh	е					Missing character @ at line @
vhe	vep	expr	malformed_unary_expr_vvep	е					Malformed unary Expression @ at line @
vhe	vep	expr	malformed_binary_expr_vvep	е					Malformed binary Expression @ at line @
vhe	vep	expr	malformed_ternary_expr_vvep	е					Malformed ternary Expression @ at line @
vhe	vep	expr	expr_found_reserved_word_vevh	е					Expected identifier but found reserved word @
vhe	vep	expr	expr_concatenation_empty_vevh	е					at line @ Concatenation empty at line @
vhe	vep	expr	ill_operator_expr_vevh	е					Illegal operator @ at line
vhe	vep	expr	ill_operand_expr_vevh	е					@ Illegal operand @ at line @
vhe	vep	file	cannot_open_file_vevh	е					Cannot open file @ at line @
vhe	vep	file	line_lenght_overflow_vevh	е					Line length overflow
vhe	vep	file	environ_var_in_filel_vevh	е					line_length @ at line @ Environ variable in file list
vhe	vep	func	undefined_func_vevh	е					at line @ Undefined function @ at
vhe	vep	inst	ill_mod_inst_name_vevh	е					line @
vhe	vep	inst	ill_entity_inst_name_vevh	е					@ at line @ Illegal entity instance @
vhe	vep	inst	ill_unit_inst_name_vevh	е					at line @ Illegal unit instance @ at
vhe	vep	lib	not_open_lib_file_vevh	е					line @ Cannot open library file
vhe	vep	list	trail_comma_list_vhc	е					@ at line @ Trailing comma in parentheses enclosed list
vhe	vep	list	list_miising_comma_vevh	W					at line @ Missing comma between
vhe	vep	mifc	mifc_port_type_unsupported_vevh	е					@ and name at line @ Port type @ unsupported
vhe	vep	mmod	mult_vhc_arg_div	е					at line @ Macro @ contains too
									many actual arguments at line @
vhe	vep	mmod	miss_vhc_arg_div	е					Macro @ is missing some actual arguments at line @
vhe	vep	mmod	not_else_vhc_div	е					Unmatched 'else directive at line @
vhe	vep	mmod	not_endif_vhc_div	е					Unmatched 'endif directive at line @
vhe	vep	mmod	not_include_vhc_div	е					Missing filename for 'include directive at line
vhe	vep	mmod	bad_include_vhc_div	е					@ Badly formed include

Vie   Vep   mmo	Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
we vep   nood   mod_miss_endmoodule_vevh   e   Messing_manuale_manuale_vevh   e   Messing_manuale_manuale_vevh   e   Messing_manuale_manuale_manuale_manuale_manuale_vevh   e   Messing_manuale_manu	vhe	ven	mmod	fmis include vhc div	6					directive at line @
vie vep mod mod_no_module_found_vevh e No modules found at line @ No mod mod_no_mit_found_vevh e No entry found at line @ No unit_found at line @ No mod mod_no_mit_found_vevh e No unit_found at line @ No unit_found at line @ No unit_found at line @ Unit_modules_found_vevh e Unit_modules_found_vevh e Unit_modules_found_vevh e Unit_modules_found_vevh e Unit_modules_found_vevh e Unit_modules_found_vevh e With evep num radx_b_num_vhc ew Illegal number radx_very expected at line @ No expected at line @	VIIC	VCP	minod	IIIIS_IIIOIddo_viio_div						#include directive at line @
vie   vsp   mod	vhe	vep	mod		е					line @
Vine         Vep         Pomod         mod of, pountly found, versh         e         No entity found at line @ vine very next           Vine         Vep         not         mod of, pountly found at line @ vine very next         No unit found at line @ vine very next           Vine         Vep         num         rads_b_num_vinc         ev         Illegal number rads, b_num_vinc           Vine         Vep         num         rads_b_num_vinc         ev         Illegal number rads, b_num_vinc           Vine         Vep         num         rads_b_num_vinc         ev         Illegal number rads, b_num_vinc           Vine         Vep         num         rads_b_num_vinc         ev         expected at line @ sexpected at line @ s	vhe	vep	mod	mod_no_module_found_vevh	е					
vine         vep         nett         Institution of path         Unsupported register type 8 at 11ms           vine         vep         num         radic_h_num_whc         ew         Illegal number radix. Vex expected at line 8 and supported register type 8 at 11ms           vine         vep         num         radix_b_num_whc         ew         Illegal number radix. Vex expected at line 8 and supported register type 1 ms           vine         vep         num         radix_b_num_whc         ew         Illegal number radix. Vex expected at line 8 and supported register type.           vine         vep         pam         mod_pam_miss_vev         e         declaration missain and states of the supported at all radios. And supported at a										No entity found at line @
vine vep num radix_h_num_hc ew lliggal number radix, in expected at line @ expected at li										
vhe vep num radix_b_num_vhc ew expected at line @ suppeted suppete										type @ at line @
vhe         vep         num         fadix_D_num_vhc         ew         Illegal number radix, operated at line @illegal number radix, opera	vhe	vep	num	radix_h_num_vhc	ew					
vhe vep parm mod_parm_miss_vev e de description de lilegal unber radix o expected at line @ vive vep parm mod_parm_miss_vev e de description de lilegal unber radix o expected at line @ vive vep parm entity_parm_miss_vev e de description de line @ vive vep parm unit_parm_miss_vev e de description de line @ vive vep parm unit_parm_miss_vev e de description missing value de line @ vive vep parm unit_parm_miss_vev e de description missing value de line @ vive vep parm unit_parm_miss_vev e de description missing value vive vep parm unit_parm_miss_vev e de description missing value vive vep parm unit_parm_miss_vev e de description missing value vive vep parm unit_parm_miss_vev e de lilegal formal port @ at ine @ lilegal formal port @ at ine @ vive vep pp pp_cannot_open_file_not_exist_vevh e Cannot open include file @, file dose not have read permission at line de lilegal formal port @ at ine @ vive vep pris define_lil_pris_vev e description de lilegal formal port @ at ine @ lilegal formal port @ at ine @ lilegal formal port @ at ine @ vive vep pris pris_part_select_vevh e description de lilegal formal port @ at ine @	vhe	vep	num	radix_b_num_vhc	ew					Illegal number radix, 'b
Vibr         Vep         num         radix_o_num_yhc         ew         Illigal number radix: operating with the parameter of expected at his @ mod_parm_miss_vev         e         Module B parameter declaration missing value at line @ Module B parameter d	vhe	vep	num	radix_d_num_vhc	ew					
vhe         vep         parm         mod_parm_miss_vev         e         Module @ parameter bedicatation missing value at line @ Module @ parameter bedicatation missing value at line @ Module @ parameter bedicatation missing value at line @ Module @ parameter bedicatation missing value at line @ Module @ parameter bedicatation missing value at line @ Module @ parameter bedicatation missing value at line @ Module @ parameter bedicatation missing value at line @ Module @ parameter bedicatation missing value at line @ Illegal formal port @ Module @ parameter bedicatation missing value at line @ Illegal formal port @ Module @ parameter bedicatation missing value at line @ Module @ parameter bedicatation missing value at line @ Module @ parameter bedicatation missing value at line @ Module @ parameter bedicatation missing value at line @ Module @ parameter bedicatation missing value at line @ Cannot open include file @ Module @ parameter bedicatation missing value at line @ Cannot open include file @ Module @ parameter bedicatation missing value at line @ Cannot open include file @ Module @ parameter bedicatation missing value at line @ Cannot open include file @ Module @ parameter bedicatation missing value at line @ Module @ parameter bedication file file doctors on the file of the parameter bedication file file file doctors on the file open file file file file file file file file	vhe	vep	num	radix_o_num_vhc	ew					Illegal number radix; 'o
whe         vep         parm         entity_parm_miss_vev         e         Module @ parameter declaration missaing value at line @ and at line @           vhe         vep         parm         unit_parm_miss_vev         e         Module @ parameter declaration missaing value at line @           vhe         vep         port         Ill_[ginzal_port_name_vevh]         e         Ill_[dingal_port_name_vevh]         e         Module @ parameter declaration missaing value at line @         Module @ parameter declaration missaing value at line @         Module @ parameter declaration missaing value at line @         Module @ parameter declaration missaing value at line @         Module @ parameter declaration missaing value at line @         Module @ parameter declaration missaing value at line @         Module @ parameter declaration missaing value at line @         Module @ parameter declaration missaing value at line @         Module @ parameter declaration missaing value at line @         Module @ parameter declaration missaing value at line @         Cannot open file_not declaration missaing value at line @         Cannot open file_not @         Cannot open file_not @         A         Cannot open file_not @ <td>vhe</td> <td>vep</td> <td>parm</td> <td>mod_parm_miss_vev</td> <td>е</td> <td></td> <td></td> <td></td> <td></td> <td>Module @ parameter declaration missing value</td>	vhe	vep	parm	mod_parm_miss_vev	е					Module @ parameter declaration missing value
vhe vep parm unit_parm_miss_vev e de declaration missing value at line @ footble parameter declaration missing value at line @ stilled parameter declaration parameter declaration value at line @ stilled parameter declaration value at line @ stilled parameter declaration value at line @ stilled parameter declaration value at line @ cannot open include file @, file does not have read permission at line @ cannot open include file @, file does not have read permission at line @ cannot open include file @, file does not have read permission at line @ stilled parameter declaration value file get whe line get whe vep prts define all prts_vev e lill_galp at select at line @ stilled value at line @ stilled value file get whe line get whe vep stimt miss_centation part whe line @ stilled value file declaration value file get whe line get whe vep still_str_char_found_vevh e lill_str_char_found_vevh e lill_str_char_found_vevh e lill_str_char_found_vevh who will_not_allowed_still_vevh who will_not_allowed_still_vevh will_n	vhe	vep	parm	entity_parm_miss_vev	е					Module @ parameter
vhe         vep         port         ill_formal_port_name_vevh         e         declaration missing value at line @           vhe         vep         pp         jpp_cannot_open_file_not_exist_vevh         e         Illegal formal port @ at line @           vhe         vep         pp         pp_cannot_open_file_not_have_read_perm_vevh         e         @ file does not exist at low exist.           vhe         vep         pp         pp_cannot_open_file_not_have_read_perm_vevh         e         @ Cannot open include file @ file does not have read permission at line @           vhe         vep         prts         define_iil_prts_vev         e         Illegal part select specifier does not at line @           vhe         vep         prts         prts_part_select_vevh         e         Badly formad part select specifier define missing at line @           vhe         vep         prts         prts_part_select_vevh         w         Badly formad part select specifier define at line @           vhe         vep         prts_part_select_vevh         w         Badly formad part select specifier define at line @           vhe         vep         stmit         miss_centrul         define_iiil_prts_vevh         e         Missing comma at line @           vhe         vep         stmit         miss_centrul         miss_centrul <t< td=""><td>vho</td><td>von</td><td>narm</td><td>unit parm miss you</td><td></td><td></td><td></td><td></td><td></td><td>at line @</td></t<>	vho	von	narm	unit parm miss you						at line @
veb         vep         port         ill_strmal_port_name_vevh         e         Illegal formal port @ at line @ line @ cannot open include file of the cose not exist at line @ cannot open include file of the cose not exist at line @ cannot open include file of the cose not nave read permon at line @ cannot open include file of the cose not nave read permon at line @ cannot open include file of the cose not nave read permon at line @ cannot open include file of the cose not nave read permon at line @ cannot open include file of the cose not nave read permon at line @ cannot open include file of the cose not nave read permon at line @ cannot open include file of the cose not nave read permon at line @ cannot open include file of the cose not exist at line @ cannot open include file of the cose not exist at line @ cannot open include file of the cose o	viie	vep	pailii	unicpani_mss_vev	е					declaration missing value
vhe vep pris define_iil_pris_vev e lillegal part select set in e @ contot pen_file_not_have_read_perm_vevh e lillegal part select set in e @ selective, define missing selective, define de	vhe	vep	port	ill_formal_port_name_vevh	е					Illegal formal port @ at
Whe         vep         pp         pp_cannot_open_file_not_have_read_perm_vevh         e         @ cannot open_file_depen_file_depen_file_depen_gen_gen_gen_gen_gen_gen_gen_gen_gen_g	vhe	vep	pp	pp_cannot_open_file_not_exist_vevh	е					@, file does not exist at
vhe         vep         prts         define_ill_prts_vev         e         Illegal part select seption, seption, at line @ seption, define missing at line @ a	vhe	vep	pp	pp_cannot_open_file_not_have_read_perm_vevh	е					
vep   pris   define_ill_pris_vev   e										read permission at line
Whe         Vep         prts         prts_part_select_vevh         e         Badly formed part select           Whe         Vep         sdir         synopsys_cdir_evvh         w         Found Synopsys complied directive at line @           Vhe         Vep         stmt         miss_comma_stmt_vhc         e         Missing comma at line @           Vhe         Vep         stmt         miss_cemicolon_stmt_vhc         e         Missing gemi colon at line @           Vhe         Vep         stmt         miss_char_stmt_vhc         e         Missing gemi colon at line @           Vhe         Vep         stmt         miss_char_stmt_vhc         e         Missing gemi colon at line @           Vhe         vep stmt         wait_kword_stmt_vhc         e         Missing gemi colon at line @           Vhe         vep stmt         miss_char_stmt_vhc         e         Missing gemi colon at line @           Vhe         vep stmt         miss_char_stmt_vhc         e         Missing gemi colon at line @           Vhe         vep stmt         miss_char_stmt_vhc         e         Missing demarker         demark	vhe	vep	prts	define_ill_prts_vev	е					Illegal part select
Vhe         vep         sdir         synopsys_cdir_evvh         w         Found Synopsys complet directive at line @ complet directive at at line @ whe vep stmt         Missing comma at line @ Missing semi colon at line @ with vep stmt         Missing semi colon at line @ Missing semi colon at line @ with vep stmt         Missing semi colon at line @ with sine @ with with sine with very with very with with sine with very with very stmt         Missing at line @ with with sine with with sine with very with very with very with very stmt. Very with very stmt         Missing at line @ with with sine with with very with very with very with very stmt. Very with ve	vhe	vep	prts	prts_part_select_vevh	е					Badly formed part select
whe vep stmt miss_comma_stmt_vho e Missing comma at line @ Missing @ Missing @ At line @ Missing @ Missing @ Missing character @ found other complete whe will missing directory at line @ Missing character @ At line @	vhe	vep	sdir	synopsys cdir evvh	w					
whe         vep         stmt         miss_char_stmt_vhc         e         Missing semi colon at line @           whe         vep         stmt         miss_char_stmt_vhc         e         Missing @ at line @           whe         vep         stmt         wait_kword_stmt_vbc         e         Missing @ at line @           whe         vep         stmt         mul_not_allowed_stmt_vevh         e         Mull statement is not allowed here at line @           whe         vep         str         ill_str_char_found_vevh         e         millegal character @ found after backslash at line @           vhe         vep         system_call_vevh         w         Found other compiler directive at line @           vhe         vep         udir         other_cdir_vevh         w         Found other compiler directive at line @           vhe         vep         udir         other_cdir_vevh         w         Found other compiler directive at line @           vhe         vhp         ccd         missplaced_csdir_ignored_vhvh         e         x         Lover case directive in wrong location, lgnored at line @           vhe         vhp         cmd         ill_candl_uselib_dir_path_vhvh         e         Illegal uselib directory path @ no such		·		, , , = =						compiler directive at line @
vhe         vep         stmt         miss_char_stmt_vhc         e         Missing@ at line @           vhe         vep         stmt         wait_kword_stmt_vhc         e         @ expected at line @           vhe         vep         stmt         null_not_allowed_stmt_vevh         e         @ expected at line @           vhe         vep         stmt         null_not_allowed_stmt_vevh         e         Mull statement is not allowed here at line @           vhe         vep         str         iil_str_char_found_vevh         e         lllegal character @ found after backslash at line @           vhe         vep         system_call_vevh         w         Found other compiler directive at line @           vhe         vep         udir         other_cotir_vevh         w         Found other compiler directive at line @           vhe         vhp         cd         misplaced_csdir_ignored_vhvh         e         x         Lower case directive in wrong location. Ignored at line @           vhe         vhp         cd         misplaced_csdir_ignored_vhvh         e         x         Lower case directive in wrong location. Ignored at line @           vhe         vhp         cmnt         iil_centry_attribute         at line @         x           vhe         vhp         cmnt					_					Missing comma at line @
whe         vep         stmt         wait, kword_stmt_vevh         e         @ expected at line @           whe         vep         stmt         null_not_allowed_stmt_vevh         e         Null statement is not allowed here at line @           whe         vep         str         iil_str_char_found_vevh         e         lillegal character @ found after backslash at line @           vhe         vep         sysc         system_call_vevh         w         Found system call @ at line @           vhe         vep         udir         Other_cdir_eveh         w         Found other compiler directive at line @           vhe         vhp         cdd         misplaced_csdir_ignored_vhvh         e         x         Lower case directive in wrong location. Ignored at line @           vhe         vhp         cmdl         iil_cmdl_uselib_dir_path_vhvh         e         Illegal 'uselib directory path @ no such directory at line @           vhe         vhp         cmnt         vhe_vhp_cmnt_miss_closing_vhvh         e         Illegal 'uselib directory path @ no such director		VCP			١					line @
Vhe         vep         stmt         null_not_allowed_stmt_vevh         e         Null statement is not allowed here at line @ lillegal character @ found after backslash at line @ vep           Vhe         vep         str         iill_str_char_found_vevh         e         illegal character @ found after backslash at line @ Found system call @ at line @           Vhe         vep         udir         other_cdir_vevh         w         Found other compiler directive at line @           Vhe         vhp         ccd         misplaced_csdir_ignored_vhvh         e         x         Lower case directive in wrong location. Ignored at line @           Vhe         vhp         cmdl         ill_cmdl_uselib_dir_path_vhvh         e         Illiegal vselib directory path @ no such directory at line @           Vhe         vhp         cmnt         vhe_vhp_cmnt_miss_closing_vhvh         e         // comment missing closing '/ at line @           Vhe         vhp         csin         miss_char_case_vhvh         e         Missing_character@ at line @           Vhe         vhp         csi         miss_char_case_vhvh         e         Malformed unary Expression @ at line @           Vhe         vhp         expr         malformed_unary_expr_vvhp         e         Malformed unary Expression @ at line @           Vhe         vhp         expr         malf										Missing @ at line @
Vhe         vep         str         ill_str_char_found_vevh         e         illegal character @ found after backslash at line @           Vhe         vep         sysc         system_call_vevh         w         Found system call @ at line @           Vhe         vep         udir         other_cdir_vevh         w         Found other compiler directive at line @           Vhe         vhp         ccd         misplaced_csdir_ignored_vhvh         e         x         Lower case directive in wrong location, ignored at line @           Vhe         vhp         cmdl         ill_cmdl_uselib_dir_path_vhvh         e         Illegal uselib directory path @ no such directory at line @           Vhe         vhp         cmnt         vhe_vhp_cmnt_miss_closing_vhvh         e         Illegal uselib directory path @ no such directory path @ no suc										Null statement is not
vhe         vep         sysc         system_call_vevh         w         Found system call @ at line @           vhe         vep         udir         other_cdir_vevh         w         Found other compiler directive at line @           vhe         vhp         ccd         misplaced_csdir_ignored_vhvh         e         x         Lower case directive in wrong location. Ignored at line @           vhe         vhp         cmdl         ill_cmdl_uselib_dir_path_vhvh         e         Illegal 'uselib directory path @ no such directory at line @           vhe         vhp         cmnt         vhe_vhp_cmnt_miss_closing_vhvh         e         /* comment missing closing '7 at line @           vhe         vhp         csi         miss_char_case_vhvh         e         Missing character @ at line @           vhe         vhp         expr         malformed_unary_expr_vvhp         e         Malformate and line @           vhe         vhp         expr         malformed_binary_expr_vvhp         e         Malformed binary           vhe         vhp         expr         malformed_ternary_expr_vvhp         e         Malformed binary           vhe         vhp         expr         malformed_ternary_expr_vvhp         e         Expression @ at line @           vhe         vhp         expr_soln @ a	vhe	vep	str	ill_str_char_found_vevh	е					Illegal character @ found
vhe         vhp         ccd         misplaced_csdir_ignored_vhvh         e         x         Lower case directive in wrong location. Ignored at line @           vhe         vhp         cmdl         ill_cmdl_uselib_dir_path_vhvh         e         Illegal 'uselib directory path @ no such directory at line @           vhe         vhp         cmnt         vhe_vhp_cmnt_miss_closing_vhvh         e         /* comment missing closing */ at line @           vhe         vhp         csi         miss_char_case_vhvh         e         Missing character @ at line @           vhe         vhp         expr         malformed_unary_expr_vvhp         e         Malformed unary Expression @ at line @           vhe         vhp         expr         malformed_binary_expr_vvhp         e         Malformed binary Expression @ at line @           vhe         vhp         expr         malformed_ternary_expr_vvhp         e         Malformed ternary Expression @ at line @           vhe         vhp         expr         expr_s_vhe         e         Expression @ at line @           vhe         vhp         expr         expr_concatenation_empty_vhvh         e         Expected identifier but found reserved word @ at line @           vhe         vhp         expr         ill_operand_expr_vhvh         e         Illegal operand @ at line @ <td>vhe</td> <td>vep</td> <td>sysc</td> <td>system_call_vevh</td> <td>W</td> <td></td> <td></td> <td></td> <td></td> <td>Found system call @ at</td>	vhe	vep	sysc	system_call_vevh	W					Found system call @ at
vhe         vhp         ccd         misplaced_csdir_ignored_vhvh         e         x         Lower case directive in wrong location. Ignored at line @           vhe         vhp         cmdl         ill_cmdl_uselib_dir_path_vhvh         e         Illegal 'uselib directory path @ no such directory at line @           vhe         vhp         cmnt         vhe_vhp_cmnt_miss_closing_vhvh         e         /* comment inissing closing */ at line @           vhe         vhp         csi         miss_char_case_vhvh         e         Missing character @ at line @           vhe         vhp         expr         malformed_unary_expr_vvhp         e         Malformed onary Expression @ at line @           vhe         vhp         expr         malformed_binary_expr_vvhp         e         Malformed binary Expression @ at line @           vhe         vhp         expr         malformed_ternary_expr_vvhp         e         Malformed ternary Expression @ at line @           vhe         vhp         expr         expr_sound_reserved_word_vvhy         e         Expression Sat line @           vhe         vhp         expr         expr_concatenation_empty_vvhyh         e         Expression Sat line @           vhe         vhp         expr         expr_concatenation_empty_vvhyh         e         Concatenation empty at line @	vhe	vep	udir	other_cdir_vevh	w					
vhe         vhp         cmdl         ill_cmdl_uselib_dir_path_vhvh         e         Illegal uselib directory path @ no such directory path @ no such directory at line @           vhe         vhp         cmnt         vhe_vhp_cmnt_miss_closing_vhvh         e         /* comment missing closing 'val tine @           vhe         vhp         csi         miss_char_case_vhvh         e         Missing character @ at line @           vhe         vhp         expr         malformed_unary_expr_vvhp         e         Malformed unary Expression @ at line @           vhe         vhp         expr         malformed_binary_expr_vvhp         e         Malformed binary Expression @ at line @           vhe         vhp         expr         malformed_ternary_expr_vvhp         e         Malformed ternary Expression @ at line @           vhe         vhp         expr         expr_s_s_vhe         e         Expression @ at line @           vhe         vhp         expr         expr_solund_reserved_word_vhvh         e         Expression @ at line @           vhe         vhp         expr         expr_solund_reserved_word_vhvh         e         Expression @ at line @           vhe         vhp         expr         expr_solund_reserved_word_vhvh         e         Expression @ at line @           vhe         vhp	vhe	vhp	ccd	misplaced_csdir_ignored_vhvh	е				х	Lower case directive in
vhe         vhp         cmnt         vhe_vhp_cmnt_miss_closing_vhvh         e         /* comment missing closing */ at line @           vhe         vhp         csi         miss_char_case_vhvh         e         Missing character @ at line @           vhe         vhp         expr         malformed_unary_expr_vvhp         e         Malformed binary Expression @ at line @           vhe         vhp         expr         malformed_binary_expr_vvhp         e         Malformed binary Expression @ at line @           vhe         vhp         expr         malformed_ternary_expr_vvhp         e         Malformed binary Expression @ at line @           vhe         vhp         expr         malformed_ternary_expr_vvhp         e         Malformed binary Expression @ at line @           vhe         vhp         expr         malformed_ternary_expr_vvhp         e         Expression @ at line @           vhe         vhp         expr         expr_s_vhe         e         Expression @ at line @           vhe         vhp         expr         expr_sound_reserved_word_vhvh         e         Expression @ at line @           vhe         vhp         expr         expr_concatenation_empty_vhvh         e         Concatenation empty at line @           vhe         vhp         expr         ill_operand_	vhe	vhp	cmdl	ill_cmdl_uselib_dir_path_vhvh	е					at line @ Illegal 'uselib directory
vhe       vhp       csi       miss_char_case_vhvh       e       Missing character @ at line @         vhe       vhp       expr       malformed_unary_expr_vvhp       e       Malformed unary Expression @ at line @         vhe       vhp       expr       malformed_binary_expr_vvhp       e       Malformed binary Expression @ at line @         vhe       vhp       expr       malformed_ternary_expr_vvhp       e       Malformed ternary Expression @ at line @         vhe       vhp       expr       expr_s_vhe       e       Expression @ at line @         vhe       vhp       expr       expr_soin S at line @       Expression @ at line @         vhe       vhp       expr       expr_soin S at line @       Expression @ at line @         vhe       vhp       expr       expr_soin S at line @       Expression @ at line @         vhe       vhp       expr_found_reserved_word_vhvh       e       Expected identifier but found reserved word @ at line @         vhe       vhp       expr_concatenation_empty_vhvh       e       Concatenation empty at line @         vhe       vhp       expr_concatenation_empty_vhvh       e       Illegal operator @ at line @         vhe       vhp       expr_concatenation_empty_vhvh       e       Illegal operator @ at line @										at line @
vhe       vhp       expr       malformed_unary_expr_vvhp       e       Malformed unary Expression @ at line @ Expression @ at line @ Malformed binary Expression @ at line @ Malformed binary Expression @ at line @ Malformed ternary Expression @ at line @ Malformed ternary Expression @ at line @ Walformed ternary Expression @ Walformed Walformed Walformed Walformed Walfor Walfo				_ ,	е					closing */ at line @
vhe       vhp       expr       malformed_unary_expr_vvhp       e       Malformed unary Expression @ at line @ Malformed binary Expression @ at line @ Malformed binary Expression @ at line @ Expression @ at line @ Malformed ternary Expression @ at line @ Malformed ternary Expression @ at line @ Expression @ at line @ Expression S at line @ Illegal operated word @ at line @ Expression S at line @ Illegal operated word @ at line @ Illegal operated word @ at line @ Illegal operator @ at line @ Illegal operator @ at line @ Illegal operator @ at line @ Illegal operand	vhe	vhp	csi	miss_char_case_vhvh	е					
vhe         vhp         expr         malformed_binary_expr_vvhp         e         Malformed binary Expression @ at line @ Malformed ternary Expression @ at line @ Malformed ternary Expression @ at line @ Yes expr           vhe         vhp         expr         expr_s_vhe         e         expression S at line @ It line @ Expression S at line @ Expression S at line @ Expression S at line @ It line Ength overflow line length @ at line @ It line & It line @ It line & It line @ It line & It line	vhe	vhp	expr	malformed_unary_expr_vvhp	е					Malformed unary
vhe     vhp     expr     malformed_ternary_expr_vvhp     e     Malformed ternary Expression @ at line @ Expression @ at line @ Expression S at line @ Illegal operated dentifier but found reserved word @ at line @ Concatenation empty at line @ Illegal operator expr_vhvh       vhe     vhp     expr     expr_concatenation_empty_vhvh     e     e     Illegal operator @ at line @ Illegal operato	vhe	vhp	expr	malformed_binary_expr_vvhp	е					Malformed binary
vhe         vhp         expr         expr_s_vhe         e         Expression S at line @           vhe         vhp         expr         expr_found_reserved_word_vhvh         e         Expected identifier but found reserved word @ at line @           vhe         vhp         expr         expr_concatenation_empty_vhvh         e         Concatenation empty at line @           vhe         vhp         expr         ill_operator_expr_vhvh         e         Illegal operator @ at line @           vhe         vhp         expr         ill_operand_expr_vhvh         e         Illegal operand @ at line @           vhe         vhp         file         cannot_open_file_vhvh         e         Cannot open file @ at line @           vhe         vhp         file         line_length_overflow_vhvh         e         Line length overflow line_length @ at line @	vhe	vhp	expr	malformed_ternary_expr_vvhp	е					Malformed ternary
the vhp expr expr_concatenation_empty_vhvh e Concatenation empty at line @  vhe vhp expr ill_operator_expr_vhvh e lllegal operator @ at line @  vhe vhp expr ill_operand_expr_vhvh e lllegal operand @ at line @  vhe vhp file cannot_open_file_vhvh e Cannot open file @ at line @  vhe vhp file line_lenght_overflow_vhvh e line_length @ at line @										Expression S at line @
vhe     vhp     expr     expr_concatenation_empty_vhvh     e     Concatenation empty at line @       vhe     vhp     expr     ill_operator_expr_vhvh     e     Illegal operator @ at line @       vhe     vhp     expr     ill_operand_expr_vhvh     e     Illegal operand @ at line @       vhe     vhp     file     cannot_open_file_vhvh     e     Cannot open file @ at line @       vhe     vhp     file     line_length_overflow_vhvh     e     Line length overflow line_length @ at line @	vhe	vhp	expr	expr_found_reserved_word_vhvh	е					found reserved word @
vhe     vhp     expr     ill_operator_expr_vhvh     e     Illegal operator @ at line @       vhe     vhp     expr     ill_operand_expr_vhvh     e     Illegal operand @ at line @       vhe     vhp     file     cannot_open_file_vhvh     e     Cannot open file @ at line @       vhe     vhp     file     line_lenght_overflow_vhvh     e     Line length overflow line_length @ at line @	vhe	vhp	expr	expr_concatenation_empty_vhvh	е					Concatenation empty at
vhe     vhp     expr     ill_operand_expr_vhvh     e     Illegal operand @ at line @       vhe     vhp     file     cannot_open_file_vhvh     e     Cannot open file @ at line @       vhe     vhp     file     line_length_overflow_vhvh     e     Line length overflow line_length @ at line @	vhe	vhp	expr	ill_operator_expr_vhvh	е					Illegal operator @ at line
vhe     vhp     file     cannot_open_file_vhvh     e     Cannot open file @ at line @       vhe     vhp     file     line_lenght_overflow_vhvh     e     Line length overflow line_length @ at line @	vhe	vhp	expr	ill_operand_expr_vhvh	е					Illegal operand @ at line
vhe     vhp     file     line_lenght_overflow_vhvh     e     Line length overflow line_length @ at line @	vhe	vhp	file	cannot_open_file_vhvh	е					Cannot open file @ at
	vhe	vhp	file	line_lenght_overflow_vhvh	е					Line length overflow
	vhe	vhp	file	environ_var_in_filel_vhvh	е					

Cat	Phase	Туре	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	vhp	func	undefined_func_vhvh	е					at line @ Undefined function @ at
vhe	vhp	inst	ill_mod_inst_name_vhvh	е					line @ Illegal module instance
vhe	vhp	inst	ill_entity_inst_name_vhvh	е					@ at line @ Illegal entity instance @
vhe	vhp	inst	ill_unit_inst_name_vhvh	е					at line @ Illegal unit instance @ at
vhe	vhp	lib	not_open_lib_file_vhvh	е					line @ Cannot open library file
vhe	vhp	list	trail_comma_list_vhh	е					@ at line @ Trailing comma in
									parentheses enclosed list at line @
vhe	vhp	list	list_miising_comma_vhvh	W					Missing comma between @ and name at line @
vhe	vhp	mifc	mifc_port_type_unsupported_vhvh	е					Port type @ unsupported at line @
vhe	vhp	mmod	mult_vhh_arg_div	е					Macro @ contains too many actual arguments
vhe	vhp	mmod	miss_vhh_arg_div	е					at line @  Macro @ is missing
viie	viip	minou	miss_vim_arg_uiv	е					some actual arguments at line @
vhe	vhp	mmod	not_else_vhh_div	е					Unmatched 'else
vhe	vhp	mmod	not_endif_vhh_div	е					directive at line @ Unmatched 'endif
vhe	vhp	mmod	not_include_vhh_div	е					directive at line @ Missing filename for
									'include directive at line @
vhe	vhp	mmod	bad_include_vhh_div	е					Badly formed include directive at line @
vhe	vhp	mmod	fmis_include_vhh_div	е					Filename missing in #include directive at line
vhe	vhp	mod	mod_miss_endmodule_vhvh	е					@ Missing endmodule at
vhe	vhp	mod	mod_no_module_found_vhvh	е					line @ No modules found at line
vhe	vhp	mod	mod_no_entity_found_vhvh	е					@ No entity found at line @
vhe	vhp	mod	mod_no_unit_found_vhvh	е					No unit found at line @
vhe	vhp	nett	nett_unsupported_reg_vhvh	е					Unsupported register type @ at line @
vhe	vhp	num	radix_h_num_vhh	ew					Illegal number radix, 'h expected at line @
vhe	vhp	num	radix_b_num_vhh	ew					Illegal number radix, 'b expected at line @
vhe	vhp	num	radix_d_num_vhh	ew					Illegal number radix, 'd expected at line @
vhe	vhp	num	radix_o_num_vhh	ew					Illegal number radix; 'o expected at line @
vhe	vhp	parm	mod_parm_miss_vhv	е					Module @ parameter declaration missing value
vhe	vhn	norm	entity_parm_miss_vhv						at line @  Module @ parameter
VIIC	vhp	parm	enuty_pann_miss_vnv	е					declaration missing value at line @
vhe	vhp	parm	unit_parm_miss_vhv	е					Module @ parameter
									declaration missing value at line @
vhe	vhp vhp	pars port	S_stmt_pars_vh ill_formal_port_name_vhvh	e					Statement S at line @ Illegal formal port @ at
vhe	vhp	pp	pp_cannot_open_file_not_exist_vhvh	е					line @ Cannot open include file
									@, file does not exist at line @
vhe	vhp	pp	pp_cannot_open_file_not_have_read_perm_vhvh	е					Cannot open include file @, file does not have
									read permission at line @
vhe	vhp	pp	include_filne	е					Include file @ not found at line @
vhe	vhp	prts	define_ill_prts_vhv	е					Illegal part select specifier, define missing
vhe	vhp	prts	prts_part_select_vhvh	е					at line @ Badly formed part select
vhe	vhp	sdir	synopsys_cdir_vhvh	w					at line @ Found Synopsys
0	٦٠٠٣	2411							compiler directive at line
vhe	vhp	stmt	miss_comma_stmt_vhh	е					Missing comma at line @
vhe	vhp	stmt	miss_semicolon_stmt_vhh	е					Missing semi colon at line @
vhe	vhp	stmt	miss_char_stmt_vhh	е					Missing @ at line @
vhe	vhp	stmt	wait_kword_stmt_vhh	е					@ expected at line @
vhe	vhp	stmt	null_not_allowed_stmt_vhvh	е					Null statement is not allowed here at line @
vhe	vhp	str	ill_str_char_found_vhvh	е					Illegal character @ found
0	٠٠.٣								after backslash at line @

Cat	Phase	Type	Name	W/E	V1995	V2001	Sys_ver	Csl	Desc
vhe	vhp	sysc	system_call_vhvh	W					Found system call @ at
									line @
vhe	vhp	udir	other_cdir_vhvh	W					Found other compiler
									directive at line @