	CSL CLASS	Language syntax	lexer/misc	parser	Parser checks	tree walker	CSLOM cmd	СЅГОМ	CSLOM checker	CSLOM elab	Adaptor	СДОМ	CDOM checker	Verilog code gen	VHDL code gen	SystemC code gen	C++ code gen	document gen	CSIM codegen	CSLC ASM	IDE	Averages crt week	Averages prev week
	cslc: Verilog Parser	NA	90	90	0	90	NA	NA	NA	NA	NA	NA	NA	NA		NA		NA	NA	NA	0	67.5	0
1 /	cslc: CDOM	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	90	5	90	0	10		NA	NA	NA	0	39	0
14	cslc: CDOMNum	NA	100	100	NA	90	NA	NA	NA	NA	NA	90	0	NA	NA	NA		NA	NA	NA	0	76	0
2	cslc: Interconn cslc: Enum	90 90	100	100 100	98 100	98 100	95 80	95 100	10	NA NA	95 100	NA NA	NA NA	NA NA		NA	0 100	30	90 NA	NA 0	0	75.08 72.5	0
3	cslc: Field	90	100	100	100	100	80	90	0	NA	80	NA		NA		NA NA	100	0	NA	0	0	72.3 70	0
4		90	100	100	100	80	80	90	0	NA	70	NA		NA		NA	0	0	0	NA	0	59.17	0
5	cslc: ISA	90	100	100	100	80	80	90	0	NA	10	NA		NA		NA	0	0	0	0	0	50	0
_	cslc: Decoder	90	100	100	100	70	90	70	0	NA	100	NA		NA		NA	0	0	0	NA	0	60	0
7	cslc: VC	80	100	100		100	80	80	0	NA	50	NA		NA		NA	NA	0	90	NA	0	68.18	0
8	cslc: Tb	80	100	100		100	80	80	0	NA	50	NA		NA		NA	NA	0	0	NA	0	60	0
21	cslc: Tb clock gen	100	100	100	100	100	80	80	0	NA	100	NA	NA	NA	NA	NA	NA	0	0	NA	0	69.09	0
9	cslc: RF	90	100	100	100	100	70	90	0	NA	90	NA	NA	NA	NA	NA	NA	0	0	NA	0	67.27	0
	cslc: Fifo	90	100	100	100	100	60	60	0	NA	90	NA	NA	NA	NA	NA	NA	0	0	NA	0	63.64	0
11	cslc: Reg	90	100	100	100	100	80	80	0	NA	80	NA	NA	NΑ	NA	NA	0	0	0	NA	0	60.83	0
12	cslc: Pipeline	70	100	100	100	0	0	0	0	0	0	NA	NA	NA	NA	NA	0	0	0	NA	0	28.46	0
13	cslc: CSLOmNum	NA	100	100	100	100	NA	100	0	0	100	NA	NA	NA	NA	NA	0	0	0	NA	0	54.55	0
	Cslc: CSL stmt/expr	30	80	80	NA	50	NA	80	0	NA	50	NA	NA	NA	NA	NA	0	0	0	NA	0	37	0
	Cslc: CSL language	80	80	80	50	50	NA	50	0	0	50	NA	NA	NA	NA	NA	0	0	0	NA	0	36.67	0
	Cslc: CSL docgen	80	0	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	0	0	NA	0	13.33	0
17	cslc: autoroute	40	100	100	0	100	NA	50	0	50	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	55	0
	cslc:automapper	40	100	100	0	50	NA	30	0	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	40	0
16	cslc: inst tree	NA	NA	NA	NA	NA	NA	65	0	25	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	30	0
	Cslc: CLI	NA	100	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	0	100	0
	Cslc: verilog PP	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	0	0	0
	Cslc: CSL PP	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA		NA	NA	NA	0	0	0
15	Cslc: CSL PP/regex	NA	50	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA		NA	NA	NA	0	50	0
	Cslc: Top Level	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA		NA	NA	NA	0	0	0
24	Cslc: cmd line args	NA	50	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA		NA	NA	NA	0	50	0
	cslc: Memory	80	0	0	0	0	10	60	0	0	100	NA	NA		NA			NA	NA	NA	0	25	0
	cslc: Buses	0	0	0	0	0	0	0	0	NA	0	NA		_				NA		NA	0	0	0
	cslc: Procon cslc: Sched	0	0	0	0	0	0	0	0	0	0	NA	NA	_				NA		NA		0	0
	cslc: Sched	0	0	0	0	0	0	0	0	NA	0	NA NA		_				NA NA		NA NA	0	0	0
	cslc: ASM	0	0	0	0	0	0	0	0	0	0	NA	NA NA					NA	NA	0	0	0	0
	sw lib: ASM	NA	0	NA	0 NA	NA	NA	NA	NA	0 NA	NA	NA	NA					NA		NA	0	0	0
	sw lib: Csim	NA	20	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA					NA		NA	0	20	0
	cslc: GUI	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA						NA		NA	0	0	0
	clsc: cmd	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA			NA			NA		NA	0	0	0
	CSL pp: Aikido	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA		_	NA			NA		NA	NA	0	0
	HW: SOC bus ifc	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA		_	NA			NA		NA	NA	0	0
	HW: Processor ring	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA		_	NA			NA		NA	NA	0	0
	HW: RISC	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA		_	NA			NA		NA	NA	0	0
	HW: ASP	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA		_	NA			NA		NA	NA	0	0
	HW: MBIST	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA		_	NA			NA		NA	NA	0	0
	cslc: Reg v2	0	0	0	0	0	0	0	0	NA	0	NA	NA	NA	NA	NA	0	0	0	NA	0	0	0
	cslc: CSLOmNum v2	NA	0	0	0	0	0	0	0	0	0	NA			NA		0	0		NA	0	0	0
21	cslc: Tb PWLW	90	90	90	90	90	90	90	90	NA	100	NA	NA	NA	NA	NA	0	0	0	NA	0	68.33	0
	cslc: Tb stall gen	90	90	90	90	90	90	90	90	NA	0	NA	NA	NA	NA	NA	0	0	0	NA	0	60	0
21	cslc: Tb bubble gen	90	90	90	90	90	90	90	90	NA	0	NA	NA	NA	NA	NA	0	0	0	NA	0	60	0

not started
under construction
under test
completed
intersection between
Not applicable
Divider

Priorities
Low priority
medium priority
high pri

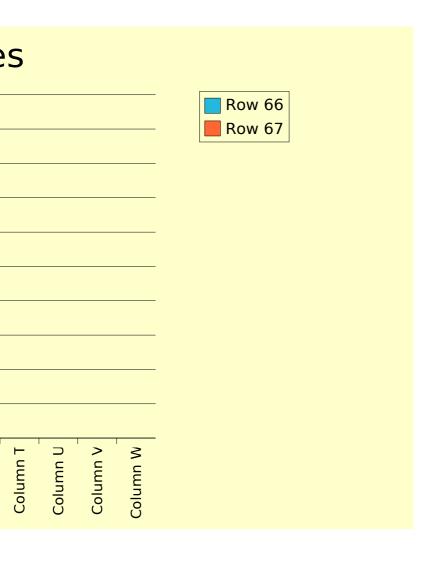
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misc/project_management/csl_class.ods

Stages	lexer	parser	tree walker	CSLOM	CSLOM checker	CSLOM elab	Adaptor	СДОМ	CDOM checker	Verilog code gen	Verilog code gen	SystemC code gen	C++ code gen	document code gen	CSIM	IDE
Averages crt week	57.11	72.22	63.77	9'.2	0.4	7.5	55.23	06	2.5	06	0	10	16.67	1.76	12	0
Averages prev week	misc/project_management/csl_class.ods	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0







erages prev week

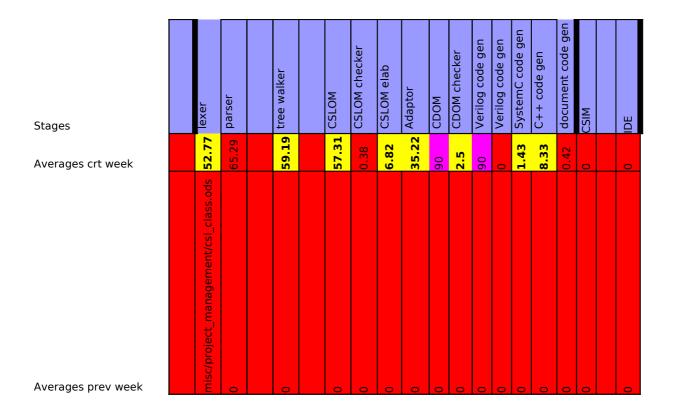


	CSL CLASS	Tests passing %	Language syntax	lexer/misc	o parser	Parser checks	tree walker	CSLOM cmd	CSLOM	CSLOM checker	CSLOM elab	Adaptor	CDOM	CDOM checker	Verilog code gen	VHDL code gen	SystemC code gen	C++ code gen	document gen	CSIM codegen	CSLC ASM	IDE IDE	Averages crt week	Averages prev week
	cslc: Verilog Parser	70	NA	90		0	90	_	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA			NA	0	67.5	0
1 /	cslc: CDOM	60	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	90	5	90	0	10	NA			NA	0	39	0
14	cslc: CDOMNum	0	NA	100	100	NA	90	NA	NA	NA	NA	NA	90	0	NA	NA	NA	NA			NA	0	76	0
T	cslc: Interconn	70	90	98	98	98	98	95	95	10	NA		NA	NA	NA	NA	NA	0	10		NA	0	65.17 66.92	0
2 3		70	90	100	100	100	100		100	0	NA		NA	NA	NA	NA	NA	100	0	0	0	0		0
_		70	90	100	100	100	100		90	0	NA		NA	NA	NA	NA	NA	100	0	0	0	0	64.62	0
4		70	90 I 00	100	100	100	80	80	90	0	NA	70	NA	NA	NA	NA	NA	0	0		NA	0	59.17	0
5		0	90	100	100	100	80	80	90	0	NA	10	NA	NA	NA	NA	NA	0	0	0	0	0	50	0
6	25.0. 200040.	70	90	100	100	100	70	90	70	0	NA	100	NA	NA	NA	NA	NA	0	0	-	NA	0	60	0
/	cslc: VC	0	80	70	70	70	80	80	80	0	NA	0	NA	NA	NA	NA	NA	0	0	_	NA	0	44.17	0
8	7.7 7	0	80	70	70	70	80	80	80	0	NA	0	NA	NA	NA	NA	NA	0	0	_	NA	0	44.17	0
21	cslc: Tb PWLW	0	0	0	0	0	0	0	0	0	NA	0	NA	NA	NA	NA	NA	0	0		NA	0	0	0
21	cslc: Tb clock gen	0	100	100	100	100	100		80	0	NA	0	NA	NA	NA	NA	NA	0	0	_	NA	0	55	0
	cslc: RF	70	90	100	100	100	100		100	0	NA		NA	NA	NA	NA	NA	0	0	_	NA	0	62.5	0
	cslc: Fifo	70	90	100	100	100	100	100		0	NA	90	NA	NA	NA	NA	NA	0	0	_	NA	0	65	0
11	cslc: Reg	0	90	100	100	100	80	70	80	0	NA	30	NA	NA	NA	NA	NA	0	0	_	NA	0	54.17	0
	cslc: Pipeline	0	70	100	100	100	0	0	0	0	0	0	NA	NA	NA	NA	NA	0	0	0	NA	0	28.46	0
13		100	NA	100	100	100	100	NA	100	0	0	100	NA	NA	NA	NA	NA	0	0	0	NA	0	54.55	0
	Cslc: CSL stmt/expr	0	30	80	50	NA	50	NA	80	0	0	50	NΑ	NA	NA	NA	NA	0	0		NA	0	30.91	0
	Cslc: CSL language	0	80	50	50	50	50	NA	50	0	0	0	NA	NA	NA	NA	NA	0	0	0	NA	0	27.5	0
	Cslc: CSL docgen	0	80	0	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	0	0	NA	0	13.33	0
17		0	0	100	100	0	100	NA	50	0	50	NA	NA	NA	NA	NA	NA	NA		NA	NA	0	50	0
18		0	0	100	100	0	50	NA	30	0	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	35	0
16	cslc: inst tree	0	NA	NA	NA	NA	NA	NA	65	0	25	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	30	0
	Cslc: CLI	0	NA	50	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	50	0
	Cslc: verilog PP	0	NA	80	NA	NA	NA	NA	NA	NA	NA	NA	NΑ	NA	NA	NA	NA	NA	NA	NA	NA	0	80	0
	Cslc: CSL PP	0	NA	50	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	50	0
15		0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	0	0
	Cslc: Top Level	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	0	0
	Cslc: cmd line args	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NΑ	NA		NA	NA	NA	NA	NA	NA	0	0	0
	cslc: Memory	0	80	0	0	0	0	10	60	0	0	0	NA			NA	0	0	0		NA		10.71	0
20	cslc: Buses	0	0	0	0	0	0	0	0	0	NA			NA		NA	0	0	0		NA		0	0
25	cslc: Procon	0	0	0	0	0	0	0	0	0	0	0		NA		_		0	0	-	NA		0	0
	cslc: Sched	0	0	0	0	0	0	0	0	0	NA	0		NA		_		0	0		NA		0	0
	cslc: Arbiter	0	0	0	0	0	0	0	0	0	0	0		_		NA		0	0		NA		0	0
	cslc: ASM	0	0	0	0	0	0	0	0	0	0	0	_	NA				0	0	0	0	0	0	0
	sw_lib: ASM	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	_	NA		NA		NA		NA			0	0
	sw_lib: Csim	0	NA	20	NA	NA	NA	NA	NA	NA	NA		_	NA		NA		NA		NA			20	0
	cslc: GUI	0	NA	0	NA	NA	NA	NA	NA	NA	NA		_	NA		NA		NA		NA			0	0
	clsc: cmd	0	NA	0	NA	NA	NA	NA	NA	NA	NA		_	NA		NA				NA			0	0
33	CSL pp: Aikido	0	NA	0	NA	NA	NA	NA	NA	NA	NA		_	NA		NA		_		NA			0	0
	HW: SOC bus ifc	0	NA	0	NA	NA	NA	NA	NA	NA	NA		_	NA		NA		_		NA			0	0
	HW: Processor ring	0	NA	0	NA	NA	NA	NA	NA	NA	NA		_	NA	-	NA	-	_		NA		NA	0	0
	HW: RISC	0	NA	0	NA	NA	NA	NA	NA	NA	NA		NΑ	NA	-	NA	-			NA		NA	0	0
	HW: ASP	0	NA	0	NA	NA	NA	NA	NA	NA	NA		NA	NA		NA	-			NA			0	0
	HW: MBIST	0	NA	0	NA	NA	NA	NA	NA	NA	NA			NA		NA				NA			0	0
	cslc: Reg v2	0	0	0	0	0	0	0	0	0	NA					NA		0	0		NA		0	0
. -	cslc: CSLOmNum v2	0	NA	0	0	0	0	0	0	0	0	0	NΑ	NA		NA		0	0		NA		0	0
21	cslc: Tb PWLW	0	0	0	0	0	0	0	0	0	NA	0	NΑ	NA		NA		0	0		NA		0	0
21	cslc: Tb stall gen	0	0	0	0	0	0	0	0	0	NA					NΑ		0	0		NA		0	0
21	cslc: Tb bubble gen	0	0	0	0	0	0	0	0	0	NA	0	NΑ	NA	NA	NA	NA	0	0	0	NA	0	0	0

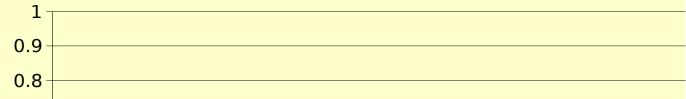
not started
under construction
under test
completed
intersection between row
Not applicable
Divider

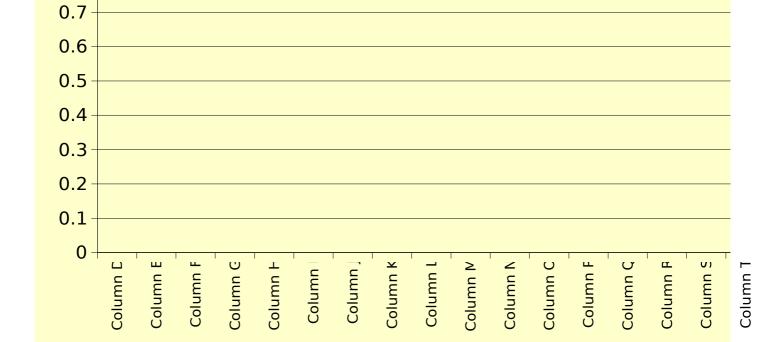
Priorities
Low priority
medium priority
high pri

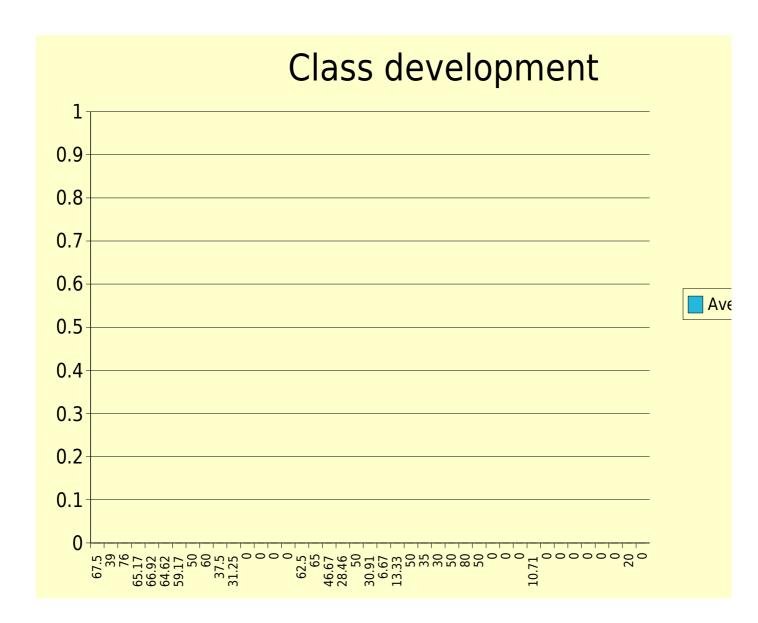
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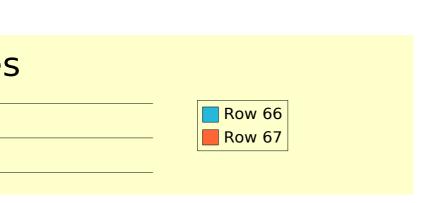


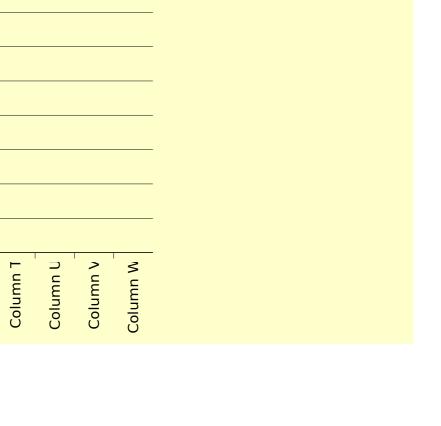
Development stage











erages prev week

	CSL CLASS	Tests passing %	Language syntax	lexer/misc	parser		tree walker	CSLOM cmd	СЅГОМ	CSLOM checker	CSLOM elab	Adaptor	СДОМ	CDOM checker	Verilog code gen	VHDL code gen	SystemC code gen	C++ code gen	document gen	CSIM codegen	CSLC ASM	IDE	Averages crt week	Averages prev week
	cslc: Verilog Parser	70	NA	90	90	0	90	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	_		NA	0	67.5	0
1 1	cslc: CDOM	60	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	90	5	90	0	10	NA	_		NA	0	39	0
14	cslc: CDOMNum	0	NA	100	100	NA	90	NA	NA	NA	NA	NA	90	0	NA	NA	NA	NA			NA	0	76	0
T	cslc: Interconn	70	90	98	98	98	98	95	95	10	NA		NA	NA	NA	NA	NA		10		NA	0	65.17	0
	cslc: Enum	70	90	100	100	100	100	80	100	0	NA		NA	NA	NA	NA NA	NA	100	0	0	0	0	66.92 64.62	0
	cslc: Field cslc: Memmap	70	90 90	100	100	100 100	80	80 80	90 90	0	NA NA		NA NA	NA NA	NA	NA	NA	100	0	0	0 NA	0	59.17	0
5		70 0	90	100	100		80	80	90	0	NA		NA		NA	NA	NA	0	0	0	0	0	50	0
6						100				0	NA		NA	NA	NA	NA	NA	-		-	-	_	60	
7	cslc: Decoder	70 0	90 80	100	100		70	90	70 80	0	NA		NA NA	NA NA	NA	NA	NA	0	0	0	NA	0	37.5	0
8		0	80	70 70	70	70	30	30	25	0	NA	0	NA	NA	NA	NA	NA	0	0	0	NA NA	0	31.25	0
21	cslc: Tb	0		0	70	70 0	0	0		0	NA	0	NA	NA	NA	NA	NA	0	0	0	NA	0	0	0
21	cslc: Tb PWLW	_	0	_			_		0	_	NA	0	NA	NA	NA	NA	NA		0	0		_		
	cslc: Tb clock gen	0	0	0	0	0	0	0	0	0	NA	0	NA	NA	NA	NA	NA	0	0	0	NA NA	0	0	0
21	cslc: Tb stall gell	0	0	0	0	0	0	0	0	0	NA	0	NA	NA	NA NA	NA NA	NA NA	0	0	0	NA	0	0	0
	cslc: RF	70	90	100	100	100	100	70	100	0	NA		NA	NA	NA	NA	NA	0	0	0	NA	0	62.5	0
	cslc: Ri	70	90	100	100	100	100	100		0	NA	90	NA	NA	NA	NA	NA	0	0	0	NA	0	65	0
11	cslc: Reg	0	60	100	100	100	50	70	50	0	NA	30	NA	NA	NA	NA	NA	0	0		NA	0	46.67	0
12	cslc: Reg	0	70	100	100	100	0	0	0	0	0	0	NA	NA	NA	NA	NA	0	0		NA	0	28.46	0
13	•	70	NA	100	100	100	100	NA	50	0	0	100	NA	NA	NA	NA	NA	0	0		NA	0	50	0
13	Cslc: CSL stmt/expr	0	30	80	50	NA	50	NA	80	0	0		NA	NA	NA	NA	NA	0	0	0	NA	0	30.91	0
	Cslc: CSL language	0	80	0	0	0	0	NA	0	0	0	0	NA	NA	NA	NA	NA	0	0	0	NA	0	6.67	0
	Cslc: CSL docgen	0	80	0	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	0	0	NA	0	13.33	0
17	cslc: csz docgen cslc: autoroute	0	0	100	100	0	100	NA	50	0	50	NA	NA	NA	NA	NA	NA	NA			NA	0	50	0
18		0	0	100	100	0	50	NA	30	0	0	NA	NA	NA	NA	NA	NA	NA	_		NA	0	35	0
16	2 2 2 2 2 2 2 2 P P 2	0	NA	NA	NA	NA	NA	NA	65	0	25	NA	NA	NA	NA	NA	NA	NA			NA	0	30	0
	Cslc: CLI	0	NA	50	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA			NA	0	50	0
	Cslc: verilog PP	0	NA	80	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA			NA	0	80	0
	Cslc: CSL PP	0	NA	50	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	_		NA	0	50	0
15	Cslc: CSL PP/regex	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA			NA	0	0	0
	Cslc: Top Level	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA		NA			NA	0	0	0
	Cslc: cmd line args	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA		NA		NA		NA	_		NA		0	0
24	cslc: Memory	0	80	0	0	0	0	10	60	0	0			NA		NA		0	0		NA	0	10.71	0
	cslc: Buses	0	0	0	0	0	0	0	0	0	NA			NA			0	0	0		NA	0	0	0
	cslc: Procon	0	0	0	0	0	0	0	0	0	0			NA		NA	0	0	0		NA	0	0	0
	cslc: Sched	0	0	0	0	0	0	0	0	0	NA			NA	NA	NA	0	0	0		NA	0	0	0
	cslc: Arbiter	0	0	0	0	0	0	0	0	0	0	0	NΑ	NA	NA	NΑ	0	0	0	0	NA	0	0	0
	cslc: ASM	0	0	0	0	0	0	0	0	0	0	0	NA	NA	NA	NA	0	0	0	0	0	0	0	0
29	sw_lib: ASM	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NΑ	NA	NA	NA	NA	NA	NΑ	NA	NA	0	0	0
30	sw_lib: Csim	0	NA	20	NA	NA	NA	NA	NA	NA	NA	NA	NΑ	NA	NA	NA	NA	NA	NA	NΑ	NA	0	20	0
31	cslc: GUI	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NΑ	NA	NA	NΑ	NA	NA	NA	NA	NA	0	0	0
	clsc: cmd	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	0	0
33	CSL pp: Aikido	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	0
	HW: SOC bus ifc	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	0
	HW: Processor ring	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	0
	HW: RISC	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	0
	HW: ASP	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	0
	HW: MBIST	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	0

not started
under construction
under test
completed
intersection between row
Not applicable

Divider

Priorities

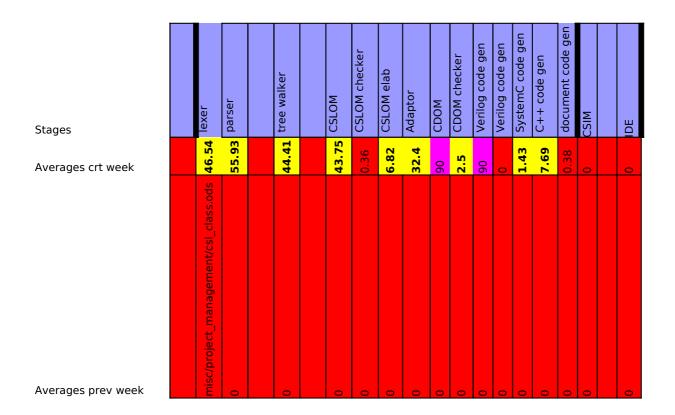
Low priority

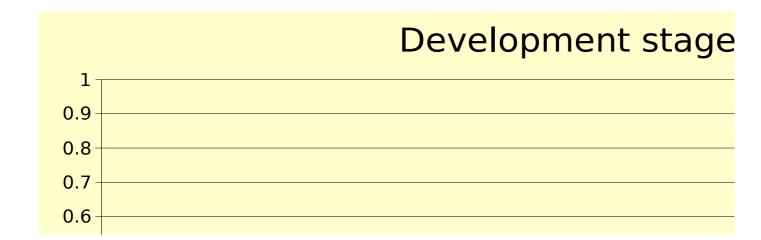
medium priority

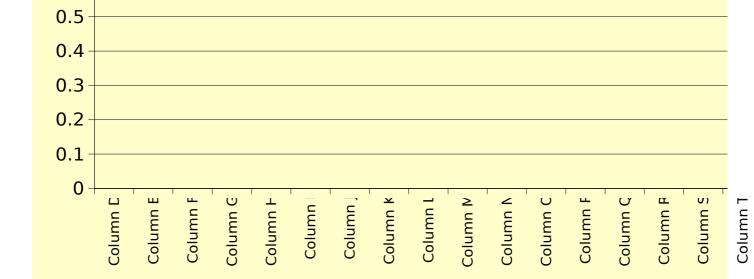
high pri

 $File\ name = csl_class.ods$

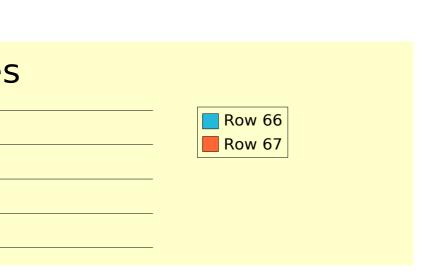
misc/project_management/csl_class.ods











Column T	
Column L	
Column V	
Column W	

erages prev week

	CSL CLASS	Tests passing %	Language syntax	lexer/misc	parser	Parser checks	tree walker	CSLOM cmd	CSLOM	CSLOM checker	CSLOM elab	Adaptor	СДОМ		Verilog code gen	VHDL code gen	SystemC code gen	C++ code gen	document gen	CSIM codegen	CSLC ASM	IDE	Averages crt week	Averages prev week
	cslc: Verilog Parser cslc: CDOM	70 60	NA NA	90	90 NA	0 NA	90 NA	NA NA	NA NA	NA NA	NA NA	NA NA	90	NA S	90	NA 0	10	NA NA	-		NA NA	0	67.5 39	NA NA
14	cslc: CDOM cslc: CDOMNum	0	NA	NA 100	100	NA	90	NA	NA	NA	NA	NA	90	0	NA	NA	NA	NA	_		NA	0	76	NA NA
1	cslc: Interconn	70	90	98	98	98	90 98	95	95	10	NA		NA	NA	NA	NA	NA	0	0		NA	0	64.33	0
2	cslc: Enum	70	90	100	100	100	100		100	0	NA		NA	NA	NA	NA	NA	100	0	0	0	0	66.92	0
	cslc: Field	70	90	100	100	100	100		90	0	NA		NA	NA	NA	NA	NA	100	0	0	0	0	64.62	0
	cslc: Memmap	70	90	100	100	100	80	80	90	0	NA		NA	NA	NA	NA	NA	0	0		NA	0	59.17	0
5		0	90	100	100	100	80	80	90	0	NA		NA	NA	NA	NA	NA	0	0	0	0	0	50	0
6		70	90	100			70	90	70	0	NA		NA	NA	NA	NA	NA	0	0	0	NA	0	60	0
7	cslc: VC	0	80	70	70	70	0	0	5	0	NA	0	NA	NA	NA	NA	NA	0	0	0	NA	0	24.58	0
8		0	80	70	70	70	30	30	25	0	NA	0	NA	NA	NA	NA	NA	0	0	0	NA	0	31.25	0
21	cslc: Tb PWLW	0	0	0	0	0	0	0	0	0	NA	0	NA	NA	NA	NΑ	NA	0	0	0	NA	0	0	0
21	cslc: Tb clock gen	0	0	0	0	0	0	0	0	0	NA	0	NA	NA	NA	NA	NA	0	0	0	NA	0	0	0
21	cslc: Tb stall gen	0	0	0	0	0	0	0	0	0	NA	0	NΑ	NA	NA	NΑ	NA	0	0	0	NA	0	0	0
	cslc: Tb bubble gen	0	0	0	0	0	0	0	0	0	NA	0	NA	NA	NA	NA	NA	0	0	0	NA	0	0	0
	cslc: RF	70	90	100	100	100	100	70	100	0	NA	90	NA	NA	NA	NA	NA	0	0	0	NA	0	62.5	0
	cslc: Fifo	70	90	100	100	100	100	100	100	0	NA	90	NA	NA	NA	NA	NA	0	0	0	NA	0	65	0
11	cslc: Reg	0	60	100	100	100	50	70	50	0	NA	30	NA	NA	NA	NA	NA	0	0	0	NA	0	46.67	0
	cslc: Pipeline	0	70	100	100	100	0	0	0	0	0	0	NA	NA	NA	NA	NA	0	0	0	NA	0	28.46	0
13	cslc: CSLOmNum	70	NA	100	100	100	100	NA	50	0	0	100	NΑ	NA	NA	NA	NA	0	0	0	NA	0	50	NA
	Cslc: CSL stmt/expr	0	30	80	50	NA	50	NA	80	0	0	50	NA	NA	NA	NA	NA	0	0	0	NA	0	30.91	0
	Cslc: CSL language	0	20	0	0	0	0	NA	0	0	0	0	NA	NA	NA	NA	NA	0	0	0	NA	0	1.67	0
	Cslc: CSL docgen	0	10	0	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	0	0	NA	0	1.67	0
17	cslc: autoroute	0	0	100	100	0	100	NA	50	0	50	NA	NA	NA	NA	NA	NA	NA	_		NA	0	50	0
18	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0	0	100	100	0	50	NA	30	0	0	NA	NA	NA	NA	NA	NA	NA	_		NA	0	35	NA
16		0	NA	NA	NA	NA	NA	NA	65	0	25	NA	NA	NA	NA	NA	NA	NA	_		NA	0	30	NA
	Cslc: CLI	0	NA	50	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	_		NA	0	50	NA
	Cslc: verilog PP	0	NA	80	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	_		NA	0	80	NA
1 -	Cslc: CSL PP	0	NA	50	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA			NA	0	50	NA
12	Cslc: CSL PP/regex	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA			NA	0	0	NA
	Cslc: Top Level	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA		NA	_	NA		0	0	NA
24	Cslc: cmd line args	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA		NA		NA		NA			NA		0	NA
	cslc: Memory cslc: Buses	0	0	0	0	0	0	10	60	0	0			NA		NA NA		0	0		NA		5	NA O
	cslc: Buses	0	0	0	0	0	0	0	0	0	NA 0			NA NA			0	0	0		NA NA	0	0	0
	cslc: Procon	0	0	0	0	0	0	0	0	0	NA						0	0	0		NA		0	0 NA
	cslc: Arbiter	0	0	0	0	0	0	0	0	0	0						0	0	0		NA		0	0
	cslc: ASM	0	0	0	0	0	0	0	0	0	0							0	0	0	0	0	0	0
	sw_lib: ASM	0	NA	0	NA	NA	NA	NA	NA	NA	NA			NA		NA		NA			NA		0	0
	sw_lib: Csim	0	NA	20	NA	NA	NA	NA	NA	NA	NA			NA		NA		NA	_		NA		20	0
	cslc: GUI	0	NA	0	NA	NA	NA	NA	NA	NA	NA								_		NA	_	0	NA
	clsc: cmd	0	NA	0	NA	NA	NA	NA	NA	NA	NA								_		NA		0	NA
	CSL pp: Aikido	0	NA	0	NA	NA	NA	NA	NA	NA	NA								_		NA		0	NA
	HW: SOC bus ifc	0	NA	0	NA	NA	NA	NA	NA	NA	NA								_		NA		0	NA
	HW: Processor ring	0	NA	0	NA	NA	NA	NA	NA	NA	NA								_		NA		0	NA
	HW: RISC	0	NA	0	NA	NA	NA	NA	NA	NA	NA								_		NA		0	NA
	HW: ASP	0	NA	0	NA	NA	NA	NA	NA	NA	NA			NA					_		NA		0	NA
	HW: MBIST	0	NA	0	NA	NA	NA	NA	NA	NA	NA			NA					_		NA		0	NA

not started
under construction
under test
completed
intersection between row
Not applicable

Divider

Priorities
Low priority
medium priority
high pri

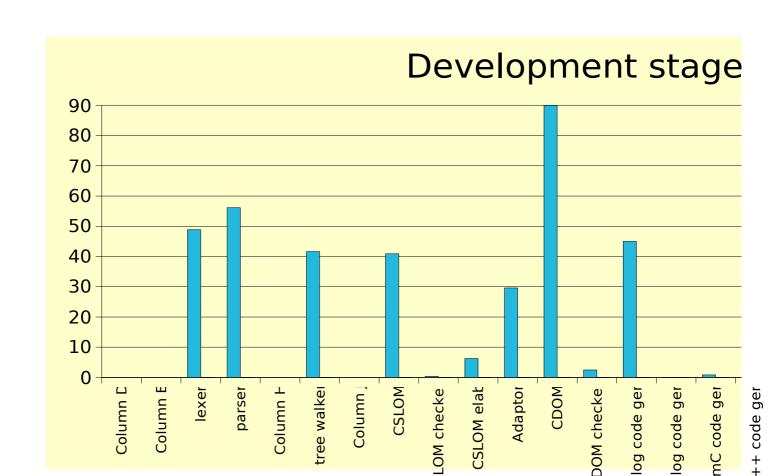
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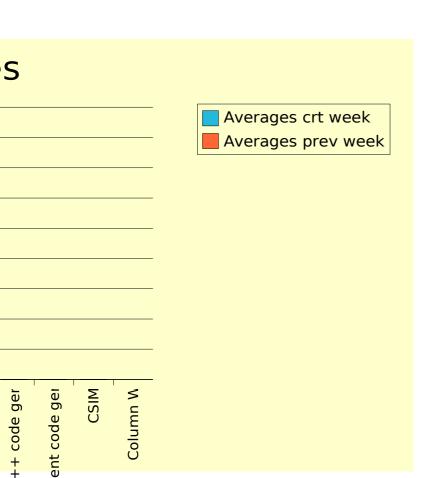
misc/project_management/csl_class.ods

lexer	parser	tree walker	CSLOM	CSLOM checker	CSLOM elab	Adaptor	СДОМ	CDOM checker	Verilog code gen	Verilog code gen	SystemC code gen	C++ code gen	document code gen	CSIM	IDE
46.54	55.93	44.41	41.07	0.36	6.82	32.4	06	2.5	06	0	1.43	69'.	0	0	0

Stages

Averages crt week Averages prev week





	CSL CLASS	Tests passing %	Language syntax	lexer/misc	parser	Parser checks	tree walker	CSLOM cmd	СЅГОМ	CSLOM checker	CSLOM elab	Adaptor	СДОМ	CDOM checker	Verilog code gen	VHDL code gen	SystemC code gen	C++ code gen	document gen	CSIM codegen	CSLC ASM	DE	Averages crt week	Averages prev week
	cslc: Verilog Parser	70	NA	90	90	0	90	NA	NA	NA	NA	NA	NA			NA	NA	NA	NA		NA	0	67.5	NA
	cslc: CDOM	60	NA	NA	NA		NA	NA	NA	NA	NA	NA	90	5	90	0	10	NA	NA	NA	NA	0	39	NA
14	cslc: CDOMNum	0	NA	100	100	NA	90	NA	NA	NA	NA	NA	90	0	0	0	0	NA	NA	NA	NA	0	47.5	NA
1	cslc: Interconn	70	90	98	98	98	98	95	95	10	NA	90	NA	NA	NA	NA	NA	0	0	0	NA	0	64.33	0
2	cslc: Enum	70	90	100	100	100	100	80	95	0	NA	100	NA	NA	NA	NA	NA	0	0	0	0	0	58.85	0
	cslc: Field	70	90	100	100	100	100	70	90	0	NA	80	NA	NA	NA	NA	NA	0	0	0	0	0	56.15	0
	cslc: Memmap	70	90	100	100	100	80	50	80	0	NA	60	NA	NA	NA	NA	NA	0	0	0	NA	0	55	0
	cslc: ISA	0	90	100	100	100	80	20	80	0	NA	10	NA	NA	NA	NA	NA	0	0	0	0	0	44.62	0
6	cslc: Decoder	70	90	100	100	100	70	70	70	0	NA	100	NA	NA	NA	NA	NA	0	0	0	NA	0	58.33	0
7	COICI VC	0	80	70	70	70	0	30	0	0	NA	0	NA	NA	NA	NA	NA	0	0	0	NA	0	26.67	0
	cslc: Tb	0	80	70	70	70	0	0	100	0	NA	0	NA	NA	NA	NA	NA	0	0	0	NA	0	32.5	0
	cslc: RF	70	90	100	100	100	100	70	100	0	NA	90	NA	NA	NA		NA	0	0	0	NA	0	62.5	0
	cslc: Fifo	70	90	100	100	100	100	100	100	0	NA	90	NA	NA	NA	NA	NA	0	0	0	NA	0	65	0
11	cslc: Reg	0	60	100	100	100	50	0	80	0	NA	20	NA	NA			NA	0	0	0	NA	0	42.5	0
12	cslc: Pipeline	0	70	100	100	100	0	0	0	0	0	0	NA	NA			NA	0	0	0	NA	0	28.46	0
13	cslc: CSLOmNum	70	NA	100	100	100	100	0	50	0	0		NA	NA			NA	0	0	0	NA	0	45.83	NA
	Cslc: CSL stmt/expr	0	0	0	0	0	0	0	0	0	0		NA	NA	NA		NA	0	0	0	NA	0	0	0
	Cslc: CSL docgen	0	0	0	0	0	0	0	0	0	0		NA	NA			NA	0	0	0	NA	0	0	0
	Cslc: CSL language	0	0	0	0	0	0	0	0	0	0	0	NA	NA			NA	0	0	0	NA	0	0	0
	cslc: autoroute	0	0	100	100	0	100	NA	50	0	50	NA	NA	NA				NA	NA		NA	0	50	0
18	cslc:automapper	0	0	100	100	0	50	NA	30	0	0		NA	NA				NA	NA		NA	0	35	NA
10	cslc: inst tree	0	NA	NA	NA	NA	NA	NA	65	0	25		NA	NA					NA		NA	0	30	NA
	Cslc: CLI	0	NA	50	NA	NA	NA	NA	NA	NA	NA		NA	NA							NA	0	50	NA
	Cslc: verilog PP	0	NA	80	NA	NA	NA	NA	NA	NA	NA		NA	NA					NA		NA	0	80	NA
1 5	Cslc: CSL PP/regex	0	NA	50	NA	NA	NA	NA	NA	NA	NA		NA	NA							NA	0	50	NA
	CSL pp: regex cslc: Bus ifc	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA					NA			0	###	NA
20		0	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA NA	NA		NA	0	0	0		NA	0	0	NA
21	cslc: Buses cslc: Clock gen	0	0	0	0	0	0	0	0	0	NA NA	0	NA NA	NA NA		NA NA	0	0	0	0	NA NA	0	0	0
	cslc: Clock gen	0	0	0	0	0	0	0	0	0	NA	0	NA	NA		NA	0	0	0	0	NA	0	0	NA
	cslc: Compare	0	0	0	0	0	0	0	0	0	NA		NA		NA			0	0	_	NA	0	0	NA
	cslc: Memory	0	0	0	0	0	0	10	60	0	0			NA	NA			0	0		NA	0	5	NA
	cslc: Procon	0	0	0	0	0	0	0	0	0	0			NA				0	0		NA	0	0	0
	cslc: Sched	0	0	0	0	0	0	0	0	0	NA				NA			0	0		NA	0	0	NA
	cslc: Sched	0	0	0	0	0	0	0	0	0	0				NA			0	0		NA	0	0	0
	cslc: ASM	0	0	0	0	0	0	0	0	0	0				NA			0	0	0	0	0	0	0
	sw_lib: ASM	0	NA	0	NA	NA	NA	NA	NA	NA	NA									NA		0	0	0
	sw lib: Csim	0	NA	0	NA	NA	NA	NA	NA	NA	NA									NA	-	0	0	0
	cslc: GUI	0	NA	0	NA	NA	NA	NA	NA	NA	NA									NA		0	0	NA
32	clsc: cmd	0	NA	0	NA	NA	NA	NA	NA	NA	NA			_						NA		0	0	NA
	CSL pp: Aikido	0	NA	0	NA	NA	NA	NA	NA	NA	NA			_						NA		NA	0	NA
	HW: Processor ring	0	NA	0	NA	NA	NA	NA	NA	NA	NA			_						NA		NA	0	NA
	HW: RISC	0	NA	0	NA	NA	NA	NA	NA	NA	NA			_						NA			0	NA
	HW: ASP	0	NA	0	NA	NA	NA	NA	NA	NA	NA		_	NA							_		0	NA

not started
under construction
under test
completed
intersection between row
Not applicable
Divider

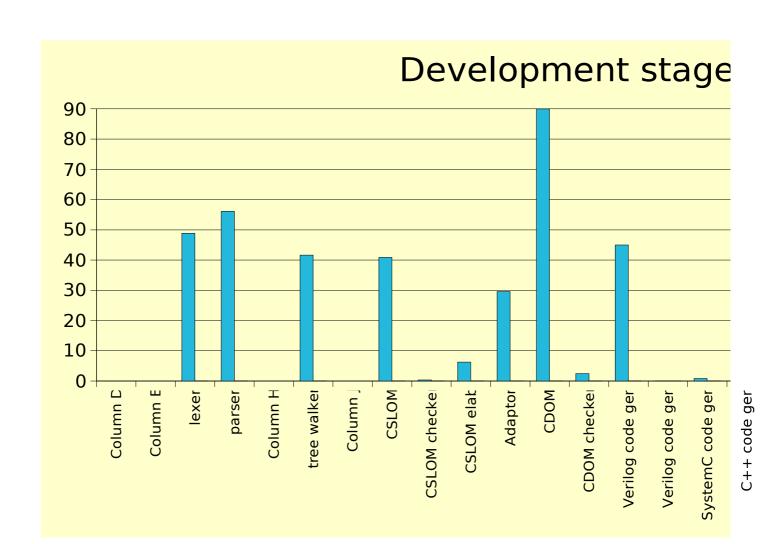
Priorities
Low priority
medium priority
high pri

File name = csl_class.ods misc/project_management/csl_class.ods

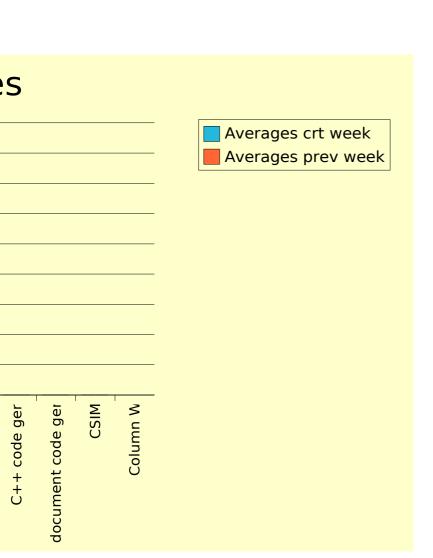
	lexer	parser	tree walker	CSLOM	CSLOM checker	CSLOM elab	Adaptor	СДОМ	CDOM checker	Verilog code gen	Verilog code gen	SystemC code gen	C++ code gen	document code gen	CSIM	IDE
	48.86	56.14	41.66	40.89	0.36	6.25	29.6	06	2.5	45	0	0.83	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Stages

Averages crt week Averages prev week









	CSL CLASS	Tests passing %	Language syntax	lexer/misc	parser	Parser checks	tree walker	CSLOM cmd	CSLOM	CSLOM checker	CSLOM elab	Adaptor	СДОМ	CDOM checker	Verilog code gen	VHDL code gen	C++ code gen	SystemC code gen	document gen	CSIM codegen	CSLC ASM	DE	Averages crt week	Averages prev week
	cslc: Verilog Parser	0	NA	90	90	0	90	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA	NA	67.5	42
	cslc: CDOM	0	NA	NA	NA		NA	NA	NA	NA	NA	NA	90	5	90	0	NA	NA	NA	NA	NA	NA	46.25	45
1	cslc: Interconn	0	90	98	98	98	98	95	95	10	NA	90	NΑ	NA	NA	NA	0	0	0	0	NA	0	59.38	46.33
2	cslc: Enum	0	90	100	100	100	100	80	95	0	NA	100	NA	NA	NA	NA	0	0	0	0	0	0	54.64	44.06
3	cslc: Field	0	90	100	100	100	100	70	90	0	NA	80	NA	NA	NA	NA	0	0	0	0	0	0	52.14	42.19
	cslc: Memmap	0	90	100	100	100	80	50	80	0	NA	60	NA	NA	NA	NA	0	0	0	0	NA	0	50.77	44.33
	cslc: ISA	0	90	100	100	100	80	20	80	0	0	10	NA	NA	NA	NA	0	0	0	0	0	0	38.67	24.41
	cslc: Decoder	0	90	100	100	100	70	70	70	0	NA	100	NA	NA	NA	NA	0	0	0	0	NA	0	53.85	44.17
7		0	60	70	70	70	0	30	0	0	NA	0	NA	NA	NA	NA	0	0	0	0	NA	0	23.08	25.33
8		0	60	70	70	70	0	0	100	0	NA	0	NA	NA	NA	NA	0	0	0	0	NA	0	28.46	27.33
9	cslc: RF	0	90	100	100	100	100	70	100	0	NA	90	NA	NA	NA	NA	0	0	0	0	NA	0	57.69	41.33
	cslc: Fifo	0	90	100	100	100	100	100	100	0	NA	90	NA	NA	NA		0	0	0	-	NA	0	60	47.33
11	cslc: Reg	0	60	100	100	100	50	0	80	0	NA	20	NA	NA	NA		0	0	0		NA	0	39.23	24
12	cslc: Pipeline	0	70	100	100	100	0	0	0	0	0	0	NA	NA		NA	0	0	0		NA	0	26.43	3.13
	cslc: CSLOmNum	0	NA	100	100	0	0	0	50	0	0		NA	NA	NA	_	0	0	0		NA	NA	26.92	10
	Cslc: CLI	0	NA	50	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA		NA	NA		NA	NA	50	10
	Cslc: verilog PP	0	NA	80	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA		NA	NA	-	NA	NA	80	10
	Cslc: CSL PP	0	NA	50	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA	_			NA	_	NA	50	10
	Cslc: CSL stmt/expr	0	0	0	0	0	0	0	0	0	0	0	NA	NA		NA	0	0	0		NA	0	0	3.13
14	cslc: CDOMNum	0	NA	100	100	NA	90	NA	NA	NA	NA	NA	90	0			_	NA	NA		NA	NA	76	54.29
	CSL pp: regex	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA					-	-	NA	NA	###	###
16	cslc: inst tree	0	NA	NA	NA	NA	NA	NA	65	0	25	NA	NA	NA		NA		0	0		NA	0	15	10.56
17	cslc: autoroute	0	NA	100	100	NA	100	NA	50	0	50	NA	NA	NA				_	NA		NA	0	66.67	39.44
18		_		100	100		50	NA	30	0	0	NA	NA				-				NA	NA	46.67	10
	cslc:automapper cslc: Bus ifc	0	NA	NA		NA	NA	NA		NA	NA	NA	NA	NA NA		NA NA		NA	NA	-	NA	NA	0	
	cslc: Bus lic	0	NA		NA	NA			NA								0	0	0		$\overline{}$		_	0
21		0	0	0	0	0	0	0	0	0	NA	0	NA	NA		NA	0	0	0		NA	NA	0	0
22	cslc: Clock gen	0	0	0	0	0	0	0	0	0	NA	0	NA	NA		NA	0	0	0		NA	0	0	0
	cslc: Compare	0	0	0	0	0	0	0	0	0	NA	0	NA	NA		NA	0	0	0		NA	NA	0	0
		0	0	0	0	0	0	0	0	0	NA	0	NA	NA		NA	0	0	0	-	NA	0	0 5	0
	cslc: Memory	0	0	0	0	0	0	10	60	0	0	0	NA	NA		NA	0	0	0		NA	0		0.33
	cslc: Procon	0	0	0	0	0	0	0	0	0	0		NA		NA		0	0	0		NA	0	0	0
	cslc: Sched	0	0	0	0	0	0	0	0	0	NA				NA		_	0	0		NA	0	0	0
	cslc: Arbiter	0	0	0	0	0	0	0	0	0	0		NA		NA			0	0	-	_	NA	0	0
	cslc: ASM	0	0	0	0	0	0	0	0	0	0		NA		NA			0	0	0	0	NA	0	0
	sw_lib: ASM	0	NA	0	NA	NA	NA	NA	NA	NA	NA						_			NA	-	NA	0	###
	sw_lib: Csim	0	NA	0	NA	NA	NA	NA	NA	NA	NA						-			NA	_	NA	0	###
3 L	cslc: GUI	0	NA	0	NA	NA	NA	NA	NA	NA	NA		_				_			NA		0	0	22
	clsc: cmd	0	NA	0	NA	NA	NA	NA	NA	NA	NA		_				_			NA		0	0	0
	CSL pp: Aikido	0	NA	0	NA	NA	NA	NA	NA	NA	NA						_			NA	_	NA	0	###
	HW: Processor ring	0	NA	0	NA	NA	NA	NA	NA	NA	NA						_			NA	-		0	10
	HW: RISC	0	NA	0	NA	NA	NA	NA	NA	NA	NA		_	NA			_			-	-		0	10
	HW: ASP	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	10

not started under construction under test completed Priorities
Low priority
medium priority
high pri

intersection between row

Not applicable

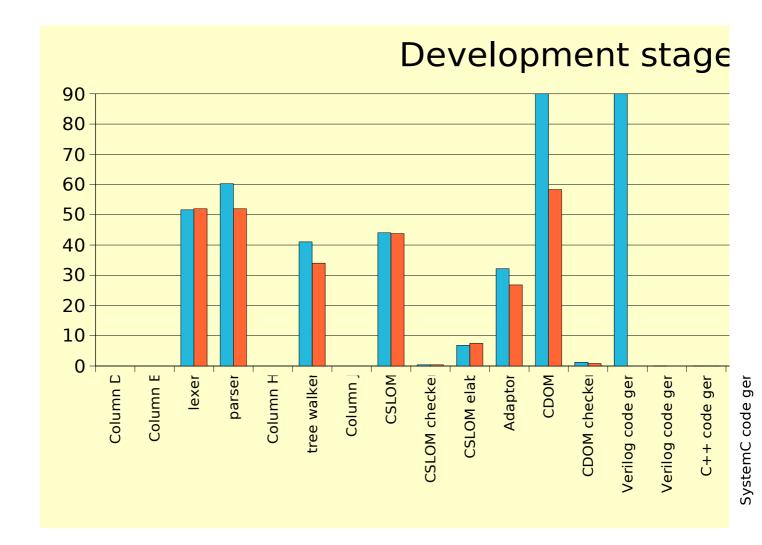
Divider

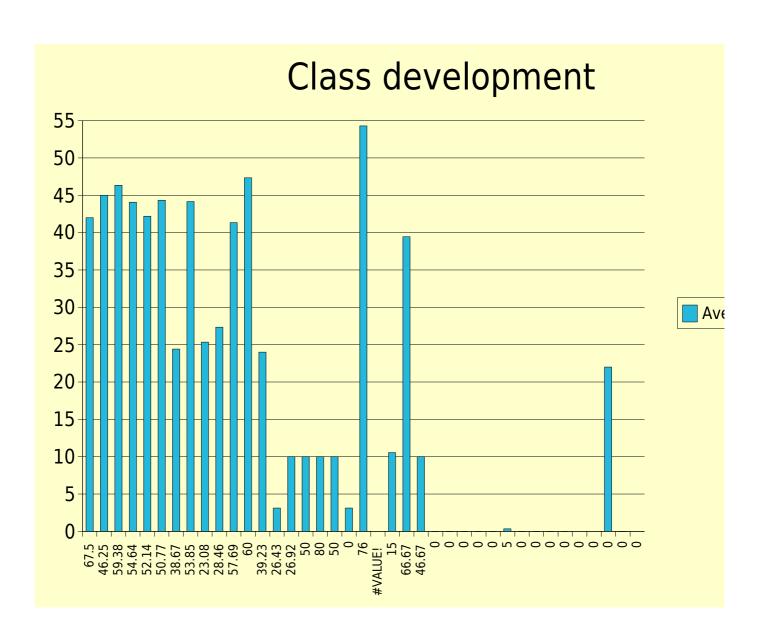
File name = csl_class.ods

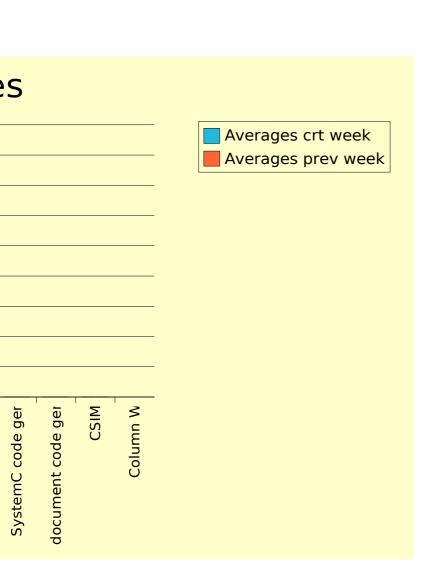
misc/project_management/csl_class.ods

Overall project average

Stages	lexer	parser	tree walker	CSLOM	CSLOM checker	CSLOM elab	Adaptor	СДОМ	CDOM checker	Verilog code gen	Verilog code gen	C++ code gen	SystemC code gen	document code gen	CSIM	IDE	
Averages crt week	51.66	60.3	41.04	44.04	0.38	6.82	32.17	06	1.25	06	0	0	0	0	0	0	
Averages prev week	52	52	34	43.8	0.4	7.5	26.82	58.33	0.83	#DIV/0!	#DIV/0!	0	0	0	0	1.52	









	CSL CLASS	IDE	cmd syntax	lexer	parser	Parser checks	Paraphrase	tree walker	CSLOM cmd	CSLOM	CSLOM checker	CSLOM elab	Adaptor	СДОМ	CDOM checker	Verilog code gen	C++ code gen	SystemC code gen	CSIM	CSLC ASM	document gen	Averages crt week	Averages prev week
	cslc: Verilog Parser	NA	NA	70	70	0	0	70	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NΑ	NA	NΑ	42	42
	cslc: CDOM	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	85	5	NA	NA	NA	NA	NA	NA	45	45
1	cslc: Interconn	0	90	90	95	80	0	90	60	90	10	NA	90	NA	NA	NA	0	0	0	NA	0	46.33	40.67
2	cslc: Enum	0	90	80	95	80	0	80	80	100	0	NA	100	NA	NA	NA	0	0	0	0	0	44.06	38.13
3	** * * * *	0	60	95	95	80	0	95	80	90	0	NA	80	NA	NA	NA	0	0	0	0	0	42.19	37.19
4	obiei i ioiiiiiap	0	80	95	95	80	0	95	95	85	0	NA	40	NA	NA	NA	0	0	0	NA	0	44.33	39
5	cslc: ISA	0	75	95	95	80	0	30	0	40	0	0	0	NA	NA	NA	0	0	0	0	0	24.41	19.71
6	cslc: Decoder	0	90	70	70	0	0	70	70	60	0	NA	100	NA	NA	NA	0	NA	NA	NA	NA	44.17	44.17
7	cslc: VC	0	60	95	95	80	0	0	0	50	0	NA	0	NA	NA	NA	0	0	0	NA	0	25.33	20
8	cslc: Tb	0	60	95	95	80	0	0	0	80	0	NA	0	NA	NA	NA	0	0	0	NA	0	27.33	22
9	cslc: RF	0	80	95	95	80	0	80	0	100	0	NA	90	NA	NA	NA	0	0	0	NA	0	41.33	36
10	cslc: Fifo	0	90	95	95	80	0	80	80	100	0	NA	90	NA	NA	NA	0	0	0	NA	0	47.33	42
11	cslc: Reg	0	30	95	95	80	0	0	0	60	0	NA	0	NA	NA	NA	0	0	0	NA	0	24	18.67
12	cslc: Pipeline	0	50	0	0	0	0	0	0	0	0	0	0	NA	NA	NA	0	0	0	NA	0	3.13	3.13
13	cslc: CSLOmNum	NA	NA	60	40		0	0	0	0	0	0	0	NΑ	NA	NA	0	NA	NΑ	NA	NΑ	10	10
14	cslc: CDOMNum	NA	NA	100	100		0	90	0	NA	NA	NA	NA	90	0	NA	NA	NA	NΑ	NA	NΑ	54.29	54.29
15	CSL pp: regex	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	NΑ	NA	NA	NA	NA	NΑ	NA	NΑ	###	###
16		5	NA	NA	NA		NA	NA	NA	65	0	25	NA	0	0	NA	NA	0	0	NA	0	10.56	10.56
17	cslc: autoroute	5	NA	70	70		0	70	NA	90	0	50	NA	NΑ	0	NA	NA	NΑ	NΑ	NA	NΑ	39.44	39.44
18	cslc:automapper	NA	NA	NA	NA		NA	NA	NA	80	0	0	NA	NA	NA	NA	NA	NA	NA	NA	NA		
19	cslc: Bus ifc	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	0	0	NA	0	0	0
	cslc: Buses	NA	0	0	0		0	0	0	0	0	NA	0	NA	NA	NA	0	0	0	NA	0	0	0
21	cslc: Clock gen	0	0	0	0		0	0	0	0	0	NA	0	NA	NA	NA	0	0	0	NA	0	0	0
22	cslc: Compare	NA	0	0	0		0	0	0	0	0	NA	0	NA	NA	NA	0	NΑ	NA	NA	NA	0	0
23	cslc: Counter	0	0	0	0		0	0	0	0	0	NA	0	NA	NA	NA	0	NA	NA	NA	NA	0	0
	cslc: Memory	0	0	0	0		0	0	0	5	0	0	0	NA	NA	NA	0	0	0	NA	0	0.33	0.33
25		0	NA	0	0		0	0	0	0	0	0	0	NA	NA	NA	0	0	0	NA	0	0	0
26	cslc: Sched	0	0	0	0		0	0	0	0	0	NA	0	NA	NA	NA	0	0	0	NA	0	0	0
27	cslc: Arbiter	NA	NA	0	0		0	0	0	0	0	0	0	NA	0	NA	0	NΑ	NΑ	NA	NA	0	0
28		NA	NA	0	0		0	0	0	0	0	0	0	NA	0	NA	0	NA	NA		NA	0	0
29		NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA		###	###
30		NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA		###	###
31	cslc: GUI	22	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA		22	22
32	clsc: Command shell	0	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA			NA	0	0
	CSL pp: Aikido	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA			###	###

not started

under construction

under test

completed

intersection between

Not applicable Divider

Priorities Low priority medium priority

high priority

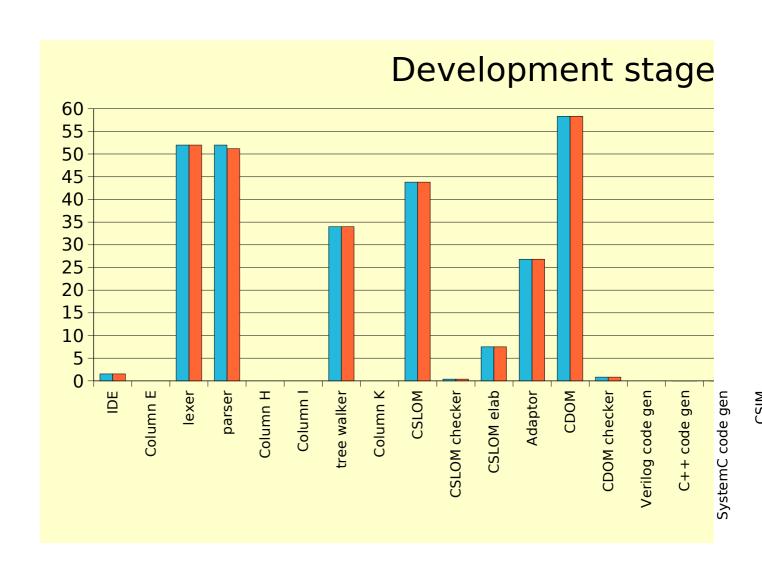
 $File\ name = csl_class.ods$ misc/project_management/csl_class.ods Overall project average

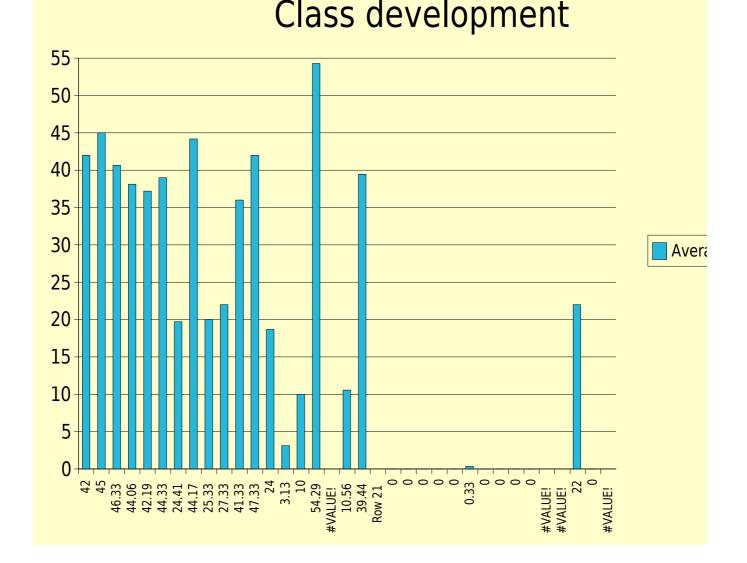
21.76

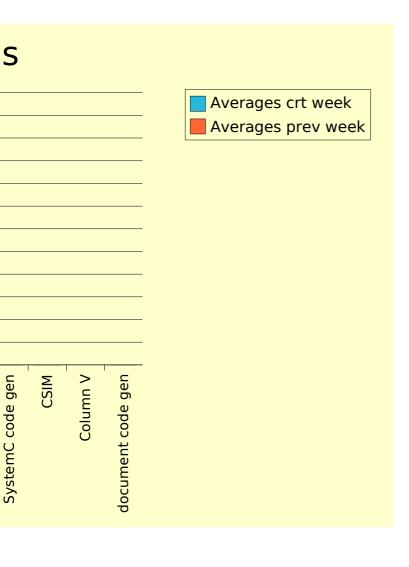
IDE	lexer parser	tree walker	CSLOM CSLOM checker	CSLOM elab Adaptor	CDOM CDOM checker	Verilog code gen C++ code gen	SystemC code gen	
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25

Stages









	CSL CLASS	IDE	cmd syntax	lexer	parser	Parser checks	Paraphrase	tree walker	CSLOM cmd	CSLOM	CSLOM checker	CSLOM elab	Adaptor	СДОМ	CDOM checker	Verilog code gen	C++ code gen	SystemC code gen	CSIM	CSLC ASM	document gen	Averages crt week	Averages prev week
	cslc: Verilog Parser	NA	NA	70	70	0	0	70	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	42	70
	cslc: CDOM	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	85	5	NA	NA	NA	NA	NA	NA	45	45
1	cslc: Interconn	0	90	90	90	0	0	90	60	90	10	NA	90	NA	NA	NA	0	0	0	NA	0	40.67	43.57
2	05101 2110111	0	90	80	80	0	0	80	80	100	0	NA	100		NA	NA	0	0	0	0	0	38.13	40
3		0	60	95	95	0	0	95	80	90	0	NA	80	NA	NA	NA	0	0	0	0	0	37.19	37
4	озгот тотттыр	0	80	95	95	0	0	95	95	85	0	NA	40	NA	NA	NA	0	0	0	NA	0	39	38.21
5	cslc: ISA	0	75	95	95	0	0	30	0	40	0	0	0	NA	NA	NA	0	0	0	0	0	19.71	18.44
6	cslc: Decoder	0	90	70	70	0	0	70	70	60	0	NA	100	NA	NA	NA	0	NA	NA	NA	NA	44.17	47.73
7	cslc: VC	0	60	95	95	0	0	0	0	50	0	NA	0	NA	NA	NA	0	0	0	NA	0	20	16.43
8	05:01 . 2	0	60	95	95	0	0	0	0	80	0	NA	0	NA	NA	NA	0	0	0	NA	0	22	13.21
9	CSICI TU	0	80	95	95	0	0	80	0	100	0	NA	90	NA	NA	NA	0	0	0	NA	0	36	37.86
10	cslc: Fifo	0	90	95	95	0	0	80	80	100	0	NA	90	NA	NA	NA	0	0	0	NA	0	42	43.57
11	cslc: Reg	0	30	95	95	0	0	0	0	60	0	NA	0	NA	NA	NA	0	0	0	NA	0	18.67	19.29
12	cslc: Pipeline	0	50	0	0	0	0	0	0	0	0	0	0	NA	NA	NA	0	0	0	NA	0	3.13	3.33
13	cslc: CSLOmNum	NA	NA	60	40		0	0	0	0	0	0	0	NA	NA	NA	0	NA	NA	NA	NA	10	10
14		NA	NA	100	100		0	90	0	NA	NA	NA	NA	90	0	NA	NA	NA	NA	NA	NA	54.29	54.29
15	CSL pp: regex	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	###	###
16		5	NA	NA	NA		NA	NA	NA	65	0	25	NA	0	0	NA	NA	0	0	NA	0	10.56	10.56
17	cslc: autoroute	5	NA	70	70		0	70	NA	90	0	50	NA	NΑ	0	NA	NA	NΑ	NA	NA	NΑ	39.44	39.44
18	cslc:automapper	NA	NA	NA	NA		NA	NA	NA	80	0	0	NA	NA	NA	NA	NA	NA	NA	NA	NA		
19	cslc: Bus ifc	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	0	0	NA	0	0	0
	cslc: Buses	NA	0	0	0		0	0	0	0	0	NA	0	NA	NA	NA	0	0	0	NA	0	0	0
21	cslc: Clock gen	0	0	0	0		0	0	0	0	0	NA	0	NA	NA	NA	0	0	0	NA	0	0	0
22	cslc: Compare	NA	0	0	0		0	0	0	0	0	NA	0	NA	NA	NA	0	NA	NA	NA	NΑ	0	0
23	cslc: Counter	0	0	0	0		0	0	0	0	0	NA	0	NA	NA	NA	0	NA	NA	NA	NA	0	0
	cslc: Memory	0	0	0	0		0	0	0	5	0	0	0	NA	NA	NA	0	0	0	NA	0	0.33	0.33
	cslc: Procon	0	NA	0	0		0	0	0	0	0	0	0	NA	NA	NA	0	0		NA	0	0	0
26		0	0	0	0		0	0	0	0	0	NA	0	NA	NA	NA	0	0		NA	0	0	0
27	cslc: Arbiter	NA	NA	0	0		0	0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA	NA	0	0
28		NA	NA	0	0		0	0	0	0	0	0	0	NA	0	NA	0	NA	NA		NA	0	0
29		NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA		###	###
30		NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA		###	###
31	cslc: GUI	22	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA		22	22
32		0	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA			NA	0	0
	CSL pp: Aikido	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA				###

not started

under construction

under test

intersection between

Not applicable Divider

Priorities Low priority

medium priority

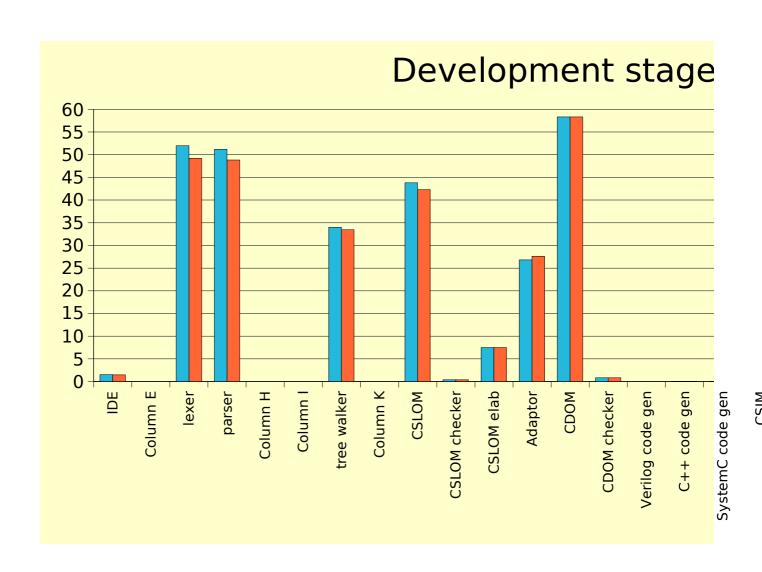
high priority

 $File\ name = csl_class.ods$ misc/project_management/csl_class.ods Overall project average

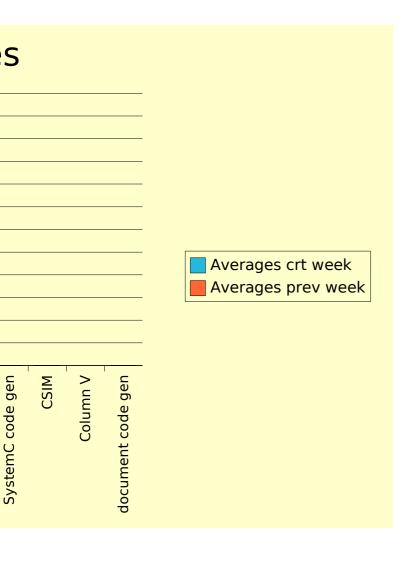
19.4

25

Stages









CSL CLASS	IDE	cmd syntax	lexer	parser	Paraphrase	tree walker	СSLOM ста	CSLOM	CSLOM checker	CSLOM elab	Adaptor	СБОМ	CDOM checker	Verilog code gen	C++ code gen	SystemC code gen	CSIM	CSLC ASM	document gen	Averages crt week	Averages prev week
cslc: Verilog Parser	NA	NA	70	70		70		NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	70	62
cslc: CDOM	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	85	5	NA	NA	NA	NA	NA	NA	45	35
cslc: GUI	22	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	22	22
clsc: Command shell	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	1.67
CSL pp: regex	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	###	25
CSL pp: Aikido	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	###	###
cslc: Arbiter	NA	NA	0	0	0	0	0	0	0	0	0	NA	0	NA	0		NA	NA	NA	0	0
cslc: ASM	NA	NA	0	0	0	0	0	0	0	0	0	NA	0	NA	0		NA	0	NA	0	0
cslc: inst tree	5	NA	NA	NA	NA	NA	NA	65	0	25	NA	0	0	NA	NA	0		NA	0	10.56	16.11
cslc: autoroute	5	NA	70	70	0	70	NA	90	0	50	NA	NA	0	NA	NA			NA	NA	39.44	41.82
cslc:automapper	NA	NA	NA	NA	NA	NA	NA	80	0	0	NA	NA	NA	NA	NA		NA		NA	0	
cslc: Bus ifc	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	0	0	0	NA	0	0	3.57
cslc: Buses	NA	0	0	0	0	0	0	0	0	NA	0	NA	NA	NA	0	0	0	NA	0	0	3.21 4.64
cslc: Clock gen cslc: CSLOmNum	0 NA	0 NA	60	0 40	0	0	0	0	0	NA 0	0	NA NA	NA NA	NA NA	0	0 NA	0 NA	NA NA	0	0 10	6.25
cslc: CDOMNum	NA	NA	100	100	0	90	0	NA	NA	NA	NA	90	0	NA	NA	NA		NA NA	NA NA	54.29	30
cslc: Compare	NA	0	0	0	0	0	0	0	0	NA	0	NA	NA	NA	0		NA	NA	NA	0	9.62
cslc: Compare	0	0	0	0	0	0	0	0	0	NA	0	NA	NA	NA	0		NA	NA	NA	0	15.36
cslc: Decoder	0	90	70	70	0	70	70	60	0	NA	95	NA	NA	NA	0		NA		NA	47.73	69.29
cslc: Enum	0	90	80	80	0	80	80	100	0	NA	90	NA	NA	NA	0	0	0	0	0	40	46
cslc: Field	0	60	90	90	0	75	80	90	0	NA	70	NA	NA	NA	0	0	0	0	0	37	44.64
cslc: Fifo	0	90	90	90	0	80	80	100	0	NA	80	NA	NA	NA	0	0	0	NA	0	43.57	48.07
cslc: Interconn	0	90	90	90	0	90	60	90	10	NA	90	NA	NA	NA	0	0	0	NA	0	43.57	61
cslc: ISA	0	75	90	90	0	0	0	40	0	0	0	NA	NA	NA	0	0	0	0	0	18.44	35
cslc: Memmap	0	80	80	90	0	75	95	85	0	NA	30	NA	NA	NA	0	0	0	NA	0	38.21	33.82
cslc: Memory	0	0	0	0	0	0	0	5	0	0	0	NA	NA	NA	0	0	0	NA	0	0.33	6.56
cslc: Pipeline	0	50	0	0	0	0	0	0	0	0	0	NA	NA	NA	0	0	0	NA	0	3.33	11.67
cslc: Procon	0	NA	0	0	0	0	0	0	0	0	0	NA	NA	NA	0	0	0	NA	0	0	6.92
cslc: Reg	0	30	90	90	0	0	0	60	0	NA	0	NA	NA	NA	0	0	0	NA	0	19.29	21.07
cslc: RF	0	80	90	90	0	80	0	100	0	NA	90	NA	NA	NA	0	0	0	NA	0	37.86	46.14
cslc: Sched	0	0	0	0	0	0	0	0	0	NA	0			NA		0		NA	0	0	9.79
cslc: Tb	0	60	60	60	0	0	0	5	0	NA	0	NA	NA	NA	0	0		NA	0	13.21	11.85
cslc: Unit	0	NA	90	90	0	90	0	80	0	NA			NA	NA	0	0		NA	0	33.85	58.62
cslc: VC	0	60	60	60	0	0	0	50	0	NA	0	NA	NA	NA		0		NA	0	16.43	23.57
sw_lib: ASM	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA NA			NA			###	0
sw_lib: Csim	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA			NA NA	_					###	0
hw_lib:Memcntl hw_lib: micro eng	NA NA	NA NA	NA NA	NA NA	NA NA	NA NA	NA NA	NA NA	NA NA	NA NA	NA NA									###	3.33 6.67
hw lib: Proc. Ring	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	_		NA		_					###	5.83
hw_lib: PSCQN	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA			NA							###	27.33
nw_nb. racqn	IVA	IVA	INA	IVA	IVA	IVA	IVA	IVA	IVA	IVA	INA	INA	IVA	INA	IVA	NA	NA	IVA	IVA	###	27.33

not started under construction under test completed intersection between r

Not applicable

Divider

Priorities Low priority medium priority high priority

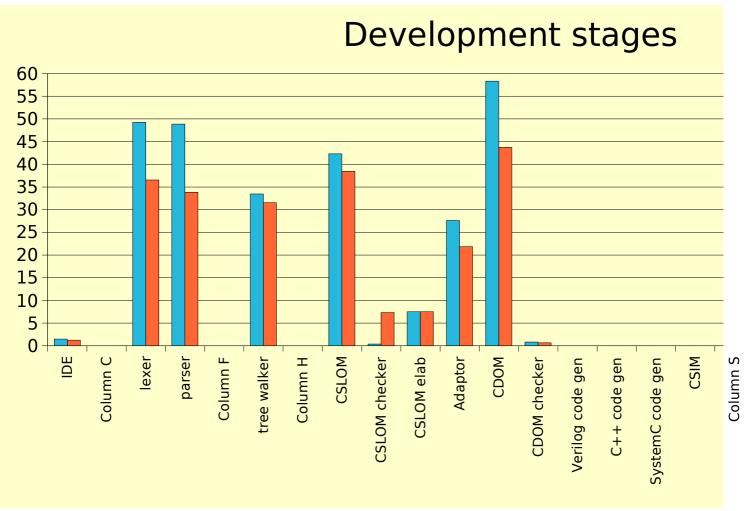
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Overall project average

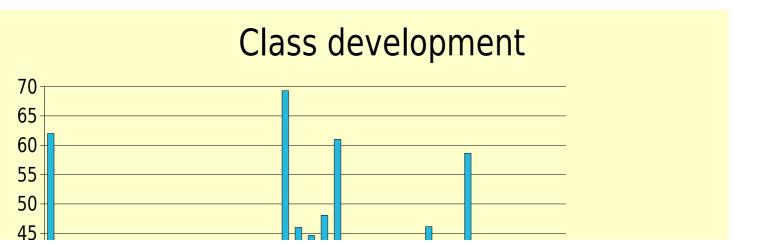
19.57

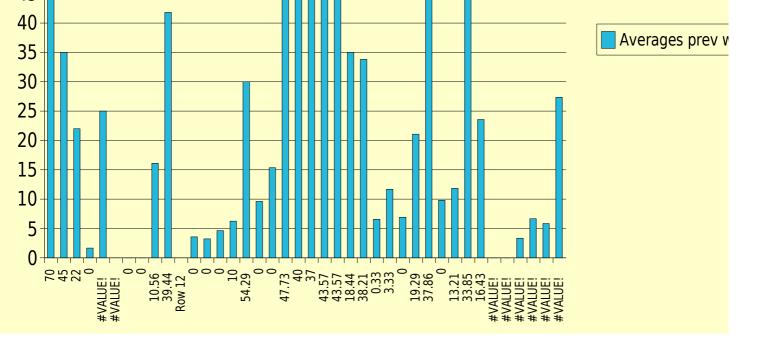
 $File\ name = csl_class.ods$ misc/project_management/csl_class.ods

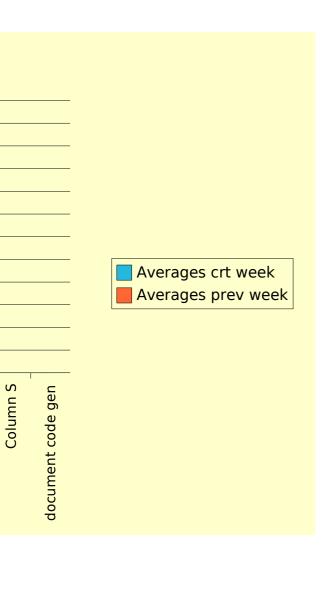




document code gen









APA cslc: CDOM NA 25 25 NA	A NA NA NA NA NA A NA NA NA NA NA NA NA
CP	A NA NA NA NA NA A NA NA NA NA NA NA NA
Signature Sign	A NA NA NA NA NA A O NA NA NA NA A O NA NA NA NA A NA NA NA NA NA
BZ CSL pp: regex 25 NA	A NA NA NA NA NA A O NA NA NA NA O NA NA NA NA A NA NA NA NA
APA cslc:Adaptor 55 55 55 55 NA	A NA NA NA NA NA A NA NA NA NA NA A NA NA NA NA NA A O NA NA NA NA O NA NA NA NA A NA NA NA NA
APA cslc:Adaptor library NA NA </td <td>A NA NA NA NA NA A NA NA NA NA NA A O NA NA NA NA O NA NA NA NA A NA NA NA NA</td>	A NA NA NA NA NA A NA NA NA NA NA A O NA NA NA NA O NA NA NA NA A NA NA NA NA
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BZ cslc: Arbiter 0 NA NA 0 0 NA	A O NA NA NA NA O NA NA NA NA A NA NA NA NA
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APO cslc: CDOMNum 0 0 NA 0 0 NA NA 0 Image: Control of the control o	A O NA NA NA NA
OS 2 cslc: Compare 50 0 0 25 50 NA NA NA NA 0 0 0 0 0 NA 0 NA 0 0 0 0 0 NA 0 0 0 0 0 0 NA 0<	0 NA NA NA NA
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APA 1 cslc: Decoder 90 90 100 25 0 NA NA NA 0 OS 90 100 100 100 NA 95 NA NA NA NA 0 AB 90 80 80 80 100 NA 0 NA NA NA NA NA NA 0 AB 90 80 80 80 100 NA 0 NA	
BZ cslc: Enum 90 0 50 40 NA NA 0 AB 90 80 80 100 0 NA 0 SP cslc: Field 10 90 75 50 80 NA NA NA 0 GD x 50 50 80 90 NA 0 0 NA 0 NA 0 0 NA 0 NA 0 0 0 0 NA 0 <td></td>	
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BZ 1 cslc: Interconn 80 70 70 50 5 NA NA NA 0 GD 90 </td <td></td>	
SP 1 cslc: ISA 90 85 85 60 90 NA NA 0 AB 75 0	
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BZ 2 cslc: Memory BZ 2 cslc: Pipeline 70 0 50 5 NA	
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	. January IVA
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25

not started light red
under construction under test light magenta
completed green
intersection between r
Not applicable dark violet
Divider light red
yellow
grelow
light magenta
green
light blue
dark violet
black

Priorities

Low priority medium priority high priority

orange 4 violet red

File name = csl_class.ods misc/project_management/csl_class.ods

Stages	documented: Syntax	documented: data structures	documented: algorithms	documented: hw circuits	coded: CSL proto C++ lib	coded: Verilog library	coded: CSIM	coded: Command shell	coded: IDE		coded: lexer	coded: parser	coded: tree walker	coded: CSLOM	coded: CSLOM checker	coded: CSLOM elab	coded: Adaptor	coded: CDOM	coded: CDOM checker	coded: Verilog code gen	VHDL	coded: C++ code gen	coded: SystemC code gen
Averages crt week	51.4	18.33	16.67	39.58	19.39	0	#DIV/0i	0	1.23		36.54	33.85	31.54	38.46	7.31	7.5	21.85	43.75	0.65	#DIV/0!	#DIV/0i	0	#DIN/0i
Averages prev week	51.26	18.18	16.52	39.58	16.65	0	#DIV/0!	0	1.23		32.31	29.62	27.31	38.65	7.31	7.5	21.48	43.75	0.65	#DIV/0!	#DIV/0!	0	#DIN/0i

coded: document code gen	uses CSLOM: CSL Info class	uses CSLOM: CSL Unit	uses CSLOM: Arbiter	uses CSLOM: Asembler	uses CSLOM: Bus ifc	uses CSLOM: Buses	uses CSLOM: Clock	uses CSLOM: Compare	uses CSLOM: Counter	uses CSLOM: Csim	uses CSLOM: Decoder	uses CSLOM: Event	uses CSLOM: FF	uses CSLOM: Isa	uses CSLOM: Mem location	uses CSLOM: Mem map	uses CSLOM: Memory	uses CSLOM: pattern_gen	uses CSLOM: Pipeline	uses CSLOM: Scheduler	uses CSLOM: State	uses CSLOM: Unit	uses CSLOM: VC	uses cslc Compiler	uses libcslc.o	uses CSL Library		CSL C++ prototype lib owner	priority	
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CSL CLASS	Averages crt w	Averages prev	week
cslc: Verilog Parser	62	62	
cslc: CDOM	35	35	
cslc: GUI	22	22	
clsc: Command shell	1.67	1.67	
CSL pp: regex	25	25	
cslc:Adaptor	55	50	
cslc:Adaptor library	90	90	
CSL pp: Aikido	#DIV/0!	#DIV/0!	
cslc: Arbiter	0	0	
cslc: inst tree	16.11	16.11	l
cslc: autoroute	41.82	41.82	
cslc: Bus ifc	3.57	3.57	l
cslc: Buses	3.21	3.21	
cslc: Clock gen	4.64	4.64	
cslc: CSLOmNum	6.25	6.25	
cslc: CDOMNum	30	30	
cslc: Compare	9.62	6.15	
cslc: Counter	15.36	12.5	
cslc: Decoder	69.29	67.5	
cslc: Enum	46	46	
cslc: Field	44.64	35	
cslc: Fifo	48.07	41.73	
cslc: Interconn	61	61	
cslc: ISA	35	34.67	
cslc: Memmap	33.82	32.94	
cslc: Memory	6.56	6.56	
cslc: Pipeline	11.67	11.67	
cslc: Procon	6.92	6.92	
cslc: Reg	21.07	21.07	
cslc: RF	46.14	39	
cslc: Sched	9.79	9.79	
cslc: Tb	11.85	11.85	
cslc: Unit	58.62	58.62	
cslc: VC	23.57	25.71	ı
sw_lib: ASM	0	0	
sw_lib: Csim	0	0	
hw_lib:Memcntl	3.33	3.33	
hw_lib: micro eng	6.67	6.67	
hw_lib: Proc. Ring	5.83	5.83	
hw_lib: PSCQN	27.33	27.33	
STATUS LEGEND but b	ercentages in t	he hoves	

not started
under construction
under test
completed
intersection between

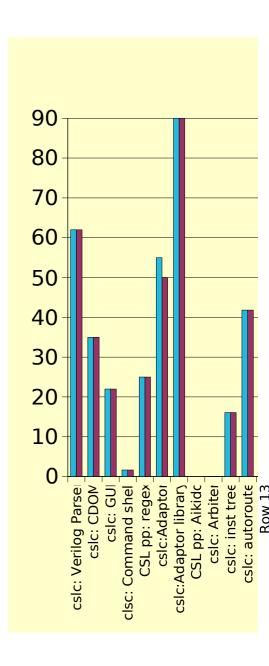
Overall project average

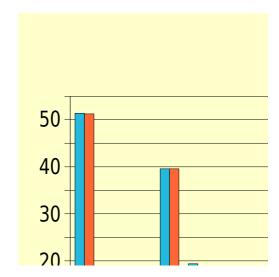
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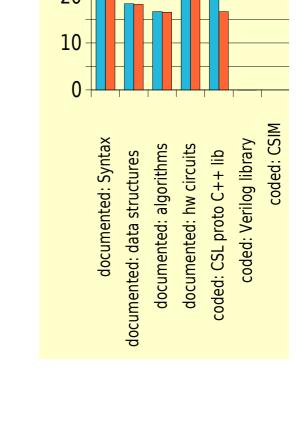
Priorities
Low priority
medium priority
high priority

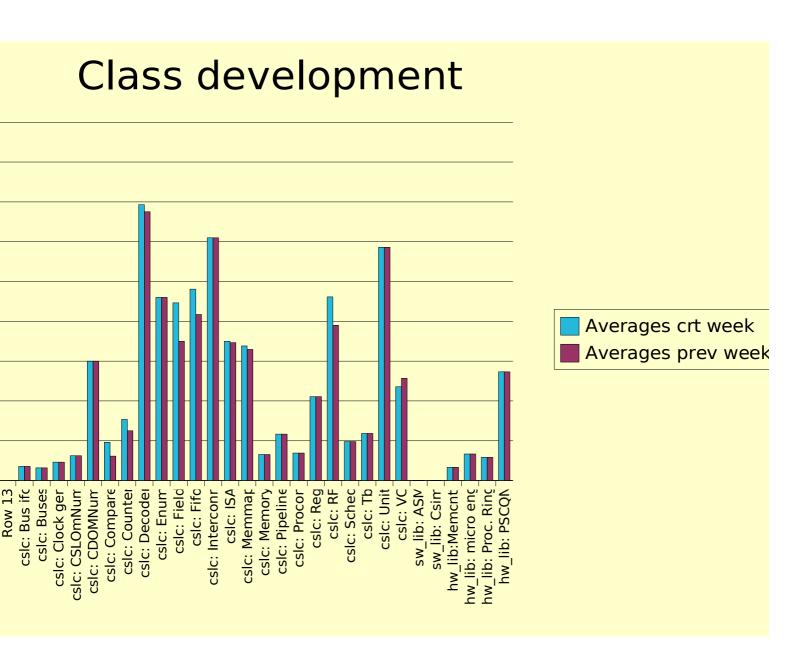
Not applicable Divider

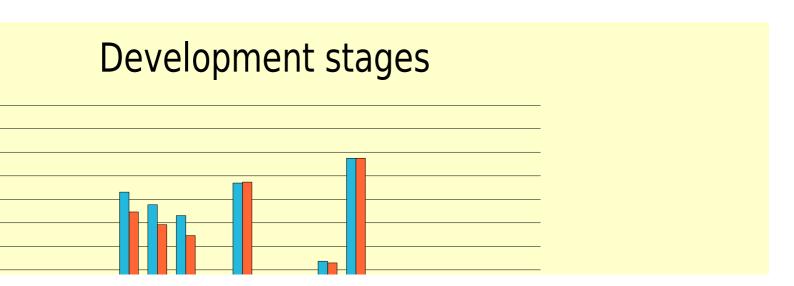
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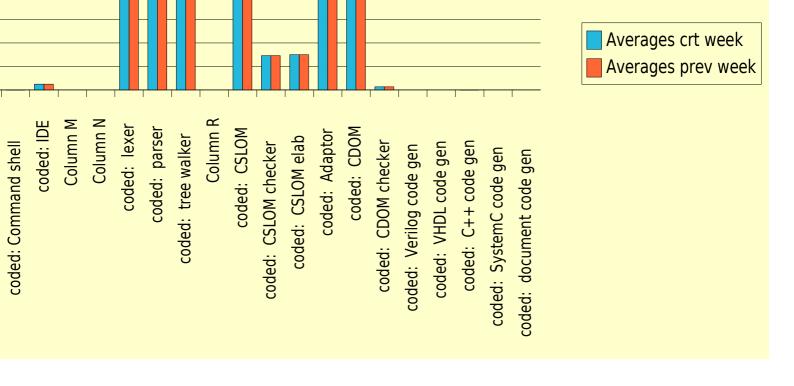
















cslc owner	cslc owner	CSL CLASS	documented: Syntax	documented: data structures	documented: algorithms	documented: hw circuits	coded: CSL proto C++ lib	coded: Verilog library	coded: CSIM	coded: Command shell	coded: IDE	L-P-Tw Owner	complete: cmd summary syntax	coded: lexer	coded: parser	coded: tree walker	coded: CSLOM cmd	coded: CSLOM	coded: CSLOM checker	coded: CSLOM elab	coded: Adaptor	coded: CDOM	coded: CDOM checker	coded: Verilog code gen		C++ code gen	coded: SystemC code gen
NA		cslc: Verilog Parser	100	NA	NA	NA	NA	NA	NA	NA	NA	0		70	70	70		NA	NA	NA	NA	NA	NA	NA	NA	NA I	NA
APA		cslc: CDOM	NA	25	25	NA	NA	NA		NA	NA			NA	NA	NA	NA	NA	NA	NA	NA	85	5	NA	NA	NA	NA
CP		cslc: GUI	NA	NA	NA	NA	NA	NA		NA	22			NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA I	NA
OS		clsc: Command shell	5	NA	NA	NA	NA	NA		0	0			NA	NA	NA	NA	NA	NA	NA	NA	NA		NA	NA	NA I	NA
BZ		CSL pp: regex	25	NA	NA	NA	NA	NA		NA	NA			NA	NA	NA	NA	NA	NA	NA	NA	NA		NA		_	NA
APA		cslc:Adaptor	50	50	50	NA	NA	NA		NA	NA			NA	NA	NA	NA	NA	NA	NA	50	NA		NA	NA	_	NA
APA		cslc:Adaptor library	NA	NA	NA	NA	NA	NA		NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	90	NA		NA		NAI	
OS DZ		CSL pp: Aikido	NA	NA	NA	NA	NA	NA		NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA	NA		NA
BZ		cslc: Arbiter	0	NA	NA	0	0	NA		NA	NA 5		NA	0	0	0	0	0 65	0	25	0	NA	0	NA		NA I	
BZ BZ	_	cslc: inst tree	NA 70	25 25	25 25	NA	NA 0	NA NA		NA NA	5		NA	70	70	70		7 5	0	50	0	0	0	NA		NA I	
BZ		cslc: autoroute cslc: Bus ifc	70 25	0	0	NA 25	0	NA		NA	0		NA 0	0	0	0		0	0	NA	NA 0	NA NA	NA 0	NA NA	NA NA		NA NA
BZ BZ		cslc: Buses	20	0	0	25	0	NA		NA	0		0	0	0	0		0	0	NA	0	NA	0	NA	NA NA		NA
BZ	2	cslc: Clock gen	40	0	0	25	0	NA		NA	0		0	0	0	0		0	0	NA	0	NA		NA			NA
APO		cslc: CSLOmNum	0	0	0	NA	0		NA	NA	0		0	60	40	0		0	0	0	0	0	0	NA	NA		NA
APO		cslc: CDOMNum	0	0	0	NA	0	-	NA	NA	0		100	100	100	90		0	0	0	0	90	0	NA	NA		NA
OS	2	cslc: Compare	50	0	0	25	5	NA		NA	NA		0	0	0	0		0	0	NA	0	NA	0	NA	NA		NA
OS	_	cslc: Counter	90	50	0	25	10	NA		NA	0		0	0	0	0		0	0	NA	0	NA	0	NA	NA	NA	NA
APA	1	cslc: Decoder	90	90	100	25	0	NA	NA	NA	0	OS	90	100	100	100		60	100	NA	90	NA	0	NA	NA	NA	NA
BZ		cslc: Enum	90	0	0	50	40	NA	NA	NA	0	AB	90	80	80	80	80	100	0	NA	0	NA	0	NA	NA	NA	NA
SP		cslc: Field	10	90	75	50	80	NA	NA	NA	0	GD	50	0	0	0	80	90	0	NA	0	NA	0	NA	NA	NA	NA
OS	3	cslc: Fifo	75	0	0	55	1	NA	NA	NA	0	OS	90	50	50	50	80	95	0	NA	80	NA	0	NA	NA	NA	NA
BZ	1	cslc: Interconn	80	70	70	50	5	NA	NA	NA	0	GD	90	90	90	90		90	90	0	90	NA	10	NA	NA	NA	NA
SP	1	cslc: ISA	90	85	85	60	90	NA	NA	NA	0	AB	70	0	0	0		40	0	0	0	NA	0	NA	NA	NA I	NA
AB	_	cslc: Memmap	70	0	0	50	90	NA		NA	0	GD	80	80	30	20	70	70	0	0	0	NA	0	NA	NA	0 1	NA
BZ		cslc: Memory	50	0	0	50	0	NA	NA	NA	0		0	0	0	0		5	0	0	0	NA		NA		_	NA
BZ		cslc: Pipeline	70	0	0	50		NA			0	OS	50	0	0	0		0	0	0		NA				NA I	
OS	?	cslc: Procon	83	0	0	NA				NA	0		NA		0	0		0	0	NA		NA			-	NA I	
OS		cslc: Reg	85	0	0					NA		GD	30	0	0	0		60	0	NA		NA			_	NA I	
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BZ OS		cslc: Sched cslc: Tb	87 89	0	0	50				NA NA	0	AB	0	0	0	0		5	0	NA		NA NA				I AN	
BZ		cslc: Tb	90	90		50				NA	0	AD	60 NA		90	90		80	0	NA NA		NA			-	NA I	
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03		sw lib: ASM	0	0	0	NA				NA		03	00	NA	NA	NA		NA	NA	NA						NA I	
		sw_lib: Csim	0	0	0	NA				NA				NA	NA	NA		NA	NA	NA					-	NAI	
CL		hw_lib:Memcntl	0	0	0	20	0			NA				NA	NA	NA		NA	NA	NA					-	NA I	
CL		hw lib: micro eng	0	0	0	40				NA				NA	NA	NA		NA	NA	NA					-	NA I	
AV		hw_lib: Proc. Ring	0	0	0	35					NA			NA	NA	NA		NA	NA	NA					-	NA I	
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not started
under construction
under test
completed
intersection between r
Not applicable
Divider

light red yellow light magenta green light blue dark violet black

Priorities
Low priori

Low priority medium priority high priority orange 4 violet red

File name = csl_class.ods misc/project_management/csl_class.ods 25

Stages	documented: Syntax	documented: data structures	documented: algorithms	documented: hw circuits	coded: CSL proto C++ lib	coded: Verilog library	coded: CSIM	coded: Command shell	coded: IDE		coded: lexer	coded: parser	coded: tree walker	coded: CSLOM	coded: CSLOM checker	coded: CSLOM elab	coded: Adaptor	coded: CDOM	coded: CDOM checker	coded: Verilog code gen	coded: VHDL code gen	coded: C++ code gen	coded: SystemC code gen
Averages crt week	51.26	18.18	16.52	39.58	16.65	0	#DIV/0!	0	1.23		32.31	29.62	27.31	38.65	7.31	7.5	21.48	43.75	0.65	#DIV/0!	#DIV/0!	0	#DIV/0!
Averages prev week	50.97	18.18	16.52	39.58	16.65	0	#DIV/0!	0	1.23		26.54	25.77	23.46	37.88	7.31	7.5	20.93	43.75	99.0	#DIV/0!	#DIV/0!	0	#DIV/0!

coded: document code gen	uses CSLOM: CSL Info class	uses CSLOM: CSL Unit	uses CSLOM: Arbiter	uses CSLOM: Asembler	uses CSLOM: Bus ifc	uses CSLOM: Buses	uses CSLOM: Clock	uses CSLOM: Compare	uses CSLOM: Counter	uses CSLOM: Csim	uses CSLOM: Decoder	uses CSLOM: Event	uses CSLOM: FF	uses CSLOM: Isa	uses CSLOM: Mem location	uses CSLOM: Mem map	uses CSLOM: Memory	uses CSLOM: pattern_gen	uses CSLOM: Pipeline	uses CSLOM: Scheduler	uses CSLOM: State	uses CSLOM: Unit	uses CSLOM: VC	uses cslc Compiler	uses libcslc.o	uses CSL Library		CSL C++ prototype lib owner	priority	
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CSL CLASS	Averages crt w	Averages prev	week
cslc: Verilog Parser	62	62	
cslc: CDOM	35	35	
cslc: GUI	22	22	
clsc: Command shell	1.67	1.67	
CSL pp: regex	25	25	
cslc:Adaptor	50	48.75	
cslc:Adaptor library	90	90	
CSL pp: Aikido	#DIV/0!	#DIV/0!	
cslc: Arbiter	0	0	
cslc: inst tree	16.11	16.11	
cslc: autoroute	41.82	41.82	
cslc: Bus ifc	3.57	3.57	
cslc: Buses	3.21	3.21	
cslc: Clock gen	4.64	4.64	
cslc: CSLOmNum	6.25	6.25	
cslc: CDOMNum	30	30	
cslc: Compare	6.15	6.15	
cslc: Counter	12.5	12.5	
cslc: Decoder	67.5	67.5	
cslc: Enum	46	25.71	
cslc: Field	35	31.07	
cslc: Fifo	41.73	38.29	
cslc: Interconn	61	61	
cslc: ISA	34.67	34	
cslc: Memmap	32.94	21.88	
cslc: Memory	6.56	6.56	
cslc: Pipeline	11.67	11.67	
cslc: Procon	6.92	6.92	
cslc: Reg	21.07	21.07	
cslc: RF	39	39	
cslc: Sched	9.79	9.79	
cslc: Tb	11.85	11.85	
cslc: Unit	58.62	58.62	
cslc: VC	25.71	25.71	ı
sw_lib: ASM	0	0	
sw_lib: Csim	0	0	
hw_lib:Memcntl	3.33	3.33	
hw_lib: micro eng	6.67	6.67	
hw_lib: Proc. Ring	5.83	5.83	
hw lib: PSCON	27.33	27.33	

under construction under test

intersection between

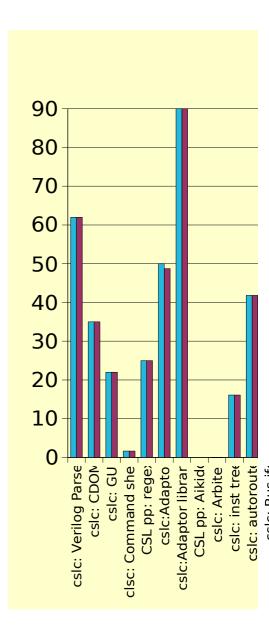
Not applicable

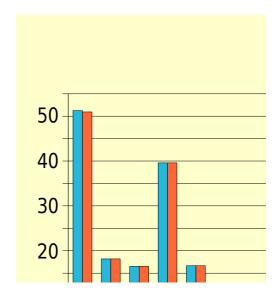
Divider

Priorities Low priority medium priority high priority

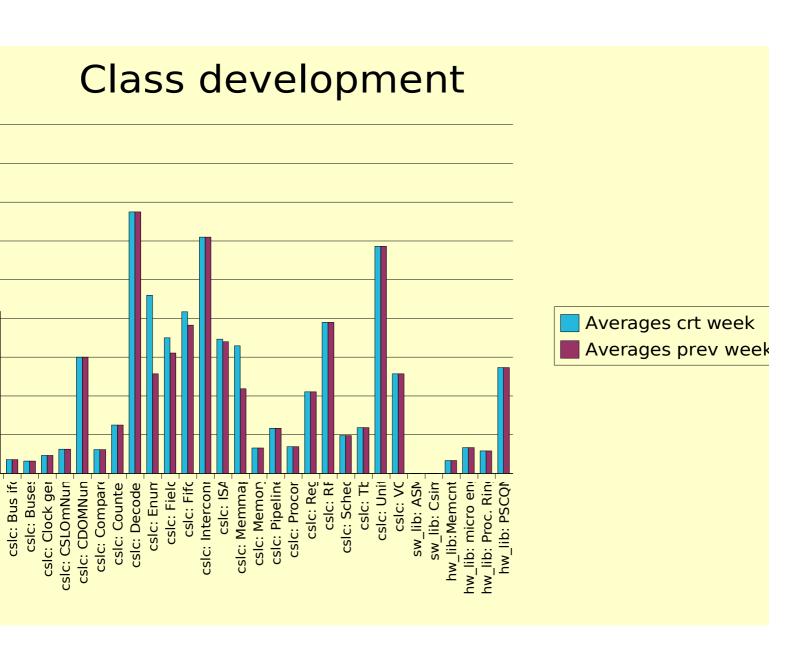
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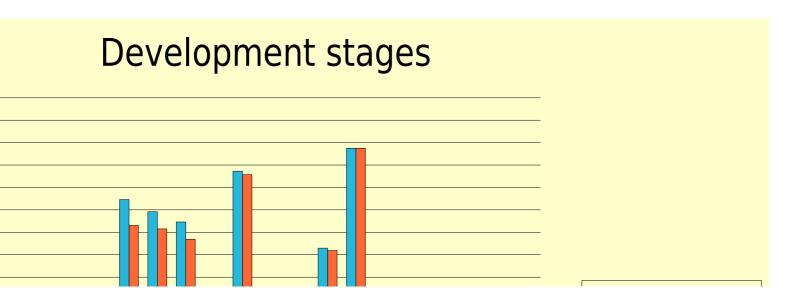
Overall project average 24.21

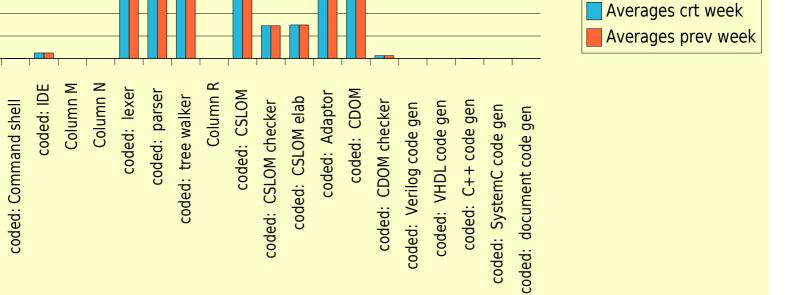


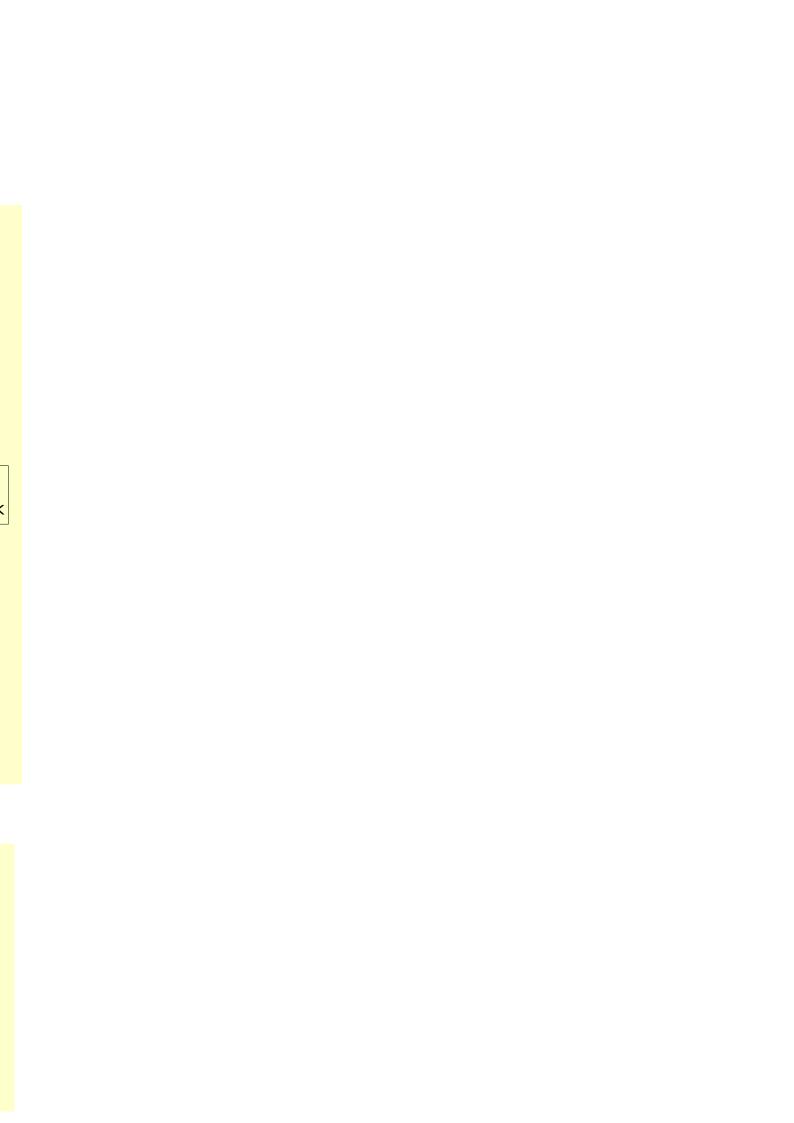


documented: Syntax
documented: data structures
documented: algorithms
documented: hw circuits
coded: CSL proto C++ lib
coded: Verilog library
coded: CSIM











cslc owner	cslc owner	CSL CLASS	documented: Syntax	documented: data structures	documented: algorithms	documented: hw circuits	coded: CSL proto C++ lib	coded: Verilog library	coded: CSIM	coded: Command shell	coded: IDE	L-P-Tw Owner	complete: cmd summary syntax	coded: lexer	coded: parser	coded: tree walker	coded: CSLOM	coded: CSLOM checker	coded: CSLOM elab	coded: Adaptor	coded: CDOM	coded: CDOM checker	coded: Verilog code gen	coded: VHDL code gen	coded: C++ code gen	SystemC c	coded: document code gen
NA		cslc: Verilog Parser	100	NA	NA	NA	NA	NA	NA	NA	NA	0		70	70	70	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
APA		cslc: CDOM	NA	25	25	NA	NA	-	NA	NA	NA			NA	NA	NA	NA	NA	NA	NA	85	5	NA	NA	NA	NA	NA
СР		cslc: GUI	NA	NA	NA	NA	NA	-	NA	NA	22			NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
OS		clsc: Command shell	5	NA	NA	NA	NA	NA		0	0			NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	
BZ		CSL pp: regex	25	NA	NA	NA	NA	NA		NA	NA			NA	NA	NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	
APA		cslc:Adaptor	50	50	50	NA	NA	NA		NA	NA		21.0	NA	NA	NA	NA	NA	NA	45	NA	NA		NA	NA	NA	
APA		cslc:Adaptor library	NA	NA	NA	NA	NA	-	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	90	NA	NA		NA	NA		
OS BZ		CSL pp: Aikido cslc: Arbiter	NA 0	NA NA	NA NA	NA 0	NA 0	NA NA		NA NA	NA NA		NA NA	NA 0	NA 0	NA 0	NA 0	NA 0	NA 0	NA 0	NA NA	NA 0	NA NA	NA NA	NA NA		
BZ		cslc: Arbiter	NA	25	25	NA	NA	NA		NA	5 5		NA	NA	NA	NA	65	0	25	0	0	0	NA	NA	NA		
BZ		cslc: mst tree	70	25	25	NA	0	NA		NA	5		NA	70	70	70	75	0	50	NA	NA	NA		NA	NA		
BZ		cslc: Bus ifc	25	0	0	25	0	NA		NA	0		0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA		
BZ		cslc: Buses	20	0	0	25	0	NA		NA	0		0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA		
BZ	2	cslc: Clock gen	40	0	0	25	0	NA		NA	0		0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA		
APO	-	cslc: CSLOmNum	0	0	0	NA	0		NA	NA	0		0	60	40	0	0	0	0	0	0	0	NA	NA	NA		
APO		cslc: CDOMNum	0	0	0	NA	0	-	NA	NA	0		100	100	100	90	0	0	0	0	90	0	NA	NA	NA		
OS	2	cslc: Compare	50	0	0	25	5		NA	NA	NA		0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA	NA	NA
OS	_	cslc: Counter	90	50	0	25	10	NA	NA	NA	0		0	0	0	0	0	0	NA	0	NA	0	NA	NΑ	NA	NA	NA
APA	1	cslc: Decoder	90	90	100	25	0	NA	NA	NA	0	OS	90	100	100	100	60	100	NA	90	NA	0	NA	NΑ	NA	NA	NA
BZ		cslc: Enum	90	0	0	50	40	NA	NA	NA	0	AB	90	0	0	0	90	0	NA	0	NA	0	NA	NA	NA	NA	NA
SP		cslc: Field	10	90	75	50	80	NA	NA	NA	0	GD	50	0	0	0	80	0	NA	0	NA	0	NA	NA	NA	NA	NA
OS	3	cslc: Fifo	75	0	0	55	1	NA	NA	NA	0	OS	90	50	50	50	95	0	NA	70	NA	0	NA	NA	NA	NA	NA
BZ	1	cslc: Interconn	80	70	70	50	5	NA	NA	NA	0	GD	90	90	90	90	90	90	0	90	NA	10	NA	NA	NA	NA	NA
SP	1	cslc: ISA	80	85	85	60	90	NA	NA	NA	0	AB	70	0	0	0	40	0	0	0	NA	0	NA	NA	NA	NA	NA
AB	1	cslc: Memmap	70	0	0	50	90	NA	NA	NA	0	GD	50	10	10	0	70	0	0	0	NA	0	NA	NA	0	NA	NA
BZ	_	cslc: Memory	50	0	0	50	0	NA		NA	0		0	0	0	0	5	0	0	0	NA	0		NA		NA	NA
BZ		cslc: Pipeline	70	0	0	50	5	147	NA	NA	0	OS	50	0	0	0	0	0	0	0	NA			NA		NA	NA
OS	?	cslc: Procon	83	0	0	NA				NA			NA		0	0	0	0	NA		NA					NA	
OS		cslc: Reg	85	0	0	50				NA		GD	30	0	0	0	60	0	NA		NA					NA	
OS DZ		cslc: RF	86	0	0	50				NA		AB	80	50	50	50	90	0	NA		NA					NA	
BZ		cslc: Sched	87	0	0	50				NA		A D	0	0	0	0	0	0	NA		NA					NA	
OS DZ		cslc: Tb	89	0	0	NA				NA		AB	60	0	0	0	5	0	NA		NA					NA	
BZ OS		cslc: Unit cslc: VC	90 90	90	90	50 50				NA	0	OS	NA 60	90	90	90	80 80	0	NA NA		NA					NA NA	
05	l	sw lib: ASM			0	NA				NA NA		<u>US</u>	60	NA	NA	NA		NA	NA		NA	0 NA					
		sw_lib: ASM sw_lib: Csim	0	0	0	NA				NA				NA	NA	NA	NA NA	NA	NA			NA			_	-	
CL		hw lib:Memcntl	0	0	0	20	0			NA				NA	NA	NA	NA	NA	NA			NA					
CL		hw lib: micro eng	0	0	0	40	0			NA				NA	NA	NA	NA	NA	NA			NA					
AV		hw_lib: Proc. Ring	0	0	0	35	0			NA				NA	NA	NA	NA	NA	NA			NA					
AV		hw_lib: PSCQN	84	0	0		40	_		NA				NA	NA	NA	NA	_	NA	_					-	-	
		STATUS LEGEND put p																									
		not started			t red																						

not started
under construction
under test
completed
intersection between a
Not applicable
Divider

light red yellow light magenta green light blue dark violet black

Priorities

Low priority medium priority high priority orange 4 violet red

File name = csl_class.ods misc/project_management/csl_class.ods

Stages	documented: Syntax	documented: data structures	documented: algorithms	documented: hw circuits	coded: CSL proto C++ lib	coded: Verilog library	coded: CSIM	coded: Command shell	coded: IDE		coded: lexer	coded: parser	coded: tree walker	coded: CSLOM	coded: CSLOM checker	coded: CSLOM elab	coded: Adaptor	coded: CDOM	coded: CDOM checker	coded: Verilog code gen	coded: VHDL code gen	coded: C++ code gen	coded: SystemC code gen	coded: document code gen
Averages crt week	50.97	18.18	16.52	39.58	16.65	0	#DIV/0i	0	1.23		26.54	25.77	23.46	37.88	7.31	7.5	20.93	43.75	0.65	#DIV/0i	#DIV/0!	0	#DIV/0!	#DIV/0!
Averages prev week	50.97	18.18	16.52	39.58	16.65	0	#DIV/0!	0	1.15		26.54	25.77	23.46	34.04	7.31	7.5	21.48	43.75	0.65	#DIV/0!	#DIV/0	0	#DIV/0!	#DIV/0!

class														tion	,		ien										owner		
uses CSLOM: CSL Info class	uses CSLOM: CSL Unit	uses CSLOM: Arbiter	uses CSLOM: Asembler	uses CSLOM: Bus ifc	uses CSLOM: Buses	uses CSLOM: Clock	uses CSLOM: Compare	uses CSLOM: Counter	Sim	uses CSLOM: Decoder	uses CSLOM: Event	ij	sa	uses CSLOM: Mem location	uses CSLOM: Mem map	uses CSLOM: Memory	uses CSLOM: pattern_gen	uses CSLOM: Pipeline	uses CSLOM: Scheduler	State	Jnit	/C	piler		ary	uses Verilog Library	CSL C++ prototype lib owner		
OM:	OM: (/ :MC) MC	JM:	J.MC):MC) :WC) :WC	uses CSLOM: Csim	J :MC	JM:	uses CSLOM: FF	uses CSLOM: Isa	J :MC	J.MC	J.MC	ЭМ: р	JM: F	S:MC	uses CSLOM: State	uses CSLOM: Unit	uses CSLOM: VC	uses cslc Compilei	orols	uses CSL Library	log L	prot		
CSL	CSL	CSL	CSL	CST(CSL(CSF(CSL	CSL	CSL	CSL	CSF	CSL	CSL	CSL	CSL	CSL	CSL	CST(CSF	CSL	CSF(CST(cslc	uses libcslc.o	CSL	. Veri	C++	ity	
səsn	nses	nses	səsn	nses	nses	nses	nses	nses	nses	nses	səsn	nses	nses	nses	nses	səsn	nses	nses	səsn	nses	nses	nses	nses	nses	səsn		CSL	priority	
																												NA	
																						L,					NA		X
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	1	1	1	1	1	ı	ı	1	1	1	1	-1	1	1	1	1	1	1	1	_	1								X
																						Н					NA	NA	X
																						Н							X
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																											NA	NA	

CSL CLASS	Averages crt v	Averages prev	week
cslc: Verilog Parser	62	77.5	
cslc: CDOM	35	35	
cslc: GUI	22	20	_
clsc: Command shell	1.67		
CSL pp: regex	25	25	
cslc:Adaptor	48.75	47.5	
cslc:Adaptor library	90	90	
CSL pp: Aikido	#DIV/0!	#DIV/0!	
cslc: Arbiter	0	0	
cslc: inst tree	16.11	16.11	
cslc: autoroute	41.82	41.82	
cslc: Bus ifc	3.57	3.57	
cslc: Buses	3.21	3.21	
cslc: Clock gen	4.64	4.64	
cslc: CSLOmNum	6.25	6.25	
cslc: CDOMNum	30	30	
cslc: Compare	6.15	6.15	
cslc: Counter	12.5	12.5	
cslc: Decoder	67.5	70.36	
cslc: Enum	25.71	23.57	
cslc: Field	31.07	27.14	
cslc: Fifo	38.29	39	
cslc: Interconn	61	61	
cslc: ISA	34	34	
cslc: Memmap	21.88	19.38	
cslc: Memory	6.56	6.56	
cslc: Pipeline	11.67	11.67	
cslc: Procon	6.92	6.92	
cslc: Reg	21.07	21.07	
cslc: RF	39	38.64	
cslc: Sched	9.79	9.79	
cslc: Tb	11.85	11.85	
cslc: Unit	58.62	58.62	
cslc: VC	25.71	25.71	•
sw_lib: ASM	0	0	
sw_lib: Csim	0	0	
hw_lib:Memcntl	3.33	3.33	
hw_lib: micro eng	6.67	6.67	
hw_lib: Proc. Ring	5.83	5.83	
hw lib: PSCON	27 33	27 33	

STATUS LEGEND put percentages in the boxes

Overall project average

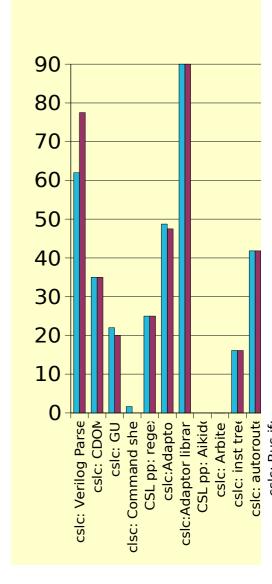
22.72

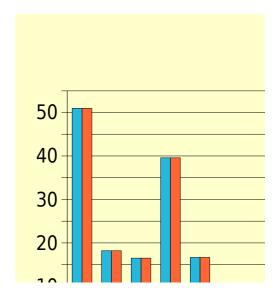
under construction under test intersection between

Not applicable Divider

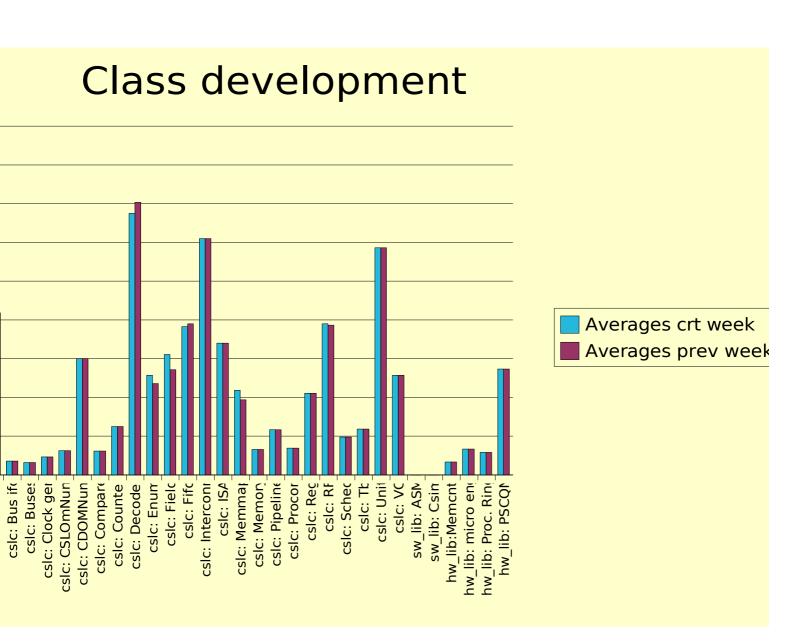
Priorities Low priority medium priority high priority

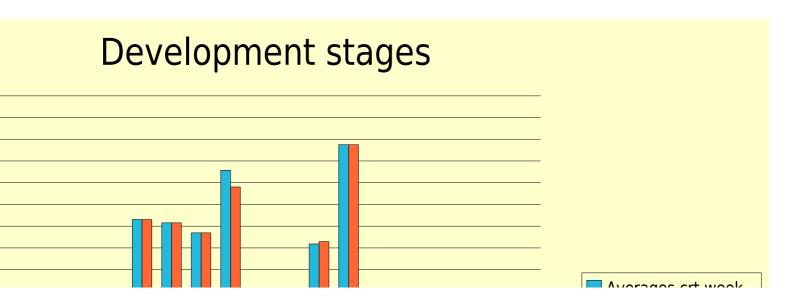
File name = $csl_class.ods$ misc/project_management/csl_class.ods





documented: Syntax
documented: data structures
documented: algorithms
documented: hw circuits
coded: CSL proto C++ lib
coded: Verilog library
coded: CSIM





Averages cit week Averages prev week

coded: IDE coded: Command shell

Column M

Column N coded: lexer

coded: parser

coded: CSLOM coded: tree walker

coded: CSLOM elab coded: CSLOM checker

coded: CDOM coded: Adaptor

coded: CDOM checker

coded: Verilog code gen coded: VHDL code gen coded: C++ code gen coded: SystemC code gen

coded: document code gen





cslc owner	cslc owner	CSL CLASS	documented: Syntax	documented: data structures	documented: algorithms	documented: hw circuits	coded: CSL proto C++ lib	coded: Verilog library	coded: CSIM	coded: Command shell	coded: IDE	L-P-Tw Owner	complete: cmd summary synta	coded: lexer	coded: parser	coded: tree walker	coded: CSLOM	coded: CSLOM checker	coded: CSLOM elab	coded: Adaptor	coded: CDOM	coded: CDOM checker	coded: Verilog code gen	coded: VHDL code gen	coded: C++ code gen	SystemC c	coded: document code gen
NA		cslc: Verilog Parser	100	NA	NA	NA	NA	NA	NA	NA	NA			70	70	70	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
APA		cslc: CDOM	NA	25	25	NA	NA	NA	NA	NA	NA			NA	NA	NA	NA	NA	NA	NA	85	5	NA	NA	NA	NA	NA
CP		cslc: GUI	NA	NA	NA	NA	NA	-	NA	NA	20			NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
OS		clsc: Command shell	5	NA	NA	NA	NA	NA		0	0			NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
BZ		CSL pp: regex	25	NA	NA	NA	NA	NA		NA	NA			NA	NA	NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	
APA		cslc:Adaptor	50	50	50	NA	NA	NA		NA	NA		21.0	NA	NA	NA	NA	NA	NA	40	NA	NA		NA	NA	NA	
APA OS		cslc:Adaptor library	NA	NA NA	NA	NA NA	NA NA	NA NA	NA	NA	NA		NA	NA	NA NA	NA NA	NA NA	NA NA	NA	90	NA NA	NA	NA NA	NA	NA		
BZ		CSL pp: Aikido cslc: Arbiter	NA 0	NA	NA NA	0	0	NA		NA NA	NA NA		NA NA	NA 0	0	0	0	0	NA 0	NA 0	NA	NA 0	NA	NA NA	NA NA		
BZ		cslc: inst tree	NA	25	25	NA	NA	NA		NA	5		NA	NA	NA	NA	65	0	25	0	0	0	NA	NA	NA		
BZ		cslc: mst tree	70	25	25	NA	0	NA		NA	5		NA	70	70	70	75	0	50	NA	NA	NA		NA	NA		
BZ		cslc: Bus ifc	25	0	0	25	0	NA		NA	0		0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA		
BZ		cslc: Buses	20	0	0	25	0	NA		NA	0		0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA		
BZ	2	cslc: Clock gen	40	0	0	25	0	NA		NA	0		0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA		
APO		cslc: CSLOmNum	0	0	0	NA	0		NA	NA	0		0	60	40	0	0	0	0	0	0	0	NA	NA	NA	NA	NA
APO		cslc: CDOMNum	0	0	0	NA	0	0	NA	NA	0		100	100	100	90	0	0	0	0	90	0	NA	NA	NA	NA	NA
OS	2	cslc: Compare	50	0	0	25	5	NA	NA	NA	NA		0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA	NA	NA
OS	1	cslc: Counter	90	50	0	25	10	NA	NA	NA	0		0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA	NA	NA
APA	1	cslc: Decoder	90	90	100	25	0	NA	NA	NA	0	OS.	90	100	100	100	100	100	NA	90	NA	0	NA	NA	NA	NA	NA
BZ		cslc: Enum	90	0	0	50	40	NA	NA	NA	0	AB	90	0	0	0	60	0	NA	0	NA	0	NA	NA	NA	NA	NA
SP		cslc: Field	10	90	75	50	80		NA	NA	0	GD	50	0	0	0	25	0	NA	0	NA	0	NA	NA	NA	NA	NA
OS	3	cslc: Fifo	75	0	0	55	1		NA	NA	0	OS	90	50	50	50	85	0	NA	90	NA	0	NA	NA	NA	NA	NA
BZ	1	cslc: Interconn	80	70	70	50	5		NA	NA	0	GD	90	90	90	90	90	90	0	90	NA	10		NA	NA	NA	
SP	1	cslc: ISA	80	85	85	60		NA		NA	0	AB	70	0	0	0	40	0	0	0	NA	0	NA	NA	NA	NA	
AB	1	cslc: Memmap	70	0	0	50			NA	NA	0	GD	50	10	10	0	30	0	0	0	NA	0	NA	NA	0	NA	
BZ		cslc: Memory	50	0	0	50	0	NA		NA	0	0.5	0	0	0	0	5	0	0	0	NA	0		NA		NA	NA
BZ		cslc: Pipeline	70	0	0	50	5	147	NA	NA	0	OS.	50	0	0	0	0	0	0	0	NA			NA		NA	NA
OS OS		cslc: Procon	83 85	0	0	NA 50				NA NA		GD	NA 30	0	0	0	60	0	NA NA		NA NA					NA NA	
OS OS		cslc: Reg cslc: RF	86	0	0	50				NA		AB	80	50	50	50	85	0	NA		NA					NA	
BZ		cslc: Sched	87	0	0	50				NA		AD	0	0	0	0	0	0	NA		NA					NA	
OS		cslc: Jened	89	0	0	NA				NA		AB	60	0	0	0	5	0	NA		NA					NA	
BZ		cslc: Unit	90	90	90	50				NA		7 (5	NA	90	90	90	80	0	NA		NA					NA	
OS	1	cslc: VC	90	0		50				NA	0	OS.	60	0	0	0	80	0	NA		NA					NA	
		sw lib: ASM	0		0	NA				NA				NA	NA	NA	NA	NA	NA			NA					
		sw_lib: Csim	0	0	0	NA				NA				NA	NA	NA	NA	NA	NA			NA				-	
CL		hw_lib:Memcntl	0	0	0	20	0			NA				NA	NA	NA	NA	NA	NA			NA					
CL		hw_lib: micro eng	0	0	0	40	0			NA				NA	NA	NA	NA	NA	NA			NA					
AV		hw_lib: Proc. Ring	0	0	0	35	0	0	NA	NA	NA			NA	NA	NA	NA	NA	NA			NA					
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		STATUS LEGEND put p	ercen	tage	s in t	he b	oxes	5																			
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not started
under construction
under test
completed
intersection between a
Not applicable
Divider

light red yellow light magenta green light blue dark violet black

Priorities

Low priority medium priority high priority

orange 4 violet red

File name = csl_class.ods misc/project_management/csl_class.ods

Stages	documented: Syntax	documented: data structures	documented: algorithms	documented: hw circuits	coded: CSL proto C++ lib	coded: Verilog library	coded: CSIM	coded: Command shell	coded: IDE		coded: lexer	coded: parser	coded: tree walker	coded: CSLOM	coded: CSLOM checker	coded: CSLOM elab	coded: Adaptor	coded: CDOM	coded: CDOM checker	coded: Verilog code gen	coded: VHDL code gen	coded: C++ code gen	coded: SystemC code gen	coded: document code gen
Averages crt week	50.97	18.18	16.52	39.58	16.65	0	#DIV/0!	0	1.15		26.54	25.77	23.46	34.04	7.31	7.5	21.48	43.75	0.65	#DIV/0	#DIV/0i	0	#DIV/0!	#DIV/0!
Averages prev week	50.97	18.18	16.52	39.58	16.65	0	#DIV/0!	0	96.0		26.54	25.77	23.46	33.65	7.31	7.5	21.3	43.75	0.65	#DIV/0!	#DIV/0	0	#DIV/0i	#DIV/0!

ass														ion			u										wner		
uses CSLOM: CSL Info class	uses CSLOM: CSL Unit	biter	uses CSLOM: Asembler	s ifc	ses	ock	uses CSLOM: Compare	uses CSLOM: Counter	<u>.E</u>	uses CSLOM: Decoder	ent			uses CSLOM: Mem location	uses CSLOM: Mem map	uses CSLOM: Memory	uses CSLOM: pattern_gen	uses CSLOM: Pipeline	uses CSLOM: Scheduler	ate	뇓		iler		,	rary	CSL C++ prototype lib owner		
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CSL CLASS Averages crt wAverages prev week cslc: Verilog Parser cslc: CDOM 35 35 cslc: GUI 20 15 clsc: Command shell CSL pp: regex 25 25 47.5 46.25 cslc:Adaptor 90 90 cslc:Adaptor library CSL pp: Aikido #DIV/0! #DIV/0! cslc: Arbiter 16.11 16.11 cslc: inst tree 41.82 cslc: autoroute 41.82 3.57 cslc: Bus ifc 3.57 3.21 3.21 cslc: Buses 4.64 cslc: Clock gen 4.64 cslc: CSLOmNum 6.25 6.25 cslc: CDOMNum 30 30 6.15 6.15 cslc: Compare cslc: Counter 12.5 70.36 70.36 cslc: Decoder cslc: Enum 23.57 23.57 27.14 cslc: Field 27.14 cslc: Fifo 39 61 61 cslc: Interconn 34 cslc: ISA 34 19.38 19.38 cslc: Memmap cslc: Memory 6.56 6.56 cslc: Pipeline 11.67 11.67 cslc: Procon 6.92 6.92 21.07 21.07 cslc: Reg 38.64 37.93 cslc: RF cslc: Sched 9.79 9.79 cslc: Tb 11.85 11.85 cslc: Unit 58.62 58.62 cslc: VC 25.71 25.71 sw_lib: ASM sw_lib: Csim 3.33 3.33 hw_lib:Memcntl 6.67 6.67 hw_lib: micro eng hw_lib: Proc. Ring 5.83 5.83 hw_lib: PSCQN 27.33 27.33

STATUS LEGEND put percentages in the boxes

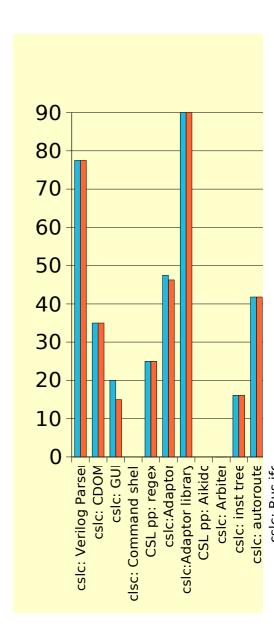
under construction under test completed intersection between I Not applicable

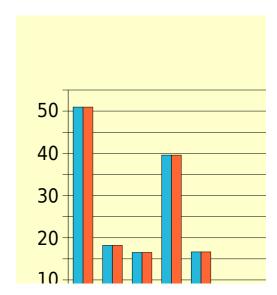
Overall project average 22.56

Priorities
Low priority
medium priority
high priority

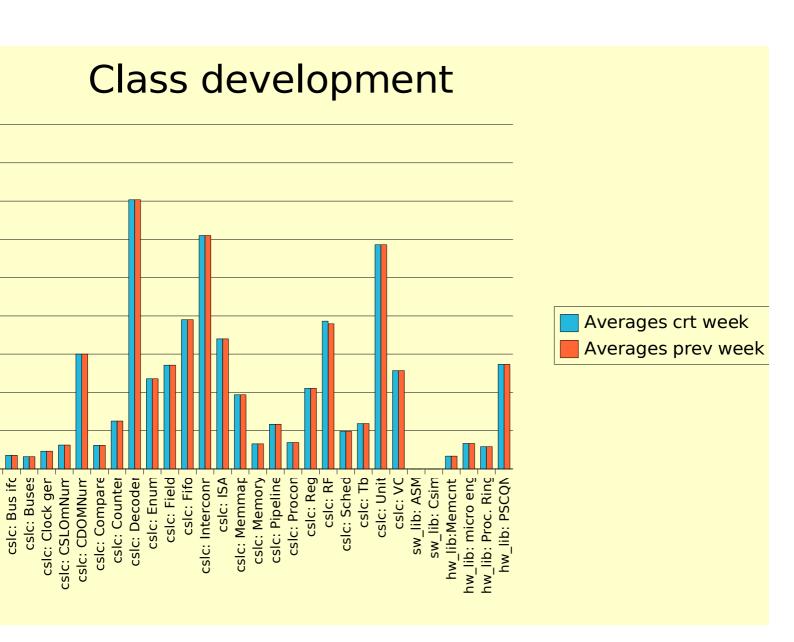
Divider

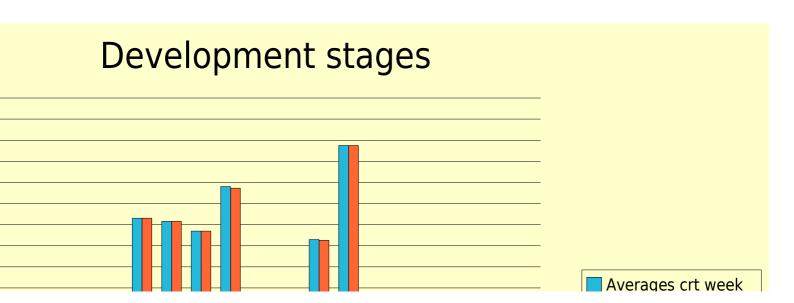
File name = csl_class.ods misc/project_management/csl_class.ods





documented: Syntax
documented: data structures
documented: algorithms
documented: hw circuits
coded: CSL proto C++ lib
coded: Verilog library
coded: CSIM





coded: Command shell

coded: IDE

Column M

Column N

coded: lexer coded: parser

coded: tree walker coded: CSLOM

coded: CSLOM checker coded: CSLOM elab

coded: Adaptor coded: CDOM

coded: CDOM checker

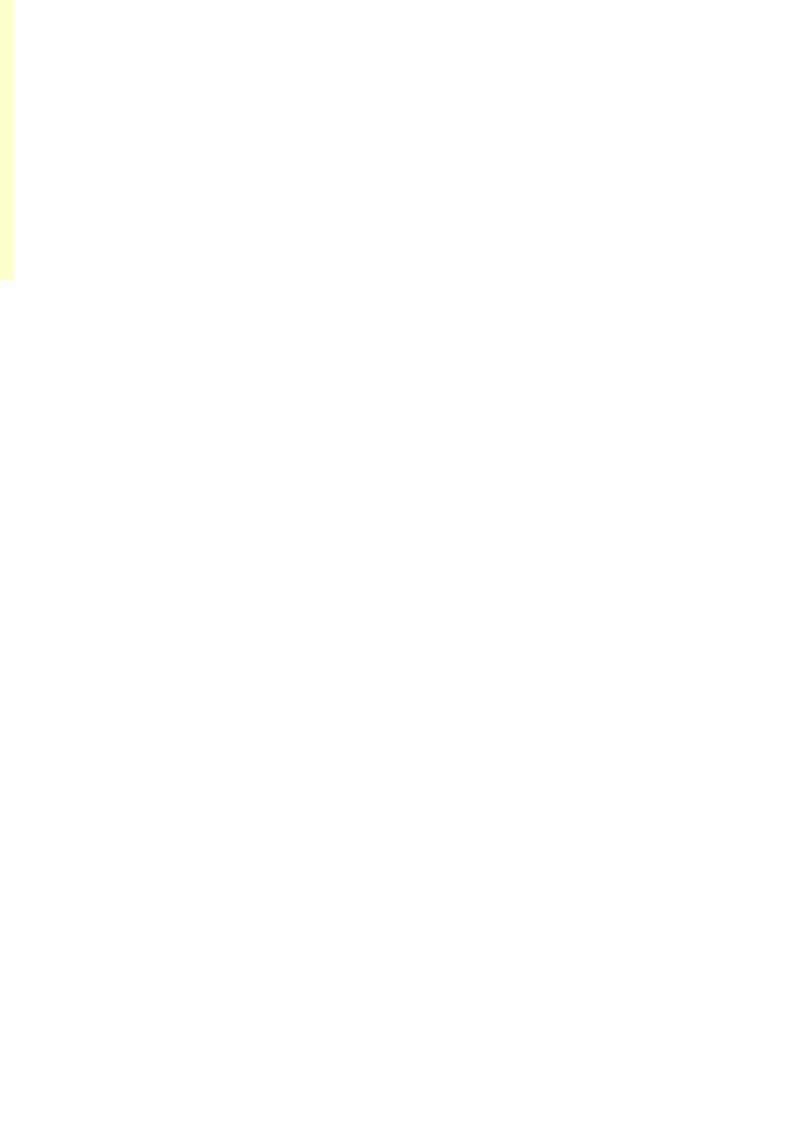
coded: Verilog code gen coded: VHDL code gen

coded: C++ code gen

coded: SystemC code gen

coded: document code gen





cslc owner	cslc owner	CSL CLASS	documented: Syntax	documented: data structures	documented: algorithms	documented: hw circuits	coded: CSL proto C++ lib	coded: Verilog library	coded: CSIM	coded: Command shell	coded: IDE	L-P-Tw Owner	complete: cmd summary synta	coded: lexer	coded: parser	coded: tree walker	coded: CSLOM	coded: CSLOM checker	coded: CSLOM elab	coded: Adaptor	coded: CDOM	coded: CDOM checker	coded: Verilog code gen	coded: VHDL code gen		coded: SystemC code gen	coded: document code gen
NA		cslc: Verilog Parser	100	NA	NA	NA	NA	NA	NA	NA	NA			70	70	70	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
APA		cslc: CDOM	NA	25	25	NA	NA	NA	NA	NA	NA			NA	NA	NA	NA	NA	NA	NA	85	5	NA	NA	NA	NA	NA
CP		cslc: GUI	NA	NA	NA	NA		_	NA	NA	15			NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
OS		clsc: Command shell	5	NA	NA	NA		_	NA	0	0			NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA	-	NA
BZ		CSL pp: regex	25	NA	NA	NA		_	NA		NA			NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA	_	NA
APA		cslc:Adaptor	50	50	50	NA		_	NA	NA	NA			NA	NA	NA	NA	NA	NA	35	NA	NA	NA		NA	_	NA
APA		cslc:Adaptor library	NA	NA	NA	NA	NA	_	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	90	NA	NA	NA		NA	_	NA
OS BZ		CSL pp: Aikido cslc: Arbiter	NA 0	NA NA	NA NA	NA 0	NA 0		NA NA	NA NA	NA NA		NA NA	NA 0	NA 0	NA 0	NA 0	NA 0	NA 0	NA 0	NA NA	NA 0	NA NA		NA NA	_	NA NA
BZ		cslc: Arbiter	NA	25	25	NA	NA		NA	NA	5		NA	NA	NA	NA	65	0	25	0	0	0	NA		NA	-	NA
BZ		cslc: autoroute	70	25	25	NA	0		NA	NA	5		NA	70	70	70	75	0	50	NA	NA	NA	NA		NA	_	NA
BZ		cslc: Bus ifc	25	0	0	25	0		NA	NA	0		0	0	0	0	0	0	NA	0	NA	0	NA		NA	_	NA
BZ		cslc: Buses	20	0	0	25	0		NA	NA	0		0	0	0	0	0	0	NA	0	NA	0	NA		NA	-	NA
BZ	2	cslc: Clock gen	40	0	0	25	0		NA	NA	0		0	0	0	0	0	0	NA	0	NA	0	NA		NA	_	NA
APO	_	cslc: CSLOmNum	0	0	0	NA	0		NA	NA	0		0	60	40	0	0	0	0	0	0	0	NA		NA	_	NA
APO		cslc: CDOMNum	0	0	0	NA	0	_	NA	NA	0		100	100	100	90	0	0	0	0	90	0	NA		NA	_	NA
OS	2	cslc: Compare	50	0	0	25	5	NA	NA	NA	NA		0	0	0	0	0	0	NA	0	NA	0	NA		NA		NA
OS	1	cslc: Counter	90	50	0	25	10	NA	NA	NA	0		0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA	NA	NA
APA	1	cslc: Decoder	90	90	100	25	0	NA	NA	NA	0	OS	90	100	100	100	100	100	NA	90	NA	0	NA	NA	NA	NA	NA
ΒZ		cslc: Enum	90	0	0	50	40	NA	NA	NA	0	AB	90	0	0	0	60	0	NA	0	NA	0	NA	NA	NA	NA	NA
SP		cslc: Field	10	90	75	50	80	NA	NA	NA	0	GD	50	0	0	0	25	0	NA	0	NA	0	NA	NA	NA	NA	NA
OS	3	cslc: Fifo	75	0	0	55	1	NA	NA	NA	0	OS	90	50	50	50	85	0	NA	90	NA	0	NA	NA	NA	NA	NA
BZ	1	cslc: Interconn	80	70	70	50	5		NA	NA	0	GD	90	90	90	90	90	90	0	90	NA	10	NA	NA	NA	NA	NA
SP	1	cslc: ISA	80	85	85	60	90	NA	NA	NA	0	AB	70	0	0	0	40	0	0	0	NA	0	NA	NA	NA	NA	NA
AB	1	cslc: Memmap	70	0	0	50	90	NA	NA	NA	0	GD	50	10	10	0	30	0	0	0	NA	0	NA	NA	0	NA	NA
BZ	_	cslc: Memory	50	0	0	50	0	NA		NA	0		0	0	0	0	5	0	0	0	NA	0		NA		-	NA
BZ	_	cslc: Pipeline	70	0	0	50	5	NA		NA	0	OS	50	0	0	0	0	0	0	0	NA				NA		NA
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OS DZ		cslc: RF	86	0	0	50				NA		AB	80	50	50	50	75	0	NA		NA				NA	-	
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		sw_lib: Csim	0	0	0	NA					NA			NA	NA	NA	NA	NA	NA	_	NA				NA		
CL		hw_lib:Memcntl	0	0	0	20	0				NA			NA	NA	NA	NA	NA	NA			NA			-	$\overline{}$	
CL		hw_lib: micro eng	0	0	0	40	0	-			NA			NA	NA	NA	NA	NA	NA			NA				-	
AV		hw_lib: Proc. Ring	0	0	0	35	0	_			NA			NA	NA	NA	NA	NA	NA			NA				-	
AV		hw_lib: PSCQN	84	0	0		40			NA				NA	NA	NA	NA	NA							-	-	
		STATUS LEGEND put p		tage	s in t																						
		not started		-	t rod																						

not started
under construction
under test
completed
intersection between r
Not applicable
Divider

light red yellow light magenta green light blue dark violet black

Priorities

Low priority medium priority high priority

orange 4 violet red

File name = csl_class.ods misc/project_management/csl_class.ods

Stages	documented: Syntax	documented: data structures	documented: algorithms	documented: hw circuits	coded: CSL proto C++ lib	coded: Verilog library	coded: CSIM	coded: Command shell	coded: IDE		coded: lexer	coded: parser	coded: tree walker	coded: CSLOM	coded: CSLOM checker	coded: CSLOM elab	coded: Adaptor	coded: CDOM	coded: CDOM checker	coded: Verilog code gen	coded: VHDL code gen	coded: C++ code gen	coded: SystemC code gen	coded: document code gen
Averages crt week	50.97	18.18	16.52	39.58	16.65	0	#DIV/0!	0	96.0		26.54	25.77	23.46	33.65	7.31	7.5	21.3	43.75	0.65	#DIV/0!	#DIV/0!	0	#DIV/0!	#DIV/0!
Averages prev week	52	17.65	16.03	40	16.13	0	#DIV/0!	0	0.93		21.85	21.11	18.89	35	7.04	7.5	20.36	43.75	0.63	#DIV/0!	#DIV/0!	0	#DIV/0!	#DIV/0!

class														tion			en										owner		
uses CSLOM: CSL Info class	uses CSLOM: CSL Unit	uses CSLOM: Arbiter	uses CSLOM: Asembler	uses CSLOM: Bus ifc	uses CSLOM: Buses	uses CSLOM: Clock	uses CSLOM: Compare	uses CSLOM: Counter	sim	uses CSLOM: Decoder	uses CSLOM: Event	Ш	ga	uses CSLOM: Mem location	uses CSLOM: Mem map	uses CSLOM: Memory	uses CSLOM: pattern_gen	uses CSLOM: Pipeline	uses CSLOM: Scheduler	tate	ınit	C	piler		ry	uses Verilog Library	CSL C++ prototype lib owner		
) :WC	OM:	M: A	M: A	JM: E	OM: E	O.W.	O:WC	OM:	uses CSLOM: Csim	J : L	OM: E	uses CSLOM: FF	uses CSLOM: Isa	M: N	M: N	JM: N	ЭМ: р	JM: P	OM: S	uses CSLOM: State	uses CSLOM: Unit	uses CSLOM: VC	uses cslc Compilei	lc.o	uses CSL Library	log Li	prot		
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cslc: Verilog Parser cslc: CDOM 35 35 cslc: GUI 15 15 clsc: Command shell CSL pp: regex 25 25 46.25 45 cslc:Adaptor cslc:Adaptor library 90 90 CSL pp: Aikido #DIV/0! #DIV/0! cslc: Arbiter 16.11 16.11 cslc: inst tree cslc: autoroute 41.82 41.82 3.85 cslc: Bus ifc 3.57 3.21 3.46 cslc: Buses 4.64 5 cslc: Clock gen cslc: CSLOmNum 6.25 6.67 cslc: CDOMNum 30 25.33 6.15 6.67 cslc: Compare cslc: Counter 13.46 70.36 cslc: Decoder 68.85 cslc: Enum 23.57 19.23 cslc: Field 27.14 27.31 cslc: Fifo 24.31 61 58.93 cslc: Interconn 31.79 cslc: ISA 34 19.38 17.33 cslc: Memmap cslc: Memory 6.56 7 cslc: Pipeline 11.67 8.93 cslc: Procon 6.92 6.92 21.07 20.38 cslc: Reg 37.93 24.69 cslc: RF 10.54 cslc: Sched 9.79 cslc: Tb 11.85 7.83 cslc: Unit 58.62 58.62 25.71 cslc: VC 23.08 sw_lib: ASM sw_lib: Csim 3.33 3.33 hw_lib:Memcntl 6.67 6.67 hw_lib: micro eng hw_lib: Proc. Ring 5.83 5.83 hw_lib: PSCQN 27.33 27.33

Averages crt wAverages prev week

STATUS LEGEND put percentages in the boxes

not started
under construction
under test
completed
intersection between
Not applicable

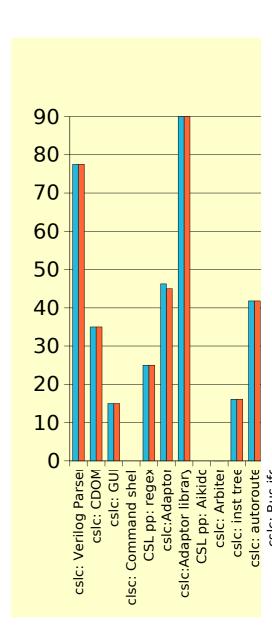
CSL CLASS

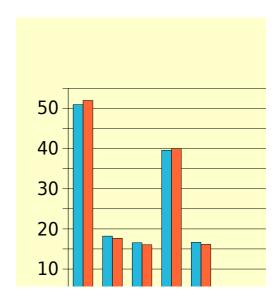
Overall project average 22.51

Priorities
Low priority
medium priority
high priority

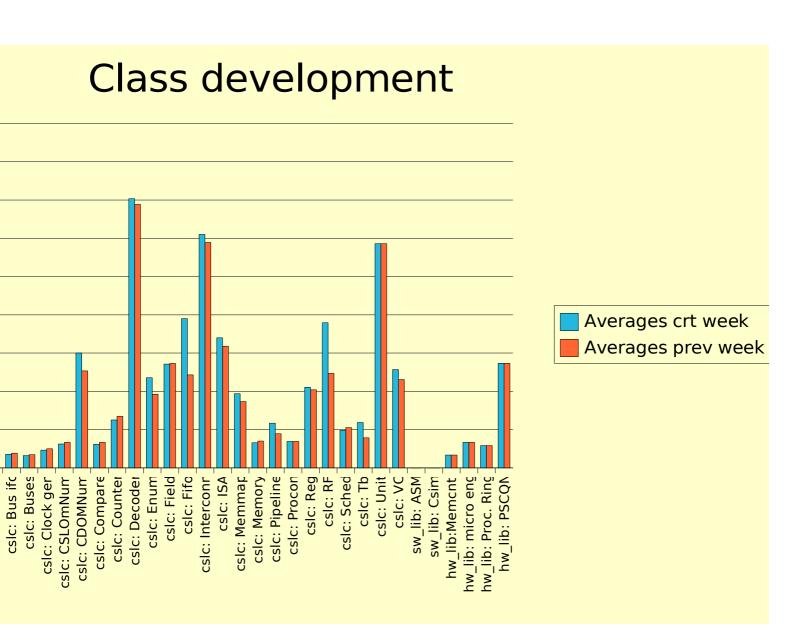
Divider

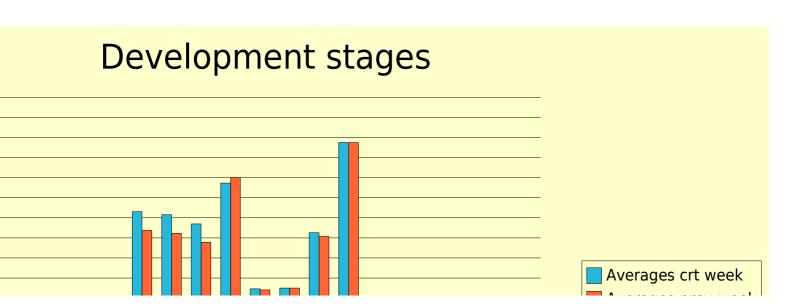
File name = csl_class.ods misc/project_management/csl_class.ods





documented: Syntax
documented: data structures
documented: algorithms
documented: hw circuits
coded: CSL proto C++ lib
coded: Verilog library
coded: CSIm





Averages prev week

coded: IDE coded: Command shell

Column N Column M

coded: lexer

coded: parser

coded: tree walker

coded: CSLOM

coded: CSLOM checker coded: CSLOM elab

coded: Adaptor

coded: CDOM

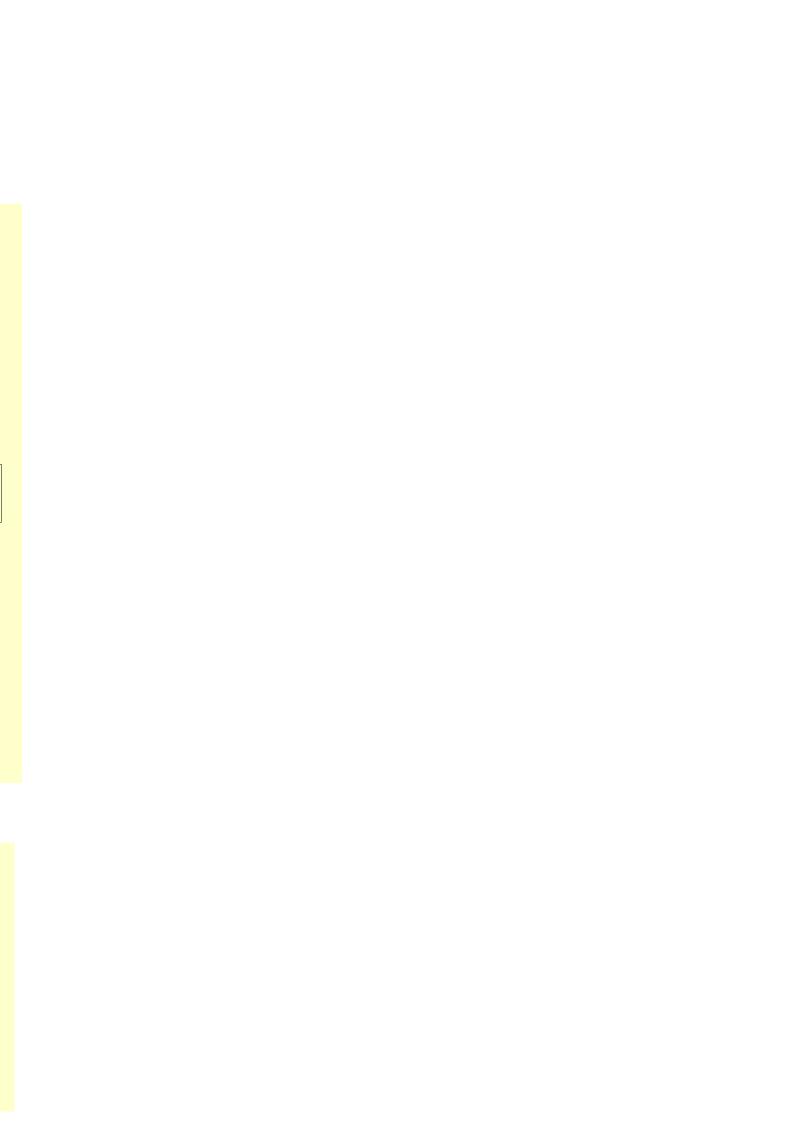
coded: CDOM checker coded: Verilog code gen

coded: VHDL code gen

coded: C++ code gen

coded: SystemC code gen

coded: document code gen





: owner	owner		documented: Syntax	documented: data structures	documented: algorithms	documented: hw circuits	coded: CSL proto C++ lib	coded: Verilog library	ed: CSIM	coded: Command shell	coded: IDE	coded: lexer	coded: parser	coded: tree walker	coded: CSLOM	coded: CSLOM checker	coded: CSLOM elab	coded: Adaptor	coded: CDOM	coded: CDOM checker	coded: Verilog code gen	coded: VHDL code gen	coded: C++ code gen	coded: SystemC code gen	coded: document code gen		s CSLOM: CSL Unit	s CSLOM: Arbiter
cslc	cslc	CSL CLASS	goc	မို	ဗို	op	l bo	pos	coded:	pos	pos	роз	p	poo	90	DO3	DO3	poo	pos	poo	l po	cod	po O	poo	cod	nses	nses	nse
NA		cslc: Verilog Parser	100	NA	NA	NA	NA		NA		NA	70	70	70	NA	NA	NA	NA	NA			NA	NA	NA	NA			
APA		cslc: CDOM	NA	25	25	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	85	5	NA	NA	NA	NA	NA			
CP		cslc: GUI	NA	NA	NA	NA	NA	NA	NA	NA	15	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		1	1
OS		clsc: Command shell	5	NA	NA	NA	NA	NA	NΑ	0	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		1	1
BZ		CSL pp: regex	25	NA	NA	NA	NA	NA	NΑ	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA			
APA		cslc:Adaptor	50	50	50	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	30	NA	NA	NA	NA	NA	NA	NA			
APA		cslc:Adaptor library	NA	NA	NA	NA	NA	NA	NΑ	NA	NA	NA	NA	NA	NA	NA	NA	90	NA	NA	NA	NA	NA	NA	NA			
OS		CSL pp: Aikido	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA			
BZ		cslc: Arbiter	0	NA	NA	0	0	NA	_		NA	0	0	0	0	0	0	0	NA	0	NA	NA	NA	NA	NA			
BZ		cslc: inst tree	NA	25	25	NA	NA	NA	_		5	NA	NA	NA	65	0	25	0	0	0		NA		NA	NA		Ш	Ш
BZ		cslc: autoroute	70	25	25	NA	0	NA	_		5	70	70	70	75	0	50		NA			NA		NA				
BZ		cslc: Bus ifc	25	0	0	25	0		NA		0	0	0	0	0	0	NA		NA			NA		NA				
BZ		cslc: Buses	20	0	0	25	0		NA		0	0	0	0	0	0	NA	0	NA			NA	-	NA			Ш	
BZ	2	cslc: Clock gen	40	0	0	25	0		NA		0	0	0	0	0	0	NA	0	NA			NA	-	NA			Ш	\vdash
APO		cslc: CSLOmNum	0	0	0	NA	0		NA		0	60	40	0	0	0	0	0	0	0		NA		NA			\sqcup	Щ
APO	_	cslc: CDOMNum	0	0	0	NA	0	0	NA	NA	0	100	100	90	0	0	0	0	90	0		NA		NA			\square	\vdash
OS		cslc: Compare	50	0	0	25	5	NA	NA		NA	0	0	0	0	0	NA	0	NA	_		NA		NA				\vdash
OS	_	cslc: Counter	90	50	0	25	10	NA	_		0	0	0	0	0	0	NA		NA	_		NA		NA				\vdash
APA	1	cslc: Decoder	90	90	100	25	0	NA			0	100	100	100	100	100	NA		NA			NA		NA		lacksquare	$\vdash \vdash$	\vdash
BZ		cslc: Enum	90	0	75	50	40		NA		0	0	0	0	70	0	NA		NA			NA		NA		lacksquare	$\vdash\vdash$	H
SP OS	2	cslc: Field cslc: Fifo	10 75	90		50 55			NA		0	0	0	0	50 95	0	NA NA		NA			NA		NA		lacksquare		H
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SP	1	cslc: Interconn cslc: ISA	80 80	70 85	85	60	90	NA	NA NA		0	0	0	0	45	0	0	90	NA NA			NA NA				lacksquare	\vdash	\vdash
AB	_	cslc: Memmap	70	0	0	50			NA		0	10	10	0	30	0	0	0	NA			NA		NA			\vdash	H
BZ		cslc: Memory	50	0	0	50	0		NA		0	0	0	0	5	0	0	0	NA		NA			NA				H
BZ	_	cslc: Pipeline	70	0	0	50	5		NA		0	0	0	0	0	0	0	0	NA			NA						\vdash
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OS		cslc: Reg	85	0	0					NA	0	0	0	0	60	0	NA		NA		NA					_		
OS		cslc: RF	86	0	0	50				NA		0	0	0	95	0	NA				NA							\Box
BZ		cslc: Sched	87	0	0	50				NA		0	0	0	0	0	NA		NA	_	NA		_					\Box
OS		cslc: State	88	0	0	50		NA			0	0	0	0	0	0	NA		NA		NA						\Box	\Box
OS		cslc: Tb	89	0	0	NA		NA			0	0	0	0	5	0	NA		NA		NA							\Box
BZ		cslc: Unit	90	90		50	_			NA		90	90	90	80	0	NA		NA		NA							
OS	<u> </u>	cslc: VC	90	0	0	50		NA			0	0	0	0	80	0	NA	_	NA		NA		_		_			
		sw lib: ASM	0	0	0	NA		NA			NA	NA	NA	NA	NA	NA	NA			NA								
		sw_lib: Csim	0	0	0	NA			_	NA		NA	NA	NA	NA	NA	NA			NA							\Box	\square
CL		hw_lib:Memcntl	0	0	0	20			NA			NA	NA	NA	NA	NA	NA			NA	_		_			i i	П	
CL		hw_lib: micro eng	0	0	0	40		-	NA		NA	NA	NA	NA	NA	NA	NA			NA	_					i i		
AV		hw_lib: Proc. Ring	0	0	0	35		-		NA		NA	NA	NA	NA	NA	NA			NA								\square
AV		hw_lib: PSCQN	84	0	0		40	_				NA			NA	NA												
	_	STATUS LEGEND put p	ercen	tage	s in t	he b	oxes																					
		not started		liah	t red																							

not started
under construction
under test
completed
intersection between
Not applicable
Divider

light red yellow light magenta green light blue dark violet black

Priorities

Low priority medium priority high priority

orange 4 violet red

File name = csl_class.ods misc/project_management/csl_class.ods

Stages	documented: Syntax	documented: data structures	documented: algorithms	documented: hw circuits	oded: CSL proto C++ lib	oded: Verilog library	coded: CSIM	oded: Command shell	coded: IDE	oded: lexer	coded: parser	coded: tree walker	coded: CSLOM	oded: CSLOM checker	oded: CSLOM elab	coded: Adaptor	coded: CDOM	coded: CDOM checker	coded: Verilog code gen	coded: VHDL code gen	coded: C++ code gen	coded: SystemC code gen	coded: document code gen
Averages crt week	52 c	17.65	16.03 c	40	16.13	0	#DIV/0!c	0	0.93	21.85 ^C	21.11	18.89	35	7.04	7.5 ^C	20.36	43.75	0.63	#DIN/0i	#DIV/0i	0	#DIN/0i	#DIV/0!
Averages prev week	52.06	13.94	12.27	40	16.13	0	#DIV/0!	0	0.74	10	10	9.63	34.26	7.04	14	12.07	21.25	0.54	#DIV/0!	#DIV/0i	0	#DIV/0!	#DIV/0!

oler	C			are	er		ler				ocation	пар	٦٧	n_gen	Je	uler							,	lib owner			
uses CSLOM: Asembler	uses CSLOM: Bus ifc	uses CSLOM: Buses	uses CSLOM: Clock	uses CSLOM: Compare	uses CSLOM: Counter	uses CSLOM: Csim	uses CSLOM: Decoder	uses CSLOM: Event	uses CSLOM: FF	uses CSLOM: Isa	uses CSLOM: Mem location	uses CSLOM: Mem map	uses CSLOM: Memory	uses CSLOM: pattern_gen	uses CSLOM: Pipeline	CSLOM: Scheduler	CSLOM: State	uses CSLOM: Unit	uses CSLOM: VC	uses cslc Compiler	slc.o	CSL Library	uses Verilog Library	CSL C++ prototype lib			
CSL	CSL	CST	CSL(CSL(CSL(CSL(CSL(CSL(CSL(CSL()TS)	CSL	CSL(CSL(CSL	CSL	CSL(CSL(CSFC	cslc	uses libcslc.o	CSL	Veri	++0	ity		
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																								NA		X	cslc: CDOM
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	\perp	1	1	1	1	1	Τ	1	1	1		1				\perp		1									clsc: Command shell
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																										X	cslc:Adaptor
																										X	cslc:Adaptor library
																			Ĺ				Ш	NA	NA		CSL pp: Aikido
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		Т					T												<u> </u>	1				SP		Х	cslc: Buses
			1																_	1				SP	4	X	cslc: Clock gen
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						_	<u> </u>		_										_							X	cslc: CDOMNum
				1			_		_										<u> </u>	1			-	SP	3		cslc: Compare
					1				_										<u> </u>	1			_	SP	2		cslc: Counter
							1											1	<u> </u>	Ļ			-	SP		X	cslc: Decoder
							1												<u> </u>	Į.				SP		X	cslc: Enum
							1												L	H	_			SP			cslc: Field
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I					-	-			-										┝	H	-			SP	1		cslc: ISA
						+-	┝		-				_			_			⊢	н	<u> </u>	+	\vdash	BZ	_	X	cslc: Memmap
			_	\vdash	\vdash	\vdash	\vdash		\vdash				_	_		_	_		\vdash		\vdash			SP	5	X	cslc: Memory
			_				\vdash			\vdash						_	_		\vdash				\vdash	SP	\vdash	Х	cslc: Pipeline
							\vdash	1					1			-		+	┝	H	<u> </u>	_		UN SP			cslc: Procon cslc: Reg
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											\vdash	\vdash							\vdash	┢	_		_		NA		hw_lib: micro eng
							\vdash		\vdash	\vdash									\vdash				_		NA		hw_lib: Proc. Ring
			\vdash	\vdash			\vdash		\vdash	T							\vdash		\vdash		I		_		NA		hw_lib: PSCQN
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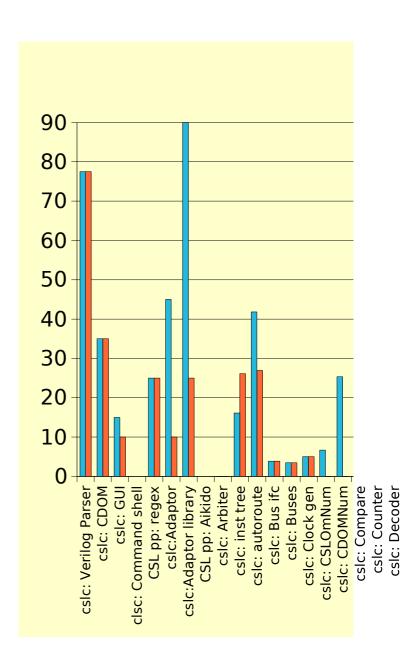
Priorities
Low priority
medium priority
high priority

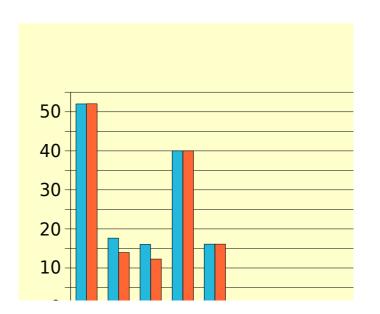
Averages crt vAverages prev week

verages crt	
77.5	77.5
35	35
15	10
25	25
45	10
90	25
#DIV/0!	#DIV/0!
0	0
16.11	26.11
41.82	26.92
3.85	3.85
3.46	3.46
5	5
6.67	0
25.33	0
6.67	6.67
13.46	13.46
68.85	68.85
19.23	13.85
27.31	27.31
24.31	19.69
58.93	58.93
31.79	31.79
17.33	17.33
7	7
8.93	8.93
6.92	6.92
20.38	20.38
24.69	20.08
10.54	10.54
10.62	10.62
7.83	7.83
58.62	16.92
23.08	23.08
0	0
0	0
3.33	3.33
6.67	6.67
5.83	5.83
27.33	27.33

ercentages in the boxes

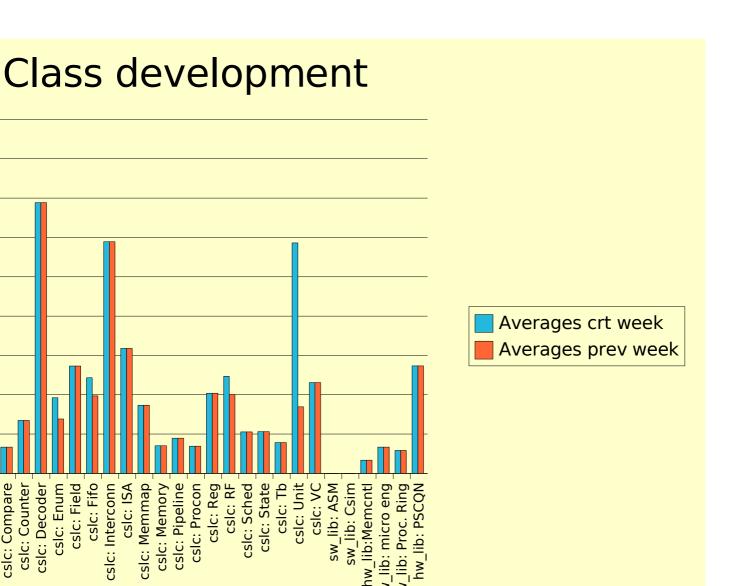
Overall project average 20.45

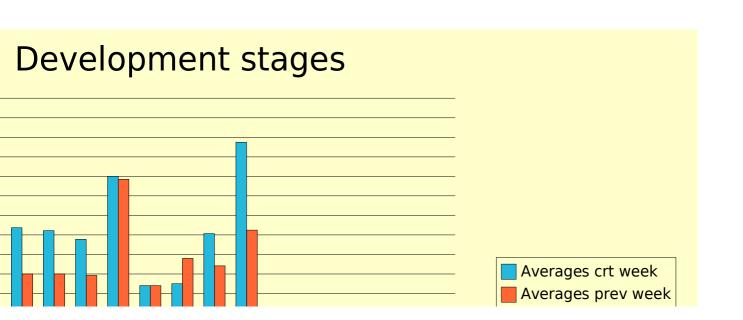




documented: Syntax documented: data structures documented: algorithms documented: hw circuits coded: IDE coded: CSIM coded: Command shell coded: CSL proto C++ lib coded: Verilog library

coded: lexer





coded: lexer

coded: parser

coded: tree walker coded: CSLOM coded: CSLOM checker

coded: CSLOM elab coded: Adaptor

coded: CDOM checker

coded: CDOM

coded: Verilog code gen

coded: VHDL code gen

coded: C++ code gen

coded: SystemC code gen

coded: document code gen

cslc owner	cslc owner	CSL CLASS	documented: Syntax	documented: data structures	documented: algorithms	documented: hw circuits	coded: CSL proto C++ lib	coded: Verilog library	coded: CSIM	coded: Command shell	coded: IDE	coded: lexer	coded: parser	coded: tree walker	coded: CSLOM	coded: CSLOM checker	coded: CSLOM elab	coded: Adaptor	coded: CDOM	coded: CDOM checker	coded: Verilog code gen	coded: VHDL code gen	coded: C++ code gen	coded: SystemC code gen	coded: document code gen	uses CSLOM: CSL Info class	uses CSLOM: CSL Unit	uses CSLOM: Arbiter
NA		cslc: Verilog Parser	100	NA	NA	NA	NA	NA	NΑ	NA	NA	70	70	70	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA			Ш
APA		cslc: CDOM	NA	25	25	NA	NA	NA	NΑ	NA	NA	NA	NA	NA	NA	NA	NA	NA	85	5	NA	NA	NA	NA	NA			
CP		cslc: GUI	NA	NA	NA	NA	NA	NA	_	NA	10	NA	NA	NA	NA	NA	NA	NA	NA	_	NA	-		NA			1	
os		clsc: Command shell	5	NA	NA	NA	NA	-	NA	0	0	NA	NA	NA	NA	NA	NA	NA	NA		NA	-		_			1	
BZ		CSL pp: regex	25	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	NA		NA	_		NA				Ш
APA		cslc:Adaptor	NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	10	NA		NA	_		NA			\square	\square
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os		CSL pp: Aikido	NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	NA		NA			_	NA		Ш	
BZ		cslc: Arbiter	0	NA	NA	0	0	NA			NA	0	0	0	0	0	0	0	NA		NA			NA			\square	
BZ	-	cslc: inst tree	NA	25	25	NA	NA	NA	NA	NA	5	NA	NA	NA	90	0	90	0	0	0	NA	-		NA			Н	\vdash
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BZ		cslc: Bus ifc	25	0	0	25	0	NA	NA		0	0	0	0	0	0	NA	0	NA	0	NA	-		NA				\vdash
BZ	_	cslc: Buses	20	0	0	25	0	NA	NA	NA	0	0	0	0	0	0	NA	0	NA	0	NA	-		NA			${f H}$	\vdash
BZ		cslc: Clock gen	40	0	0	25	0	NA		NA	0	0	0	0	0	0	NA	0	NA	0	NA	-		NA			$\vdash\vdash$	$\vdash\vdash$
APO		cslc: CSLOmNum	0	0	0	NA	0	0	NA	NA	0	0	0	0	0	0	0	0	0	0	NA			NA			$\vdash\vdash$	$\vdash\vdash$
APO		cslc: CDOMNum	0	0	0	NA	0	0	NA	NA	0	0	0	0	0	0	0	0	0	0	NA			NA			$\vdash\vdash$	H
OS OS	_	cslc: Compare cslc: Counter	50	50	0	25 25	5 10	NA	NA	NA NA	NA 0	0	0	0	0	0	NA NA	0	NA	0	NA NA			NA				H
APA	_	cslc: Counter	90 90	90	100	25	0	NA	NA NA		0	100	100	100	100	100	NA		NA NA	0	NA	-		NA NA				\vdash
BZ	-	cslc: Enum	90	0	0	50		NA	NA	NA	0	0	0	0	0	0	NA	0	NA	0	NA	-		NA			\vdash	H
SP		cslc: Field	10	90		50		NA	NA	NA	0	0	0	0	50	0	NA	0	NA	0	NA	_		NA			H	Н
OS	3	cslc: Fifo	75	0	0	55	1	NA	NA	NA	0	0	0	0	95	0	NA	30	NA	0	NA	_		NA				\vdash
BZ	1	cslc: Interconn	80	70	70	50	5	NA	NA	NA	0	90	90	90	90	90	0	90	NA	10	NA			NA				\vdash
SP	1	cslc: ISA	80	85	85	60	90	NA	NA	NA	0	0	0	0	45	0	0	0	NA	0	NA			NA			H	\vdash
AB	1	cslc: Memmap	70	0	0	50		NA	NA	NA	0	10	10	0	30	0	0	0	NA	0	NA			NA			\vdash	\vdash
BZ	2	cslc: Memory	50	0	0	50	0	NA	NA	NA	0	0	0	0	5	0	0	0	NA	0	NA	-		NA				Н
BZ	_	cslc: Pipeline	70	0	0	50	5	NA	NA		0	0	0	0	0	0	0	0	NA	0		NA						\square
OS		cslc: Procon	83	0	0	NA	0	NA		NA	0	0	0	0	0	0	NA	0	NA	0		NA						П
OS		cslc: Reg	85	0	0	50	70	NA	NA	NA	0	0	0	0	60	0	NA	0	NA	0		NA						一
OS		cslc: RF	86	0	0	50	_	NA				0	0	0	95	0	NA					NA					T	П
BZ		cslc: Sched	87	0	0	50		NΑ				0	0	0	0	0	NA		NA			NA						\Box
os		cslc: State	88	0	0	50		NA				0	0	0	0	0	NA		NA			NA					П	П
os		cslc: Tb	89	0	0	NA		NA				0	0	0	5	0	NA		NA			NΑ						П
BZ		cslc: Unit	90	0	0	50	_	NA				0	0	0	80	0	NA		NA			NA					T	П
os		cslc: VC	90	0	0	50			NA		0	0	0	0	80	0	NA	0	NA	_		NA						
		sw_lib: ASM	0	0	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA			
		sw_lib: Csim	0	0	0	NA	0	NΑ	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA			П
CL	_	hw_lib:Memcntl	0	0	0	20	0		NΑ			NA	NA	NA	NA	NA	NA	NA		_		NΑ					П	
CL	_	hw_lib: micro eng	0	0	0	40			NΑ			NA	NA	NA	NA	NA	NA			NA	_							
AV		hw_lib: Proc. Ring	0	0	0	35	0	_		NA			NA	NA	NA	NA	NA			NA								
AV	-	hw_lib: PSCQN	84	0	0	40	40	_				NA	NA	NA	NA	NA	NA											
		STATUS LEGEND put p	ercen	tage	s in t	he b	oxes	5																				
		not started		ligh	t red																							

light red yellow light magenta green light blue dark violet black

Priorities

Low priority medium priority high priority

orange 4 violet red

File name = csl_class.ods misc/project_management/csl_class.ods 25

Stages	documented: Syntax	documented: data structures	documented: algorithms	documented: hw circuits	coded: CSL proto C++ lib	oded: Verilog library	coded: CSIM	oded: Command shell	coded: IDE	oded: lexer	coded: parser	coded: tree walker	coded: CSLOM	coded: CSLOM checker	coded: CSLOM elab	coded: Adaptor	coded: CDOM	coded: CDOM checker	coded: Verilog code gen	coded: VHDL code gen	coded: C++ code gen	coded: SystemC code gen	coded: document code gen
Averages crt week	52.06	13.94	12.27	40	16.13	0	#DIV/0!	0	0.74	10	10	9.63	34.26	7.04	14	12.07	21.25	0.54	#DIN/0i	#DIV/0i	0	#DIN/0i	#DIV/0i
Averages prev week	52.06	13.94	12.27	40	16.13	0	#DIV/0!	0	0.74	10	10	9.63	32.41	7.04	7.5	12.07	21.25	0.37	#DIV/0	#DIV/0!	0	#DIV/0!	#DIV/0!

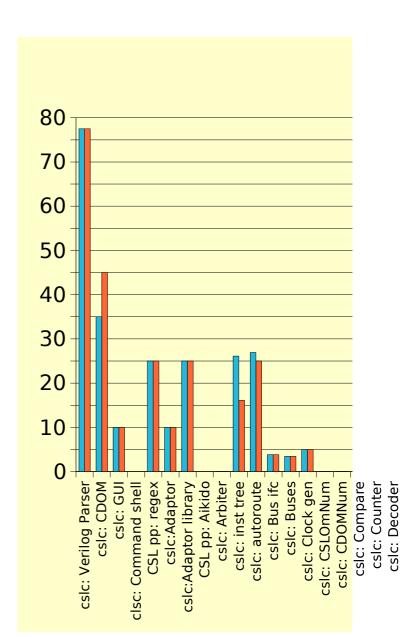
nbler	ifc	Si	_	pare	ıter		oder	ıt			location	ı map	iory	ern_gen	line	aduler	o)			L			ry	oe lib owner		
uses CSLOM: Asembler	uses CSLOM: Bus ifc	uses CSLOM: Buses	uses CSLOM: Clock	uses CSLOM: Compare	uses CSLOM: Counter	uses CSLOM: Csim	uses CSLOM: Decoder	uses CSLOM: Event	uses CSLOM: FF	uses CSLOM: Isa	uses CSLOM: Mem location	uses CSLOM: Mem map	uses CSLOM: Memory	uses CSLOM: pattern_gen	uses CSLOM: Pipeline	uses CSLOM: Scheduler	uses CSLOM: State	uses CSLOM: Unit	uses CSLOM: VC	uses cslc Compiler	uses libcslc.o	uses CSL Library	uses Verilog Library	CSL C++ prototype lib	;y	
es (es (es (es (es (es (es (es (es (es (es (es (es (es (es (es (es (es (es (es (es (es	es (es \	j. O	priority	
ns	sn	ns	sn	sn	ns	sn	šn	ns	sn	sn	sn	ns	ns	sn	ns	sn	sn	ns	ns	ns	sn	sn				CSL CLASS
					<u> </u>	₩	├		_	_														NA		cslc: Verilog Parser
																				-				NA		cslc: CDOM
	1	+	1	1	1	1	H.	1	1	+	1	1	1	1	+	+	1	1		_				NA	NA	cslc: GUI
1				1	Н		1	1	1	1	Н						1	1						NI A	NI A	clsc: Command shell
					-	┢	-													_			Н	NA	NA	CSL pp: regex
					-	-	-													_			Н			cslc:Adaptor
					-	-	-													-			Н	.		cslc:Adaptor library
						\vdash	⊢		_											H			Н	NA SP	NA	CSL pp: Aikido
					\vdash	\vdash	┝													-			Н		N I A	cslc: Arbiter
					-	\vdash	┢												Н	_			_	NA		cslc: inst tree
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		÷				-	H	1											Н			1		SP		cslc: Bus ifc
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						\vdash	-																Н	CD		cslc: CDOMNum
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					\vdash	\vdash	-		\vdash											÷		÷		BZ	1	
					\vdash	┢	┢													÷		÷		SP	5	cslc: Memmap
			\vdash	\vdash	\vdash	\vdash	\vdash		\vdash			\vdash				<u> </u>	\vdash		\vdash				\vdash	SP)	cslc: Memory cslc: Pipeline
			\vdash	\vdash		\vdash	\vdash									_	 		Н	÷				UN	Н	cslc: Procon
							\vdash												\vdash				H	SP		cslc: Procon
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				\vdash	\vdash	\vdash	\vdash			\vdash	\vdash								H					BZ		cslc: State
						\vdash			\vdash	\vdash	\vdash	\vdash	1			_			1				-	NA		cslc: Tb
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			<u> </u>			1						.					l			÷				OB	_	cslc: VC
					П	П																		NA		sw lib: ASM
				\vdash	\vdash											\vdash			\vdash				_		NA	sw_lib: Csim
											\vdash								\vdash				-		NA	hw_lib:Memcntl
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_			-	\vdash			\vdash		\vdash			\vdash				<u> </u>	-		\vdash						NA	hw_lib: Proc. Ring
			\vdash	\vdash			\vdash					\vdash					\vdash		\vdash		<u> </u>		_		NA NA	hw_lib: PSCQN
				_	_	_					_					_	_							T17-T	TVA	STATUS LEGEND put p
																										not started
																										under construction

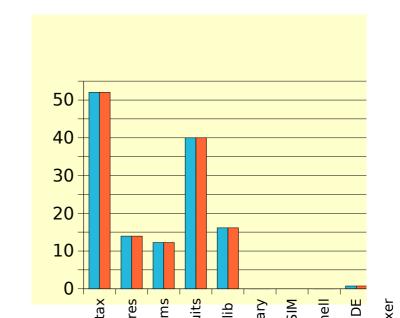
Priorities
Low priority
medium priority
high priority

Averages crt wAverages prev week

77.5	77.5
35	45
10	10
25	25
10	10
25	25
#DIV/0!	#DIV/0!
0	0
26.11	16.11
26.92	25
3.85	3.85
3.46	3.46
5	5
0	0
0	0
6.67	6.67
13.46	13.46
68.85	68.85
13.85	13.85
27.31	27.31
19.69	19.69
58.93	58.93
31.79	31.79
17.33	17.33
7	7
8.93	8.93
6.92	6.92
20.38	20.38
20.08	20.08
10.54	10.54
10.62	10.62
7.83	7.83
16.92	16.92
23.08	23.08
0	0
0	0
3.33	3.33
6.67	6.67
5.83	5.83
27.33	27.33
rcentages in t	the boxes

Overall project average 16.82





nent/csl_class.ods

coded: lexe

coded: CSIN coded: Command she

coded: CSL proto C++ lib coded: Verilog librar

-

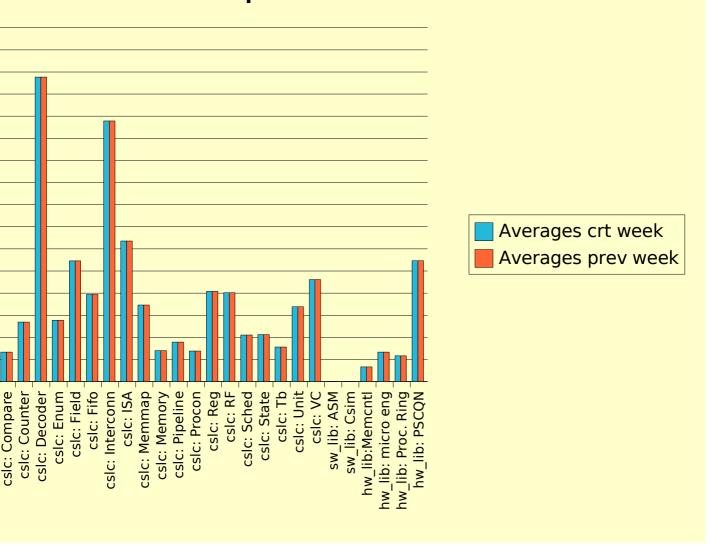
documented: hw circuit

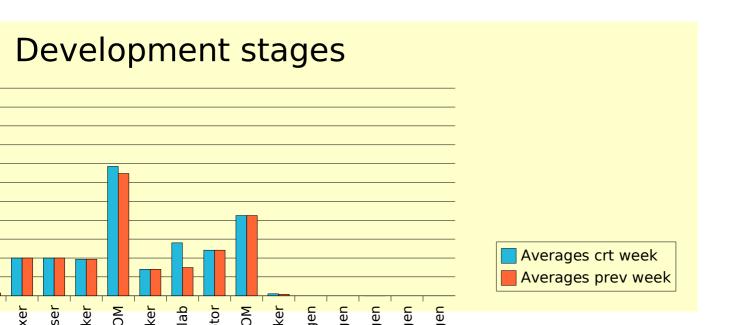
documented: algorithm

documented: data structure

documented: Syntax

Class development





coded: lexe

coded: parse

coded: tree walke coded: CSLON coded: CSLOM checke

coded: CSLOM elal coded: Adapto coded: CDOM checke

coded: CDON

coded: Verilog code ger

coded: VHDL code ger

coded: C++ code ger

coded: SystemC code ger

coded: document code ger

cslc owner	cslc owner	CSL CLASS	documented: Syntax	documented: data structures	documented: algorithms	documented: hw circuits	coded: CSL proto C++ lib	coded: Verilog library	coded: CSIM	coded: Command shell	coded: IDE	coded: lexer	coded: parser	coded: tree walker	coded: CSLOM	coded: CSLOM checker	coded: CSLOM elab	coded: Adaptor	coded: CDOM	coded: CDOM checker	coded: Verilog code gen	coded: VHDL code gen	coded: C++ code gen	coded: SystemC code gen	coded: document code gen	uses CSLOM: CSL Info class	uses CSLOM: CSL Unit	uses CSLOM: Arbiter
NA		cslc: Verilog Parser	100	NA	NA	NA	NA	NA	NA	NA	NA	70	70	70	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA			
APA		cslc: CDOM	NA	25	25	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	85	NA	NA	NA	NA	NA	NA			
CP		cslc: GUI	NA	NA	NA	NA	NA	NA	NA	NA	10	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA			1
OS		clsc: Command shell	5	NA	NA	NA	NA	NA	NA	0	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		1	1
BZ		CSL pp: regex	25	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	1		
APA		cslc:Adaptor	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	10	NA	NA	NA	NA	NA	NA	NA			
APA		cslc:Adaptor library	NA	NA	NA	NA	NA	NA	NΑ	NA	NA	NA	NA	NA	NA	NA	NA	25	NA	NA	NΑ	NA	NA	NA	NA			Ш
OS		CSL pp: Aikido	NA	NA	NA	NA	NA	NA	NΑ	NA	NA	NA	NA	NA	NA	NA	NA	NA	NΑ	NA	NΑ	NA	NA	NA	NA			
BZ		cslc: Arbiter	0	NA	NA	0	0	NA	NA	NA	NA	0	0	0	0	0	0	0	NA	0	NA	NA	NA	NA	NA	1		
ΒZ		cslc: inst tree	NA	25	25	NA	NA	NA	NA	NA	5	NA	NA	NA	65	0	25	0	0	0	NA	NA	NA	NA	NA			Ш
ΒZ		cslc: autoroute	70	25	25	NA	0	NA	NA	NA	5	0	0	0	75	0	50	75	NA	0	NA	NA	NA	NA	NA			Ш
BZ		cslc: Bus ifc	25	0	0	25	0	NA	NA	NA	0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA	NA	NA			1
BZ		cslc: Buses	20	0	0	25	0	NA	NA	NA	0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA	NA	NA			П
BZ	2	cslc: Clock gen	40	0	0	25	0	NA	NA	NA	0	0	0	0	0	0	NA	0	NA	0	NA	NA		NA			П	П
APO		cslc: CSLOmNum	0	0	0	NA	0		NΑ		0	0	0	0	0	0	0	0	0	0	NA	NA	NA	NA	NA		П	П
APO		cslc: CDOMNum	0	0	0	NA	0	0	NA	NA	0	0	0	0	0	0	0	0	0	0	NA	NA	NA	NA	NA			П
OS	2	cslc: Compare	50	0	0	25	5	NA	NΑ	NA	NA	0	0	0	0	0	NA	0	NA	0	NA	NA	NA	NA	NA		П	П
OS		cslc: Counter	90	50	0	25	10	NA	NA	NA	0	0	0	0	0	0	NA	0	NA	0	NA	NA		NA				П
APA	1	cslc: Decoder	90	90	100	25		NA	NA	NA	0	100	100	100	100	100	NA	90	NA	0	NA	NA	NA	NA	NA			П
BZ		cslc: Enum	90	0	0	50	40	NA	NA	NA	0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA	NA	NA		П	П
SP		cslc: Field	10	90	75	50	80	NA	NΑ	NA	0	0	0	0	50	0	NA	0	NA	0	NA	NA	NA	NA	NA		П	П
os	3	cslc: Fifo	75	0	0	55	1	NA	NΑ	NA	0	0	0	0	95	0	NA	30	NΑ	0	NΑ	NA	NA	NA	NA		1	П
BZ	1	cslc: Interconn	80	70	70	50	5	NA	NΑ	NA	0	90	90	90	90	90	0	90	NA	10	NΑ	NΑ	NA	NA	NA			П
SP	1	cslc: ISA	80	85	85	60	90	NA	NΑ	NA	0	0	0	0	45	0	0	0	NA	0	NΑ	NA	NΑ	NA	NA			П
AB	1	cslc: Memmap	70	0	0	50	90	NA	NΑ	NA	0	10	10	0	30	0	0	0	NΑ	0	NΑ	NA	0	NA	NA	1		П
BZ	_	cslc: Memory	50	0	0	50	0	NA	NΑ	NA	0	0	0	0	5	0	0	0	NΑ	0	NΑ	NA	0	NA	NA		1	П
BZ	2	cslc: Pipeline	70	0	0	50	5	NA	NA	NA	0	0	0	0	0	0	0	0	NA	0	NΑ	NA	NΑ	NA	NA			П
OS	?	cslc: Procon	83	0	0	NA	0	NA	NΑ	NA	0	0	0	0	0	0	NA	0	NA	0	NΑ	NA	NΑ	NA	NA	1		П
OS		cslc: Reg	85	0	0	50	70				0	0	0	0	60	0	NA	0	NA				NΑ			1		П
OS		cslc: RF	86	0	0	50	0	NA	NΑ	NA	0	0	0	0	95	0	NA	30	NA	0	NΑ	NΑ	NΑ	NA	NA	1		П
BZ		cslc: Sched	87	0	0	50	0	NA	NΑ	NA	0	0	0	0	0	0	NA	0	NA	0	NΑ	NA	NΑ	NA	NA			П
ОВ		cslc: State	88	0	0	50	0	NA	NΑ	NA	0	0	0	0	0	0	NA	0	NA	0	NΑ	NΑ	NΑ	NA	NA			П
ОВ		cslc: Tb	89	0	0	NA	0	NA	NA	NA	0	0	0	0	5	0	NA	0	NA	0	NA	NA	NA	NA	NA	1	1	П
BZ		cslc: Unit	90	0	0	50	0	NA	NA	NA	0	0	0	0	80	0	NA	0	NA	0	NA	NA	NA	NA	NA		1	П
ОВ		cslc: VC	90	0	0	50	80	NA	NA	NA	0	0	0	0	80	0	NA	0	NA	0	NA	NA	NA	NA	NA			
		sw_lib: ASM	0	0	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA						1		
		sw_lib: Csim	0	0	0	NA	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA			NA								\square
CL		hw_lib:Memcntl	0	0	0	20	0	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	1		
CL		hw_lib: micro eng	0	0	0	40	0	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	1		
AV		hw_lib: Proc. Ring	0	0	0	35				NA		NA	NA	NA	NA	NA	NA			NA							П	\square
AV		hw_lib: PSCQN	84	0	0	40	40						_	NA	NA	NA	NA		_	_	_	_	_					
		STATUS LEGEND put p	ercen	tage	s in t	he h	OXES																					
		not started	3. 56.1	-	t rad		2	•																				

light red
yellow
light magenta
green
light blue
dark violet
black

Priorities

Low priority medium priority high priority

orange 4 violet red

File name = csl_class.ods misc/project_management/csl_class.ods 25

Stages	documented: Syntax	documented: data structures	documented: algorithms	documented: hw circuits	oded: CSL proto C++ lib	oded: Verilog library	coded: CSIM	oded: Command shell	coded: IDE	oded: lexer	coded: parser	coded: tree walker	coded: CSLOM	oded: CSLOM checker	oded: CSLOM elab	coded: Adaptor	coded: CDOM	coded: CDOM checker	oded: Verilog code gen	coded: VHDL code gen	coded: C++ code gen	coded: SystemC code gen	coded: document code gen
Averages crt week	52.06 d	13.94 d	12.27 d	40 d	16.13 c	0	#DIV/0!c	0	0.74 c	10	10 C	o 63	32.41 ^C	7.04 ^C	7.5 ^C	12.07 ^C	21.25 C	0.37 ^C	#DIV/0i	#DIV/0!	0	#DIV/0i	#DIV/0!
Averages prev week	52.06	13.94	12.27	39.6	16.13	0	#DIV/0!	0	0.74	10	10	6.63	32.41	7.04	7.5	12.07	21.25	0.37	#DIV/0	#DIV/0!	0	#DIV/0!	#DIV/0!

Asembler	3us ifc	guses	Clock	Compare	Counter	Ssim	Decoder	Event	H	sa	uses CSLOM: Mem location	CSLOM: Mem map	demory	oattern_gen	ipeline	CSLOM: Scheduler	State	Jnit)/C	piler		ary	ibrary	otype lib owne			
uses CSLOM: Asembler	uses CSLOM: Bus ifc	uses CSLOM: Buses	uses CSLOM: Clock	uses CSLOM: Compare	uses CSLOM: Counter	uses CSLOM: Csim	uses CSLOM: Decoder	uses CSLOM: Event	uses CSLOM: FF	uses CSLOM: Isa	s CSLOM: I	s CSLOM: I	s CSLOM: Memory	s CSLOM: pattern	s CSLOM: Pipeline	s CSLOM:	s CSLOM: State	uses CSLOM: Unit	s CSLOM: VC	uses cslc Compile	uses libcslc.o	s CSL Library	uses Verilog Library	CSL C++ prototype lib	priority		
nse	nse	nse	nse	nse	nse	nse	nse	nse	nse	nse	nse	nses	nses	nses	nses	nses	nses	nse	nses	nse	nse	nses	nse	CSI	pric		CSL CLASS
																								NA			cslc: Verilog Parser
																								NA	NA		cslc: CDOM
\perp	1	1	1	1	1	1	1	1	1	1	1	-	1	-	\pm	\mathbf{I}	-	1	1					NA	NA		cslc: GUI
1	1	1	1	1	1	1	1	1	1	1	1	1	1	Τ	\mathbf{I}	1	1	1	1								clsc: Command shell
																								NA	NA		CSL pp: regex
																											cslc:Adaptor
																											cslc:Adaptor library
																								NA	NA		CSL pp: Aikido
	$ldsymbol{ldsymbol{ldsymbol{ldsymbol{eta}}}$					_					1							1	$oxed{oxed}$	1	<u> </u>	$ldsymbol{ld}}}}}}$	Ш	SP			cslc: Arbiter
																							-	NA			cslc: inst tree
																								NA	NA		cslc: autoroute
	1	1					1	1	1									1				1		SP			cslc: Bus ifc
		1					Τ													1				SP			cslc: Buses
			1																	1				SP	4		cslc: Clock gen
																											cslc: CSLOmNum
																											cslc: CDOMNum
				T																T				SP	3		cslc: Compare
					1															Τ		1		SP	2		cslc: Counter
							Τ											1		1				SP			cslc: Decoder
							1													1		1		SP			cslc: Enum
							1													1		1		SP			cslc: Field
				1	1		1		1				1					1		1		1		ΒZ			cslc: Fifo
							1			1										1		1		SP	1		cslc: Interconn
-							1													1		1		SP	1		cslc: ISA
												1								1		1		ΒZ			cslc: Memmap
											1									1		1		SP	5		cslc: Memory
															1					1		1		SP			cslc: Pipeline
					-1			1			1		1					1		1		-1		UN			cslc: Procon
					1				1									1		1		1		SP			cslc: Reg
				1			1		1		1		1	1				1		1		1		SP			cslc: RF
																1		1		1			-	UN			cslc: Sched
																	1			1			-	ΒZ			cslc: State
			-1	1	1		1	1					1				1	1	1	1	oxdot			NA			cslc: Tb
																		1		1				UN			cslc: Unit
																			1	1		1		ОВ			cslc: VC
1																				1			_	NA			sw_lib: ASM
						1																		NA			sw_lib: Csim
				1	1		1		1				1			1						1		NA			hw_lib:Memcntl
1					1									1	1			1				1	-	NA			hw_lib: micro eng
																								NA			hw_lib: Proc. Ring
																				L				NA	NA		hw_lib: PSCQN
																											STATUS LEGEND put p
																										ı	not started

Priorities
Low priority
medium priority
high priority

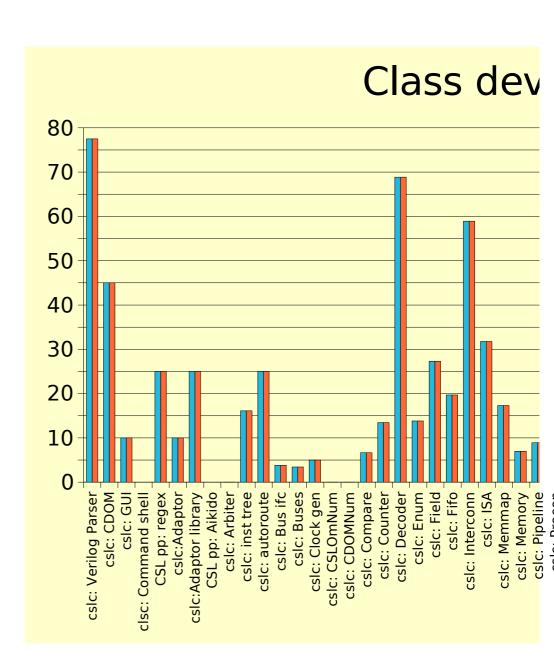
File name = csl_class.c misc/project_managen

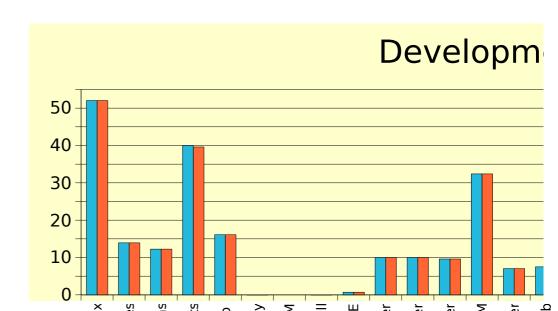
Averages crt wAverages prev week

Averages crt v	Averages prev
77.5	77.5
45	45
10	10
25	25
10	10
25	25
#DIV/0!	#DIV/0!
0	0
16.11	16.11
25	25
3.85	3.85
3.46	3.46
5	5
0	0
0	0
6.67	6.67
13.46	13.46
68.85	68.85
13.85	13.85
27.31	27.31
19.69	19.69
58.93	58.93
31.79	31.79
17.33	17.33
7	7
8.93	8.93
6.92	6.92
20.38	20.38
20.08	20.08
10.54	10.54
10.62	10.62
7.83	7.83
16.92	16.92
23.08	23.08
0	0
0	0
3.33	3.33
6.67	5
5.83	5.83
27.33	27.33

ercentages in the boxes

Overall project average 16.56





oas nent/csl_class.ods

coded: CSLOM elab

coded: parser

coded: CSL proto C++ lib

documented: hw circuits

documented: algorithms

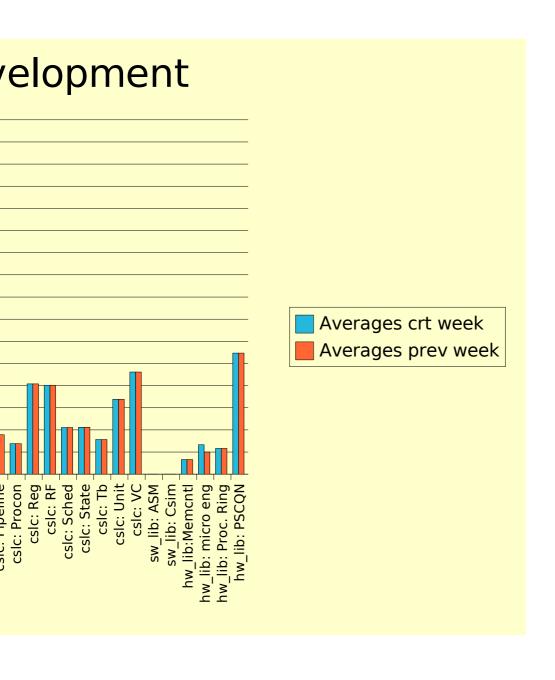
documented: data structures

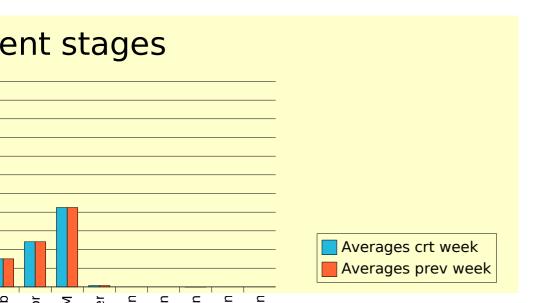
documented: Syntax

coded: Verilog library

coded: CSIM

coded: Command shell coded: IDE coded: lexer coded: tree walker coded: CSLOM coded: CSLOM checker





coded: CSLUM elab

coded: Adaptor

coded: CDOM

coded: CDOM checker

coded: Verilog code gen

coded: VHDL code gen

coded: SystemC code gen

coded: C++ code gen

coded: document code gen

cslc owner	cslc owner	CSL CLASS	documented: Syntax	documented: data structures	documented: algorithms	documented: hw circuits	coded: CSL proto C++ lib	coded: Verilog library	coded: CSIM	coded: Command shell	coded: IDE	coded: lexer	coded: parser	coded: tree walker	coded: CSLOM	coded: CSLOM checker	coded: CSLOM elab	coded: Adaptor	coded: CDOM	coded: CDOM checker	coded: Verilog code gen	coded: VHDL code gen	coded: C++ code gen	coded: SystemC code gen	coded: document code gen	uses CSLOM: CSL Info class	uses CSLOM: CSL Unit	uses CSLOM: Arbiter
NA		cslc: Verilog Parser	100	NA	NA	NA	NA	NA			NA	70	70	70	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA			
APA		cslc: CDOM	NA	25	25	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	85	NA	NA	NA	NA	NA	NA			
CP		cslc: GUI	NA	NA	NA	NA	NA	NA	NΑ	NA	10	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA			1
OS		clsc: Command shell	5	NA	NA	NA	NA	NA	NΑ	0	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NΑ	NA	NA	NA		1	1
BZ		CSL pp: regex	25	NA	NA	NA	NA	NA	NΑ	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	1	Ш	
APA		cslc:Adaptor	NA	NA	NA	NA	NA	NA	NΑ	NA	NA	NA	NA	NA	NA	NA	NA	10	NA	NA	NA	NA	NA	NA	NA		Ш	
APA		cslc:Adaptor library	NA	NA	NA	NA	NA	NA	NΑ	NA	NA	NA	NA	NA	NA	NA	NA	25	NA	NA	NA	NA	NA	NA	NA		Ш	
OS		CSL pp: Aikido	NA	NA	NA	NA	NA	NA	NΑ	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		Ш	
BZ		cslc: Arbiter	0	NA	NA	0	0	NA	_	NA	NA	0	0	0	0	0	0	0	NA	0		NA		NA		1	Ш	
BZ		cslc: inst tree	NA	25	25	NA	NA	NA	_		5	NA	NA	NA	65	0	25	0	0	0		NA		NA			Ш	
BZ		cslc: autoroute	70	25	25	NA	0	NA	NΑ	NA	5	0	0	0	75	0	50	75	NA	0	NA	NA	NA	NA	NA			_
BZ		cslc: Bus ifc	25	0	0	25	0	NA	NΑ	NA	0	0	0	0	0	0	NA	0	NA	0	NA	NΑ	NA	NA	NA		1	
BZ		cslc: Buses	20	0	0	25	0	NA	NΑ	NA	0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA	NA	NA		Ш	
BZ	2	cslc: Clock gen	40	0	0	25	0	NA	NΑ	NA	0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA	NA	NA		Ш	_
APO		cslc: CSLOmNum	0	0	0	NA	0	0	NA	NA	0	0	0	0	0	0	0	0	0	0		NA		NA	NA		Ш	
APO		cslc: CDOMNum	0	0	0	NA	0	0	NA	NA	0	0	0	0	0	0	0	0	0	0		NA		NA			Ш	
OS	2	cslc: Compare	50	0	0	25	5	NA	NA		NA	0	0	0	0	0	NA	0	NA			NA					Ш	
OS	1	cslc: Counter	90	50	0	25	10	NA			0	0	0	0	0	0	NA	0	NA			NA		NA		1	4	
APA	1	cslc: Decoder	90	90	100	25		NA	NΑ		0	100	_	100	100		NA	90	NA			NA		NA			\sqcup	_
BZ		cslc: Enum	90	0	0	50	40	NA	NA	NA	0	0	0	0	0	0	NA	0	NA					NA	NA		$\vdash \vdash$	
SP	_	cslc: Field	10	90	75	50	80	NA	NA	NA	0	0	0	0	50	0	NA	0	NA	_		_						\dashv
OS	3	cslc: Fifo	75	0	0	55	1	NA	NA	NA	0	0	0	0	95	0	NA	30							NA			_
BZ	1	cslc: Interconn	80	70	70	50	5	NA	NA	NA	0	90	90	90	90	90	0	90	NA	10		NA			NA		\vdash	\dashv
SP	1	cslc: ISA	80	85	85	60	90	NA	NA		0	0	0	0	45	0	0	0	NA			NA					$\vdash\vdash$	-
AB	1	cslc: Memmap	70	0	0	50	90	NA	NA		0	10	10	0	30	0	0	0	NA			NA		NA				-
BZ	2	cslc: Memory	50	0	0	50	<u>5</u>	NA			0	0	0	0	5	0	0	0	NA			NA		NA	NA		-	_
BZ OS	2	cslc: Pipeline	70	0		50 NA		NA	NA		_	0	0	0	0	0		0	NA			NA		NA	NA		$\vdash\vdash$	\dashv
OS	:	cslc: Procon cslc: Reg	83 85	0	0	50				NA NA	0	0	0	0	60	0	NA NA	0	NA NA	_			NA NA					\dashv
OS		cslc: RF	86	0	0	50	_			NA	0	0	0	0	95	0		30					NA					\dashv
BZ		cslc: Sched	87	0	0	50				NA	0	0	0	0	0	0	NA	0	NA	_			NA					\dashv
OB		cslc: State	88	0	0	50				NA	0	0	0	0	0	0	NA	0	NA				NA				\vdash	-
ОВ		cslc: Tb	89	0	0	NA				NA	0	0	0	0	5	0	NA	0	NA				NA					-
BZ		cslc: Unit	90	0	0	50				NA	0	0	0	0	80	0	NA	0	NA				NA			'	Ħ	\dashv
OB		cslc: VC	90	0	0	50			NA		0	0	0	0	80	0	NA	0	NA	_		_	NA					
-		sw lib: ASM	0	0	0	NA		NA			NA	NA	NA	NA	NA	NA	NA			NA								
		sw lib: Csim	0	0	0	NA				NA		NA	NA	NA	NA	NA	NA			NA							П	\dashv
CL		hw_lib:Memcntl	0	0	0	20				NA		NA	NA	NA	NA	NA	NA			NA								
CL		hw lib: micro eng	0	0	0	30		_		NA		NA	NA	NA	NA	NA	NA		_	NA							П	
AV		hw lib: Proc. Ring	0	0	0	35				NA		NA	NA	NA	NA	NA	NA			NA							П	\dashv
AV		hw_lib: PSCQN	84	0	0		40			-		NA	_	NA	NA	_	NA		_	_		_					口	\Box
		STATUS LEGEND put p																									_	
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light red yellow light magenta green light blue dark violet black

Priorities

Low priority medium priority high priority orange 4 violet red

File name = csl_class.ods misc/project_management/csl_class.ods 25

52.06	documented: Syntax
13.94	documented: data structures
12.27	documented: algorithms
39.6	documented: hw circuits
16.13	coded: CSL proto C++ lib
C	coded: Verilog library
#DIV/0!	coded: CSIM
0	coded: Command shell
0.74	coded: IDE
10	coded: lexer
10	coded: parser
9.63	coded: tree walker
32.41	coded: CSLOM
7.04	coded: CSLOM checker
7.5	coded: CSLOM elab
12.07	coded: Adaptor
21.25	coded: CDOM
0.37	coded: CDOM checker
#DIV/0!	coded: Verilog code gen
#DIV/0!	coded: VHDL code gen
0	coded: C++ code gen
#DIV/0!	coded: SystemC code gen
#DIV/0i code	coded: document code gen

uses CSLOM: Asembler	uses CSLOM: Bus ifc	uses CSLOM: Buses	uses CSLOM: Clock	uses CSLOM: Compare	uses CSLOM: Counter	uses CSLOM: Csim	uses CSLOM: Decoder	uses CSLOM: Event	uses CSLOM: FF	uses CSLOM: Isa	uses CSLOM: Mem location	uses CSLOM: Mem map	uses CSLOM: Memory	uses CSLOM: pattern_gen	uses CSLOM: Pipeline	uses CSLOM: Scheduler	uses CSLOM: State	uses CSLOM: Unit	uses CSLOM: VC	uses cslc Compiler	uses libcslc.o	uses CSL Library	uses Verilog Library	CSL C++ prototype lib owner	priority	CSL CLASS
							_				_	_										_		NA		cslc: Verilog Parser
																								NA		cslc: CDOM
1	1	1	1	1	1	1	1	1	1	1	1	1	1	-	-	=	1	1	1					NA	NA	cslc: GUI
-	1	1	-	1	1		1	1	1	1	1	\perp	1	\perp	\pm	\pm	_	1	1							
																								NA	NA	CSL pp: regex
																								NA	NA	CSL pp: Aikido
											\mathbf{I}							1		1				SP		cslc: Arbiter
																								NA	NA	cslc: inst tree
																								NA	NA	cslc: autoroute
		П							ы													1		SP		cslc: Bus ifc
		Ť					Ť													T				SP		cslc: Buses
																				T				SP	4	cslc: Clock gen
																				Г						cslc: cslNum
																										cslc: CDOMNum
				1																T				SP	3	cslc: Compare
					1															Т		1		SP	2	cslc: Counter
							1											1		T				SP		cslc: Decoder
							i													Т				SP		cslc: Enum
							Ť													T		1		SP		cslc: Field
				1			Ť											1		T		1		ΒZ		cslc: Fifo
							Ť			T								Ċ		1		1		SP	1	cslc: Interconn
							Ť													Т		T		SP	1	cslc: ISA
												1								Т		T		ΒZ		cslc: Memmap
																				T		1		SP	5	cslc: Memory
																				1		L		SP		cslc: Pipeline
					1			1			1		1					L		1		1		UN		cslc: Procon
					L				T											T		1		SP		cslc: Reg
				1			L		L				L							1		1		SP		cslc: RF
																1		1		1				UN		cslc: Sched
																	I			1				ΒZ		cslc: State
			L	1	1		1	1					L				L	Т	1	1				NA	NA	cslc: Tb
																		L		1				UN		cslc: Unit
						_			_										1	T		1		ОВ		cslc: VC
1																				T				NA		sw_lib: ASM
																								NA		sw_lib: Csim
				L	L		L		1				1											NA		hw_lib:Memcntl
					L																	1		NA		hw_lib: micro eng
																								NA		hw_lib: Proc. Ring
																								NA		hw_lib: PSCQN
																										STATUS LEGEND put p
																										STATOS LEGEND put p

Priorities
Low priority
medium priority
high priority

File name = csl_class.c misc/project_managen

Averages 77.5 45 10 25 10 25 #DIV/0! 16.11 25 3.85 3.46 5 0 6.67 13.46 68.85 13.85 27.31 19.69 58.93 31.79 17.33 7 8.93 6.92 20.38 20.08 10.54 10.62 7.83 16.92 23.08 0 3.33 5 5.83 27.33

ercentages in the boxes #DIV/0!

Overall project average 16.54

ods nent/csl_class.ods

				res																			ر	딦	SS				
				data structures	SL	t2	₽								پ					en	ا _		gen	document code gen	CSL Info class				
			×	stru	ቱ] S	+	ح							Ske Ke				ker	e g	gen	gen	code	ğo	Je (Unit	L	je	
			Syntax	ta s	algorithms	documented: hw circuits	coded: CSL proto C++ lib	coded: Verilog library					ker		CSLOM checker	elab			CDOM checker	Verilog code gen	code	j əp	S	Ħ		LU	Arbiter	Asembl	s ifc
				da		ا ځ	70 TO	g≡				<u>_</u>	tree walker	Σ	Σ	Σ	tor	>	√ C	o Gc	8	code	SystemC	me	CS	CSL	Ark	Ase	Bus
L	ار		ed:	ed:	ed:	ed:	Lp	jo	Σ	_	lexer	parser	e l	CSLOM); 	CSLOM	Adaptor	СБОМ	00	erilo	VHDL	C++	ste	In J	.: ⊠	Ξ.	Σ	Σ.	Ξ
ownei	owner		ent	ent	ent	eut	CS	Vel	CSIM	GU		ed					AC				>	Ċ			CSLOM:	CSLOM:	CSLOM:	CSLOM:	CSLOM:
o v	ő		Ш	un	E	틸	ed:	:pe	:pe	:p	eq:	ed:	ed:	eq:	ed:	ed:	ed:	ed:	ed:	ed:	ed:	ed:	ed:	ed:					
cslc	cslc	CSL CLASS	documented:	documented:	documented:	힣	po	po	coded:	coded: GUI	coded:	coded:	coded:	coded:	coded:	coded:	coded:	coded:	coded:	coded:	coded:	:pəpoɔ	coded:	coded:	nses	nses	nses	nses	nses
NA		cslc: Verilog Parser	100	NA	NA	NA	NA		NA	NA	70	70	70	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA			NA I	
APA		cslc: CDOM	NA	25	25	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA	NA	85	NA	NA	NA		NA		NA			NA I	
СР		cslc: GUI	NA	NA	NA	NA	NA	NA		10	NA	NA	NA	NA	NA	NA		NA	NA		NA	NA	NA	NA	NA			0	
BZ		CSL pp: regex	25	0	0	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA		NA	NA			NA	NA	NA	0	NA	NA	NA I	NA
OS		CSL pp: Aikido	NA	0	0	NA	NA		NA	NA	NA	NA	NA	NA	NA	NA		NA	NA	NΑ		NA	NA	NA	NA		-	NA	
BZ		cslc: Arbiter	0	0	0	0	0	NA	0	NA	0	0	0	0	0	0	0	NA	0	NA	NΑ	NA	NA	NA	0		1		
BZ		cslc: inst tree	NA	25	25	NA	NA	NA	NA	0	NA	NA	NA	NA	NA	25	NA	NA	NA	NΑ	NA	NA	NA	NA	NA			\Box	
BZ		cslc: autoroute	70	25	25	NA	0	NA	0	0	0	0	0	75	0	50	75	NA	0	NΑ	NA	NA	NA	NA	NA				
BZ		cslc: Bus ifc	25	0	0	0	0	NA	0	0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA	NA	NA	NA	1		7	
BZ		cslc: Buses	20	0	0	0	0	NA	0	0	0	0	0	0	0	NA		NA	0	NA	_	NA	NA	NA	NA			T	
BZ	2	cslc: Clock gen	40	0	0	0	0	NA	0	0	0	0	0	0	0	NA		NA	0	NA	NA	NA	NA	NA	NA			寸	
os		cslc: Compare	50	0	0	0	5	NA	0	NA	0	0	0	0	0	NA		NA	0	NΑ	NA	NA	NA	NA	NA			ヿ	
OS	1	cslc: Counter	90	50	0	1	10	NA	0	0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA	NA	NA	0	\mathbf{T}		\Box	
APA	1	cslc: Decoder	90	90	100	0	0	NA	0	0	100	100	100	100	100	NA	90	NA	0	NA	NA	NA	NA	NA	NA				
BZ		cslc: Enum	90	0	0	50	40	NA	0	0	0	0	0	0	0	NA	0	NA	0	NA	NA	NA	NA	NA	NA				
SP		cslc: Field	10	90	75	50	80	NA	NA	0	0	0	0	50	0	NA	0	NA	0	NA	NA	NA	NA	NA	NA				
OS	3	cslc: Fifo	75	0	0	55	1	NA	0	0	0	0	0	95	0	NA	0	NA	0	NA	NA	NA	NA	NA	NA	1			
BZ	1	cslc: Interconn	80	70	70	50	5	NA	0	0	90	90	90	90	90	0	90	NA	10	NA	NA	NA	NA	NA	NA				
SP	1	cslc: ISA	80	85	85	60	90	NA	NA	0	0	0	0	0	0	0	0	NA	0	NA	NA	NA	NA	NA	NA				
AB		cslc: Memmap	70	0	0	50	90	NA	0	0	10	10	0	30	0	0	0	NA	0		NA	0	NA		0			_	
BZ	_	cslc: Memory	50	0	0	50	0	NA	0	0	0	0	0	5	0	0	0	NA	0		NA	0	NA		NA	-		_	_
BZ		cslc: Pipeline	70	0	0	50	5	NA	0	0	0	0	0	0	0	0	0	NA	0		_	NA	NA		NA			_	
OS		cslc: Procon	83	0	0	NA	0	NA	0	0	0	0	0	0	0	NA	0	NA	0			NA	NA		0			_	
OS		cslc: Pscqn	84	0	0	NA	0	NA	0	0	0	0	0	0	0	NA	0	NA	0	NA		NA	NA		0			\dashv	_
os		cslc: Reg	85	0	0	50	70	NA	0	0	0	0	0	60	0	NA	0	NA	0		_	NA	NA		0	Η.		\dashv	_
OS		cslc: RF	86	0	0	50	0	NA	0	0	0	0	0	95	0	NA	0	NA	0		_		-		0	1		\dashv	_
BZ		cslc: Sched	87	0	0	50		NA		0	0	0	0	0	0	NA		NA							NA			\dashv	_
OB		cslc: State cslc: Tb	88	0	0	50		NA		0	0	0	0	0	0	NA		NA							NA			\dashv	-
OB BZ		csic: 16 cslc: Unit	89	0	0	NA 50		NA NA		0	0	0	0	5	0	NA NA		NA					NA		0 NA			\dashv	_
APO		cslc: onit cslc: cslNum	90	0	0	0	0	0	0	0	0	0	0	08	0	0	0	NA 0	0	0	0	0			NA	_		\dashv	\dashv
APO		cslc: CDOMNum	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0		NA			\dashv	
OB	<u> </u>	cslc: CDOMNam	90	0	0	50		NA	0	0	0	0	0	80	0	NA		NA							NA				
		sw lib: ASM	0	0	0	NA			NA		NA	NA	NA	NA	NA				NA						1171				
	_	sw_lib: ASM	0	0	0	NA				NA	NA	NA	NA	NA	NA				NA									-	\dashv
CL	_	hw lib:Memcntl	0	0	0	20	0	0		NA	0	0	0	0	0				NA									\dashv	\dashv
CL		hw lib: micro eng	0	0	0	30	0	0		NA	0	0	0	0	0				NA										\dashv
AV		hw_lib: Proc. Ring	0	0	0	35		0		NA	0	0	0	0	0				NA										\dashv
AV	_	hw_lib: PSCQN	0	0	0		40			NA		0	0	0	0				NA										
		STATUS LEGEND put p	ercer		es in																								
	—	DO LECENTO PUE P	3. 561	9																									

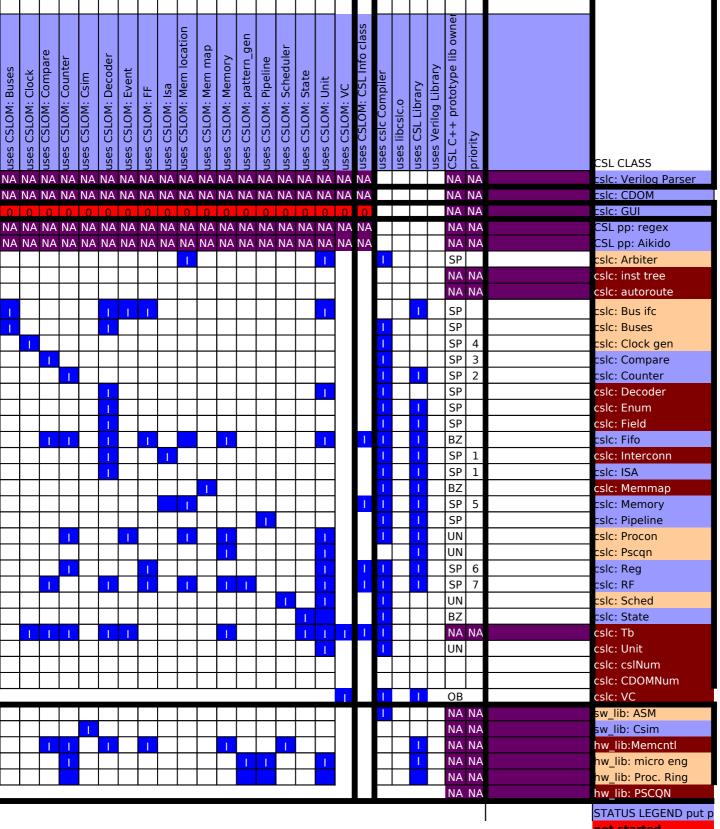
light red
yellow
light magenta
green
light blue
dark violet
black

Priorities
Low priority

medium priority
high priority

orange 4 violet red

File name = csl_class.ods misc/project_management/csl_class.ods 25



status Legend put protestarted
under construction
under test
completed
intersection between
Not applicable
Divider

Priorities
Low priority
medium priority
high priority

File name = csl_class.c misc/project_managen

Averages

77.5 45 10 8.33 0

18.75 22.86

1.79 1.43

2.86

4.23 10.79

62.14 12.86

27.31

16.14

55

28.57 16.25

6.56

8.33

6.38

6.46 18.93

16.5

9.79

9.86

7.23

15.71

0

0

21.43

0

1.67

2.5

2.92 6.67

ercentages in the boxes

14.43

13.31

ods nent/csl_class.ods

CSL CLASS	Mem location	Compare	Counter	Clock	State	Event	#	Decoder	Arbiter	Scheduler
Isa								Х		
Pipe										
Vc										
Tb				Х						
Fifo							Х			
Memmap										
Reg										
Rf							Х	Х		
Arbiter									Х	
Scheduler										Х
Procon										
Pscqn										
Decoder								X		
Asm								Х		
Bus										
Memcount							Χ	X	Х	Х
Processoring							Χ			
Microengine										

X Isa	Pipe	۸c	Мет тар	Memory	pattern_gen	Pscqn	Asembler	Bus ifc
X								
	Х							
		Х						
			X	X				
			X					
			X	Х				
			X		Х			
			Х	Х				
			Х					
				X X		Χ		
				X				
X								
X				Х				Х
	Х		X	Х				
	Χ		Х	Х			X	
Х	X				Х		X	

			Generated by	
× Internal compiler	Csl C++ lib	CSLOm	Hand writing	Both
Χ				
Х				
Х				
Х				
Х				
Х				
Х				
Х				
Х				
Х				
Х				
Х				
Х				
Х				
Х	Х			
Х	Х			
Х	Х			

	Overall proje	ct average
April 07	16.54	
April 12	16.56	
April 16	16.82	
April 23	20.45	
April 30	22.51	
May 07	22.56	
May 14	22.72	
May 21	24.21	
June 4	25.28	
June 14	19.57	
June 21	19.4	



