Control block inputs/outputs

		both nodes	processor node	memory node	fair_counter	bo
inputs	pr_msg.cmd	1	0	0	0	0
	pr_msg.valid	1	0	0	0	0
	pr_msg.age/timeout	1	0	0	0	0
	mq_qm_full	1	0	0	0	0
	mq_qm_empty	1	0	0	0	0
	nios_busy	0	1	0	0	0
	mem_busy	0	0	1	0	0
	addr	0	0	0	0	0
	dst_id	0	0	0	0	0
	cycle_count	0	0	0	1	0
outputs	bo_send_msg	0	0	0	0	1
	mq_push	1	0	0	0	0
	mq_pop	1	0	0	0	0
	mem_wr_en	0	0	1	0	0
	mem_rd_en	0	0	1	0	0
	sq_push	0	0	1	0	0
	sq_pop	0	0	1	0	0
	dm_wr_en	0	1	0	0	0
	dm_rd_en	0	1	0	0	0
	im_wr_en	0	1	0	0	0
	im_rd_en	0	1	0	0	0

mq – message queue , sq – send queue , dm - data memory , im – instr memory

		m0	m3	au	qm
inputs	pr_msg.cmd	0	0	1	1
	pr_msg.valid	0	0	1	0
	pr_msg.age/timeout	0	0	0	0
	mq_qm_full	0	0	0	0
	mq_qm_empty	0	0	0	0
	nios_busy	0	0	0	1
	mem_busy	0	0	0	0
	addr	0	0	1	0
	dst_id	0	0	1	0
	cycle_count	0	0	0	0
outputs	bo_send_msg	0	0	0	0
	mq_push	0	0	0	1
	mq_pop	0	0	0	1
	mem_wr_en	0	0	0	0
	mem_rd_en	0	0	0	0
	sq_push	0	0	0	0
	sq_pop	0	0	0	0
	dm_wr_en	0	0	1	0
	dm_rd_en	0	0	1	0
	im_wr_en	0	0	1	0
	im_rd_en	0	0	1	0
	m0_cntl	1	0	0	0
	m3_cntl	0	1	0	0
	dma_wr_en	0	0	1	0
	dma_rd_en	0	0	1	0
	rb_wr_en	0	0	1	0
	rb_rd_en	0	0	1	0
	sb_wr_en	0	0	1	0
	sb_rd_en	0	0	1	0