Name\Week	8.06	15.06	22.06	29.06	6.07	13.07
BZ(cslom)	memmap, fix some field problems	bugs, refactor	Mem leak fix	Mem leak fix	Mem leak fix	automapper, fix field bugs
APa (adapter)	bugs	memmap	Mem leak fix	Mem leak fix	Mem leak fix	Signal group CSLOM
AB					Cmd summary fix, code gen bug fixes	Synplicity file parser
TH(TB)	verinum	verinum	Test Code gen	Test Code gen	Test Code gen	testbench vectors(CSLOM)
OS	LP(Decoder, Register, RF)	LP(Decoder, Register, RF)	LP(TB, VC, ISA)	LP(Memory, Pipeline)	Integrating symtree	Parser refactoring, Changing tokens to literals
SP	W(Field, Enum, Memmap)	W(Field, Memmap)	Regresion script	Regresion script	Regresion script	Make regression distributed with perl
AI					Learning	C++ code gen visitor
MP			C++ code gen	C++ code gen	Refactoring cslom_cmd+bug fixes	Refactoring cslom_cmd+bug fixes
AS			Driver code, CSLOM MemMap	SC codegen from CSLOM	Refactoring cslom_cmd+bug fixes	Refactoring cslom_cmd+bug fixes
EM	CSL interconn, test codegen	CSL memmap test codegen	Enum, Field csl test gen	Enum, Field csl test gen	Enum, Field csl test gen	Test Verilog output
AO	CSL fifo, test codegen	CSL fifo, test codegen	MemMap csl test gen	ISA csl test gen	Reg, RF, Memory csl test gen	PDF codegen, ISA
APo						SystemC codegen from CDOM
IC	Field, FIFO	Field, Interconnect test fix	Memmap, Interconnect test fix	Memmap	Interconnect test fixes	Register, Field
AM	Field, Enum	ISA, MemMap	Memmap	Memmap	RF, FIFO	Memmap
PE	Memmap	Memmap, Field, Enum	Field, Enum	Field, FIFO	Register, Field	ISA
CGH	Memmap	MemMap	Memmap, RF	Field, FIFO	Field, Enum	Memmap
CP						

20.07	27.07	3.08
ISA	ISA sg group(start)	sg group pipeline(start)
Signal group CSLOM	memmap	ISA
Synplicity file parser	TB vectors, state data (adapter)	state data (adapter)
state data(CSLOM)	ISA CSLOM	ISA CSLOM
Parser refactoring, Changing tokens to literals	Bugs	Bugs
Make regression distributed with perl	Make regression distributed with perl	Bugs
C++ code gen visitor	C++ code gen visitor	
C++ codegen from CSLOM	C++ codegen from CSLOM	C++ codegen driver code+bugs
Test Verilog output		
PDF codegen, ISA	PDF codegen, ISA	PDF codegen, ISA
SystemC codegen from CDOM	SystemC codegen from CDOM	SystemC codegen from CDOM
VC, FIFO	VC, FIFO	VC, FIFO
TB, Memmap	TB, Memmap	RF, Register
RF, Register	RF, Register	TB, Memmap
RF, FIFO	-	-

IDE