

### 3.1 Get methods

```
string fifo_hid.get_reset_name();  
string fifo_hid.get_clock_name();  
string fifo_hid.get_rd_clock_name();  
string fifo_hid.get_wr_clock_name();  
string fifo_hid.get_push_name();  
string fifo_hid.get_pop_name();  
string fifo_hid.get_full_name();  
string fifo_hid.get_empty_name();  
string fifo_hid.get_wr_data_name();  
string fifo_hid.get_rd_data_name();  
string fifo_hid.get_valid_name();
```

### 3.2 Csl\_fifo get methods

```
string fifo_hid.get_reset_name();
```

**DESCRIPTION :**

It gets the *name* for the reset port of fifo.

[Get methods]

Sets the reset name for a unit named *u* using get\_reset\_name() method.

**CSL CODE**

```
csl_fifo FO{
    FO(){
        set_width(32);
        set_depth(4);
        set_reset_name("rst");
    }
};

csl_unit u{
    csl_signal sig;
    FO FO;
    u(){
        set_signal_prefix(FO.get_reset_name());
    }
};
```

**VERILOG CODE**

```
string fifo_hid.get_clock_name();
```

**DESCRIPTION :**

It get the *name* for the clock port of fifo.

[Get methods]

Sets the clock name for a unit named *u* using get\_clock\_name() method.

**CSL CODE**

```
csl_fifo FO{
    FO(){
        set_width(32);
        set_depth(4);
        set_clock_name("clk");
    }
};

csl_unit u{
    csl_signal sig;
    FO FO;
    u(){
        set_signal_prefix(FO.get_clock_name());
    }
};
```

**VERILOG CODE**

```
string fifo_hid.get_rd_clock_name();
```

**DESCRIPTION :**

It gets the *name* for the read clock port of fifo.

[Get methods]

Sets the read clock name for a unit named *u* using get\_rd\_clock\_name() method.

**CSL CODE**

```
csl_fifo FO{
  FO(){
    set_width(32);
    set_depth(4);
    set_rd_clock_name("rd_clk");
  }
};

csl_unit u{
  csl_signal sig;
  FO FO;
  u(){
    set_signal_prefix(FO.get_rd_clock_name());  }
};
```

**VERILOG CODE**

```
string fifo_hid.get_wr_clock_name();
```

**DESCRIPTION :**

It gets the *name* for the write clock port of fifo.

[Get methods]

Sets the write clock name for a unit named *u* using get\_wr\_clock\_name() method.

**CSL CODE**

```
csl_fifo FO{
    FO(){
        set_width(32);
        set_depth(4);
        set_wr_clock_name("wr_clk");
    }
};

csl_unit u{
    csl_signal sig;
    FO FO;
    u(){
        set_signal_prefix(FO.get_wr_clock_name());
    }
};
```

**VERILOG CODE**

```
string fifo_hid.get_push_name();
```

**DESCRIPTION :**

It gets the *name* for the push port of fifo.

[Get methods]

Sets the push port name for a unit named *u* using get\_push\_name() method.

**CSL CODE**

```
csl_fifo FO{
    FO() {
        set_width(32);
        set_depth(4);
        set_push_name("push");
    }
};

csl_unit u{
    csl_signal sig;
    FO FO;
    u() {
        set_signal_prefix(FO.get_push_name());
    }
};
```

**VERILOG CODE**

```
tring fifo_hid.get_pop_name();
```

**DESCRIPTION :**

It gets the *name* for the pop port of fifo.

[Get methods]

Sets the pop port name for a unit named *u* using get\_pop\_name() method.

**CSL CODE**

```
csl_fifo FO{
    FO(){
        set_width(32);
        set_depth(4);
        set_pop_name("pop");
    }
};

csl_unit u{
    csl_signal sig;
    FO FO;
    u(){
        set_signal_prefix(FO.get_pop_name()); }
};
```

**VERILOG CODE**

```
string fifo_hid.get_full_name();
```

**DESCRIPTION :**

It gets the *name* for the full port of fifo.

[Get methods]

Sets the full port name for a unit named *u* using get\_full\_name() method.

**CSL CODE**

```
csl_fifo FO{
    FO(){
        set_width(32);
        set_depth(4);
        set_full_name("full");
    }
};

csl_unit u{
    csl_signal sig;
    FO FO;
    u(){
        set_signal_prefix(FO.get_full_name()); }
};
```

**VERILOG CODE**



```
string fifo_hid.get_empty_name();
```

**DESCRIPTION :**

It gets the *name* for the empty port of fifo.

[Get methods]

Sets the empty port name for a unit named *u* using `get_empty_name()` method.

**CSL CODE**

```
csl_fifo FO{
    FO(){
        set_width(32);
        set_depth(4);
        set_empty_name("empty");
    }
};

csl_unit u{
    csl_signal sig;
    FO FO;
    u(){
        set_signal_prefix(FO.get_empty_name()); }
};
```

**VERILOG CODE**

```
string fifo_hid.get_wr_data_name();
```

**DESCRIPTION :**

It gets the *name* for the wr\_data port of fifo.

[Get methods]

Sets the write data port name for a unit named *u* using get\_wr\_data\_name() method.

**CSL CODE**

```
csl_fifo FO{
    FO(){
        set_width(32);
        set_depth(4);
        set_wr_data_name("write_data");
    }
};

csl_unit u{
    csl_signal sig;
    FO FO;
    u(){
        set_signal_prefix(FO.get_wr_data_name());
    }
};
```

**VERILOG CODE**

```
string fifo_hid.get_rd_data_name();
```

**DESCRIPTION :**

It gets the *name* for the rd\_data port of fifo.

[Get methods]

Sets the read data port name for a unit named *u* using get\_rd\_data\_name() method.

**CSL CODE**

```
csl_fifo FO{
    FO(){
        set_width(32);
        set_depth(4);
        set_rd_data_name("read_data");
    }
};

csl_unit u{
    csl_signal sig;
    FO FO;
    u(){
        set_signal_prefix(FO.get_rd_data_name());
    }
};
```

**VERILOG CODE**

```
string fifo_hid.get_valid_name();
```

**DESCRIPTION :**

It gets the *name* for the valid port of fifo.

[Get methods]

Sets the valid port name for a unit named *u* using get\_valid\_name() method.

**CSL CODE**

```
csl_fifo FO{
    FO(){
        set_width(32);
        set_depth(4);
        set_valid_name("valid");
    }
};

csl_unit u{
    csl_signal sig;
    FO FO;
    u(){
        set_signal_prefix(FO.get_valid_name()); }
};
```

**VERILOG CODE**