Designing an SRAM Memory System for the LH7A400: A 16-bit Example

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INTRODUCTION

System design time can be saved by taking advantage of the LH7A400's Static Memory Controller (SMC) that seamlessly interfaces to both static memory devices (such as SRAM) and PC-cards. The SMC handles memory interfacing transparently with any external memory system width, and any transaction size. Data transactions between the SMC and external memory occur over the External Bus Interface (EBI).

This application note describes static RAM memory system design for the LH7A400, specifically illustrating the use of wait states, byte lane enables, and ensuring timing constraints. This application note presents hardware design and timing constraints, as well as register setup to implement the chosen design.

CHOOSING MEMORY DEVICES

The first task is to choose the memory devices for your system. The LH7A400 supports 8-bit, 16-bit, and 32-bit SRAM. In addition, the 8-bit chips can be configured as 8-bits wide, 16-bits wide (2 chips), or 32-bits wide (4 chips), depending on your requirements. Regardless of the memory system width you choose, the SMC automatically handles transactions of 8-, 16-, or 32-bits with any configuration.

Memory width selection should consider the word size generally stored in the bank and the cost of implementing different widths. This application note describes a 16-bit memory system constructed both of single 16-bit SRAM elements, and also with two 8-bit SRAM elements.

Another significant parameter when choosing SRAM is the access speed. Generally, slower access SRAM is less expensive, but may not be fast enough for the application. For the examples in this application note, medium-speed 55 ns SRAM is used.

MEMORY SYSTEM WITH 16-BIT SRAM

The first design example implements a 16-bit-wide memory system with 512KB × 16 SRAM. For illustration, the Samsung K6X8016C3B-B is referenced. Using a 16-bit SRAM for a 16-bit-wide system simplifies the hardware connection somewhat.

Hardware Design

The first example uses 512KB × 16 SRAM devices to implement a half-word-wide memory bank. A 16-bit-wide memory system can be designed two different ways.

SIMPLIFIED DESIGN

Two Write Byte Lane Enable signals are available for 16-bit systems: nWE0 and nWE1/A0. If only half-word-wide Writes will be used, the SRAM Upper Byte Enable and Lower Byte Enable can be tied to VSS. Then, nWE0 can be used as the Write Enable with A0/nWE1 left unconnected, as shown in Figure 1. With this design, there is no glue logic required. Since the Byte Enables are always TRUE, the data is gated with nCS and either nOE (for Reads) or nWE0 (for Writes).

Note that nWE1 is multiplexed with address line A0. When the SMC is programmed for a 16-bit memory system, this pin always functions as a write enable, not as an address line. This may affect your design of other peripherals using address line decoding in the same bank (same Chip Select). The unused data lines, D[31:16] in this case, must have pull-up or pull-down resistors installed to prevent the bus from floating when the SMC is accessing external memory.

Connect the LH7A400 A1 address line to A0 on the SRAM. The unused upper address bits can be connected to parse the Bank 2 memory space in any convenient way.

Additional SRAM could be easily added using the remaining address lines to uniquely position them in the memory space. For this example, I chose to place this space within static memory Bank 2, meaning that nCS2 is the active Chip Select signal to connect to the SRAM devices. The Chip Selects are uniquely encoded in the LH7A400, so nCS2 can be directly connected to the SRAMs. (See Table 4-5 in the LH7A400 User's Guide for memory bank selection.)

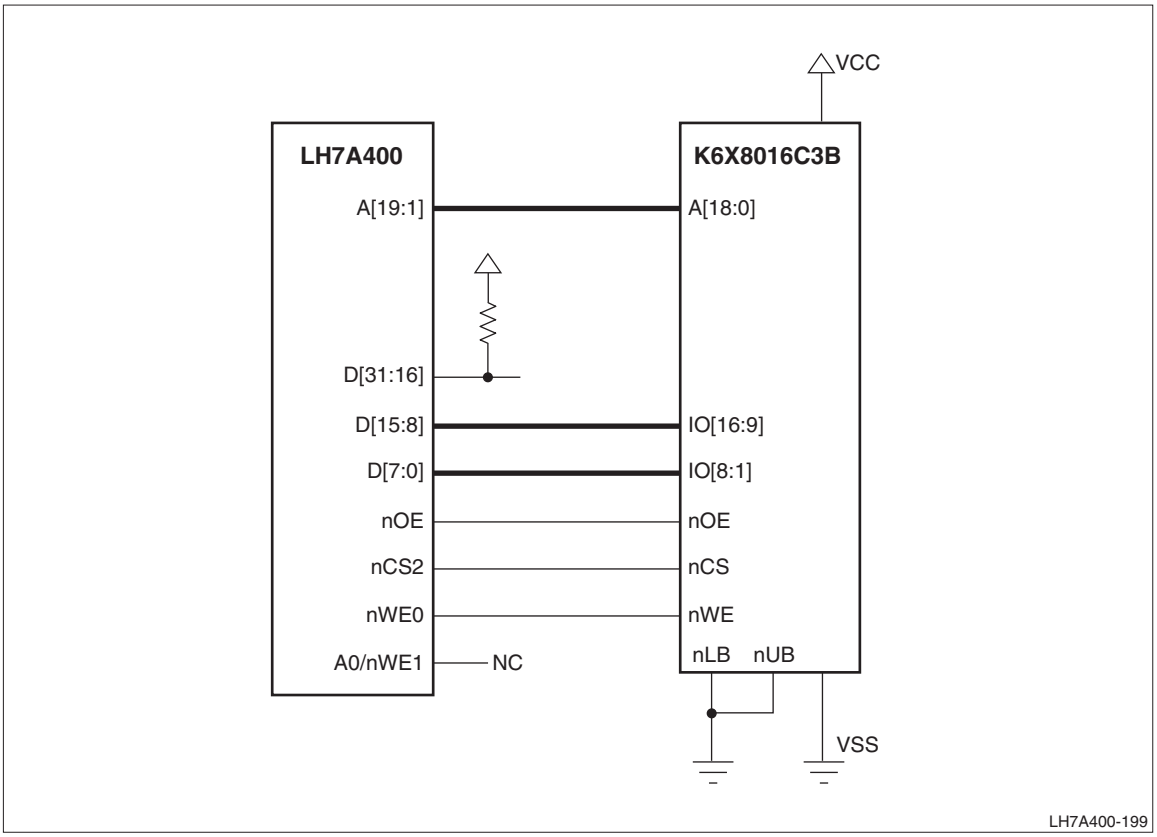

Figure 1. Simplified Memory System Using a Single 16-bit SRAM

DESIGN FOR BYTE OR HALF-WORD WRITES

If the half-word-wide memory system needs to be able to write byte-size data as well as half-word-size data, the Byte Lane Enables must be decoded for writing. For byte-size Reads, the SMC handles the logic to parse the incoming half-word-size data and select the proper byte.

This design uses both nWE0 and A0/nWE1 for Byte Lane Enable signals, as well as Write Enables. The nOE signal is still used as the sole signal for reading. To accomplish this, three AND gates decode the signals for the SRAM. This design is shown in Figure 2.

When reading byte-size data, the operating software must ignore the upper byte when requesting only the lower byte of data. When requesting the upper byte (i.e. reading from an odd-offset address, such as 0x0001), the SMC logic will automatically place the upper byte in the least-significant-byte position, and again the operating software simply ignores the upper-byte data.

As with the simplified design, note that nWE1 is multiplexed with address line A0. When the SMC is programmed for a 16-bit memory system, this pin always functions as a write enable, not as an address line.

Differing Size Memory Reads

The 16-bit architecture of the external memory system in this example does not restrict the SMC to 16-bit transactions. The SMC internally processes memory transaction to ensure size matching. If the SMC requires 32-bit data from the 16-bit system, it will automatically increment the address and read two half-words. For 8-bit Reads, the SMC ignores the upper or lower byte of the half word, depending on an odd or even address read.

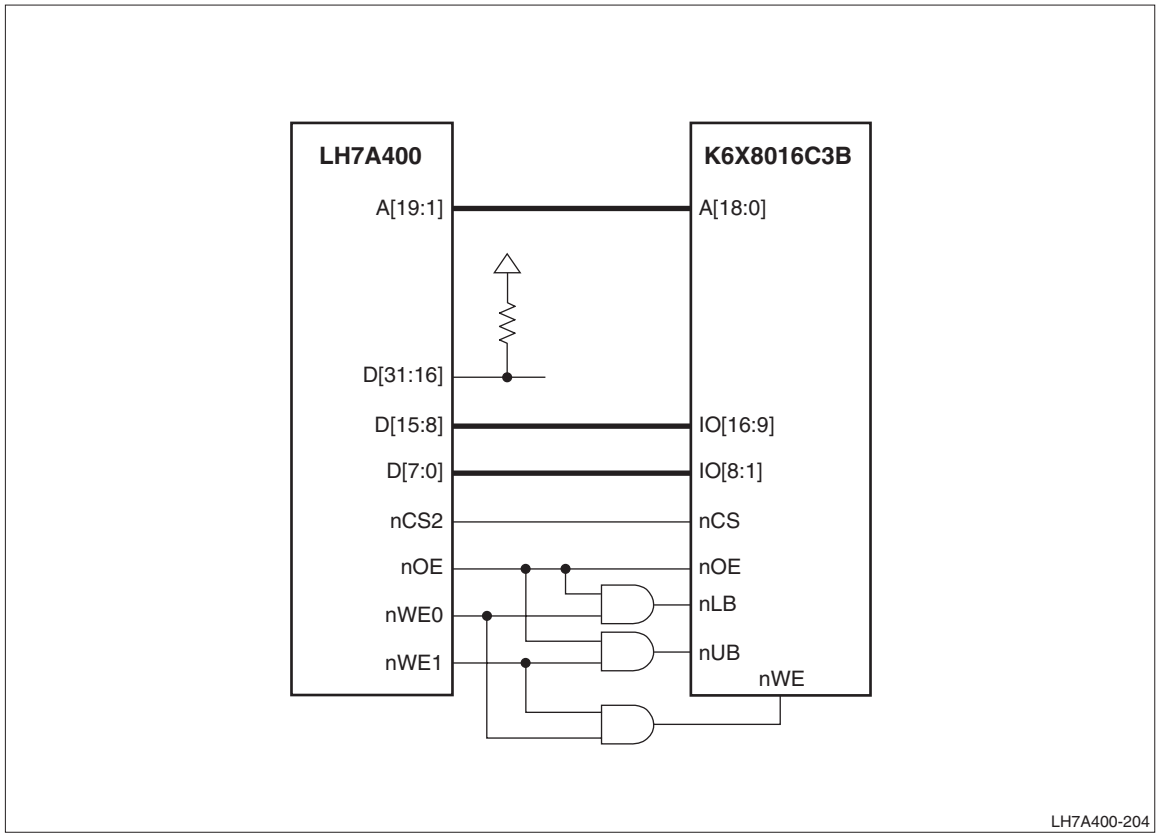

Figure 2. Byte and Half-Word Writable Memory System Using a Single 16-bit SRAM

TIMING

The LH7A400 uses synchronous internal circuitry to generate the asynchronous signals on the EBI. Therefore, timing from the LH7A400 perspective is in multiples of the internal system clock, HCLK ('C' in the datasheet and timing diagrams), and depends on the speed at which the SoC bus is operating. For this application note, it is assumed that the SoC bus is operating at an HCLK frequency of 100 MHz (10 ns period). All timing parameters should be matched to the SRAM timing specifications to ensure complete compatibility.

- HCLK = 100 MHz; therefore
- C = 10 ns

Timing Parameters

Timing parameters for the SRAM devices are defined in Table 1. These parameters are used in the timing tables discussion that follows. These parameters are overlaid on the timing diagrams appearing in Figure 3 through Figure 5.

Table 1. Timing Parameter Definitions

PARAMETER	DESCRIPTION
READ PARAMETERS	
tRC	Read Cycle Time
tAA	Address valid to Data valid
tCO	Chip Select valid to Data valid
tOE	Output Enable valid to Data valid
tOH	Data Output Hold from Address change
tOHZ	Output Disable to High-Z on SRAM
WRITE PARAMETERS	
tWC	Write Cycle Time
tDW	Data valid to rising Write edge
tDH	Data Hold from rising Write edge
tAW	Address valid to rising Write edge
tCW	Chip Select valid to rising Write edge
tAS	Address valid to Chip Select valid (Address setup time)
tWP	Write Pulse width
tWHZ	Rising Write edge to High-Z on SRAM

Write Timing

Figure 3 shows the zero wait-state timing for an SMC Write operation, and Table 2 reproduces the timing constraints from the LH7A400 Data Sheet. Table 3 reproduces the timing constraints from the K6X8016C3B-B SRAM.

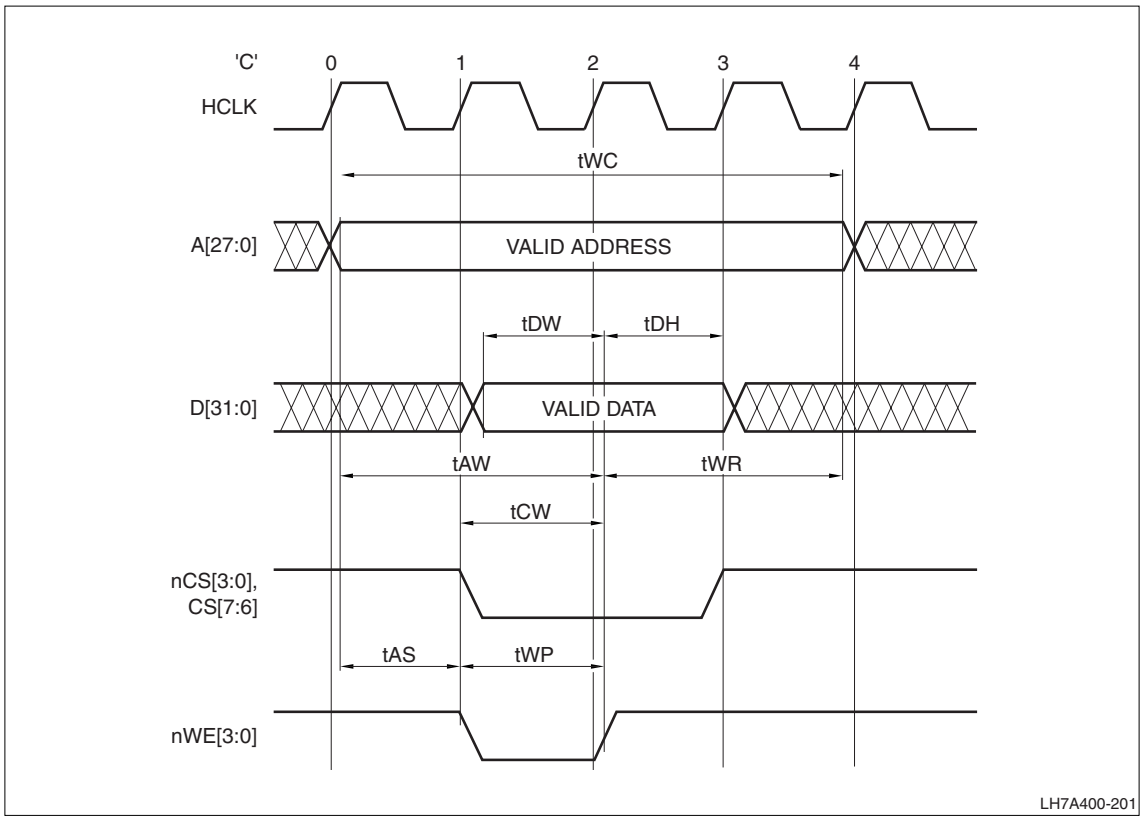

Figure 3. Write Timing with 0 Wait States (BCRx:WST1 = 0)

Determining the number of wait states required to properly operate requires analysis of each of the timing parameters in Table 2 and Table 3. Then, the parameter requiring the most wait states sets the *de facto* number of Write Cycle wait states. At 100 MHz, each wait state extends the timing parameter 10 ns.

Write Timing Analysis at 100 MHz

- tWC: The total cycle time of an SMC Write (tWC) in Table 2 is 40 ns. To meet the SRAM-required 55 ns, two wait states are needed to ensure proper operation.
- tDW: The Data Valid to rising Write edge (tDW) for the LH7A400 is 0 ns. The SRAM requires 20ns, thus this parameter requires two wait states.
- tDH: This parameter is the Data Hold from the rising Write edge, and is 3 ns. The SRAM needs no hold (0 ns), so no wait states are required by tDH.
- tAW: The Address Valid before Write edge (tAW) is 10 ns. The SRAM requires 45 ns. Thus, to extend tAW to 50 ns, four wait states are necessary.
- tCW: The minimum time between Chip Select assertion and the rising Write edge is tCW. The SRAM requires 45 ns, which means the LH7A400 10 ns needs four wait states to meet this minimum timing.
- tAS: The Address setup time prior to Chip Select (tAS) has a minimum value of 10 ns for the LH7A400. The SRAM needs no setup, so no wait states are required.
- tWP: The width of the Write Pulse (nWE LOW) required by the SRAM is 40 ns. To ensure operation, the LH7A400 needs four wait states to stretch tWP to 40 ns.

Three timing parameters require four wait states to be compatible with the chosen K6X8016C3B-B SRAM, thus four wait states are necessary to meet these timing constraints, overriding the other parameters.

- 4 Write Wait States are required for Write timing.

Figure 4 shows Write timing with four wait states.

Table 2. SMC Timing

PARAMETER	VALUE	VALUE AT 100 MHz
READ CYCLE		
tRC	3C-3 ns	27 ns
tAA	3C-20 ns	10 ns
tCO	3C-10 ns	10 ns
tOE	2C-10 ns	10 ns
tOH	0 ns	0 ns
WRITE CYCLE		
tWC	4C	40 ns
tDW	C – 11 ns	0
tDH	C + 3 ns	3 ns
tAW	2C – 10 ns	10 ns
tCW	2C – 10 ns	10 ns
tAS	C	10 ns
tWP	C – 10 ns	0

Table 3. K6X8016C3B-B Timing

PARAMETER	MIN.	MAX.
READ CYCLE		
tRC	55 ns	
tAA		55 ns
tCO		55 ns
tOE		25 ns
tOH	10 ns	
tOHZ	0 ns	20 ns
WRITE CYCLE		
tWC	55 ns	
tDW	20 ns	
tDH	0 ns	
tAW	45 ns	
tCW	45 ns	
tAS	0 ns	
tWP	40 ns	
tWHZ	0 ns	20 ns

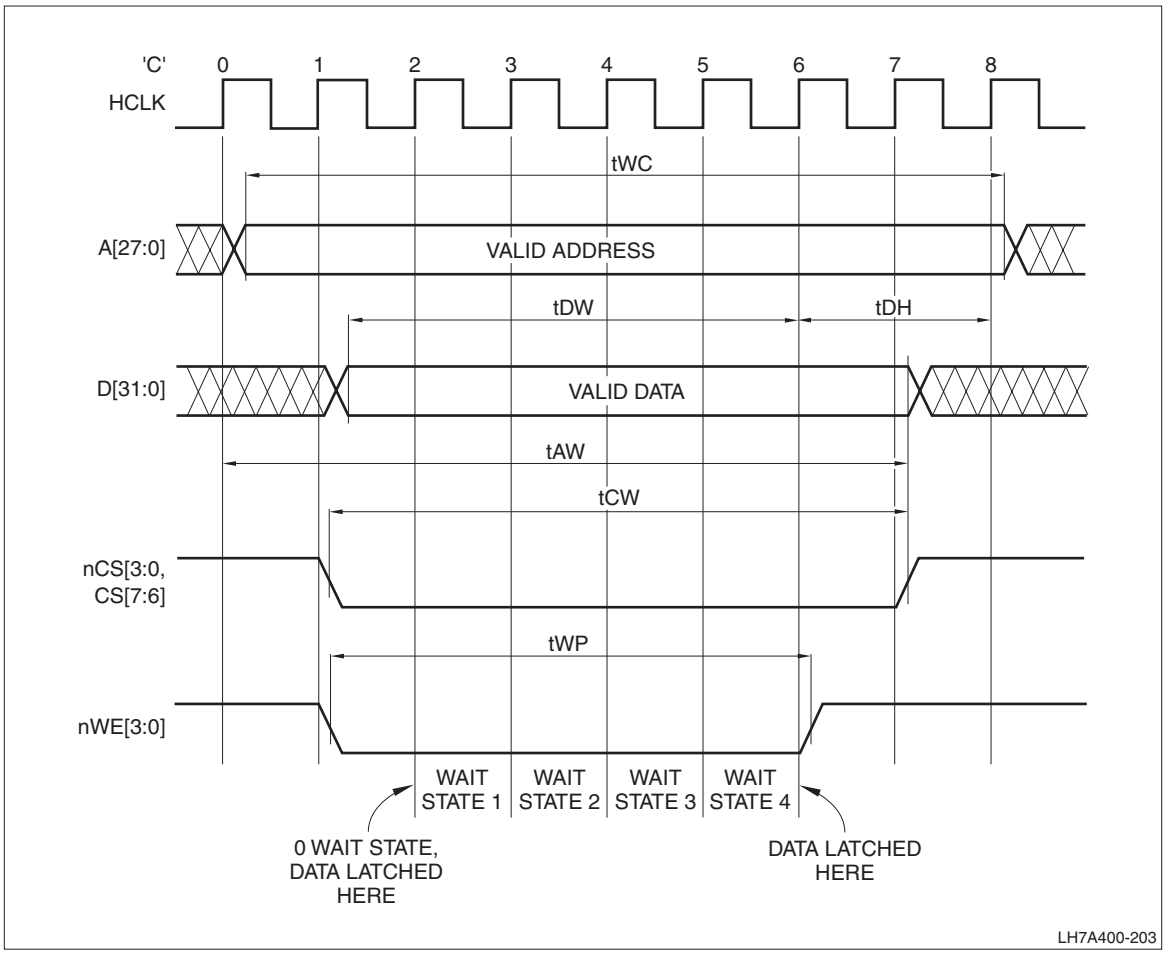

Figure 4. Write Timing with Four Wait States (BCRx:WST1 = 0b100)

Read Timing

Read timing is analyzed in the same way as Write timing. Once Read and Write have been analyzed, the larger number (Read or Write) of wait states will be used to program the SMC.

Read Timing Analysis at 100 MHz

- tRC: The minimum read cycle time, tRC, for the K6X8016C3B-B is 55 ns. Table 2 shows that for the SMC with no wait states, tRC is 3C-3 ns, or 27 ns. This is too fast for the SRAM, so wait states are needed to ensure proper data integrity for Reads. Adding three wait states stretches tRC (as well as the nCS2 and nOE signals) by 10 ns for each wait state, resulting in a new tRC of 57 ns.
- tAA: The minimum Address valid to Data valid time from Table 2 is 10 ns. The SRAM has a maximum of 55 ns. Thus, 10 ns meets the spec. Note that this signal is not extended by wait states.
- tCO: From Table 2, the time from Chip Select valid to Data valid is 20 ns, maximum. The maximum allowed by the SRAM is 55 ns, so this parameter meets the spec. Note that this signal is not extended by wait states.
- tOE: The minimum time from Output Enable valid to Data valid (tOE) for the LH7A400 is 10 ns. The SRAM requires 25 ns maximum and this parameter is not extended by wait states, so the spec is met.
- tOH: Data Output Hold following Address change is tOH. The SMC requires no hold time and the SRAM holds data for a minimum of 10 ns, so the requirement of the SMC is exceeded.

Both Read and Write maximum wait states are four. In the LH7A400, both Read and Write wait states are programmed with the BCRx:WST1 bit, so:

- 4 Read Wait States for our design.

Figure 3 shows the resultant Read timing with four wait states inserted.

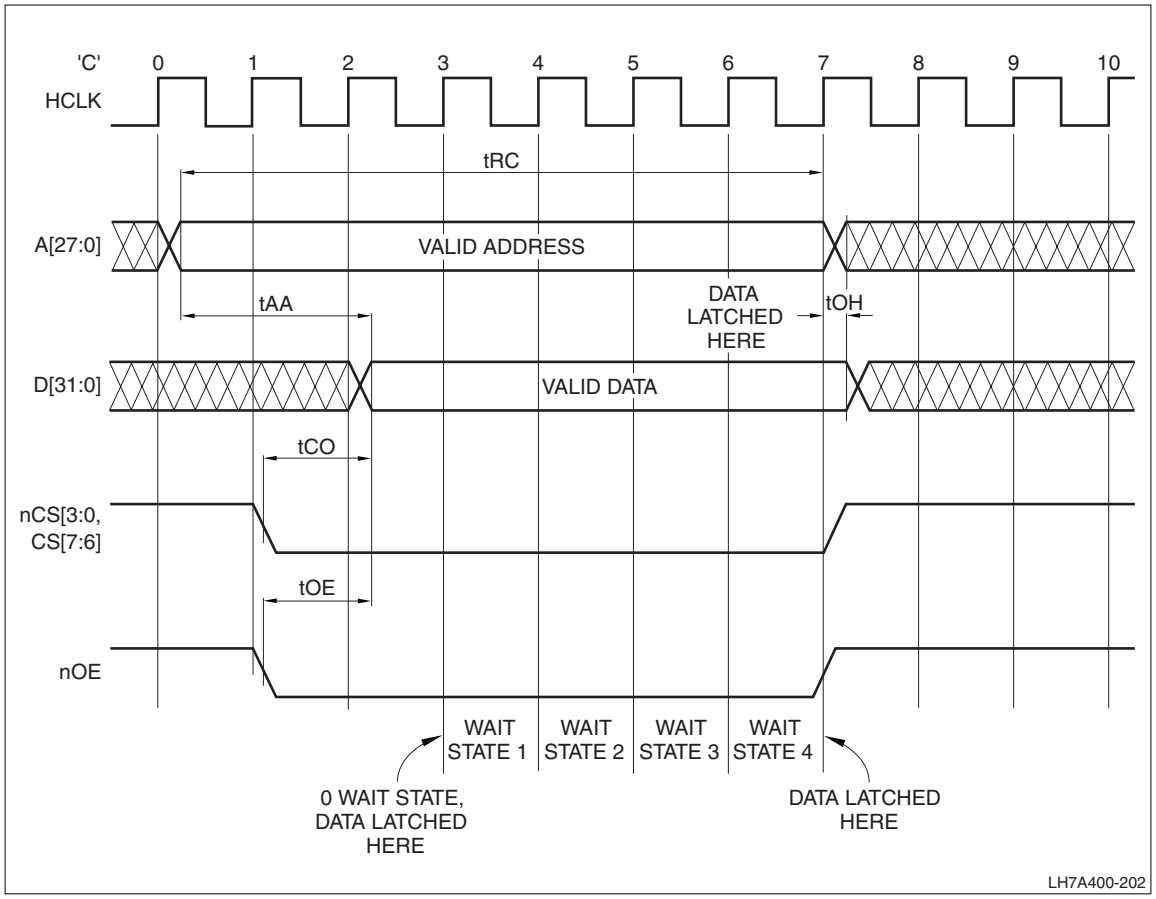

Figure 5. Read Timing with Four Wait States (BCRx:WST1 = 0b100)

Idle Cycle Timing

The LH7A400 turns the bus around from Read to Write (and vice-versa) in 1 C period. In Table 3, both the Read (tOHZ) and Write (tWHZ) bus turn around times for the K6X8016C3B-B can take a maximum of 20 ns. Thus, the Idle Cycle time needs to be programmed to extend an additional 1C period to never be shorter than the maximum possible requirement of the SRAM.

Register Setup

Once the hardware and timing has been reconciled, the necessary register configurations that your software must handle can be defined.

Referring to the LH7A400 User's Guide, the first task for your application's software is to configure the PINMUX register as described in the User's Guide. It requires that PINMUX:CLK0EN = 0 (CS6) and PINMUX:CLK1_2EN = 0 (CS7). This is the default value of those bits following reset. Even though it is the default value and those Chip Selects may not be needed, it is a good idea to assure the proper programming of PINMUX.

Next, the Bank Control Register (BCRx) for the particular bank needs to be programmed. Since we chose Bank 2, BCR2 must be programmed to match the hardware configuration. Refer to the LH7A400 User's Guide, and program the BCR2 fields as shown in the Table 4. For this case, program BCR2 to 0x1000081.

This completes design and programming for a 16-bit external memory system using 16-bit SRAM.

Table 4. BCR2 Program Values for One 16-bit Device

BITS	FIELD	VALUE	DESCRIPTION
31:30	///	00	**Reserved** Reading returns 0. Write the reset value (00).
29:28	MW	01	**Memory Width** Selects the external device memory width: 01 = 16 bits; nWE0 and A0/nWE1 are active
27	PME	0	**Page Mode Enable** 0 = Disables page mode.
26	WP	0	**Write Protect** Selects the memory access protection level: 0 = SRAM
25	WPERR	0	**Write Protect Error** 0 = No write protect error. Writing any value to this field clears an existing Write Protect error.
24:16	///	0x000	**Reserved** Reading returns 0. Write the reset value.
15:11	WST2	0b000000	**Wait State 2** This field controls Page Mode transactions. This note assumes that we are not using Page Mode and therefore, program this field to all zeros.
10	///	0	**Reserved** Reading returns 0. Because setting this field can cause anomalous activity on the nWE[3:0] signals (pins C8, N16, M14, and D10 respectively), ensure this bit is 0 when writing to this register.
9:5	WST1	0b00100	**Wait State 1** Program this value to set the SRAM Read and Write wait states. Since we calculated that four wait states are necessary to ensure proper timing, program this field to 0b00100. Access Time = (WST1 + 1) × HCLK.
4	///	0	**Reserved** Reading returns 0. Values written cannot be read.
3:0	IDCY	0001	**Idle Cycle** Program this value to set the memory data bus turnaround time, from a read cycle to a write cycle: (IDCY + 1) × HCLK. The currently programmed value can be ascertained by reading this field.

MEMORY SYSTEM WITH 8-BIT SRAM

The LH7A400 can also accommodate a 16-bit external memory system constructed of two 8-bit devices. The schematic for this system is shown in Figure 4. The Samsung K6X8008T2B-F SRAM chosen for the example have the same timing as the 16-bit SRAM, so the same parameters apply. Since this is also a 16-bit wide memory system, BCR2 is programmed to the same value, 0x1000081, as in the first example.

Hardware Design

The design with two chips is very similar to the single-chip memory system. As shown in Figure 4, each of the two K6X8008T2B-F SRAMs is connected to the proper byte of data signals from the LH7A400. Since two byte lane enables are available in a 16-bit system, nWE0 connects to the least-significant-byte device, and nWE1 connects to the most-significant byte.

The same discussion regarding address applies to the two-chip solution. Also, D[31:16] must be pulled HIGH or LOW so that it doesn't float.

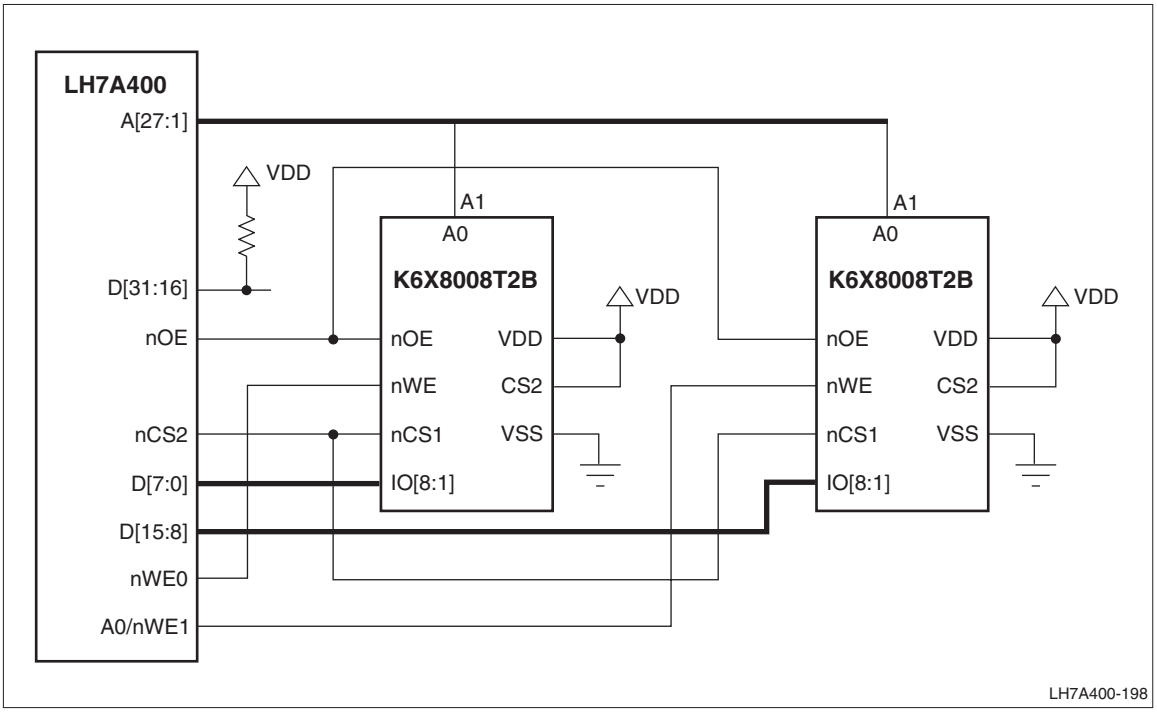

Figure 6. LH7A400 Memory System Using Two 8-Bit SRAMs

TIMING

A device with identical timing to the 16-bit SRAM was chosen for easier design. Thus, four wait states are required for the 8-bit timing as well.

Table 5. BCR2 Register Values for Two 8-bit Devices

BITS	FIELD	VALUE	DESCRIPTION
31:30	///	00	**Reserved** Reading returns 0. Write the reset value (00).
29:28	MW	01	**Memory Width** Selects the external device memory width: 01 = 16 bits (two 8-bit SRAMs); nWE0 and A0/nWE1 are active
27	PME	0	**Page Mode Enable** 0 = Disables page mode.
26	WP	0	**Write Protect** Selects the memory access protection level: 0 = SRAM
25	WPERR	0	**Write Protect Error** 0 = No write protect error. Writing any value to this field clears an existing Write Protect error.
24:16	///	0x000	**Reserved** Reading returns 0. Write the reset value.
15:11	WST2	0b000000	**Wait State 2** This field controls Page Mode transactions. This note assumes that we are not using Page Mode and therefore, program this field to all zeros.
10	///	0	**Reserved** Reading returns 0. Because setting this field can cause anomalous activity on the nWE[3:0] signals (pins C8, N16, M14, and D10 respectively), ensure this bit is 0 when writing to this register.
9:5	WST1	0b00100	**Wait State 1** Program this value to set the SRAM Read and Write wait states. Since we calculated that four wait states are necessary to ensure proper timing, program this field to 0b00100. Access Time = (WST1 + 1) × HCLK.
4	///	0	**Reserved** Reading returns 0. Values written cannot be read.
3:0	IDCY	0001	**Idle Cycle** Program this value to set the memory data bus turnaround time, from a read cycle to a write cycle: (IDCY + 1) × HCLK. The currently programmed value can be ascertained by reading this field.

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