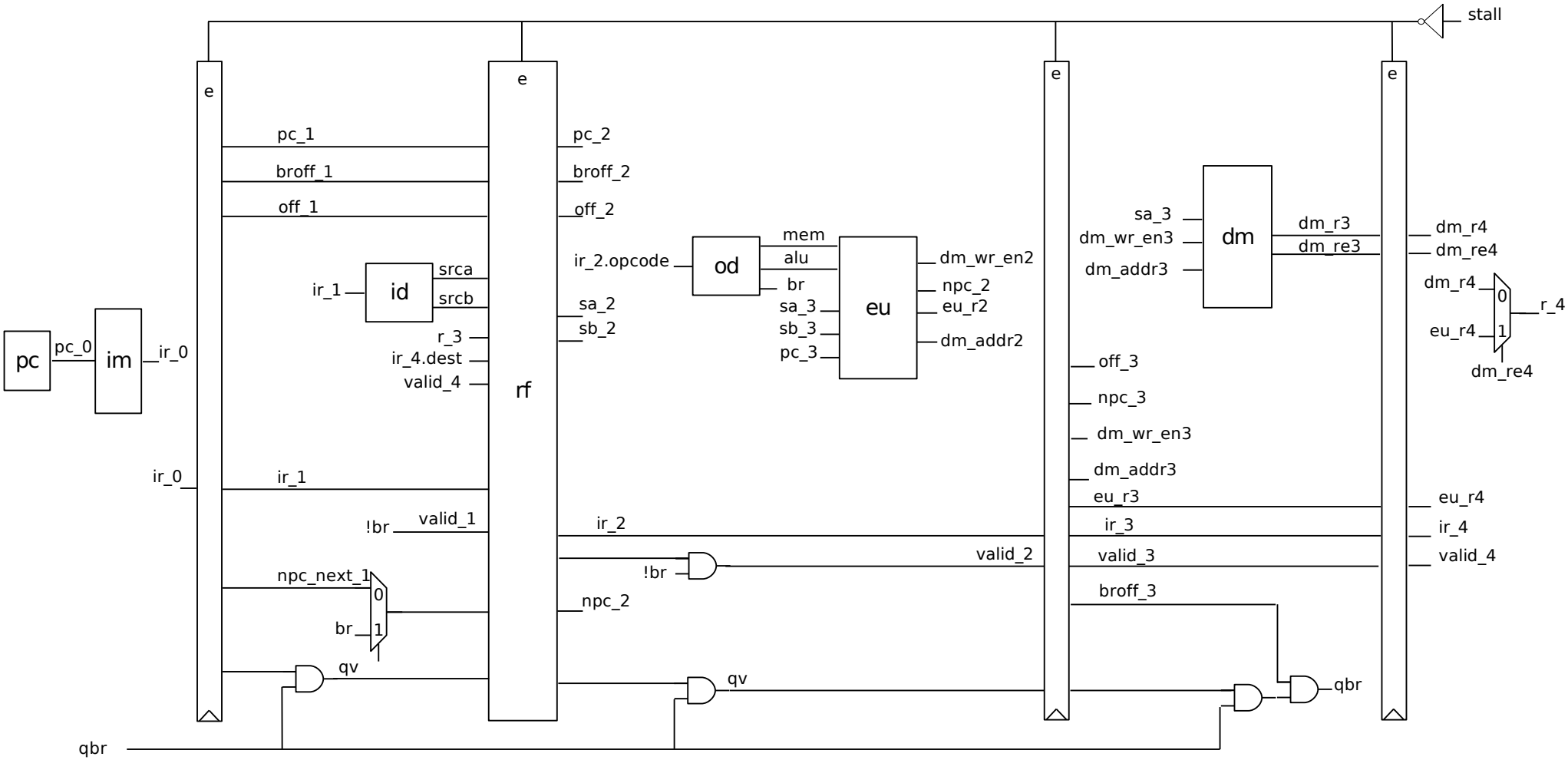
Microengine

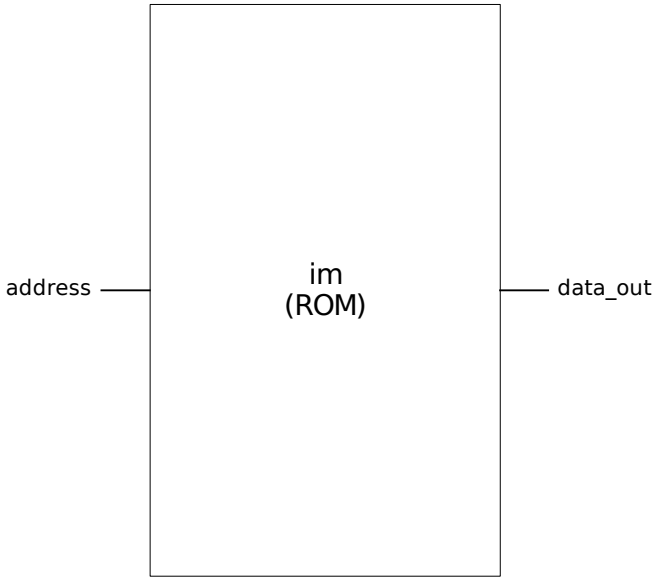


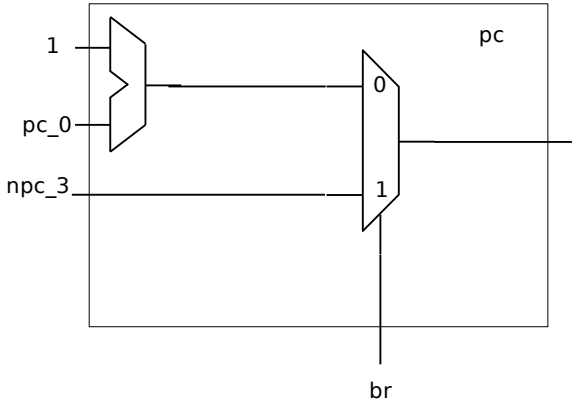
pc = program counter
im = instruction memory
id = instruction decode
rf = register file
od = operation decoder
eu = execution unit
dm = data memory

ir = instruction register
ir = format1 | format2 | format3 | format4

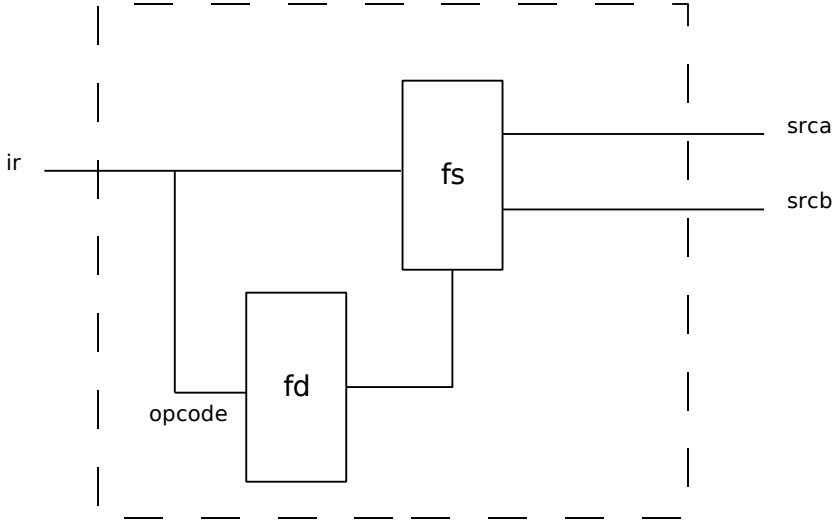
format1 = {opcode}
format2 = {opcode, src, dst}
format3 = {opcode, srca, srcb, dst}
format4 = {opcode, addr_src, cond_src, cond}

Instruction Memory(im)



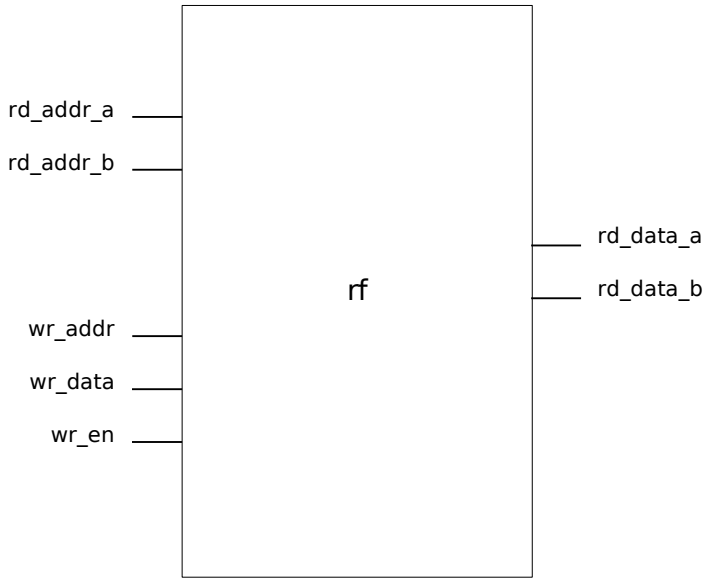


Instruction Decoder(id)

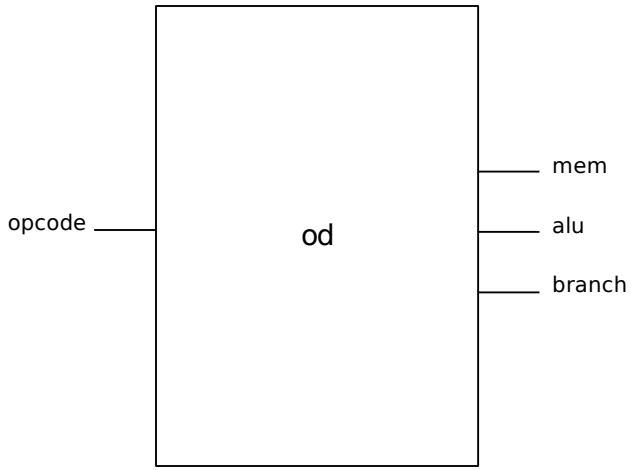


fd = format decoder
fs = field select

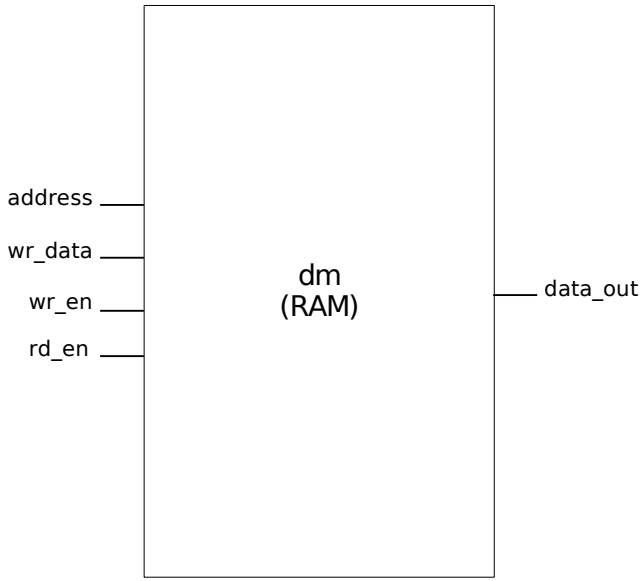
Register File(rf)



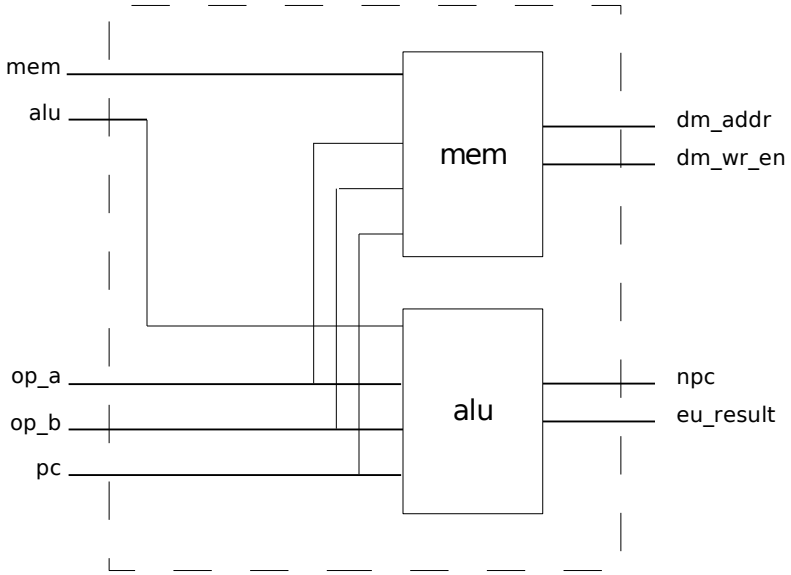
Operation Decoder(id)

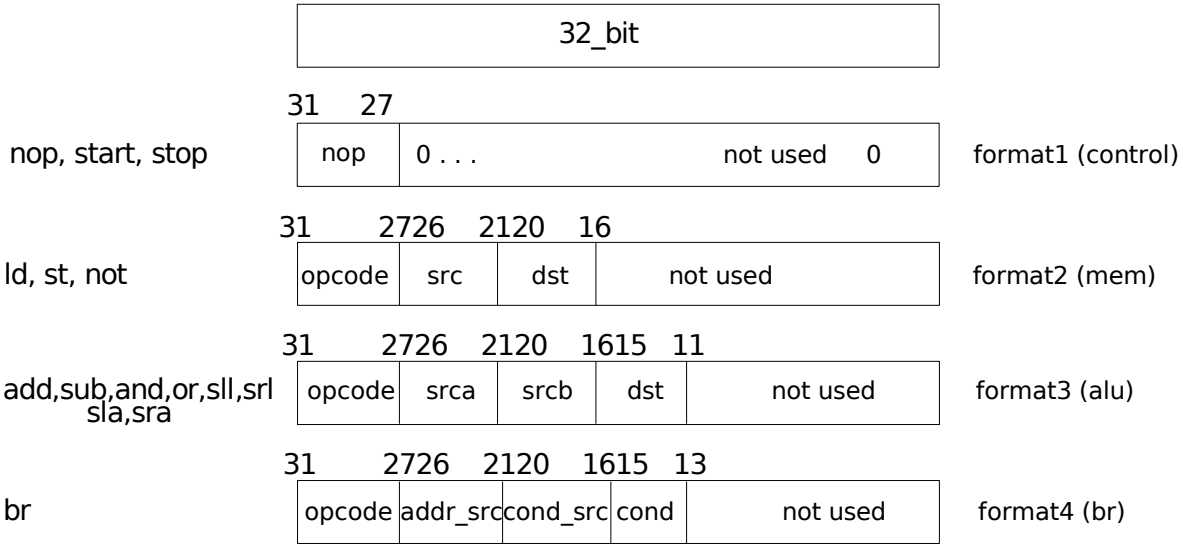


Data Memory(dm)



Execution Unit(eu)





	opcode	op
format 1	00000	nop
	00001	start
	00010	stop
format 2	01000	ld
	01001	st
	01010	not
format 3	10000	add
	10001	sub
	10010	and
	10011	or
	10100	sll
	10101	srl
	10110	sla
	10111	sra
format 4	11000	br