

CHAPTER 1 Basics

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FIGURE 1.1

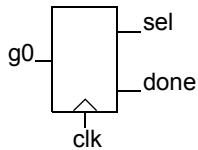
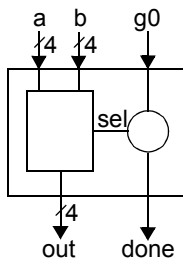


FIGURE 1.2



make the connections and use the proper logic below so that you can add two bits per cycle and then design the state machine to run this.

FIGURE 1.3

