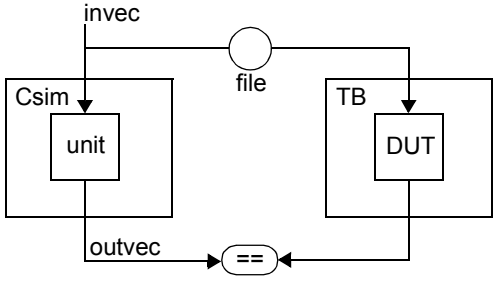
CHAPTER 1 Company Meeting Handout

1.1 CSL concepts (23.07.2006)

Three main stages of chip testing:

- RTL (Register Transfer Logic)
- Testbench (TB)
- C++ simulator (Csim)

FIGURE 1.1 Stages of chip testing



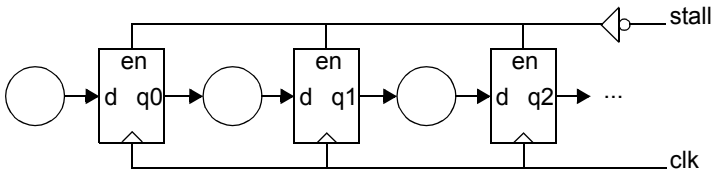
*DUT stands for design under test

1.1.1 Interface consistency problem

If the interface of the RTL (the width of a vector) were to unexpectedly be modified by the hardware designer for certain reasons, the testbench and the C++ simulator would run into problems (even crash) and the resulting testing operation will fail. This shows the need to have interface related data (such as vector dimensions) automatically generated (the interface consistency problem)

1.1.2 The pipeline process

FIGURE 1.2 Generic Pipeline



DFF code:

```
class reg {
  d,q
  reg() { master_register_array(this) };
  d writeData();
  propagate() { q=d; }
}

reset();
while(1) {
  clk();
  generate();
  propagate();
}
postprocessing();
```

clock signal generation code:

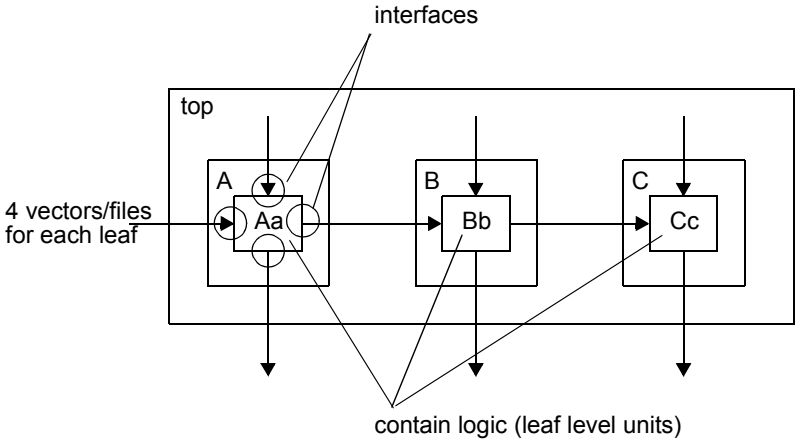
```
clk() {
  if(clk!=x) // x is a preset value
    clk++;
  else
    clk=0;
}
```

1.1.3 Design repository

A design repoository is a:

- set of specific files which describe our design
- leaf level units (contain logic)

FIGURE 1.3 Bottom up testing



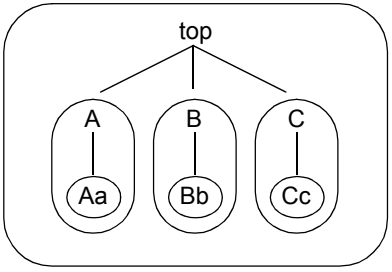


FIGURE 1.4 Binary file comparison

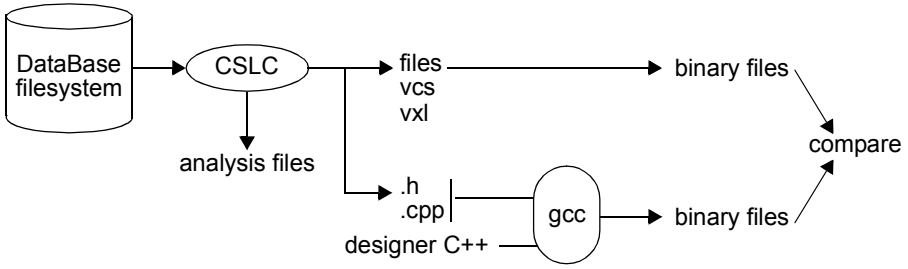
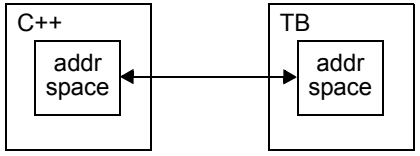


FIGURE 1.5 Managing memory addresses



Use a STL map to load values into registers

TABLE 1.1

address	register
0	*a
1	*b
2	*c
3	*d

1.1.4 General Block diagrams

FIGURE 1.6

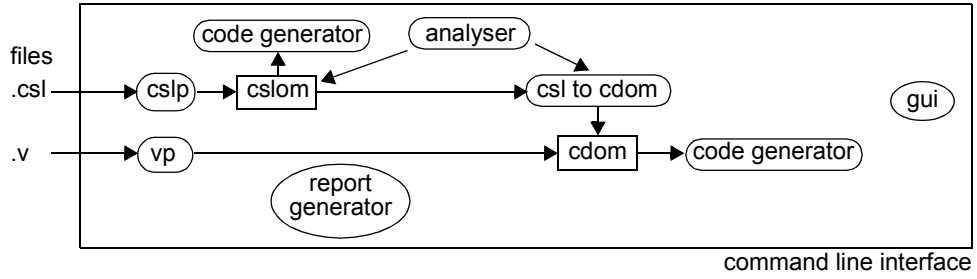


FIGURE 1.7