What Comes After Verilog?

"An Analysis of the North American Marketplace for Front-End EDA Tools"

by

The Telesis Group

August 10, 2006

Table of Contents

Introduction

Over the past decade, a number of technical and market factors have impacted the practice of developing high-performance, digital systems & products --- *e.g., dotcom meltdown, growth of outsourcing, SystemVerilog and SystemC, 90 nanometers, etc.* Of specific interest (and was the driving force for this report) were those factors affecting the adoption of front-end, EDA tools & processes: Architectural Modeling, Detailed Design, and Design Verification.

To obtain a deeper insight into the impact of these factors, a market-analysis project was undertaken focused on the following goals:

1. *for* The Telesis Group – obtain additional case information from which to base recommendations regarding the successful introduction of a new product into a mature marketplace such as EDA.

2. *for* Bluespec [(1)] – seek an independent assessment of the EDA marketplace they are targeting.

3. *for* both Parties – identify any under-served application needs.

The "raw data" for this analysis was obtained from a combination of Internet-based surveys and live telephone & in-person interactions totaling 144 participants representing some 76 companies. The companies ranged in size from startups to the very largest chipmakers.

To provide a balanced viewpoint, some recent Industry articles are included that complement the general problems and solutions covered in this report. – See Industry Articles– Page 18.

(1) ***www.bluespec.com*** *co-sponsored this project*

Summary

Using a time horizon of 3-5 years, the project started with the question
"What Comes After Verilog?"
and was the segue to probe at the issues to be addressed to improve the probability of success of first-pass silicon:

- *What are the issues?*
- *What solutions are you considering for adoption?*
- *What new EDA capabilities do you want beyond what you have today?*
- *What costs & tradeoffs are you willing to incur to obtain these new capabilities?*
- *What criteria, what process do you use to evaluate new EDA tool and vendors?*
- *What obstacles may limit the adoption of any new tool or process?*

Findings

Driving Forces for Something New in EDA

The survey reinforced the (widely reported) intention to adopt SystemVerilog and SystemC over the next 3-5 years as driven by two expectations:

- Provide significant improvement in 1st Pass silicon (FPGA, SoC, ASIC)
- Facilitate the on-time achievement of development schedules.

A reading of in-between-the-lines, however, of the "raw data" indicates skepticism of just what percentage of the claimed benefits will ever be achieved.

Obstacles to be Overcome for a New EDA Tool

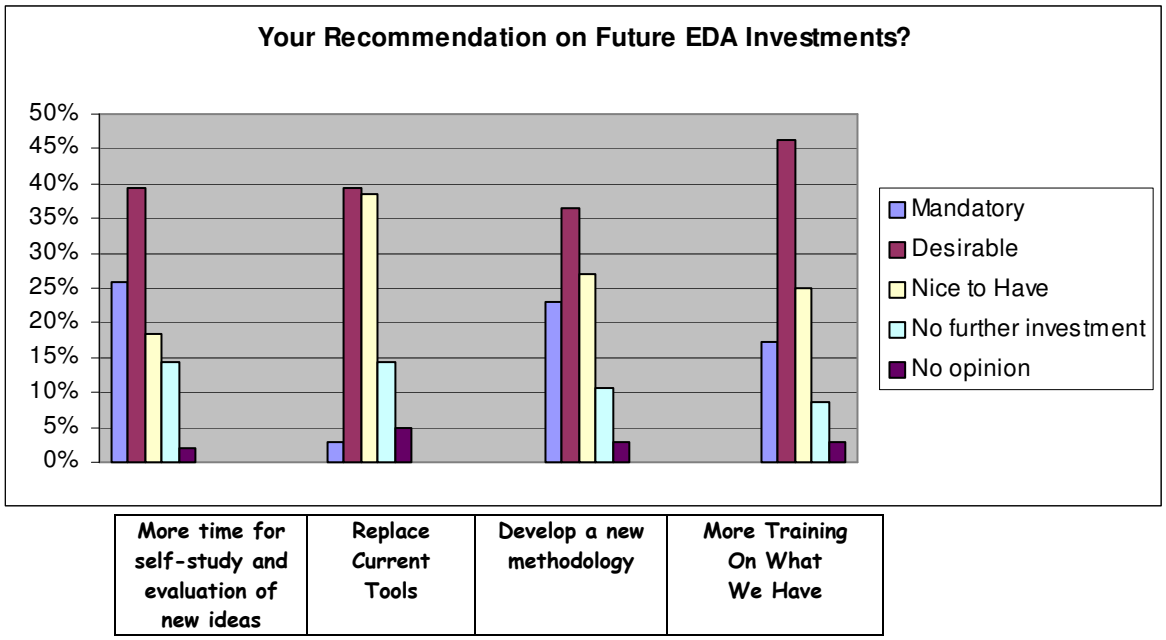
No one issue stood out as the limiting factor to the adoption of a new tool. Rather, the obstacles are a blend of factors relating to: corporate culture, product maturity, compatibility with existing process, time (or the lack thereof) to spend in evaluating, learning and then deploying, and just how many people and processes have to change in order to fully benefit from the new offering.

Probability of Adoption of SystemVerilog and SystemC

Applied To	SystemVerilog	SystemC /C++
Architectural Modeling	less than or equal to **25%**	greater than **75%**
Detailed Design (RTL)	in the range of **25-75%** *depends on whether Assertions is the driving force*	less than or equal to **25%**
Design Verification	greater than **75%**	greater than **75%**

Relative Importance of Future Investments

What to invest in over the next 3-5 years? --- More of what they already have? Replace with something new? The participants were about equally split on what (EDA) investments they would recommend to their management.

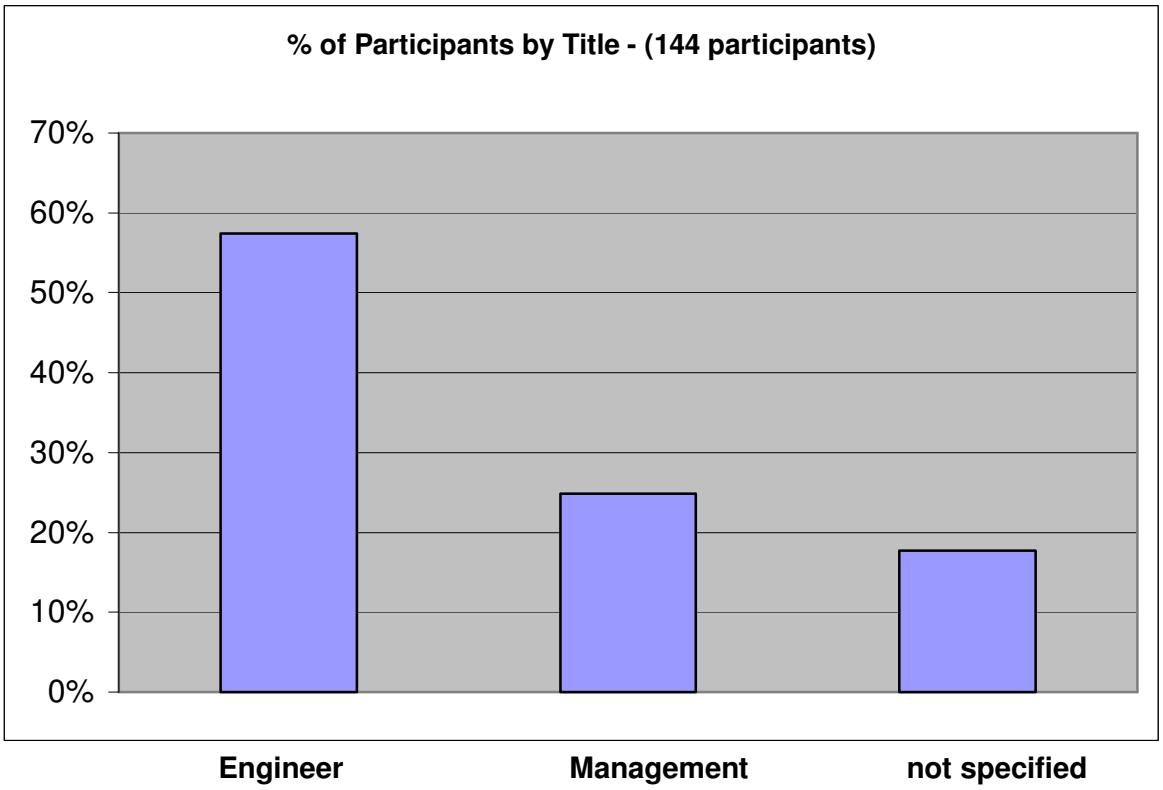


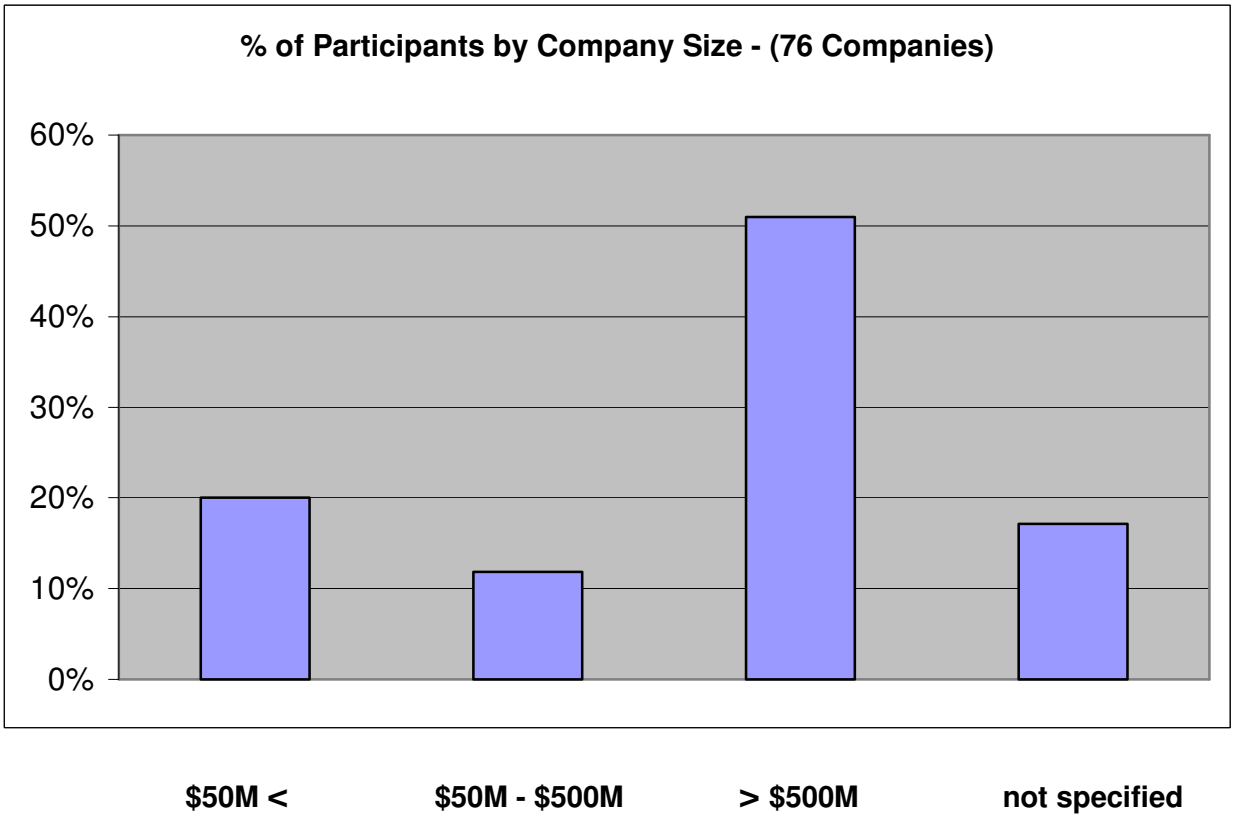
Under-served Opportunities?

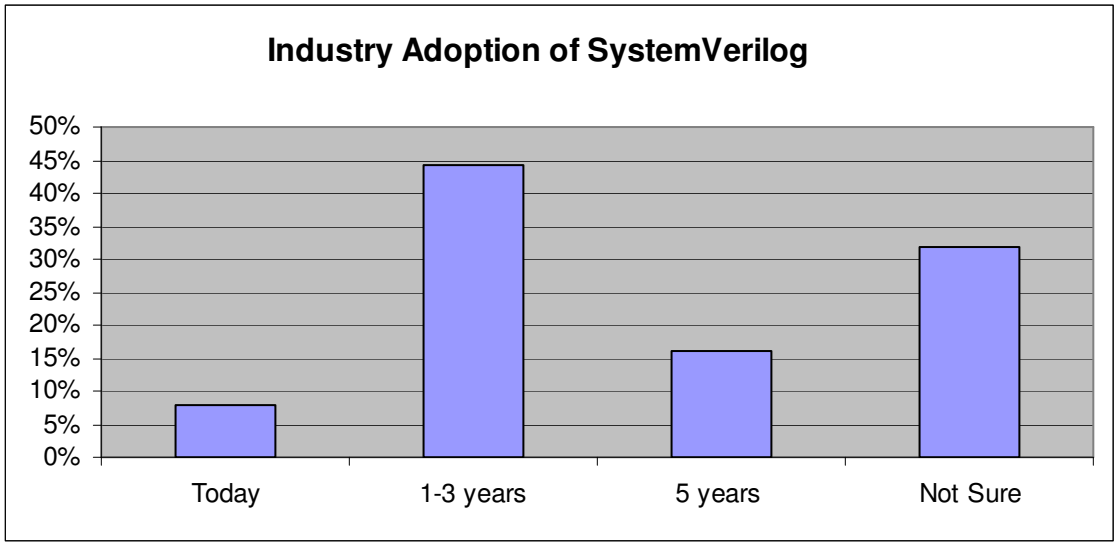
The survey indicated under-served needs in the areas of:

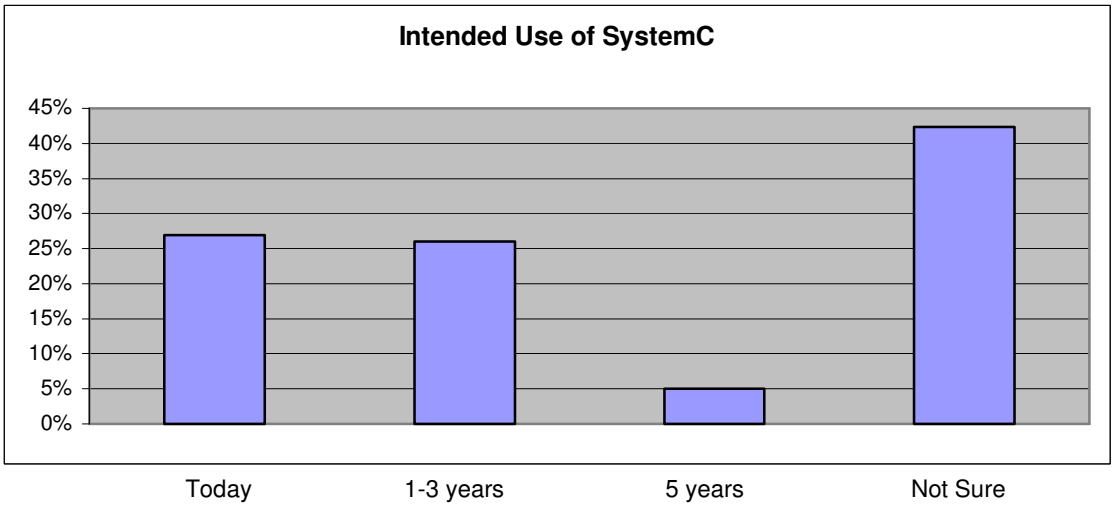
- Integration of IP
- Evaluation of Various Implementation Alternatives
- Power Estimation
- Development, Management and Enforcement of Customer / Design Specifications

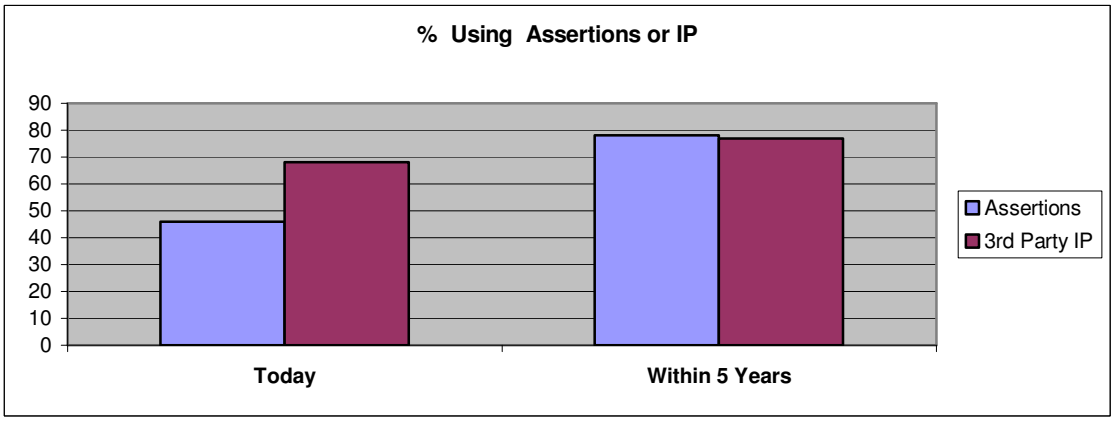
Statistically Speaking

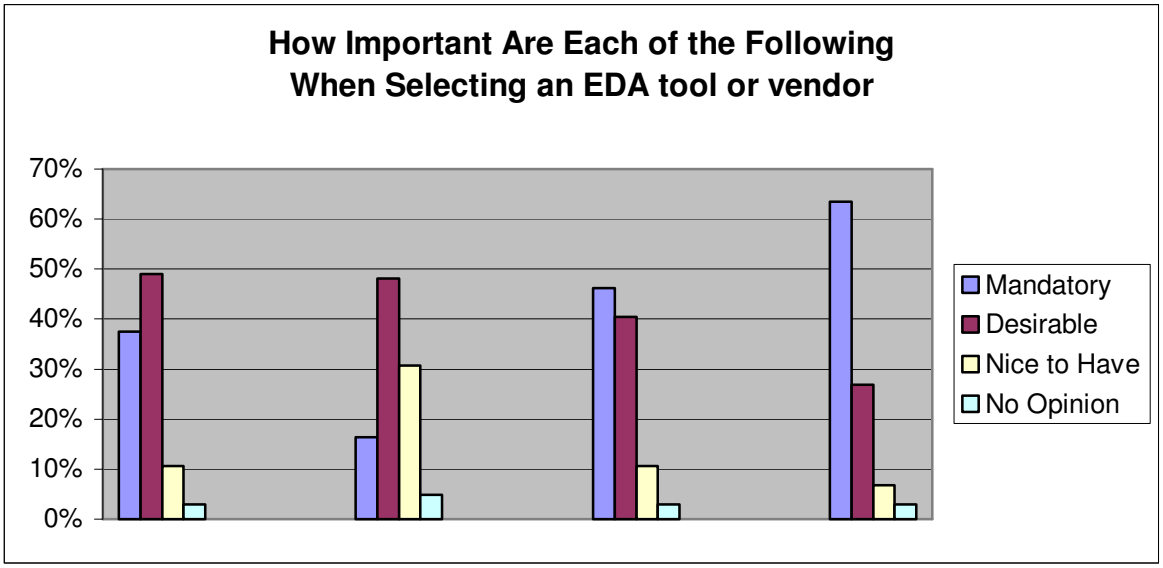


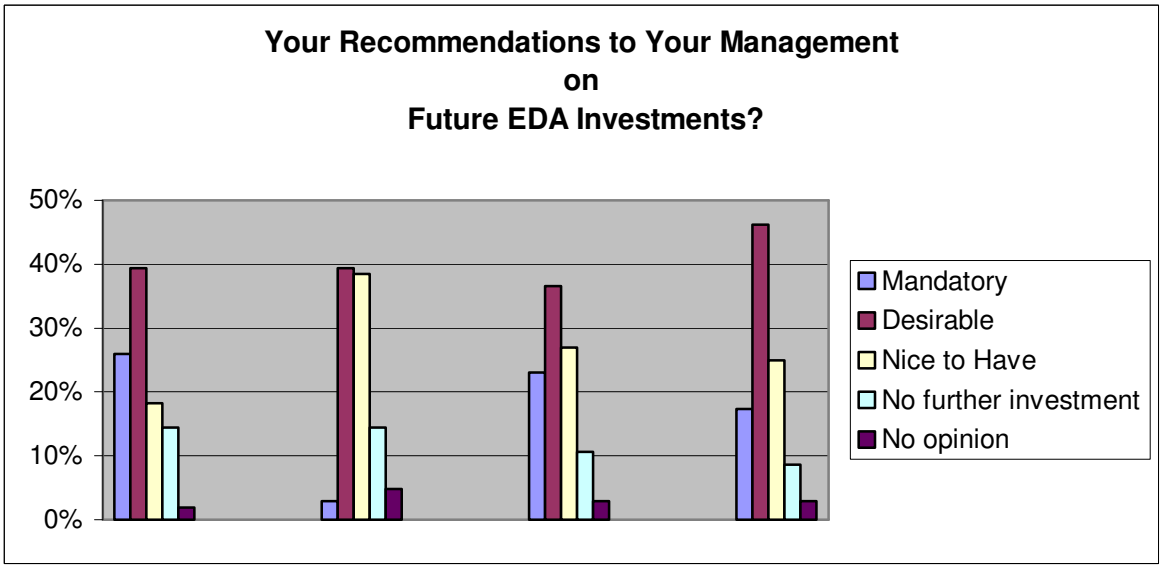












SystemVerilog -- Conflicting Data??

This report had two sources of data: 1) Internet-based Survey and 2) Live Interviews (phone and in-person). Overall, there is good agreement between the two sources except in one area –----- the adoption of SystemVerilog.

The Dichotomy

From the Internet Survey responses, one would conclude that the probability of SystemVerilog becoming the language of choice for all three-application areas (Architectural Modeling, Detailed Design and Design Verification) is about 70%.

The data from 22 of the participants who both filled-out the survey and who were also interviewed also supported the position that there was a 70% chance that the industry would be using SystemVerilog, **BUT** only 60% of these participants indicated they would actually be using SystemVerilog themselves. Furthermore, 85% of these participants indicated they would be using SystemC within 5 years.

Reconciliation

The following is offered as a reconciliation of this data and represents an estimate of the probability of adoption of these two technologies over the next 5 years.

Probability of Being Adopted

Applied To	SystemVerilog	SystemC /C++
Architectural Modeling	less than or equal to **25%**	greater than **75%**
Detailed Design (RTL)	in the range of **25-75%** *depends on whether Assertions is the driving force*	less than or equal to **25%**
Design Verification	greater than **75%**	greater than **75%**

Anecdotally, *"heard on the street"*

On IP

"I am locked into my IP vendors -- can't use anything they aren't using"

"We have to do a lot of rework on the IP before we can use it"

"We have a lot of internal IP -- but the originals keep getting changed so much that I might as well have done it from scratch – isn't there away to describe IP so that it can truly be reused"

"We have tons of IP (internal and external) and whatever (new tool) we adopt has to compatible with this IP"

"We are moving away from VHDL so that we can take advantage of the 3rd party IP"

On New Tools

"A new tool? Great! Give it to me -- I might spend 3 weeks over the next 6-12 months"

"We don't need new tools, we need more time to leverage what we have"

"selecting new tools? overcoming resistance to change? -- comes down to the same success factors as getting the product out on time, on quality, on budget -- the technical management"

"we use a number of tools from several vendors -- if something new comes to market we need compatibility across the board with all our tools -- not one or two"

Resistance to Change

"why should I be the guinea pig, let someone else debug it"

"we don't have the time or the staff to look at anything new"

"we will simply wait until we see that we will probably fail without it, then we will switch "

"I don't listen to a salesman's pitch (about a new tool), I want to talk to the design engineers at companies who have successfully deployed it"

"We will take risks in the marketplace – we won't take risks getting there"

Time, Cost, etc

"I will invest in whatever it takes to reduce the number of errors in 1st Pass silicon (SoC, ASIC or FPGA)"

"My problem isn't Verification –my problem is getting the 1st Silicon to Pass"

"Cost be damned – I just can't get the PERFORMANCE out of this one particular Subsystem – I need to look at some alternatives but every minute I do I am holding up the whole product line and my bonus check"

"Design takes place in several (geographically dispersed) sites ---- the tough problem is keeping them in sync"

"We don't need productivity tools – we need realistic schedules"

"reduce the time it takes? I would be ecstatic if I could just stay on schedule"

"we design it once and then change it forever"

"I can spend a couple of weeks and succeed in getting the timing to close ---but when it comes to Power ----that is another story"

"If I had the right tools to reconfigure my ARM, DSP, MPEG configuration, I might be able to reduce the POWER consumption by 25%"

"The big challenge going forward is POWER – consumption, dissipation, distribution"

"Once the company recognizes the impact of a respin time for a respin will be built into the overall product plan resulting in a pragmatic timetable"

On Architectural Modeling

"Need a way to declare the spec so we can sign off on the detail —especially with the customer"

"architectural modeling? – we put a couple of smart guys into a room with some pads of paper, a lot of #2 pencils and EXCEL ---voila' what they come up with is what we implement"

"We should be doing more Architectural modeling –but we don't"

On Verification

"if they (EDA vendors) gave me a magic tool that would cut my current Design Verification time in half, then I would verify for twice as long – maybe even longer"

"Reduce my verification time? I want to increase the quality of the result (1st Pass Silicon)"

"Everything is more or less a block box – need to put blocks together and know (instantly) they will work (or not) so I can concentrate on system level verification"

"SystemVerilog is to be our gateway into adopting Assertions"

"Assertions are fine for checking design intent but not architectural (system) intent
The functions we can Assert, we could already Verify,
the stuff we have problems with are we don't have detailed specs to Assert"

"There are many benefits to having the designer responsible for writing assertions
but it is like pulling teeth to get them to do it
---- we end up with the verification engineers writing the assertions"

Findings, *"what I think it all means"*

Driving Forces for Something New in EDA

The survey reinforced the (widely reported) intention to adopt SystemVerilog and SystemC over the next 3-5 years as driven by two expectations:

- Provide significant improvement in 1st Pass silicon (FPGA, SoC, ASIC)
- Facilitate the on-time achievement of development schedules.

A reading of in-between-the-lines, however, of the "raw data" indicates skepticism of just what percentage of the claimed benefits will ever be achieved.

SystemVerilog for? Verification RTL Architectural Modeling

Overall, the survey indicated a widespread intention to adopt SystemVerilog for Design Verification -- *not much of a surprise given its roots in VERA*. When queried, however, about its application to RTL or Architectural modeling, the reasons given for adoption were fuzzy except for its Assertion functionality.

Architectural Modeling

The large majority of organizations (independent of size) do not have a formal architectural design process. A number of companies have tried to use C/C++ for such modeling. Without a way, however, to generate hardware directly from this source, the design has to be completely re-written for detailed implementation. This creates a huge gap from Model to Hardware. Sections of the design may be analyzed / simulated, but in the main, the "tools" being used for architectural modeling today are:

"paper, pencil, EXCEL and a few smart engineers"

Adopting a formal process for Architectural Modeling appears to be limited by a lack of:

- Expertise in performing the modeling;
- Adequate time to perform the analysis;
- Accurate & complete starting point documentation;
- A unified methodology that facilitates the reuse of Architectural Modeling output in the downstream RTL design and verification process.

On the flip side, there is growing pressure to get the design right the first time (1st Pass Silicon) as reflected by the customer's viewpoint (requirements / specifications) and as implemented by engineering. What is indicated is a need for a formal method for declaring the product specifications usable at every step in the product development process.

SystemVerilog vs SystemC

The debate as to which language is best for Design Verification will rage on and on.

SystemC/C++/C is expected to be the most widely adopted tool in architectural modeling, while on the flip side, SystemC for RTL design does not seem to hold much favor.

It does not appear that SystemVerilog / Verilog-2005 will replace Verilog 95 /2001 en masse' for RTL design any time soon. This survey indicated that there was more use of Verilog 95 than Verilog 2001 – *some 4-5 years after its first delivery and 9 years after it was first announced.*

Verilog vs VHDL

Although a representative number of companies contacted were using VHDL, most of them choose not to participate based on what I can only surmise to be one or more of the following reasons:

"we are VHDL, nothing new is coming down the pike – so why talk about its successor?"

"why would we want something that was inferior to VHDL?"

"we got what we got and we ain't switching!"

For those companies who did participate and are migrating from VHDL to Verilog, they seemed to have their hands full for the next few years with this migration and didn't put SystemVerilog or SystemC high on their priority list ---they were much more focused on: infrastructure, IP and training.

Obstacles to Adoption of New EDA Tools

There are four anecdotes that encapsulate the obstacles to be addressed for the successful introduction of something new in the front-end EDA space.

"It ain't broke so why fix it"

"OK, but I will go slowly and on an incremental basis"

"I still have not deployed most of the good stuff that I bought 18 months ago"

"they should just stop talking and show me the silicon that was produced using it"

There was no one issue that stood out as the limiting factor to the adoption of a new tool. Rather, the obstacles were based on a blend of the following:

- Maturity – *"why should I pay to be a guinea pig"*
- Compatibility –*"does it produce output that my downstream processes can use"*
- Interoperability – *"do all the tools work together"*
- Training & Learning Curve –*"we will adopt it incrementally"*
- Pricing –*"my current vendor will give it to me at no additional cost"*
- Uncertainty –"*what I got now produces chips – does theirs?"*
- CHANGE – *"how many of my staff have to make a (disruptive) change?"*
- Compatibility with Legacy – *"have tons of modules that I need to reuse"*
- SO WHAT? ---*"what do I get out of using it?"*
- Catch 22 –*"I have customers and vendors who supply IP – can't adopt anything new until they adopt it– and they won't adopt until we adopt"*
- One Size Fits Does NOT Fill All --*"just as no one microprocessor or DSP chip can be used for all designs, no one language can be used (optimally) for all design types -- so let's be at the task of finding ways to formally mix 'n match the best tool for the application and in particular having one set of models (libraries) that can be used in all three applications".*
- Variations on a Theme Need Not Apply -- *"until the vendors (at least the major ones) support one standard in a consistent manner, I will not push for widespread adoption within my enterprise".*

Under-served Opportunities?

This analysis identified the following under-served needs:

1) Integration of IP
A rapid, less error prone way to "stitch" the IP together –that is, a way for the design team to rapidly get an indication that two pieces of IP work together (or don't).

2) Implementation Alternatives - to empower the product team to evaluate:

- Alternatives to provide a better tradeoff of conflicting customer requirements
- Alternative sources of IP
- Alternatives to improve performance

3) Power Estimation – provide at the planning stages a means of exploring alternate forms of implementation and their impact on both consumption and local & global distribution.

4) Specifications – Starting with customer requirements: How to Declare, Manage and Enforce Compliance for the critical functional and performance criteria. Is there a possible direct path from Product Specs to System Level Modeling to RTL without have to completely rewrite at each step?

OpEd

What if solutions for such Under-Served Opportunities were available today?

Would this be enough to foster widespread adoption?

I am just not sure!

For sure, the issues of legacy, interoperability, training, learning curve, and reliability must be addressed; but given that; there are still several factors that will significantly influence their rate of adoption of any such solutions.

By the User Community, there needs to be:

- Management who insists on objective assessment of alternative product configurations based on some critical product parameters as defined by all the stakeholders.
- A commitment to develop schedules that are constructed allocating more time in the up-front steps of the development process yielding a reduction in the overall schedule and increase in quality.
- A dramatic improvement in how the product requirements are specified, documented and compliance measured to.

By the EDA Vendors
Even as evidenced in parts of this paper, the vendors' value propositions are too often couched in *"motherhood and apple pie"* or focus on the detailed descriptions of the technology. Neither approach is very effective in convincing users and their management to part with their money. The vendors simply do not make a case that their vision for the future resonates with that of customer. What if the EDA vendors were to put more effort into proving how their claims map into customer solutions or in the words of some participants? For ESL to fulfill its potential the EDA vendors will have to help to educate the marketplace with hard data that supports their value propositions.

"free downloads, evaluation copies -- they're kidding! – what about my costs (real and opportunity) to prove their claims – they should be paying us!"

"can't they just stop talking about the guts of SystemVerilog or SystemC and show me the roadmap that I have to follow to benefit from it?"

"how long (in both effort & calendar time) will it take my best engineer to be productive?"

"what about my not-so-best engineers?"

"what can they show me that proves that it works?"

"what do I have to change in what I am doing now – how long, how much $$?"

"how long will it take to be as productive on the new as I am with the old?"

"who is going to get today's job done while they are coming up to speed?"

The easiest part of all the above will probably be, that which has to be done by the EDA vendors. You (those skilled in the art of developing high-performance, digital systems) must create the demand for such changes within your enterprise ---the EDA vendors will surely follow
---– *not unlike a Field of Dreams but in reverse.*

Industry Articles

To provide a balanced viewpoint, some recent Industry articles are included that complement with the general problems and solutions covered in this report.

ESL Now! Survey
www.esl-now.com
July, 2005

Results from the 141 Respondents to the ESL Now! Online Survey covering the following topics:

- *How much of your next design will be created from the reuse of existing IP?*
- *Agreement/Disagreement with productivity increases when using ESL methods?*
- *What is driving your company to adopt ESL?*

http://www.esl-now.com/pdfs/survey_results.pdf

EETimes and Deutsche Bank EDA Survey
Summer, 2005

An exclusive survey conducted by EE Times and co-sponsored by Deutsche Bank of EDA users at the 2005 Design Automation Conference. The survey covered 339 ASIC/IC designers, 116 FPGA designers and 698 PCB designers. Richard Goering provides insights into the results. The report covers five typical global design teams and the challenges they are facing.
http://www.eet.com/edasurvey

Mentor Graphics – January, 2006
by
Shawn McCloud, Product Line Director of High Level Synthesis

Mentor Graphics conduced a survey of European electronics professionals to find out about current and former applications, general design problems they have encountered and their perceptions and experiences with electronic system level design methods.

http://www.mentor.com/products/c-based_design/upload/ESL_Survey_Report_EU.pdf

http://www.electronicsweekly.com/Articles/2006/02/03/37527/IndustrysurveyWhatisitwithESL.htm

"A New Generation of ESL Tools To Generate EDA Revenue Growth"
Summer, 2005 and April, 2006
by
Daya Nadamuni of the Gartner Group

Three articles by the Gartner Group showing that the demand for ESL tools, which integrate hardware and embedded software design, will grow rapidly.

http://www.gartner.com/resources/129700/129769/gartner_highlights_semicondu_129769.pdf

http://www.gartner.com/resources/132100/132194/systemonchip_worldwide_marke_132194.pdf

http://gartner11.gartnerweb.com/DisplayDocument?doc_cd=132194

A Census of 338 Engineers on Design Verification Tool Use
October, 2005
by
John Cooley

CADENCE SYSTEMC -- Overall SystemC adoption is only at 42% in 2005. Pretty much only the verification/modeling crowd are using SystemC. Few hardware designers are using/thinking SystemC as an implementation language.
http://www.deepchip.com/items/dvcon05-03.html

SYNOPSYS MESSES UP -- Last year users were waiting for Cadence and Mentor to support System Verilog in their tools. Oops! Everyone *assumed* Synopsys would have System Verilog fully implemented in the SNPS flow -- wrong! This year Synopsys *should* deliver on System Verilog, but until then it's still only 1 in 5 engineers using/thinking System Verilog. Oops.
http://www.deepchip.com/items/dvcon05-04.html

To each participant, my sincere, Thank You !
I hope you will find this report to be of value as you formulate
your going-forward investments in EDA.
Your additional feedback and questions are most welcome.

The Telesis Group also wishes to thank Bluespec, Inc (www.bluespec.com)
for co-sponsoring this project; and especially
for the freedom to conduct it with no "commercial interruptions"

Jozef Sliwkowski
The Telesis Group
40 Candy Hill Road
Sudbury, MA 01776
978-443-2966 (0)
978-246-0249 (f)
jozef_sliwkowski@verizon.net
www.sliktimes.com