Table 4. Register 2-Polarity Inversion Register

BIT	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Default	1	1	1	1	0	0	0	0

Table 5. Register 3-Direction Register

BIT	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Default	1	1	1	1	1	1	1	1

Table 6. Register 4-Status Register

BIT	S7	S6	S5	S4	S3	S2	S1	S0
Default	x	x	x	x	x	x	x	1