|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Op** | **RegDst** | **RegWrite** | **ExtOp** | **ALUSrc** | **Beq** | **Bne** | **J** | **MemRead** | **MemWrite** | **MemtoReg** |
| R-type | 1 | 1 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **addi** | 0 (rt) | 1 | 1 (sign) | 1 (Imm) | 0 | 0 | 0 | 0 | 0 | 0 |
| **slti** | 0 (rt) | 1 | 1 (sign) | 1 (Imm) | 0 | 0 | 0 | 0 | 0 | 0 |
| **andi** | 0 (rt) | 1 | 0 (zero) | 1 (Imm) | 0 | 0 | 0 | 0 | 0 | 0 |
| **ori** | 0 (rt) | 1 | 0 (zero) | 1 (Imm) | 0 | 0 | 0 | 0 | 0 | 0 |
| **xori** | 0 (rt) | 1 | 0 (zero) | 1 (Imm) | 0 | 0 | 0 | 0 | 0 | 0 |
| **lw** | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| **sw** | x | 0 | 1 (sign) | 1 (Imm) | 0 | 0 | 0 | 0 | 1 | x |
| **beq** | x | 0 | x | 0 | 1 | 0 | 0 | 0 | 0 | x |
| **bne** | x | 0 | x | 0 (BusB) | 0 | 1 | 0 | 0 | 0 | x |
| **j** | x | 0 | x | x | 0 | 0 | 1 | 0 | 0 | x |

Main control signals^