Introduction to Digital Logic
EECS/CSE 31L

Assignment 3

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Due on Saturday 11/1/2014 11:00pm. Note: this is a one-week assignment

1 Implementing a 32-bit ALU [100 points + 5 bonus points]

The goal of this assignment is to practice multi-component logic design in VHDL and learn how to build a 32-bit Arithmetic and Logic Unit (ALU) at both structural and behavioral levels.

1.1 Assignment Description

The objective of this project is to assess your understanding of how to implement a complicated combinational hardware block using the codes you have developed in the last assignment. In this assignment you are supposed to implement a 32-bit ALU using 1-bit ALU component you have already developed in Assignment-2. Also consider using GENERATE statement for instantiating 1-bit ALU components. In this assignment you are supposed to develop your own testbench for 32-bit ALU verification.

1.1.1 ALU Entity

Code 1: Sample entity of 32-bit ALU in VHDL

```
ENTITY alu_32bit IS
 PORT(
  A         : IN STD_LOGIC_VECTOR(31 DOWNTO 0);
  B         : IN STD_LOGIC_VECTOR(31 DOWNTO 0);
  opsel     : IN STD_LOGIC_VECTOR(2 DOWNTO 0);
  mode      : IN STD_LOGIC;
  output    : OUT STD_LOGIC_VECTOR(31 DOWNTO 0);
  cout      : OUT STD_LOGIC
 );
END alu_32bit;
```

1.1.2 ALU Description

The ALU is supposed to have the following functionalities both in Arithmetic and Logic computing. a and b are 32-bit data inputs, shown as A and B in the entity description, respectively. Output is the *output* port.

Table 1: ALU operation description

mode	**opsel**	**Micro-operation**	**Description**
0	000	$a + b$	Add
0	001	$a + \bar{b}$	Sub with borrowed carry
0	010	a	Move
0	011	$a + \bar{b} + 1$	Sub
0	100	$a + 1$	Increment
0	101	$a - 1$	Decrement
0	110	$a + b + 1$	Add & Increment
1	000	$a\ AND\ b$	bit-wise AND
1	001	$a\ OR\ b$	bit-wise OR
1	010	$a\ XOR\ b$	bit-wise Exclusive OR
1	011	$\bar{a}$	Compliment
1	101	shl	32-bit shift left

1.2 Assignment Deliverables

Your submission should include the following:

- Design report of ALU
- Waveform snapshot for each function
- ALU design VHDL code files
- ALU Testbench VHDL code file

Note: Remember to compress all VHDL files (with rar or zip extension) and name your compressed file as **assignment3_STUDENT-ID_alu.rar** and your report as **assignment3_STUDENT-ID_alu.pdf**.