

Introduction to Digital Logic EECS/CSE 31L

Assignment 4 Design Report Designing RAM

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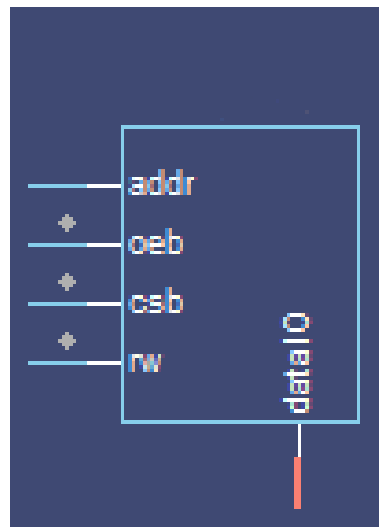
1 BLOCK Description

This is a 32-bit RAM that can read and write a 32-bit number in 2048 different addresses. It has a chip select option which allows the user to select which chip the RAM will be using as well as a output disable to stop the RAM from reading a number. The read and write function cannot run at the same time, so this RAM can either read or write at a given time.

2 Input/Output Port Description

Port Name	Port Size	Port Type	Description
addr	11	IN	Address location
rw	1	IN	Read/Write Enable
csb	1	IN	Chip Selector
oeb	1	IN	Output Disabler
dataIO	32	IN/OUT	Signal for Input and Output

3 Design Schematic



4 Wave

11'h001	11'h003		11'h001	11'h000		
32'h00000001	32'h00000003	32'h00000003	32'h00000001	32'h00000000	32'h00000001	