Introduction to Digital Logic
EECS/CSE 31L

Assignment 1 Design Report Sample
Designing Combinational Circuits

prepared by: Pooria M.Yaghini
Student ID: 12345678

EECS Department
Henry Samueli School of Engineering
University of California, Irvine

October, 18, 2014

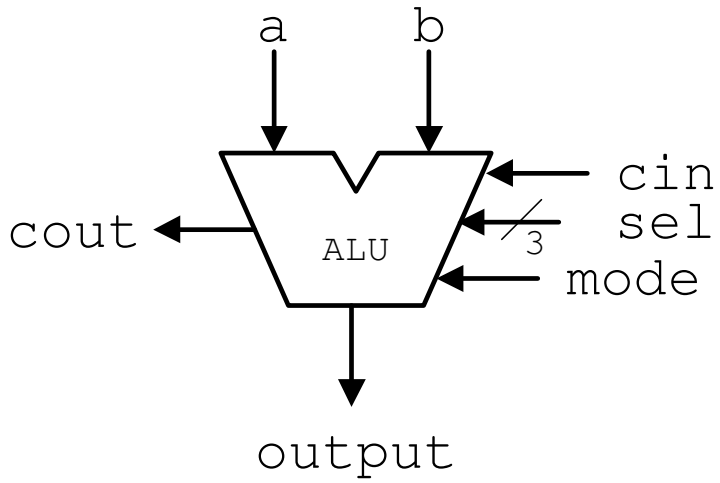
1 BLOCK Description

This block is designed to get 2 input, perform operation X.

2 Input/Output Port Description

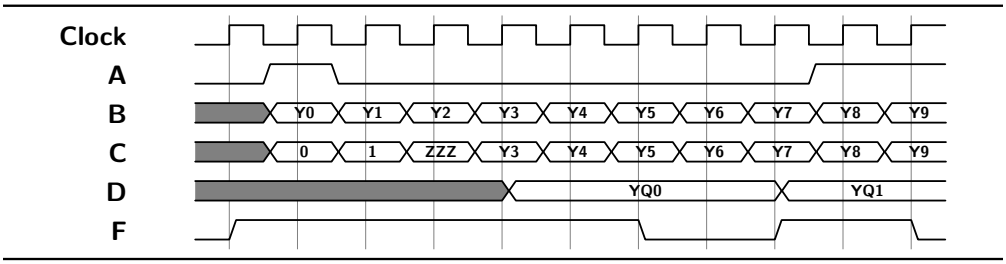
Port name	Port size	Port Type	Description
input0	1	IN	gets the first operand
input1	1	IN	gets the second operand
output	1	OUT	will have the operation result

3 Design Schematic



4 Expected and Simulation Waveform

Expected Waveform is as follows:



Simulation Waveform is as follows: