

Introduction to Digital Logic EECS/CSE 31L

Assignment 4 Design Report Designing Register

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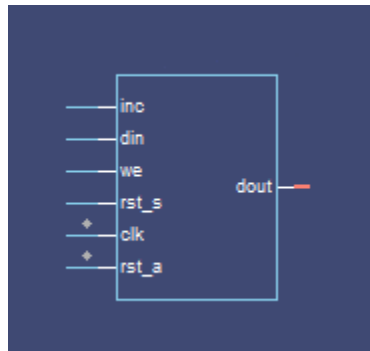
1 REGISTER Description

This 32-bit register is designed to receive a 32-bit input and read out the 32-bit input as the 32-bit output if write enable is active. It supports asynchronous and synchronous resets, meaning when the asynchronous signal is enabled, the output will be 0 whether the clock signal is on or off and when the synchronous signal is enabled, the out should be 0 only when the clock signal is on. This design also features an incrementing feature, which increments the output by one.

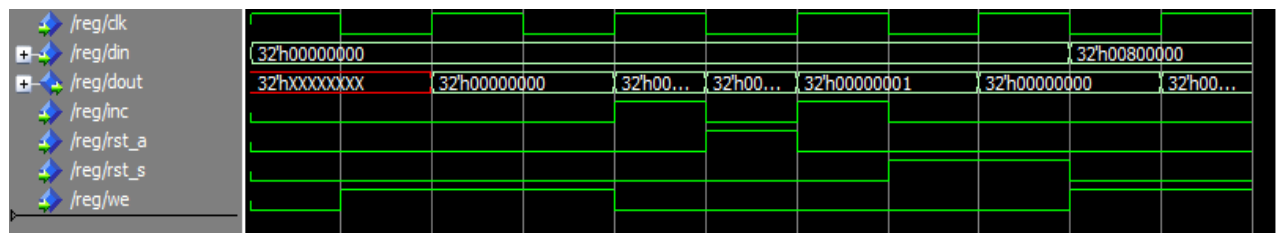
2 Input/Output Port Description

Port Name	Port Size	Port Type	Description
clk	1	IN	Clock Signal
rst_a	1	IN	Asynchronous Reset Signal
rst_s	1	IN	Synchronous Reset Signal
inc	1	IN	Increment Signal
we	1	IN	Write Enable Signal
din	32	IN	32-bit Input
dout	32	OUT	32-bit Output

3 Design Schematic



4 Wave Map



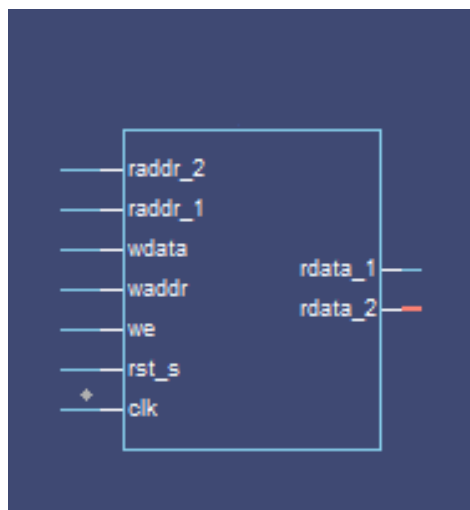
1 REGISTER FILE Description

This 32-bit Register File is a single-port register file that supports two read and one write at each clock cycle. This register file only has a synchronous reset and does not have an asynchronous reset, meaning the only way to reset the data is when there is a rising clock edge. Every time the rising clock edge appears, it will read two addresses the user inputs and writes a 32-bit into the address the user inputs.

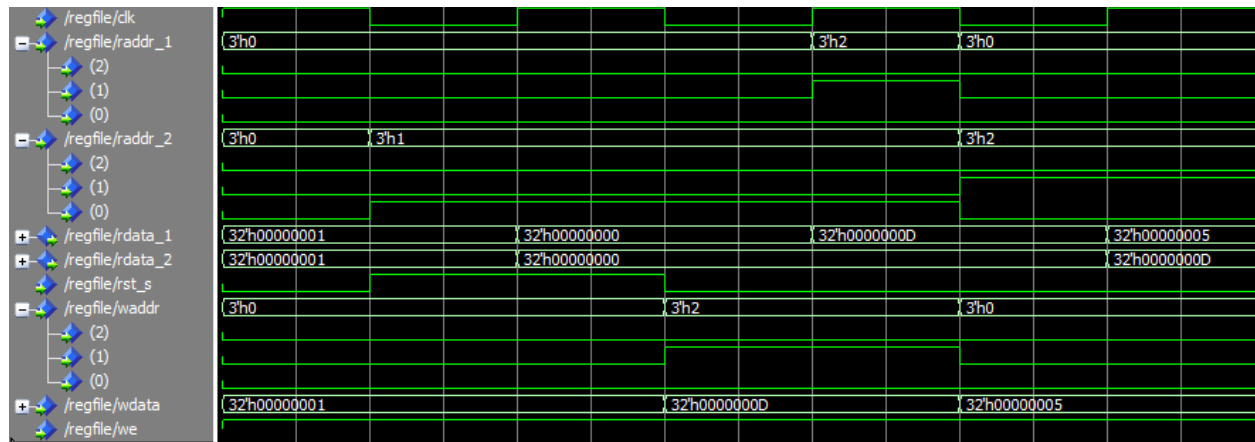
2 Input/Output Port Description

Port Name	Port Size	Port Type	Description
clk	1	IN	The Clock Cycle
rst_s	1	IN	Synchronous Reset Signal (1 = Reset)
we	1	IN	Write Enable Signal
raddr_1	3	IN	1 st Read Address Signal
raddr_2	3	IN	2 nd Read Address Signal
waddr	3	IN	Write Address Signal
rdata_1	32	OUT	1 st Read Data Signal
rdata_2	32	OUT	2 nd Read Data Signal
wdata	32	IN	Write Data Signal

3 Design Schematic



4 Wave



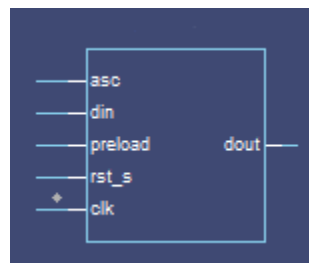
1 COUNTER Description

This 32bit counter takes a 32bit input and counts up or down depending on the ascending mode given, 0 meaning decrement and 1 meaning increment. This counter circuit is also synchronous, meaning it will rely on the clock cycle to take action, so only when the clock is 1, the counter will increment or decrement. The preload mode also enables the user to load their input into the counter. There is also a reset mode, where when enabled, all inputs and counts will return to 0.

2 Input/Output Port Description

Port Name	Port Size	Port Type	Description
clk	1	IN	The Clock Cycle
rst_s	1	IN	Synchronous Reset Signal (1 = Reset)
asc	1	IN	Ascending Signal (0 = Decrement, 1 = Increment)
preload	1	IN	Mode Selection (0=Arithmetic, 1=Logical)
din	32	IN	32-bit Input
dout	32	OUT	32-bit Output

3 Design Schematic



4 Wave

