Introduction to Digital Logic
EECS/CSE 31L

Assignment 1

University of California, Irvine

October, 11, 2014

Due on Saturday 10/18/2014 11:00pm. Note: this is a one-week assignment

Lab assignments in this course are defined in a way to employ different aspects of your knowledge required in logic design. The assignments span various levels of abstraction: gate, structural, and behavioral level. Each level needs its own metrics in order to prove the efficiency of your work.

1 Digital basic block design [100 points + 5 bonus points]

The goal of this assignment is to get familiar with the structure of VHDL and how to implement a digital schematic design at gate level in VHDL.

1.1 Assignment Description

The objective of this project is to assess your understanding of how to implement combinational hardware blocks using VHDL. In this assignment you are supposed to implement the following basic blocks in VHDL and verify to see they are working as expected. The blocks are:

Block 1: 4-input multiplexer

Block 2: 1-bit full adder/subtractor

Block 3: 1-bit comparator

Block 4: 2-bit encoder

Block 5: 1-bit decoder

1.1.1 Multiplexer

Code 1: Sample entity of 4-input multiplexer in VHDL

```
ENTITY mux4to1 IS
 PORT(
  in_0 : IN std_logic;
  in_1 : IN std_logic;
  in_2 : IN std_logic;
  in_3 : IN std_logic;
  sel_0 : IN std_logic;
  sel_1 : IN std_logic;
  f    : OUT std_logic
 );
END mux4to1;
```

1.1.2 Adder/Subtractor

Code 2: Sample entity of 1-bit full adder in VHDL

```
ENTITY addsub IS
 PORT(
  in_0:   IN std_logic;
  in_1:   IN std_logic;
  cin :   IN std_logic;
  AddOrSub:   IN std_logic;
  sum:   OUT std_logic;
  cout:   OUT std_logic
 );
END addsub;
```

1.1.3 Comparator

Code 3: Sample entity of 1-bit comparator in VHDL

```
ENTITY comparator IS
    PORT (
              in_0 : IN  STD_LOGIC;
              in_1 : IN  STD_LOGIC;
              greater   : OUT  STD_LOGIC;
              equal   : OUT  STD_LOGIC;
              less   : OUT  STD_LOGIC
      );
END comparator;
```

1.1.4 Encoder

Code 4: Sample entity of 2-bit encoder in VHDL

```
ENTITY encoder IS
    PORT (
              in_0 : IN  STD_LOGIC;
              in_1 : IN  STD_LOGIC;
              enable : IN  STD_LOGIC;
              f   : OUT  STD_LOGIC
      );
END encoder;
```

1.1.5 Decoder

Code 5: Sample entity of 1-bit decoder in VHDL

```
ENTITY decoder IS
    PORT (
              in_0 : IN  STD_LOGIC;
              enable : IN  STD_LOGIC;
              f_0   : OUT  STD_LOGIC;
              f_1   : OUT  STD_LOGIC
      );
END decoder;
```

1.2 Assignment Deliverables

Your submission should include the following:

- Design report of each block
- Waveform snapshot for each block
- VHDL code file for each block

Note: Remember to name your files as **assignment1_STUDENT-ID_BLOCK-NAME.vhd** and **assignment1_STUDENT-ID_BLOCK-NAME.pdf**.