Introduction to Digital Logic
EECS/CSE 31L

Assignment 5

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November, 15, 2014

Due on Saturday 11/22/2014 11:00pm. Note: this is a one-week assignment

1 RAM Design [100 points + 5 bonus points]

The goal of this assignment is to practice sequential logic blocks in VHDL.

1.1 Assignment Description

The objective of this project is to assess your understanding of how to implement a Random Access Memory (RAM) blocks. This RAM design will be used as a data memory in the processor design project later.

The RAM block contains 2048 lines, each line 32 bits. It has active-low Chip Select ($\overline{CS}$), active-low Output Enable ($\overline{OE}$), and Read/Write ($R/\overline{W}$) control signals. The top-level data port is used for both input and output. The RAM, should be implemented with 512x32 memory blocks.

Table 1: RAM operation description (X, H, and L represent don't care, High, and Low, respectively.)

$\overline{CS}$	$\overline{OE}$	$R/\overline{W}$	**Mode**	**dataIO**
H	X	X	Not Selected	High Z
L	H	H	Output Disable	High Z
L	L	H	Read	Data Out
L	X	L	Write	Data In

Code 1: Sample entity of a RAM in VHDL

```
ENTITY ram IS
   port (
        addr   : IN std_logic_vector(10 DOWNTO 0);
        rw     : IN std_logic;
        csb    : IN std_logic;
        oeb    : IN std_logic;
        dataIO  : INOUT std_logic_vector(31 DOWNTO 0));
 END ram;
```

Note: Remember to compress all VHDL files (with rar or zip extension) and name your compressed file as **assignment5_STUDENT-ID_codes.rar** and your report as **assignment5_STUDENT-ID_ram.pdf**.