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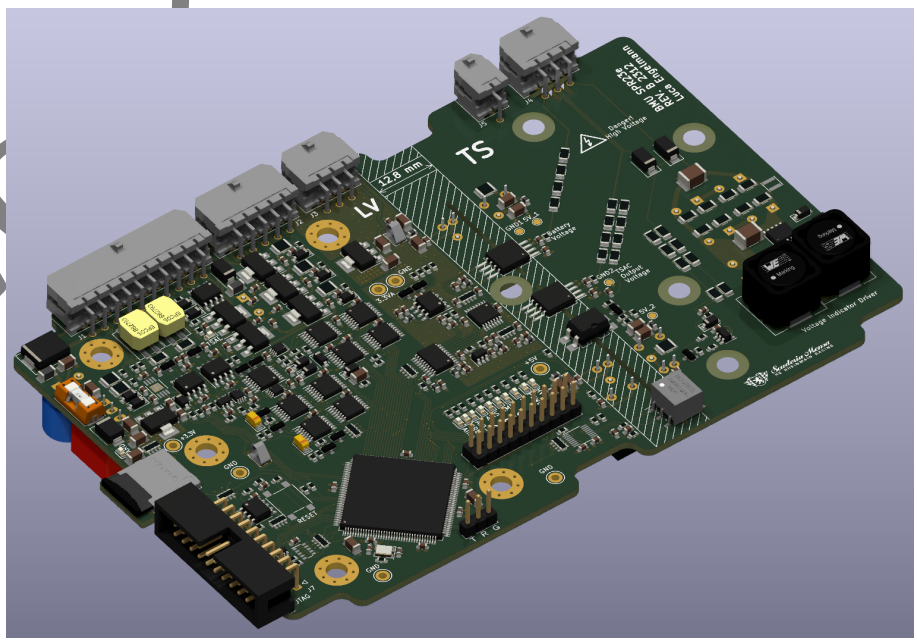
Design Report

Battery Management System for SPR23e



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Season: 2023/2024

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Glossary

AIR Accumulator Isolation Relay

AMS Accumulator Management System (See BMS)

BMS Battery Management System

BMU Battery Management Unit

BOM Bill Of Material

CAN Controller Area Network

CSV Comma-separated Values

EMI Electromagnetic Interference

ESD Electrostatic Discharge

FSG Formula Student Germany

HIL Hardware In the Loop

IMD Insulation Monitoring Device

LED Light Emitting Diode

LVS Low Voltage System

MCU Microcontroller Unit

PCB Printed Circuit Board

TS Tractive System

TSAC Tractive System Accumulator Container

TSAL Tractive System Active Light

UART Universal Asynchronous Receiver Transmitter

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1. Introduction

1.1. Accumulator

Kurz auf den Akku eingehen; Zellen, Konfiguration und Rendering.

1.1.1. System Overview

Blockdiagramm mit Stacks, BMS Slave, AIRs und Sicherung, AIR-PCB mit pre-charge und abgesicherte Messabgriffe, Stromsensor, BMU, IMD

1.2. Requirements

1.2.1. General Requirements

The requirements are mostly based on the FSG rule set for 2023 [1]. Some general requirements for the vehicle integration apply also. These include

- Power supply from the low-voltage system (LVS) in a range from 18 V to 25 V, which is the unregulated voltage from the low-voltage accumulator.
- One CAN bus with a bitrate of 1 Mbit/s for the communication with the Vehicle Control Unit.
- One IsoSPI [2] interface for the communication with the BMS slaves on the accumulator stacks.
- Isolated voltage measurement for the accumulator and TSAC output voltage with an accuracy better than 1 % of the full measuring range.
- Isolated current measurement with a resolution better than ± 140 A, which is two times the fuse rating to allow for any short current peaks, and an accuracy better than 1 % of the full measuring range.

1.2.2. Rule Requirements

Since the BMU contains many different parts required by the rules, all of the following rules have to be fulfilled. For the TSAL logic in the accumulator these rules apply:

- EV 4.10.3 [p. 85][1] *The TSAL itself must have a green light, continuously on, active if and only if the LVS is active and ALL of the following conditions are true:*
  - *All AIRs are opened.*
  - *The pre-charge relay, see EV 5.7.2, is opened.*
  - *The voltage at the vehicle side of the AIRs inside the TSAC does not exceed 60 V DC or 50 V AC RMS.*

- EV 4.10.4 [p. 85][1] *The mentioned voltage detection must be performed inside the respective TS enclosure.*
- EV 4.10.5 [p. 85][1] *The mentioned states of the relays (opened/closed) are the actual mechanical states. The mechanical state can differ from the intentional state, i.e. if a relay is stuck. Any circuitry detecting the mechanical state must meet EV 5.6.2.*
- EV 4.10.6 [p. 85][1] *The voltage detection circuit of the red light and the relay state and voltage detection circuit of the green light must be independent. Any plausibility check between both lights is not allowed. A TSAL state with both lights simultaneously active might occur and must not be prevented.*
- EV 4.10.9 [p. 85][1] *The TSAL and all needed circuitry must be hard-wired electronics. Software control is not permitted.*
- EV 4.10.10 [p. 85][1] *A green indicator light in the cockpit that is easily visible even in bright sunlight and clearly marked with "TS off" must light up if TSAL green light is on, see EV 4.10.3.*
- EV 4.10.11 [p. 86][1] *Signals influencing the TSAL and the indicator according to EV 4.10.10 are SCS, see T 11.9. The individual safe state of each of the TSAL lights is off. The TSAL has an active indication of the absence of failures (continuous green illumination) and thus the red light must not be illuminated for a visible check, see T 11.9.5.*
- EV 4.10.13 [p. 86][1] *The TSAL's green light relay state detection circuit, see EV 4.10.3, does not need to detect an open circuit, as required by T 11.9, when the intentional state of the used (auxiliary) contact is opened. A plausibility check against the intentional relay state must be implemented in a way that the TSAL's green light stays off after the open circuit is detectable.*
- EV 4.10.14 [p. 86][1] *The TSAL's green light voltage detection circuit, see EV 4.10.3, does not need to detect an open circuit, as required by T 11.9, when no voltage is present. A plausibility check against the intentional relay states must be implemented in a way that the TSAL's green light stays off after the open circuit of the accumulator voltage detection circuit is detectable.*
- EV 4.10.14 [p. 86][1] *The latching required by EV 4.10.13 and EV 4.10.14 must not be triggered during normal operation conditions and must only be reset by power cycling the LVS.*

1.2.3. Additional Requirements

Firlefanz, der von der Regeln nicht gefordert wird, aber trotzdem drin ist

1.3. SPR21evo BMU

Kurz auf 21er BMU eingehen, Bild der Platine und Beschreibung der Key Features.

1.4. Comparing Legacy and Contemporary Solutions

Was kann die alte BMU anders als die neue? Welche Features kamen hinzu? Welche sind entfernt worden? Was ist der Ausblick auf Software-Seite? Logging auf SD-Karte, EEPROM, 2 CAN-Busse

Auch auf AIR-PCB und Stromsensor eingehen

2. Potential Improvements

Mögliche Verbesserungen

3. BMU Hardware Design

3.1. Implementations

Umsetzung der Anforderungen in REV A und REV B beschreiben.

Für REV A wird nur auf den Schaltplan und einen Changelog im Anhang verwiesen. REV B wird im Detail beschrieben

The TSAL logic will be implemented in the following way:

- The actual states of the relays will be monitored using auxiliary contacts in the relays. They are mechanically linked to the main contacts as explained in the application note [3, p. 2]: "*The auxiliary contact actuating method will indicate the true position of the main contacts. The auxiliary contact actuation is directly coupled to the main contact moving bridge, and will not indicate "open" unless both contact gaps of the double-make, Form X contact are fully disconnected.*"
- The plausibility check to fulfill EV 4.10.5 is done against the intentional state indicated by the BMU. The following possible states can trigger the latch:
  - The intentional state is active, the actual state reports inactive: A line break in the state detection is to be assumed.
  - The intentional state is inactive, the actual state reports active: The relay is most probably stuck

  Due to its mechanical construction, the relay takes 25 ms to switch from the opened to the closed position and 10 ms for the reverse [4, p. 2]. In these time periods, the relay states are implausible and must not trigger the latch, as EV 4.10.14 indicates.
- In order to fulfill EV 4.10.13, a line break in the state detection is detected by a plausibility check against the TSAC output voltage in the following way. In case the TSAC output voltage detection circuit detects a voltage greater than 60 V although all relays are open, these possibilities can occur:
  - The discharge circuit is still active after the relay opened. This is not a fault condition, since the discharge circuit takes about 2 seconds to discharge the TS below 60 V.
  - If the fault persists for more than 3 seconds than the discharge should have finished and it is to be expected that the relays are stuck and the state detection circuitry is broken.

  Note that the permissible state during discharge must not lead to a detected fault. However, a delay of 3 seconds to detect the fault is permissible by the rule.
- Likewise, a line break in the voltage detection circuitry is detected using a plausibility check against the relay states. If the relays are closed and the voltage detection circuitry detects no voltage, a fault in the detection circuitry is to be assumed and must lead to the latched deactivation of the green light.
- Since the TSAL accumulator logic is located on the BMU PCB and all TS components needed to perform the checks are located inside the TSAC, EV 4.10.4 is fulfilled.

- The circuit will be build with logic gates without any software control. Therefore, EV 4.10.9 is fulfilled as well. The final circuit is discussed in full detail in section 3.3.3.

3.2. Hardware Block Diagram

Blockdiagramm der BMU Hardware

3.3. Schematic Explanation

The schematic is rather complex and would not fit on one page. It is divided into 11 logical modules, which are connected on the top-level schematic seen in Figure 3.1. Each module will be discussed in the following subsections. The full schematic is available in Appendix C.

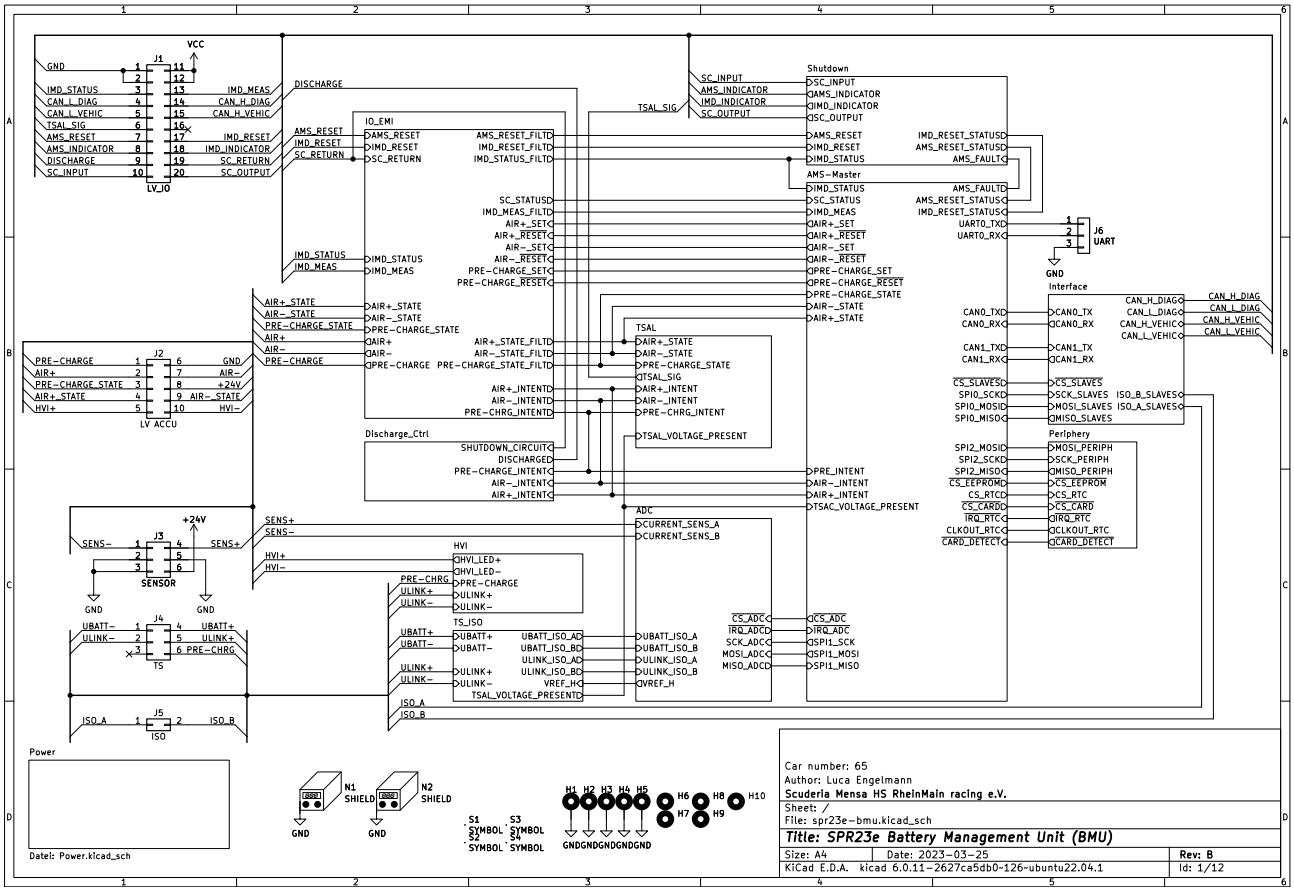

Figure 3.1.: Top-level BMU schematic.

3.3.1. Power Supply

The power supply schematic provides input protection and all necessary power rails for the BMU. The schematic for the power supply section is shown in Figure 3.2. At the input, L_1, C_{77}, and C_{78} form a low-pass filter to filter out any high-frequency noise which might be on the low-voltage system. D_{16} is used

in conjunction with F_1 to protect the BMU against over-voltages. D_15 not only protects the BMU from reverse-polarity, but it also isolates the BMU supply from the low-voltage system. A high-current spike will not drain C_{78}, leading to a stable power supply of the BMU in case of voltage dips caused by switching of the cooling fans or pumps. The 18 V to 25 V provided by the LVS is stepped-down to 5 V using an integrated DC to DC converter. Two low-dropout regulators U_{25} and U_{26} generate the main 3.3 V digital voltage rail used by the microcontroller and the other digital circuits and a secondary 3.3 V voltage rail used by the analog circuits. The use of two independent regulators for analog and digital circuits prevents noise coupling from the digital to the analog circuit. A power LED signalizes that the BMU is powered. Test points for all voltage rails are provided for easy measurement on the PCB.

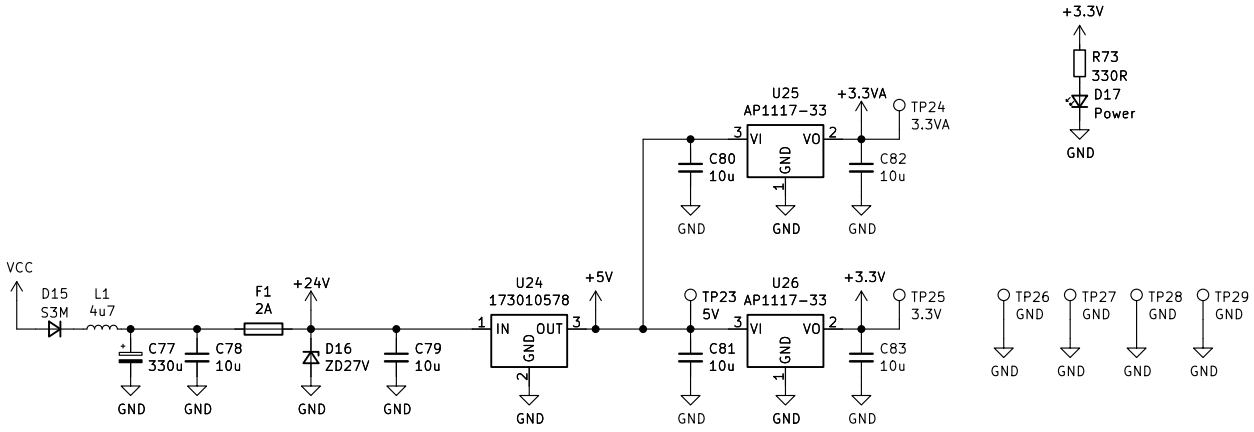

Figure 3.2.: Schematic of the power supply section.

3.3.2. I/O

This section of the schematic conditions the input signals for the BMU logic and drives the AIRs. It can be seen in Figure 3.3. Since the digital section operates at 3.3 V and the signals outside the BMU operate at LVS levels, zener diodes are used to limit the voltages. Each signal has a pull-down resistor to ensure stable logic levels in case of unconnected inputs. The 2.2 kΩ resistors at the inputs for the state detection of each relay ensure the minimum wetting current needed for the LEV100 relays: *"Minimum Aux Contact Load 10mA/12Vdc"* [4, p. 3]. Likewise, the pull-down resistors R_{77} and R_{78} for the IMD are the recommended values from the datasheet [5, p. 5]. Note that these resistors have to dissipate some power at the maximum voltage of the LVS: $P_{d,pull-down} = \frac{(25\ \text{V})^2}{2.2\ \text{k}\Omega} = 0.28$ W. Therefore, resistors in a 1210 package are used, since they are rated for 0.5 W of power [6]. The capacitors form in combination with the zener diode dropper resistors a low-pass filter used to filter out any noise which might be picked up by the signal wires. The status of the shutdown circuit is also evaluated by the BMU. The same input protection circuit is used to measure the voltage of it. The relays are directly supplied from the shutdown circuit. L_2 and C_{96} form low-pass filter, which limits the current spike caused by the switching of the relays. D_{18} is important to separate the high-current path from the detection path. Imagine that the AIRs are not energized and the shutdown circuit is active. Now, one emergency button is pressed. The shutdown circuit is turned off but C_{96} is still charged. Without D_{18}, it would lead to a false reading of the SC_STATUS signal until the capacitor is discharged. With D_{18}, C_{96} is blocked from holding up the voltage at the SC_RETURN node in this scenario. This ensures, that the microcontroller and the latches U_{28A}, U_{28B}, and U_{29A} detect a power-loss in the shutdown circuit without any noticeably delay.

The AIRs are controlled by ITS4200 high-side switches [7] which are supplied by the shutdown circuit. This is required by EV 6.1.1 [1]. U_{30} is used as level shifters to drive the high-side switches. This step is needed,

since the ITS4200 is advertised with a "*CMOS compatible input*" [7, p. 2] and has an input voltage turn-on threshold of 3.0 V [7, Table 4]. Its input is driven with 5 volt instead of 3.3 V to avoid potential problems. The inputs of the 74HCT logic series recognize a logical high signal at and above 2.0 V. The ITS4200 is internally protected against short-circuits and voltage backfeed, making it an ideal output driver for the BMU. The relays are not directly controlled by the BMU. Instead, flip-flops isolate the control from the microcontroller to the outputs. The MCU can set and clear the flip-flops. Additionally, the flip-flops can be cleared by the shutdown circuit signal. This has the advantage that the relays are not only de-energized by the loss of power but also the turn-on request is cleared in hardware. In the BMU for the SPR21e, this was solely done in software. Now imagine that the flip-flops were omitted and the microcontroller crashes as soon as the AIRs are energized. If the emergency switch is pushed, the AIRs will de-energize. However, since the crashed microntroller still requests the positive and negative AIR to be energized, re-activation of the emergency switch results in an uncontrolled re-activation of the tractive system without pre-charging. Due to the large current spike, both the positive and negative AIR will be most likely stuck after this event. This has happened in the early testing phase of the SPR21e. With the hardware flip-flops, it doesn't matter if the microcontroller crashes while the AIRs are energized. The flip-flops will only react on the rising-edge of the SET-signals and will be cleared, as soon as the shutdown circuit opens. The intentional states of the relays are taken from the outputs of the flip-flops. Notice that the flip-flops are reset-dominant, meaning that they cannot be set if the clear input is set to a logical zero.

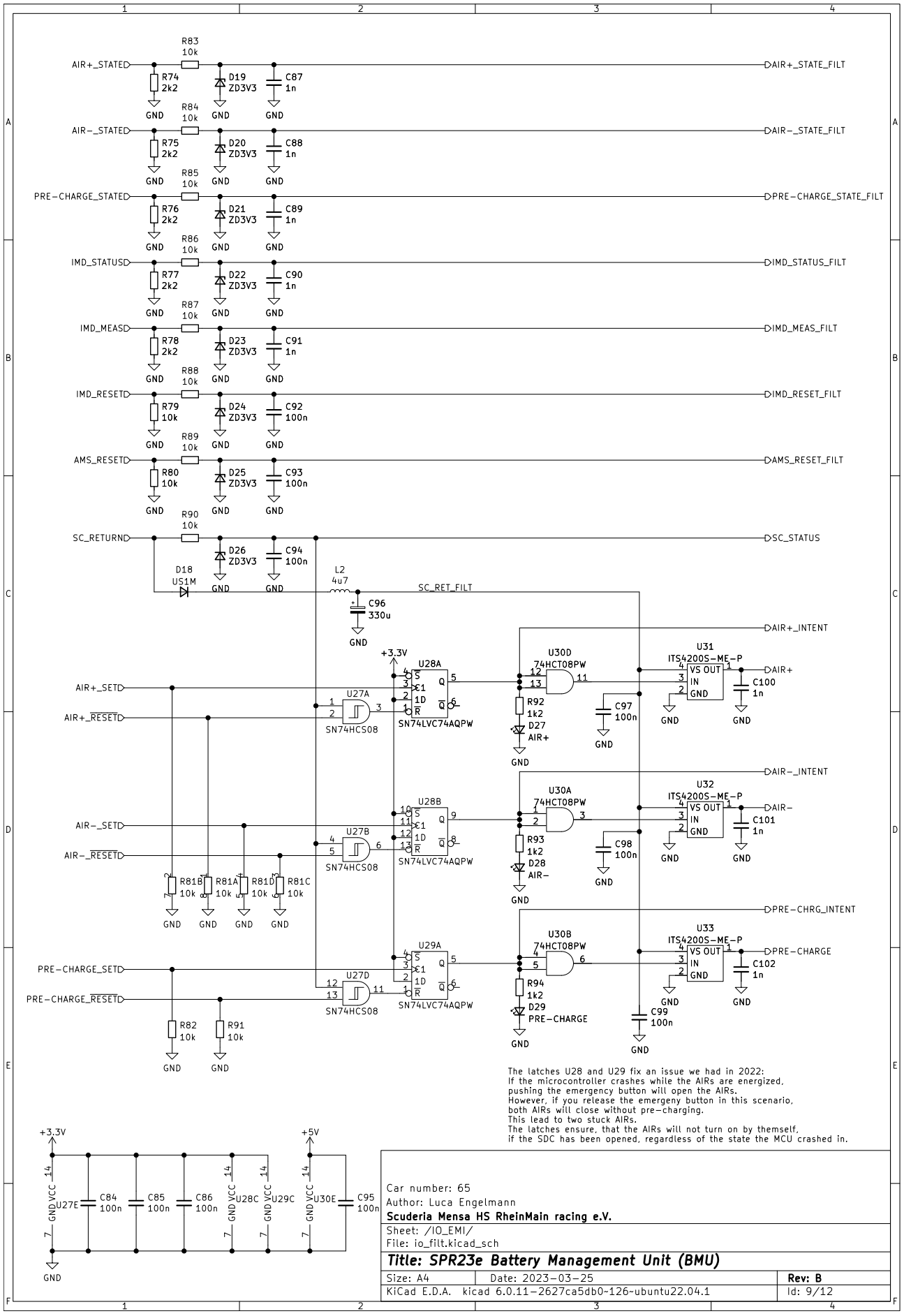

Figure 3.3.: Schematic of the I/O section.

3.3.3. TSAL

The TSAL schematic can be divided into three logical sections. The top section checks the three AIRs for plausible states. The second section checks the TS detection circuit for plausibility. The third section controls the green light and contains the required latch. Figure 3.4 shows the schematic of the TSAL logic.

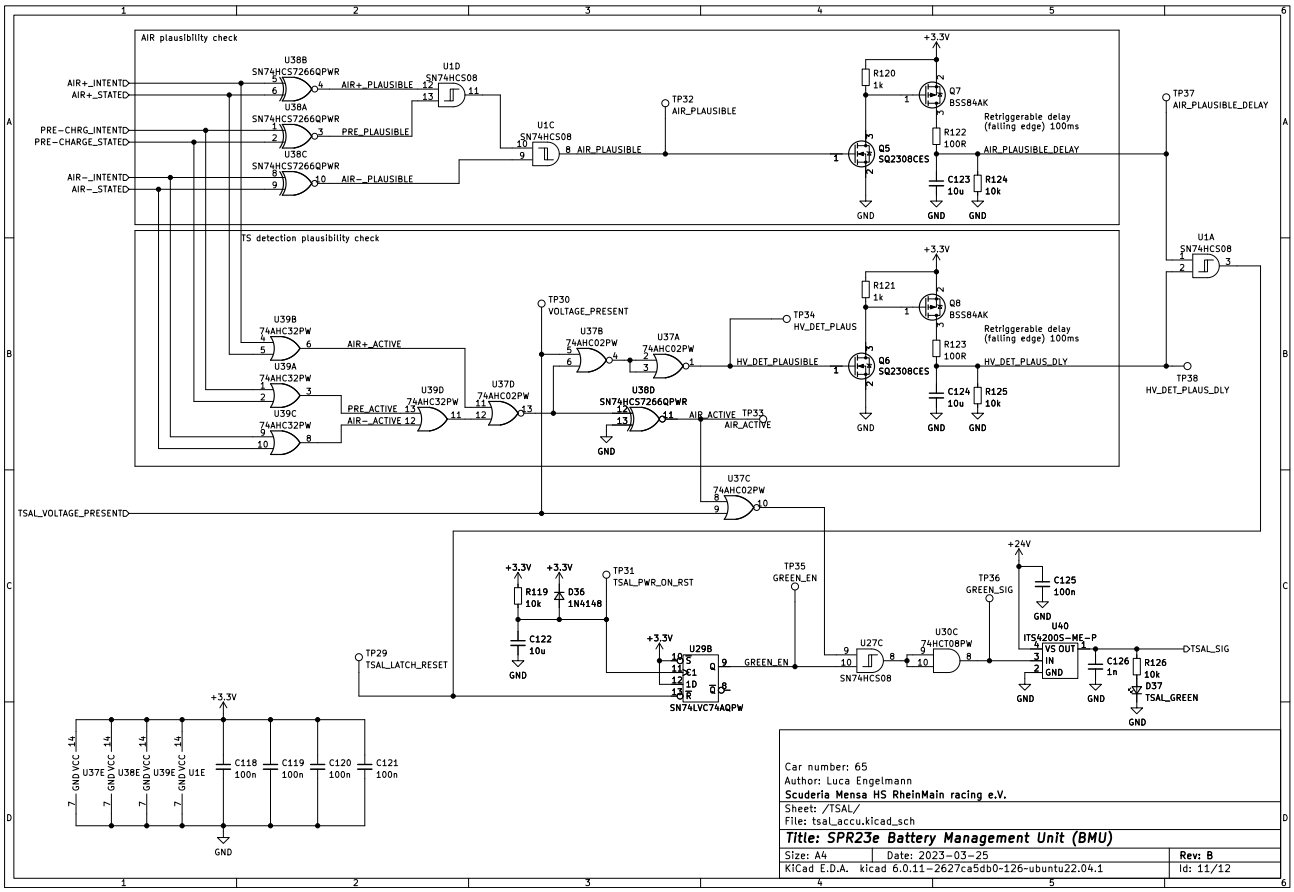

Figure 3.4.: Schematic of the TSAL accumulator logic.

The logic evaluates if the current state is plausible. A plausible state is always reached when the TSAC output voltage matches the relay state and if the actual relay state matches the intentional state. The truth table for the AIR plausibility check for each AIR is shown in Table 3.1. The resulting boolean function corresponds to an exclusive NOR gate (U_{38} in Figure 3.4).

Table 3.1.: Truth table for the plausibility check for each AIR.

AIR intentional	AIR actual	plausible	Comment
inactive	inactive	yes	No error
inactive	active	no	AIR stuck
active	inactive	no	State detection or coil wire broken
active	active	yes	No error

The AND gate U_1 (Figure 3.4) combines the plausibility of all AIRs to one signal AIR_PLAUSIBLE, which is low as soon as one of the AIRs is implausible and high if all AIRs are plausible. A retriggerable delay circuit accommodates for the mechanical switching time of the AIRs. It delays the falling edge only and passes the rising edge through without any delay. The delay time is set by the time constant of C_{123} and

R_{124} (Figure 3.4) and the input threshold of the following AND gate (U_1, Figure 3.4). The following gate needs to have Schmitt trigger inputs due to the slow falling edge caused by the delay. The input thresholds have a large tolerance and are not specified for a supply voltage of 3.3 V [8, Section 6.5]. The interpolated values for the negative threshold are $0.61\ \text{V} < U_{T-} < 1.22\ \text{V}$. At the maximum lower input threshold, the delay time is minimal and corresponds to the RC time constant τ. The circuit ensures a minimum delay time of 100 ms. At the minimum lower input voltage threshold, the delay time will increase to 170 ms.

The plausibility check for the TSAC output voltage detection uses both the intentional and the actual AIR states for comparison. U_{37} and U_{39} combine the six signals to one signal. If any of the AIRs is active (either intentional or unintentional) the signal AIR_ACTIVE will be high. The complex appearing connection of U_{37} and U_{38D} results in an efficient utilization of the four independent gates within a package. U_{38D} is configured to behave like an inverter. The signal HV_DET_PLAUSIBLE is a combination of the TSAC output voltage detection and the AIR state with the truth table shown below. The corresponding boolean function is an OR gate with one inverted input.

Table 3.2.: Truth table for the TSAC output voltage plausibility check.

Voltage present	**AIR active**	**plausible**	**Comment**
no	no	yes	No error
no	yes	no	Voltage detection broken wire
yes	no	**yes**	See text
yes	yes	yes	No error

A voltage greater than 60 V present at the TSAC output while no AIR is active is not considered as implausible since this happens on every discharge cycle. In this case, the green and the red LED of the TSAL will be active. This edge case is allowed by rule EV 4.10.6 and is thus not prevented. The HV_DET_PLAUSIBLE signal uses an identical retriggerable delay circuit. In this case, it is used to accommodate for the sum of the pre-charge time and the relay turn-on time. During pre-charge, the TSAC output voltage will rise depending on the time constant of the pre-charge resistor and the DC-Link capacitor. In order to detect a broken wire in the voltage detection circuitry, the plausibility check waits for the DC-Link voltage to rise above 60 V. This ensures that the broken wire is detected if the implausibility persists after the pre-charge time and pre-charging will not lead to a false triggering. The time it takes for the DC-Link voltage to rise above 60 V can be calculated with the basic capacitor charging formula shown in Equation 3.1.

$$U_c(t) = U_0 \cdot (1 - e^{-\frac{t}{\tau}}) \tag{3.1}$$

Re-arranging Equation 3.1 to solve for t is shown in Equation 3.2. The maximum t will be at the minimum battery voltage of 430 V. Solving for $U_c(t) = 60$ V, $U_0 = 430$ V, $\tau = RC = 1000\ \Omega \cdot 300$ µF, Equation 3.2 yields:

$$t_{pre} = -\tau \cdot \ln\left(1 - \frac{U_c(t)}{U_0}\right) = -(1\ \text{k}\Omega \cdot 300\ \mu\text{F}) \ln\left(1 - \frac{60}{430}\right) = 45\ \text{ms} \tag{3.2}$$

The turn-on time of the relays add to the pre-charge time. The resulting total pre-charge time $t_{pre,sum}$ equals:

$$t_{pre,sum} = t_{on,relay} + t_{pre} = 25\ \text{ms} + 45\ \text{ms} = 70\ \text{ms} \tag{3.3}$$

Therefore, a delay of 100 ms is sufficient as well.

The last section of the TSAL logic combines the plausibility check, the voltage detection signal, and the AIR_ACTIVE signal to control the green light of the TSAL. The flip-flop U_{29B} is the latch required by EV 4.10.13 and EV 4.10.14. It is set on startup after a short delay, to ensure that all signals which clear the latch are stable. If the AIRs or the voltage detection are implausible, the latch is cleared. The output of the latch is used as enable signal for the green light. Therefore, the green light can only be activated, if the whole system is in a plausible state. The green light is then controlled by the AIR_ACTIVE and TSAL_VOLTAGE_PRESENT signal in a way that either of these signals turn off the green light. This ensures that the green light is deactivated as soon as at least one AIR is active and reactivated only if the voltage at the TSAC output is less than 60 V and all AIRs are off. The signal output uses the same method as described in subsection 3.3.2. The signal produced by U_{40} is sent to the TSAL logic in the inverter, where it is routed to the TSAL lights.

4. Battery Disconnect Unit

Hier auf AIR-PCB und Stromsensor eingehen und die Platzierung der Komponenten in der BDU; Rendering

4.1. AIR PCB

Schaltplan und Beschreibung der Funktion, Rendering

4.2. Current Sensor

Schaltplan, Beschreibung der Komponenten, Berechnung der Genauigkeit und Rendering

5. Software Architecture

Softwarearchitektur erläutern

5.1. <Software Modul>

Softwaremodule erläutern

6. Test and Validation

6.1. Test Setup

Testaufbau erklären

6.2. TSAL Test

The TSAL accumulator logic has been simulated with LTSpice before putting it onto the PCB. The simulation tests all possible error conditions, including stuck relays, broken relay state detections and a line break in the voltage detection. The simulation results have been checked against the real behavior using a Hardware-in-the-loop (HIL) test procedure. A S32K144-Q100 evaluation board [9] is connected via CAN to the BMU and controls the relays in the test setup based on the commands sent by the BMU. It also feeds back the current state of the TSAL signal. The BMU runs a modified firmware which contains the test procedures. These tests can be initiated via the UART interface. During the test, the BMU will output all necessary values in CSV format over the UART interface in 50 ms time intervals. The BMU firmware uses the measured DC-Link and battery voltages to perform the pre-charge. The simulation performs the pre-charge using a constant timing for the relays. Stuck relays may lead to different pre-charge times than usual. The simulation will not account for that fact. However, it does not influence the behavior of the TSAL logic. Furthermore, the slow appearing rise and fall times in the test results are an artifact from the 50 ms time slices. They do not represent the real rise and fall times. Another artifact from the same source are shifted edges by ± 50 ms. The following pages show the simulation result on the left side and the real behavior on the right side in the following order:

1. No error
2. Positive AIR stuck
3. Pre-charge relay stuck
4. Negative AIR stuck
5. Voltage detection broken wire
6. Positive AIR state detection broken wire
7. Pre-charge relay state detection broken wire
8. Negative AIR state detection broken wire

The graphs in each plot represent the logic signals at the most important points in the circuit. The upper most plot shows the output of the TSAL logic, which controls the green light. The second graph shows the voltage detection with a logical high at 3.3 V representing a detected voltage > 60 V. The relay intent and state plots are self explanatory. They represent the intentional and actual state of the relay with a logical high representing an active state. The last plot shows the DC-Link voltage measured by the BMU. The simulation uses the accumulator voltage of 600 V while the HIL test uses 24 V. The plots of the HIL tests use 0 and 1 to denote the logical states.

Test 1: No error

In this test, the BMU performs a pre-charge and a discharge cycle. The TSAL green light shall turn off, as soon as at least one AIR is closed or the voltage across the DC-Capacitor is greater than 2.5 V and shall turn back on, if all AIRs are open and the DC-Link voltage is less than 2.5 V. The 24 V$/2.5$ V ratio between the battery voltage in the test setup and the TS detection threshold is approximately the same as in the real setup with a ratio of 600 V$/60$ V. As seen in Figure 6.2, the TSAL logic behaves exactly as simulated. The test would not be passed, if the LED would not turn off at the 1 s mark or would remain off at the 4.4 s mark.

Test 2: Positive AIR stuck

This test simulates a stuck positive AIR. The AIR+ state is therefore always high. During pre-charging, the negative AIR closes. Therefore, the pre-charge resistor is bridged in this scenario. Notice that the simulation uses a simple time-controlled pre-charging while the real BMU performs the pre-charging based on the DC-Link and battery voltage. This explains the short on-time of the pre-charge relay compared to the simulation due to the fast rise time of the DC-Link voltage. Notice also, that the BMU with the final firmware would not allow to close any relay if one of the relay is stuck. Both the simulation in Figure 6.3 and the HIL test in Figure 6.4 show, that the TSAL green light never turns on, as required.

Test 3: Pre-charge relay stuck

A stuck pre-charge relay does not directly lead to malfunction of the pre-charge sequence or the general function of the tractive system. However, it would violate EV 5.6.2 [1, p. 90]. A stuck pre-charge relay is detected correctly as Figure 6.5 and Figure 6.6 show. The TSAL's green light does not turn on at all.

Test 4: Negative AIR stuck

Similarly to test 3, a stuck negative AIR causes no direct malfunction of the system but it will also violate EV 5.6.2 [1, p. 90]. This fault is correctly detected as well, as seen in Figure 6.7 and Figure 6.8.

Test 5: Voltage detection broken wire

A broken wire or blown fuse in the voltage detection circuit is simulated in this test. Since the voltage detection circuit and the TSAC output voltage measurement share the same wire and fuse, the DC-Link voltage and the voltage detection in both the simulation and the real hardware read always zero. Additionally, since the simulation does not use the DC-Link voltage to perform the pre-charge, the relay sequence looks identical to any other test (Figure 6.9). The BMU will remain in the pre-charge state since the DC-Link voltage does not reach 95 % of the battery voltage, causing the positive AIR to never energize (Figure 6.10). It is apparent that as soon as the negative AIR and the pre-charge relay turn on, the green light turns off and remains off, after both relays de-energize again.

Tests 6, 7, and 8: Relay state detection broken

Due to their similarities, the last three tests are summarized here. As seen in Figure 6.12, Figure 6.14, and Figure 6.16, the state detection of the positive AIR, pre-charge relay, and negative AIR read constantly zero. This fault is detectable, as soon as the corresponding relay is energized. The green light turns of, as soon as the AIRs are energized and remains off after the relays de-energize due to the fault latching.

TSAL Test: Summary

In summary, the tests show that the TSAL accumulator logic recognizes all possible faults correctly and behaves rule compliant. While these tests seem extremely elaborate and time-consuming, it is important to fully validate the functionality of the TSAL logic, since it is a safety-critical part that must behave under all circumstances as expected.

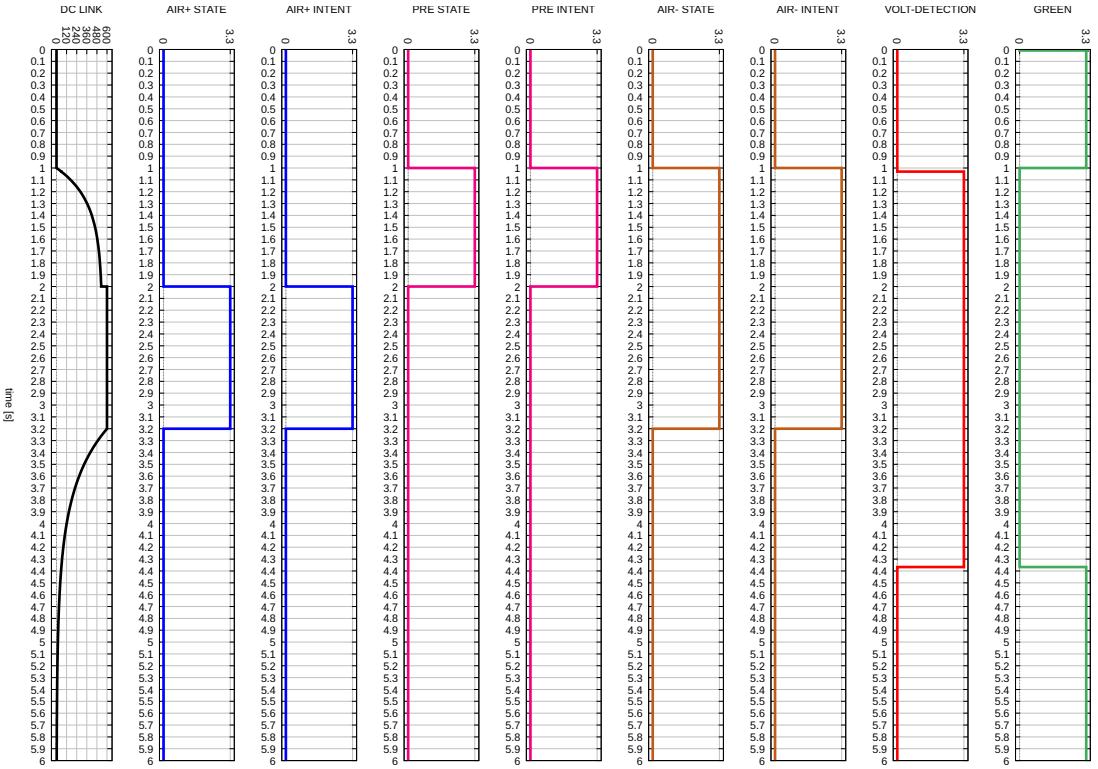

Figure 6.1.: TSAL simulation result. Test: No errors.

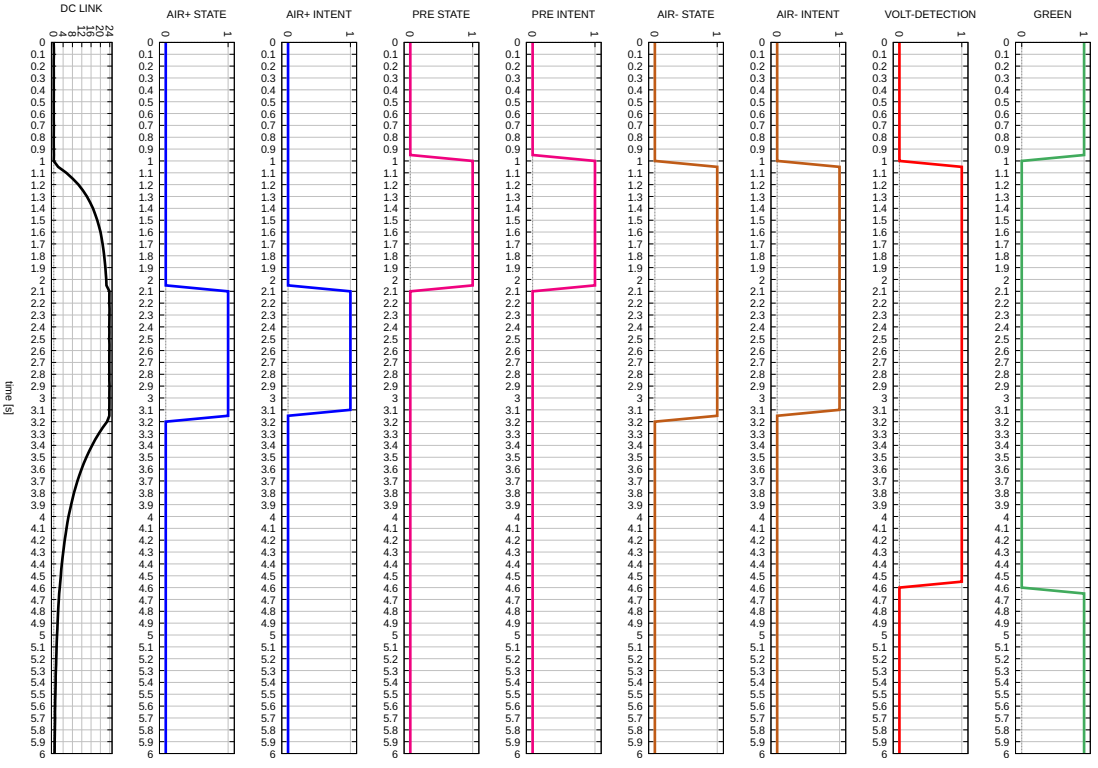

Figure 6.2.: TSAL HIL result. Test: No errors.

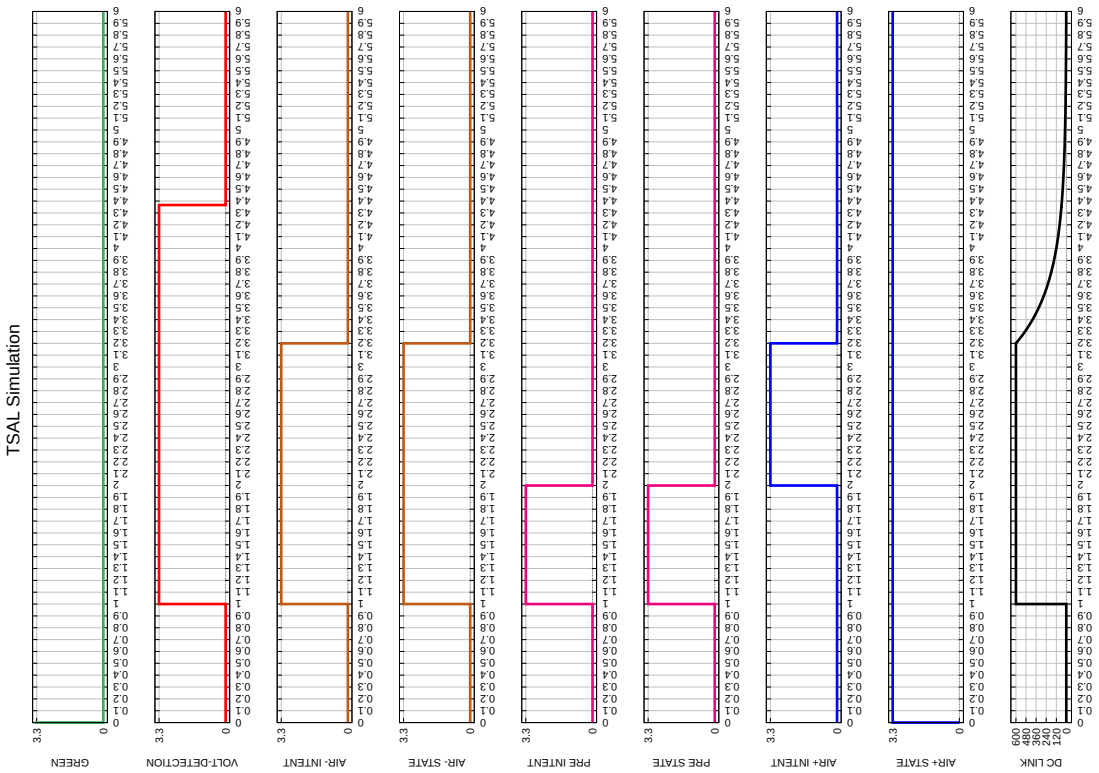

Figure 6.3.: TSAL simulation result. Test: Positive AIR stuck.

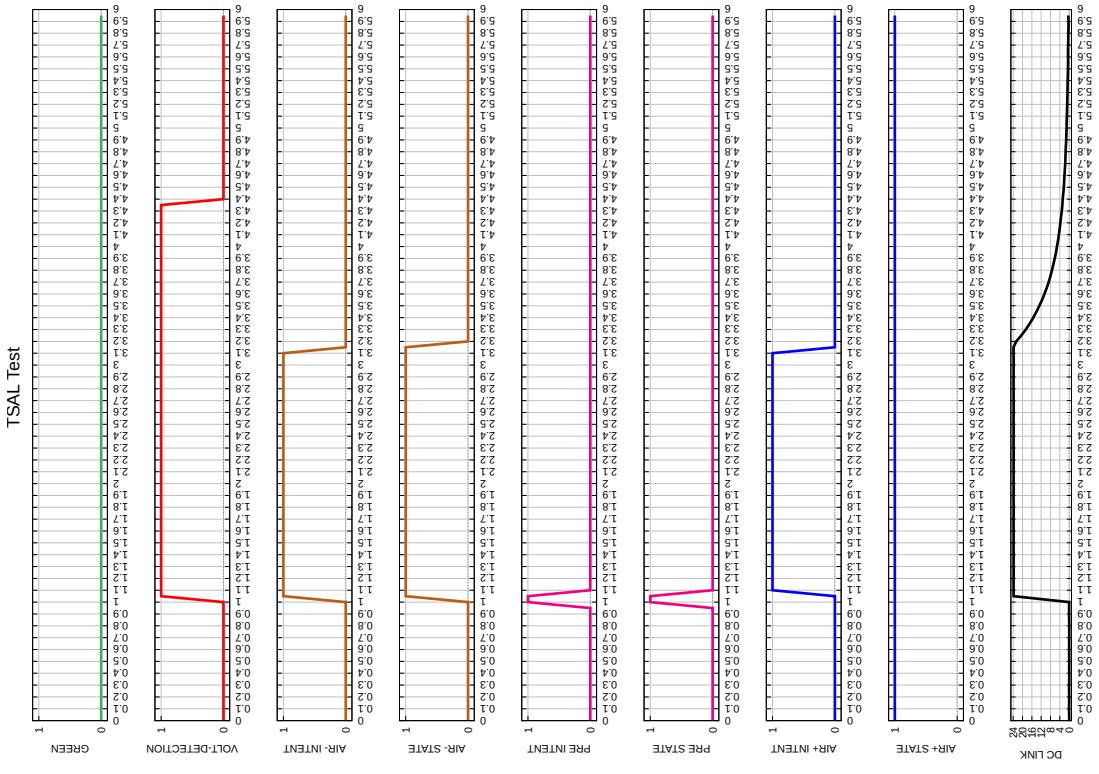

Figure 6.4.: TSAL HIL result. Test: Positive AIR stuck.

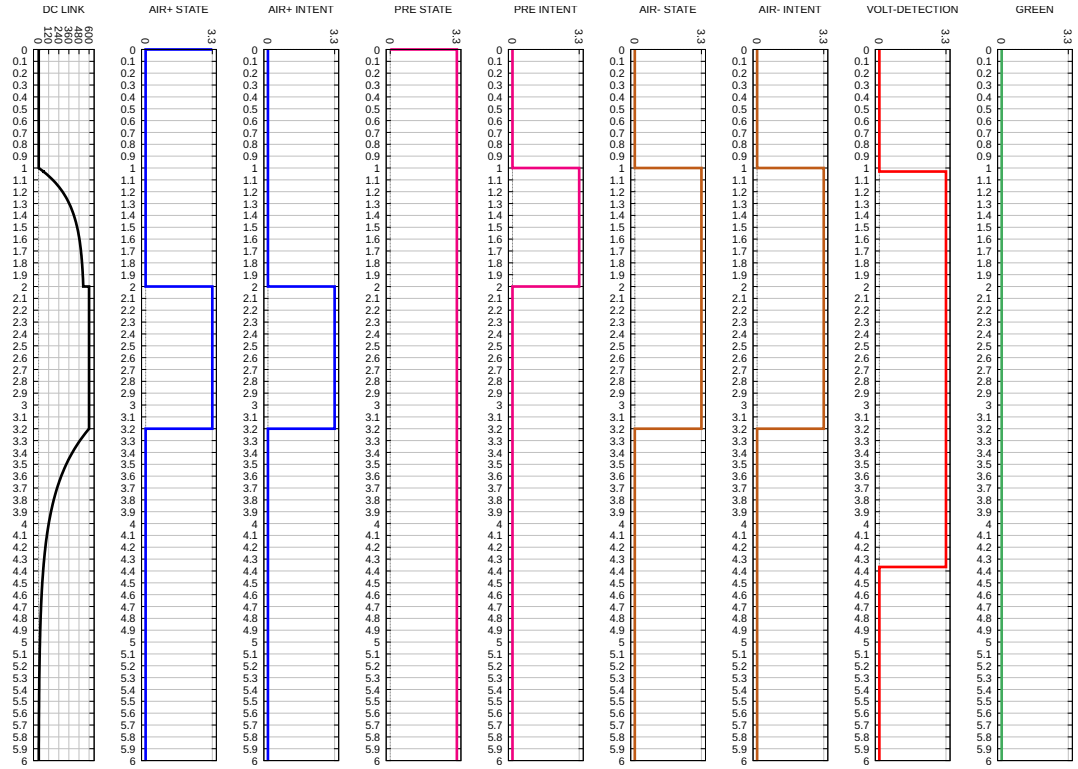

Figure 6.5.: TSAL simulation result. Test: Pre-charge relay stuck.

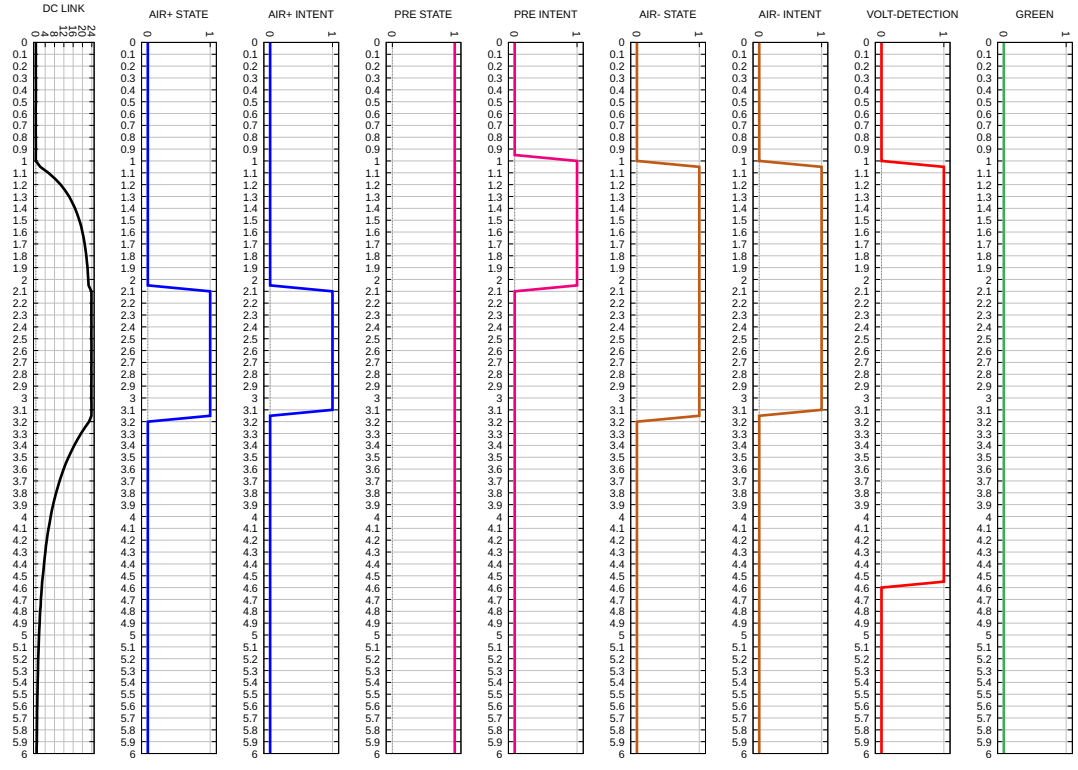

Figure 6.6.: TSAL HIL result. Test: Pre-charge relay stuck.

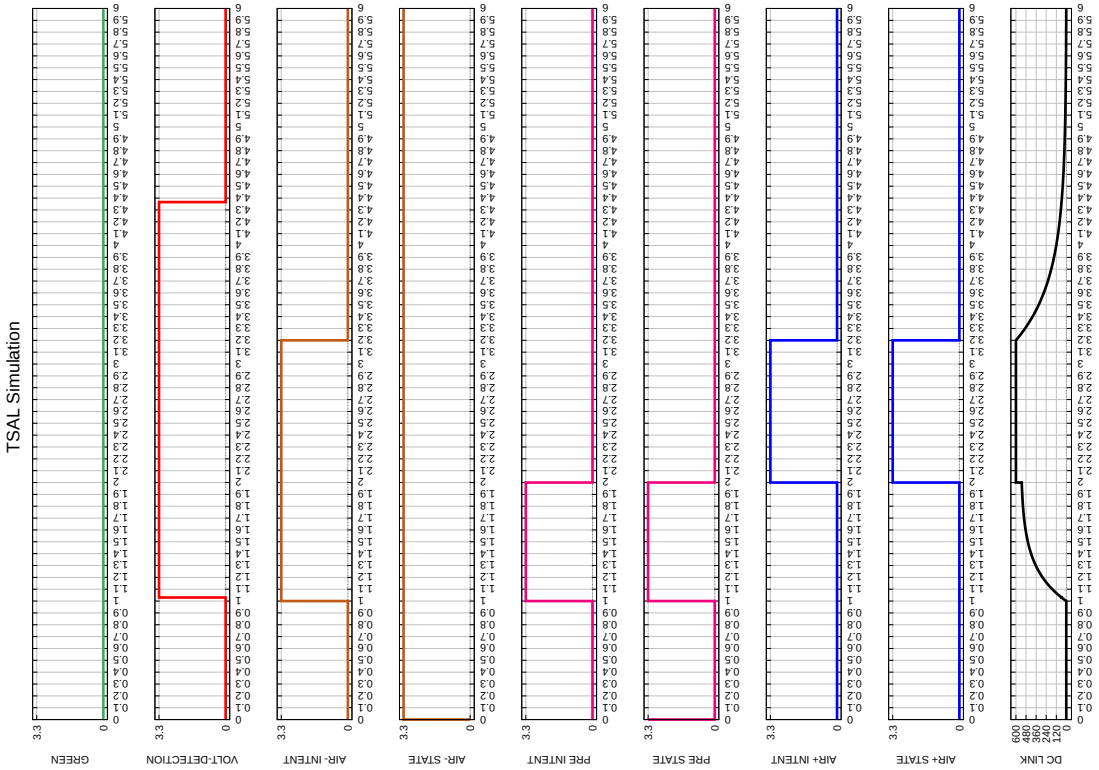

Figure 6.7.: TSAL simulation result. Test: Negative AIR stuck.

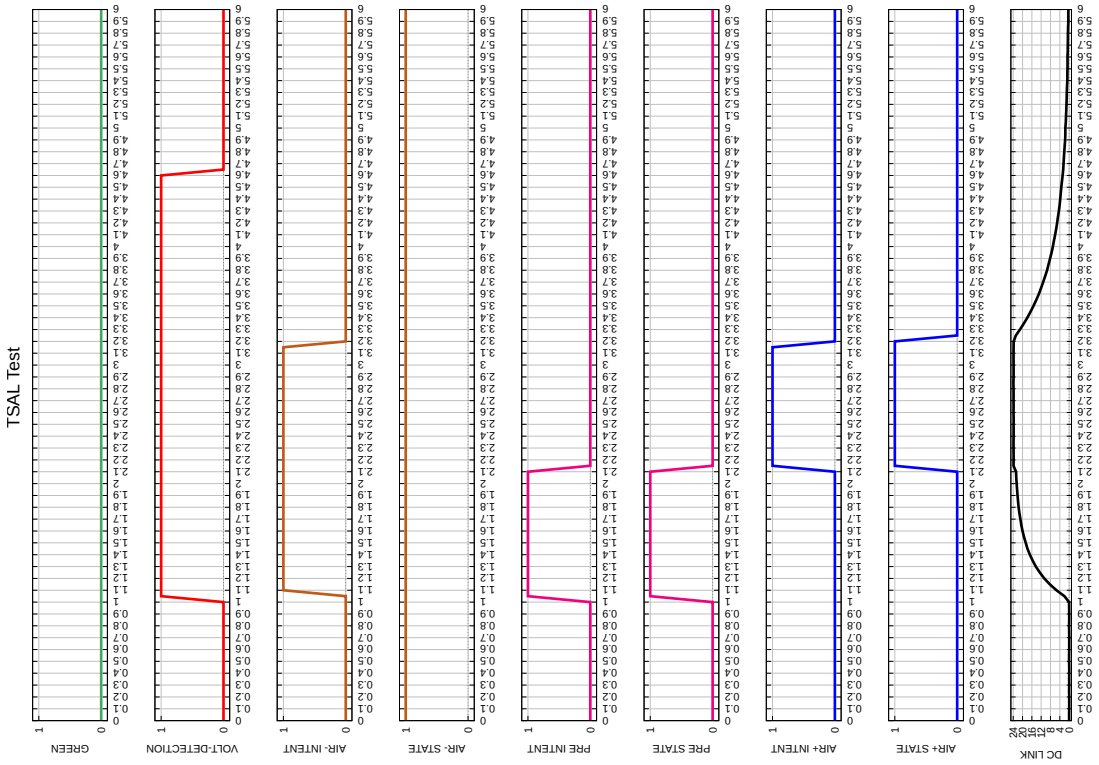

Figure 6.8.: TSAL HIL result. Test: Negative AIR stuck.

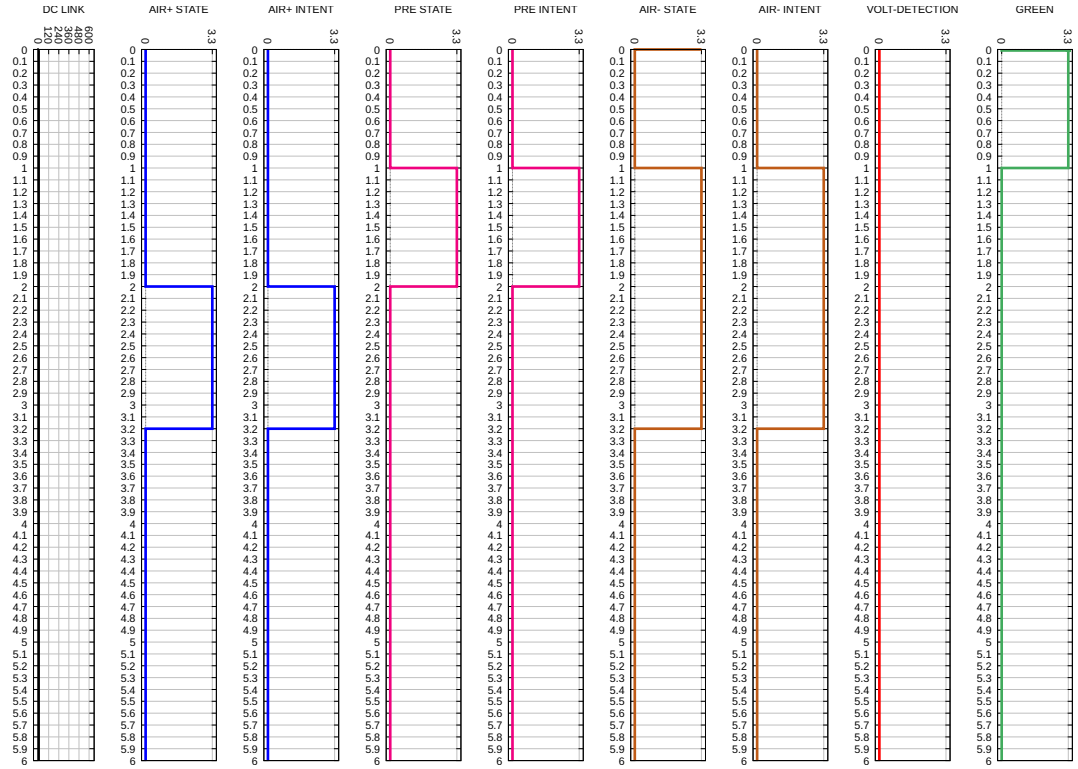

Figure 6.9.: TSAL simulation result. Test: Voltage detection broken wire.

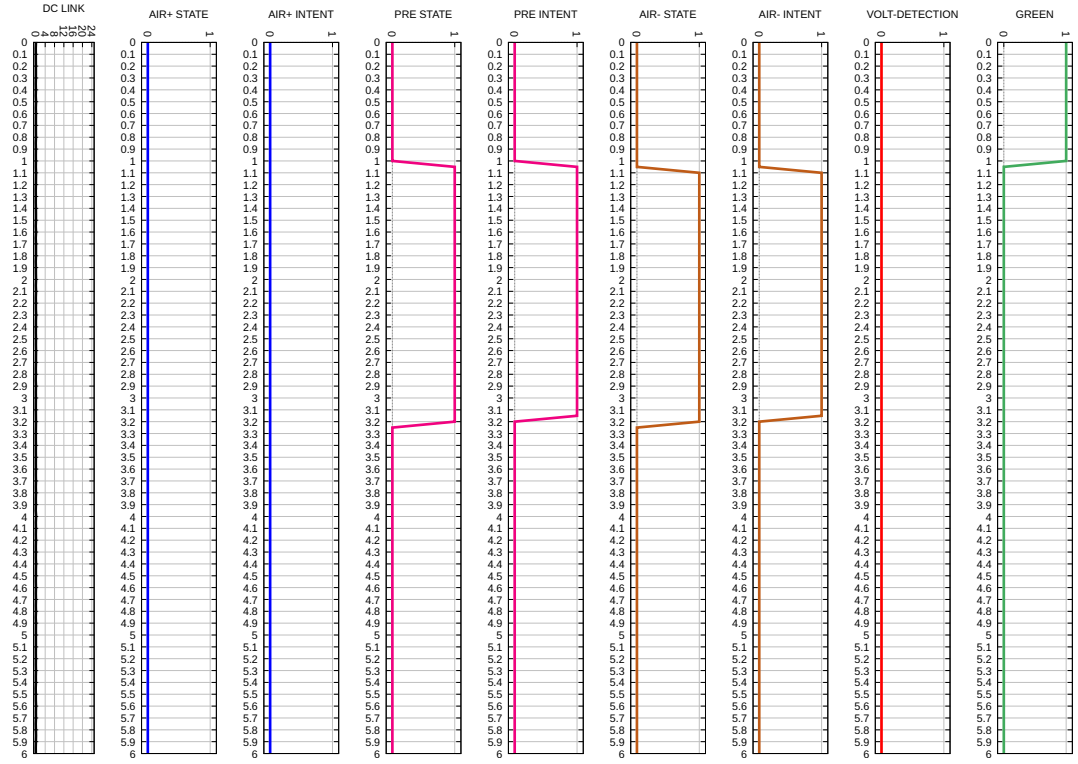

Figure 6.10.: TSAL HIL result. Test: Voltage detection broken wire.

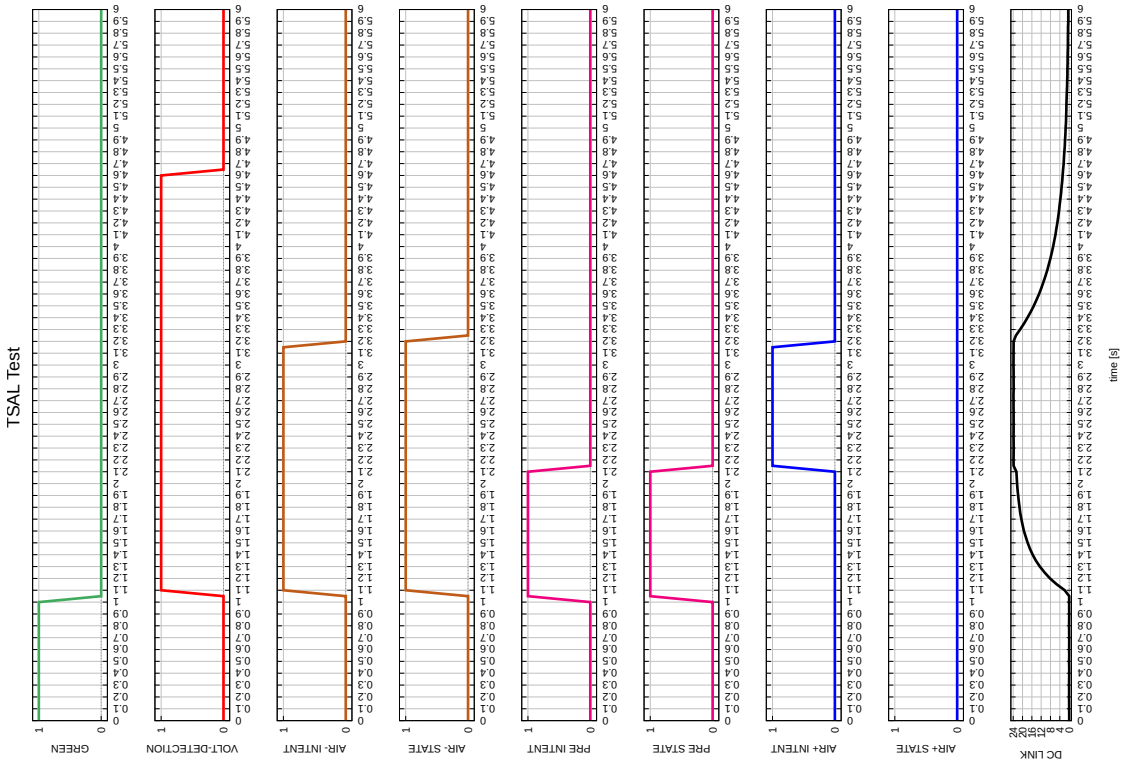

Figure 6.12.: TSAL HIL result. Test: Positive AIR state detection broken wire.

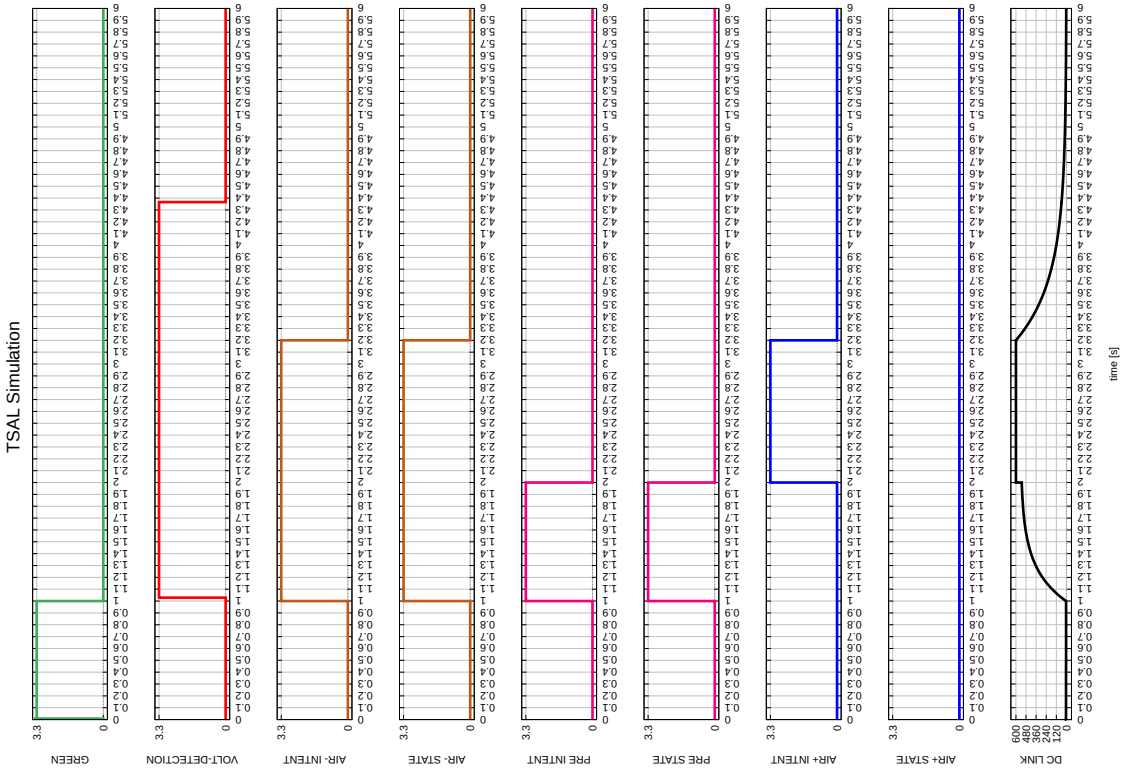

Figure 6.11.: TSAL simulation result. Test: Positive AIR state detection broken wire.

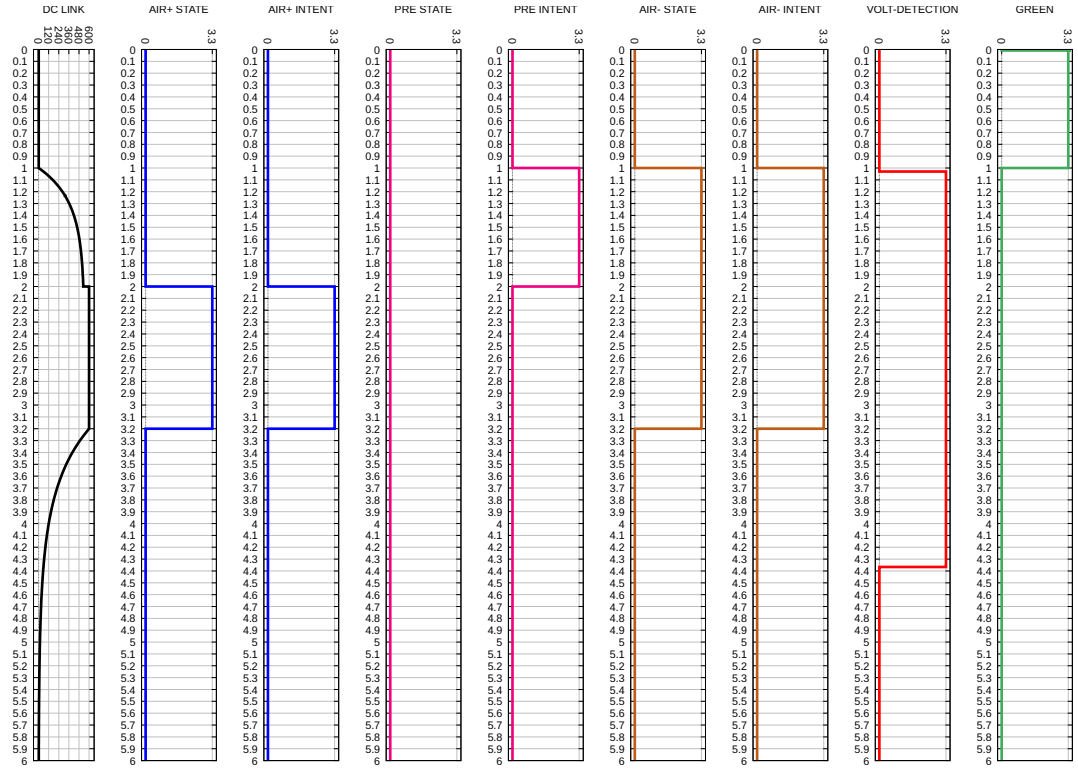

Figure 6.13.: TSAL simulation result. Test: Pre-charge relay state detection broken wire.

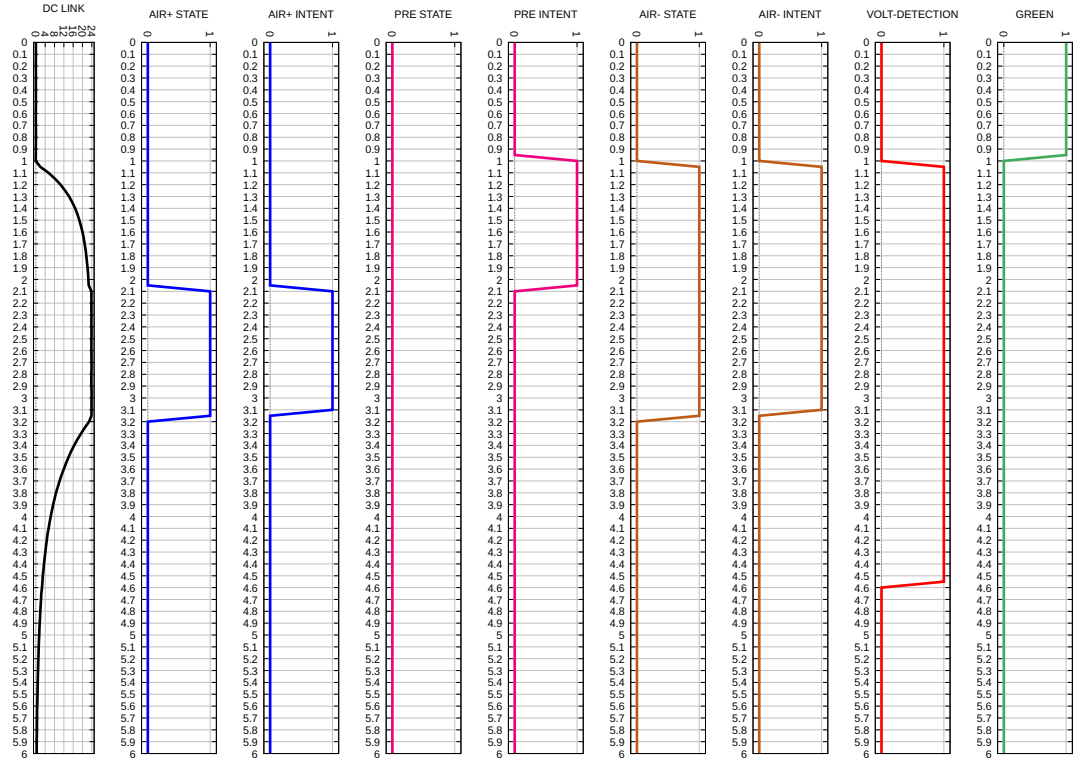

Figure 6.14.: TSAL HIL result. Test: Pre-charge relay state detection broken wire.

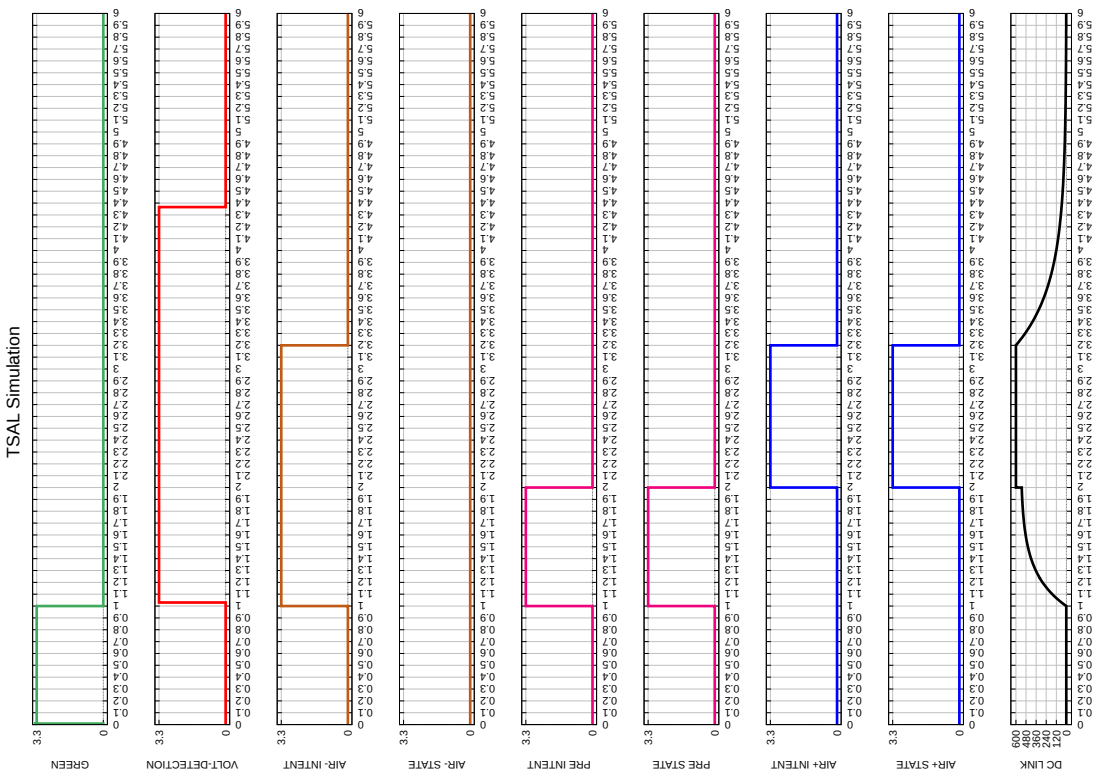

Figure 6.15.: TSAL simulation result. Test: Negative AIR state detection broken wire.

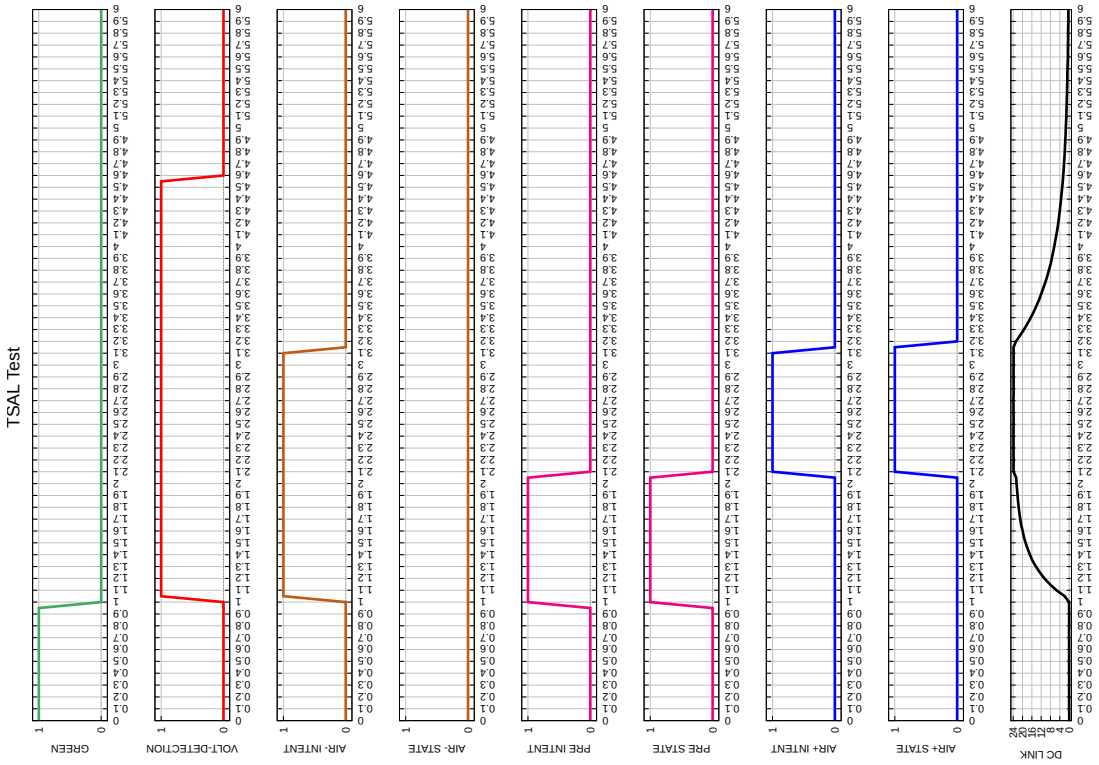

Figure 6.16.: TSAL HIL result. Test: Negative AIR state detection broken wire.

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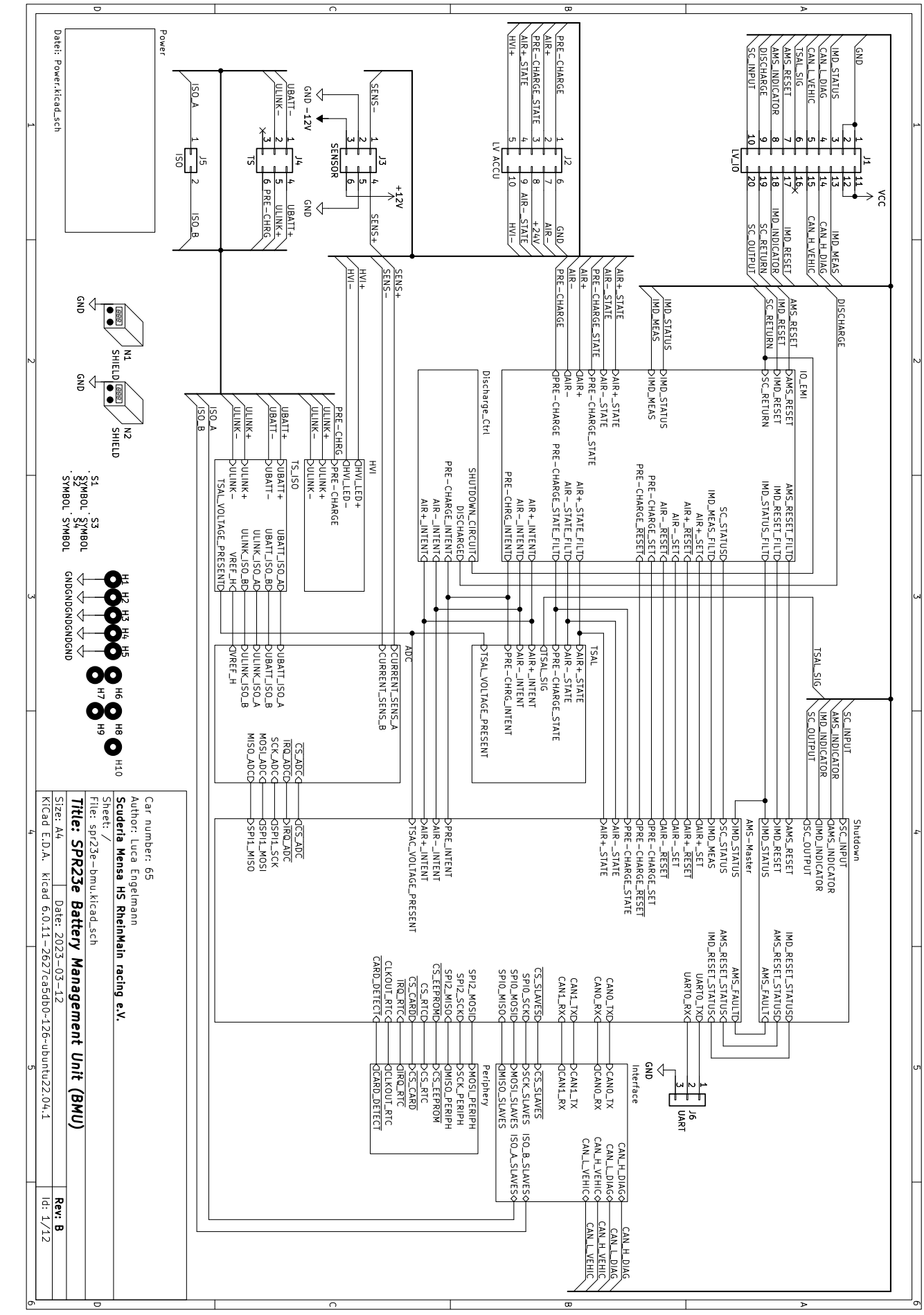
A. Schematics Revision A (Only for reference!)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Rev: B
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Id: 1/12
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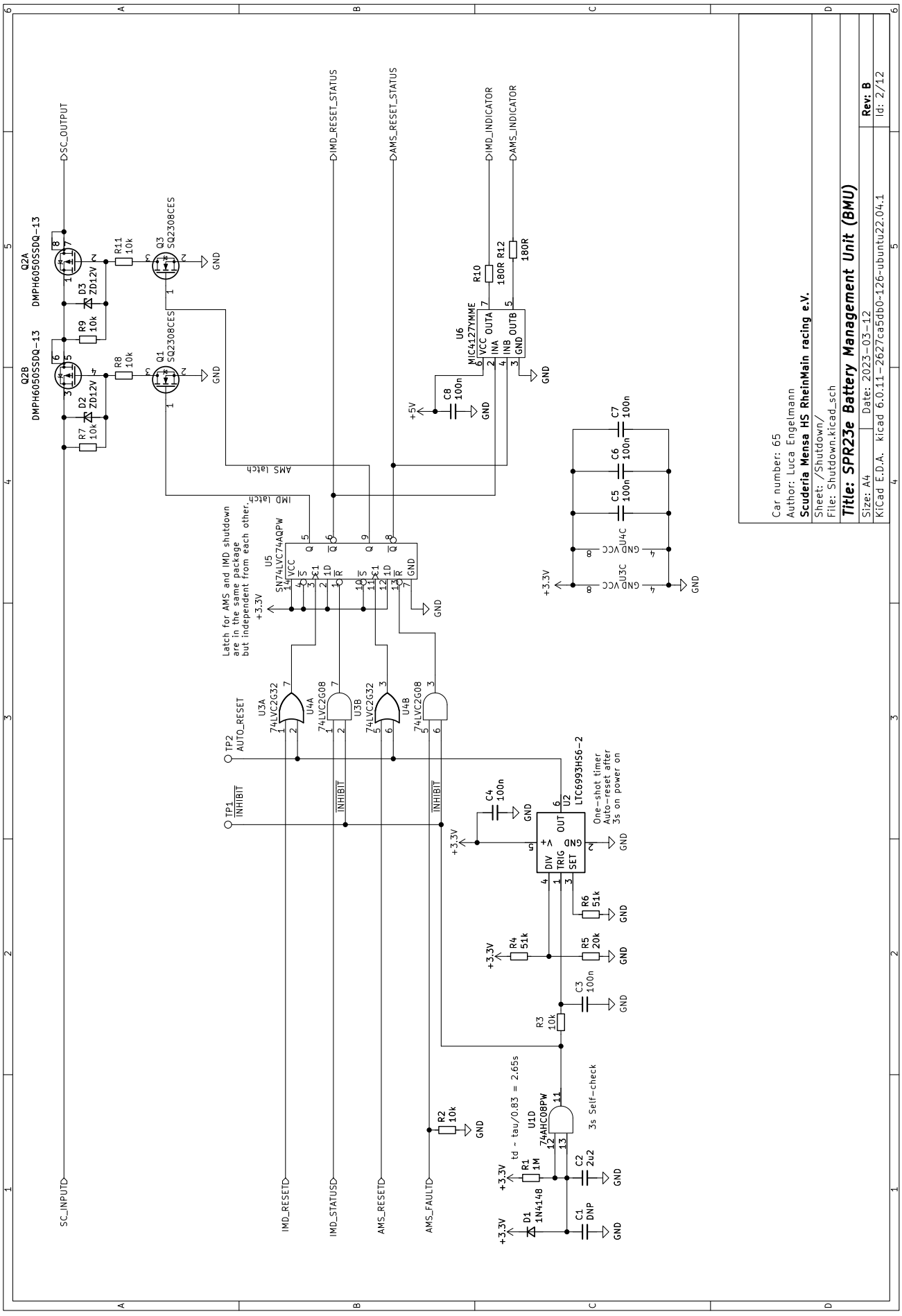
AMS-Master
Interface
Periphery
Discharge_Ctrl
TSAL
HVI
ADC
VCC
GND
SENSOR
LV ACCU
TS
ISO
LV_IO
SHIELD
SYMBOL
GNDGNDGNDGNDGND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Rev: B
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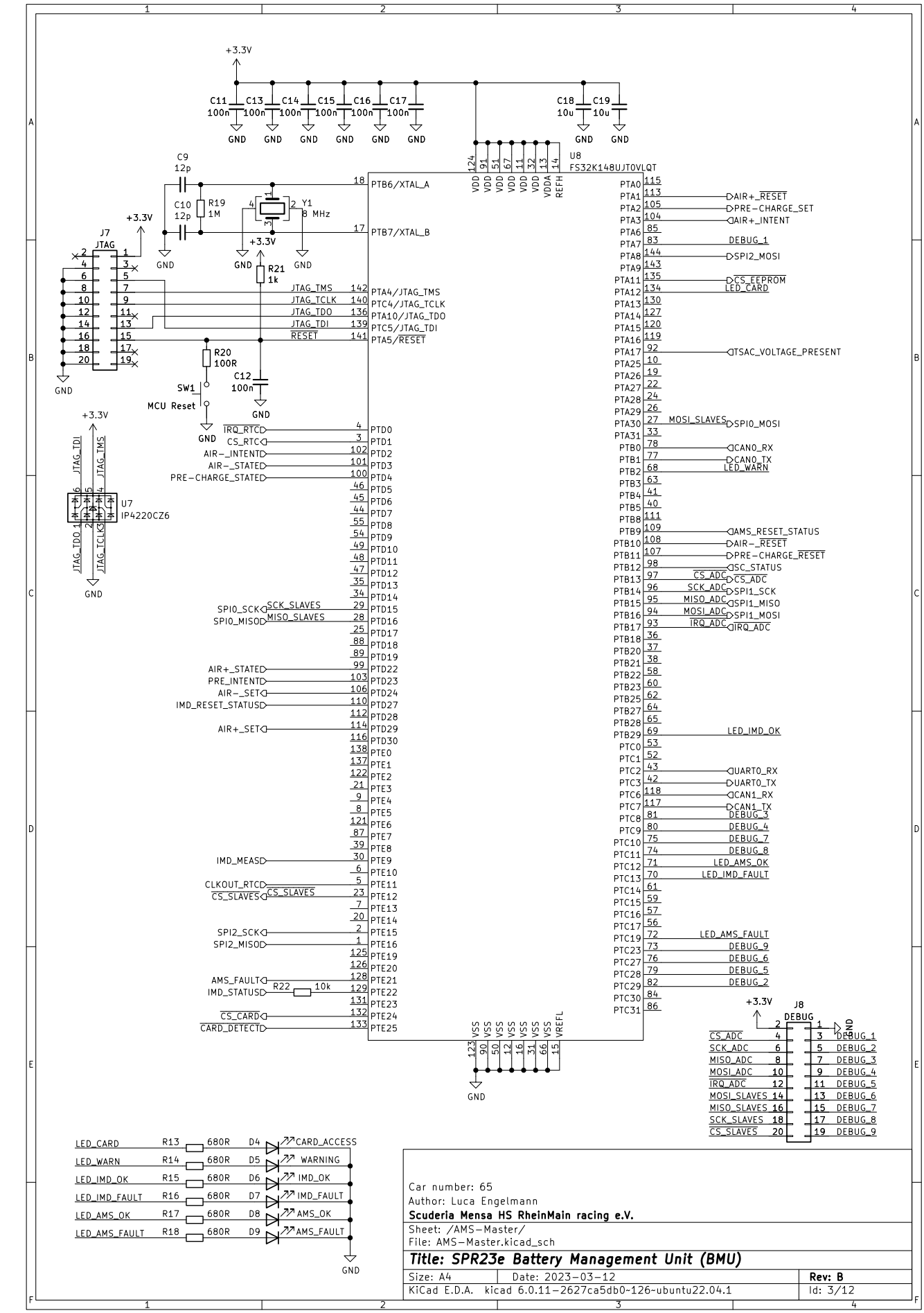
Id: 2/12
SC_INPUT
SC_OUTPUT
IMD_RESET_STATUS
AMS_RESET_STATUS
IMD_INDICATOR
AMS_INDICATOR
IMD_RESET
IMD_STATUS
AMS_RESET
AMS_FAULT
Latch for AMS and IMD shutdown are in the same package but independent from each other.
AMS latch
IMD latch
INHIBIT
One-shot timer Auto-reset after 3s on power on
td ~ tau/0.83 = 2.65s
3s Self-check
DMPH6050SSDQ-13
ZD12V
SQ2308CES
SN74LVC74AQPW
74LVC2G32
74LVC2G08
74AHC08PW
MIC4127YMME
LTC6993HS6-2
1N4148
DNP
AUTO_RESET
+3.3V
+5V
GND


+3.3V
C11 100n
C13 100n
C14 100n
C15 100n
C16 100n
C17 100n
C18 10u
C19 10u
GND
U8
FS32K148UJT0VLQT
C9 12p
C10 12p
R19 1M
Y1 8 MHz
R21 1k
J7 JTAG
R20 100R
C12 100n
SW1
MCU Reset
U7 IP4220CZ6
PTB6/XTAL_A
PTB7/XTAL_B
PTA4/JTAG_TMS
PTC4/JTAG_TCLK
PTA10/JTAG_TDO
PTC5/JTAG_TDI
PTA5/RESET
JTAG_TMS
JTAG_TCLK
JTAG_TDO
JTAG_TDI
RESET
IRQ_RTC
CS_RTC
AIR-_INTENT
AIR-_STATE
PRE-CHARGE_STATE
SPI0_SCK
SPI0_MISO
SCK_SLAVES
MISO_SLAVES
AIR+_STATE
PRE_INTENT
AIR-_SET
IMD_RESET_STATUS
AIR+_SET
IMD_MEAS
CLKOUT_RTC
CS_SLAVES
SPI2_SCK
SPI2_MISO
AMS_FAULT
IMD_STATUS
R22 10k
CS_CARD
CARD_DETECT
AIR+_RESET
PRE-CHARGE_SET
AIR+_INTENT
DEBUG_1
SPI2_MOSI
CS_EEPROM
LED_CARD
TSAC_VOLTAGE_PRESENT
MOSI_SLAVES
SPI0_MOSI
CAN0_RX
CAN0_TX
LED_WARN
AMS_RESET_STATUS
AIR-_RESET
PRE-CHARGE_RESET
TSC_STATUS
CS_ADC
SCK_ADC
MISO_ADC
MOSI_ADC
IRQ_ADC
SPI1_SCK
SPI1_MISO
SPI1_MOSI
LED_IMD_OK
UART0_RX
UART0_TX
CAN1_RX
CAN1_TX
DEBUG_3
DEBUG_4
DEBUG_7
DEBUG_8
LED_AMS_OK
LED_IMD_FAULT
LED_AMS_FAULT
DEBUG_9
DEBUG_6
DEBUG_5
DEBUG_2
J8 DEBUG
LED_CARD R13 680R D4 CARD_ACCESS
LED_WARN R14 680R D5 WARNING
LED_IMD_OK R15 680R D6 IMD_OK
LED_IMD_FAULT R16 680R D7 IMD_FAULT
LED_AMS_OK R17 680R D8 AMS_OK
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Scuderia Mensa HS RheinMain racing e.V.
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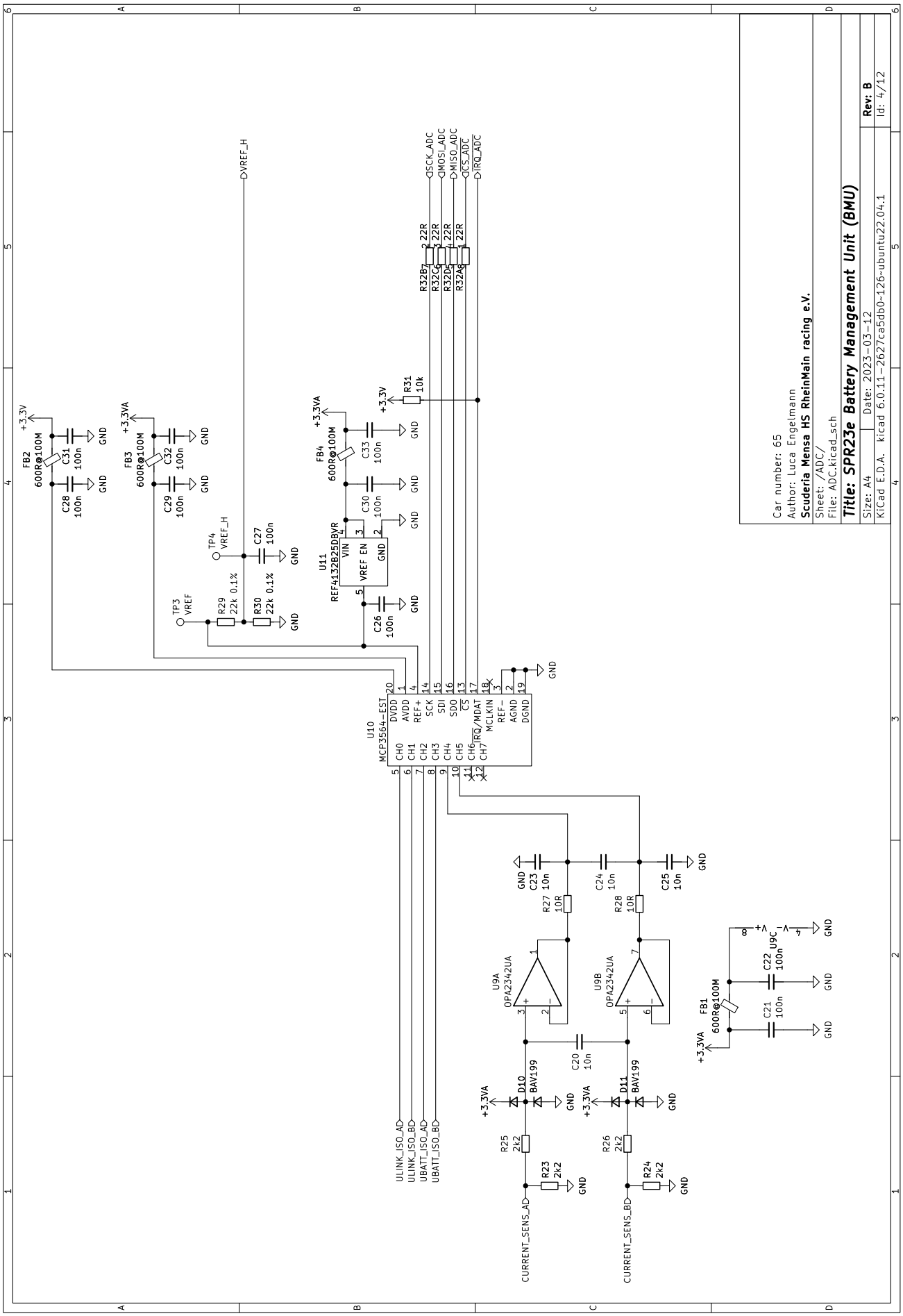
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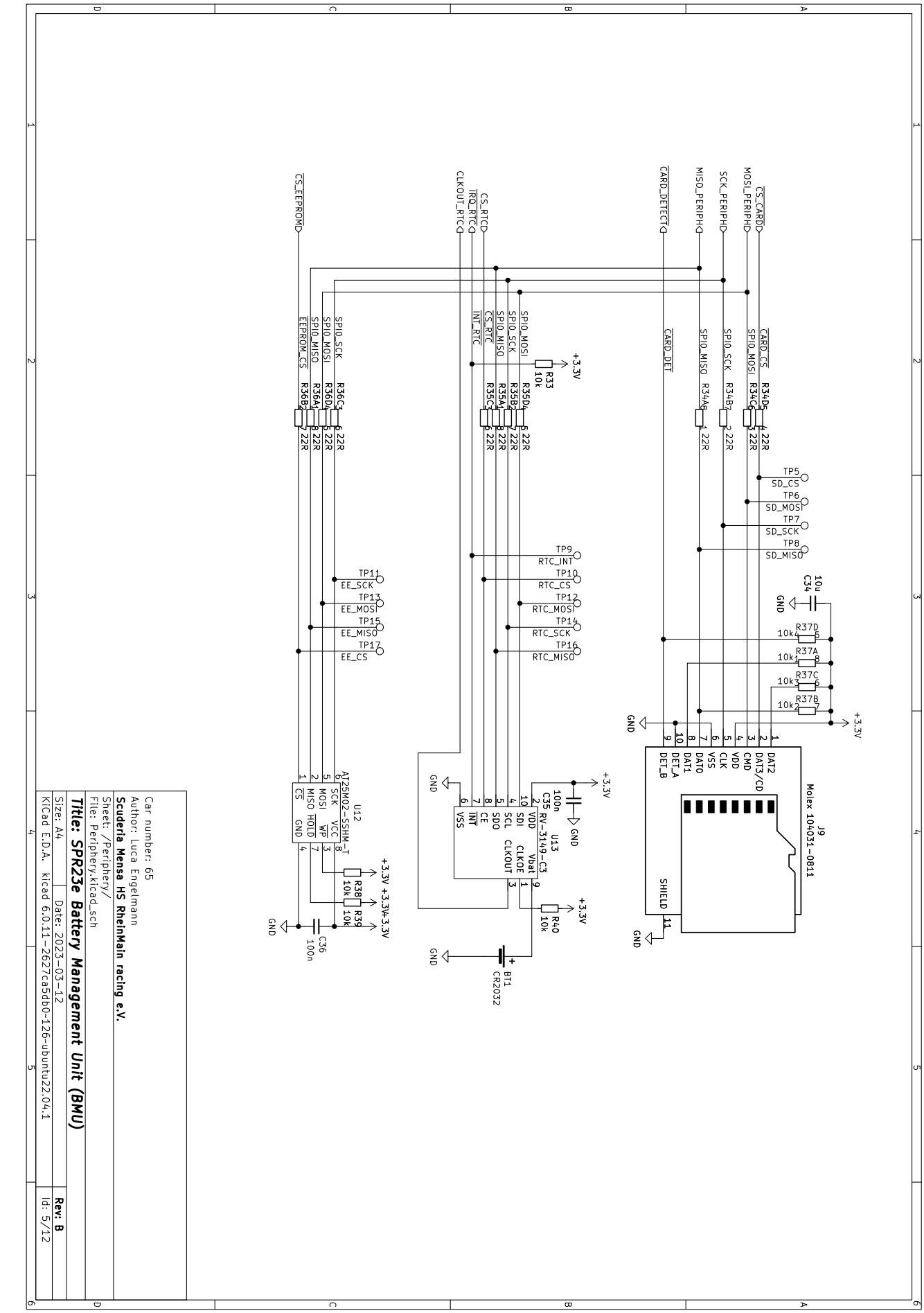
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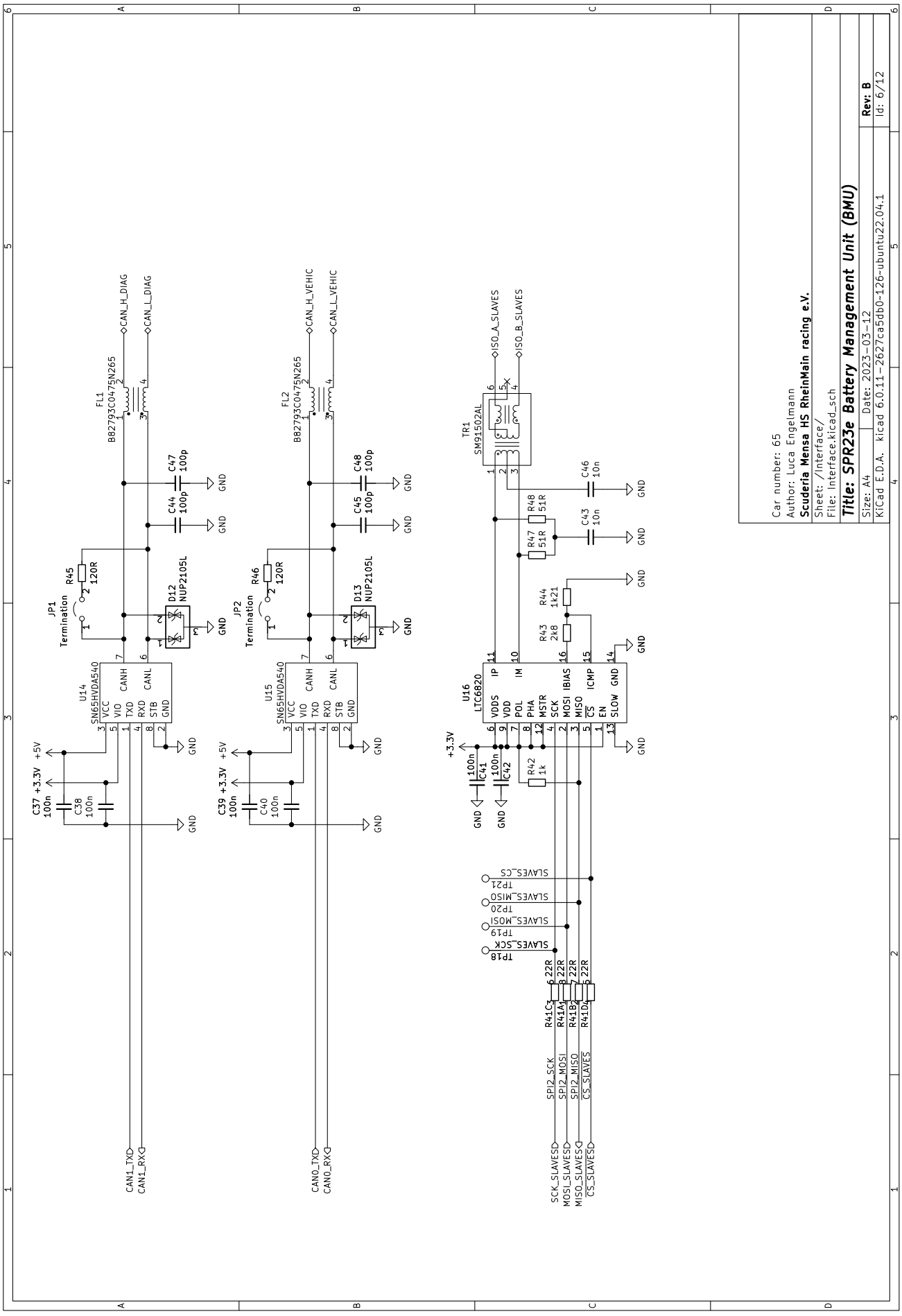
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FL2
B82793C0475N265
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SM91502AL
U14
SN65HVDA540
U15
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U16
LTC6820
JP1
Termination
JP2
Termination
R45
120R
R46
120R
D12
NUP2105L
D13
NUP2105L
CAN_H_DIAG
CAN_L_DIAG
CAN_H_VEHIC
CAN_L_VEHIC
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ISO_B_SLAVES
CAN1_TXD
CAN1_RXD
CAN0_TXD
CAN0_RXD
SCK_SLAVES
MOSI_SLAVES
MISO_SLAVES
CS_SLAVES
SPI2_SCK
SPI2_MOSI
SPI2_MISO
CS_SLAVES
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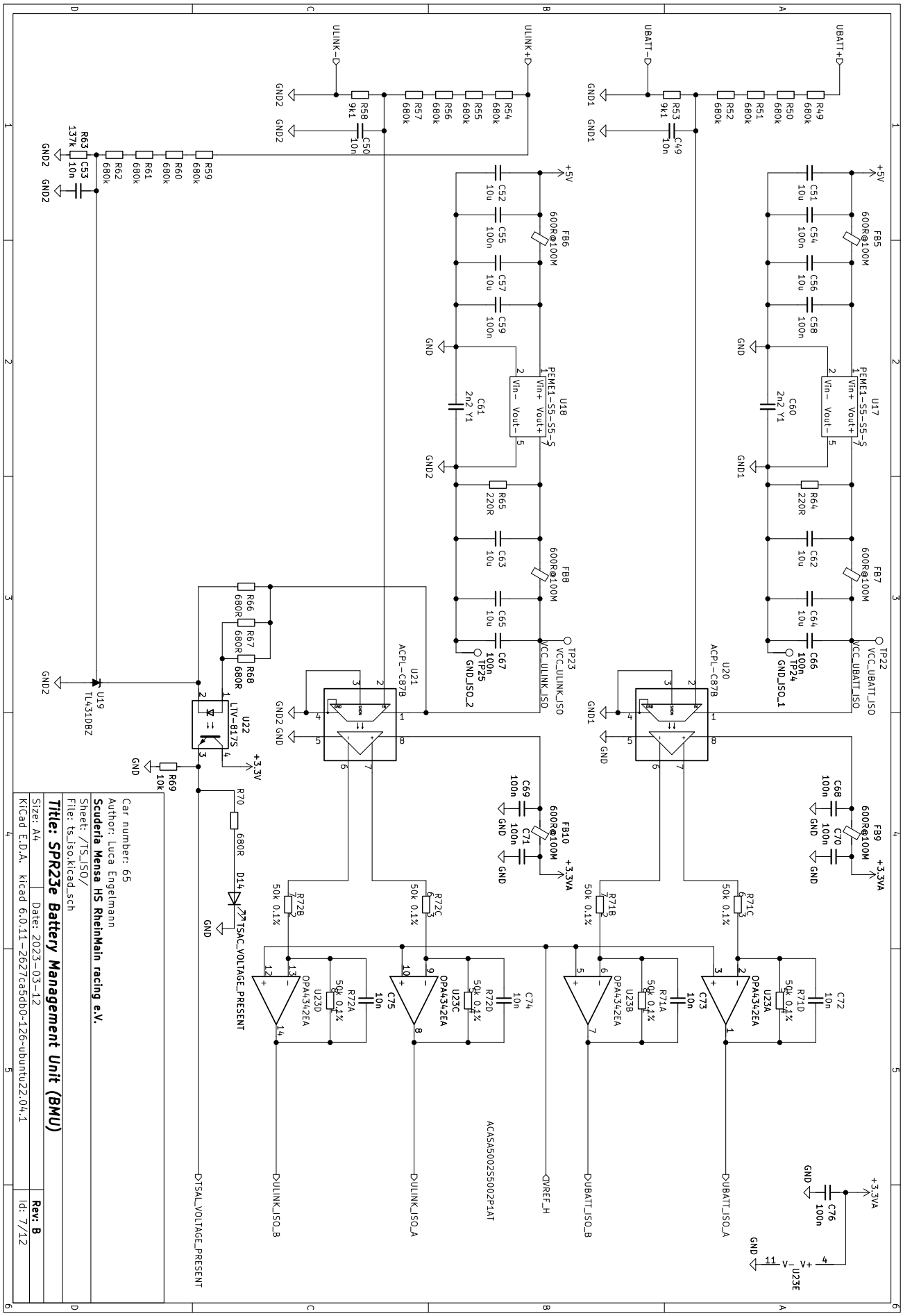
SLAVES_MISO
SLAVES_CS
+5V
+3.3V
GND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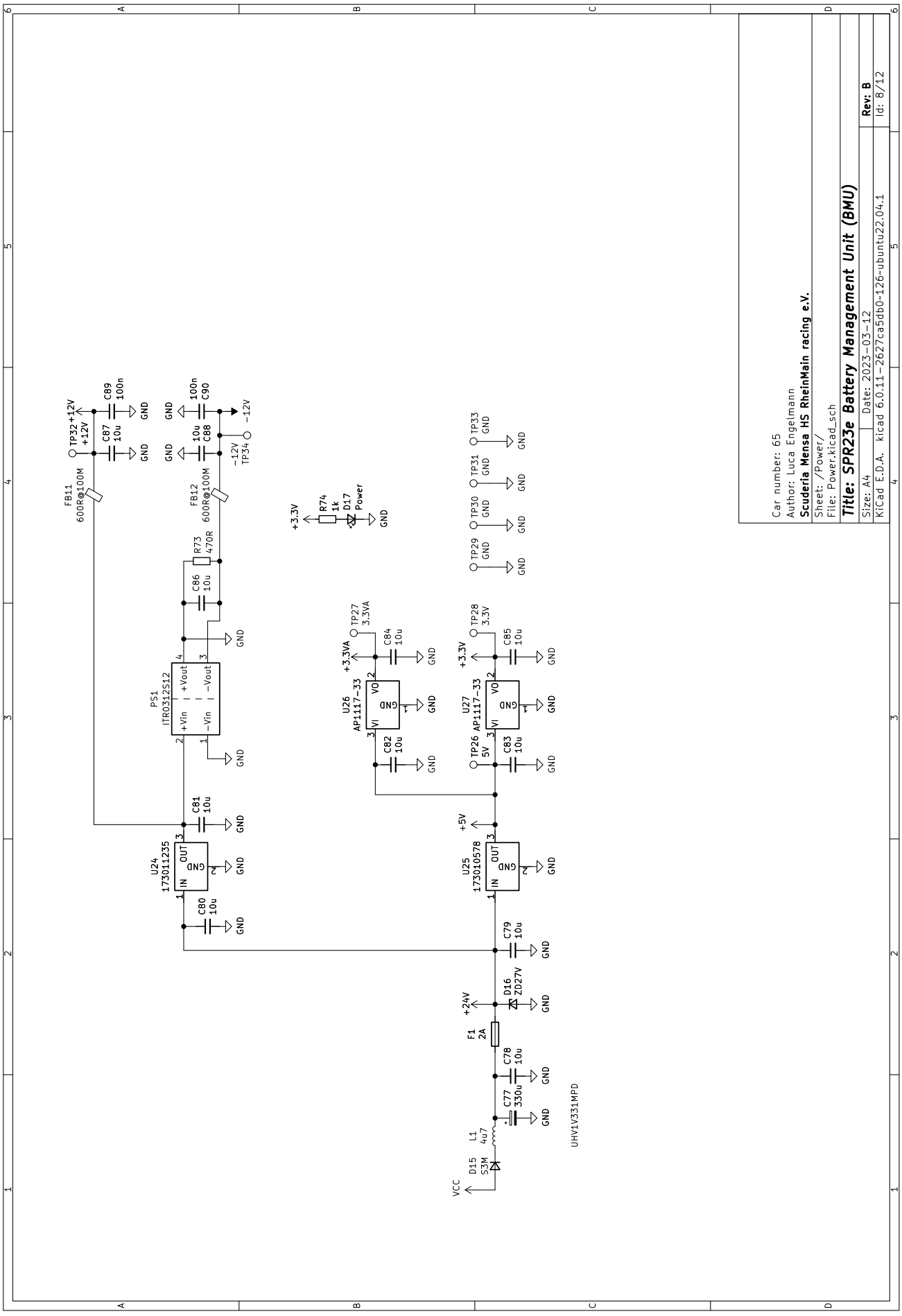
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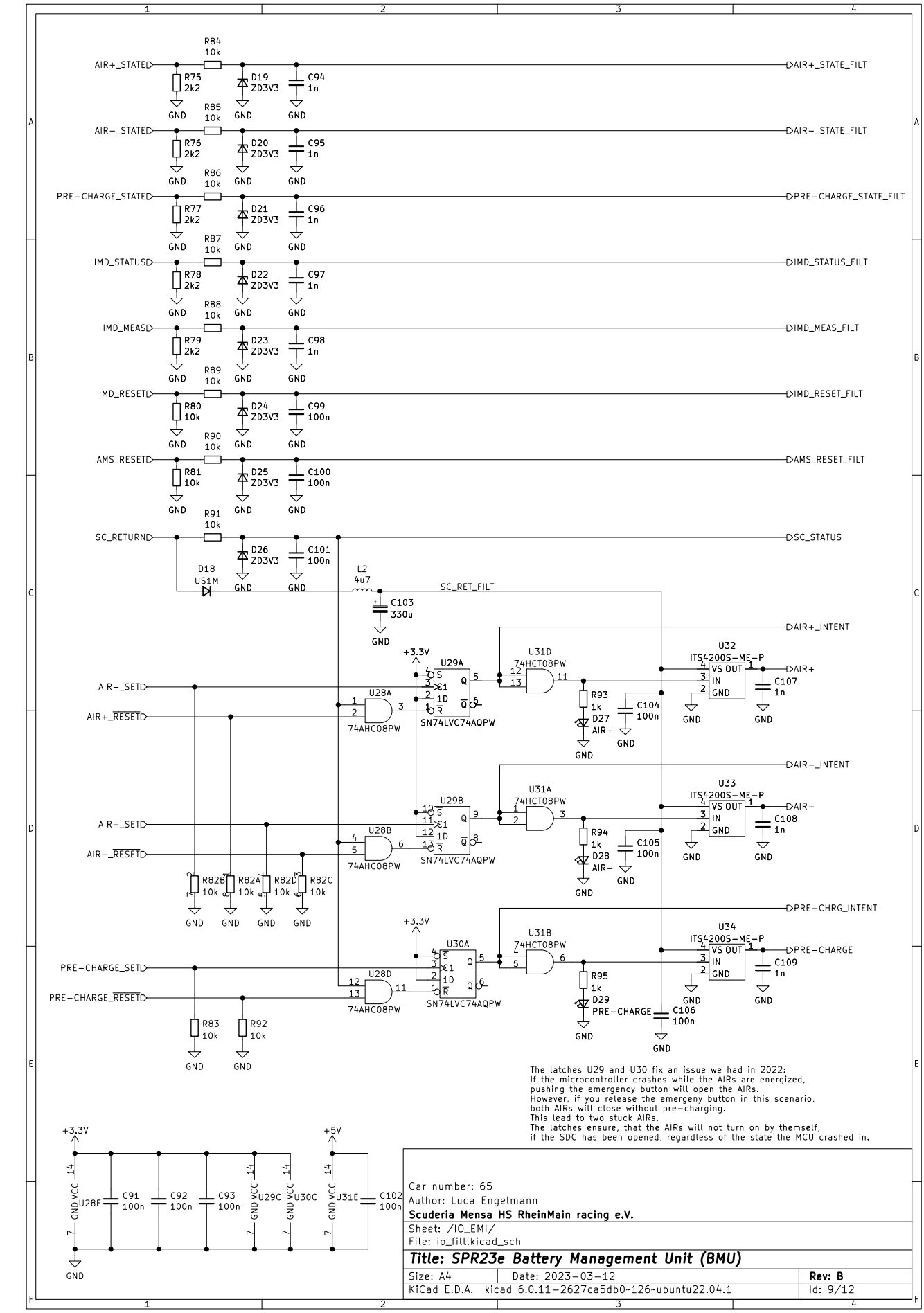
C89 100n
C97 10u
FB11 600R@100M
FB12 600R@100M
C90 100n
C88 10u
TP34 -12V
R73 470R
C86 10u
PS1 ITR0312S12
C81 10u
U24 173011235
C80 10u
R74 1k
D17 Power
+3.3V
TP27 3.3VA
C84 10u
U26 AP1117-33
C82 10u
TP28 3.3V
C85 10u
U27 AP1117-33
TP26 5V
C83 10u
TP29 GND
TP30 GND
TP31 GND
TP33 GND
+5V
U25 173010578
C79 10u
D16 ZD27V
+24V
F1 2A
C78 10u
C77 330u
L1 4u7
D15 S3M
VCC
UHV1V331MPD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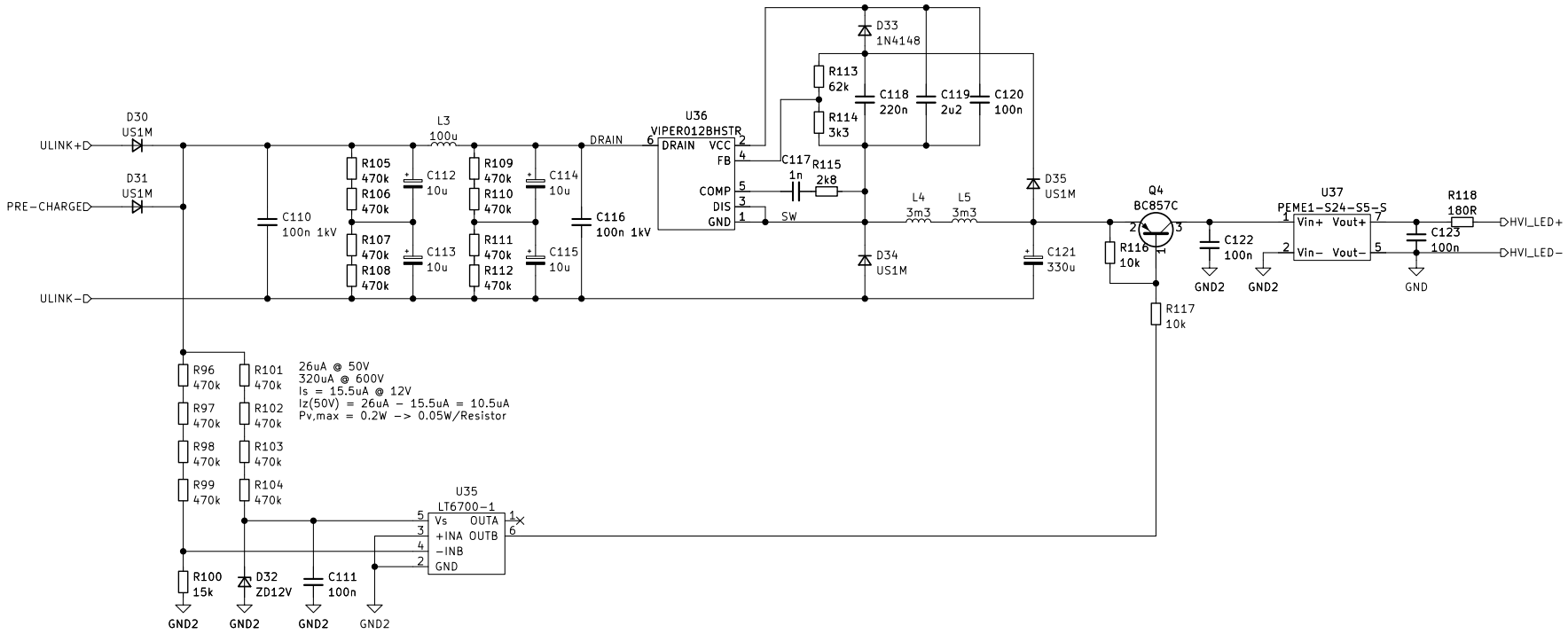
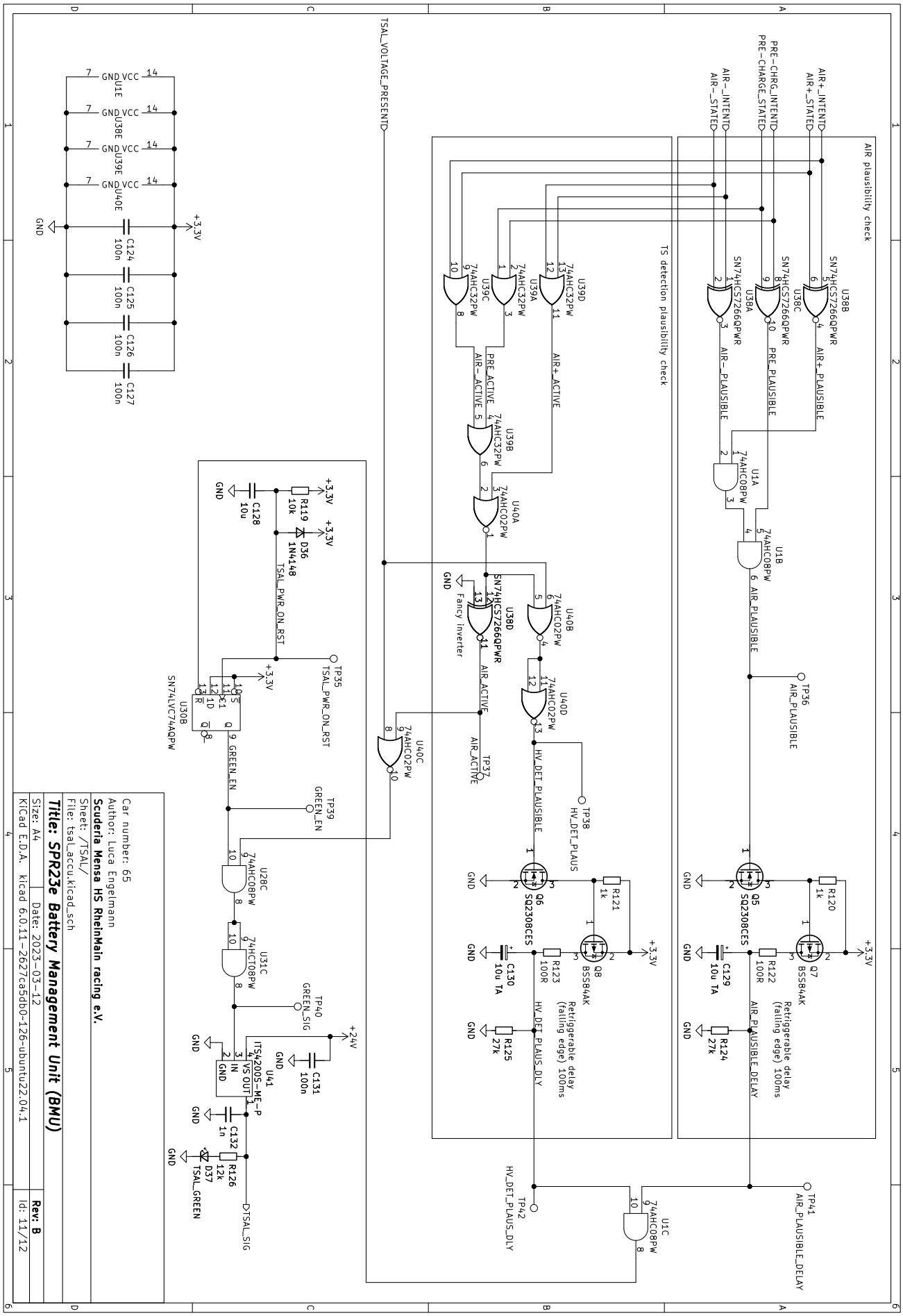
AIR−_STATE
PRE−CHARGE_STATE
IMD_STATUS
IMD_MEAS
IMD_RESET
AMS_RESET
SC_RETURN
R84 10k
R85 10k
R86 10k
R87 10k
R88 10k
R89 10k
R90 10k
R91 10k
R75 2k2
R76 2k2
R77 2k2
R78 2k2
R79 2k2
R80 10k
R81 10k
D19 ZD3V3
D20 ZD3V3
D21 ZD3V3
D22 ZD3V3
D23 ZD3V3
D24 ZD3V3
D25 ZD3V3
D26 ZD3V3
C94 1n
C95 1n
C96 1n
C97 1n
C98 1n
C99 100n
C100 100n
C101 100n
GND
AIR+_STATE_FILT
AIR−_STATE_FILT
PRE−CHARGE_STATE_FILT
IMD_STATUS_FILT
IMD_MEAS_FILT
IMD_RESET_FILT
AMS_RESET_FILT
SC_STATUS
D18 US1M
L2 4u7
C103 330u
SC_RET_FILT
AIR+_INTENT
AIR−_INTENT
PRE−CHRG_INTENT
AIR+_SET
AIR+_RESET
AIR−_SET
AIR−_RESET
PRE−CHARGE_SET
PRE−CHARGE_RESET
+3.3V
U28A
U28B
U28D
74AHC08PW
U29A
U29B
U30A
SN74LVC74AQPW
U31A
U31B
U31D
74HCT08PW
R82A 10k
R82B 10k
R82C 10k
R82D 10k
R83 10k
R92 10k
R93 1k
R94 1k
R95 1k
D27 AIR+
D28 AIR−
D29 PRE−CHARGE
C104 100n
C105 100n
C106 100n
U32
U33
U34
ITS4200S−ME−P
VS OUT
IN
C107 1n
C108 1n
C109 1n
AIR+
AIR−
PRE−CHARGE
The latches U29 and U30 fix an issue we had in 2022:
If the microcontroller crashes while the AIRs are energized,
pushing the emergency button will open the AIRs.
However, if you release the emergeny button in this scenario,
both AIRs will close without pre−charging.
This lead to two stuck AIRs.
The latches ensure, that the AIRs will not turn on by themself,
if the SDC has been opened, regardless of the state the MCU crashed in.
+5V
U28E
U29C
U30C
U31E
C91 100n
C92 100n
C93 100n
C102 100n
VCC
GND
Car number: 65
Author: Luca Engelmann
Scuderia Mensa HS RheinMain racing e.V.
Sheet: /IO_EMI/
File: io_filt.kicad_sch
Title: SPR23e Battery Management Unit (BMU)
Size: A4
Date: 2023−03−12
Rev: B
KiCad E.D.A. kicad 6.0.11−2627ca5db0~126~ubuntu22.04.1
Id: 9/12

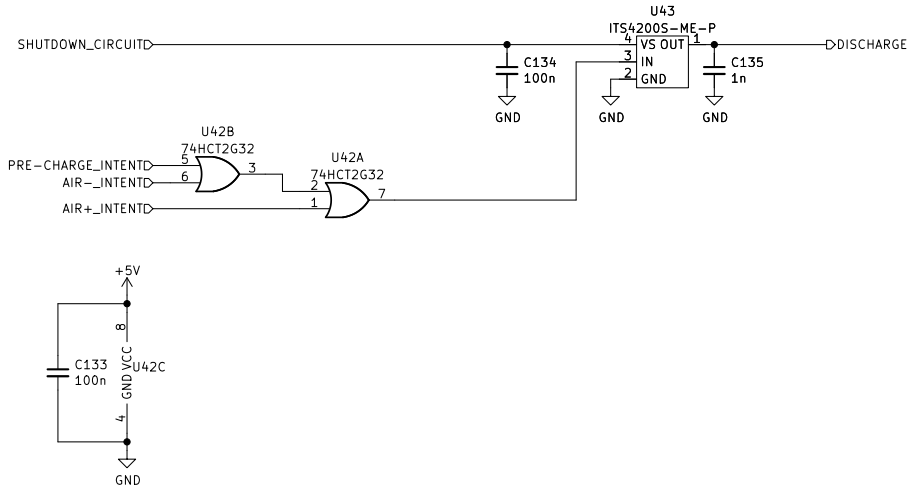
U35 is a regulated buck converter, which converts the TS voltage down to 24V.
It operates in a range of 50V to 600V and is not galvanically isolated.
Below 50V, the output is unstable and starts to pulse at a slow rate.
U36 is a galvanically isolated DCDC converter, which isolates the LED supply from the TS.
To ensure a hard on/off transistion of the LED at 50V,
U34 compares the input voltage to an internal reference.
It is powered from the TS, since it has to operate even if U35 is not regulating yet.
The circuit is powered from the TSAC output as well as from the node between pre-charge relay and pre-charge resistor. Otherwise, the circuit would load the TS voltage down during pre-cahrge, effectively preventing the pre-charge.



Car number: 65 Author: Luca Engelmann **Scuderia Mensa HS RheinMain racing e.V.**		
Sheet: /HVI/ File: voltage_indicator.kicad_sch		
Title: SPR23e Battery Management Unit (BMU)		
Size: A4	Date: 2023-03-12	**Rev: B**
KiCad E.D.A.	kicad 6.0.11-2627ca5db0~126~ubuntu22.04.1	Id: 10/12


AIR plausibility check
TS detection plausibility check
AIR+_INTENTD
AIR+_STATED
PRE-CHRG_INTENTD
PRE-CHARGE_STATED
AIR-_INTENTD
AIR-_STATED
TSAL_VOLTAGE_PRESENTD
U38B SN74HCS72G6QPWR
U38C SN74HCS72G6QPWR
U38A SN74HCS72G6QPWR
U39D 74AHC32PW
U39A 74AHC32PW
U39C 74AHC32PW
U39B 74AHC32PW
U40A 74AHC02PW
U38D SN74HCS72G6QPWR
U40B 74AHC02PW
U40D 74AHC02PW
U40C 74AHC02PW
U1A 74AHC08PW
U1B 74AHC08PW
U1C 74AHC08PW
U28C 74AHC08PW
U31C 74HCT08PW
U30B SN74LVC74AQPW
U41 ITS4200S-ME-P
U1E GND VCC
U38E GND VCC
U39E GND VCC
U40E GND VCC
C124 100n
C125 100n
C126 100n
C127 100n
C128 10u
C129 10u TA
C130 10u TA
C131 100n
C132 1n
R119 10k
R120 1k
R121 1k
R122 100R
R123 100R
R124 27k
R125 27k
R126 12k
D36 1N4148
D37 TSAL_GREEN
Q5 SQ2308CES
Q6 SQ2308CES
Q7 BSS84AK
Q8 BSS84AK
Retriggerable delay (falling edge) 100ms
Retriggerable delay (falling edge) 100ms
Fancy inverter
PRE_PLAUSIBLE
AIR-_PLAUSIBLE
AIR+_PLAUSIBLE
AIR_PLAUSIBLE
AIR_PLAUSIBLE_DELAY
PRE_ACTIVE
AIR-_ACTIVE
AIR+_ACTIVE
AIR_ACTIVE
HV_DET_PLAUSIBLE
HV_DET_PLAUS_DLY
TSAL_PWR_ON_RST
GREEN_EN
GREEN_SIG
TSAL_SIG
TP35 TSAL_PWR_ON_RST
TP36 AIR_PLAUSIBLE
TP37 AIR_ACTIVE
TP38 HV_DET_PLAUS
TP39 GREEN_EN
TP40 GREEN_SIG
TP41 AIR_PLAUSIBLE_DELAY
TP42 HV_DET_PLAUS_DLY
+3.3V
+24V
GND
Car number: 65
Author: Luca Engelmann
Scuderia Mensa HS RheinMain racing e.V.
Sheet: /TSAL/
File: tsal_accu.kicad_sch
Title: SPR23e Battery Management Unit (BMU)
Size: A4
Date: 2023-03-12
KiCad E.D.A. kicad 6.0.11-2627ca5db0-126~ubuntu22.04.1
Rev: B
Id: 11/12

The discharge circuit in the inverter is controlled by the shutdown circuit. To ensure that the discharge circuit is still enabled while the shutdown circuit is closed but TS is still off, the intentional states of the AIRs are used. The discharge circuit is disabled as soon as any of the AIRs is active but still re-activated if an AIR is stuck.

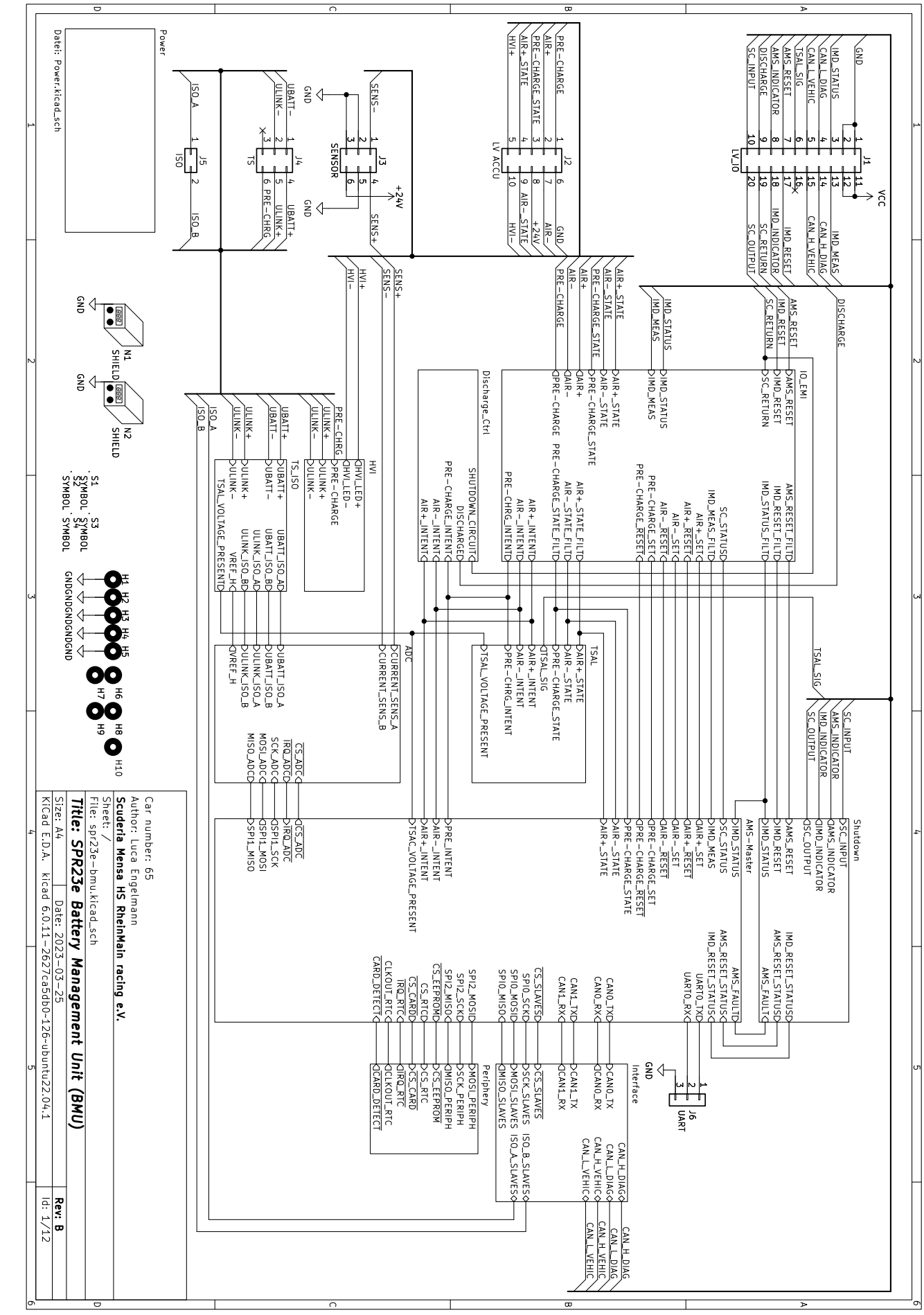


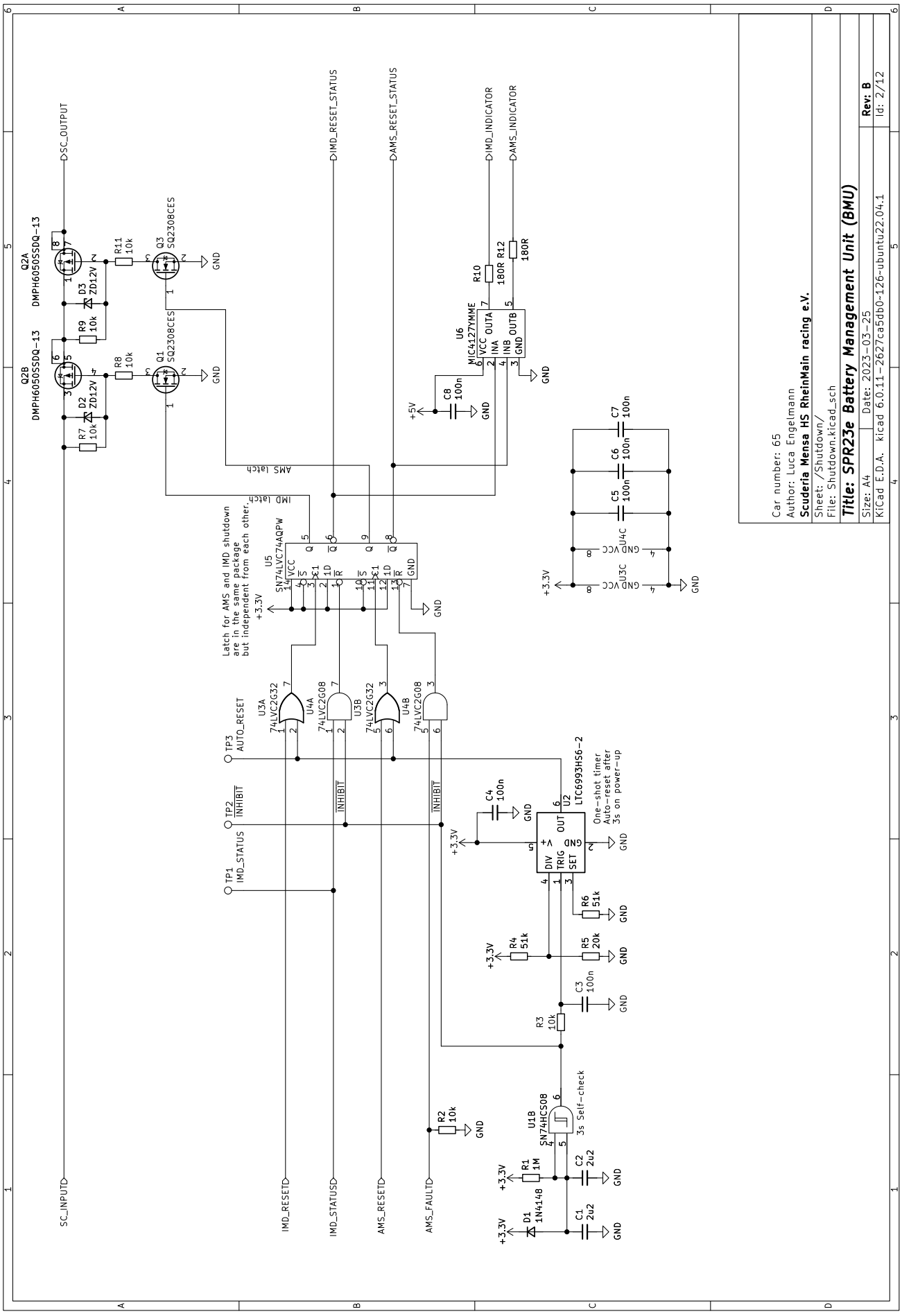
Car number: 65 Author: Luca Engelmann **Scuderia Mensa HS RheinMain racing e.V.**		
Sheet: /Discharge_Ctrl/ File: discharge.kicad_sch		
Title: SPR23e Battery Management Unit (BMU)		
Size: A4	Date: 2023-03-12	**Rev: B**
KiCad E.D.A. kicad 6.0.11-2627ca5db0-126-ubuntu22.04.1		Id: 12/12

B. Changelog Revision B

- Corrected pinout of 74xx08
- Corrected pinout of 74xx2G08
- Corrected pinout of 74xx32
- Corrected pinout of 74xx2G32
- 74AHC08PW has no "real" Schmitt trigger inputs. Replaced by SN74HCS08.
- Removed ± 12 V power supplies from the BMU to clear out some space. It is only needed for the current sensor. Therefore it has been moved to the sensor PCB.
- Different comparator circuit for the voltage indicator for a sharp transition between on and off.
- Added minimum load for the isolated DCDC converters
- Increased the resistance value of the zener diode current limiting resistors at the inputs.
- Added test points for VREF, VREF_H and the outputs of the isolated DCDC converters.
- Increased the power-on-reset time for the TSAL latch
- Added ESD and overvoltage protection for the current sensor inputs
- Corrected the footprints of the electrolytic capacitors
- Corrected the footprints of the EMI suppression capacitors
- Corrected the control of the indicator LEDs. The LEDs must light up, if the power stage is disabled.
- Added pull-down resistor for the AMS fault signal
- Added a diode between SC_RET_FILT and SC_RETURN to decouple the high power signal from the low power signal.
- Typos corrected
- Changed reverse polarity protection diode for a higher current type
- Changed LED dropper resistors for equalized brightness
- Changed shutdown circuit auto-reset time to 3 s since IMD takes up to two seconds to power up.
- Only one power LED at the 3.3 V rail
- Reduced the delay time for the AIR plausibility to 100 ms to reduce BOM. 100 ms is sufficient.

C. Schematics Revision B


Car number: 65
Author: Luca Engelmann
Scuderia Mensa HS RheinMain racing e.V.
Sheet: /
File: spr23e-bmu.kicad_sch
Title: SPR23e Battery Management Unit (BMU)
Size: A4
Date: 2023-03-25
Rev: B
KiCad E.D.A. kicad 6.0.11-2627ca5db0~126~ubuntu22.04.1
Id: 1/12
Power
Datei: Power.kicad_sch
Shutdown
AMS-Master
Interface
Periphery
Discharge_Ctrl
HVI
TSAL
ADC
IO_EMI
VCC
SENSOR
LV ACCU
TS
ISO
GND
+24V
SHIELD
UART
SCH_INPUT
AMS_INDICATOR
IMD_INDICATOR
SC_OUTPUT
AMS_RESET
IMD_RESET
SC_RETURN
IMD_STATUS
IMD_MEAS
DISCHARGE
TSAL_SIG
AIR+_STATE
AIR-_STATE
PRE-CHARGE_STATE
AIR+
AIR-
PRE-CHARGE
PRE-CHARGE_SET
PRE-CHARGE_RESET
AIR+_SET
AIR+_RESET
AIR-_SET
AIR-_RESET
IMD_MEAS_FILTD
SC_STATUS
AMS_FAULT
IMD_RESET_STATUS
UART0_TX
UART0_RX
CAN0_TX
CAN0_RX
CAN1_TX
CAN1_RX
CAN_H_DIAG
CAN_L_DIAG
CAN_H_VEHIC
CAN_L_VEHIC
CS_SLAVES
SPI0_SCK
SPI0_MOSI
SPI0_MISO
SCK_SLAVES
MOSI_SLAVES
MISO_SLAVES
ISO_B_SLAVES
ISO_A_SLAVES
SPI2_MOSI
SPI2_SCK
SPI2_MISO
CS_EEPROM
CS_RTC
CS_CARD
IRQ_RTC
CLKOUT_RTC
CARD_DETECT
MOSI_PERIPH
SCK_PERIPH
MISO_PERIPH
CS_EEPROM
CS_RTC
CS_CARD
IRQ_RTC
CLKOUT_RTC
CARD_DETECT
PRE_INTENT
AIR-_INTENT
AIR+_INTENT
TSAC_VOLTAGE_PRESENT
TSAL_VOLTAGE_PRESENT
AIR+_INTENT
AIR-_INTENT
PRE-CHRG_INTENT
SHUTDOWN_CIRCUIT
DISCHARGED
PRE-CHARGE_INTENT
AIR-_INTENT
AIR+_INTENT
AIR+_STATE_FILTD
AIR-_STATE_FILTD
PRE-CHARGE_STATE_FILTD
AIR+_INTENT
AIR-_INTENT
PRE-CHRG_INTENT
AMS_RESET_FILTD
IMD_RESET_FILTD
IMD_STATUS_FILTD
SENS+
SENS-
HVI+
HVI-
PRE-CHRG
PRE-CHARGE
ULINK+
ULINK-
UBATT+
UBATT-
ISO_A
ISO_B
TS_ISO
UBATT_ISO_A
UBATT_ISO_B
ULINK_ISO_A
ULINK_ISO_B
VREF_H
TSAL_VOLTAGE_PRESENT
CURRENT_SENS_A
CURRENT_SENS_B
CS_ADC
IRQ_ADC
SCK_ADC
MOSI_ADC
MISO_ADC
CSPI1_SCK
CSPI1_MOSI
CSPI1_MISO
HVI_LED+
HVI_LED-
N1
N2
S1
S2
S3
S4
SYMBOL
H1
H2
H3
H4
H5
H6
H7
H8
H9
H10
GNDGNDGNDGNDGND
J1
J2
J3
J4
J5
J6


Car number: 65
Author: Luca Engelmann
Scuderia Mensa HS RheinMain racing e.V.
Sheet: /Shutdown/
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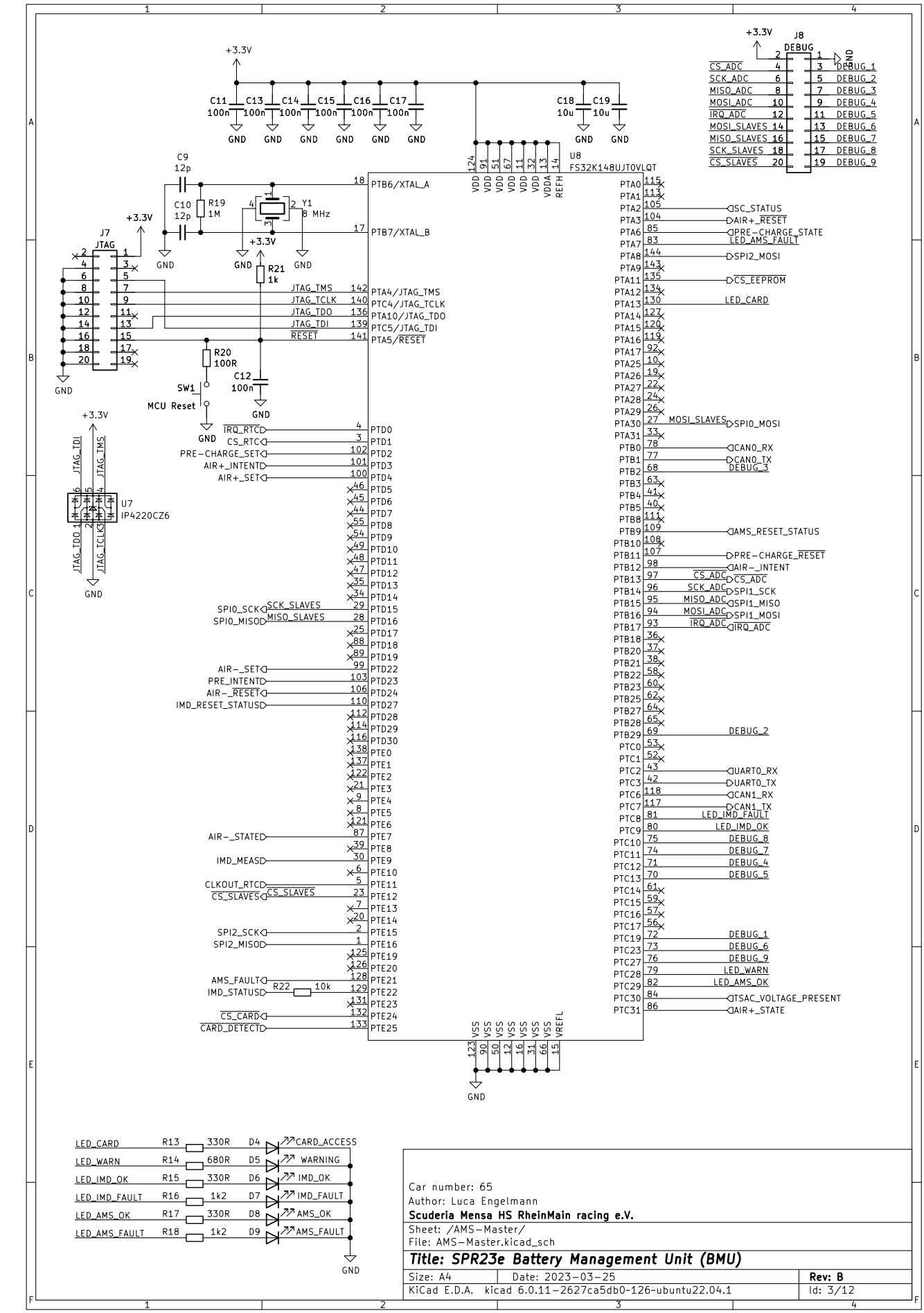
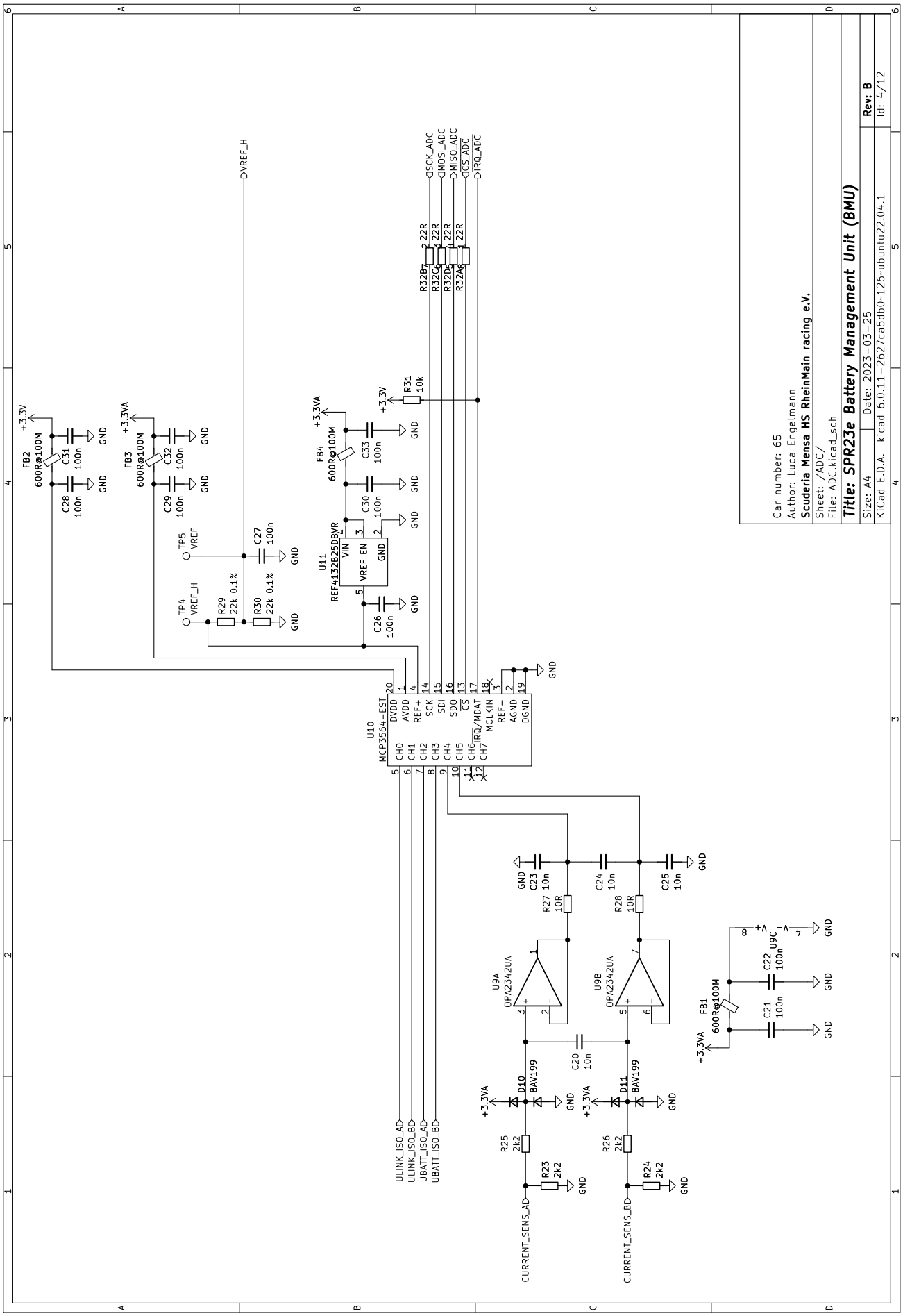
Title: SPR23e Battery Management Unit (BMU)
Size: A4
Date: 2023-03-25
Rev: B
KiCad E.D.A. kicad 6.0.11-2627ca5db0-126-ubuntu22.04.1
Id: 2/12
SC_OUTPUT
IMD_RESET_STATUS
AMS_RESET_STATUS
IMD_INDICATOR
AMS_INDICATOR
Q2A DMPH6050SSDQ-13
Q2B DMPH6050SSDQ-13
Q1 SQ2308CES
Q3 SQ2308CES
D2 ZD12V
D3 ZD12V
R7 10k
R8 10k
R9 10k
R11 10k
R10 180R
R12 180R
U6 MIC4127YMME
C8 100n
C7 100n
C6 100n
C5 100n
AMS latch
IMD latch
Latch for AMS and IMD shutdown are in the same package but independent from each other.
U5 SN74LVC74AQPW
U3A 74LVC2G32
U4A 74LVC2G08
U3B 74LVC2G32
U4B 74LVC2G08
U3C
U4C
TP3 AUTO_RESET
TP2 INHIBIT
TP1 IMD_STATUS
INHIBIT
C4 100n
U2 LTC6993HS6-2
One-shot timer
Auto-reset after
3s on power-up
R6 51k
R4 51k
R5 20k
C3 100n
R3 10k
R2 10k
U1B SN74HCS08
3s Self-check
R1 1M
C2 2u2
C1 2u2
D1 1N4148
SC_INPUTD
IMD_RESETD
IMD_STATUSD
AMS_RESETD
AMS_FAULTD
+3.3V
+5V
GND


U8
FS32K148UJT0VLQT
J7
JTAG
J8
DEBUG
U7
IP4220CZ6
SW1
MCU Reset
Y1
8 MHz
C9
12p
C10
12p
R19
1M
R21
1k
R20
100R
C12
100n
C11
100n
C13
100n
C14
100n
C15
100n
C16
100n
C17
100n
C18
10u
C19
10u
+3.3V
GND
JTAG_TMS
JTAG_TCLK
JTAG_TDO
JTAG_TDI
RESET
PTB6/XTAL_A
PTB7/XTAL_B
PTA4/JTAG_TMS
PTC4/JTAG_TCLK
PTA10/JTAG_TDO
PTC5/JTAG_TDI
PTA5/RESET
IRQ_RTC
CS_RTC
PRE-CHARGE_SET
AIR+_INTENT
AIR+_SET
SPI0_SCK
SPI0_MISO
SCK_SLAVES
MISO_SLAVES
AIR-_SET
PRE_INTENT
AIR-_RESET
IMD_RESET_STATUS
AIR-_STATE
IMD_MEAS
CLKOUT_RTC
CS_SLAVES
SPI2_SCK
SPI2_MISO
AMS_FAULT
IMD_STATUS
R22
10k
CS_CARD
CARD_DETECT
CS_ADC
SCK_ADC
MISO_ADC
MOSI_ADC
IRQ_ADC
MOSI_SLAVES
MISO_SLAVES
SCK_SLAVES
CS_SLAVES
DEBUG_1
DEBUG_2
DEBUG_3
DEBUG_4
DEBUG_5
DEBUG_6
DEBUG_7
DEBUG_8
DEBUG_9
CS_STATUS
AIR+_RESET
PRE-CHARGE_STATE
LED_AMS_FAULT
SPI2_MOSI
CS_EEPROM
LED_CARD
SPI0_MOSI
CAN0_RX
CAN0_TX
AMS_RESET_STATUS
PRE-CHARGE_RESET
AIR-_INTENT
SPI1_SCK
SPI1_MISO
SPI1_MOSI
UART0_RX
UART0_TX
CAN1_RX
CAN1_TX
LED_IMD_FAULT
LED_IMD_OK
TSAC_VOLTAGE_PRESENT
AIR+_STATE
LED_CARD
R13
330R
D4
CARD_ACCESS
LED_WARN
R14
680R
D5
WARNING
LED_IMD_OK
R15
330R
D6
IMD_OK
LED_IMD_FAULT
R16
1k2
D7
IMD_FAULT
LED_AMS_OK
R17
330R
D8
AMS_OK
LED_AMS_FAULT
R18
1k2
D9
AMS_FAULT
Car number: 65
Author: Luca Engelmann
Scuderia Mensa HS RheinMain racing e.V.
Sheet: /AMS-Master/
File: AMS-Master.kicad_sch
Title: SPR23e Battery Management Unit (BMU)
Size: A4
Date: 2023-03-25
Rev: B
KiCad E.D.A. kicad 6.0.11-2627ca5db0~126~ubuntu22.04.1
Id: 3/12


Car number: 65
Author: Luca Engelmann
Scuderia Mensa HS RheinMain racing e.V.
Sheet: /ADC/
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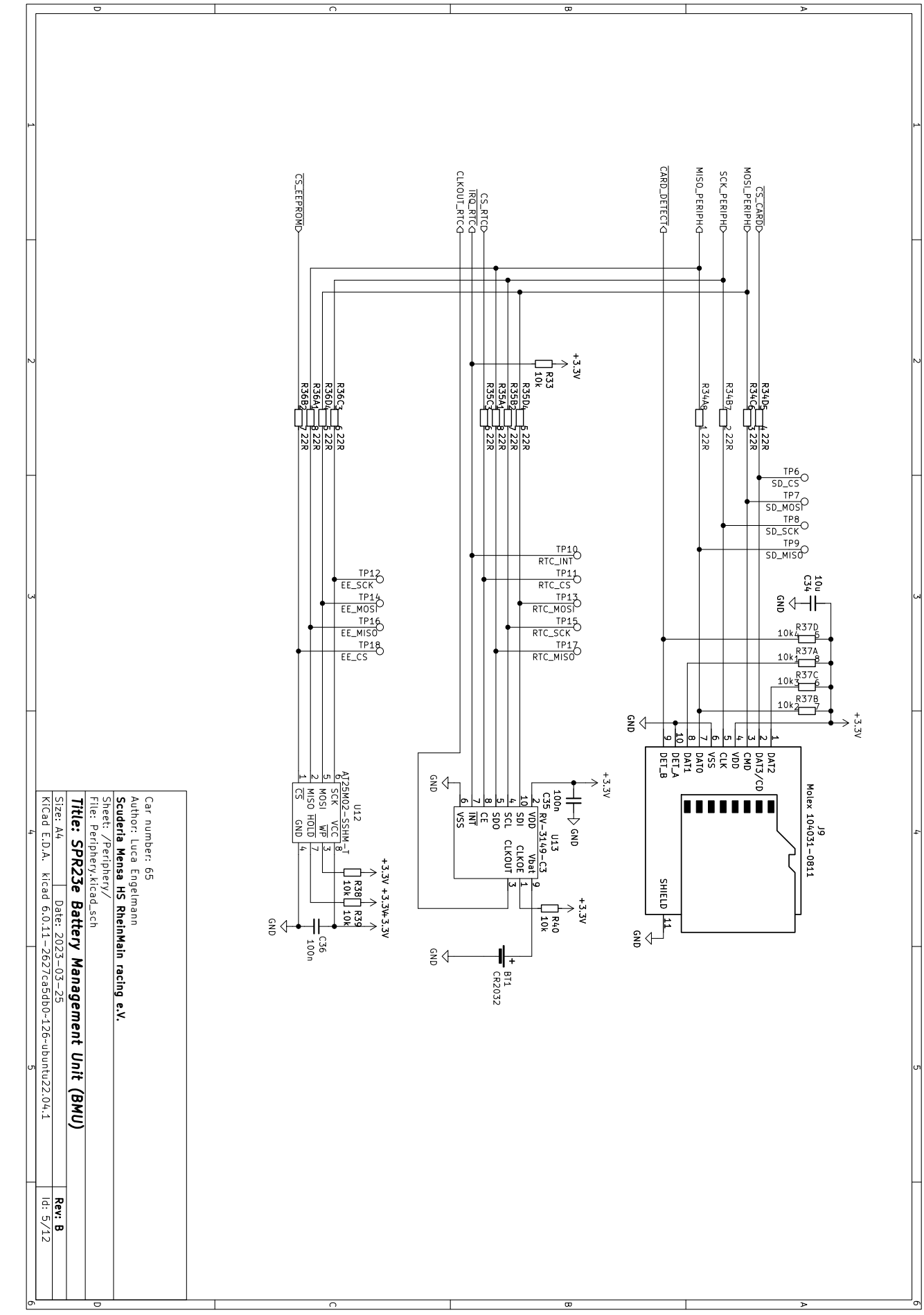
Title: SPR23e Battery Management Unit (BMU)
Size: A4
Date: 2023-03-25
Rev: B
KiCad E.D.A. kicad 6.0.11-2627ca5db0-126-ubuntu22.04.1
Id: 4/12
U10
MCP3564-EST
U11
REF4132B25DBVR
U9A
OPA2342UA
U9B
OPA2342UA
U9C
OPA2342UA
D10
BAV199
D11
BAV199
FB1
FB2
FB3
FB4
600R@100M
TP4
VREF_H
TP5
VREF
+3.3V
+3.3VA
GND
VREF_H
SCK_ADC
MOSI_ADC
MISO_ADC
CS_ADC
IRQ_ADC
ULINK_ISO_AD
ULINK_ISO_BD
UBATT_ISO_AD
UBATT_ISO_BD
CURRENT_SENS_AD
CURRENT_SENS_BD


Car number: 65
Author: Luca Engelmann
Scuderia Mensa HS RheinMain racing e.V.
Sheet: /Periphery/
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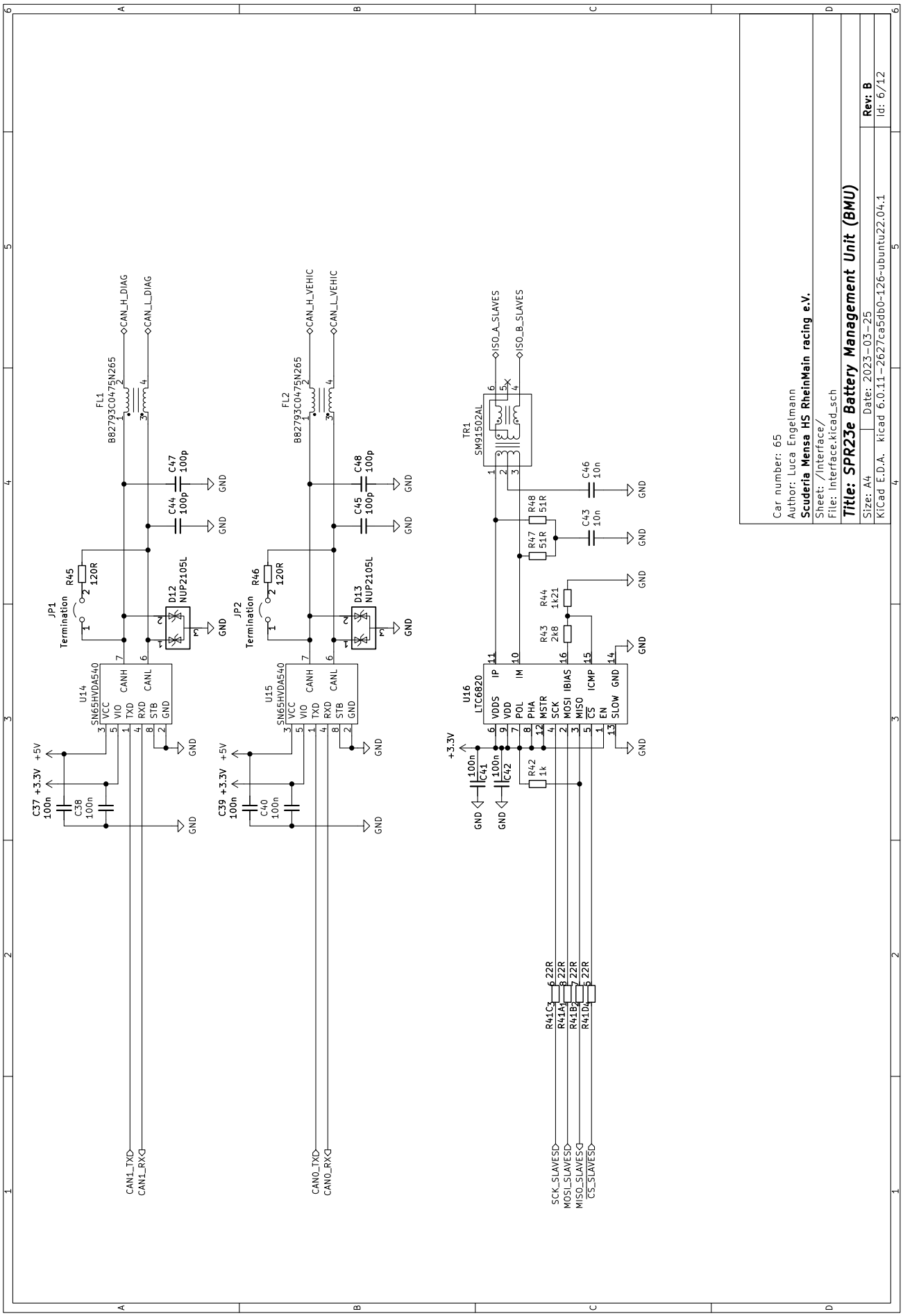
Title: SPR23e Battery Management Unit (BMU)
Size: A4
Date: 2023-03-25
Rev: B
KiCad E.D.A. kicad 6.0.11-2627ca5db0-126~ubuntu22.04.1
Id: 5/12
CS_CARD
MOSI_PERIPH
SCK_PERIPH
MISO_PERIPH
CARD_DETECT
CS_RTC
IRQ_RTC
CLKOUT_RTC
CS_EEPROM
SD_CS
SD_MOSI
SD_SCK
SD_MISO
RTC_INT
RTC_CS
RTC_MOSI
RTC_SCK
RTC_MISO
EE_SCK
EE_MOSI
EE_MISO
EE_CS
Molex 104031-0811
AT25M02-SSHM-T
RV-3149-C3
CR2032
+3.3V
GND


Car number: 65
Author: Luca Engelmann
Scuderia Mensa HS RheinMain racing e.V.
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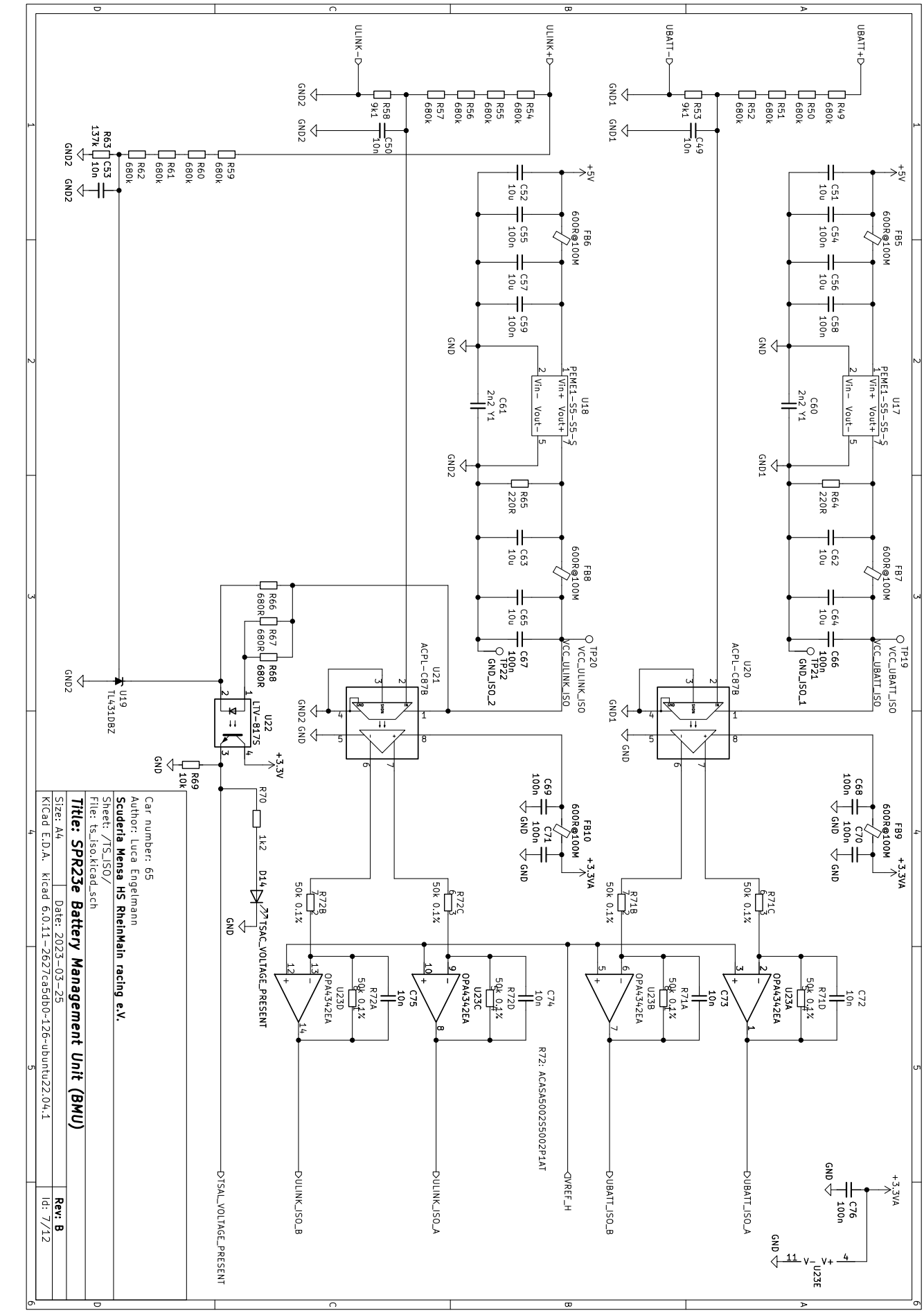
Title: SPR23e Battery Management Unit (BMU)
Size: A4
Date: 2023-03-25
Rev: B
KiCad E.D.A. kicad 6.0.11-2627ca5db0-126-ubuntu22.04.1
Id: 6/12
FL1
B82793C0475N265
FL2
B82793C0475N265
TR1
SM91502AL
U14
SN65HVDA540
U15
SN65HVDA540
U16
LTC6820
JP1
Termination
JP2
Termination
R45
120R
R46
120R
D12
NUP2105L
D13
NUP2105L
C37 100n
C38 100n
C39 100n
C40 100n
C41 100n
C42 100n
C43 10n
C44 100p
C45 100p
C46 10n
C47 100p
C48 100p
R41A 22R
R41B 22R
R41C 22R
R41D 22R
R42 1k
R43 2k8
R44 1k21
R47 51R
R48 51R
+5V
+3.3V
GND
CAN_H_DIAG
CAN_L_DIAG
CAN_H_VEHIC
CAN_L_VEHIC
ISO_A_SLAVES
ISO_B_SLAVES
CAN1_TXD
CAN1_RXD
CAN0_TXD
CAN0_RXD
SCK_SLAVES
MOSI_SLAVES
MISO_SLAVES
CS_SLAVES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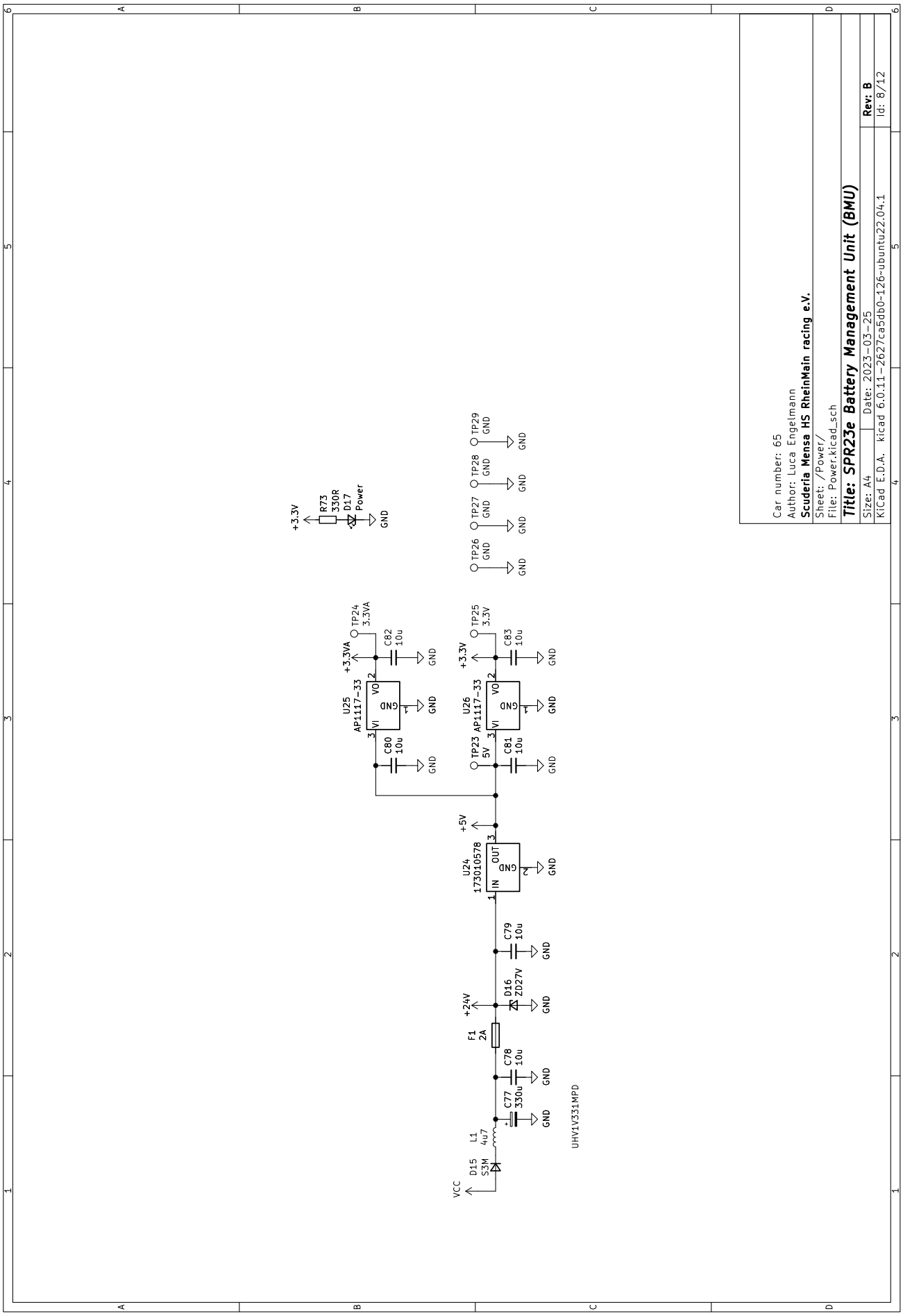
Author: Luca Engelmann
Scuderia Mensa HS RheinMain racing e.V.
Title: SPR23e Battery Management Unit (BMU)
Sheet: /TS_ISO/
File: ts_iso.kicad_sch
Size: A4
Date: 2023-03-25
KiCad E.D.A. kicad 6.0.11-2627ca5db0-126~ubuntu22.04.1
Rev: B
Id: 7/12


Car number: 65
Author: Luca Engelmann
Scuderia Mensa HS RheinMain racing e.V.
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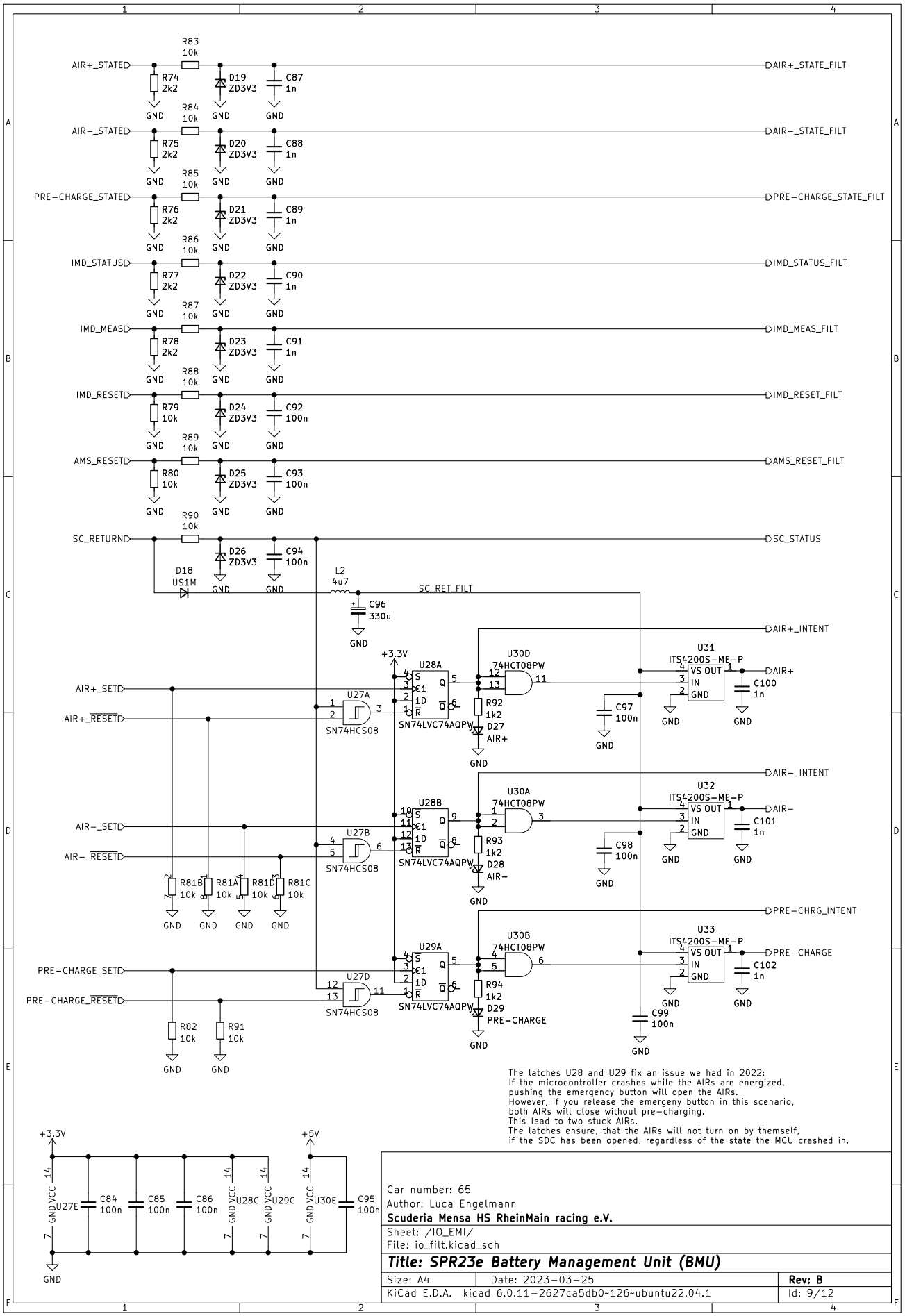
File: Power.kicad_sch
Title: SPR23e Battery Management Unit (BMU)
Size: A4
Date: 2023-03-25
Rev: B
KiCad E.D.A. kicad 6.0.11-2627ca5db0-126-ubuntu22.04.1
Id: 8/12
+3.3V
R73
330R
D17
Power
GND
TP29
TP28
TP27
TP26
TP24
3.3VA
TP25
3.3V
C82
10u
C83
C80
C81
U25
AP1117-33
U26
TP23
5V
+3.3VA
+5V
U24
173010578
C79
D16
ZD27V
+24V
F1
2A
C78
C77
330u
L1
4u7
D15
S3M
VCC
UHV1V331MPD



The latches U28 and U29 fix an issue we had in 2022:
If the microcontroller crashes while the AIRs are energized,
pushing the emergency button will open the AIRs.
However, if you release the emergeny button in this scenario,
both AIRs will close without pre−charging.
This lead to two stuck AIRs.
The latches ensure, that the AIRs will not turn on by themself,
if the SDC has been opened, regardless of the state the MCU crashed in.

Car number: 65
Author: Luca Engelmann
Scuderia Mensa HS RheinMain racing e.V.

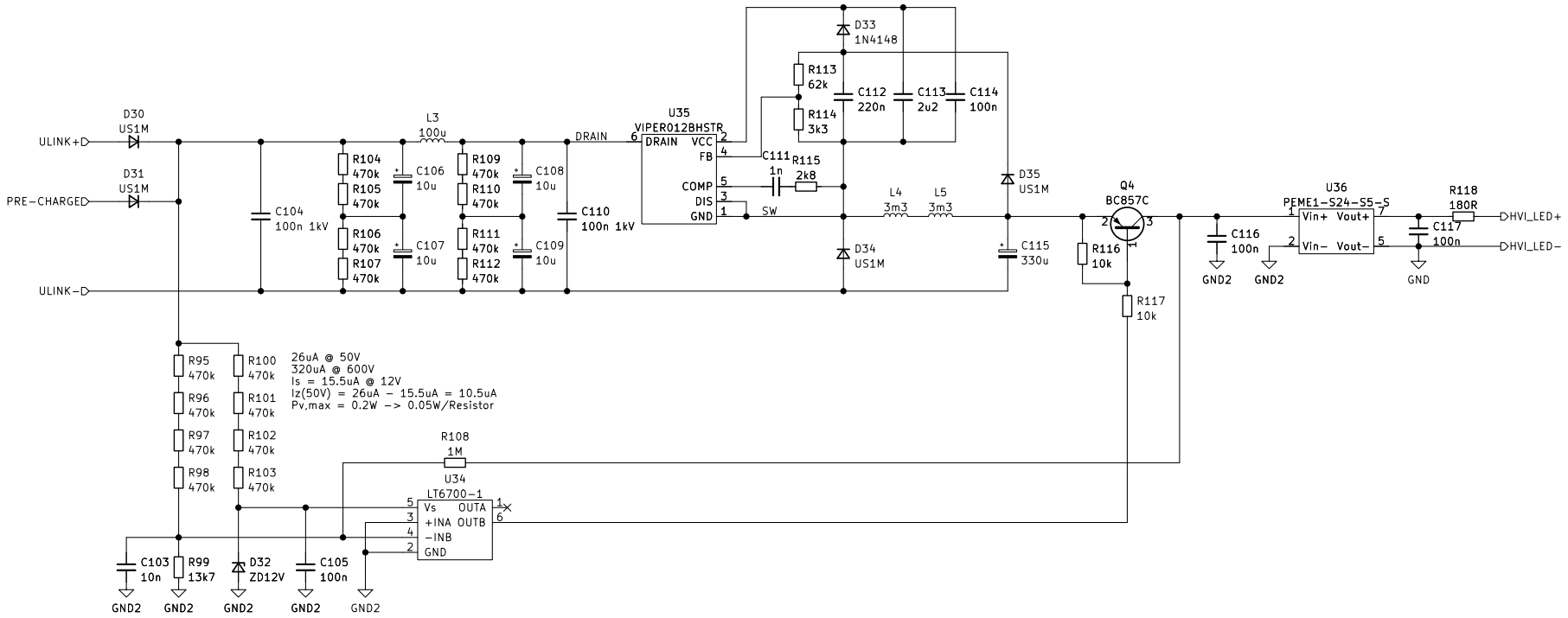
Sheet: /IO_EMI/
File: io_filt.kicad_sch

Title: SPR23e Battery Management Unit (BMU)

Size: A4	Date: 2023−03−25	**Rev: B**
KiCad E.D.A. kicad 6.0.11−2627ca5db0~126~ubuntu22.04.1		Id: 9/12

U35 is a regulated buck converter, which converts the TS voltage down to 24V.
It operates in a range of 50V to 600V and is not galvanically isolated.
Below 50V, the output is unstable and starts to pulse at a slow rate.
U36 is a galvanically isolated DCDC converter, which isolates the LED supply from the TS.
To ensure a hard on/off transistion of the LED at 50V,
U34 compares the input voltage to an internal reference.
It is powered from the TS, since it has to operate even if U35 is not regulating yet.
The circuit is powered from the TSAC output as well as from the node between pre-charge
relay and pre-charge resistor. Otherwise, the circuit would load the TS voltage down
during pre-cahrge, effectively preventing the pre-charge.

R108 adds some hysteresis, resulting in a turn-on threshold of 56V and a turn-off threshold of 40V



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Author: Luca Engelmann
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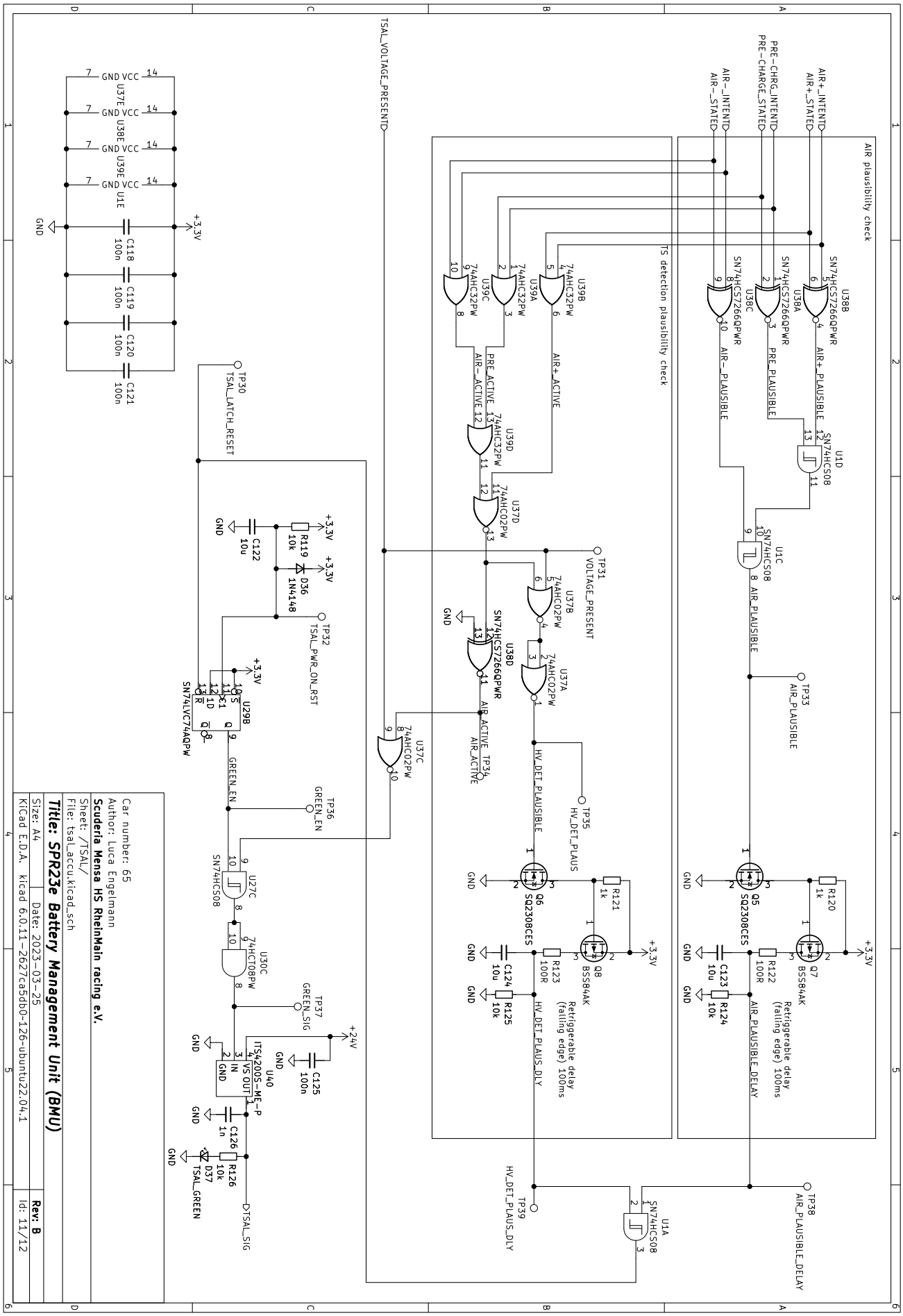
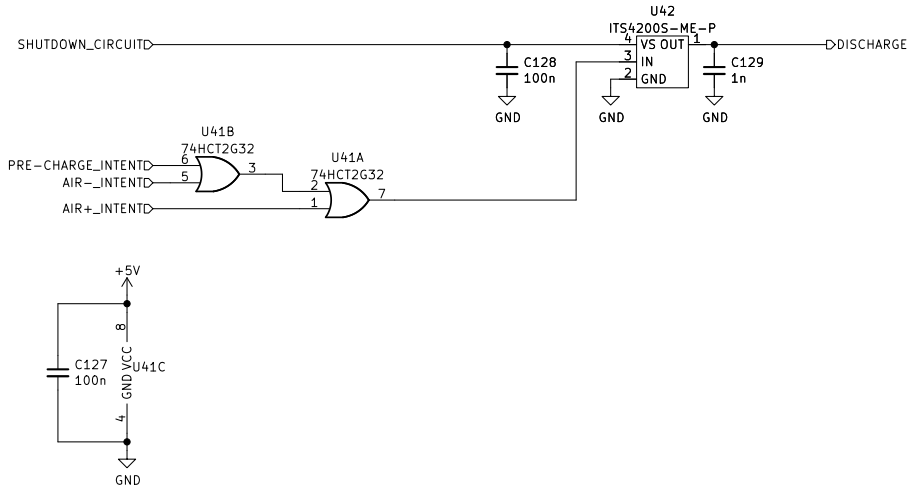
Sheet: /HVI/
File: voltage_indicator.kicad_sch

Title: SPR23e Battery Management Unit (BMU)

Size: A4	Date: 2023-03-25	**Rev: B**
KiCad E.D.A.	kicad 6.0.11-2627ca5db0~126~ubuntu22.04.1	Id: 10/12


AIR plausibility check
TS detection plausibility check
AIR+_INTENTD
AIR+_STATED
PRE-CHRG_INTENTD
PRE-CHARGE_STATED
AIR-_INTENTD
AIR-_STATED
TSAL_VOLTAGE_PRESENTD
U38B SN74HCS72660PWR
U38A
U38C
U39B 74AHC32PW
U39A
U39C
U39D
U37D 74AHC02PW
U37B
U37A
U38D SN74HCS72660PWR
U37C
U1D SN74HCS08
U1C
U1A
AIR+_PLAUSIBLE
PRE_PLAUSIBLE
AIR-_PLAUSIBLE
AIR+_ACTIVE
PRE_ACTIVE
AIR-_ACTIVE
AIR_ACTIVE
AIR_PLAUSIBLE
HV_DET_PLAUSIBLE
HV_DET_PLAUS_DLY
TP30 TSAL_LATCH_RESET
TP31 VOLTAGE_PRESENT
TP32 TSAL_PWR_ON_RST
TP33 AIR_PLAUSIBLE
TP34 AIR_ACTIVE
TP35 HV_DET_PLAUS
TP36 GREEN_EN
TP37 GREEN_SIG
TP38 AIR_PLAUSIBLE_DELAY
TP39 HV_DET_PLAUS_DLY
U29B SN74LVC74AQPW
U27C SN74HCS08
U30C 74HCT08PW
U40 ITS4200S-ME-P
D36 1N4148
D37 TSAL_GREEN
Q5 SQ2308CES
Q6 SQ2308CES
Q7 BSS84AK
Q8 BSS84AK
Retriggerable delay (falling edge) 100ms
AIR_PLAUSIBLE_DELAY
TSAL_SIG
U37E U38E U39E U1E
GND VCC
+3.3V
+24V
GND
C118 100n
C119 100n
C120 100n
C121 100n
C122 10u
C123 10u
C124 10u
C125 100n
C126 1n
R119 10k
R120 1k
R121 1k
R122 100R
R123 100R
R124 10k
R125 10k
R126 10k
Car number: 65
Author: Luca Engelmann
Scuderia Mensa HS RheinMain racing e.V.
Sheet: /TSAL/
File: tsal_accu.kicad_sch
Title: SPR23e Battery Management Unit (BMU)
Size: A4
Date: 2023-03-25
KiCad E.D.A. kicad 6.0.11-2627ca5db0-126~ubuntu22.04.1
Rev: B
Id: 11/12

The discharge circuit in the inverter is controlled by the shutdown circuit. To ensure that the discharge circuit is still enabled while the shutdown circuit is closed but TS is still off, the intentional states of the AIRs are used. The discharge circuit is disabled as soon as any of the AIRs is active but still re-activated if an AIR is stuck.



Car number: 65 Author: Luca Engelmann **Scuderia Mensa HS RheinMain racing e.V.**		
Sheet: /Discharge_Ctrl/ File: discharge.kicad_sch		
Title: SPR23e Battery Management Unit (BMU)		
Size: A4	Date: 2023-03-25	**Rev: B**
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