

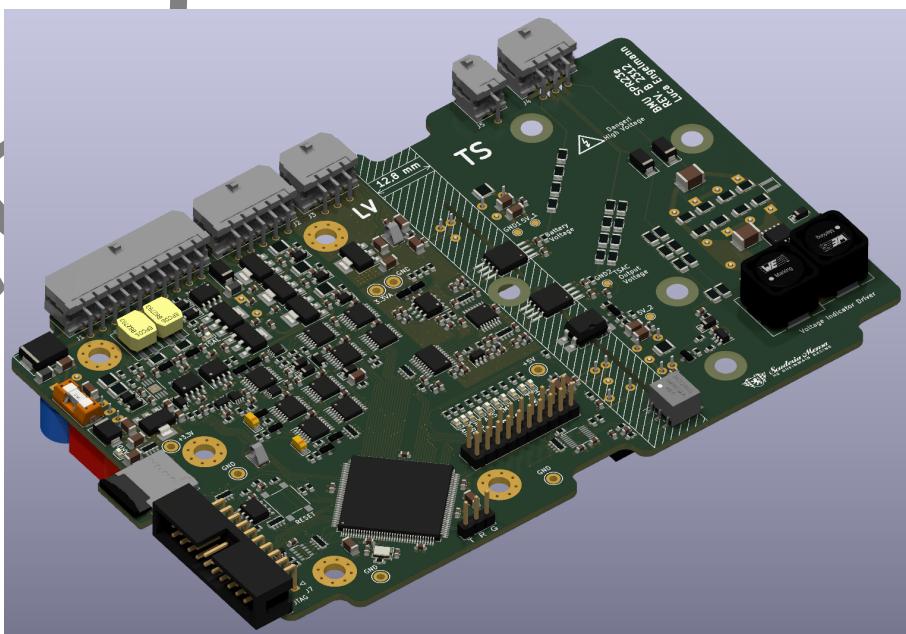
Sauderia Mensa

HS RHEIN MAIN RACING



Design Report

Battery Management System for SPR23e



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Season: 2023/2024



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Glossary

AIR Accumulator Isolation Relay

AMS Accumulator Management System (See BMS)

BMS Battery Management System

BMU Battery Management Unit

BOM Bill Of Material

CAN Controller Area Network

CSV Comma-separated Values

EMI Electromagnetic Interference

ESD Electrostatic Discharge

FSG Formula Student Germany

HIL Hardware In the Loop

IMD Insulation Monitoring Device

LED Light Emitting Diode

LVS Low Voltage System

MCU Microcontroller Unit

PCB Printed Circuit Board

TS Tractive System

TSAC Tractive System Accumulator Container

TSAL Tractive System Active Light

UART Universal Asynchronous Receiver Transmitter



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1. Introduction

1.1. Accumulator

Kurz auf den Akku eingehen; Zellen, Konfiguration und Rendering.

1.1.1. System Overview

Blockdiagramm mit Stacks, BMS Slave, AIRs und Sicherung, AIR-PCB mit pre-charge und abgesicherte Messabgriffe, Stromsensor, BMU, IMD

1.2. Requirements

1.2.1. General Requirements

The requirements are mostly based on the FSG rule set for 2023 [1]. Some general requirements for the vehicle integration apply also. These include

- Power supply from the low-voltage system (LVS) in a range from 18 V to 25 V, which is the unregulated voltage from the low-voltage accumulator.
- One CAN bus with a bitrate of 1 Mbit/s for the communication with the Vehicle Control Unit.
- One IsoSPI [2] interface for the communication with the BMS slaves on the accumulator stacks.
- Isolated voltage measurement for the accumulator and TSAC output voltage with an accuracy better than 1 % of the full measuring range.
- Isolated current measurement with a resolution better than ± 140 A, which is two times the fuse rating to allow for any short current peaks, and an accuracy better than 1 % of the full measuring range.

1.2.2. Rule Requirements

Since the BMU contains many different parts required by the rules, all of the following rules have to be fulfilled. For the TSAL logic in the accumulator these rules apply:

- EV 4.10.3 [p. 85][1] *The TSAL itself must have a green light, continuously on, active if and only if the LVS is active and ALL of the following conditions are true:*
 - All AIRs are opened.
 - The pre-charge relay, see EV 5.7.2, is opened.
 - The voltage at the vehicle side of the AIRs inside the TSAC does not exceed 60 V DC or 50 V AC RMS.



-
- EV 4.10.4 [p. 85][1] *The mentioned voltage detection must be performed inside the respective TS enclosure.*
 - EV 4.10.5 [p. 85][1] *The mentioned states of the relays (opened/closed) are the actual mechanical states. The mechanical state can differ from the intentional state, i.e. if a relay is stuck. Any circuitry detecting the mechanical state must meet EV 5.6.2.*
 - EV 4.10.6 [p. 85][1] *The voltage detection circuit of the red light and the relay state and voltage detection circuit of the green light must be independent. Any plausibility check between both lights is not allowed. A TSAL state with both lights simultaneously active might occur and must not be prevented.*
 - EV 4.10.9 [p. 85][1] *The TSAL and all needed circuitry must be hard-wired electronics. Software control is not permitted.*
 - EV 4.10.10 [p. 85][1] *A green indicator light in the cockpit that is easily visible even in bright sunlight and clearly marked with "TS off" must light up if TSAL green light is on, see EV 4.10.3.*
 - EV 4.10.11 [p. 86][1] *Signals influencing the TSAL and the indicator according to EV 4.10.10 are SCS, see T 11.9. The individual safe state of each of the TSAL lights is off. The TSAL has an active indication of the absence of failures (continuous green illumination) and thus the red light must not be illuminated for a visible check, see T 11.9.5.*
 - EV 4.10.13 [p. 86][1] *The TSAL's green light relay state detection circuit, see EV 4.10.3, does not need to detect an open circuit, as required by T 11.9, when the intentional state of the used (auxiliary) contact is opened. A plausibility check against the intentional relay state must be implemented in a way that the TSAL's green light stays off after the open circuit is detectable.*
 - EV 4.10.14 [p. 86][1] *The TSAL's green light voltage detection circuit, see EV 4.10.3, does not need to detect an open circuit, as required by T 11.9, when no voltage is present. A plausibility check against the intentional relay states must be implemented in a way that the TSAL's green light stays off after the open circuit of the accumulator voltage detection circuit is detectable.*
 - EV 4.10.14 [p. 86][1] *The latching required by EV 4.10.13 and EV 4.10.14 must not be triggered during normal operation conditions and must only be reset by power cycling the LVS.*

1.2.3. Additional Requirements

Firlefanz, der von der Regeln nicht gefordert wird, aber trotzdem drin ist

1.3. SPR21evo BMU

Kurz auf 21er BMU eingehen, Bild der Platine und Beschreibung der Key Features.

1.4. Comparing Legacy and Contemporary Solutions

Was kann die alte BMU anders als die neue? Welche Features kamen hinzu? Welche sind entfernt worden?
Was ist der Ausblick auf Software-Seite? Logging auf SD-Karte, EEPROM, 2 CAN-Busse



Auch auf AIR-PCB und Stromsensor eingehen



2. Potential Improvements

Mögliche Verbesserungen



3. BMU Hardware Design

3.1. Implementations

Umsetzung der Anforderungen in REV A und REV B beschreiben.

Für REV A wird nur auf den Schaltplan und einen Changelog im Anhang verwiesen. REV B wird im Detail beschrieben

The TSAL logic will be implemented in the following way:

- The actual states of the relays will be monitored using auxiliary contacts in the relays. They are mechanically linked to the main contacts as explained in the application note [3, p. 2]: “*The auxiliary contact actuating method will indicate the true position of the main contacts. The auxiliary contact actuation is directly coupled to the main contact moving bridge, and will not indicate “open” unless both contact gaps of the double-make, Form X contact are fully disconnected.*”
- The plausibility check to fulfill EV 4.10.5 is done against the intentional state indicated by the BMU. The following possible states can trigger the latch:
 - The intentional state is active, the actual state reports inactive: A line break in the state detection is to be assumed.
 - The intentional state is inactive, the actual state reports active: The relay is most probably stuck

Due to its mechanical construction, the relay takes 25 ms to switch from the opened to the closed position and 10 ms for the reverse [4, p. 2]. In these time periods, the relay states are implausible and must not trigger the latch, as EV 4.10.14 indicates.

- In order to fulfill EV 4.10.13, a line break in the state detection is detected by a plausibility check against the TSAC output voltage in the following way. In case the TSAC output voltage detection circuit detects a voltage greater than 60 V although all relays are open, these possibilities can occur:
 - The discharge circuit is still active after the relay opened. This is not a fault condition, since the discharge circuit takes about 2 seconds to discharge the TS below 60 V.
 - If the fault persists for more than 3 seconds than the discharge should have finished and it is to be expected that the relays are stuck and the state detection circuitry is broken.

Note that the permissible state during discharge must not lead to a detected fault. However, a delay of 3 seconds to detect the fault is permissible by the rule.

- Likewise, a line break in the voltage detection circuitry is detected using a plausibility check against the relay states. If the relays are closed and the voltage detection circuitry detects no voltage, a fault in the detection circuitry is to be assumed and must lead to the latched deactivation of the green light.
- Since the TSAL accumulator logic is located on the BMU PCB and all TS components needed to perform the checks are located inside the TSAC, EV 4.10.4 is fulfilled.



- The circuit will be build with logic gates without any software control. Therefore, EV 4.10.9 is fulfilled as well. The final circuit is discussed in full detail in section 3.3.4.

3.2. Hardware Block Diagram

Blockdiagramm der BMU Hardware

3.3. Schematic Explanation

The schematic is rather complex and would not fit on one page. It is divided into 11 logical modules, which are connected on the top-level schematic seen in Figure 3.1. Each module will be discussed in the following subsections. The full schematic is available in Appendix C.

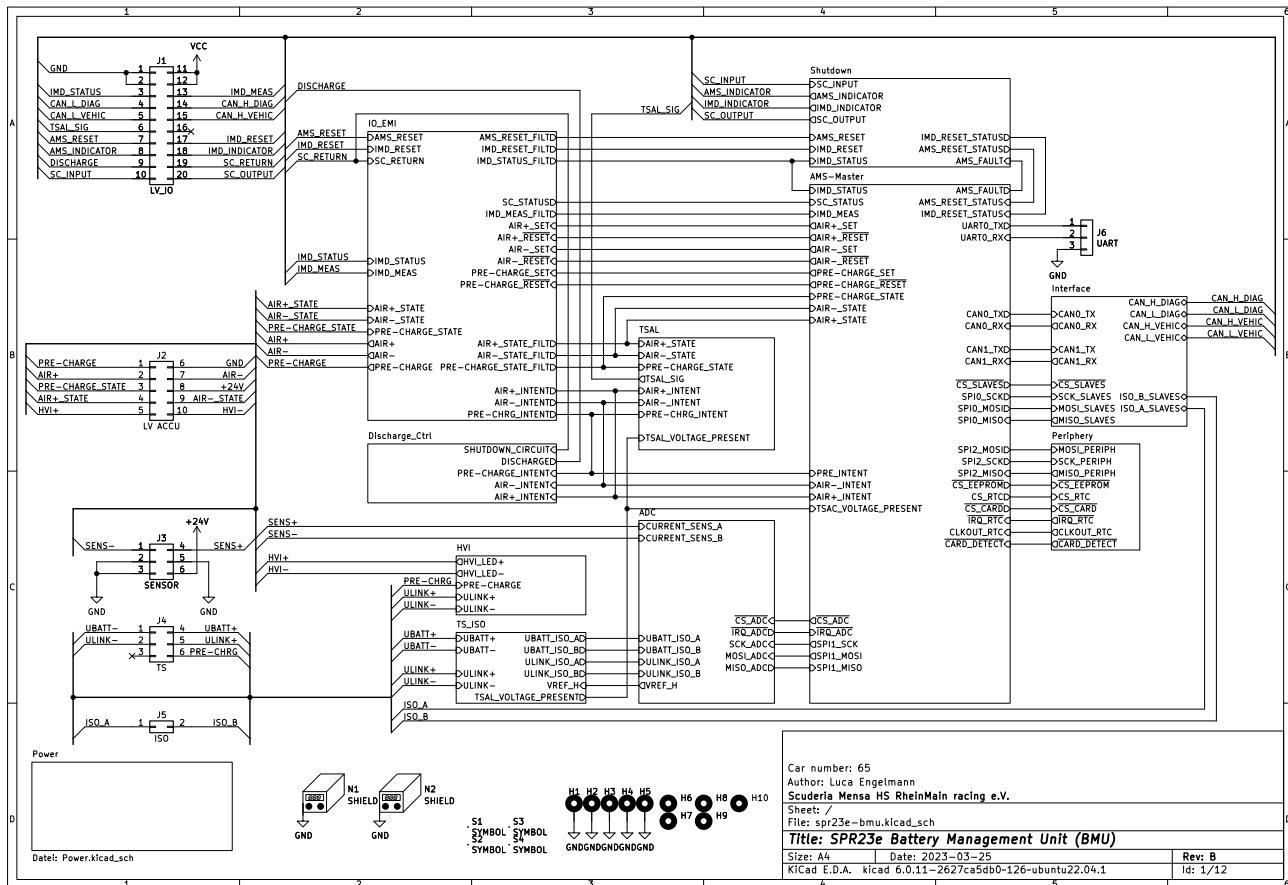


Figure 3.1.: Top-level BMU schematic.

3.3.1. Power Supply

The power supply schematic provides input protection and all necessary power rails for the BMU. The schematic for the power supply section is shown in Figure 3.2. At the input, L_1 , C_{77} , and C_{78} form a low-pass filter to filter out any high-frequency noise which might be on the low-voltage system. D_{16} is used



in conjunction with F_1 to protect the BMU against over-voltages. D_{15} not only protects the BMU from reverse-polarity, but it also isolates the BMU supply from the low-voltage system. A high-current spike will not drain C_{78} , leading to a stable power supply of the BMU in case of voltage dips caused by switching of the cooling fans or pumps. The 18 V to 25 V provided by the LVS is stepped-down to 5 V using an integrated DC to DC converter. Two low-dropout regulators U_{25} and U_{26} generate the main 3.3 V digital voltage rail used by the microcontroller and the other digital circuits and a secondary 3.3 V voltage rail used by the analog circuits. The use of two independent regulators for analog and digital circuits prevents noise coupling from the digital to the analog circuit. A power LED signalizes that the BMU is powered. Test points for all voltage rails are provided for easy measurement on the PCB.

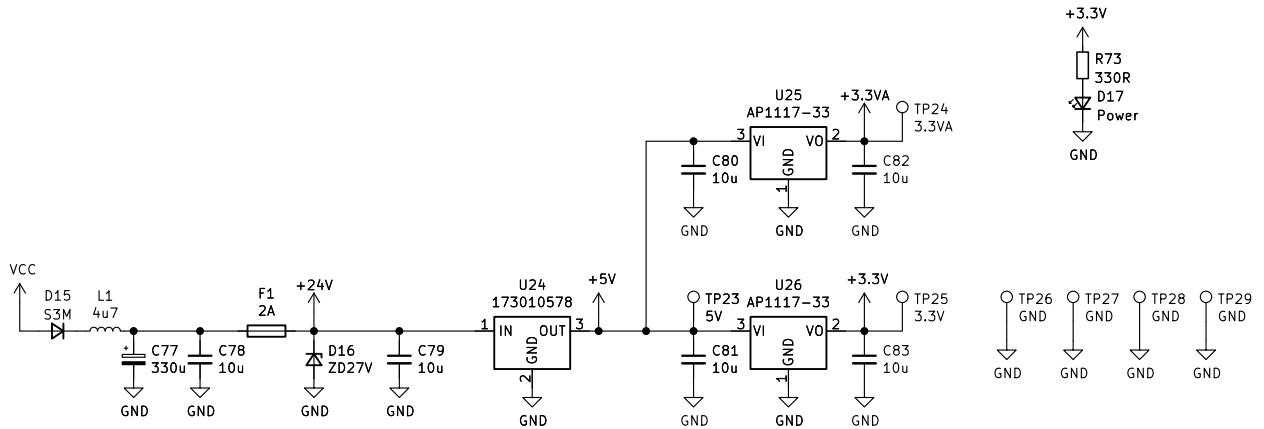


Figure 3.2.: Schematic of the power supply section.

3.3.2. I/O

This section of the schematic conditions the input signals for the BMU logic and drives the AIRs. It can be seen in Figure 3.3. Since the digital section operates at 3.3 V and the signals outside the BMU operate at LVS levels, zener diodes are used to limit the voltages. Each signal has a pull-down resistor to ensure stable logic levels in case of unconnected inputs. The 2.2 k Ω resistors at the inputs for the state detection of each relay ensure the minimum wetting current needed for the LEV100 relays: "*Minimum Aux Contact Load 10mA/12Vdc*" [4, p. 3]. Likewise, the pull-down resistors R_{77} and R_{78} for the IMD are the recommended values from the datasheet [5, p. 5]. Note that these resistors have to dissipate some power at the maximum voltage of the LVS: $P_{d,pull-down} = \frac{(25\text{ V})^2}{2.2\text{ k}\Omega} = 0.28\text{ W}$. Therefore, resistors in a 1210 package are used, since they are rated for 0.5 W of power [6]. The capacitors form in combination with the zener diode dropper resistors a low-pass filter used to filter out any noise which might be picked up by the signal wires. The status of the shutdown circuit is also evaluated by the BMU. The same input protection circuit is used to measure the voltage of it. The relays are directly supplied from the shutdown circuit. L_2 and C_{96} form low-pass filter, which limits the current spike caused by the switching of the relays. D_{18} is important to separate the high-current path from the detection path. Imagine that the AIRs are not energized and the shutdown circuit is active. Now, one emergency button is pressed. The shutdown circuit is turned off but C_{96} is still charged. Without D_{18} , it would lead to a false reading of the SC_STATUS signal until the capacitor is discharged. With D_{18} , C_{96} is blocked from holding up the voltage at the SC_RETURN node in this scenario. This ensures, that the microcontroller and the latches U_{28A} , U_{28B} , and U_{29A} detect a power-loss in the shutdown circuit without any noticeably delay.

The AIRs are controlled by ITS4200 high-side switches [7] which are supplied by the shutdown circuit. This is required by EV 6.1.1 [1]. U_{30} is used as level shifters to drive the high-side switches. This step



is needed, since the ITS4200 is advertised with a "*CMOS compatible input*" [7, p. 2] and has an input voltage turn-on threshold of 3.0 V [7, Table 4]. Its input is driven with 5 volt instead of 3.3 V to avoid potential problems. The inputs of the 74HCT logic series recognize a logical high signal at and above 2.0 V. The ITS4200 is internally protected against short-circuits and voltage backfeed, making it an ideal output driver for the BMU. The relays are not directly controlled by the BMU. Instead, flip-flops isolate the control from the microcontroller to the outputs. The MCU can set and clear the flip-flops. Additionally, the flip-flops can be cleared by the shutdown circuit signal. This has the advantage that the relays are not only de-energized by the loss of power but also the turn-on request is cleared in hardware. In the BMU for the SPR21e, this was solely done in software. Now imagine that the flip-flops were omitted and the microcontroller crashes as soon as the AIRs are energized. If the emergency switch is pushed, the AIRs will de-energize. However, since the crashed microcontroller still requests the positive and negative AIRs to be energized, re-activation of the emergency switch results in an uncontrolled re-activation of the tractive system without pre-charging. Due to the large current spike, both the positive and negative AIR will be most likely stuck after this event. This has happened in the early testing phase of the SPR21e. With the hardware flip-flops, it doesn't matter if the microcontroller crashes while the AIRs are energized. The flip-flops will only react on the rising-edge of the SET-signals and will be cleared, as soon as the shutdown circuit opens. The intentional states of the relays are taken from the outputs of the flip-flops. Notice that the flip-flops are reset-dominant, meaning that they cannot be set if the clear input is set to a logical zero.

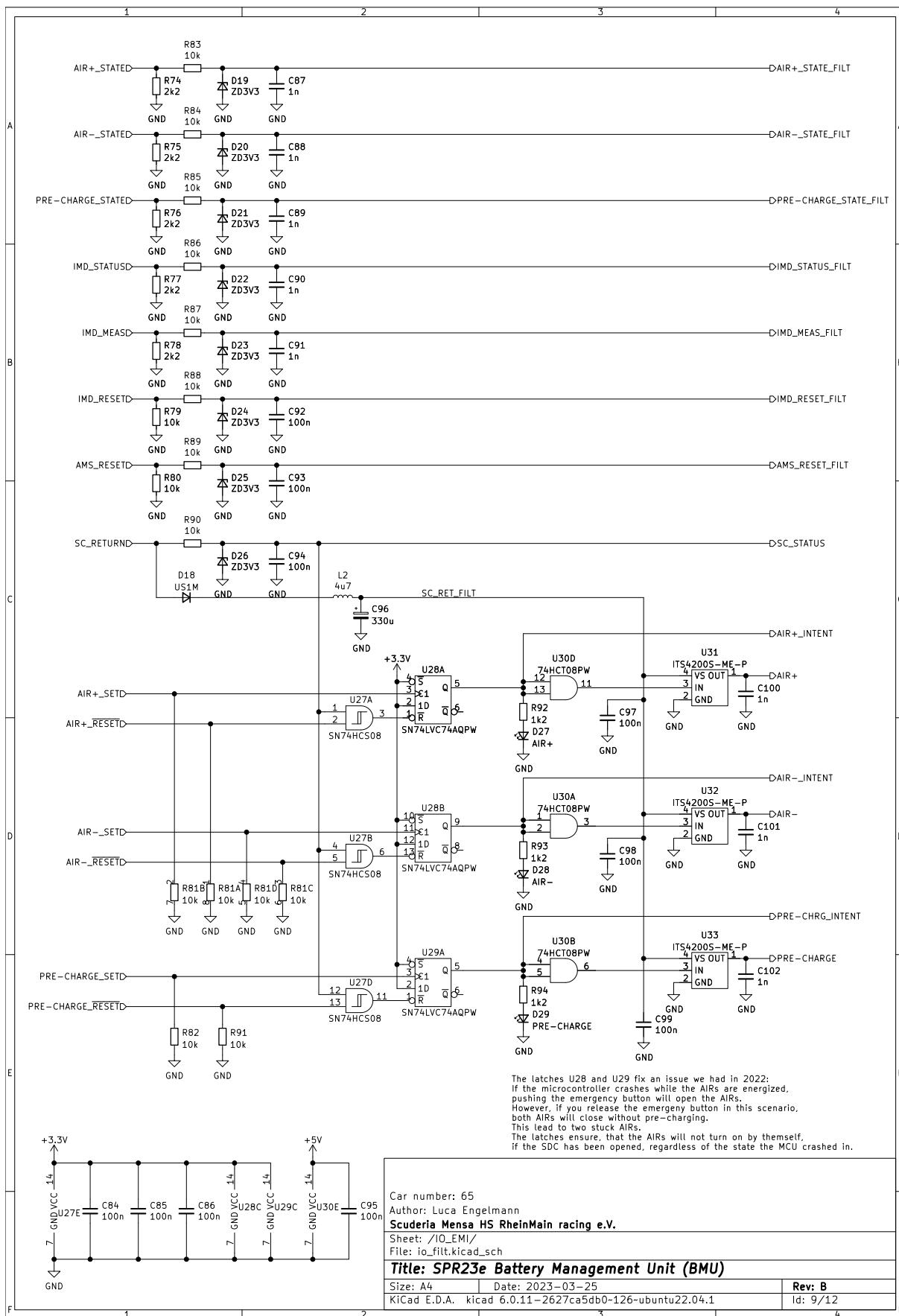


Figure 3.3.: Schematic of the I/O section.



3.3.3. Discharge Control

The discharge circuit is located in the inverter and discharges the DC-Link capacitors within 2 s. Without this circuit, it would take about 30 min for the DC-Link voltage to fall below 60 V. EV 6.1.5 requires the DC-Link voltage to fall within five seconds [1, p. 92]. The discharge circuit is normally active and controlled by the shutdown circuit, as required by EV 4.9.2 [1, p. 84]. If it would be controlled by the shutdown circuit only, it would be de-activated as soon as the shutdown circuit is closed. To add some extra safety, in this design the discharge circuit is controlled by the shutdown circuit and the intentional state of the relays. This ensures, that the discharge circuit is only deactivated if the activation of the tractive system is requested. To ensure that the discharge circuit remains active if the relays are stuck, only the intentional states are used. The discharge is designed to constantly handle the voltage in this scenario, as required by EV 4.9.1 [1, p. 84]. The schematic is shown in Figure 3.4.

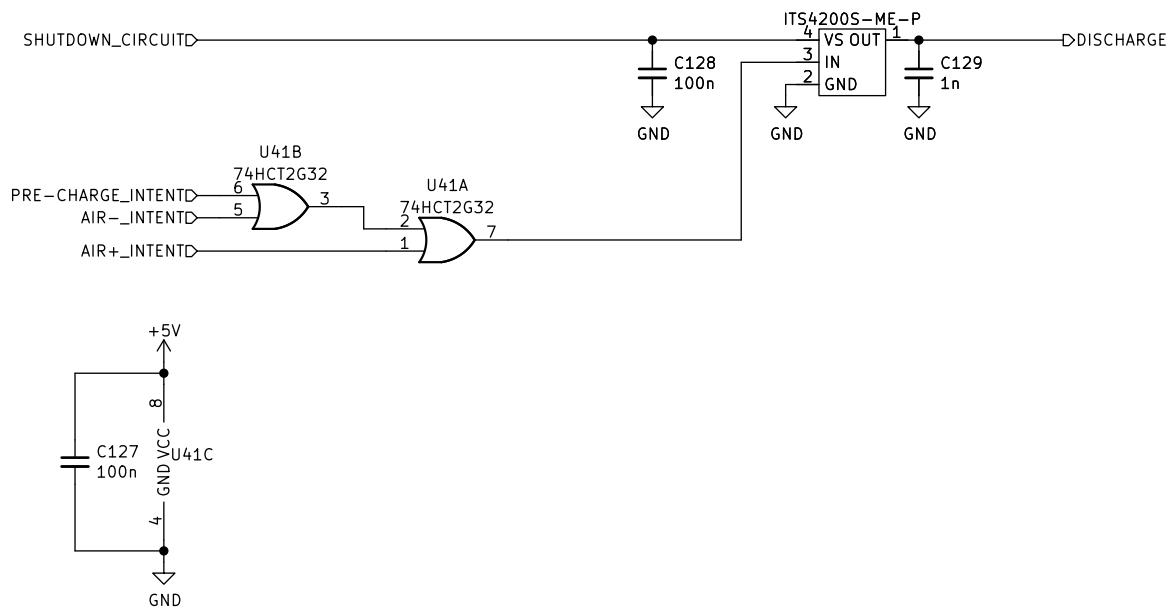


Figure 3.4.: Schematic of the discharge control section.

3.3.4. TSAL

The TSAL schematic can be divided into three logical sections. The top section checks the three AIRs for plausible states. The second section checks the TS detection circuit for plausibility. The third section controls the green light and contains the required latch. Figure 3.5 shows the schematic of the TSAL logic.

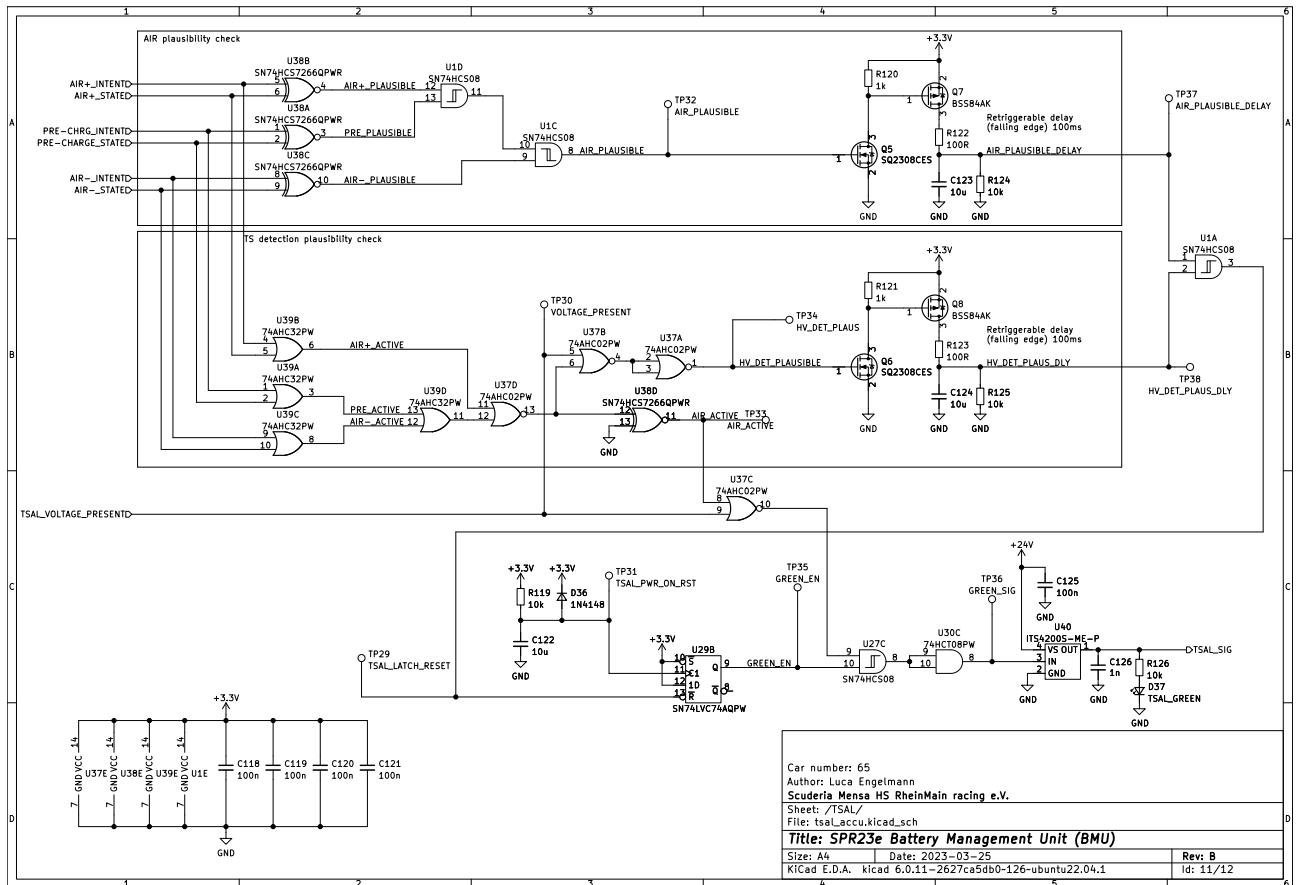


Figure 3.5.: Schematic of the TSAL accumulator logic.

The logic evaluates if the current state is plausible. A plausible state is always reached when the TSAC output voltage matches the relay state and if the actual relay state matches the intentional state. The truth table for the AIR plausibility check for each AIR is shown in Table 3.1. The resulting boolean function corresponds to an exclusive NOR gate (U_{38} in Figure 3.5).

Table 3.1.: Truth table for the plausibility check for each AIR.

AIR intentional	AIR actual	plausible	Comment
inactive	inactive	yes	No error
inactive	active	no	AIR stuck
active	inactive	no	State detection or coil wire broken
active	active	yes	No error

The AND gate U_1 (Figure 3.5) combines the plausibility of all AIRs to one signal AIR_PLAUSIBLE, which is low as soon as one of the AIRs is implausible and high if all AIRs are plausible. A retriggerable delay circuit accommodates for the mechanical switching time of the AIRs. It delays the falling edge only and passes the rising edge through without any delay. The delay time is set by the time constant of C_{123} and R_{124} (Figure 3.5) and the input threshold of the following AND gate (U_1 , Figure 3.5). The following gate needs to have Schmitt trigger inputs due to the slow falling edge caused by the delay. The input thresholds have a large tolerance and are not specified for a supply voltage of 3.3 V [8, Section 6.5]. The interpolated values for the negative threshold are $0.61 \text{ V} < U_{T-} < 1.22 \text{ V}$. At the maximum lower input threshold, the delay time is minimal and corresponds to the RC time constant τ . The circuit ensures a minimum delay time of 100 ms. At the minimum lower input voltage threshold, the delay time will increase to 170 ms.



The plausibility check for the TSAC output voltage detection uses both the intentional and the actual AIR states for comparison. U_{37} and U_{39} combine the six signals to one signal. If any of the AIRs is active (either intentional or unintentional) the signal AIR_ACTIVE will be high. The complex appearing connection of U_{37} and U_{38D} results in an efficient utilization of the four independent gates within a package. U_{38D} is configured to behave like an inverter. The signal HV_DET_PLAUSIBLE is a combination of the TSAC output voltage detection and the AIR state with the truth table shown below. The corresponding boolean function is an OR gate with one inverted input.

Table 3.2.: Truth table for the TSAC output voltage plausibility check.

Voltage present	AIR active	plausible	Comment
no	no	yes	No error
no	yes	no	Voltage detection broken wire
yes	no	yes	See text
yes	yes	yes	No error

A voltage greater than 60 V present at the TSAC output while no AIR is active is not considered as implausible since this happens on every discharge cycle. In this case, the green and the red LED of the TSAL will be active. This edge case is allowed by rule EV 4.10.6 and is thus not prevented. The HV_DET_PLAUSIBLE signal uses an identical retriggerable delay circuit. In this case, it is used to accommodate for the sum of the pre-charge time and the relay turn-on time. During pre-charge, the TSAC output voltage will rise depending on the time constant of the pre-charge resistor and the DC-Link capacitor. In order to detect a broken wire in the voltage detection circuitry, the plausibility check waits for the DC-Link voltage to rise above 60 V. This ensures that the broken wire is detected if the implausibility persists after the pre-charge time and pre-charging will not lead to a false triggering. The time it takes for the DC-Link voltage to rise above 60 V can be calculated with the basic capacitor charging formula shown in Equation 3.1.

$$U_c(t) = U_0 \cdot (1 - e^{-\frac{t}{\tau}}) \quad (3.1)$$

Re-arranging Equation 3.1 to solve for t is shown in Equation 3.2. The maximum t will be at the minimum battery voltage of 430 V. Solving for $U_c(t) = 60$ V, $U_0 = 430$ V, $\tau = RC = 1000 \Omega \cdot 300 \mu F$, Equation 3.2 yields:

$$t_{pre} = -\tau \cdot \ln \left(1 - \frac{U_c(t)}{U_0} \right) = -(1 \text{ k}\Omega \cdot 300 \mu F) \ln \left(1 - \frac{60}{430} \right) = 45 \text{ ms} \quad (3.2)$$

The turn-on time of the relays add to the pre-charge time. The resulting total pre-charge time $t_{pre,sum}$ equals:

$$t_{pre,sum} = t_{on,relay} + t_{pre} = 25 \text{ ms} + 45 \text{ ms} = 70 \text{ ms} \quad (3.3)$$

Therefore, a delay of 100 ms is sufficient as well.

The last section of the TSAL logic combines the plausibility check, the voltage detection signal, and the AIR_ACTIVE signal to control the green light of the TSAL. The flip-flop U_{29B} is the latch required by EV 4.10.13 and EV 4.10.14. It is set on startup after a short delay, to ensure that all signals which clear the latch are stable. If the AIRs or the voltage detection are implausible, the latch is cleared. The output of the latch is used as enable signal for the green light. Therefore, the green light can only be activated,



if the whole system is in a plausible state. The green light is then controlled by the AIR_ACTIVE and TSAL_VOLTAGE_PRESENT signal in a way that either of these signals turn off the green light. This ensures that the green light is deactivated as soon as at least one AIR is active and reactivated only if the voltage at the TSAC output is less than 60 V and all AIRs are off. The signal output uses the same method as described in subsection 3.3.2. The signal produced by U_{40} is sent to the TSAL logic in the inverter, where it is routed to the TSAL lights.

3.3.5. Shutdown Circuit Control

The IMD and AMS must open the shutdown circuit in case of faults or critical values. EV 6.1.6 [1, p. 94] requires a non-programmable latch for this action. Figure 3.6 shows the schematic of the shutdown circuit latches. Once latched, they must only be manually reset as EV 6.1.6 requires [1, p. 93]. The latches will start in the cleared state on power-up. To avoid resetting the latches manually on power-up, an auto-reset circuit based on U_{1B} , U_2 , and the surrounding components will clear the latches automatically after 3 s. U_5 is reset-dominant as well. Therefore, the automatic reset will only work, if the IMD and AMS do not report any faults by pulling the IMD_STATUS or AMSFAULT signals low. During the 3 s auto-reset, the manual reset buttons are disabled to allow for a self-check of the indicator LEDs required by T 11.9.5 [1, p. 59]. U_2 is needed to convert the inhibit-signal to a short pulse, which will set the latch. If the signal would be constantly active, the manual reset buttons could not be used anymore to set the latches, since the clock inputs of the latches are edge triggered. The indicator LEDs are driven by U_6 , which is a gate driver. Although not specifically designed to drive LEDs, it is a cheap and small solution which works flawlessly. The power stage for the shutdown circuit is comprised by Q_2 and the surrounding components. D_2 and D_3 limit the gate-source voltage of the mosfets to safe values. Q_1 and Q_3 are used to control the power stage mosfets. The power stages are active, if the Q outputs of U_5 are active. The negated outputs of U_5 are used to drive the indicator LEDs and to feed the current state of the latches to the microcontroller.

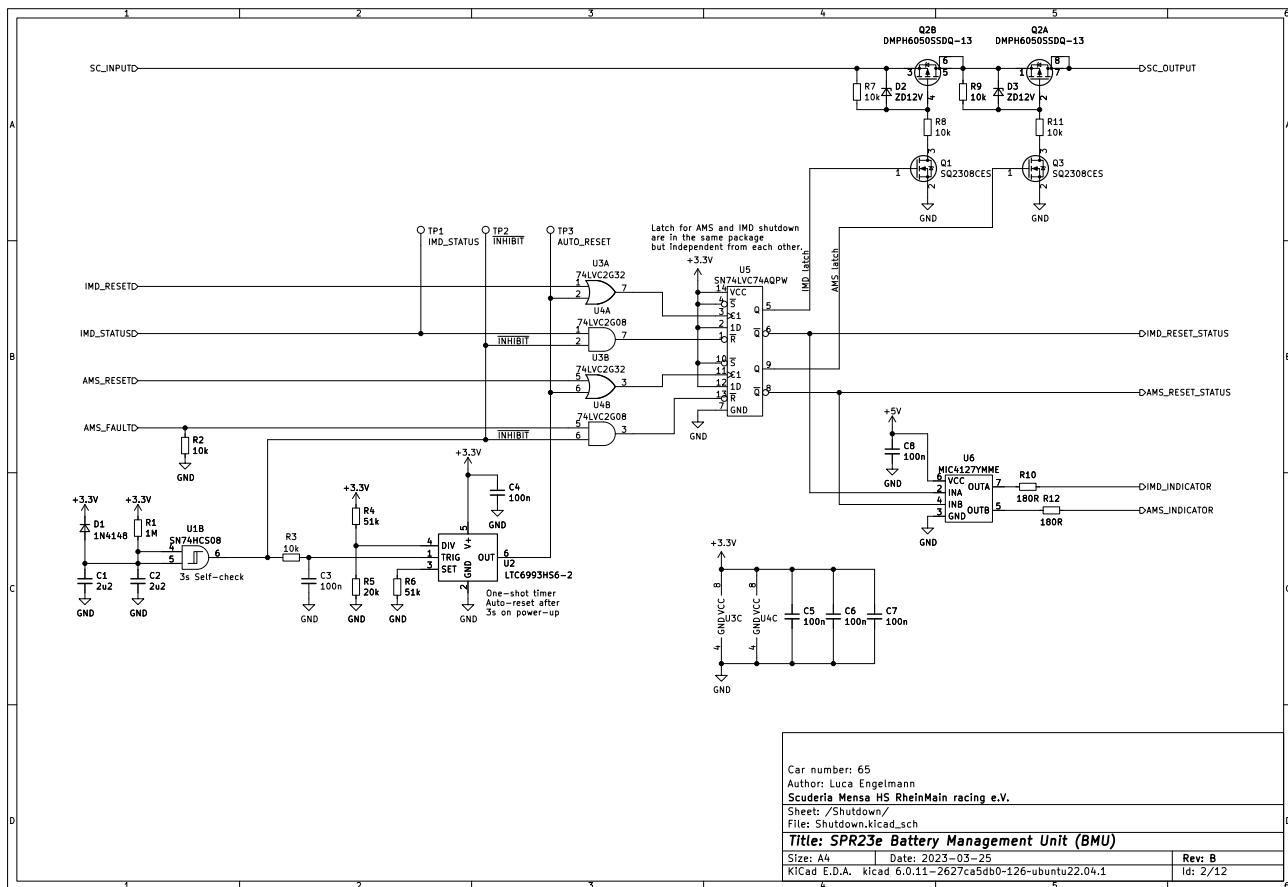


Figure 3.6.: Schematic of the shutdown circuit control.



4. Battery Disconnect Unit

Hier auf AIR-PCB und Stromsensor eingehen und die Platzierung der Komponenten in der BDU; Rendering

4.1. AIR PCB

Schaltplan und Beschreibung der Funktion, Rendering

4.2. Current Sensor

Schaltplan, Beschreibung der Komponenten, Berechnung der Genauigkeit und Rendering



5. Software Architecture

Softwarearchitektur erläutern

5.1. <Software Modul>

Softwaremodule erläutern



6. Test and Validation

6.1. Test Setup

Testaufbau erklären

6.2. TSAL Test

The TSAL accumulator logic has been simulated with LTSpice before putting it onto the PCB. The simulation tests all possible error conditions, including stuck relays, broken relay state detections and a line break in the voltage detection. The simulation results have been checked against the real behavior using a Hardware-in-the-loop (HIL) test procedure. A S32K144-Q100 evaluation board [9] is connected via CAN to the BMU and controls the relays in the test setup based on the commands sent by the BMU. It also feeds back the current state of the TSAL signal. The BMU runs a modified firmware which contains the test procedures. These tests can be initiated via the UART interface. During the test, the BMU will output all necessary values in CSV format over the UART interface in 50 ms time intervals. The BMU firmware uses the measured DC-Link and battery voltages to perform the pre-charge. The simulation performs the pre-charge using a constant timing for the relays. Stuck relays may lead to different pre-charge times than usual. The simulation will not account for that fact. However, it does not influence the behavior of the TSAL logic. Furthermore, the slow appearing rise and fall times in the test results are an artifact from the 50 ms time slices. They do not represent the real rise and fall times. Another artifact from the same source are shifted edges by ± 50 ms. The following pages show the simulation result on the left side and the real behavior on the right side in the following order:

1. No error
2. Positive AIR stuck
3. Pre-charge relay stuck
4. Negative AIR stuck
5. Voltage detection broken wire
6. Positive AIR state detection broken wire
7. Pre-charge relay state detection broken wire
8. Negative AIR state detection broken wire

The graphs in each plot represent the logic signals at the most important points in the circuit. The upper most plot shows the output of the TSAL logic, which controls the green light. The second graph shows the voltage detection with a logical high at 3.3 V representing a detected voltage > 60 V. The relay intent and state plots are self explanatory. They represent the intentional and actual state of the relay with a logical high representing an active state. The last plot shows the DC-Link voltage measured by the BMU. The simulation uses the accumulator voltage of 600 V while the HIL test uses 24 V. The plots of the HIL tests use 0 and 1 to denote the logical states.



Test 1: No error

In this test, the BMU performs a pre-charge and a discharge cycle. The TSAL green light shall turn off, as soon as at least one AIR is closed or the voltage across the DC-Capacitor is greater than 2.5 V and shall turn back on, if all AIRs are open and the DC-Link voltage is less than 2.5 V. The 24 V/2.5 V ratio between the battery voltage in the test setup and the TS detection threshold is approximately the same as in the real setup with a ratio of 600 V/60 V. As seen in Figure 6.2, the TSAL logic behaves exactly as simulated. The test would not be passed, if the LED would not turn off at the 1 s mark or would remain off at the 4.4 s mark.

Test 2: Positive AIR stuck

This test simulates a stuck positive AIR. The AIR+ state is therefore always high. During pre-charging, the negative AIR closes. Therefore, the pre-charge resistor is bridged in this scenario. Notice that the simulation uses a simple time-controlled pre-charging while the real BMU performs the pre-charging based on the DC-Link and battery voltage. This explains the short on-time of the pre-charge relay compared to the simulation due to the fast rise time of the DC-Link voltage. Notice also, that the BMU with the final firmware would not allow to close any relay if one of the relay is stuck. Both the simulation in Figure 6.3 and the HIL test in Figure 6.4 show, that the TSAL green light never turns on, as required.

Test 3: Pre-charge relay stuck

A stuck pre-charge relay does not directly lead to malfunction of the pre-charge sequence or the general function of the tractive system. However, it would violate EV 5.6.2 [1, p. 90]. A stuck pre-charge relay is detected correctly as Figure 6.5 and Figure 6.6 show. The TSAL's green light does not turn on at all.

Test 4: Negative AIR stuck

Similarly to test 3, a stuck negative AIR causes no direct malfunction of the system but it will also violate EV 5.6.2 [1, p. 90]. This fault is correctly detected as well, as seen in Figure 6.7 and Figure 6.8.

Test 5: Voltage detection broken wire

A broken wire or blown fuse in the voltage detection circuit is simulated in this test. Since the voltage detection circuit and the TSAC output voltage measurement share the same wire and fuse, the DC-Link voltage and the voltage detection in both the simulation and the real hardware read always zero. Additionally, since the simulation does not use the DC-Link voltage to perform the pre-charge, the relay sequence looks identical to any other test (Figure 6.9). The BMU will remain in the pre-charge state since the DC-Link voltage does not reach 95 % of the battery voltage, causing the positive AIR to never energize (Figure 6.10). It is apparent that as soon as the negative AIR and the pre-charge relay turn on, the green light turns off and remains off, after both relays de-energize again.



Tests 6, 7, and 8: Relay state detection broken

Due to their similarities, the last three tests are summarized here. As seen in Figure 6.12, Figure 6.14, and Figure 6.16, the state detection of the positive AIR, pre-charge relay, and negative AIR read constantly zero. This fault is detectable, as soon as the corresponding relay is energized. The green light turns off, as soon as the AIRs are energized and remains off after the relays de-energize due to the fault latching.

TSAL Test: Summary

In summary, the tests show that the TSAL accumulator logic recognizes all possible faults correctly and behaves rule compliant. While these tests seem extremely elaborate and time-consuming, it is important to fully validate the functionality of the TSAL logic, since it is a safety-critical part that must behave under all circumstances as expected.

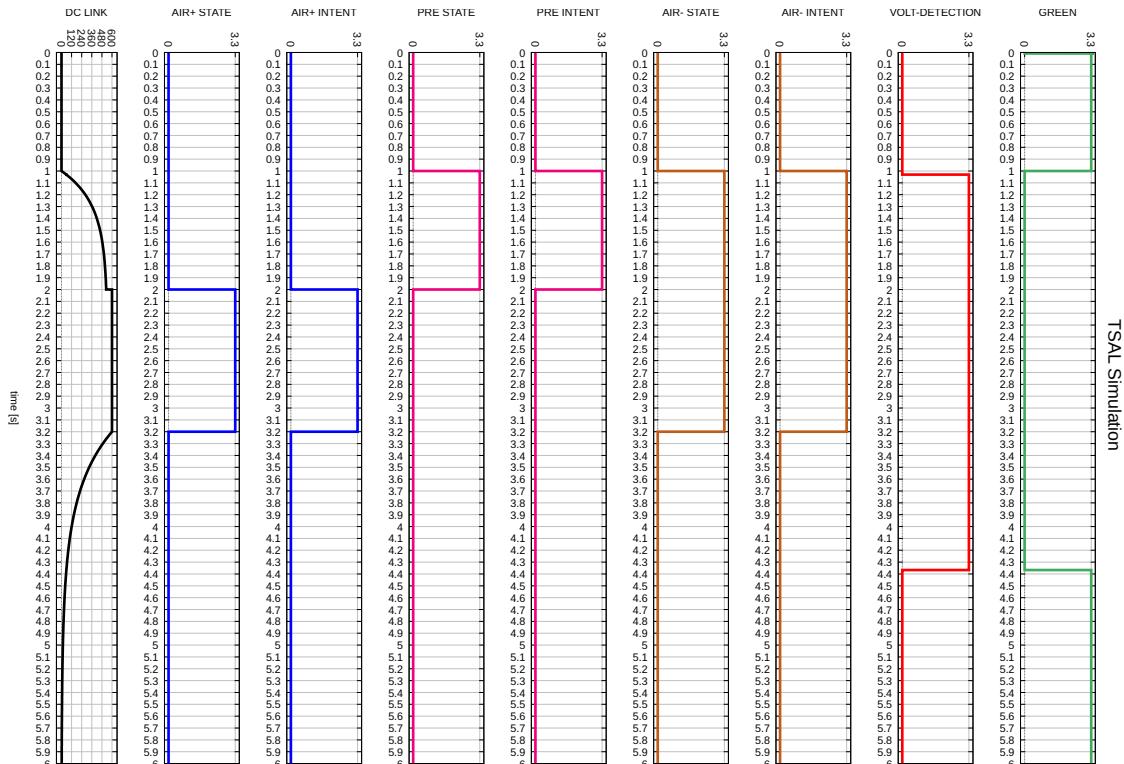


Figure 6.1.: TSAL simulation result. Test: No errors.

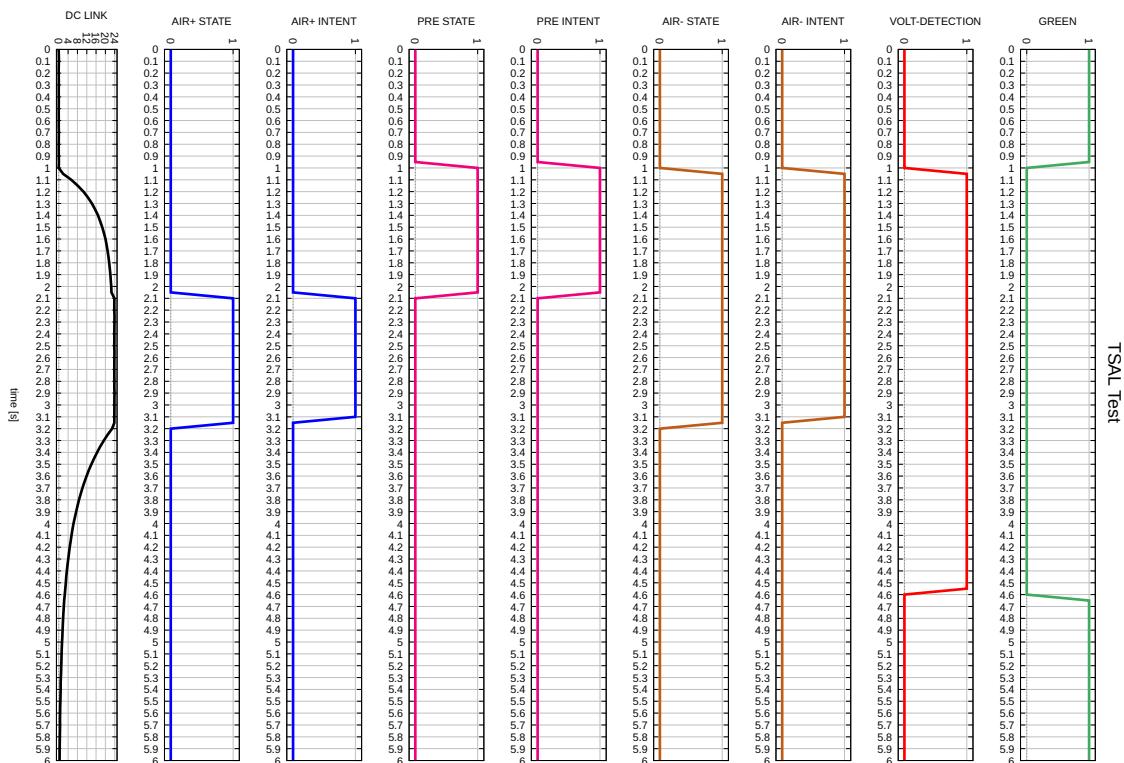


Figure 6.2.: TSAL HIL result. Test: No errors.

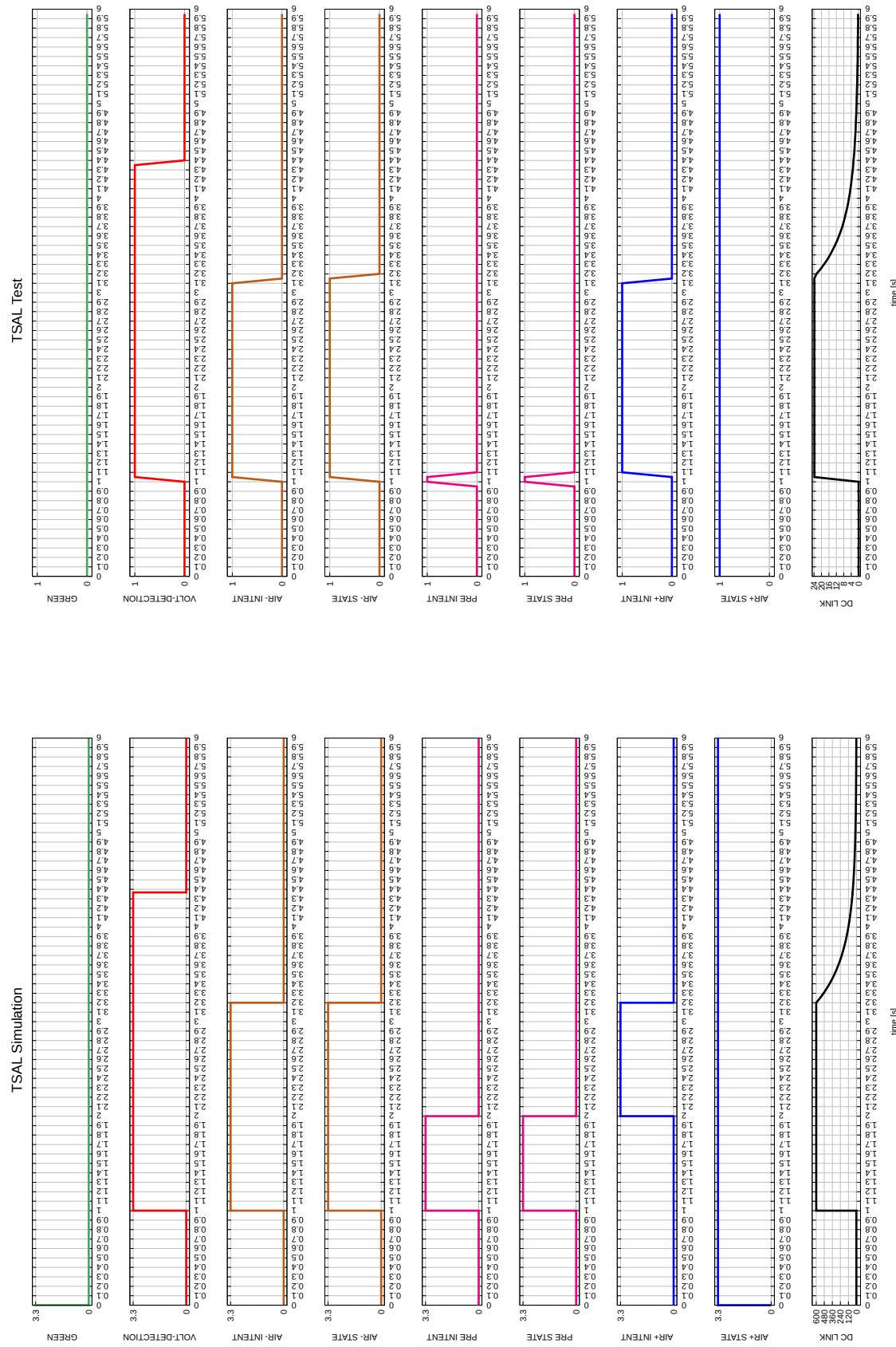


Figure 6.3.: TSAL simulation result. Test: Positive AIR stuck.

Figure 6.4.: TSAL HIL result. Test: Positive AIR stuck.

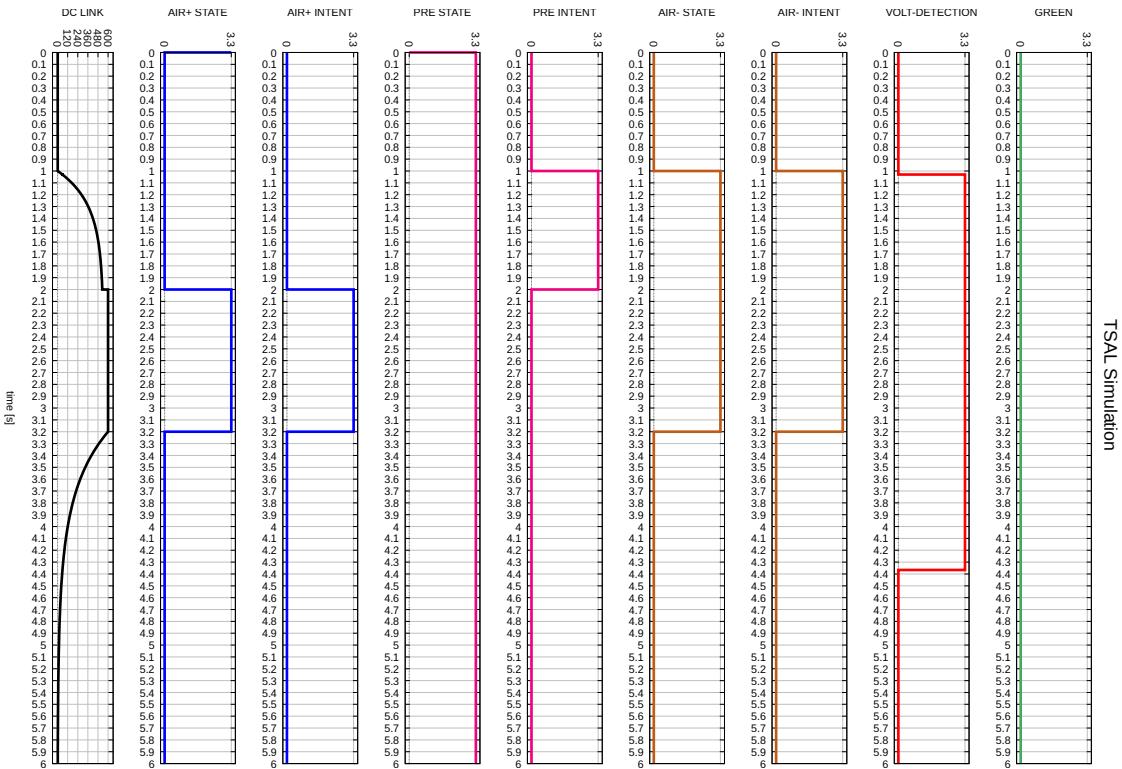


Figure 6.5.: TSAL simulation result. Test: Pre-charge relay stuck.

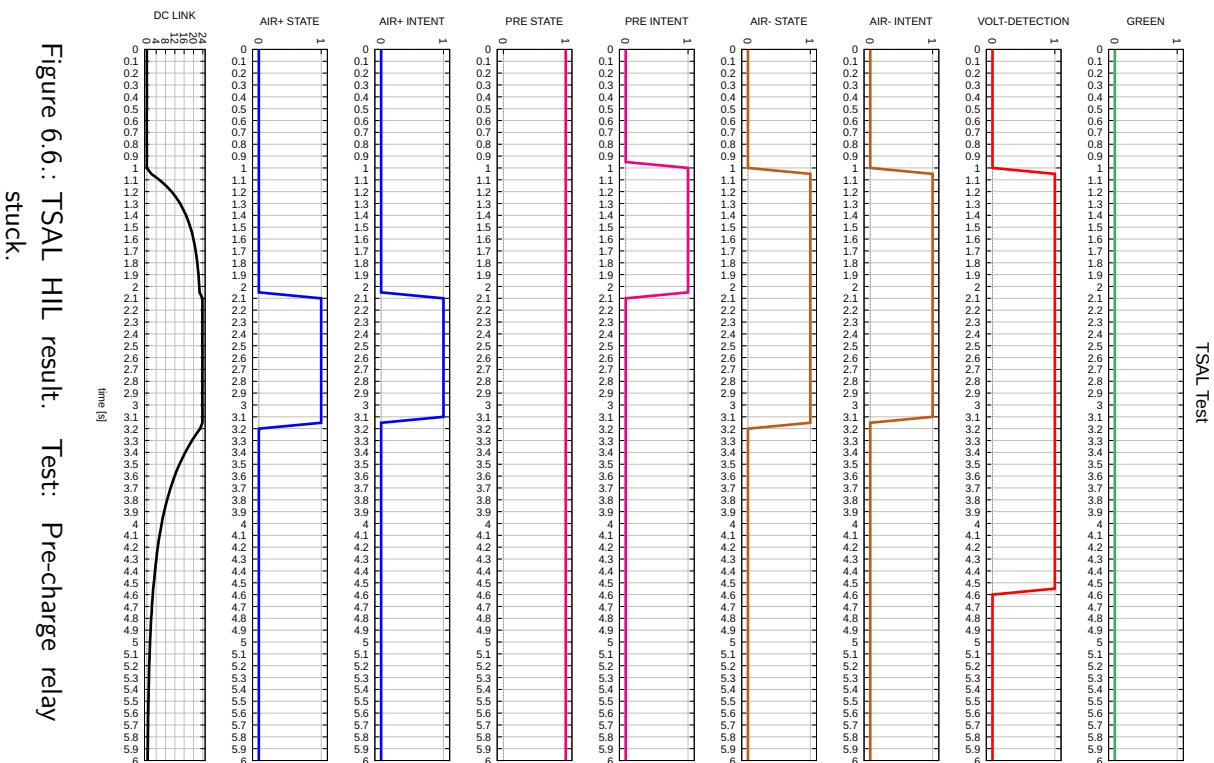


Figure 6.6.: TSAL HIL result. Test: Pre-charge relay stuck.

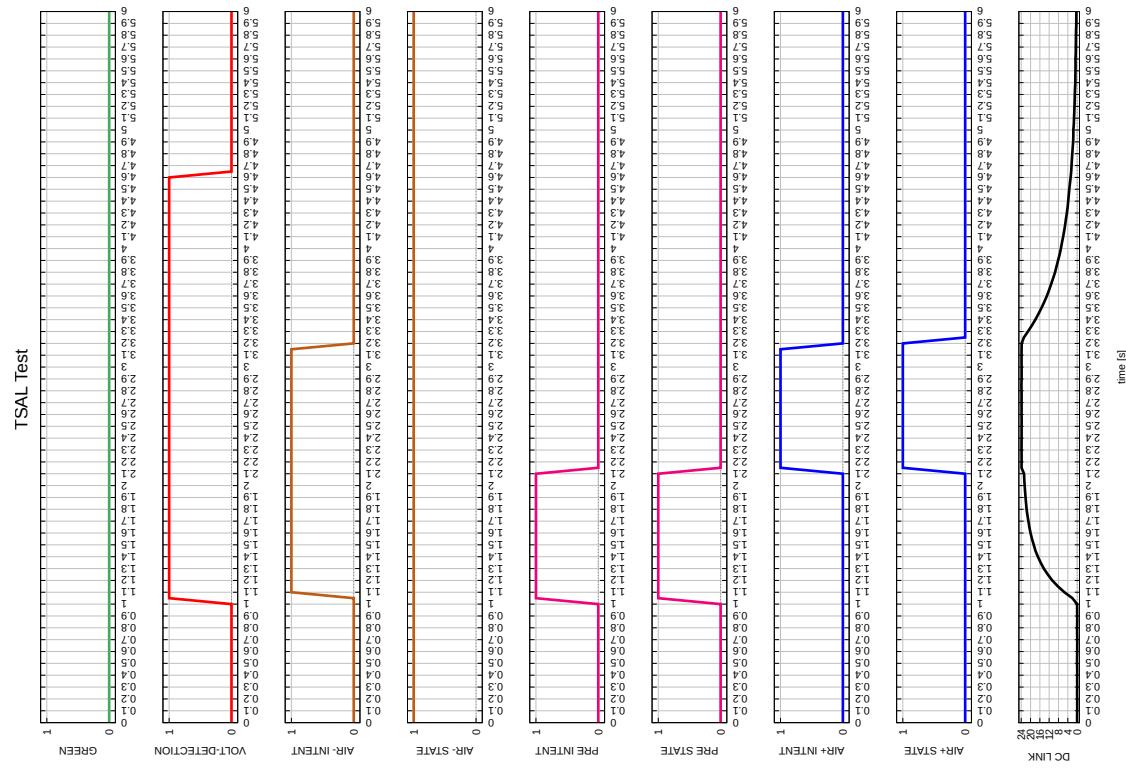


Figure 6.8.: TSAL HIL result. Test: Negative AIR stuck.

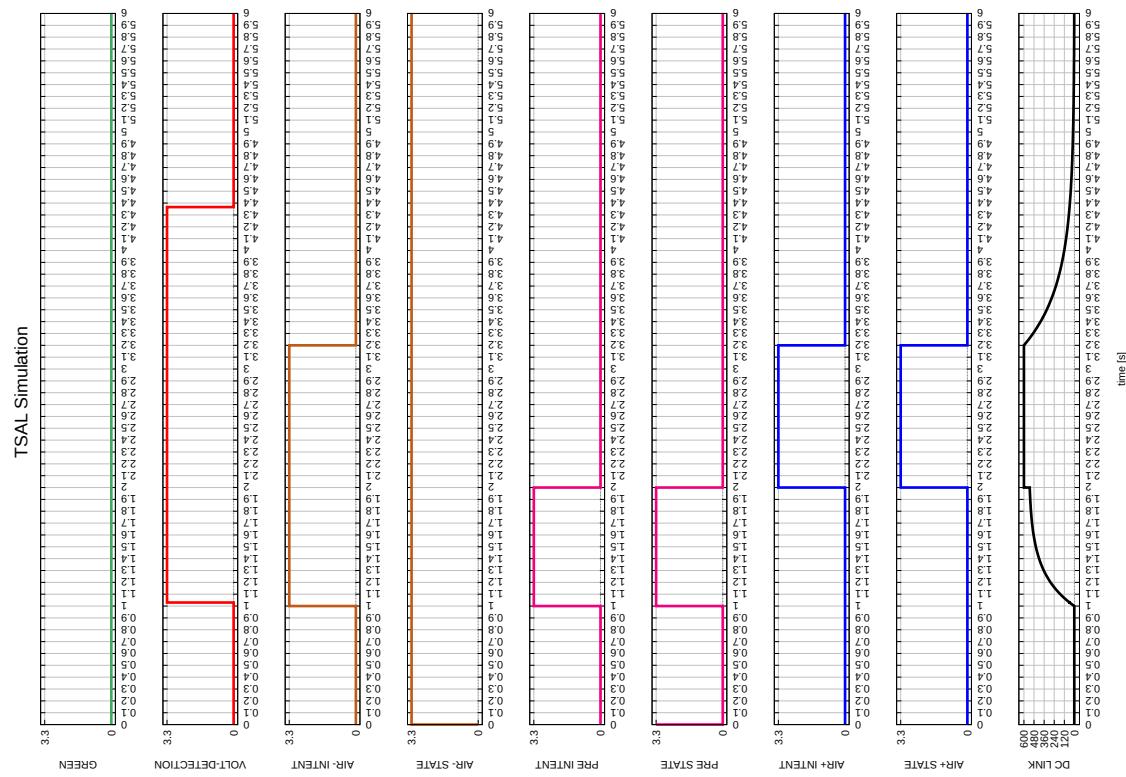


Figure 6.7.: TSAL simulation result. Test: Negative AIR stuck.

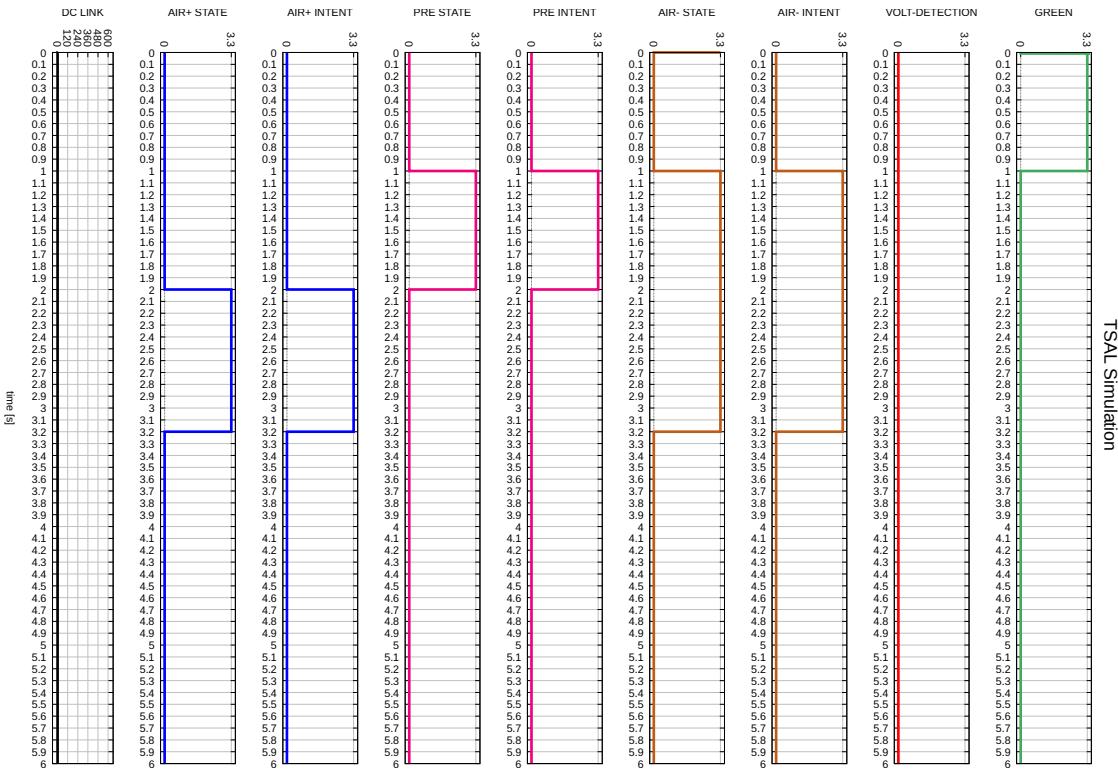


Figure 6.9.: TSAL simulation result. Test: Voltage detection broken wire.

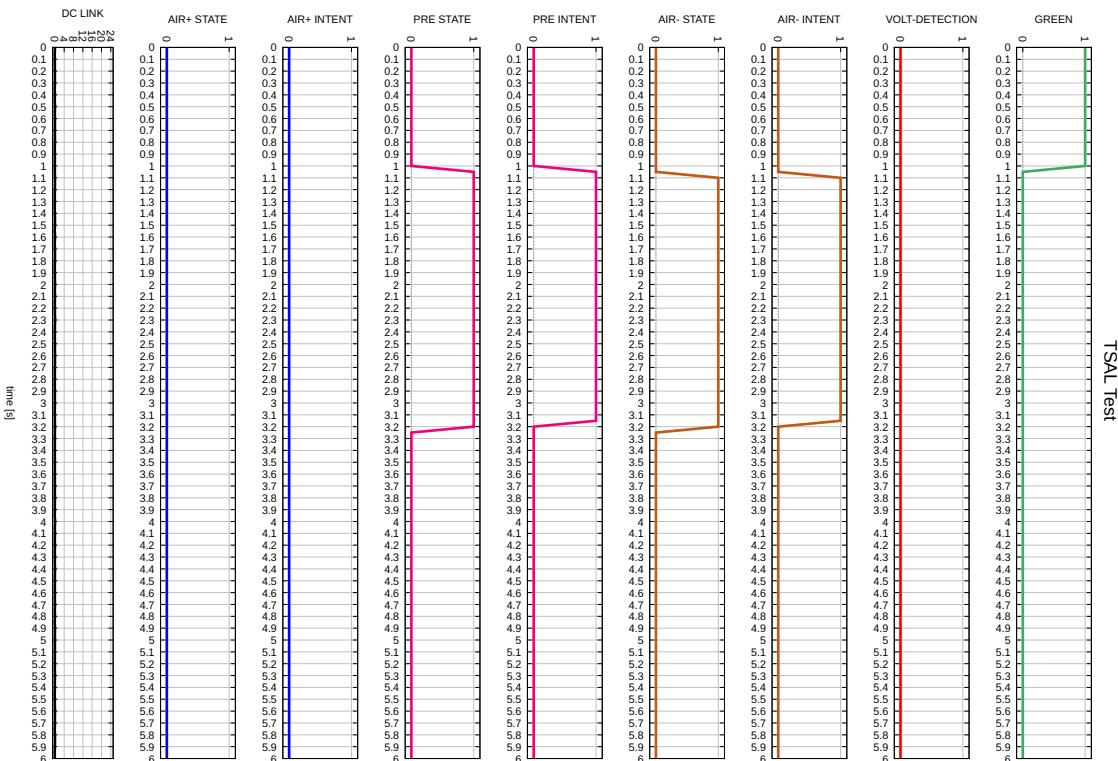


Figure 6.10.: TSAL HIL result. Test: Voltage detection broken wire.

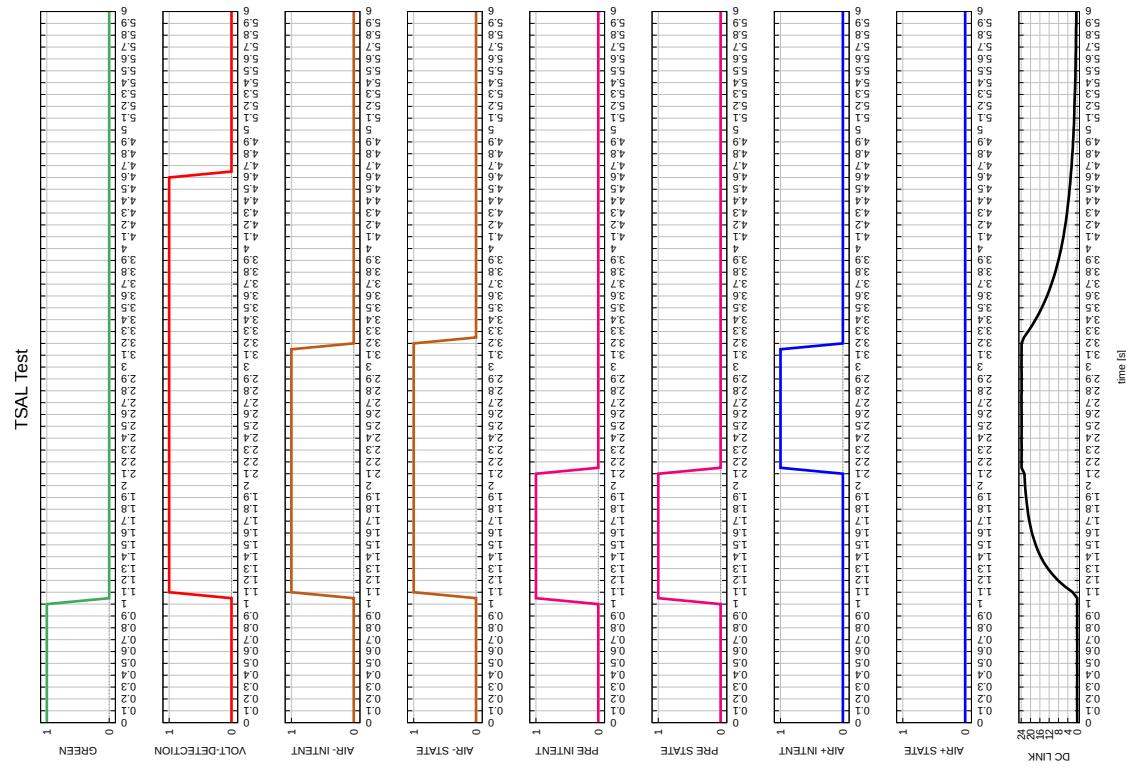


Figure 6.12.: TSAL HIL result. Test: Positive AIR state detection broken wire.

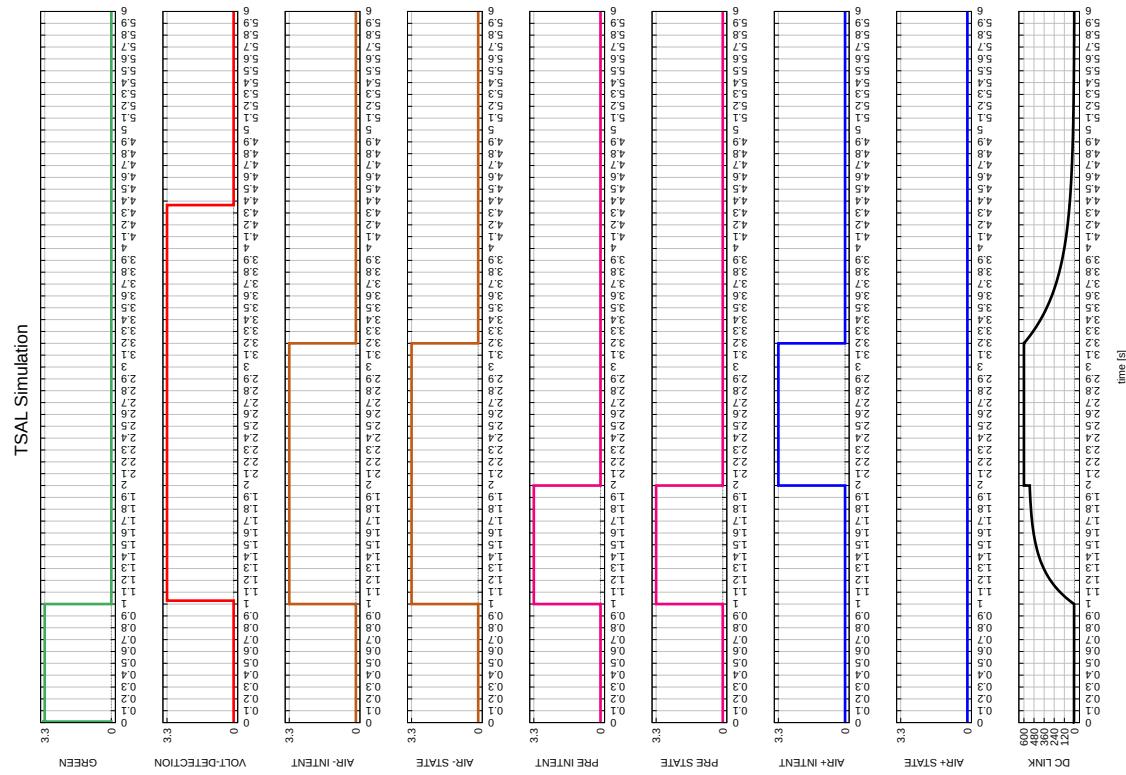


Figure 6.11.: TSAL simulation result. Test: Positive AIR state detection broken wire.

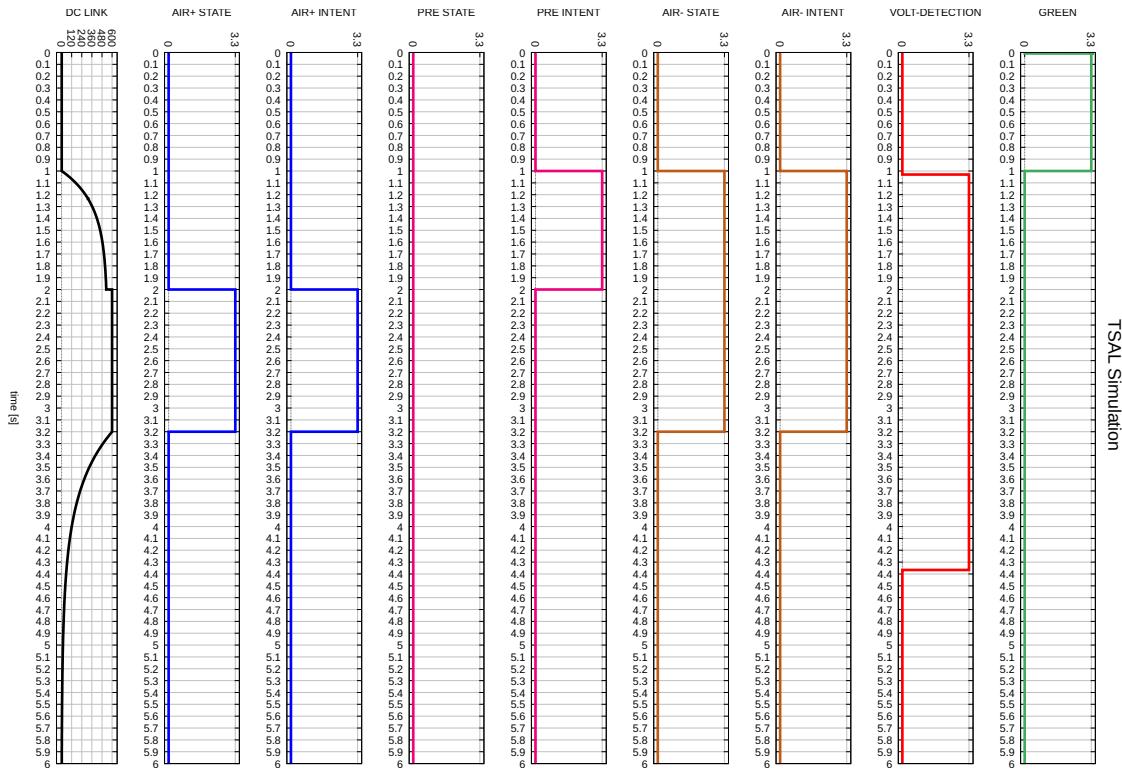


Figure 6.13.: TSAL simulation result. Test: Pre-charge relay state detection broken wire.

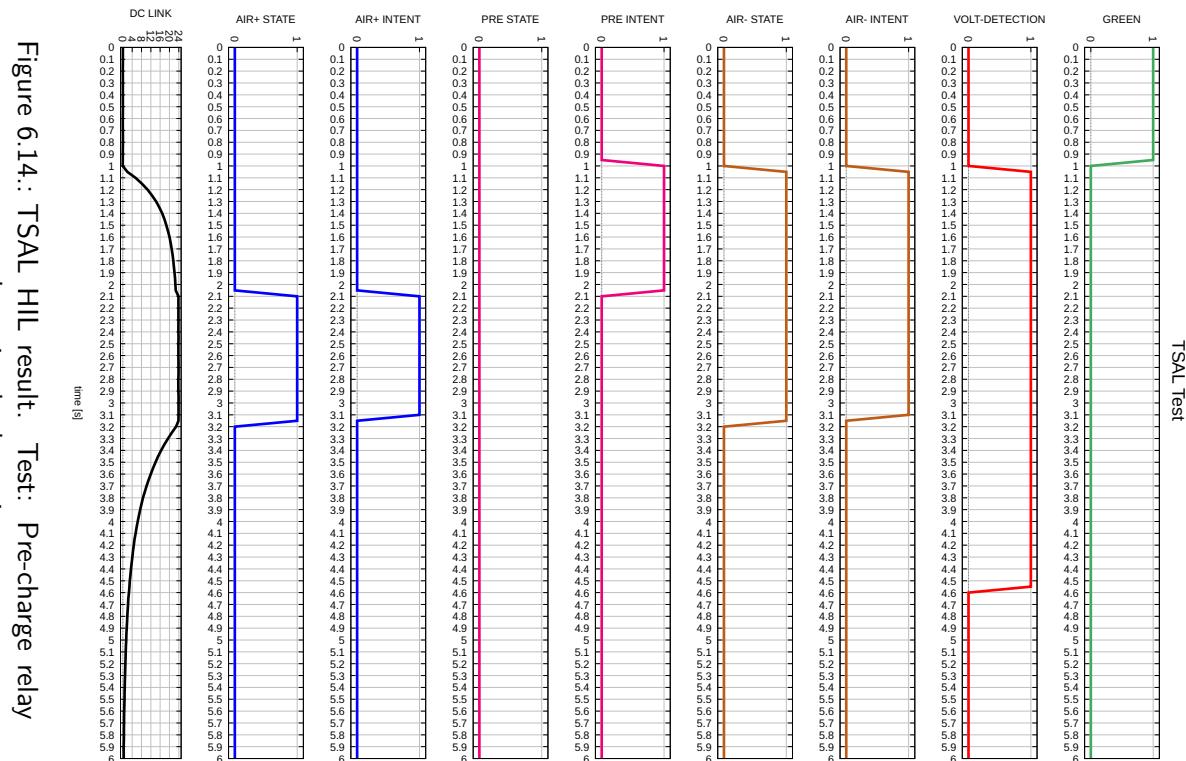


Figure 6.14.: TSAL HIL result. Test: Pre-charge relay state detection broken wire.

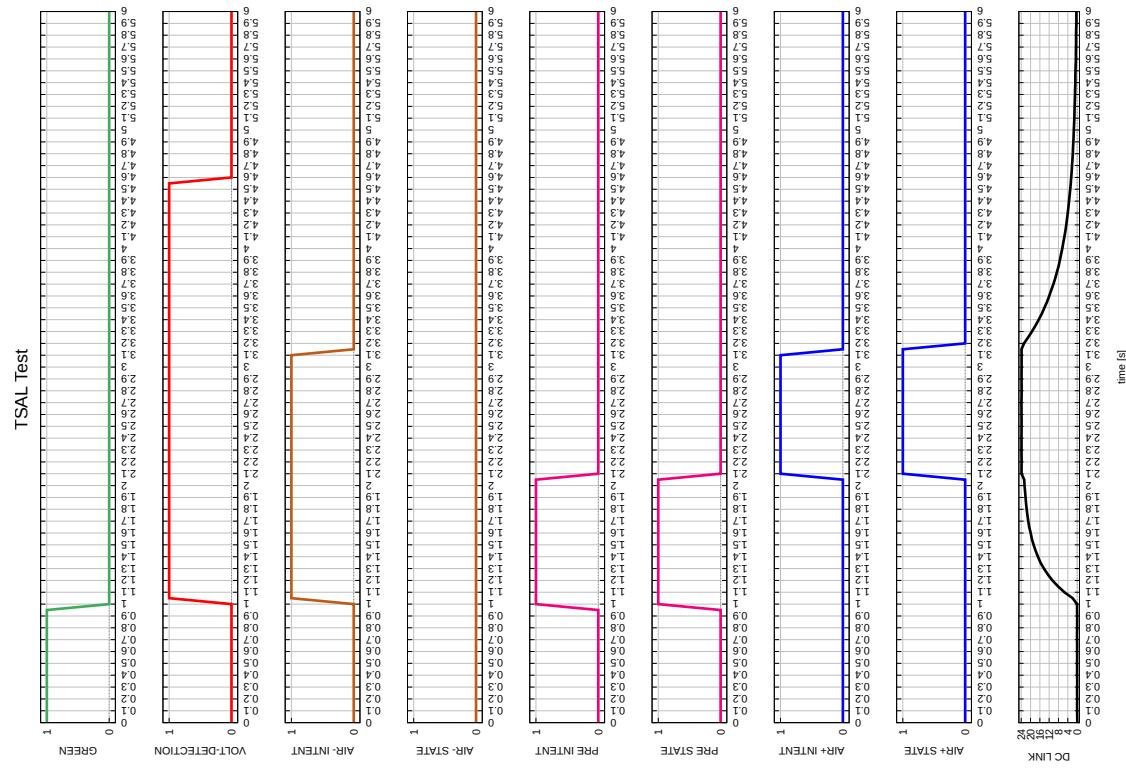


Figure 6.16.: TSAL HIL result. Test: Negative AIR state detection broken wire.

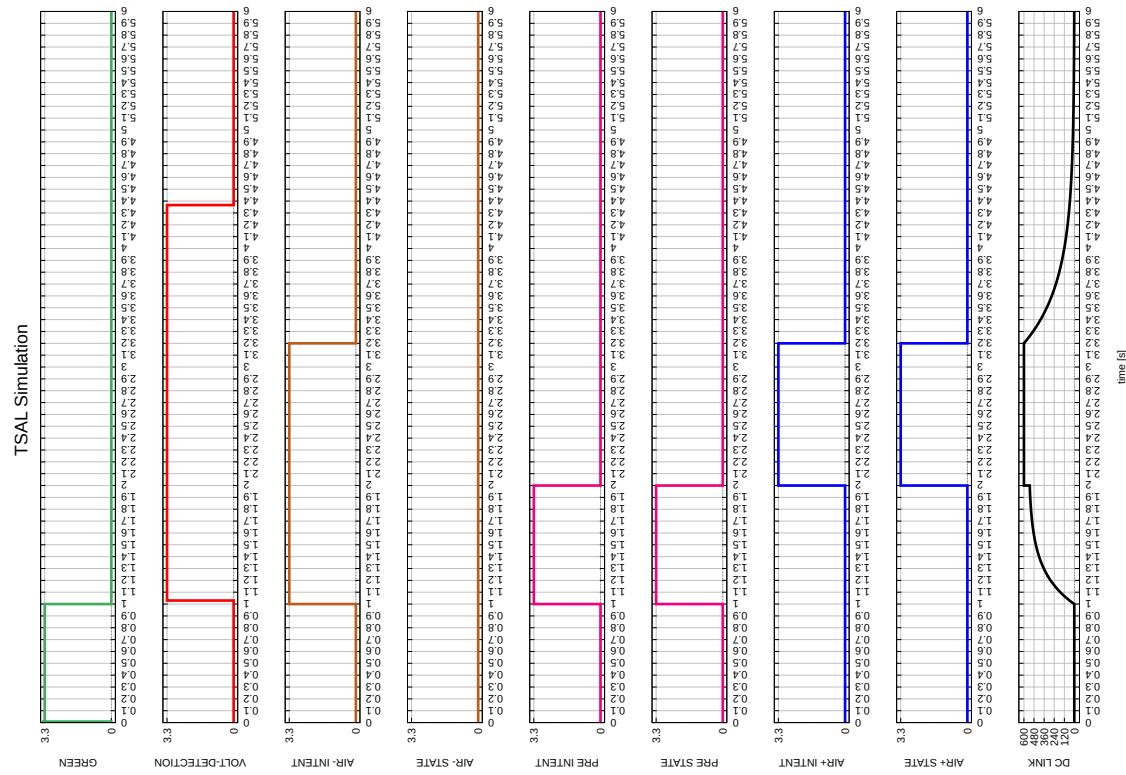


Figure 6.15.: TSAL simulation result. Test: Negative AIR state detection broken wire.

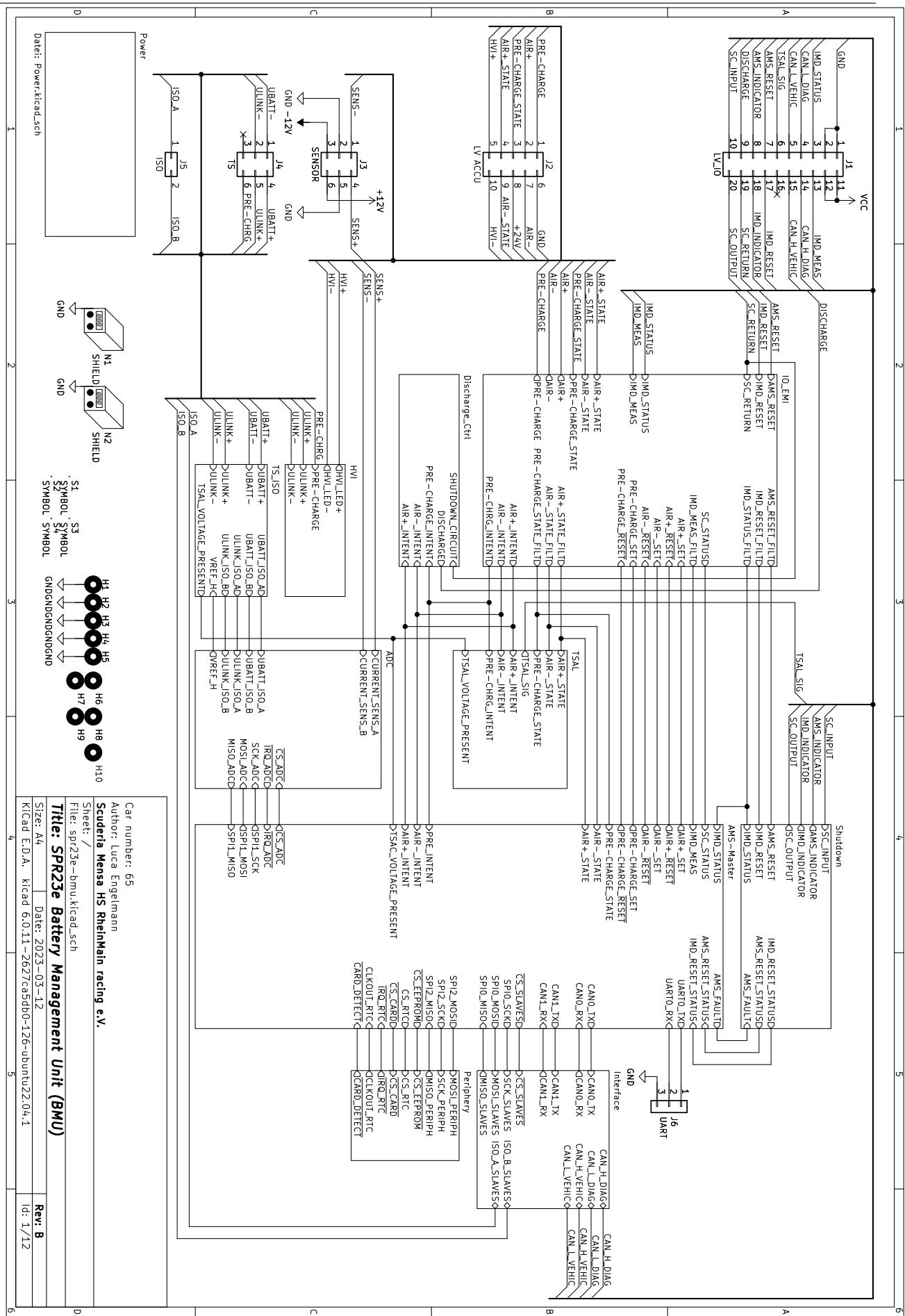


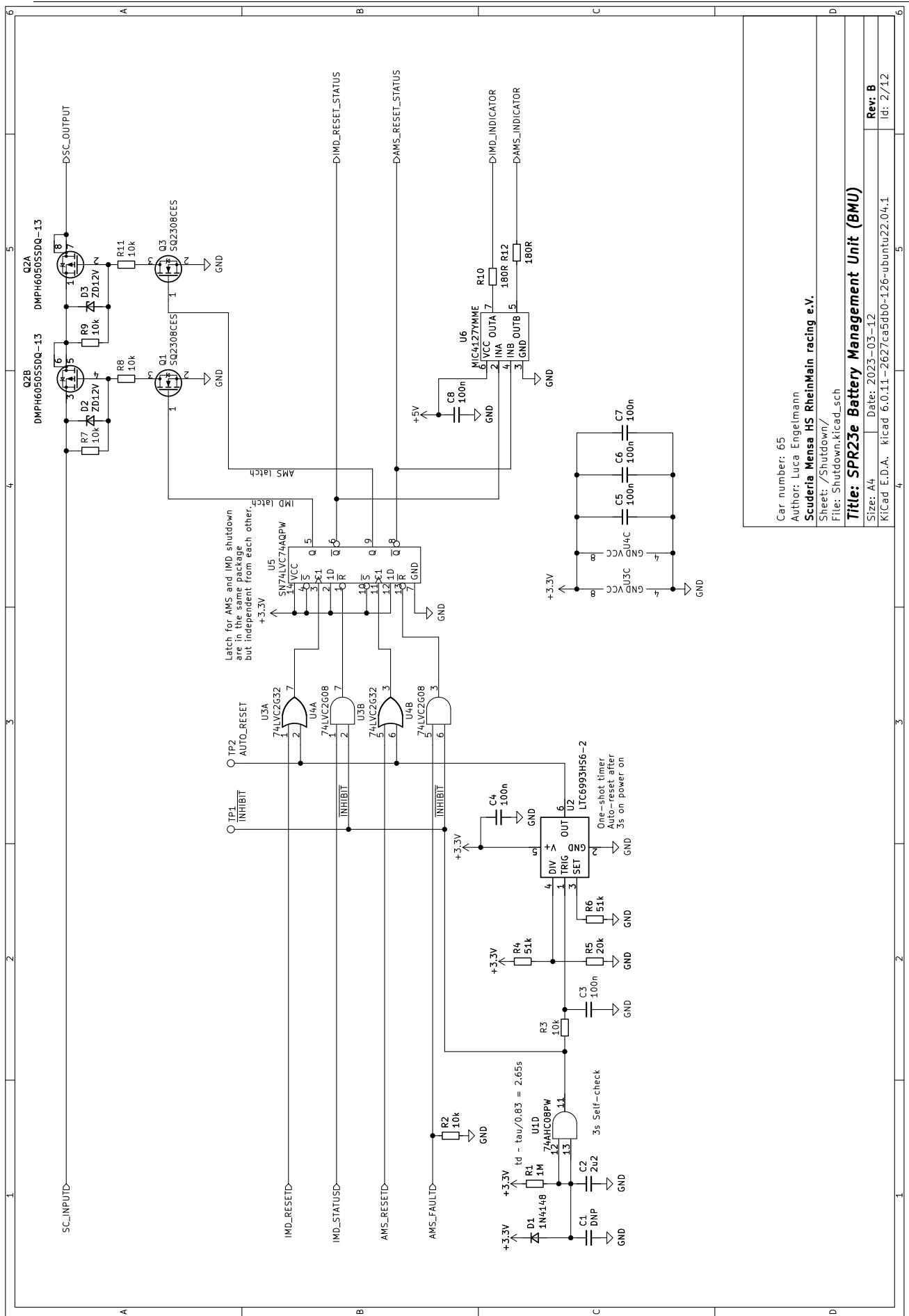
7. Bibliography

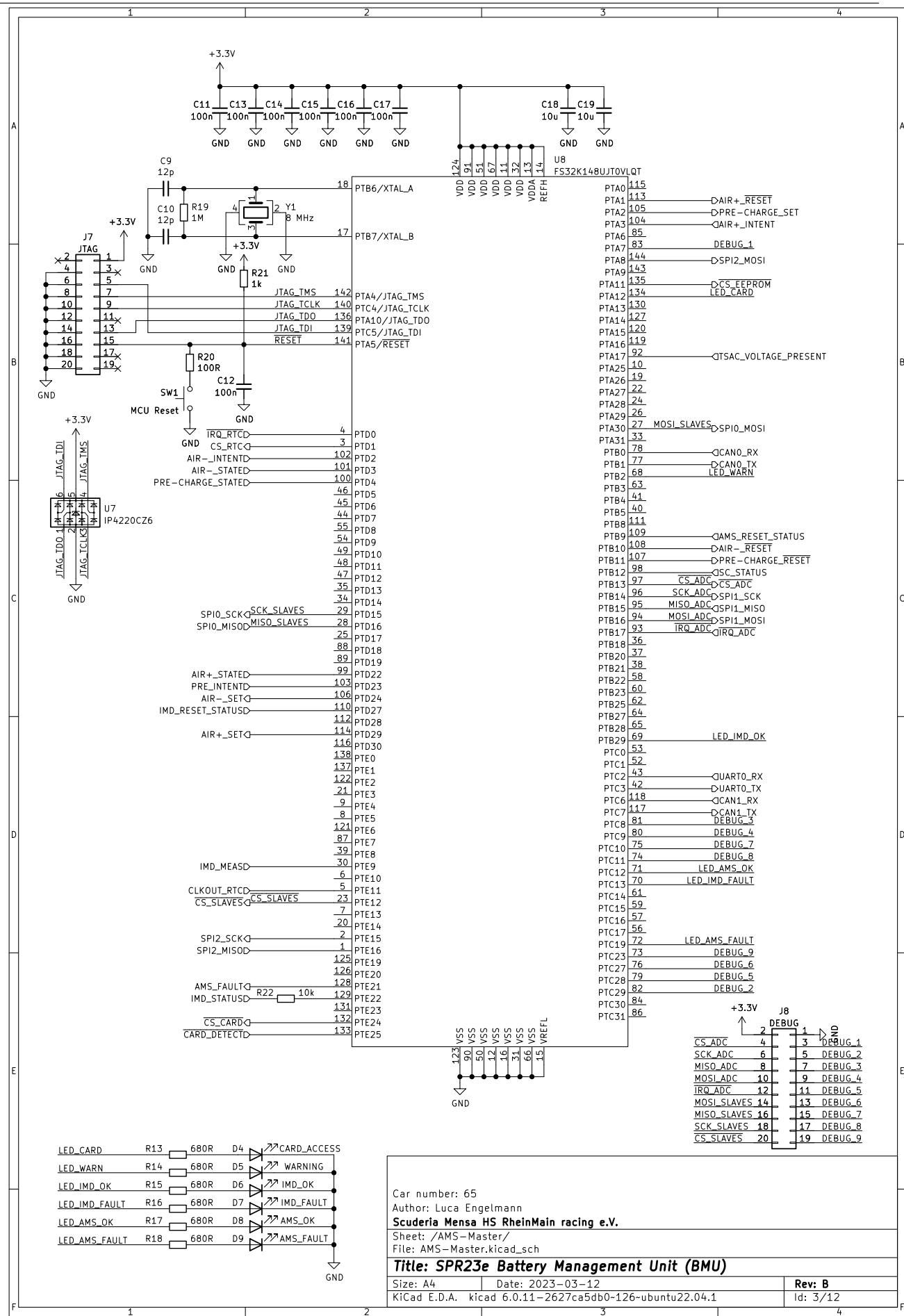
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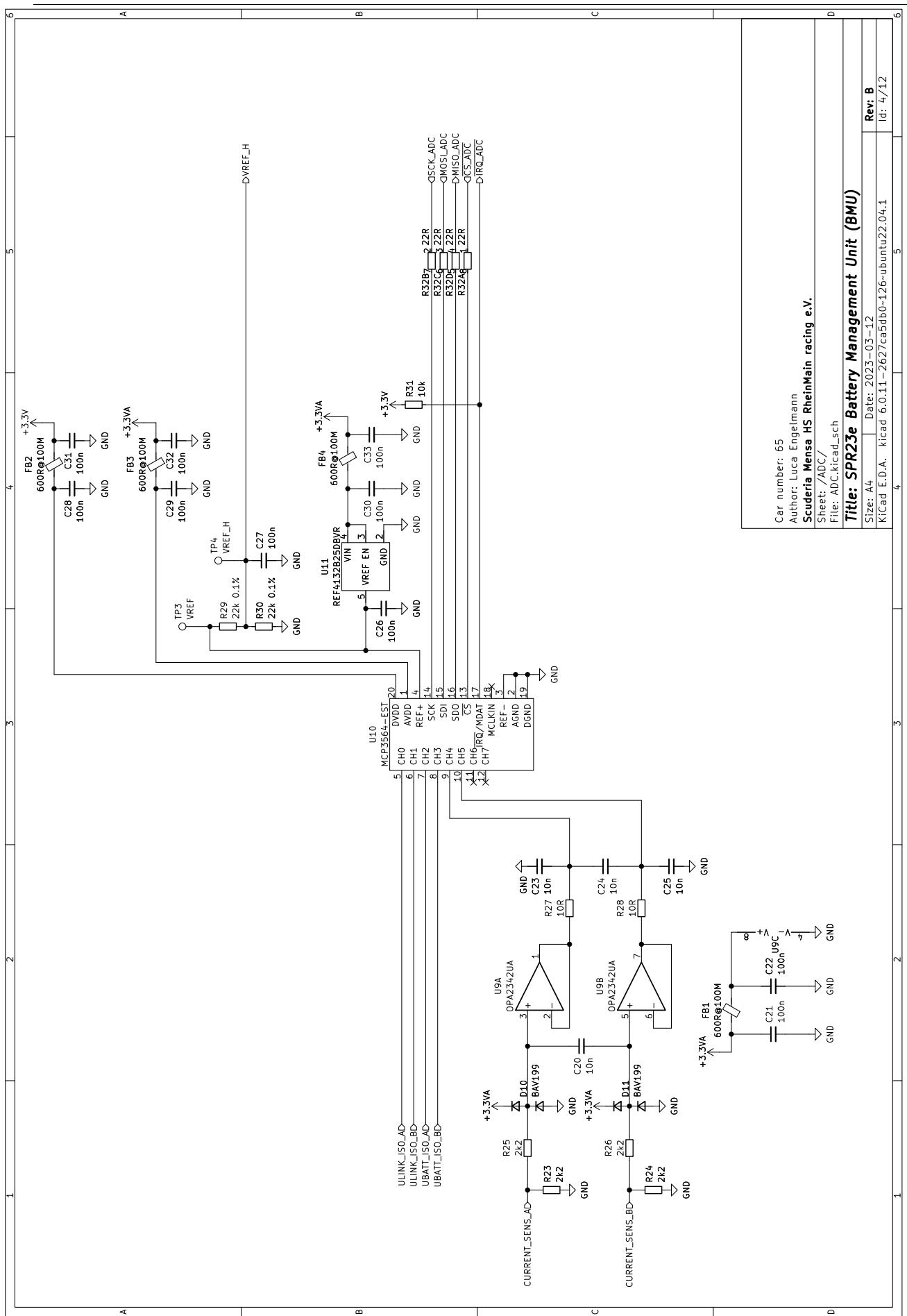


A. Schematics Revision A (Only for reference!)









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Scuderia Mensa HS RheinMain racing e.V.

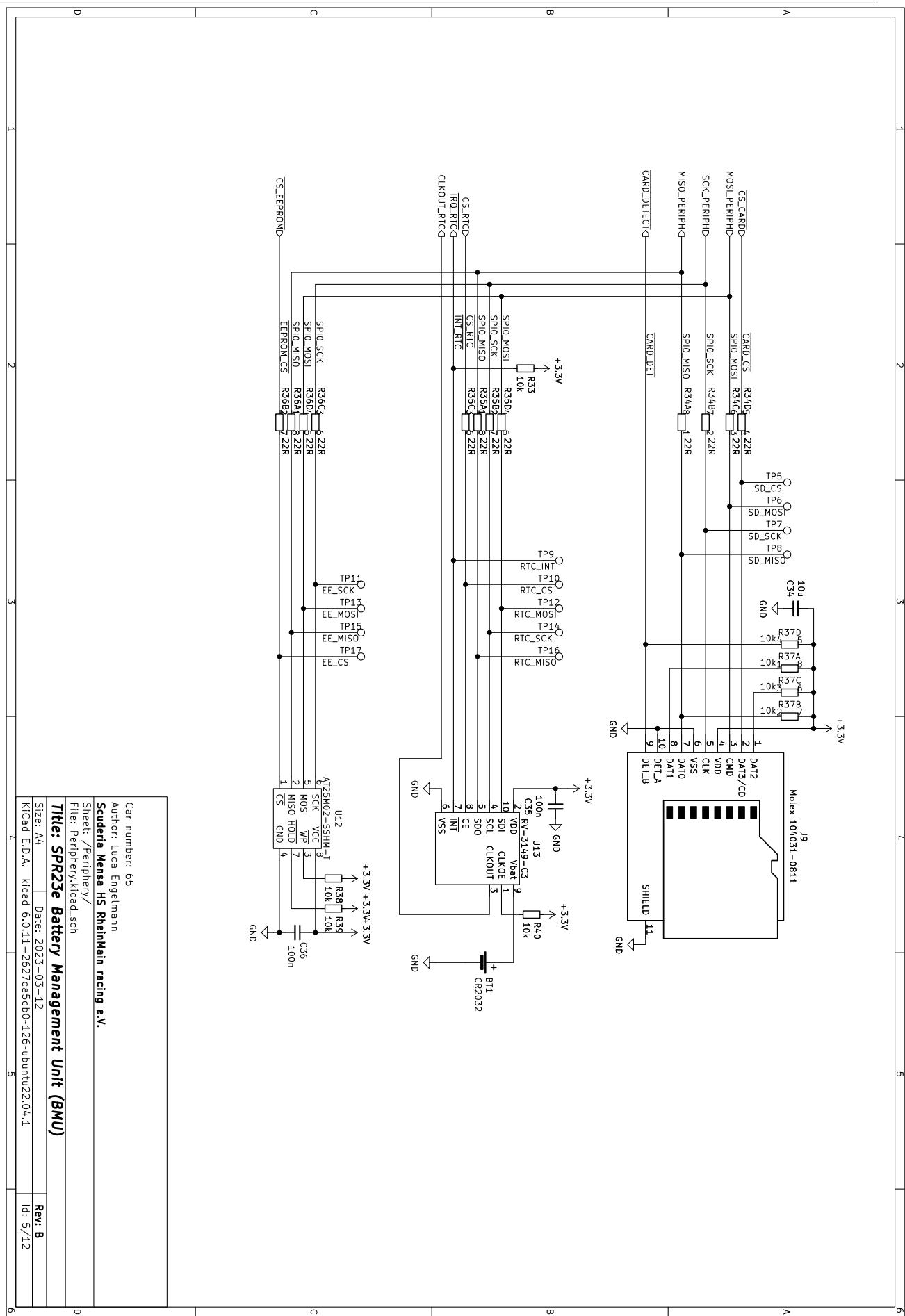
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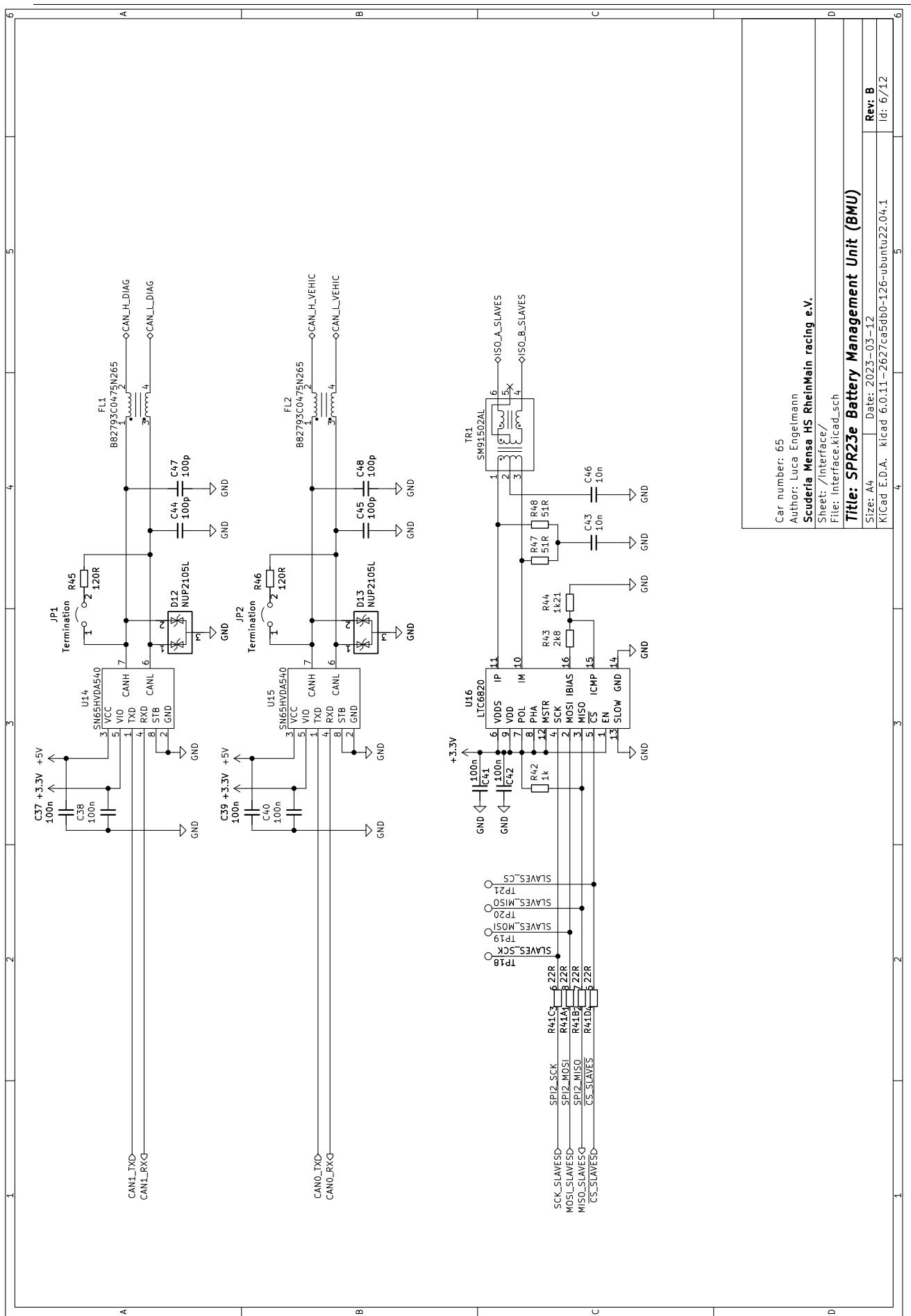
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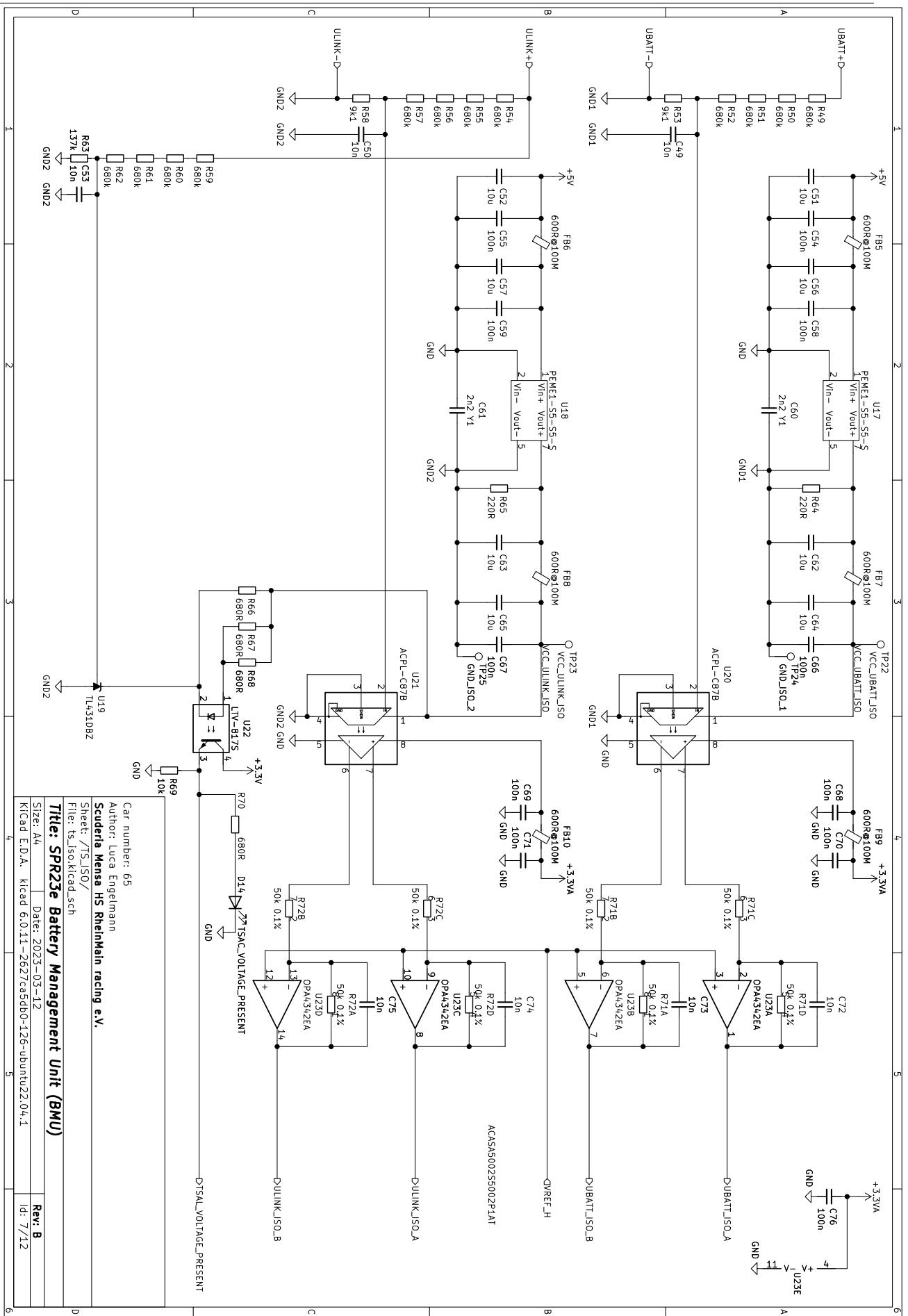
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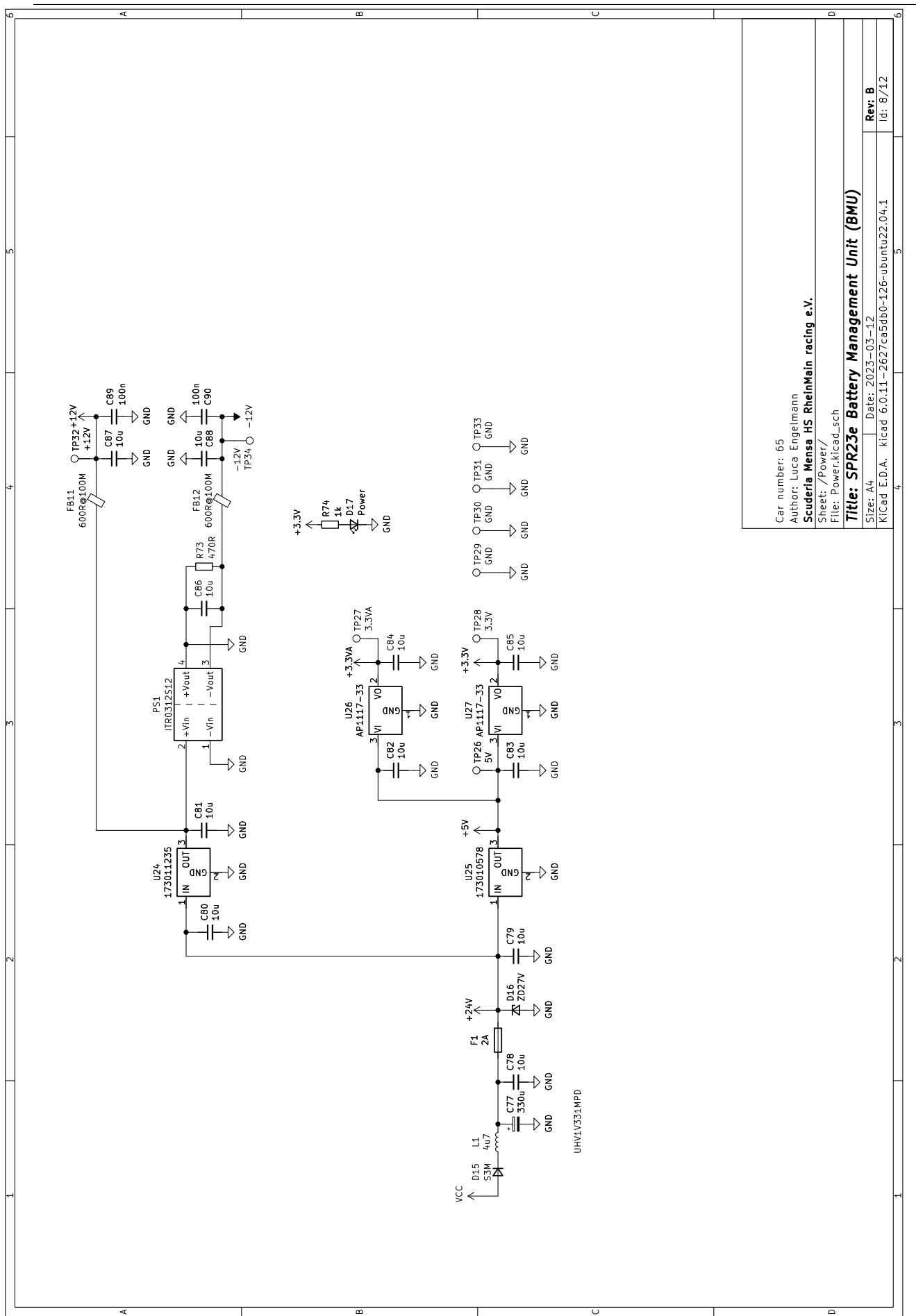
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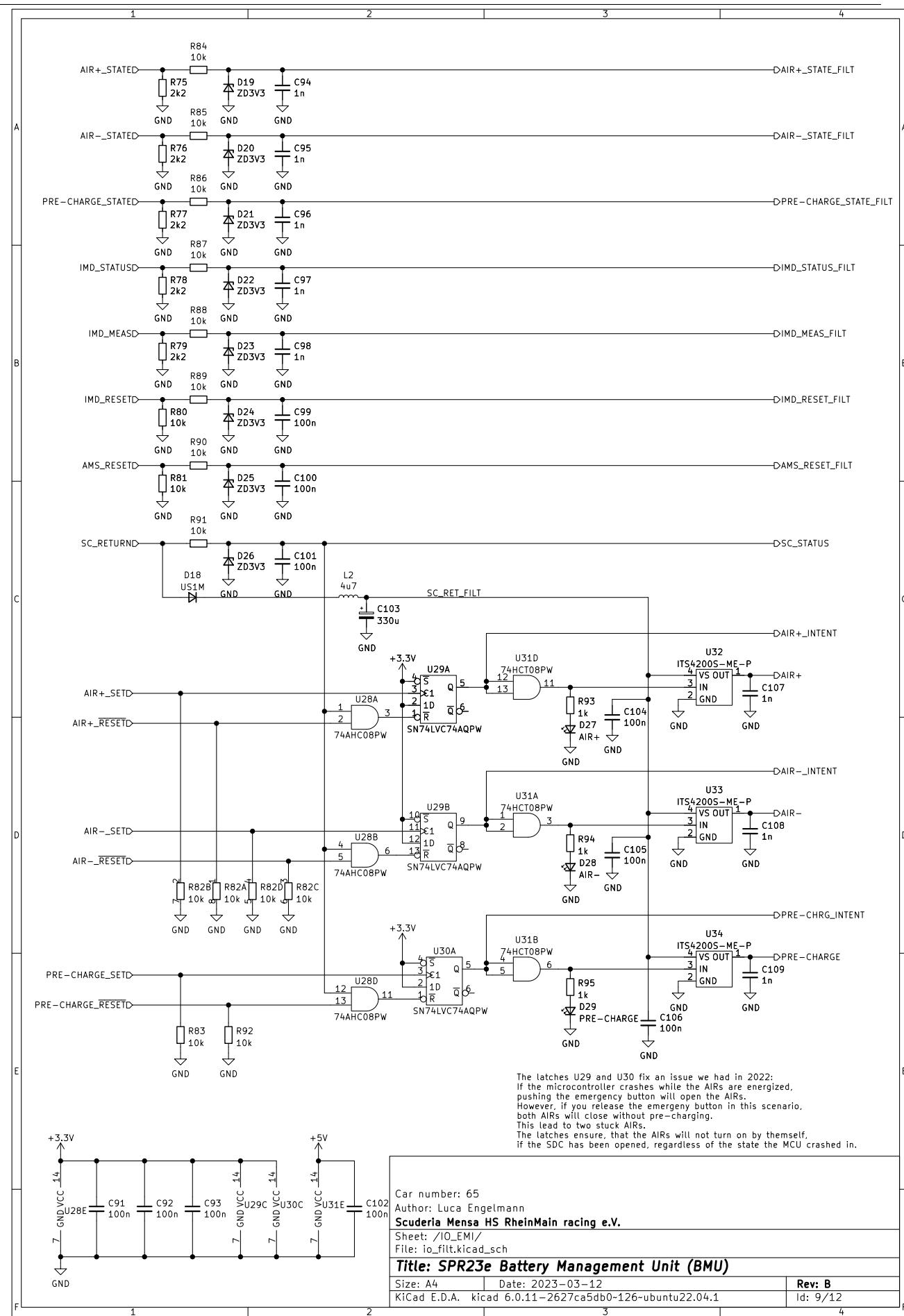
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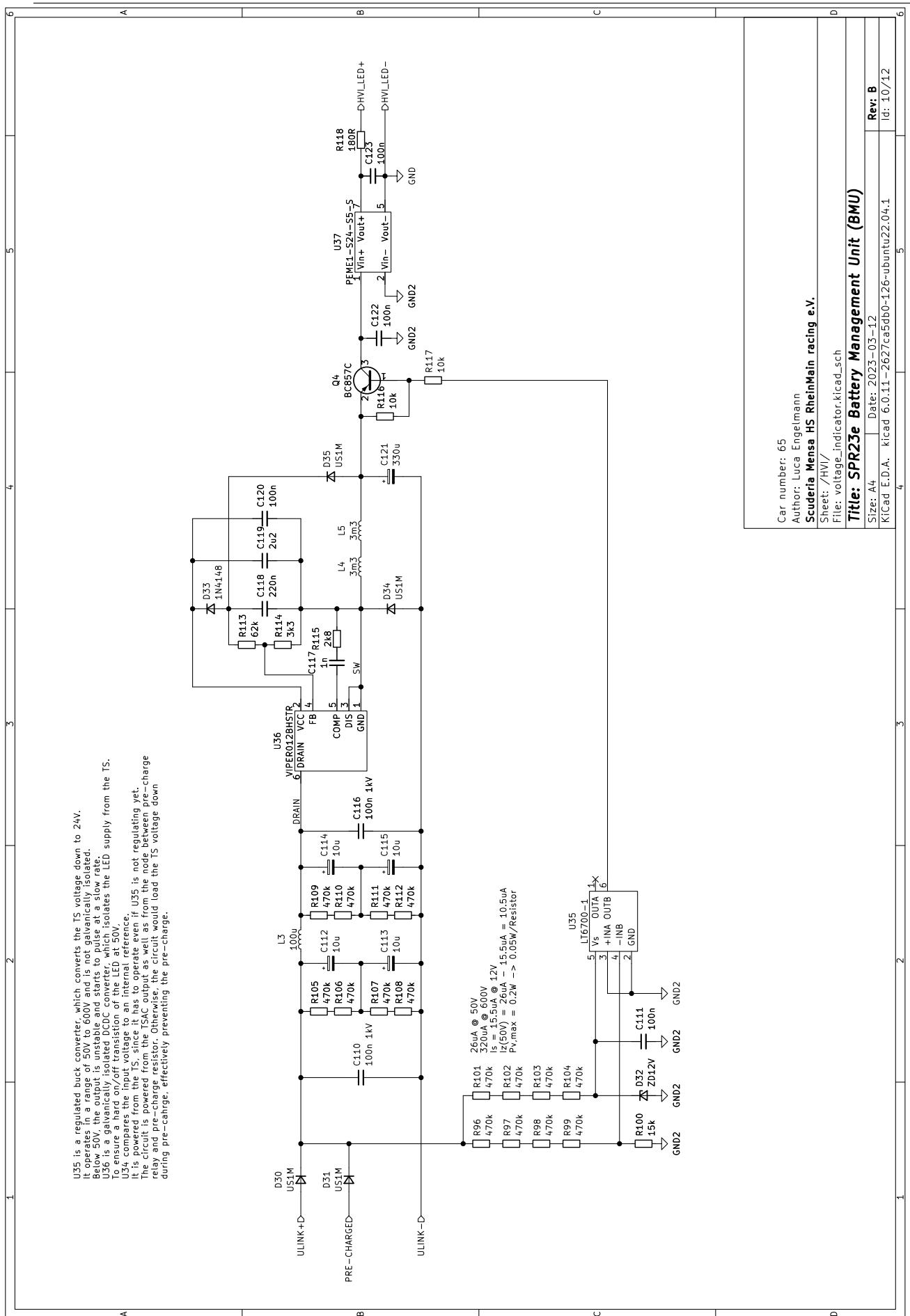


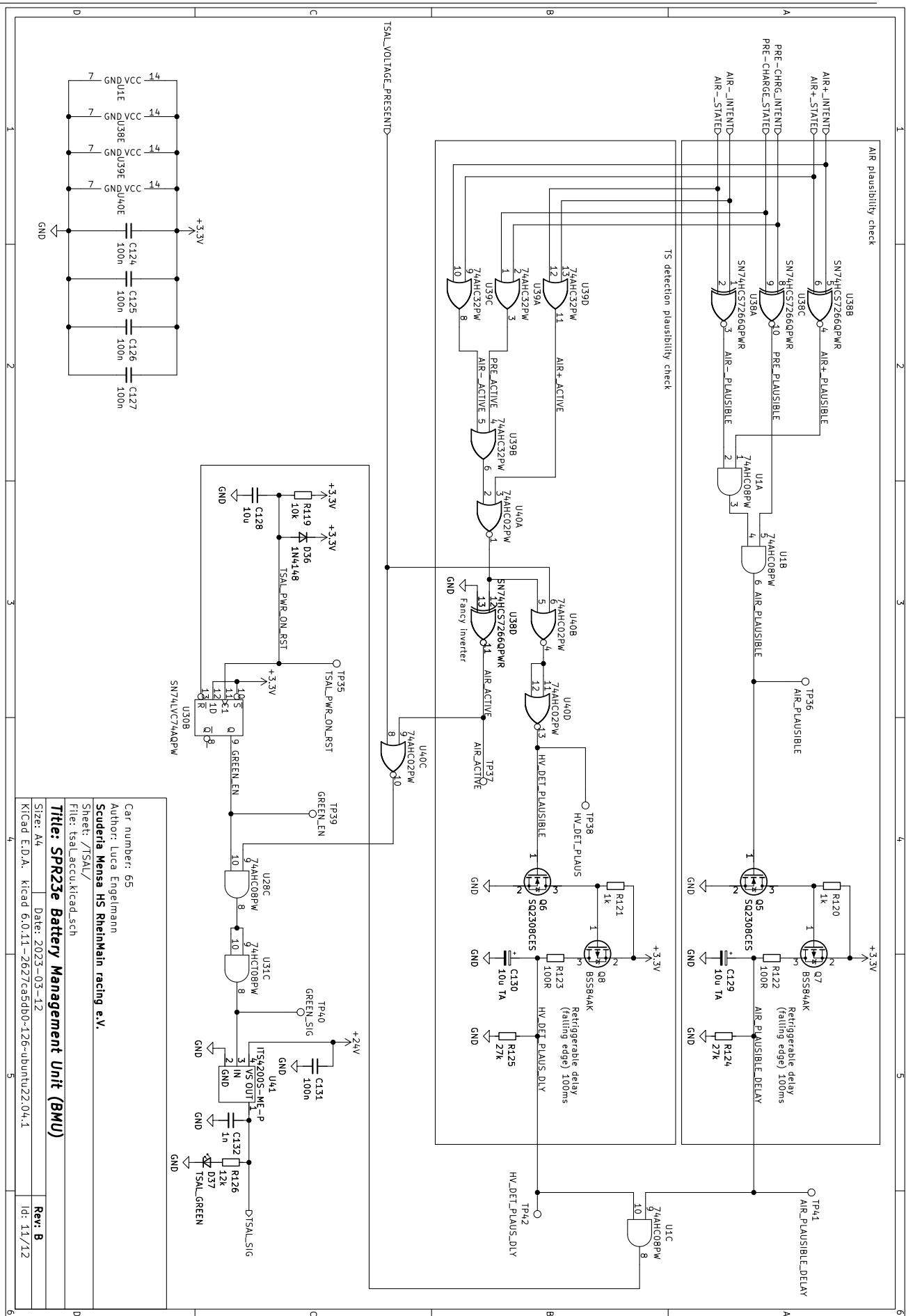


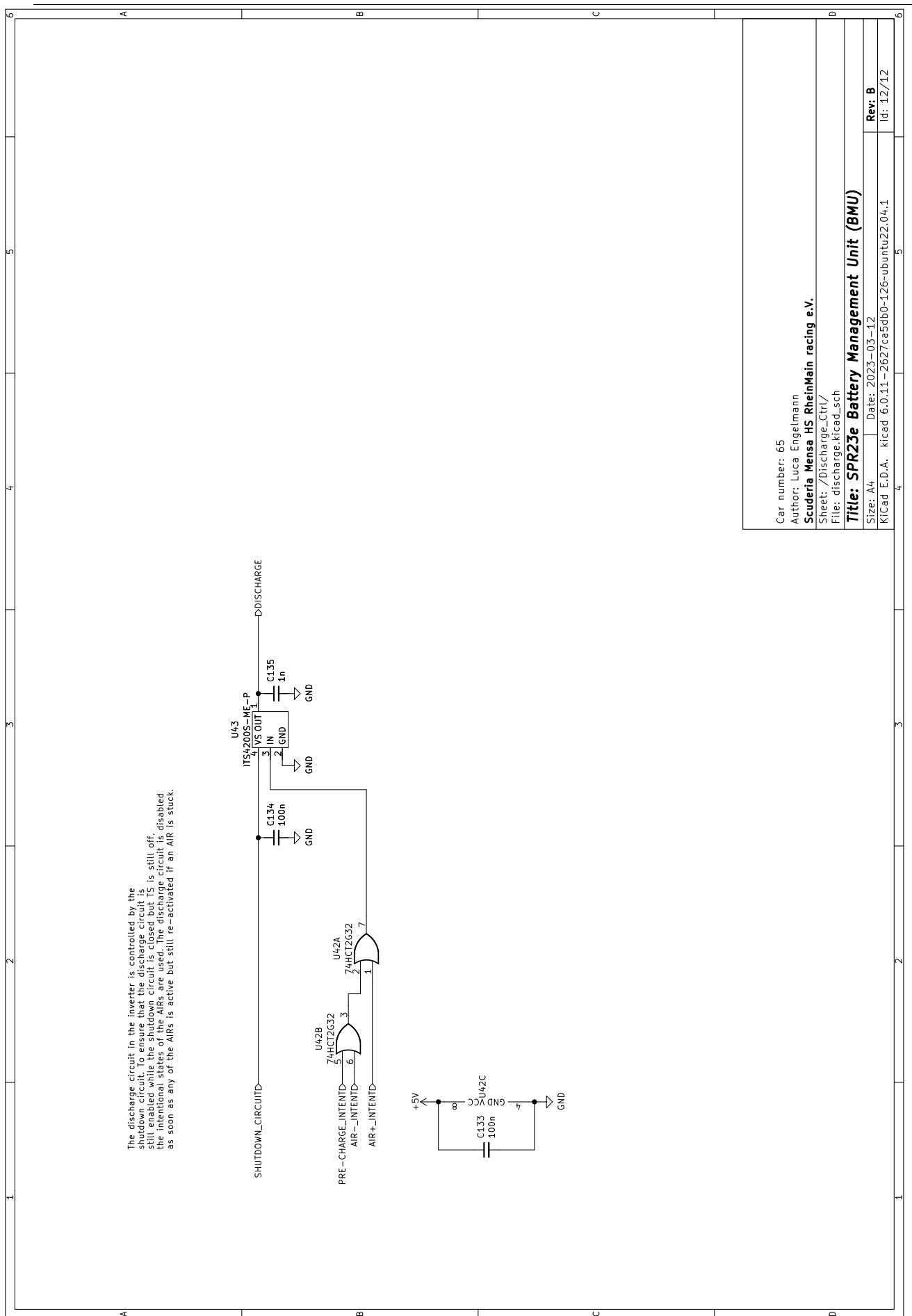














B. Changelog Revision B

- Corrected pinout of 74xx08
- Corrected pinout of 74xx2G08
- Corrected pinout of 74xx32
- Corrected pinout of 74xx2G32
- 74AHC08PW has no "real" Schmitt trigger inputs. Replaced by SN74HCS08.
- Removed ± 12 V power supplies from the BMU to clear out some space. It is only needed for the current sensor. Therefore it has been moved to the sensor PCB.
- Different comparator circuit for the voltage indicator for a sharp transition between on and off.
- Added minimum load for the isolated DCDC converters
- Increased the resistance value of the zener diode current limiting resistors at the inputs.
- Added test points for VREF, VREF_H and the outputs of the isolated DCDC converters.
- Increased the power-on-reset time for the TSAL latch
- Added ESD and overvoltage protection for the current sensor inputs
- Corrected the footprints of the electrolytic capacitors
- Corrected the footprints of the EMI suppression capacitors
- Corrected the control of the indicator LEDs. The LEDs must light up, if the power stage is disabled.
- Added pull-down resistor for the AMS fault signal
- Added a diode between SC_RET_FILT and SC_RETURN to decouple the high power signal from the low power signal.
- Typos corrected
- Changed reverse polarity protection diode for a higher current type
- Changed LED dropper resistors for equalized brightness
- Changed shutdown circuit auto-reset time to 3 s since IMD takes up to two seconds to power up.
- Only one power LED at the 3.3 V rail
- Reduced the delay time for the AIR plausibility to 100 ms to reduce BOM. 100 ms is sufficient.



C. Schematics Revision B

