/main/SW	0z00000000							
[9]								
[8]								
[7]								
[6]								
[5]								
[4]								
[3]								
[2]								
[1]								
[0]								
/main/KEY	0011	0010	0011	0010	0011
[3]					
[2]					
[1]					
[0]					
/main/LEDR	00001110	00011100	00111000
[7]			
[6]			
[5]			
[4]			
[3]			
[2]			
[1]			
[0]			
/main/LSR			

60000 ps 70000 ps 80000 ps 90000 ps 100000 p

Entity:main Architecture: Date: Wed Oct 17 02:34:19 EDT 2018 Row: 2 Page: 2

Signal	Value		
/main/SW	0z00000000		
[9]			
[8]			
[7]			
[6]			
[5]			
[4]			
[3]			
[2]			
[1]			
[0]			
/main/KEY	0010	0011	
[3]			
[2]			
[1]			
[0]			
/main/LEDR	00111000	01110000	
[7]			
[6]			
[5]			
[4]			
[3]			
[2]			
[1]			
[0]			
/main/LSR			

Left shift goes through several clock cycles after loading in values

110000 ps   120000 ps   130000 ps   140000 ps   150000 p

Entity:main Architecture: Date: Wed Oct 17 02:34:19 EDT 2018 Row: 3 Page: 3