Derek Albosta
1)
subi

RegDst	Branch	MemRead	MemToReg	ALUop1	ALUop2	MemWrite	ALUSrc	RegWrite
0	0	0	0	0	1	0	1	1

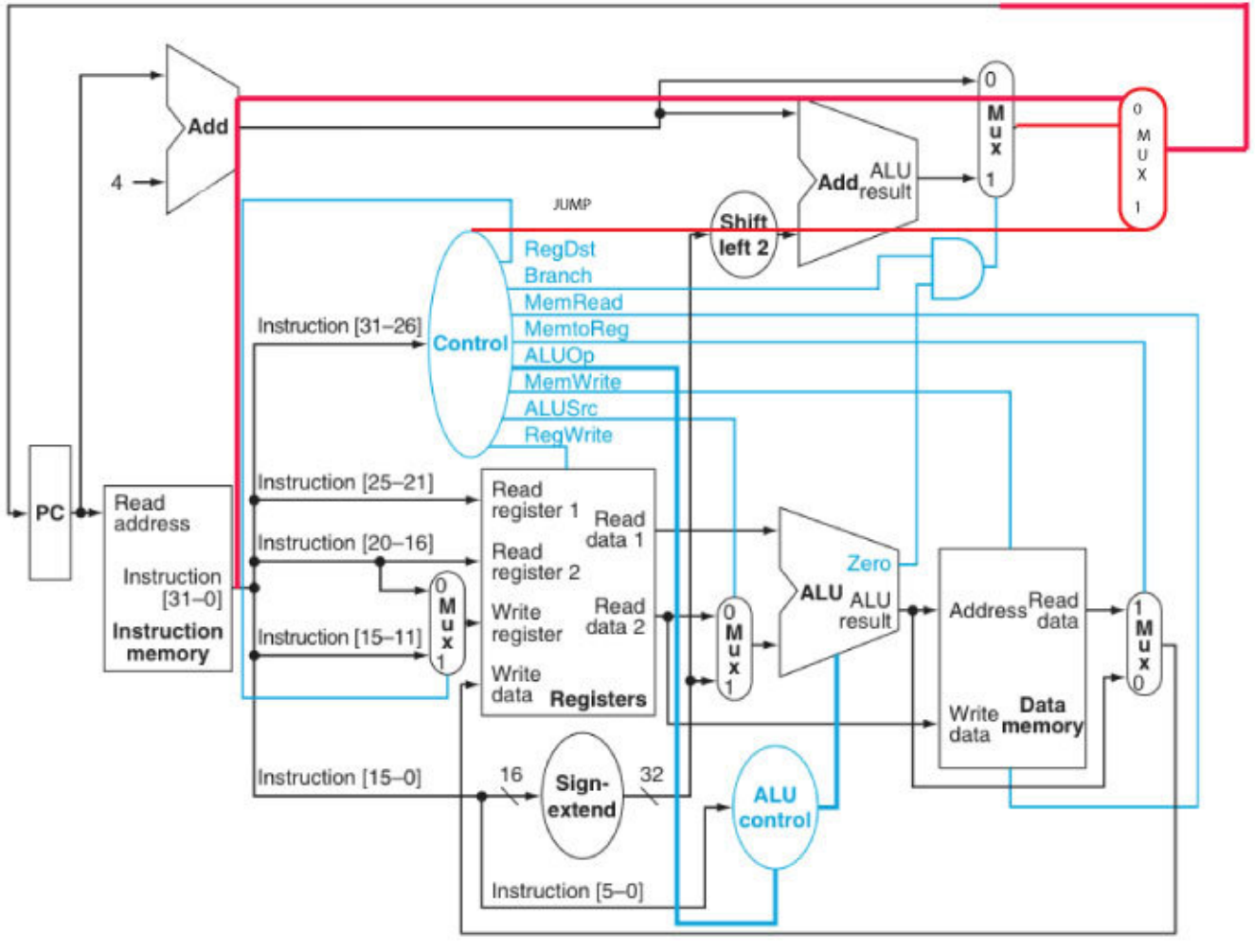
no wiring needed

2)
jr

RegDst	Branch	MemRead	MemToReg	ALUop1	ALUop2	MemWrite	ALUSrc	RegWrite	J ump
0	0	1	0	0	0	0	0	0	1

wiring needed to go back and jump to register. multiplexer needed to differentia te
Sw/Lw shift. (on image)

3)
  a) MemWrt = (Op0 * !Op1 * Op2 * !Op3 * Op4 * Op5)
  b) ALUSrc = (Op0 * !Op1 * (Op2 + !Op2) * !Op3 * Op4 * Op5)
  c) MemtoReg = (Op0 * !Op1 * !Op2 * !Op3 * Op4 * Op5)


Add
4
JUMP
Shift left 2
Add
ALU result
0
M
u
x
1
0
M
U
X
1
RegDst
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
Control
Instruction [31–26]
PC
Read address
Instruction [31–0]
Instruction memory
Instruction [25–21]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]
Instruction [5–0]
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
16
Sign-extend
32
ALU
Zero
ALU result
ALU control
Address
Read data
Write data
Data memory
1
M
u
x
0