

# 11 - register transfer and microoperations

microoperations = the operations on the data in the registers.

↳ ex: shift, load, clear, arithmetic, logic

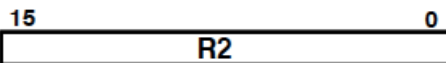
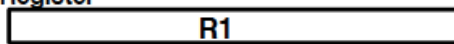
in transfer level  
language notation

## List of BC Registers

DR	16	Data Register	Holds memory operand
AR	12	Address Register	Holds address for memory
AC	16	Accumulator	Processor register
IR	16	Instruction Register	Holds instruction code
PC	12	Program Counter	Holds address of instruction
TR	16	Temporary Register	Holds temporary data
INPR	8	Input Register	Holds input character
OUTR	8	Output Register	Holds output character

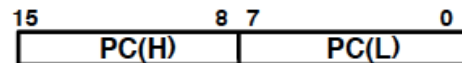
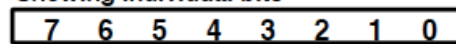
different block diagram of registers

Register



Numbering of bits

Showing Individual bits



Subfields

organization of a digital system = registers + microoperations + control signals  
(Computer)

Register Transfer Language

in register transfer level

register transfer =  $R3 \leftarrow R5$  → copying all the contents of one register to another

- during one clock pulse, parallel load in R3

- R5 remains same

- there one control lines to perform action

control functions = P:  $R3 \leftarrow R5$

- if  $P=1$ , then load the contents of register R5 into R3.

simultaneous operation = P:  $R3 \leftarrow R5, MAR \leftarrow IR$

## basic symbols for register transfers

Symbols	Description	Examples
Capital letters & numerals	Denotes a register	MAR, R2
Parentheses ()	Denotes a part of a register	R2(0-7), R2(L)
Arrow $\leftarrow$	Denotes transfer of information	$R2 \leftarrow R1$
Colon :	Denotes termination of control function	P:
Comma ,	Separates two micro-operations	$A \leftarrow B, B \leftarrow A$

connecting registers:

- instead  $\rightarrow$  not practical to use  $n(n-1)$  lines to load each register with all other register contents  
 the bus = one centralized set of circuits for data transfer  
 $\rightarrow$  have control circuits to select source and destination registers  
 $\rightarrow$  using decoders, muxes, three state buffers,  
 $R2 \leftarrow R1 = \text{BUS} \leftarrow R1, R2 \leftarrow \text{BUS}$

memory: (ram)

$\rightarrow$  a sequential circuit that contains some number of registers

M = memory, MAR/AR = memory address register

memory read:  $R1 \leftarrow M[MAR] \rightarrow$  read a value from a location in memory and load it into a register

memory write:  $M[MAR] \leftarrow R1 \rightarrow$  write a value from a register to a location in memory

microoperations in computer systems

- ① register transfer
- ② arithmetic
- ③ logic  $\rightarrow$  16 different logic functions between two bits
- ④ shift

$A \leftarrow B$	Transfer content of reg. B into reg. A
$AR \leftarrow DR(AD)$	Transfer content of AD portion of reg. DR into reg. AR
$A \leftarrow \text{constant}$	Transfer a binary constant into reg. A
$ABUS \leftarrow R1, R2 \leftarrow ABUS$	Transfer content of R1 into bus A and, at the same time, transfer content of bus A into R2
AR	Address register
DR	Data register
$M[R]$	Memory word specified by reg. R
M	Equivalent to $M[AR]$
$DR \leftarrow M$	Memory <i>read</i> operation: transfers content of memory word specified by AR into DR
$M \leftarrow DR$	Memory <i>write</i> operation: transfers content of DR into memory word specified by AR

① register transfer

## Summary of Typical Arithmetic Micro-Operations

$R3 \leftarrow R1 + R2$	Contents of R1 plus R2 transferred to R3
$R3 \leftarrow R1 - R2$	Contents of R1 minus R2 transferred to R3
$R2 \leftarrow R2'$	Complement the contents of R2
$R2 \leftarrow R2' + 1$	2's complement the contents of R2 (negate)
$R3 \leftarrow R1 + R2' + 1$	subtraction
$R1 \leftarrow R1 + 1$	Increment
$R1 \leftarrow R1 - 1$	Decrement

② arithmetic

– Selective-set	$A \leftarrow A + B$
– Selective-complement	$A \leftarrow A \oplus B$
– Selective-clear	$A \leftarrow A \cdot B'$
– Mask (Delete)	$A \leftarrow A \cdot B$
– Clear	$A \leftarrow A \oplus B$
– Insert	$A \leftarrow (A \cdot B) + C$
– Compare	$A \leftarrow A \oplus B$

③ logic

### logic microoperations

selective set:  $A \leftarrow A + B$  → if a bit in B is set to 1, that same position in A gets set to 1, otherwise that bit in A keeps its previous value *set certain bits*  
 not addition!  
 ex: 1100 A<sub>+</sub>  
 1010 B  
 1110 A<sub>(+1)</sub> ( $A \leftarrow A + B$ )

selective complement:  $A \leftarrow A \oplus B$   $\rightarrow$  if a bit in B is set to 1, that same position in A gets complemented from its original value, otherwise it is unchanged. complement certain bit

ex:  $\begin{array}{cccc} 1 & 1 & 0 & 0 & A \\ 1 & 0 & 1 & 0 & B \\ \hline 0 & 1 & 1 & 0 & A(+1) \quad (A \leftarrow A \oplus B) \end{array}$

selective clear:  $A \leftarrow A.B'$   $\rightarrow$  if a bit in B is set to 1, that position in A gets set to 0, otherwise it is unchanged clear certain bits

ex:  $\begin{array}{r} 1100 \text{ A} \\ 1010 \text{ B} \\ \hline 0100 \text{ A}_{t+1} \text{ (A} \leftarrow \text{A.B')} \end{array}$

mask operation:  $A \leftarrow A \cdot B \rightarrow$  if a bit in  $B$  is set to 0, that same position in  $A$  gets to be set 0, otherwise it is unchanged. *clear certain bits*

ex:

1100	$A$
1010	$B$
1000	$A_{(t+1)} \quad (A \leftarrow A \cdot B)$

clear operation:  $A \leftarrow A \oplus B \rightarrow$  if the bits in the same position in  $A$  and  $B$  are the same, they are cleared in  $A$ , otherwise they are set in  $A$ .

ex: 
$$\begin{array}{r} 1100 \text{ } A \\ 1010 \text{ } B \\ \hline 0110 \text{ } A(t+1) \end{array} \quad (A \leftarrow A \oplus B)$$

insert operation:  $A \leftarrow (A.B) + C \rightarrow$

- to introduce a specific bit pattern into A register, leaving the other bit positions unchanged: done as:
  - $\hookrightarrow$  a mask operation to clear the desired bit positions
  - $\hookrightarrow$  an OR operation to introduce the new bits into the desired positions

ex:  $1101100010110001 \rightarrow A \text{ original}$   
 $1101100010110100 \rightarrow A \text{ desired}$

$\hookrightarrow$

$1101100010110001 \rightarrow A$
$1111111111110000 \rightarrow \text{mask}$
<hr/>
$1101100010110000 \rightarrow A \text{ (intermediate)}$
$0000000000001010 \rightarrow \text{added bits}$
<hr/>
$1101100010110100 \rightarrow A \text{ desired}$

## shift microoperations

① logical shift

the serial input to the shift is a 0. (right shift of 111 is 011, left shift 110)

shl: logical shift left     $R2 \leftarrow shr\ R2$   
shr: logical shift right     $R3 \leftarrow shl\ R3$  } in a register transfer language

② circular shift

the serial input is the bit that shifted out of the other end of the register

$R_2 \leftarrow \text{cil } R_2$   
 $R_3 \leftarrow \text{cir } R_3$

$\text{cir}$ : circular shift right  $R3 \leftarrow \text{cir } R3$

③ arithmetic shift

meant for signed integers, (keeps the sign of the number the same as right/left shifts)

asr: arithmetic shift right  $\rightarrow$  divides a signed number by two ( $1010011 \rightarrow 1101001$ )

ashl: arithmetic shift left  $\rightarrow$  multiplies a signed number by two ( $1010011 \rightarrow 0100110$ )  
 $\hookrightarrow R_2 \leftarrow \text{ashr } R_1$        $R_2 \leftarrow \text{ashl } R_1$

overflow = ash left shift must check, if the leftmost two bits differ  $\rightarrow$  the shift will result in an over.