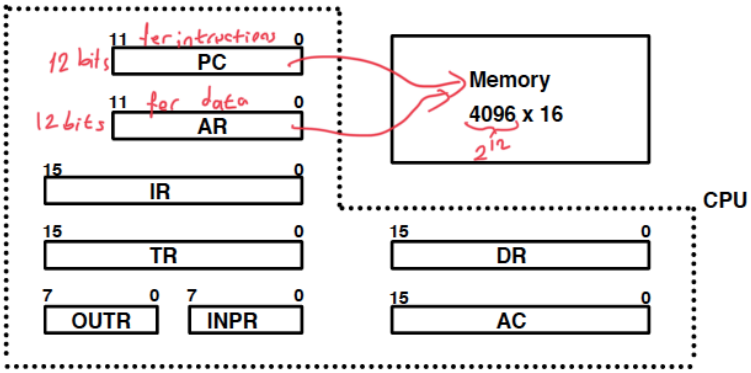
12 - digital system design

BASIC COMPUTER (BC) REGISTERS

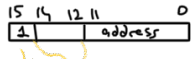
Registers in the Basic Computer



List of BC Registers

DR	16	Data Register	Holds memory operand
AR	12	Address Register	Holds address for memory
AC	16	Accumulator	Processor register
IR	16	Instruction Register	Holds instruction code
PC	12	Program Counter	Holds address of instruction
TR	16	Temporary Register	Holds temporary data
INPR	8	Input Register	Holds input character
OUTR	8	Output Register	Holds output character

basic computer = processor (CPU) + memory

instruction format → 

16 bits

bc → memory 4096 x 16

addressing mode: 0 direct, 1 indirect

opcode = operation code

IR = instructions are placed in instruction register

PC = program counter holds the memory address of the next instruction (increased by 1)

AR = address register keeps track of what locations in the memory that is being addressed

DR = when operand is found, it is placed in data register (then processor uses this value as data for its operation)

AC = the basic computer has a single general purpose register, the accumulator

TR = temporary register holds the intermediate / temporary results

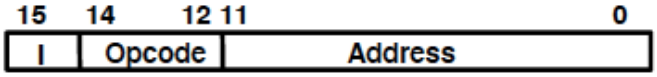
INPR = input register holds data gotten from an input device

OUTR = output register holds data to be send to an output device

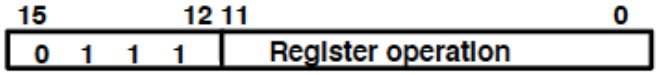
common bus system = the registers (this ones) are connected using a bus

basic computer instructions — format

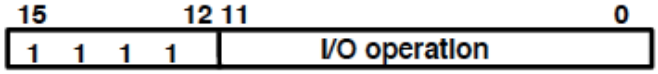
Memory-Reference Instructions (OP-code = 000 ~ 110)



Register-Reference Instructions (OP-code = 111, I = 0)



Input-Output Instructions (OP-code =111, I = 1)



Symbol	Hex Code I = 0	Hex Code I = 1	Description
AND	0xxx	8xxx	AND memory word to AC
ADD	1xxx	9xxx	Add memory word to AC
LDA	2xxx	Axxx	Load AC from memory
STA	3xxx	Bxxx	Store content of AC into memory
BUN	4xxx	Cxxx	Branch unconditionally
BSA	5xxx	Dxxx	Branch and save return address
ISZ	6xxx	Exxx	Increment and skip if zero
CLA	7800		Clear AC
CLE	7400		Clear E
CMA	7200		Complement AC
CME	7100		Complement E
CIR	7080		Circulate right AC and E
CIL	7040		Circulate left AC and E
INC	7020		Increment AC
SPA	7010		Skip next instr. if AC is positive
SNA	7008		Skip next instr. if AC is negative
SZA	7004		Skip next instr. if AC is zero
SZE	7002		Skip next instr. if E is zero
HLT	7001		Halt computer
INP	F800		Input character to AC
OUT	F400		Output character from AC
SKI	F200		Skip on input flag
SKO	F100		Skip on output flag
ION	F080		Interrupt on
IOF	F040		Interrupt off

memory reference instructions

register reference instructions

input-output instructions

interrupt initiated input-output = the device does not check input at each clock cycle, there is just another interrupt signal that shows if there is an input or not.

von Neumann architecture = program instructions and data in one memory (most of the computers)

harvard architecture = storage of instructions and data are separated in different memories (in embaded systems)

☆ when you write a program in high level language, it works in all processors, bc if you compile it, convert it to a machine language, it would be specific to the processor.

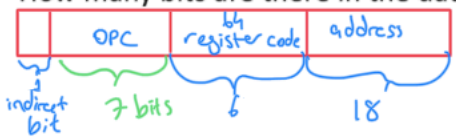
5.1 A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.

a. How many bits are there in the operation code, the register code part, and the address part.

b. Draw the instruction word format and indicate the number of bits in each part.

c. How many bits are there in the data and address inputs of the memory?

(b)



→ 32 bits

$256K = 2^8 \cdot 2^{10} \rightarrow 2^{18}$

32 − 25 = 7

(c) data → 32 bits

address → 256K = 2^n → n → 18

EX 1. A digital system has 16 registers, each with 32 bits. It is necessary to provide parallel data transfer from each register to each other register.

(a) How many lines are needed for direct parallel transfer?

(b) How many lines are needed for transfer along a common bus?

(c) Let the registers in memory be designated by R0 to R15. List the sequence of micro-operations for a transfer of the content of R6 to R13. (Assuming registers form a scratch-pad memory)

(a) 16 registers → for each of them connected with all → $16 \cdot 15 \cdot \frac{32}{2}$ ($n \cdot n-1$, each has) → 7680 → two ways connection

(b) 32 (for the bus) + 512 (16×32) from the bus to each register in bus system transfer is in two ways

(c) address of R6 → 0110

(memory address register)

MAR ← 0111 (R6)

MBR ← M (read content of the R6 into mbr) (memory buffer register)

MAR ← 1101 (address of R13)

M ← MBR (store in R13)