



Spintronics based random access memory: a review

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This article reviews spintronics based memories, in particular, magnetic random access memory (MRAM) in a systematic manner. Debuted as a humble 4 Mb product by FreeScale in 2006, the MRAM has grown to a 256 Mb product of Everspin in 2016. During this period, MRAM has overcome several hurdles and have reached a stage, where the potential for MRAM is very promising. One of the main hurdles that the MRAM overcome between 2006 and 2016 is the way the information is written. The 4 Mb MRAM used a magnetic field based switching technology that would be almost impossible to scale below 100 nm. The 256 Mb MRAM, on the other hand uses a different writing mechanism based on Spin Transfer Torque (STT), which is scalable to very low dimensions. In addition to the difference in the writing mechanism, there has also been a major shift in the storage material. Whereas the 4 Mb MRAM used materials with in-plane magnetic anisotropy, the 256 Mb MRAM uses materials with a perpendicular magnetic anisotropy (PMA). MRAM based on PMA is also scalable to much higher densities.

The paper starts with a brief history of memory technologies, followed by a brief description of the working principles of MRAM for novice. Reading information from MRAM, the technologies, materials and the physics behind reading of bits in MRAM are described in detail. As a next step, the physics and technologies involved in writing information are described. The magnetic field based writing and its limitations are described first, followed by an explanation of STT mechanism. The materials and physics behind storage of information is described next. MRAMs with in-plane magnetization, their layered material structure and the disadvantages are described first, followed by the advantages of MRAMs with perpendicular magnetization, their advantages etc. The technologies to improve writability and potential challenges and reliability issues are discussed next. Some of the future technologies that might help the industry to move beyond the conventional MRAM technology are discussed at the end of the paper, followed by a summary and an outlook.

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Introduction

We live in the era of information and social networks. Due to the advent of high performance computing and mobile devices with video cameras, enormous information is generated and stored. This is made possible due to the growth in the storage and memory technologies. Hard disk drives (HDD) with a capacity of 10 MB were sold for about \$5300 in the 1980s, and were unaffordable for many during Apple and IBM PC era. However, HDDs with 12 TB capacity (a million times larger capacity) are available at the time of writing (2017). The computers of the 1980s had memory of hundreds of kB. The growth in the memory is also close to a million-fold and most common computers have about 8 GB random access memory (RAM). Even mobile gadgets have a dynamic random access memory (DRAM) capacity of about 4 GB, at the time of writing.

Despite such a growth, dynamic RAMs (DRAMs) which are based on semiconductor technologies face limitations in maintaining a significant growth rate. The charge leakage that occurs when the device sizes are scaled down causes an increase in power consumption. A non-volatile memory would not consume much static power, in contrast with dynamic RAMs. Due to potentially lower power consumption and instant-on capability, a search for non-volatile memory technologies has been actively pursued for more than a decade. Magnetic random access memories (MRAM), which work on the principles of spintronics, are intensively being researched at this point as a replacement for several of the purely semiconductor based memory technologies. Spintronics based magnetic random access memories such as Spin Transfer Torque MRAM (STT-MRAM) [1–5] have already found their place in niche products as embedded memory.

Electrons have a charge and spin associated with them. While the conventional semiconductor electronics makes use of the charge property of the electron only, the spintronics devices makes use of the spin property of an electron. The use of magnetic materials in spintronics devices helps to store information, to provide non-volatility and to provide an endurance that is unmatched by other memory technologies such as resistive or phase-change memory. Making use of the spin nature of electrons provide new and effective ways to control the motion of electrons, which help in writing and reading information. More importantly, these mechanisms can be integrated on top of the conventional Si-based memory technologies. As a result, these memory devices have a huge potential. The aim of this review article is to introduce various types of current and emerging spintronics-based memory technologies. The unique nature of the review article lies in its tutorial format, explaining the basics and covering the breadth of this field to a non-expert in this field.

In Section “History”, a brief history of memory devices and their evolution is presented. Section “Working principle of MRAM” gives a description of the working principles of MRAM. The basics behind the three criteria required of a memory device, readability, writability and retention of data, are described briefly. The magnetoresistance effects, which enable reading of information in MRAM are presented in Section “Reading in MRAM: magnetoresistance”. Starting with the fundamentals of giant magnetoresistance (GMR), latest advances in tunneling magnetoresistance (TMR), which have enabled commercial MRAM products are

described in details. The methods of writing information in MRAM, such as magnetic field-assisted writing and STT based writing are discussed in Section “Writing methods for MRAM”. At first, the scalability problems of magnetic field-assisted writing and the advantages of STT-based writing are discussed. The focus is then shifted to storage layers. In Section “Storage methods and choice of materials”, storage layers having an in-plane magnetization and the problems faced by them are discussed first. The latter part of Section “Storage methods and choice of materials” explains the advantages of MRAM with perpendicular magnetization. Different materials, which are considered perpendicular MRAM are presented. Thermal stability, which is a key requirement to store the information for specific duration, is also presented. Section “Writing improvements” discusses writability limitations and methods to improve them. Several concepts such as nanocontacts, reference layer (pinned layer) with tilted magnetization etc., are covered. Section “Reliability issues of MRAM” discusses the reliability issues associated with MRAM. In Section “Emerging memories”, a discussion has been made about the emerging spintronics based memories, which might help in moving beyond the limitations of current MRAM and possibly become prominent in future. New writing schemes such as Spin Hall Effect and electric-field induced switching are discussed. New storage schemes such as multilevel MRAM, domain wall memory and Skyrmion based memory are also discussed. In the last section, a summary and outlook is provided.

History

The first electronic random access memory (RAM) was practically introduced with Williams Kilburn tube in 1947, which made use of electrically charged spots written on the cathode ray tube as bits [6,7]. This became the galvanizing point for the beginning of RAM's future, particularly as the electronic memories matched the speed of electronic components of a computer as compared to the slow mechanical memories prior to the invention of Williams Kilburn Tube [8]. However, this memory technology was not very reliable and did not last long. The magnetic core memories, where data was stored in the arrays of magnetic rings, emerged in the 1950s and lasted for two decades. The introduction of dynamic random access memory (DRAM) in 1968, based on semiconductor technology provided scalability, mass-manufacturing options and was compatible with the rest of the electronics in the then-emerging integrated chips. Hence, DRAM outshined the magnetic core memory and came into application for standard uses [9–20]. However, it is interesting to note that the magnetic based memory took about half-a-century to be seriously considered again as a product in the market.

The seeds for MRAM technology were sown in the 1960s, when it was suggested to replace the toroid of core memory with magnetoresistive elements [21]. Even though such MRAMs had an advantage of non-volatility, many issues have to be addressed before they could take over semiconductor memories. The research activities on MRAM surged again with the introduction of GMR in 1988 [22,23], and later in the 1990s, with the invention of magnetic tunnel junctions (MTJ) [24,25]. The possibility to achieve TMR at room temperature in excess of 50% increased the focus of research in this field as larger resistance results in

better signal, which enables easier detection of the written bits. However, the research in MRAMs declined again in the early 2000s, as it was realized that the technique of magnetic field-based switching was not scalable, viz., the technology is not extendable to small sizes, which would enable high-density MRAM applications. With the advent of the possibility to use STT effect to switch the magnetization, MRAM became a promising candidate again through a potentially faster switching capability, reliability, and scalability for future applications [26–32]. Because STT-MRAMs hold such a promising ability, the research activities on MRAMs resurged.

While MRAM has already found a niche market and is heading toward disruptive growth, there are also many other memory candidates proposed based on the principles of spintronics. Domain wall memory devices [33] and Spin-Hall/Rashba based memory devices [34,35] belong to this category of emerging memory technologies. Parkin et al. proposed domain wall memory devices in the early 2000s, as this technology could provide higher capacities as well as a faster access speed. The article will also briefly cover these technologies.

Working principle of MRAM

Magnetoresistive random access memory (MRAM) is a non-volatile and non-destructive read out memory, which is based on a magnetic anisotropy energy to retain information and the principle of magnetoresistance to retrieve information [36]. The writing and reading mechanisms have undergone various changes since the first proposal of MRAM in the late 1960s. Five decades later, only recently, MRAM was released as a memory for some niche applications. Researchers believe that MRAM could possibly replace Static Random Access Memory (SRAM) and DRAM as technology progresses.

Figure 1 shows an illustration of MRAM architecture. Arrays of several MRAM cells form a memory device. A typical MRAM cell has a transistor and a magnetoresistive element, quite similar to a DRAM, which contains a transistor and a capacitor. While the charge stored in the capacitor of a DRAM defines its memory

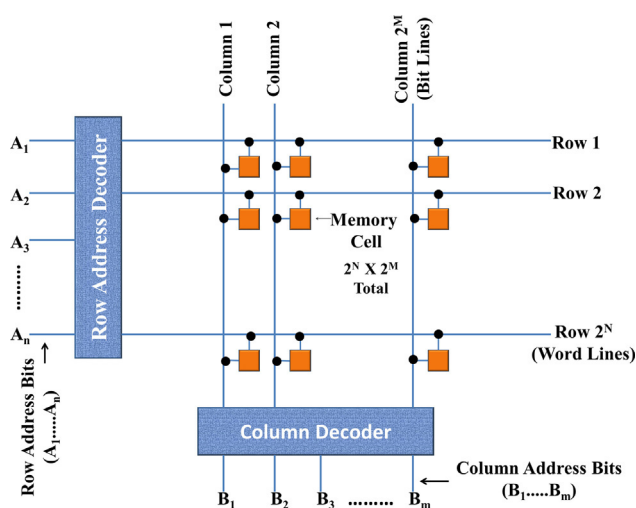


FIGURE 1

Schematic view of an array of MRAM cells in a typical memory architecture. The orange box typically includes a transistor and a magnetic tunnel junction element.

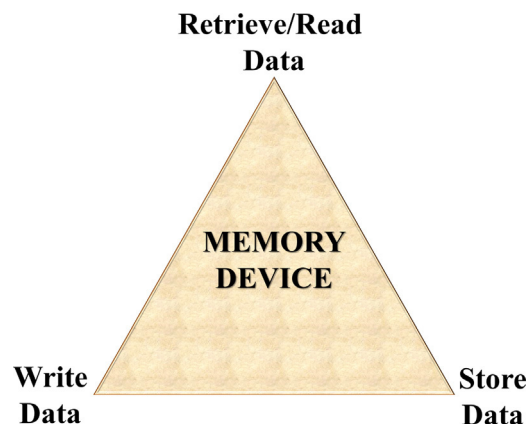


FIGURE 2

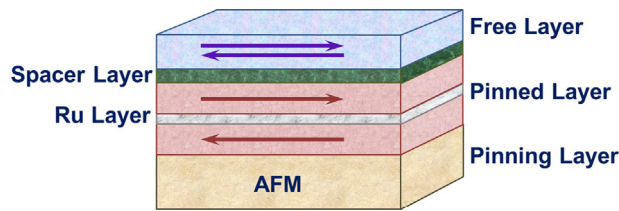
Three key requirements of a memory device.

state, the resistance of the magnetoresistive element determines 1 and 0 states. A transistor for every MRAM cell is required, as the absolute difference between the resistances and hence, the voltages of two states is not high enough to function without a transistor. Moreover, the transistor also provides the current required for the write operation.

As shown in Fig. 2, a memory device should follow at least three key requirements: (1) the proposed device should be able to store information. If the information is stored for long periods of time even without power, then it is called a non-volatile memory device; (2) there should be mechanisms to read information from the device and (3) there should be mechanisms to write information onto the device. To achieve these requirements in MRAM, researchers have designed and investigated various kinds of MRAM schemes in the past. In MRAM, these functions are performed as following: (i) The read operation is carried out by sensing the resistance difference between two states of a magnetoresistive device. (ii) The storage of information relies on the magnetic retention properties, arising from the magnetic anisotropy of storage layer. (iii) The write operation is performed by changing the orientation of storage layer magnetization, which can be achieved by inducing a magnetic field, or by using the principles of STT.

The first storage element used in MRAM for storing information was based on spin valve structure, which mainly consisted of two ferromagnetic layers sandwiching a non-magnetic conductive layer. The two ferromagnetic layers are called the free/soft layer and the hard/pinned layer, respectively. An antiferromagnetic (AFM) layer is used in proximity of or in contact with the pinned layer in order to pin the magnetization direction of the layer, which should not be reversed during the operation of the memory device. For better functionality of the memory device, the pinned layer (PL) is made of two antiferromagnetically coupled layers to reduce the stray field, which may affect the free layer (FL) stability. Although a pinned layer is mainly used in in-plane MRAM, we use pinned layer to refer to the fixed layer or reference layer of a perpendicular MRAM.

In MRAM designs, which involve a synthetic antiferromagnetic layer, the antiferromagnetic coupling is induced by a thin ruthenium layer as shown in Fig. 3. The ruthenium layer induces a strong antiferromagnetic exchange coupling between the two

**FIGURE 3**

Schematics of spin valve structure used in read-sensors of hard disk drive and in the initial investigations of magnetic random access memory.

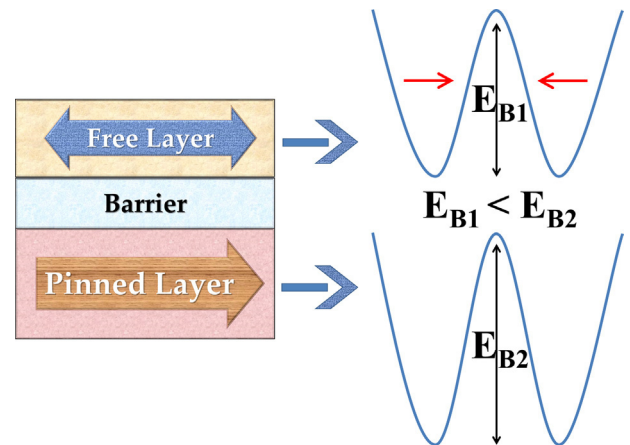
magnetic sub-layers [37]. As a result, the synthetic antiferromagnetic layer helps to cancel out the magnetostatic field from the pinned layer onto the free layer [38–40]. Although the spin valve devices had been used for the earlier MRAM memory research studies, they still suffered from their low reading signal.

With the high reading signal found in MTJ, research interest in spin valves decreased strongly. The MTJ structure is similar to spin valves, except that the non-magnetic spacer is replaced by an insulating layer, which is also called as tunnel barrier. MTJ is the predominant storage element in MRAMs for the past decade. The current MRAM products use MTJs because the difference between the resistance states is significant enough to produce the voltage swing required for application. An MTJ cell consists of a thin layer of an insulating material, sandwiched by two magnetic layers (pinned layer and free layer). Similar to a spin valve, the resistance states can be high (antiparallel orientation) or low (parallel orientation) based on the relative orientation of magnetizations of pinned layer and FL. The writing mechanism, to change the relative magnetization orientations in the MTJ, is explained in Section “Writing methods for MRAM”.

A memory device should provide at least two states ‘bit’, so that they can be assigned to digital signals of ‘0’ and ‘1’, respectively. In the case of spin valves and MTJs, the resistance states of these devices are different when the magnetizations of the two magnetic layers are aligned parallel (low resistance) or antiparallel (high resistance) to each other. These observations in spin valves and MTJs are called GMR and TMR, respectively. These mechanisms are discussed in details in Section “Reading in MRAM: magnetoresistance”.

The storage principle of an MRAM is based on the energy barrier required to switch the magnetization of a single-domain magnet from one direction to the other (Fig. 4). The magnetization will be fixed in a particular direction, if the energy barrier for magnetization reversal is high enough to overcome the external stray fields and the thermally assisted reversal of magnetization. This storage principle is very similar to that used in magnetic recording, although the way the materials are designed and the information is written, are different.

In an MRAM, the magnetization direction of the reference layer (or PL) is fixed and only the magnetization direction of the free layer (FL) varies to store ‘0’ and ‘1’ states. Since the direction of the reference layer must never be changed, it is made of materials, which have a huge energy barrier. The free layer is designed with materials that have a magnetic anisotropy, just sufficiently high enough to store the magnetization for certain years (typically 10 years in the case of magnetic

**FIGURE 4**

Relative energy barriers of free layer and fixed layer in a magnetic tunnel junction. Both E_{B1} and E_{B2} are much larger than the thermal energy $k_B T$.

recording). The energy barrier that helps to store the information is typically proportional to $K_u V$ (where K_u is the magnetic anisotropy constant and V is the volume of the free layer). This energy must be much larger (60 times, for storage time longer than 10 years) than the thermal energy $k_B T$. In certain cases, the energy barrier E_B may be different from $K_u V$ and hence, the thermal stability factor is simply written as $\Delta (=E_B/k_B T)$. Although a high anisotropy is preferred for storing information, the anisotropy of these materials cannot be too high, as their magnetization direction needs to be oriented at will, to write 0 and 1 states. Based on the storage mechanism, the MTJs may be classified into two types; (i) in-plane MTJ, which has magnetization of ferromagnetic layers in the film plane and (ii) perpendicular MTJ having the magnetization perpendicular to the film plane [41].

Reading in MRAM: magnetoresistance

As discussed in the previous section, being able to read information is one of the three important criteria. The magnetoresistance (MR) effect is the key to read information reliably. The voltage difference between the low resistance state and the high resistance state must be above 0.2 V, in order to read the information reliably. Therefore, it is essential to achieve a high magnetoresistance to make the MRAM more reliable. This section talks about the magnetoresistance in detail.

W. Thomson first observed magnetoresistance in pieces of iron and nickel in 1856. His observations were based on the changes in the resistance of iron and nickel, when the orientation of magnetic field was altered [42]. The MR effect arises due to the spin–orbit coupling. The change in orientation of magnetization deforms the electron cloud slightly, resulting a change in the amount of scattering of conduction electrons traveling across the lattice. This change leads to different resistance values when the orientation of magnetizations is different. The MR effect depends on both strength and relative direction of the magnetic field. MR effect has also been reported in non-magnetic materials like In, Al, Sb, Mo, Cu, Au, Pt, and others, but it is saturated at different specific conditions [43]. In materials like ferromagnets, MR effect of 2% order has been reported and it is anisotropic in

nature. Hence, it is called anisotropic magnetoresistance (AMR) effect. The AMR of Permalloy (NiFe) was used in the earlier generation of magnetoresistive heads of hard disk drives, due to its relatively large effect at room temperature and low saturation fields, in comparison to the inductive head technology [44–46]. The change in resistance in polycrystalline ferromagnets like (Ga, Mn)As depends on the angle between the magnetization and current density [47].

The magnetoresistance value got a significant enhancement, when sandwich structures containing ferromagnetic (Fe) layers and a thin non-magnetic film (Cr) were investigated. This new effect that caused an enhanced magnetoresistance is known as GMR effect, and was discovered by Albert Fert and Peter Grünberg independently in the late 1980s. The application of GMR in the reading head made a revolutionary change in the hard disk drives as a high GMR lead to a high reading signal. Albert Fert and Peter Grünberg received Nobel Prize in Physics (2007) for this effort.

The enhanced or so-called ‘giant’ magnetoresistance effect is a consequence of spin dependent scattering. When the magnetizations of two layers of neighboring magnetic layers are aligned in anti-parallel direction, both the minority and majority electrons get scattered (Fig. 5). As a result, a high resistance is observed. However, a drop in resistivity is observed when the magnetic orientations of ferromagnetic layers are parallel to each other. This is because, for parallel orientation of magnetization, the majority electrons scattered less in comparison to the minority electrons.

The GMR effect also has been observed in multi-stacked films like Co/Cu, Ni/Fe, Fe/Au and others. The Co/Cu and CoFe/Cu show high MR [22,23,48–53]. Although GMR was an interesting observation, it was not directly applicable to hard disk drives, as the effect requires a field larger than those produced by a magnetic medium. The invention of spin valves (discussed in Section “Working principle of MRAM”) helped to solve the problems of GMR and made spin valve a suitable magnetoresis-

tive device for hard disk applications. In case of materials like Heusler alloys, the maximum GMR of 61% was observed in the ballistic Co/H₂Pc/Co junction [54]. Although, the practical GMR observed for reading head application has remained about 10–20% [55,56]. This change was not significant enough to produce a significant voltage difference between the high and low resistance states. Therefore, GMR is not of practical interest in MRAM applications.

TMR, which was first reported at room temperature by Moodera et al. and Miyazaki et al. in 1995, was a major boost for MRAM applications [24,25]. They reported TMR values of about 16% at room temperature, which was very high at that point of time. Moreover, the fact that the TMR was reported at room temperature was a great leap. The amorphous AlO_x was the insulating layer that they used in the magnetic tunnel junction [24,25,57]. Since then, several developments such as the use of MgO crystalline barriers have occurred, resulting in the observation of TMR values more than 600% in laboratory demonstrations. At the point of writing, TMR values of 100–200% are readily achieved in MRAM devices, which provide sufficient voltage difference between 0 and 1 states.

In an MTJ for TMR, two ferromagnetic layers sandwich a very thin insulating film, typically a few atomic layers thin, so that electrons can tunnel through the insulating layer depending on the available free electron states on the ferromagnetic layer. In the advanced MTJ devices with MgO tunnel barrier, the TMR also depends on the band matching nature of the interfaces. Unlike GMR, where the resistance is caused by spin-dependent scattering, the resistance difference in TMR is caused by spin-dependent tunneling. When the magnetizations of the layers are aligned parallel, more majority electrons tunnel through the barrier. However, when the magnetizations of the layers are aligned antiparallel, the probability of tunneling for both the majority and minority electrons is reduced, resulting in a higher resistance. The resistance difference of different magnetic orientations is measured by the TMR ratio, which can be calculated by the following:

$$\text{TMR ratio} = \frac{R_{ap} - R_p}{R_p} \quad (1)$$

where, R_{ap} and R_p are the resistances of the device, when the free layer and reference layer magnetizations are antiparallel and parallel, respectively.

The insulating barrier in the MTJ and the design of the whole stack, decide the TMR and the reading performance of an MRAM. In the case of an amorphous barrier, such as AlO_x, the tunneling depends mainly on the electronic band structure of the ferromagnetic materials. A maximum value in TMR of 70% was achieved using AlO_x [58]. However, when crystalline barriers such as MgO, with crystalline and band matched magnetic materials such as Fe were used in an MTJ, the tunneling depends on electronic band matching. Consequently, majority electrons have a larger probability of tunneling for parallel magnetization. However, for antiparallel magnetization orientation, the probability of tunneling is very low for majority and minority electrons. This effect was theoretically predicted by Butler and J. Mathon and A. Umerski independently in 2001 [59] and the experimental results, which involve MgO started pouring in

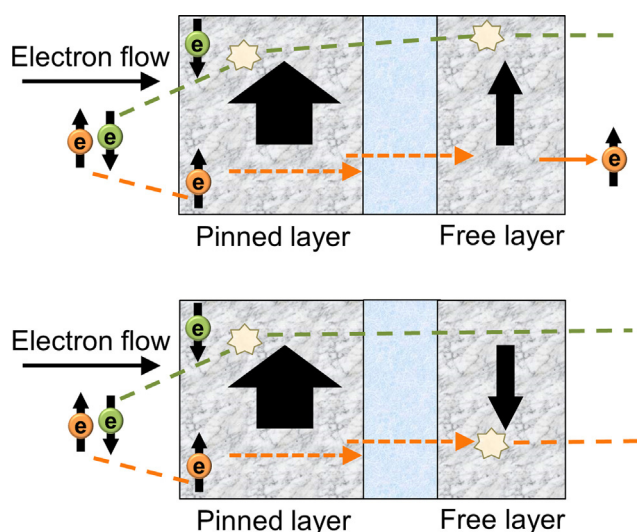


FIGURE 5

Illustration of spin dependent conduction in spin valve. The bold arrows indicate magnetization states of pinned and free layers. The arrows with e indicate the electron spins. The scattering of electrons is higher when the magnetizations of the two layers are aligned in antiparallel directions.

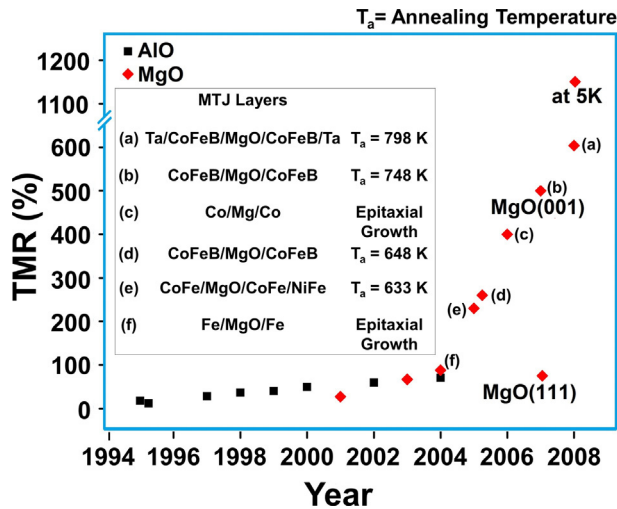


FIGURE 6

Evolution of tunnel magnetoresistance (TMR) (%) from Refs. [24,25,66–73], (a) [64], (b) [65], (c) [74], (d) [62], (e) [61], and (f) [75]. Slower growth was observed in the case of amorphous barriers such as AIO. The rapid growth in TMR has occurred since the introduction of crystalline barriers such as MgO with band-matched structures (red symbols).

the middle of the 2000s [60–62]. Yuasa et al. and Parkin et al. showed that the TMR of MgO based MTJs can be greater than that of AlO_x barriers [60,63]. In the same year, Djayaprawira et al. demonstrated TMR ratio higher than 200% in CoFeB/MgO/CoFeB MTJ [61]. The TMR achieved using MgO gradually increased to record high values of about 1000% at low temperature [64,65] (Fig. 6).

Designing of MTJ is crucial in achieving a high TMR. In the case of MTJs with MgO crystalline barrier, it is essential that the MgO layer has a (001) texture. This crystallographic texture provides the band matching and the highest TMR. It is also essential to design the magnetic materials at both sides of the MgO layer to have a (001) texture. In the fabrication of MTJ stack, the most common interface is of the type CoFeB/MgO/CoFeB. The CoFeB layer is amorphous in the as-deposited condi-

tion. When MgO is deposited on such an amorphous layer, it develops a (001) texture under suitable deposition conditions. However, one needs a crystalline interface for high TMR. To achieve a crystalline CoFe with a (001) texture, the MTJ is annealed at a temperature of about 300 °C. During the annealing, B migrates out of CoFeB layer and the MgO (001) texture helps to achieve a (001) texture in CoFe. When forming the MgO based MTJs, one must be careful to avoid CoFe(111) texture. The presence of CoFe layers with a (111) texture has been shown to reduce TMR [65].

Writing methods for MRAM

The second requirement of the memory device is that there should be a method to write data in the memory cells. The writing in MRAM has been evolving and is achieved using different methods in the past and in the recent past. One of the oldest methods used to write information is based on applying a magnetic field, generated by current carrying wires. According to Biot-Savart law, a current carrying conductor will generate a magnetic field. This principle was used until a decade back, to achieve writing (also called switching of magnetization or simply switching). In this method, the MRAM architecture consists of bit line and word line (Fig. 7). When a current is sent through the bit line and word line corresponding to a particular MRAM cell, two magnetic fields are produced orthogonal to each other (Fig. 7(a)). The current in the word line generates a magnetic field H_W along the easy axis, and the current in the bit line generates a magnetic field H_B in transverse direction to the easy axis. Since field-assisted MRAMs were developed with in-plane magnetization, the easy axes in such MRAMs lie along the longer axis of the ellipsoid cells. It is worthy to mention that STT-MRAM architecture (to be discussed next) is simpler than that in the case of magnetic field based switching.

Under the Stoner–Wohlfarth switching mechanism, the threshold field required for resulting in magnetic field switching is given by

$$H_W + H_B = H_K^{2/3}. \quad (2)$$

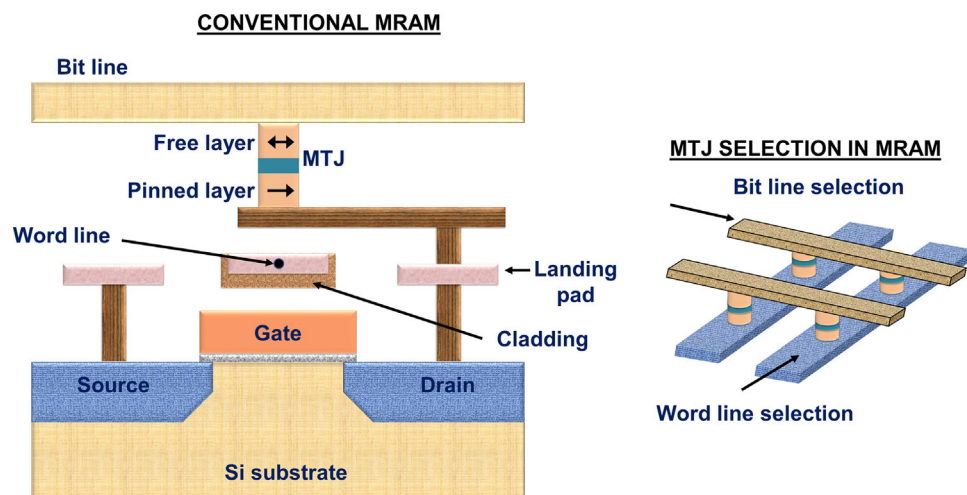


FIGURE 7

Schematic of conventional MRAM based on magnetic field induced writing and the selection process involved in the selection of a particular MRAM cell. Only the free layer of selected MRAM cell will switch, due to a higher applied total magnetic field.

where H_K is the anisotropy of the single domain magnet under consideration (in the case of MRAM, the free layer part of the MRAM cell) [76]. The magnetic state of the free layer changes, when the resultant field strength exceeds the switching threshold (H_K). It can be noticed from this equation, for H_W or H_B not exceeding H_K , that the switching occurs only when the magnetic fields from both the currents are present and together they exceed H_K , satisfying Eq. (2). This helps in the selection of the preferred MRAM cell and in preventing the other cells from spontaneous switching (i.e., undesirable erasing of other data) [77].

The current required for generating the magnetic field depends on the magnetic and morphological properties of the storing element. The switching field is inversely proportional to the area of the storing element. As a result, scalability toward smaller dimensions becomes a problem, since a higher current is needed to achieve a higher switching field. The scalability of field-assisted MRAM is limited to about 90 nm, due to a larger current requirement to induce the magnetic field in small cross section of wires [41,78].

MRAM was almost given up by several researchers for a short while, as the field-based switching was found to be not scalable to smaller dimensions and there was no clear indication of an alternative. Thermally assisted MRAM, which relies on the joule heating and exchange coupling between an antiferromagnetic material and a ferromagnetic material to improve thermal stability was proposed in 2000s [79,80]. This technology is still being pursued by a few groups, although STT based switching is much widely being researched.

Nevertheless, the proposal on STT based switching for MRAM revived the research interest and the subsequent commercial interest [81–84]. It is surprising that the proposal of STT-MRAM took almost a decade, even though the theoretical predictions were made independently by Berger and Slonczewski in 1996 [26,27]. The STT switching in magnetic nanopillars was first experimentally observed by Katine et al. in 2000 [28]. The first few proposals on STT-MRAM appeared in 2006 [85–87].

As shown in Fig. 8(b), STT method does not require any external magnetic field to switch the state of magnetization. Rather, the switching of magnetizations is induced by sending a current through the device. Interestingly, switching by current is scalable (Fig. 9), which also simplifies the MRAM design (Fig. 10), and

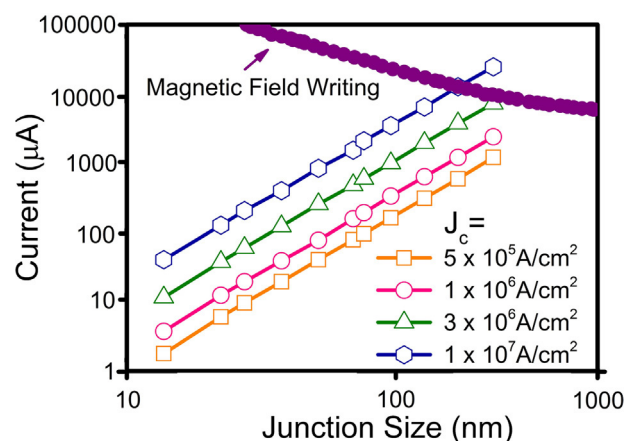


FIGURE 9

Required writing currents for switching of free layers in different types of MRAMs for different cell sizes. The current required in the case of field MRAM increases when the cell size decreases whereas that required by STT-MRAM decreases with cell size [65].

hence, the fabrication process as well. In the STT switching process, electrons are sent from pinned layer to free layer, if the magnetization direction needs to be changed from antiparallel to parallel. When the electrons flow through the pinned layer, the minority electrons get scattered and the majority electrons pass through to the free layer. This process of selectively transferring one type of electrons as the majority is called polarization. When these polarized electrons reach the free layer, the spin angular momentum exerts a torque on the magnetization of the layer that is oriented antiparallel to the pinned layer as shown in Fig. 10(a). As the result of this torque generated by several electrons, the magnetization changes from antiparallel direction to parallel direction.

When it is required to achieve an antiparallel magnetization configuration, the current direction is reversed. In this case, the electrons are sent from the free layer toward the pinned layer. The majority electrons pass through the interface and the minority electrons are scattered back to the free layer. The transfer of spin angular momentum between the reflected electrons and the magnetization results in an antiparallel magnetization con-

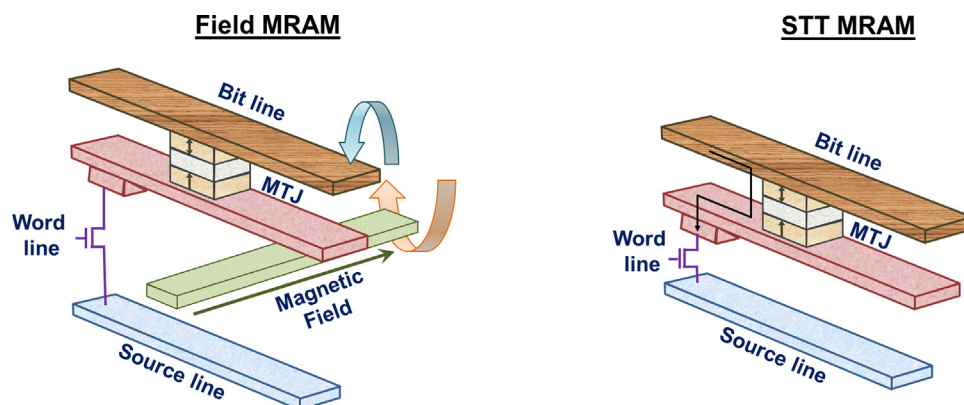
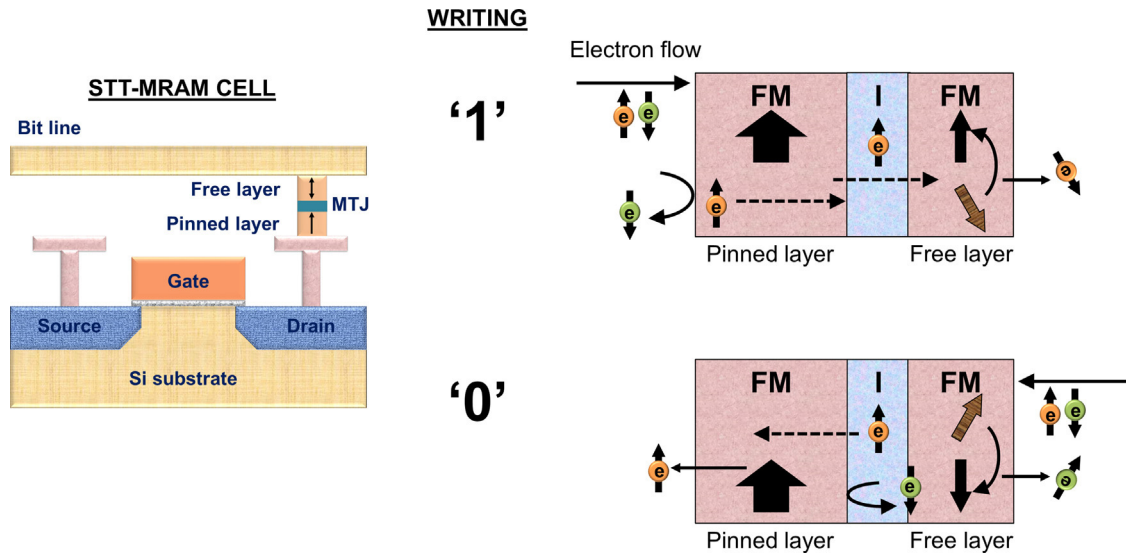
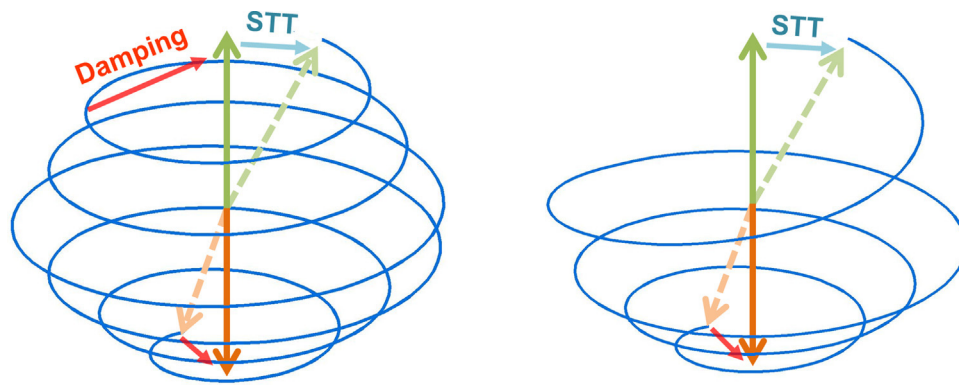


FIGURE 8

A comparison of the architecture of MRAMs with (a) field induced switching (b) Spin Transfer Torque (STT) switching. In STT switching, the current is sent through the MTJ and the resultant structure is much less complex than that of field MRAM.

**FIGURE 10**

Schematic illustration of an STT-MRAM cell and the STT switching mechanism to achieve 1 and 0 states. The bold arrows indicate the magnetization states of the pinned and free layers. The arrows with e indicate the electron spins.

**FIGURE 11**

Precession of the spin in switching state for (a) $J = J_c$ and (b) $J > J_c$. The blue line shows the trajectory and the bold arrows show the initial and final states of magnetization. The dotted arrows show an intermediate state of magnetization.

figuration (Fig. 10(b)). The magnetic state of free layer changes only when the torque is strong enough. If the current is not enough, the magnetization may rotate and revert back to its initial state. If the current is very large, the reversal may happen at a faster rate, but this leads to a significant power consumption (Fig. 11). The critical current J_c is needed to reverse the magnetization of the free layer and the critical current density J_c is given by [26]

$$J_c = \left(\frac{\alpha}{\eta} \right) \left(\frac{2e}{\hbar} \right) M_s t H_K + 2\pi M_s \quad (3)$$

where M_s is saturation magnetization, t is thickness of the film, and α is the Gilbert damping constant, which represents the rate at which the magnetization relaxes to its equilibrium position. The parameter η in above equation is the STT efficiency parameter, which is related to the spin polarization of the injected current.

Storage methods and choice of materials

Based on the storage methods, MRAMs can be classified into two categories: (1) in-plane MRAM and (2) perpendicular MRAM. In

the case of in-plane MRAM, the magnetizations of the reference and the free layers lie in the film-plane. In the case of perpendicular MRAM, the magnetizations of the reference and the free layers lie perpendicular to the film-plane. In this section, we will discuss details of these two types of storage principles, materials and their advantages and disadvantages for MRAM application.

In-plane MRAM

In the earlier generations of MRAM and until recently, the storage layers used in MTJ devices are in-plane magnetized. The main advantage of in-plane MRAMs are that they are relatively easy to manufacture than their counterparts. Another reason for using materials with in-plane magnetization was that the magnetic field produced in the field-switching MRAMs were in-plane magnetic fields. Such fields are able to switch in-plane magnetizations. The disadvantage of in-plane MRAM is that they are not scalable to very high densities. This is mainly due to a continuous increase of the magnetostatic field as the device lateral size shrinks. It is believed that this trend of using in-plane MRAM will continue only for a few more years.

During early research on MRAM, materials such as Fe, NiFe, Co and CoFe were used in the in-plane MRAM design. These materials when miniaturized, exhibits magnetization curling at the edges of the films. This magnetization curling leads to the formation of vortex magnetization in the films. In order to prevent this vortex formation, the aspect ratio (length/width) of these films was designed to be more than or equal to 2. The aspect ratio also provides a direction for the easy axis of magnetization along the major axis, due to shape anisotropy. However, due to scalability concerns, MTJs with elliptical shapes are not desired as they take larger space than circular dots and hence, decrease the density of MRAM [88–90]. The curling of magnetization also causes the problem of anomalous switching in in-plane MTJ [91–93].

In the current technology, CoFeB is used as the free layer in an MgO based MTJ. As discussed earlier, thermal stability of STT-MRAM is a very important factor for its functionality and long lasting performance. The data retention probability of MRAM depends on the thermal stability of the MTJ. The thermal stability factor $\Delta = E_b/K_B T$, must be greater than 60 for retaining data for more than 10 years. For the uniform rotation of magnetization, the energy barrier E_b is the anisotropy energy ($K_u V$), where K_u is the uniaxial anisotropy constant and V is the volume. Furthermore,

$$K_u = H_K M_s / 2 \quad (4)$$

(where H_K is the anisotropy field and M_s is the saturation magnetization of the free layer). The thermal stability factor can be defined as [24,25,79]

$$\Delta = \frac{H_K M_s V}{2 k_B T} \quad (5)$$

For a storage life of 10 years, it is essential to have Δ of about 60, which results in a cell diameter of 60 nm as the ultimate size for in-plane MRAM for materials such as CoFeB, with a thickness of 5 nm and a K_u of about 8×10^4 ergs/cc. For sizes smaller than 60 nm, it is essential to look at perpendicular MRAMs.

Besides the thermal stability of the free layer, it is also essential to achieve the thermal stability of magnetization of the reference layer. However, the magnetization of the reference layer has to be fixed at all times and it is not necessary to reverse its direction. Shape anisotropy, associated with cylindrical shaped dots is one way to achieve a higher anisotropy and coercivity for the reference layer. However, the achievable density is not so high with this technique. Therefore, exchange bias is used as a technique to pin the direction of the magnetic layer [94]. For this purpose, an antiferromagnetic layer such as IrMn is deposited in contact to the reference layer. A magnetic field annealing is carried out to pin the direction of magnetization of pinned layer. To achieve exchange bias, the sample is annealed at a temperature above the blocking temperature (T_B) of antiferromagnetic layer and below the Curie temperature (T_C) of the ferromagnetic layer. At this temperature $T_B < T < T_C$, the antiferromagnetic material does not have its anisotropy but the reference layer does have its magnetic ordering. When a magnetic field is applied and the sample is cooled from this temperature, the magnetization of the reference layer is oriented along the magnetic field direction. The magnetic moments of the atoms of the antiferromagnetic layer

in contact with the magnetic layer are also frozen in this direction. As a result, the exchange coupling of the antiferromagnetic layer is also set along this direction.

Devices fabricated using in-plane anisotropy materials for MRAMs have been sampled since 2012. However, thermal stability of in-plane MTJ for devices smaller than about 60 nm forces researchers to look for alternative technologies that will enable smaller devices. As a result, the future of in-plane MTJ structure in MRAM is limited and there is a growing research in MTJs with a perpendicular anisotropy.

Perpendicular MRAM

In the past decade, there has been significant amount of research in the field of MTJs with a perpendicular magnetization (pMTJ). It has to be noted that the transition from longitudinal to perpendicular magnetic recording technology for hard disk drives took place, when it was practically impossible to push the density of longitudinal recording technology. Similar transition is expected to take place in MRAM, too, when it is not practically viable to scale the current products based on in-plane MTJs.

A perpendicular magnetic anisotropy (PMA) enables magnetization to remain in the direction perpendicular to the film-plane, whereas the magnetization direction for a film without PMA is in-plane. Moreover, most films with a PMA have been found to have a higher anisotropy constant. There are also additional benefits in writing mechanism, arising from a PMA configurations. As a result, the research on PMA has been growing in the recent past. The first few publications that advocated and demonstrated the use of PMA configurations for MRAM applications are based on well-established PMA materials once used in/considered for magneto-optic recording. A higher TMR ratio of 50% in perpendicular MTJ with GdFe/CoFe layers, as compared to the in-plane MTJ was reported by Nishimura et al. [95]. Alloys of transition metals like TbFeCo, GdFeCo were also adopted to obtain PMA. However, these materials have drawbacks in the form of corrosion. The oxidation of these materials is unavoidable, which results in deterioration of magnetic properties and hence, it is a challenge to use such materials [95,96].

Transition metals like Co, Fe, when formed as multilayers in combinations of noble metals such as Pt, Pd, Au show PMA. For example, these layers can be used together as (Co/Pd)_m, (Co/Pt)_m, (Co/Fe)_n and (Co/Ni)_n where n is the number of sets of bilayers. These multilayers possess large value of PMA close to 10^7 erg/cc [97–100]. The CoPd multilayers have been used with FeMn as an AFM layer to induce exchange bias constituting a structure, which was similar to the conventional in-plane spin valve [101]. Another structure called pseudo spin valve without any AFM layer was demonstrated later, where the coercive properties of these films can be tailored by altering the thickness of Co and Pd, and the number of periods. Even though the Co/Pd or Co/Pt multilayers could be used as pMTJ candidates, they have two significant issues, when they are used as free layers. (i) Their anisotropy and the damping factor is very high, the writing current would be also high as can be revealed from Eq. (3) and will be discussed in next section. (ii) They have an fcc (111) structure. As a result, when MgO is grown on them, the MgO layer would not achieve the desired (001) texture and hence, the achieved

TMR would be low (Fig. 5). A breakthrough was needed to realize the advantages of PMA in MRAM and it came in the form of thin CoFeB layers.

It was surprising that the CoFeB, which was predominantly used for in-plane MRAMs provided the much needed breakthrough for the pMTJs as well. It was pointed out in 2010 that MTJs based on CoFeB-MgO could show PMA when the thickness of CoFeB layers is smaller than 1.5 nm, whereas for films thicker than that value in-plane anisotropy is observed as usual [102]. It has been pointed out that both Ta and MgO are crucial to achieve the interface anisotropy. Replacing Ta with Ru or other such material did not yield promising results [103]. The crystallized pMTJ system with CoFeB-MgO has shown TMR of more than 100%. The demonstrated film also exhibits good thermal stability and low switching current. The annealing process is a crucial step for PMA of the CoFeB layer to get good TMR, low resistance and low critical current density [104]. The TMR value of CoFeB degraded as the thickness of CoFeB decreases, so the optimization of the film thickness is also required for better STT-based switching. It is widely believed that the first generation of pMTJs will be made using thin CoFeB based MRAMs.

Thermal stability

Irrespective of whether Co/Pd multilayers or the thin CoFeB based MTJs are used for MRAM applications, the thermal stability of magnetization is important to store the information for longer periods without self-erasure. In the case of pMTJs, a free layer with an anisotropy constant in the order of 1×10^7 erg/cc is required for future. For a thickness of about 5 nm, such material can support cell diameter around 10 nm, at operating temperatures of about 70 °C.

For perpendicular MTJs, the anisotropy arises from different sources and there are several notations describing each contribution. When the PMA arises from a magnetocrystalline anisotropy, this is denoted as the bulk anisotropy energy density K_u^{bulk} . If the anisotropy arises from interfacial effects, this is called as surface anisotropy energy density σ . It must be noted that the densities are with respect to volume and area in the case of bulk and surface anisotropies respectively. The shape anisotropy energy density K_D , arising from the geometrical shapes of the devices, goes against the PMA and tries to keep the magnetization in-plane. For the non-patterned films and large devices (about a μm), K_D is given by $K_D = -2\pi M_s$. The value of H_K that is anisotropy field also varies for different types of PMA.

For bulk-PMA, the anisotropy field is given by,

$$H_K = \frac{2K_u^{bulk}}{M_s} - 4\pi M_s \quad (6)$$

For interfacial-PMA, the anisotropy field is given by,

$$H_K = \frac{2\sigma}{M_s t} - 4\pi M_s \quad (7)$$

By using the above equations the thermal stability factor Δ for PMAs can be written as follows:

For materials with a magnetocrystalline anisotropy,

$$\Delta = (K_u^{bulk} t - 2\pi M_s t) \frac{\pi A R \omega^2}{4 K_B T} \quad (8)$$

For materials with an interfacial anisotropy,

$$\Delta = (\sigma - 2\pi M_s t) \frac{\pi A R \omega^2}{4 K_B T} \quad (9)$$

where AR is the aspect ratio (length to width), ω the width and t the thickness of the cell [32,102,105].

For in-plane cells of elliptical shape, the anisotropy field is given by

$$H_K = 2 \frac{4\pi M_s (AR - 1)}{\omega AR} \quad (10)$$

and Δ is given by

$$\Delta = \frac{\pi^2 (M_s t)^2 \omega (AR - 1)}{K_B t} \quad (11)$$

In essence, in MRAM devices based on materials with a PMA arising from magnetocrystalline anisotropy (bulk), the thermal stability can be increased by simply increasing the thickness of the film (for a fixed diameter). However, in the case of PMA based on interface anisotropy, it is not possible as the interface anisotropy is the major factor in thermal stability. Any increase in thickness, leads to a reduction in thermal stability as per the second term of Eq. (9) and also the loss of PMA.

One way to overcome the thermal stability issues of interface PMA based MTJs is to find out alternatives, such as multilayers, which would increase thermal stability with thickness. CoFeB/TaN based multilayers have been proposed as potential candidates [106]. Another possibility is to use dual interfaces, such as MgO/CoFeB/Ta/CoFeB/MgO, instead of Ta/CoFeB/MgO alone. In such dual-pMTJs, both the layers of CoFeB are sandwiched by a layer of Ta and MgO and hence, both develop a perpendicular magnetic anisotropy. As the thickness of each layer can be about 1 nm each, the thermal stability is increased. Sato et al. have reported the increase of thermal stability in such double interface structure by a factor of 1.9 from the highest value of perpendicular MTJs with single CoFeB-MgO interface structure [107].

To increase the storage density, multi-level MRAM has been reported using complex magnetoresistive spin valve with perpendicular anisotropy [108]. The structure consists of two free layers and one reference layer, all based on Co/Pd multilayer exhibiting different four resistance levels. The selection of free layer for storing data can be done by distinct level of resistance and their respective STT switching current [109].

Writing improvements

As discussed earlier, STT principle has been widely accepted as the method to write information. Any new methods implemented in the design of MRAM must improve the writing speed, reduce the writing current and consumption of power. This section discusses, in detail, the methods in which writability or speed can be increased.

Eq. (3) indicates that the critical current to switch the magnetization of the free layer depends on the damping factor α . Therefore, it is essential to find materials that have a low damping factor, in order to reduce writing current. Materials such as FePt or Co/Pd, which were once researched for pMTJ applications due to their high K_u , have a large damping factor. Therefore, even though these materials could be scaled down to smaller devices with high thermal stability, writing information on these devices

would consume significant power. In this context, the invention of interface-pMTJ based on Ta/CoFeB/MgO came as a boon for the STT-MRAM. CoFeB has a much lower damping factor and could be written with much lower currents, as compared to FePt or Co/Pd. Interface-pMTJ devices could be used down to 20 nm sizes, beyond which one may consider materials such as Co/Pd, Co/Pt or FePt, although the writing issues on such materials should be solved. It is important to mention that Co/Pd or Co/Pt multilayers have to be used in combination with other materials such as CoFeB for example for better matching with MgO in term of crystal structure.

Another way to reduce the writing current in STT-MRAMs is to increase the STT efficiency (η denominator in Eq. (2)). One way to improve the STT efficiency is to increase the spin polarization of the materials used. CoFeB with a reasonably high spin polarization is used at the interfaces of MTJ, even if materials such as Co/Pd are used as the reference layers. Heusler alloys, with a much higher spin polarization, are also being research as future candidates [110]. η can also be increased by using dual MTJs with two reference layers and one free layer [111]. An MTJ with double tunnel barrier and two reference layer was reported by Hu et al. [112]. η was reported to improve by two folds as compared to a single MTJ with same resistance-area product (RA).

Orthogonal spin-transfer magnetic random access memory (OST-MRAM) has been proposed to increase the speed of magnetization reversal. This technology uses a spin-polarizing layer magnetized perpendicularly to a free layer to achieve large spin-transfer torques and ultrafast energy efficient switching. Reliable switching has been observed by the researchers at room temperature with 500 ps pulses, indicating high-speed switching in the range of 2 GHz. The switching has been reported to require an energy of less than 450 fJ [113,114].

Magnetic nano-contacts are another alternative to increase writing efficiency. Sbiaa et al. studied the STT switching in perpendicular free layer with magnetic nano-contacts and found a strong dependency of switching time on the size of nano-contact, as the time reduces from 1.6 ns to 0.8 ns by decreasing the size of the nano-contact. The value of critical writing current and switching time was found to be less for fewer numbers of nano-contacts compared to those with larger number of nano-contacts [115].

The tilting of the free layer with respect to the reference layer in perpendicular MTJ can also increase the writing performance of MRAM in terms of switching time and switching current [116]. As reported, for a tilt angle of 5°, switching speed of free layer is improved by 30% and switching current is reduced by 36%. The critical current density reduced from 5% to 30% as tilted angle increased from 1° to 5°.

Fast switching speed is one of the advantages of STT-MRAM. In comparison to its rivals such as resistive RAM or phase change RAM, the STT-MRAM is about 100× faster. The switching speed is directly proportional to the switching current and inversely proportional to the RA. Therefore, it is essential to reduce RA in order to improve the speed of MRAM. RA is usually reduced by making thinner MgO barriers. However, this must be achieved without sacrificing the tunneling magnetoresistance. High switching speed can also be achieved by applying high switching current I_c , which is achieved by a high bias voltage applied across

the device. It has been reported that the combination of both (high current and a thinner barrier layer) can result in the breakdown of the AlO layer limiting the lifetime of MTJ [41]. The MgO layer, used in current products, is more advantageous compared to AlO, as it has a higher breakdown voltage, which increases the lifetime of the MTJ. Moreover, MgO is highly spin selective, which results in a large STT and TMR effect, and it induces very high perpendicular magnetic anisotropy (PMA).

The Damping factor α , plays a major role in the switching speed of the devices. When a magnetic field or spin torque current is applied, the magnetization precesses and changes the direction (Fig. 11). This reversal time depends inversely on the damping factor. The damping factor, α of magnetic materials depends on both intrinsic and extrinsic factors. The intrinsic factors are mostly related to spin-orbit interaction. The spin-orbit interaction varies with the atomic number (Z) of magnetic materials. A magnetic material with a high value of Z has high spin-orbit interaction, which leads to a high value of α [117,118]. The CoFeB film has been reported to have low value of $\alpha = 0.001$ –0.1, as it contains only low Z elements [119]. The extrinsic factors include energy dissipation via interaction with adjacent layers, dissipation due to scattering from the interface 2-magnon scattering etc. [120,121]. These factors depend on the film roughness, thickness, growth method and coupling with seeding, and capping layer. The value of α is reported to be increased for thin films compared to the bulks [102,122]. It has to be mentioned that the value of α also defines the switching current in STT and thermal magnetic noise for TMR head [26,27,123]. A high α , which leads to faster switching might lead to undesirable effects when it comes to writing current.

It can be noticed from the previous discussions that the damping factor plays contradicting roles in the performance of writing current and writing speed. A free layer with a higher damping factor leads to the desired higher speed, but also results in a requirement for higher writing current, which is not desired. Piramanayagam et al. have proposed a design where the free layer consists of two layers, one with a high damping factor and another with a lower damping factor. Depending on the combination of the two damping factors and the coupling between the layers, writing current and speed may be optimized [124].

In multilevel MRAMs discussed in the previous section, it is a challenge to switch a particular layer to achieve the desired bit. Such a problem can be solved by introducing STT from an oscillating layer. The use of oscillating layer is also reported to address the particular layer to be switched and to reduce the switching time in the conventional MTJs [109].

In order to improve the writability and read-signals, alternative materials are also sought. One such system of materials is Heusler alloys. The interest in the Heusler alloy thin films is widely increasing due to properties like tunable anisotropy, large spin polarization and high Curie temperature, making them attractive for spintronic applications like high density magnetic storage, STT-MRAM and magnonic devices [65,125–127]. Ferromagnetic layers exhibit a higher value of damping constant α , when the thickness is reduced. However, a record low damping constant α of 0.0015 ± 0.0001 has been obtained in 53 nm thick Co₂FeAl corresponding to an optimum substrate temperature of 300 °C [128]. Such low value of damping constant inspires the

application of Heusler alloys in MRAM. Besides for the writing application, use of Heusler alloys have also been reported for reading improvement due to large magnetic moments, 100% spin polarization and the high Curie temperature [129,130]. The reading signal of an MRAM can be improved by increasing the magnetoresistance ratio. Investigations to improve the magnetoresistance ratio using Heusler alloys for read sensors have also been explored. A GMR ratio of 74.8% has been already reported by Sato et al. using a junction consisting of $\text{Co}_2\text{Fe}_{0.4}\text{Mn}_{0.6}\text{Si}/\text{Ag}/\text{Co}_2\text{Fe}_{0.4}\text{Mn}_{0.6}\text{Si}$ [131]. On the other hand, a TMR ratio of 386% has been reported for $\text{Co}_2\text{FeAl}_{0.5}\text{Si}_{0.5}$ at room temperature [132]. Moreover, researchers have predicted the TMR ratio of 1000% within next 10 years [133]. However, the path of obtaining the half metallicity in Heusler alloys films confront obstacles such as the atomic displacement, misfit dislocation, and symmetry break in the vicinity of the surface of the films. Nevertheless, once the half metallicity is achieved, antiferromagnetic Heusler-alloy films can be combined with non-magnetic films to form Heusler junctions, which may be used in MRAM. So far, this research is still in its early stage

Reliability issues of MRAM

The reliability of the MRAM is the most important issue for its application. In 2004, Åkerman et al. studied the reliability of 4 MB MTJ MRAM based on field-induced switching. The device was found to be stable up to temperatures of 120 °C in terms of dielectric breakdown, resistance drift and data retention. The life time of the device with maximum operation temperature of 70 °C was calculated to be 10 years [134]. In comparison to the field-switching MRAM, the STT-MRAM is more promising and hence, we have paid more attention in this section to the problems associated with it.

Regardless of the various advantages, STT-MRAM also confronts important challenges. Although the write current is lower than in many other memory technologies, still it is very high [135,136]. Such high current leads to a high energy consumption [137,138]. Along with the issue of high-energy consumption, MRAM also confronts other failure issues. The errors due to these failures can be categorized into fixable/correctable errors or non-fixable/non-correctable errors. The fixable errors occur due to the properties of free layer and can be fixed by sending the new signal. These errors are caused by thermal fluctuations. The non-fixable errors occur due to the properties of the barrier oxide layer and as their name suggests they cannot be fixed. These errors occur due to the voltage breakdown of the MTJ or due to the waned TMR ratio under the impact of the bias voltage [63,102].

The fixable errors turn up to be due to the wrong signals. The data can be failed to be stored due to a reversal of the magnetization orientation caused by thermal fluctuations. It can be avoided by increasing the writing current or duration of the current pulse. But, these solutions can lead to the breakdown of the barrier oxide layer. Another possible error can be due to erroneous reading, that is changes in the stored data while reading it. The thermal stability factor is responsible for the data retention. The high value of reading current or the longer reading duration can change the orientation of magnetization.

The non-fixable errors rise up due to the barrier oxide layer. The errors could be the breakdown of the MTJ device limiting

the life-time, which has been discussed earlier or the waning TMR ratio under the influence of bias voltage. In order to get a low RA value, thin barrier oxide layers are used. The resistance variation ratio can be larger than the TMR, which can disturb the sensing operations resulting in errors while reading the data [136,139–141]. Moreover, the write path itself is a challenge in STT-MRAM. In STT-MRAM, the read and write operations share the same access path (through the junction), which damages the reliability such as mistakenly flipping the bit during the read operation. Third, the long write latencies usually prohibit the use of STT-MRAM in first level caches [142].

Emerging memories

New writing schemes

Spin Hall Effect based memory

Due to certain shortcomings of the STT-MRAM, alternative spin-based memories are also being researched. One such candidate is Spin Hall Effect (SHE) based MRAM, which promises lower power consumption in comparison to STT-MRAM. SHE is a phenomenon, where spin-orbit coupling leads to deflection of electrons of different spin in different directions producing a pure spin current, transverse to an applied charge current [143–149]. Pt was one of the first promising metallic materials studied for the SHE, as it exhibits a substantial value of the effect, even at room temperature [150]. The spin Hall conductivity in Pt at room temperature had been noticed to be larger than the low temperature's spin Hall conductivity of other metals like Al. Such a high value of spin Hall conductivity arises from a high magnitude of spin-orbit coupling [151].

First SHE in Pt was interpreted to arise due to the side jumps, skew scattering and other extrinsic mechanisms [152]. But later, studies of intrinsic mechanisms for such high effect in Pt also have been done, which suggested the origin of this effect in Pt to be due to intrinsic mechanisms [153,154]. The use of SHE for MRAM with β -Tantalum layer was reported by Liu et al. in 2012 [34]. In their experiment, the electric current sent through a thin Ta layer, which induced spin torque switching due to SHE in the adjacent ferromagnetic (CoFeB) layer for both, perpendicular and in-plane magnetized samples at room temperature. The use of Ta was preferred over Pt due to the larger spin Hall angle of Ta as compared to that of Pt, which gives a higher ratio of spin current density to charge current density, arising from the SHE. Secondly, unlike Pt, Ta does not produce damping in the adjacent ferromagnetic layer [155,156]. The principle behind this is that, due to SHE the oscillating current in Ta produces an oscillating spin current, which enforces an oscillating spin torque on the magnetic moment of the ferromagnetic layer.

The performance of SHE MRAM (in-plane) and STT-MRAM (interface perpendicular) based cache memory was comparatively studied by the J. Kim et al. using similar material parameters and device dimensions with CoFeB as free layer [157]. The study, based on simulations, reported that the SHE MRAM showed better results for critical spin current, write delay, and retention failure rate (%) with respect to thermal stability. Y. Kim et al. proposed a STT-bit cell based on SHE, suitable for high performance on-chip memory, advocated by the 10 times lesser need of writing energy and exhibiting 1.6 times faster reading

time as compared to the 1T1R (One transistor one resistor) in-plane STT-MRAM [158].

Besides low power consumption and faster switching, the use of three terminal MTJ-based on spin orbit torque is also beneficial in isolating the read and the write path. In spin orbit torque MRAM (SOT-MRAM), the read and the write paths are separated from each other, which significantly improves the reading reliability [159]. Moreover, the write current is much lower and also the write time is supposed to be much faster, as the write path can now be optimized independently.

The MTJ cell is the core part of a bit-cell in SOT-MRAM as in STT-MRAM. However, to eliminate the shortcomings of STT-MRAM, the SOT-MRAM cell has an additional terminal to separate the (unidirectional) read and the (bidirectional) write path, which are perpendicular to each other. The terminals comprise a bit line, a write line, a source line, and a word line as shown in Fig. 12(b). The word line is used to access the required cell during the read operation. While in the write operation, the current flows between the source line and the write line. Direction of the current affects the magnetization of the free layer and hence, the value stored in the bit-cell. If the current flows from the source line to the write line, the MTJ resistance will be low. To achieve a high MTJ resistance, the current needs to flow from write to source line (high potential for the write line) [160].

Although spin-orbit torque is effective in achieving magnetization switching, the underlying physical relation between the current and the magnetic field orientation is still under discussion. Gambardella et al. and Miron et al. described Rashba effect to be a cause of the current-induced magnetization switch [35,161]. On the other hand, Liu et al. attributed SHE to be the cause [34]. Nonetheless, irrespective of the actual effect, the spin-orbit torque is responsible for the switching of free layer magnetization and hence the name SOT-MRAM. Because of all the advantages of SOT-MRAM, it can be a prominent memory to be used in the future. However, still more investigations on the SOT-MRAM needs to be done to make it practical for commercial applications.

Electric field assisted switching for MRAM

We have already mentioned that the writing process in the STT-MRAM using spin polarized current is highly energy consuming.

SOT-MRAM is considered as one technology to reduce power consumption. Another efficient route to manipulate the magnetization in MTJ is by using the voltage control of magnetic anisotropy (VCMA) [162,163]. In this scheme, a voltage is applied to a magnetic material/insulator interface, which produces an electric field and changes the magnetic anisotropy of the material. The reduced anisotropy of the magnetic layer enables magnetization switching at a lower power. Because of the promising potential of energy efficiency, the electric field assisted switching of memory based on VCMA is catching lot of interest [164–168].

The first ever electric field control of ferromagnetic properties was demonstrated by Ohno et al. in 2000 [169]. Later, modification of coercivity, magnetic anisotropy, and Curie temperature by altering the carrier density with a gate voltage also were demonstrated [169–171]. VCMA effect relies on electric field induced change of atomic orbital occupancy at interface. This change is in synchronic connection with spin-orbital interaction, which consequently results in the change of anisotropy [172–174]. A qualitative explanation based on Rashba effect also has been given for VCMA, which relies on the Dzyaloshinskii–Moriya mechanism [175].

In 2010, electric field effects on thickness dependent magnetic properties of CoFeB layers was investigated at room temperature. This study demonstrated the electric field manipulation of magnetic anisotropy in in-plane 2 nm thick CoFeB. On the other hand, for 1.16 nm and 1.02 nm thick perpendicularly magnetized CoFeB electric field induced alteration of coercivity was observed [176]. Wang et al. in 2012 demonstrated the electric-field-assisted switching in perpendicular MTJs [177]. The usual MTJs have thick ferromagnetic layers (>3 nm), where the magnetic anisotropy is independent of the ferromagnetic barrier oxide layer interface [24,25,60,61]. The electric field effect in these layers is negligible due to the screening of electrons. In the case of electric field assisted switching, the thickness of CoFeB is relatively thin (1.6 nm). For this thickness, the PMA arises from the oxide layer interface. As a result of the applied field, the interface anisotropy is affected and the magnetic orientation is changed [102,177].

The main advantage of using the VCMA based memory is the dramatic reduction in power dissipation. By reducing the required current to operate the device, Ohmic dissipation is sig-

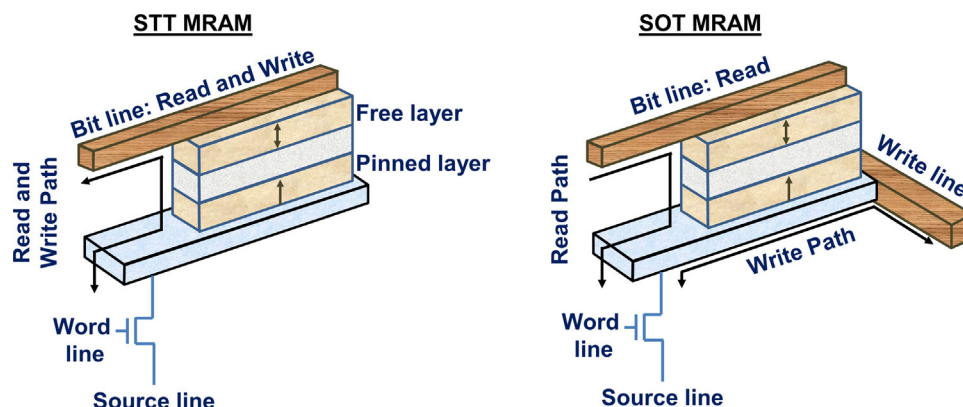


FIGURE 12

Illustration of the path of write and read currents in (a) STT-MRAM and (b) SOT MRAM. SOT MRAM uses separate paths for reading and writing information, as shown by the arrows.

nificantly reduced, which in most cases of magnetic memory, is the predominant loss mechanism [178,179]. Contrary to STT-MRAM for which the pulse polarity determines the switching direction, the write process in VCMA based memory is non-deterministic: only one write pulse amplitude and width is used to achieve both 0 to 1 and 1 to 0 states switching. Hence, a pre-read step is required to determine the initial state (0 or 1) before writing. On the other hand, the barrier being voltage dependent, reading error induced by thermal activation across the barrier during read operation can be nearly eliminated by using a reverse voltage read, and hence faster read time can be achieved with less reading errors [180].

In another scheme, Han et al. [181] reported on the electric field assisted switching in SAF pinned perpendicular MTJ for MRAM. On the basis of experiments and simulations, the bidirectional switching was reported to be possible only by the guidance of bipolar external magnetic field (can be as low as 10 Oe). In the absence of STT effect, fast switching in the range of nanoseconds can be done with a large damping constant and a high electric field efficiency. More recently, study of the feasibility of voltage assisted unipolar switching in perpendicular MTJ without a help of external magnetic field using micromagnetic simulations has been reported [165]. It was demonstrated that for smaller MTJ size, larger change in voltage induced anisotropy field is required.

An alternative approach depends on the reduction of anisotropy energy by applying voltage [182,183]. The reduction in anisotropy energy lowers the energy barrier between free layer states. Due to the reduction in energy barrier, switching of magnetization may be accomplished by thermal activation across the barrier or precessional reorientation, depending on the amplitude of applying voltage. A deterministic switching in both directions is achievable by thermal activation, using a combination of STT and VCMA [177,178,183]. However, this approach was successfully realized only at a slow speed (μ s to ms). Moreover, a significant high efficiency of STT and VCMA is required. On the other hand, precessional takes place at much faster speed, but still requires a timing of voltage pulse width to achieve 180° reorientation [184]. However, this approach is nondeterministic and requires some alteration in circuit design. Switching of free layer from parallel to antiparallel and vice versa is possible by applying a pulse with correct polarity and right pulse width [179]. This scheme facilitates the realization of crossbar memory arrays, resulting in a very small cell area. A fast switching memory with high-density memory arrays is achievable by using this scheme.

All these studies depict that the electric field assisted memory is very promising and holds the potential to become the prominent memory in future. However, a comprehensive study on electric field assisted based memory is still required to commercialize.

Storage schemes

Multilevel storage

With the amount of data stored in MRAM, it cannot compete with higher density storage devices, such as flash memory devices. Several schemes have been proposed in the past in an attempt to solve this problem. One way of improving the density of STT-MRAM is by using the multi-level storage scheme [185]. In

this scheme, a two-bit multilayer for spin transfer switching event that corresponds to four levels of resistance at zero bias was proposed. This two-bit multi-level cell design with MgO layer was demonstrated in MTJ. Two bit cell can be achieved by using single MgO layer MTJ, whose free layer has two domains. These two domains switch at different spin-polarized current, forming a multiple level resistance. The free layer has inhomogeneous magnetization with a soft and hard domain. In this inhomogeneous magnetization, localized injection of STT has been suggested to reduce J_c [186,187]. Another approach using vertical MTJ stack for two bit multi-level storage was proposed by Ishigaki et al. [188]. This design was based on two MTJ having different area size. The two step read and write technique was also proposed for four level operations of this design. However, the fabrication steps increased for this design, making the fabrication process little complex.

Besides these MTJ stacks, a multi-level MRAM was also proposed with spin valve structures. A four distinct resistance level could be achieved using magnetic field in a dual spin-valve was reported by Law et al. which used the multilayers of Co/Pd and CoFe/Pd. The thickness of spin filter layer was varied in this experiment to demonstrate the tuning of resistance levels [189]. The first demonstration of multilevel MRAM using STT was reported by Sbiaa et al. [108]. In their scheme a magnetically hard ferromagnetic layer is deposited between two magnetically soft ferromagnetic layers. It is similar to dual spin valve where the ferromagnetic layers are made of (Co/Pd) multilayers with different properties. As the switching current for these type of materials with large damping constant is very high, a synthetic antiferromagnetically coupled in-plane polarizer was used at each of two soft layers to facilitate the reduction of the required STT switching current. This synthetic structure, over an uncompensated structure, has the advantage of reducing the edge dipolar field from in-plane polarizer that may affect the stability of the soft layer. In order to achieve controllable switching fields (or currents) for the individual layers, the number of bilayers in the multi-layered structure was varied to adjust the magnetic anisotropy. It was shown that four different resistance states can be achieved at remanence using electrical current or voltage.

Recently, a theoretical simulation of the magnetization dynamics based on the free layer and the polarizer layers was reported [190]. The use of polarizers allows the oscillating spin torque with the specific frequency to reverse the magnetization of a particular free layer. Hence, this frequency selection writing process reduces the probability of over-writability on one hand and moreover, has been reported to reduce the writing current too. The demonstration of all these multiple bit storage schemes represents the potential in STT-MRAM for the use of high-density storage in future. But, to implement these schemes to practical world, further investigations are still needed.

Domain wall memory

Ferromagnets are composed of magnetic domains, within which every magnetic moment is aligned. The directions of magnetization of neighboring domains are not parallel. As a result, there is a magnetic domain wall (DW) between neighboring domains. These domain walls can be pushed by spin torque currents and the information can be read by sensing the magnetization direc-

tions of the domains. Hence, memories based on such principles are called domain wall memories. These DW based memories possess the potential of storing information at ultrahigh capacities.

Current driven motion of DW in ferromagnet were demonstrated independently by Tsoi et al., Yamanouchi et al. and Yamaguchi et al. [191–193]. The ability to move DW by applying current attracted lot of focus from the researchers [194–202]. In racetrack memory, a technology proposed by Parkin et al., the movements of DW in magnetic nanowires is controlled by short pulses of spin polarized current and the information is read using MTJ devices [33]. The information is written using electromagnetic writers as in hard disk drives or using STT mechanism. Because of the stacking of domain wall tracks in three dimensions, a high capacity is possible.

In racetrack memory, a ferromagnetic nanowire is formed on the silicon wafer. The nanowire can be configured horizontally or vertically. When domains are formed, the domain wall positions are deterministic in most cases and it is not desirable. The domain length could be long or short and in random positions if one relies on natural pinning sites of the material. On the other hand, the length and positions of the domain walls can be controlled more precisely by the fabrication of artificial pinning sites. Such pinning sites are created along the racetrack, by various methods like modifying the racetrack size, material properties, or patterning the notches along the edges of racetrack, which also give stability to the DW from external perturbation [33,203]. Limited reproducibility of the domain wall pinning strength and the high cost due to the complexity of fabrication are the shortcomings for such technique [204].

To cope up with the limitations of the domain wall pinning with notches, Polenciuc et al. have reported an easier way of fabrication by depositing crossed ferromagnetic and antiferromagnetic wires. A series of antiferromagnetic wires above and below ferromagnetic wires and perpendicular to them were fabricated. When field cooled, the antiferromagnetic wires induce exchange bias at the antiferromagnetic/ferromagnetic, the crossing points act as pinning sites. Due to the simplicity of design and fabrication, this racetrack memory concept has significant advantages over conventional designs [205].

The writing in domain wall memory can be carried out by several schemes such as spin transfer torque effect, self-field effect of current passed along the neighboring nanowires, or by using the fringing fields from the controlled motion of a magnetic DW [26,27]. All of the above mentioned methods are used to flip the magnetic orientation of the domain wall as uniform magnetic field cannot be used here unlike for the conventional MRAMs due to the movement of neighboring DW in opposite direction.

Read operation in DW memory can be carried out by TMR effect, by keeping an MTJ based sensor in either the proximity or in contact with the racetrack. A vertically configured racetrack memory is in 'U' shape and it stores data normal to the plane of substrate providing highest storage density (Fig. 13).

Although the racetrack memory can store several bits along the nanowires, it is difficult to fabricate. Sbiaa et al. have proposed an alternative form of domain wall memory, which is not too long and is relatively easy to fabricate [206]. This pro-

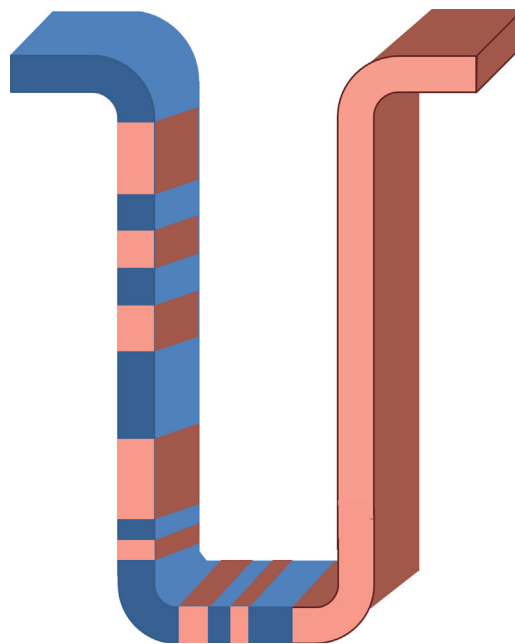


FIGURE 13

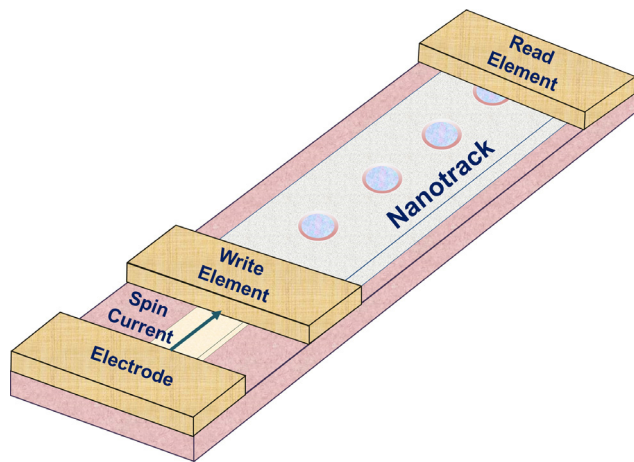
Domain walls in vertical configuration of nanowire. A forest of such nanowires is expected to make a racetrack memory.

posed domain wall memory could serve as an intermediate approach before the more complicated domain wall memories are manufactured. This memory has a reference layer and free layer, similar to an MRAM device. However, both these layers are made of nanowires and the free layer can be magnetized to form domains of various proportions. The TMR value of the domain wall memory device will be different, depending on the domain wall position.

The backbone of the DW memory is the movement of the DWs, which is achieved by applying short pulses of spin polarized current as demonstrated in permalloy. The movement takes place only when a specific critical current is applied. The direction of the DW motion is opposite to the direction of the current. By changing the direction of current, DWs can move toward both sides. The drawback of this technology is the need of a high current density, which increases the temperature of the nanowire. Resonant amplification, which is done by using short current pulses of particular length matched to the innate precessional frequency of pinned DW can be the solution to achieve a low value for the critical current [197,200]. NEC Corporation (NEC) and NEC Electronics Corporation (NECEL) announced the world's first development of a MRAM with current-induced domain wall motion using perpendicular magnetic anisotropy material in 2009. The size of this memory cell was limited to the large scale integration. Further improvements are still needed to implement this technology for very large scale integration. Domain wall based memory is still evolving, as several research groups are working on it to make it more efficient for real world application.

Skyrmion based memories

The domain wall memory devices that have been studied so far are in the dimensions of a few hundred nanometers, which do

**FIGURE 14**

Schematic illustration of a Skyrmion based racetrack memory. The dots represent Skyrmions.

not offer very high areal densities. Therefore, researchers are looking at skyrmions, which have the potential to offer high areal densities. A skyrmion race track memory, shown in Fig. 14, is very similar to a domain wall memory. In a domain wall memory, the domain walls are moved whereas in a Skyrmion based memory, the Skyrmions are moved. In the Skyrmion based memory, the presence or absence of a Skyrmion represents 1 and 0 states.

Skyrmions are topologically protected vortex like swirling spin structures, which can be found in chiral magnets with inversion asymmetry. The main mechanism for formation of the magnetic skyrmions in the chiral magnets is the Dzyaloshinskii–Moriya interaction (DMI). Theoretically, the magnetic skyrmions were reported in 1974 [207]. However, experimental observations of magnetic skyrmions were first reported only in 2009 in cubic B20 MnSi compound [208,209]. Later, the observation of skyrmions was also reported in other B20 compounds such as FeCoSi and FeGe [210,211]. The emergence of skyrmions at the interface of epitaxial ultrathin layers also has been observed later, due to a strong interface DMI. Recently, spin cycloids and nanoscale skyrmion lattices have been observed in epitaxial ultrathin transition metal films by spin-polarized scanning tunneling microscopy at ultralow temperatures [212]. The sturdy nature of skyrmions due to the topological stability, high mobility of skyrmions and their nanoscale features make them promising candidate for the application of magnetic memory devices [213]. However, the synthetic generation and the motions of skyrmions in all these earlier studies were reported at very low temperatures, which makes them inoperable for the working temperature of a memory device.

More recently, strong interfacial DMI in polycrystalline thin-film with heavy metal/ferromagnet/insulating stack such as Pt/CoFe/MgO and Pt/Co/AlO_x has been identified at room temperature [214,215]. Jiang et al. have demonstrated the generation of skyrmion bubbles at room temperature in a constricted geometry of Ta/CoFe/TaO_x trilayer using spin orbit torque [216]. However, short dispersion length in polycrystalline Co leads to local pinning of skyrmions from grain boundaries. This local pinning results in the reduction of skyrmion velocity. As a solution to overcome

this issue, amorphous CoFeB, which offers lower pinning of skyrmions by local DMI has been recommended over polycrystalline Co for a reliable current driven skyrmion motion [217]. Moreover, the use of amorphous CoFeB resulted in higher resultant skyrmion velocity. The mechanism of generation of skyrmions in these multi-layer structures can be linked to the magnetic interactions like interface interaction and DMI, but to comprehensively understand the dynamics at picoseconds or nanoseconds, where certainly intriguing magnetization dynamics occurs, demands further experimental and theoretical investigations. These observations have caused an excitement among the researchers that the room temperature skyrmion based memory is possible. Although micromagnetic simulations have been reported for the skyrmion based race track memory for both low temperatures and room temperature [213,218–221], the experimental demonstration is yet impending.

One of the earlier problems identified with skyrmions is that they experience skyrmion Hall Effect (SkHE). When a skyrmion moves along a nanotrack by a current, SkHE drives it away from the center [222]. This can lead to the annihilation of skyrmion at the walls during the high-speed operation [223,224]. Researchers have investigated this phenomenon and have identified ways to solve this problem. One way of reducing the SkHE is by using the spin wave for driving skyrmions. As reported, the skyrmions can be moved by magnon induced thermal gradients in insulating chiral ferromagnets. However, in current-driven skyrmion scheme, it is difficult to generate spin waves in a nanometer-size nanotrack with spectral properties needed for driving the motion of a skyrmion [127,225–231].

Recently, antiferromagnetically exchange-coupled bilayer system has been reported for suppressing the SkHE. In this bilayer system, two perpendicularly magnetized ferromagnets are strongly coupled via antiferromagnetic exchange interaction with a heavy metal layer under the bottom ferromagnetic layer. Under a strong antiferromagnetic exchange coupling, when a skyrmion is nucleated in the top ferromagnetic layer, another skyrmion is generated in bottom one too. These skyrmions move simultaneously in two ferromagnetic layers. The skyrmion in top layer follows the motion of skyrmion in bottom layer, even when the current is injected in the bottom ferromagnetic layer. Micromagnetic simulations have shown the suppression of SkHE in this bilayer system, exhibiting the motion of skyrmion in a straight line along the nano-track for sufficiently strong antiferromagnetic exchange-coupling exchange coupling [221]. In near future, these approaches for skyrmion's generation and dynamics could enable the application of skyrmions based memory devices like skyrmion racetrack memory.

Summary and outlook

In this review paper, the fundamentals and the recent advances in spintronics based memory have been presented. Starting with a description of the working principles of MRAM, we described the basics behind the three criteria required for a memory device: readability, writability, and retention of data. The magnetoresistance effects, which enable reading of information in MRAM, the methods of writing information in MRAM, such as magnetic field-assisted writing, and STT based writing were discussed in

detail. Storage layers having an in-plane magnetization and the problems faced by them, the advantages of MRAM with perpendicular magnetization and the different materials, which are considered perpendicular MRAM were presented. Thermal stability, writability limitations, and the reliability issues associated with MRAM were also discussed. A discussion was made about the emerging spintronics based memories, which might help in moving beyond the limitations of current MRAM and possibly become prominent in future.

At the time of writing, MRAMs with in-plane magnetization are reaching their limits. MRAMs with perpendicular magnetization are considered for the near future. Recently, 8 Mb of STT-MRAM in embedded 28 nm logic platform with high TMR ratio and retention of 10 years was reported [232]. Another demonstration, which showed the promising potential of STT-MRAM was given by Chung et al. in 2016. A high density (4 Gb) STT-MRAM with compact cell structure with 90 nm pitch was demonstrated through optimizing parasitic resistance. In this demonstrated MRAM, performance factors like read margin and write errors were also improved [233]. STT-MRAMs have already found a niche market in embedded flash memory. They are considered superior to SRAMs in applications that require low power consumption, such as wearable electronics and internet of things. A controller chip with perpendicular STT-MRAMs has been demonstrated for application in the display units. STT-MRAM was found to be as good as SRAM for such applications. The fact that the fabrication of STT-MRAM involves fewer steps and that the power consumption is less, makes STT-MRAM more attractive. However, the fabrication of MRAM faces several challenges. Fabricating the devices, which needs to undergo process at 400 °C is one challenge, but this is expected to be solved soon. Although achieving 25 nm MRAM is not a significant challenge at low densities, fabrication of MRAM at higher packing densities is a challenge. In particular, the etching process causes redeposition at the MgO, shunts the insulating layer and reduces TMR. This is one reason why embedded memory, which does not require high density, is a place for MRAM at this point.

From a materials perspective, identifying new materials that have a higher anisotropy, lower damping constant will be key to achieve thermal stability and writability without sacrificing power consumption. Materials and designs that provide larger spin Hall angle are key for devices operating on the basis of Spin Hall Effect. Materials with a larger voltage controlled magnetic anisotropy coefficient are key for devices with electric field switching based MRAM. For the case of domain wall memory, methods to achieve domain wall pinning are important. Achieving high domain wall velocity, domain wall stability through DMI are some key issues. Research on skyrmions is also a promising area, as skyrmions hold a high potential for high density memory and logic. However, these topics are at their infancy and they will take a long time to be commercialized.

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References

- [1] I. Zutic, J. Fabian, S.D. Sarma, *Rev. Mod. Phys.* 76 (2) (2004) 323.
- [2] S. Wolf et al., *Science* 294 (5546) (2001) 1488–1495.
- [3] S.A. Wolf et al., *Proc. IEEE* 98 (12) (2010) 2155–2168.
- [4] A. Fert, *Rev. Mod. Phys.* 80 (4) (2008) 1517.
- [5] A.D. Kent, D.C. Worledge, *Nat. Nanotechnol.* 10 (3) (2015) 187–191.
- [6] F. Williams, T. Kilburn, *Nature* 162 (4117) (1948) 487.
- [7] F. Williams, T. Kilburn, G. Tootill, *Proc. IEE* 98 (61 Pt 2) (1951) 13–28.
- [8] S.H. Lavington, *Early British Computers: The Story of Vintage Computers and the People Who Built Them*, Manchester University Press, 1980.
- [9] A.A. Cohen, W.R. Keye, *Selective Alteration of Digital Data in a Magnetic Drum Computer Memory*, DTIC Document, 1947.
- [10] P. Morton, in: *Proceedings of the Institute of Radio Engineers*, 1950.
- [11] W.N. Papiian, *Proc. IRE* 40 (4) (1952) 475–478.
- [12] W. Malthaner, H. Vaughan, *Proc. IRE* 41 (10) (1953) 1341–1347.
- [13] J.N.B. Wales, *Means for manufacturing magnetic memory arrays*, Google Patents, 1955.
- [14] T. Noyes, W. Dickinson, *IBM J. Res. Dev.* 1 (1) (1957) 72–75.
- [15] *Memory system*, Google Patents, 1957.
- [16] *Field-effect transistor memory*, Google Patents, 1968.
- [17] R.A. Abbott, W.M. Regitz, J.A. Karp, *IEEE J. Solid-State Circuits* 8 (5) (1973) 292–298.
- [18] V.L. Rideout, *IEEE Trans. Electron Devices* 26 (6) (1979) 839–852.
- [19] B.J. Copeland, *Colossus: The Secrets of Bletchley Park's Code-breaking Computers*, OUP Oxford, 2006.
- [20] S. Mittal, *Int. J. High Perform. Syst. Archit.* 4 (2) (2012) 110–119.
- [21] J. Raffel, T. Crowther, *A Proposal for an Associative Memory Using Magnetic Films*, DTIC Document, 1964.
- [22] M.N. Baibich et al., *Phys. Rev. Lett.* 61 (21) (1988) 2472.
- [23] G. Binasch et al., *Phys. Rev. B* 39 (7) (1989) 4828.
- [24] T. Miyazaki, N. Tezuka, *J. Magn. Magn. Mater.* 139 (3) (1995) L231–L234.
- [25] J.S. Moodera et al., *Phys. Rev. Lett.* 74 (16) (1995) 3273.
- [26] J.C. Slonczewski, *J. Magn. Magn. Mater.* 159 (1) (1996) L1–L7.
- [27] L. Berger, *Phys. Rev. B* 54 (13) (1996) 9353.
- [28] J. Katine et al., *Phys. Rev. Lett.* 84 (14) (2000) 3149.
- [29] W. Kim et al., in: *Electron Devices Meeting (IEDM), 2011 IEEE International*, IEEE, 2011.
- [30] M. Gajek et al., *Appl. Phys. Lett.* 100 (13) (2012) 132408.
- [31] T. Kawahara et al., *Microelectron. Reliab.* 52 (4) (2012) 613–627.
- [32] A. Khvalkovskiy et al., *J. Phys. D: Appl. Phys.* 46 (7) (2013) 074001.
- [33] S.S.P. Parkin, M. Hayashi, L. Thomas, *Science* 320 (5873) (2008) 190–194.
- [34] L. Liu et al., *Science* 336 (6081) (2012) 555–558.
- [35] I.M. Miron et al., *Nature* 476 (7359) (2011) 189–193.
- [36] J. Akerman, *Science* 308 (5721) (2005) 508–510.
- [37] C.H. Marrows, L.C. Chapon, S. Langridge, *Mater. Today* 12 (7–8) (2009) 70–77.
- [38] B. Dieny et al., *J. Appl. Phys.* 69 (8) (1991) 4774–4779.
- [39] S.S.P. Parkin, D. Mauri, *Phys. Rev. B* 44 (13) (1991) 7131.
- [40] J.G. Zhu, *IEEE Trans. Magn.* 35 (2) (1999) 655–660.
- [41] R. Sbiaa, H. Meng, S.N. Piramanayagam, *Phys. Status Solidi* 5 (12) (2011) 413–419.
- [42] W. Thomson, *Proc. R. Soc. Lond.* 8 (1856) 546–550.
- [43] J. Nickel, *Magnetoresistance Overview*, Hewlett-Packard Laboratories, Technical Publications Department, Palo Alto, CA, USA, 1995.
- [44] R. Sbiaa, *Magnetoresistive Read Heads: Fundamentals and Functionality*, *Developments in Data Storage: Materials Perspective*, 2011, p. 97.
- [45] C. Tsang et al., *IEEE Trans. Magn.* 26 (5) (1990) 1689–1693.
- [46] T.-i. Yogi et al., *IEEE Trans. Magn.* 26 (5) (1990) 2271–2276.
- [47] E. De Ranieri et al., *N. J. Phys.* 10 (6) (2008) 065003.
- [48] Grünberg et al., *J. Appl. Phys.* 69 (8) (1991) 4789–4791.
- [49] S.S.P. Parkin, R. Bhadra, K. Roche, *Phys. Rev. Lett.* 66 (16) (1991) 2152.
- [50] B. Rodmacq, G. Palumbo, P. Gerard, *J. Magn. Magn. Mater.* 118 (1–2) (1993) L11–L16.
- [51] S.S.P. Parkin et al., *Phys. Rev. Lett.* 72 (23) (1994) 3718.
- [52] K. Shintaku, Y. Daitoh, T. Shinjo, *Phys. Rev. B* 47 (21) (1993) 14584.
- [53] S. Araki, *J. Appl. Phys.* 73 (8) (1993) 3910–3916.
- [54] S. Schmaus, *Spintronics With Individual Metal-Organic Molecules*, vol. 2, KIT Scientific Publishing, 2011.
- [55] D.J. Sellmyer, R. Skomski, *Advanced Magnetic Nanostructures*, Springer Science & Business Media, 2006.
- [56] M. Getzlaff, *Fundamentals of Magnetism*, Springer Science & Business Media, 2007.

- [57] M. Urech, V. Korenivski, D.B. Haviland, *J. Magn. Magn. Mater.* 249 (3) (2002) 513–518.
- [58] D. Wang et al., *IEEE Trans. Magn.* 40 (4) (2004) 2269–2271.
- [59] W. Butler et al., *Phys. Rev. B* 63 (5) (2001) 054416;
J. Mathon, A. Umerski, *Phys. Rev. B* 63 (2001) 220403(R).
- [60] S.S.P. Parkin et al., *Nat. Mater.* 3 (12) (2004) 862–867.
- [61] D.D. Djayaprawira et al., *Appl. Phys. Lett.* 86 (9) (2005) 092502.
- [62] J. Hayakawa et al., *Jpn. J. Appl. Phys.* 44 (4L) (2005) L587.
- [63] S. Yuasa et al., *Nat. Mater.* 3 (12) (2004) 868–871.
- [64] S. Ikeda et al., *Appl. Phys. Lett.* 93 (8) (2008) 2508.
- [65] S. Ikeda et al., *IEEE Trans. Electron Devices* 54 (5) (2007) 991–1002.
- [66] S. Kumagai, N. Tezuka, T. Miyazaki, *Jpn. J. Appl. Phys.* 36 (11B) (1997) L1498.
- [67] R. Sousa et al., *Appl. Phys. Lett.* 73 (22) (1998) 3288–3290.
- [68] S.S.P. Parkin et al., *J. Appl. Phys.* 85 (8) (1999) 5828–5833.
- [69] X.-F. Han et al., *Appl. Phys. Lett.* 77 (2) (2000) 283–285.
- [70] H. Kano et al., in: *Magnetics Conference, 2002. INTERMAG Europe 2002, Digest of Technical Papers. 2002 IEEE International, IEEE*, 2002.
- [71] D. Wang et al., *IEEE Trans. Magn.* 40 (4) (2004) 2269–2271.
- [72] M. Bowen et al., *Appl. Phys. Lett.* 79 (11) (2001) 1655–1657.
- [73] J. Faure-Vincent et al., *Appl. Phys. Lett.* 82 (25) (2003) 4507–4509.
- [74] S. Yuasa et al., in: *Nanotechnology Materials and Devices Conference, 2006. NMDC 2006, IEEE*, 2006.
- [75] S. Yuasa et al., *Jpn. J. Appl. Phys.* 43 (4B) (2004) L588.
- [76] C.S. Edmund, *Rep. Prog. Phys.* 13 (1) (1950) 83.
- [77] J. Daughton, *Thin Solid Films* 216 (1) (1992) 162–168.
- [78] J.-G. Zhu, *Proc. IEEE* 96 (11) (2008) 1786–1798.
- [79] I. Prejbeanu et al., *J. Phys.: Condens. Matter* 19 (16) (2007) 165218.
- [80] R.S. Beech et al., *J. Appl. Phys.* 87 (9) (2000) 6403–6405.
- [81] M. Hosomi et al., *IEDM Tech. Dig.* 459 (2005).
- [82] E.Y. Tsymlal, O.N. Mryasov, P.R. LeClair, *J. Phys.: Condens. Matter* 15 (4) (2003) R109.
- [83] S.S.P. Parkin et al., *Proc. IEEE* 91 (5) (2003) 661–680.
- [84] T. Yang et al., *J. Nanosci. Nanotechnol.* 7 (1) (2007) 259–264.
- [85] W. Zhao et al., in: *2006 IEEE International Behavioral Modeling and Simulation Workshop 2006, IEEE*, 2006.
- [86] Y. Huai, P.P. Nguyen, F. Albert, *Three-terminal magnetostatically coupled spin transfer-based MRAM cell*, Google Patents, 2006.
- [87] K.-T. Nam et al., in: *Non-Volatile Memory Technology Symposium, NVMTS 2006. 7th Annual, IEEE*, 2006.
- [88] R. Gomez et al., *J. Appl. Phys.* 85 (8) (1999) 6163–6165.
- [89] E. Girgis et al., *Appl. Phys. Lett.* 76 (25) (2000) 3780–3782.
- [90] J. Shi, S. Tehrani, M. Scheinfein, *Appl. Phys. Lett.* 76 (18) (2000) 2588–2590.
- [91] Y. Zheng, J.-G. Zhu, *J. Appl. Phys.* 81 (8) (1997) 5471–5473.
- [92] J. Shi et al., *Appl. Phys. Lett.* 74 (17) (1999) 2525–2527.
- [93] B. Schrag et al., *J. Appl. Phys.* 87 (9) (2000) 4682–4684.
- [94] M.J. Carey, R.E. Fontana Jr., B.A. Gurney, *Magnetic sensors having antiferromagnetically exchange-coupled layers for longitudinal biasing*, Google Patents, 2001.
- [95] N. Nishimura et al., *J. Appl. Phys.* 91 (8) (2002) 5246–5249.
- [96] M. Nakayama et al., *J. Appl. Phys.* 103 (7) (2008) 07A710.
- [97] P. Carcia, A. Meinhaldt, A. Suna, *Appl. Phys. Lett.* 47 (2) (1985) 178–180.
- [98] F. Den Broeder et al., *J. Appl. Phys.* 61 (8) (1987) 4317–4319.
- [99] B.N. Engel et al., *J. Appl. Phys.* 70 (10) (1991) 5873–5875.
- [100] T. Sugimoto et al., *J. Magn. Magn. Mater.* 104 (1992) 1845–1846.
- [101] H. Joo et al., *J. Appl. Phys.* 99 (8) (2006).
- [102] S. Ikeda et al., *Nat. Mater.* 9 (9) (2010) 721–724.
- [103] S. Karthik et al., *J. Appl. Phys.* 111 (8) (2012) 083922.
- [104] H. Meng et al., *J. Appl. Phys.* 110 (3) (2011) 033904.
- [105] D. Worledge et al., *Appl. Phys. Lett.* 98 (2) (2011) 2501.
- [106] T. Tahmasebi, S.N. Piramanayagam, *Magnetoresistance Device*, Google Patents, 2012.
- [107] H. Sato et al., *Appl. Phys. Lett.* 101 (2) (2012) 022414.
- [108] R. Sbiaa et al., *Appl. Phys. Lett.* 99 (9) (2011) 092506.
- [109] R. Sbiaa, *Appl. Phys. Lett.* 105 (9) (2014) 092407.
- [110] M. Jourdan, *Mater. Today* 17 (8) (2014) 362–363.
- [111] Z. Diao et al., *Appl. Phys. Lett.* 90 (13) (2007) 132508.
- [112] G. Hu et al., in: *Electron Devices Meeting (IEDM), 2015 IEEE International, IEEE*, 2015.
- [113] H. Liu et al., *Appl. Phys. Lett.* 101 (3) (2012).
- [114] H. Liu et al., *Appl. Phys. Lett.* 97 (24) (2010).
- [115] R. Sbiaa, S.N. Piramanayagam, T. Liew, *Phys. Status Solidi* 7 (5) (2013) 332–335.
- [116] R. Sbiaa, *J. Phys. D: Appl. Phys.* 46 (39) (2013) 395001.
- [117] V. Kambarský, *Phys. Rev. B* 76 (13) (2007) 134416.
- [118] M. Fähnle, C. Illg, *J. Phys.: Condens. Matter* 23 (49) (2011) 493201.
- [119] S. Mizukami et al., *J. Appl. Phys.* 105 (7) (2009) 7D306.
- [120] A. Brataas, A.D. Kent, H. Ohno, *Nat. Mater.* 11 (5) (2012) 372–381.
- [121] K. Lenz et al., *Phys. Rev. B* 73 (14) (2006) 144424.
- [122] L. Lagae et al., *J. Magn. Magn. Mater.* 286 (2005) 291–296.
- [123] N. Smith, P. Arnett, *Appl. Phys. Lett.* 78 (10) (2001) 1448–1450.
- [124] S.N. Piramanayagam, R. Sbiaa, T. Tahmasebi, *Magnetoresistance Device and Memory Device Including the Magnetoresistance Device*, Google Patents, 2012.
- [125] Q. Ma et al., *Sci. Rep.* 5 (2015).
- [126] Z. Bai et al., *Data storage: review of Heusler compounds*, Spin, World Scientific, 2012.
- [127] A. Chumak et al., *Nat. Phys.* 11 (6) (2015) 453–461.
- [128] S. Husain et al., *Sci. Rep.* 6 (2016).
- [129] I. Galanakis, H. Dederichs, *Half-metallicity and Slater–Pauling behavior in the ferromagnetic Heusler alloys, Half-metallic Alloys*, Springer, 2005, pp. 1–39.
- [130] A. Hirohata et al., *Curr. Opin. Solid State Mater. Sci.* 10 (2) (2006) 93–107.
- [131] J. Sato et al., *Appl. Phys. Express* 4 (11) (2011) 113005.
- [132] N. Tezuka et al., *Appl. Phys. Lett.* 94 (16) (2009) 162504.
- [133] A. Hirohata et al., *IEEE Trans. Magn.* 51 (10) (2015) 1–11.
- [134] J. Åkerman et al., *IEEE Trans. Device Mater. Reliab.* 4 (3) (2004) 428–435.
- [135] M. Hosomi et al., in: *Electron Devices Meeting, IEDM Technical Digest. IEEE International. 2005, IEEE*, 2005.
- [136] W. Zhao et al., *Microelectron. Reliab.* 52 (9) (2012) 1848–1852.
- [137] X. Dong et al., in: *Design Automation Conference, DAC 2008. 45th ACM/IEEE, IEEE*, 2008.
- [138] G. Sun et al., in: *IEEE 15th International Symposium on High Performance Computer Architecture, 2009. HPCA 2009, IEEE*, 2009.
- [139] L.-B. Faber et al., in: *4th International Conference on Design & Technology of Integrated Systems in Nanoscale Era, DTIS'09. 2009, IEEE*, 2009.
- [140] G. Panagopoulos, C. Augustine, K. Roy, in: *Device Research Conference (DRC), 2011 69th Annual, IEEE*, 2011.
- [141] C. Yoshida et al., in: *Reliability Physics Symposium, 2009 IEEE International. 2009, IEEE*, 2009.
- [142] M.-T. Chang et al., in: *2013 IEEE 19th International Symposium on High Performance Computer Architecture (HPCA2013), IEEE*, 2013.
- [143] M. Dyakonov, V. Perel, *Phys. Lett. A* 35 (6) (1971) 459–460.
- [144] J. Hirsch, *Phys. Rev. Lett.* 83 (9) (1999) 1834.
- [145] S. Zhang, *Phys. Rev. Lett.* 85 (2) (2000) 393.
- [146] J. Sinova et al., *Phys. Rev. Lett.* 92 (12) (2004) 126603.
- [147] S. Murakami, N. Nagaosa, S.-C. Zhang, *Science* 301 (5638) (2003) 1348–1351.
- [148] Y. Kato et al., *Nature* 427 (6969) (2004) 50–53.
- [149] S.O. Valenzuela, M. Tinkham, *Nature* 442 (7099) (2006) 176–179.
- [150] E. Saitoh et al., *Appl. Phys. Lett.* 88 (18) (2006) 182509.
- [151] T. Kimura et al., *Phys. Rev. Lett.* 98 (15) (2007) 156601.
- [152] L. Vila, T. Kimura, Y. Otani, *Phys. Rev. Lett.* 99 (22) (2007) 226604.
- [153] J. Schliemann, *Int. J. Mod. Phys. B* 20 (09) (2006) 1015–1036.
- [154] G. Guo et al., *Phys. Rev. Lett.* 100 (9) (2008) 096401.
- [155] T. Tanaka et al., *Phys. Rev. B* 77 (16) (2008) 165117.
- [156] D. Ralph, M.D. Stiles, *J. Magn. Magn. Mater.* 320 (7) (2008) 1190–1216.
- [157] J. Kim et al., in: *Device Research Conference (DRC), 2015 73rd Annual, IEEE*, 2015.
- [158] Y. Kim, S.H. Choday, K. Roy, *IEEE Electron Device Lett.* 34 (10) (2013) 1259–1261.
- [159] K. Jabeur et al., in: *Proceedings of World Academy of Science, Engineering and Technology, World Academy of Science, Engineering and Technology (WASET), 2013*.
- [160] R. Bishnoi et al., in: *Design Automation Conference (ASP-DAC), 2014 19th Asia and South Pacific. 2014, IEEE*, 2014.
- [161] P. Gambardella, I.M. Miron, *Philos. Trans. R. Soc. Lond. A: Math. Phys. Eng. Sci.* 369 (1948) (2011) 3175–3197.
- [162] V. Garcia et al., *Science* 327 (5969) (2010) 1106–1110.
- [163] Y.-H. Chu et al., *Nat. Mater.* 7 (6) (2008) 478–482.
- [164] J. Zhu et al., *Phys. Rev. Lett.* 108 (19) (2012) 197203.
- [165] P. Khalili Amiri et al., *J. Appl. Phys.* 113 (1) (2013) 013912.
- [166] C. Grezes et al., *AIP Adv.* 6 (7) (2016) 075014.
- [167] S. Kanai, F. Matsukura, H. Ohno, *Appl. Phys. Lett.* 108 (19) (2016) 192406.
- [168] C. Song et al., *Prog. Mater. Sci.* 87 (2017) 33–82.
- [169] H. Ohno et al., *Nature* 408 (6815) (2000) 944–946.
- [170] D. Chiba et al., *Science* 301 (5635) (2003) 943–945.
- [171] D. Chiba et al., *Nature* 455 (7212) (2008) 515–518.
- [172] C.-G. Duan et al., *Phys. Rev. Lett.* 101 (13) (2008) 137201.

- [173] M.K. Niranjan et al., *Appl. Phys. Lett.* 96 (22) (2010) 222504.
- [174] J. Velez, S. Jaswal, E. Tsybal, *Philos. Trans. R. Soc. Lond. A: Math. Phys. Eng. Sci.* 369 (1948) (2011) 3069–3097.
- [175] S.E. Barnes, J.i. Ieda, S. Maekawa, *Sci. Rep.* 4 (2014) 4105.
- [176] M. Endo et al., *Appl. Phys. Lett.* 96 (21) (2010) 212503.
- [177] W.G. Wang et al., *Nat. Mater.* 11 (1) (2012) 64–68.
- [178] J.G. Alzate et al., in: *Electron Devices Meeting (IEDM), 2012 IEEE International, IEEE, 2012.*
- [179] K. Amiri et al., *IEEE Trans. Magn.* 51 (11) (2015) 1–7.
- [180] C. Grezes et al., *IEEE Magn. Lett.* (2016).
- [181] G. Han et al., *IEEE Trans. Magn.* 51 (11) (2015) 1–7.
- [182] Y. Shiota et al., *Appl. Phys. Lett.* 101 (10) (2012) 102406.
- [183] K. Amiri, K.L. Wang, K. Galatsis, Voltage-controlled magnetic anisotropy (VCMA) switch and magneto-electric memory (MeRAM), Google Patents, 2015.
- [184] H. Lee et al., *IEEE Trans. Magn.* 51 (5) (2015) 1–7.
- [185] X. Lou et al., *Appl. Phys. Lett.* 93 (24) (2008) 242502.
- [186] P. Braganca et al., *Phys. Rev. B* 77 (14) (2008) 144423.
- [187] P. Braganca et al., *Appl. Phys. Lett.* 87 (11) (2005) 112507.
- [188] T. Ishigaki et al., in: *2010 Symposium on VLSI Technology (VLSIT), IEEE, 2010.*
- [189] R. Law et al., *J. Appl. Phys.* 105 (10) (2009) 103911.
- [190] R. Sbiaa, *J. Phys. D: Appl. Phys.* 48 (19) (2015) 195001.
- [191] M. Yamanouchi et al., *Nature* 428 (6982) (2004) 539–542.
- [192] A. Yamaguchi et al., *Phys. Rev. Lett.* 92 (7) (2004) 077205.
- [193] M. Tsoi, R. Fontana, S.S.P. Parkin, *Appl. Phys. Lett.* 83 (13) (2003) 2617–2619.
- [194] M. Laufenberg et al., *Phys. Rev. Lett.* 97 (4) (2006) 046602.
- [195] M. Yamanouchi et al., *Phys. Rev. Lett.* 96 (9) (2006) 096601.
- [196] C.-Y. You, I.M. Sung, B.-K. Joe, *Appl. Phys. Lett.* 89 (22) (2006) 222513.
- [197] L. Thomas et al., *Nature* 443 (7108) (2006) 197–200.
- [198] A. Thiaville et al., *EPL Europhys. Lett.* 69 (6) (2005) 990.
- [199] G. Meier et al., *Phys. Rev. Lett.* 98 (18) (2007) 187202.
- [200] L. Thomas et al., *Science* 315 (5818) (2007) 1553–1556.
- [201] D. Wong et al., *J. Appl. Phys.* 119 (15) (2016) 153902.
- [202] S. Goolaup et al., *J. Phys.: Conf. Ser.* (2011).
- [203] A. Hubert, R. Schäfer, *Magnetic Domains: The Analysis of Magnetic Microstructures*, Springer Science & Business Media, 2008.
- [204] A. Annunziata et al., in: *Electron Devices Meeting (IEDM), 2011 IEEE International, IEEE, 2011.*
- [205] I. Polenciuc et al., *Appl. Phys. Lett.* 105 (16) (2014) 162406.
- [206] R. Sbiaa, S.N. Piramanayagam, *Appl. Phys. A* 114 (4) (2014) 1347–1351.
- [207] G. Hooft, *Nucl. Phys.: B* 79 (2) (1974) 276–284.
- [208] S. Mühlbauer et al., *Science* 323 (5916) (2009) 915–919.
- [209] A. Neubauer et al., *Phys. Rev. Lett.* 102 (18) (2009) 186602.
- [210] W. Münzer et al., *Phys. Rev. B* 81 (4) (2010) 041203.
- [211] X. Yu et al., *Nat. Mater.* 10 (2) (2011) 106–109.
- [212] S. Heinze et al., *Nat. Phys.* 7 (9) (2011) 713–718.
- [213] A. Fert, V. Cros, J. Sampaio, *Nat. Nanotechnol.* 8 (3) (2013) 152–156.
- [214] S. Emori et al., *Nat. Mater.* 12 (7) (2013) 611–616.
- [215] S. Pizzini et al., *Phys. Rev. Lett.* 113 (4) (2014) 047203.
- [216] W. Jiang et al., *Science* 349 (6245) (2015) 283–286.
- [217] S. Woo et al., *Nat. Mater.* (2016).
- [218] Tomasello, R., et al., A strategy for the design of skyrmion racetrack memories, 2014. **xiv:1409.6491.
- [219] W. Kang et al., *Sci. Rep.* 6 (2016).
- [220] X. Zhang, et al., Skyrmion-skyrmion and skyrmion-edge repulsions in skyrmion-based racetrack memory, 2014. **xiv:1403.7283.
- [221] X. Zhang, Y. Zhou, M. Ezawa, *Nat. Commun.* 7 (2016).
- [222] J. Zang et al., *Phys. Rev. Lett.* 107 (13) (2011) 136804.
- [223] X. Zhang, Y. Zhou, M. Ezawa, *Sci. Rep.* 6 (2016).
- [224] J. Barker, O.A. Tretiakov, *Phys. Rev. Lett.* 116 (14) (2016) 147203.
- [225] J. Iwasaki, A.J. Beekman, N. Nagaosa, *Phys. Rev. B* 89 (6) (2014) 064412.
- [226] C. Schütte, M. Garst, *Phys. Rev. B* 90 (9) (2014) 094423.
- [227] X. Zhang et al., *Nanotechnology* 26 (22) (2015) 225701.
- [228] T. Schwarze et al., *Nat. Mater.* 14 (5) (2015) 478–483.
- [229] S. Schroeter, M. Garst, *Low Temp. Phys.* 41 (10) (2015) 817–825.
- [230] L. Kong, J. Zang, *Phys. Rev. Lett.* 111 (6) (2013) 067203.
- [231] S.-Z. Lin et al., *Phys. Rev. Lett.* 112 (18) (2014) 187203.
- [232] Y.J. Song et al., in: *Electron Devices Meeting (IEDM), 2016 IEEE International, IEEE, 2016.*
- [233] S.-W. Chung et al., in: *Electron Devices Meeting (IEDM), 2016 IEEE International, IEEE, 3–7, Dec. 2016, <https://doi.org/10.1109/IEDM.2016.7838490>.*