Synthesis and Analysis of STT-RAM Switching Characteristics

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Abstract - Spin transfer torque random access memory is a latest cutting edge memory technology which is suitable to be considered for universal memory. In Spin transfer torque random access memory, the magnetic state of magnetic tunneling junction is switched by passing the spin-polarized current through the junction. We have synthesized the HSpice model of STT-RAM to analyze the parallel and anti-parallel switching with change in switching resistance across the fixed and free layer. In this paper, performance comparison between 1-bit STT-RAM cell and Dynamic Random Access Memory (DRAM) is presented. The STT-RAM having high speed, low power consumption, high endurance, zero standby power, high reading and writing speed. In case of STT-RAM storing of bit '1' causes the MTJ resistance to increase up to a specific value and the value of MTJ resistance is 1.4KΩ and current is 700mA. In storing '0' the MTJ resistance is low and value is 0.7KΩ. MTJ current value is -700mA. The leakage power is reduced by 60% in case of STT-RAM when compared to DRAM.

Keywords—Spin Torque Transfer (STT-RAM); Magnetic Random Access Memory (MeRAM), Magnetic Tunnel Junction (MTJ), Dynamic Random Access Memory (DRAM).

I. INTRODUCTION

As the usual memory technologies, e.g. Flash memory, SRAM, DRAM, etc are future end of their lives. Nowadays a new concept is going around particularly known as "Universal Memory". The predictable characteristic of so called universal memory consist of high endurance, low cost, high density, low standby power, low power consumption, high speed (For both read and write), random accessibility, non-volatile and unlimited staying power.

In STT-RAM, the stored data is represented as the measured resistance across the magnetic tunneling junction (MTJ) device. The resistance can be varied between low and high value by passing polarized current through the device. The scalability of the STT-RAM is much better than charge based mechanism of data storage. The STT-RAM power consumption and density is improved, magnetic tunneling junction (MTJ) resistance variations and geometry variation, become famous.

The discovery of giant magneto resistance (GMR; Barthelemy et al. 1999) has initialed an enormous research interest in data storage devices which uses ferromagnetic film (multilayered) separated by metallic spacer (thin) using polarized current as switching source of magnetic domains. Studying the further developments in this research helps in the discovery of tunnel magneto resistance (TMR) in which there exist tunneling current depending on external magnetic field between two ferromagnetic films separated by the oxide layer (thin). The development of tunnel magneto resistance extensively increases the variation in resistance across the ferromagnetic layers to large extent even at room temperatures. The magnitude of TMR has been increased by using crystalline MgO barrier.

II. BASIC PHENOMENON IN MTJs

Taking the structure of two sandwiched ferromagnetic layers with thin insulator layer, the magnitude of the current consists of following composites (1) the tunneling current depending on the density of states of electrode present at Fermi level; (2) The current due to minority and majority bands for electrons having different spin in ferromagnetic materials; (3) parallel two current components because of spin down and up character. The variation of resistance between parallel and anti-parallel magnetization for this usual model can be expressed as:

$$\mathrm{TMR} = \frac{2P_1P_2}{1-P_1P_2}$$

$$P_{1,2} = \frac{N_{1,2}^{maj} - N_{1,2}^{min}}{N_{1,2}^{maj} + N_{1,2}^{min}}$$

Where $P_{1,2}$ are the tunneling spin polarization. The above mentioned expression demonstrates the presence of magneto resistance effect and illustration showing the mechanism of the TMR.

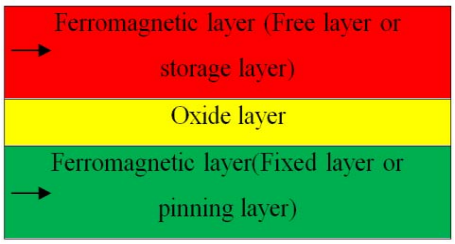

Figure1a: State transition of parallel free layer domains w.r.t fixed layer

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Top: spin down (⇩ are allowed to tunnel from majority to majority bands, and from minority to minority bands for parallel aligned magnetization as sketched left, electron around the Fermi level with spin up (⇧ and, tunnel takes place from majority to minority bands, which specific reduce the total tunneling current.

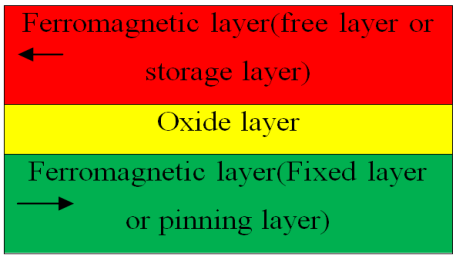

Figure1b: State transition of anti-parallel free layer domains w.r.t fixed layer

For the electrodes the magnetization direction can be manipulated independently as an aspect of TMR. The magnetization direction can be varied with including of intrinsic difference in magnetic hysteresis of the ferromagnetic material exchange biasing with anti-ferromagnetic interlayer coupling across nano-magnetic metallic films. In the mentioned layers of ferromagnetic materials, one layer is fixed layer and other one is free layer with the configurations as follows: a) Parallel b) Anti-Parallel. Parallel configuration of domains provides low resistance '0' whereas the other anti-parallel configuration provides higher resistance '1'.

III. STRUCTURE OF 1-BIT STT-RAM MEMORY CELL

The basic structure uses an MTJ as the storage element and an N-channel MOSFET (1 MTJ -1T) as the selection device.

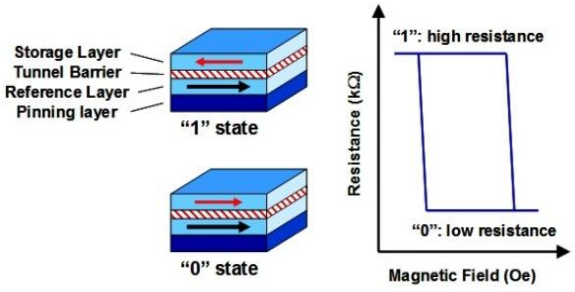

Figure 2: MTJ structure anti-parallel ('1' state) and parallel ('0' state)

IV. READ OR WRITE OPERATION

The switching of the states in MTJ is obtained by changing the direction of current through it. When writing '0' the current flow from BL to SL, whereas when writing '1' the current flow in opposite direction i.e. SL to BL.

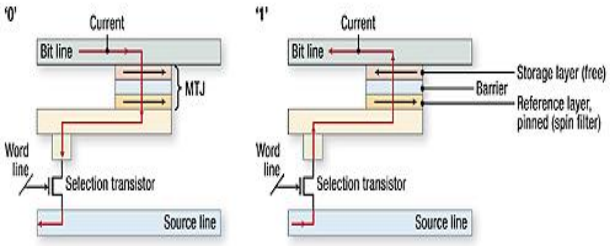

Figure 3: Writing operation of '0' and '1' in STT-RAM cell

For the read operation, reference voltage is required in STT-RAM. Particular transistor is selected by making the high word line. The comparison of reference signal with bit line current can be performed after applying the read voltage.

V. STATIC MODELING

Static behavior of the MTJ is shown in this type of modeling. MTJ static behavior modeling is based on following equations:

- MTJ simplified resistance model considering height of the oxide barrier and voltage dependency is used:

$$R(0) = \frac{t_{ox}}{223.76 * \varphi^{1/2} * surface} * \exp(1.025 * t_{ox} * \varphi^{\frac{1}{2}}) \quad (1)$$

$$R(V) = \frac{R(0)}{1 + [\left(\frac{t_{ox} * e * V}{2 * h}\right)^2 * (\frac{m}{\varphi})]} \quad (2)$$

Where V represents applied voltage, e represents electron charge, m represents mass of electron, h represents reduced Plank constant, oxide barrier height is represented by φ, 223.76 is the F factor and t_{ox} represents the thickness of the oxide layer. Conductance is taken with respect to θ in reference to free layer:

$$G(\theta) = G_T(1 + P^2 \cos\theta) + G_{SI} \quad (3)$$

Where $G_T = G_0\frac{CT}{sinCT}$ with G_0 the conductance at zero temperature, $C = 1.387*10^4 t_{ox}/\sqrt{\varphi}$, G_{ST} is the inelastic tunneling conductance and P represents spin polarization.

- STT-RAM critical current switching model particularly explains the switching behavior of the MTJ and the critical current.

$$J_{co} = \frac{2e*\alpha*\mu_0 M_s*d}{h*g_{sv}} * (H_{ext} \pm H_{ani} \pm \frac{H_d}{2}) \quad (4)$$

$$g_{sv} = (-4 + (P^{1/2} + P^{-1/2}) * (3 + \cos(\theta))/4)^{-1} \quad (5)$$

$$I_{co} = J_{co} * \text{Width} * \text{Length} \quad (6)$$

Where I_{co} represents the critical current, g_{sv} represents spin polarization efficiency, d represents thickness of the free layer, μ_0 is permeability in free space, α represents the damping factor and J_{co} is the critical current density.

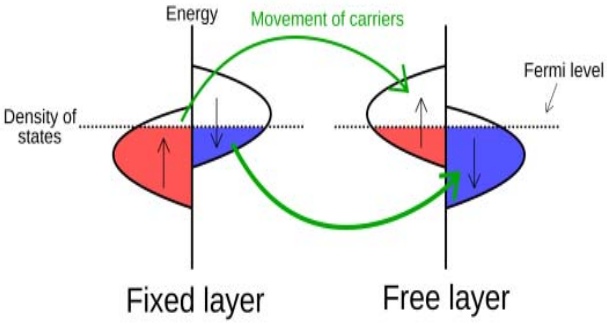

Figure 4: Schematic illustration showing the mechanism of TMR

Total efficiency is calculated as:

$$g = g_{sy} \pm g_{tunnel} \quad (7)$$

Where $g_{tunnel} = \frac{P/2}{1+P^2\cos(\theta)}$ mostly contributes to the tunnel junction efficiency.

The working regimes of the magnetic tunnel junction basically depend on the current density, required switching time where the equation of current density acts as the function of pulse width

$$J_c^{\text{PRECESSIONAL}} = J_{CO} + \frac{c\ln\frac{\pi}{2}}{\tau_{pw}} \quad (8)$$

$$J_c^{DYNAMIC} = \frac{J_C^{THERMAL} + J_c^{PRECESIONAL} * \exp(-A*(\tau_{pw} - T))}{1+\exp(-A*(\tau_{pw} - T))} \quad (9)$$

Table 1: Comparison between SRAM, DRAM, STTRAM

Technology	STT-RAM	DRAM	SRAM
Energy/bit(fJ)	100	1000	100
Write Speed (ns)	1.8	20	1
Read Speed (ns)	2	30	1
Density (area in F^2)	10-30	6-10	>30
Endurance (cycle)	Very High	Very High	Very High
Non-volatile	Yes	No	No
Standby power	None	Refresh Current	Leakage current
Non-volatile logic capacity	Very Limited	No	No

$$J_c^{THERMAL} = J_{co}(1 - \frac{1}{\Delta} In \frac{\tau_{pw}}{\tau_0}) \quad (10)$$

τ_{pw}> 20 ns for thermal activation switching.

10ns > $\tau_{pw} > 30\ ns$ in case of dynamic reversal switching, $\tau_{pw} < 3\ ns$ for processional switching, Where Δ represents thermal stability of magnetization, T, C and A represents fitting parameters.

- MR effect bias-voltage dependence model: (TMR ratio resembles the distinction between low and high resistance states and this is used as main parameter for the sensing mechanism)

$$TMR_{real} = \frac{TMR(0)}{1+(\frac{V_{bias}}{V_h})^2} \quad (11)$$

Where TMR(0) shows the TMR at zero bias voltage, V_h represents free bias voltage when equals TMR_{real} half of TMR (0).

VI. DYNAMIC MODELING

Landau-Lifshitz Gilbert (LLG) equation explains the switching dynamic of the free layer. Constant magnetization vector is taken as the assumption for LLG equation.

$$\frac{dm}{dt} = -\gamma\mu_0[m * H_{eff}] + \alpha[m * \frac{dm}{dt}] + \Gamma \quad (12)$$

$$\Gamma = \frac{\gamma hJ}{M_s et}[(m * (p * m) + '(p * m)] \quad (13)$$

Where γ represents the geometric ratio

VII. SIMULATION RESULT

The switching behavior of an MTJ is generally divided into two regimes: precessional and thermally activated switching figure shows that Processional switching occurs when more than one critical switching current flows through an STT-RAM MTJ or when the perpendicular anisotropy. The free layer magnetic moment switches states on a nanosecond or sub-nanosecond time scale and the dynamics are well described by the Landau-Lifshitz-Gilbert.

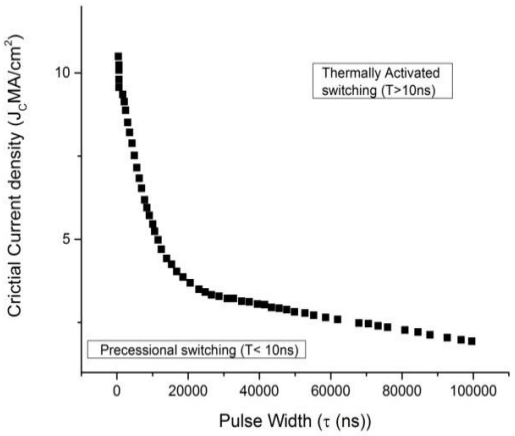

Figure 5: Change in J_c w.r.t pulse width

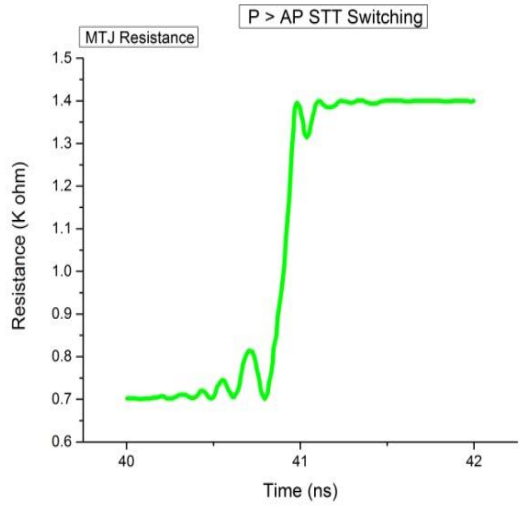

Figure 6.1: Resistance switching from parallel to anti-parallel layer domains

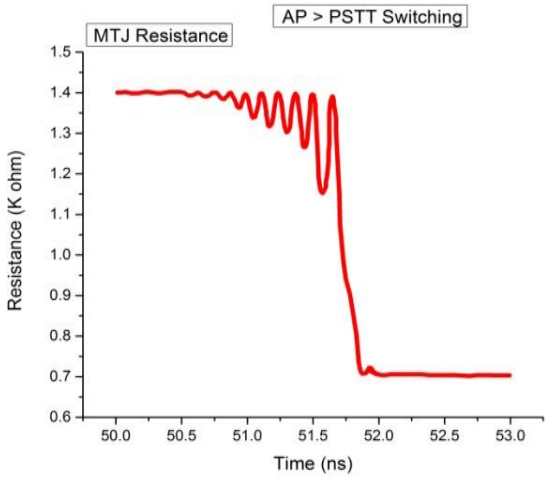

Figure 6.2: Transition of resistance switching from anti-parallel to parallel layer domains

VIII. CONCLUSION

We have observed the change in switching resistances from high to low and vice-versa as the layer domains change their directions from anti-parallel to parallel and parallel to anti-parallel. The highest resistance during the switching is 1.4Kohm representing the logic '1' and lowest resistance during the switching is 0.7Kohm representing the logic '0'. The transient variations of resistance during the switching from anti-parallel to parallel are higher when compared to the resistance variations from parallel to anti-parallel due to non uniformity in magnetization factor and geometric ratio.

REFERENCES

[1] Yiran Chen, Wang. Xiaobin, Hai Li, Haiwen Xi, Yuan Yan, Zhu. Wenzhong, "Design Margin Exploration of Spin-Transfer Torque RAM (STT-RAM) in Scaled Technologies," *In IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol.18, no.12, pp.1724-1734,Dec. 2010

[2] Li.Hai, XiHaiwen, Yiran Chen, Stricklin, J.Xiaobin Wang; Tong Zhang, "Thermal-Assisted Spin Transfer Torque Memory (STT-RAM) Cell Design Exploration," *In* IEEE *Computer Society Annual Symposium on. VLSI,* pp.217-222, 13-15 May 2009

[3] Ping Zhou, Bo.Zhao, Yang.Jun, Youtao Zhang, "Energy reduction for STT-RAM using write early e termination," *In IEEE ACM International Conference on* Computer-Aided Design - Digest of Technical Papers (ICCAD), pp.264-268, 2-5 Nov. 2009

[4] F.B .Yahya, M.M.Mansour, J.Tschanz, M.M.Khellah, "Designing low-V_{TH} STT-RAM for write energy reduction in scaled technologies," *In: Proceeding of 16th International Symposium* Quality Electronic Design (ISQED), 2015

[5] H.Farkhani, A.Peiravi, J.K.Madsen, F.Moradi, "STT- RAM write energy consumption reduction by differential write termination method," *In IEEE International Symposium on* Circuits and Systems (ISCAS),pp.2936-2939, 24-27 May 2015

[6] Wang.Yuhao, Yang Shang, Yu.Hao, "Design of non-destructive single-sawtooth pulse based readout for STT-RAM by NVM-SPICE," *In: Proceeding of* Non-Volatile Memory Technology Symposium (NVMTS), pp.68-72, Oct. 31 2012-Nov. 2 2012

[7] A.Nigam, V.Mohan, E.Chen, S.Gurumurthi, M.R.Stan, "Delivering on the promise of universal memory for spin-transfer torque RAM (STT-RAM)," *In: Proceeding of International Symposium* Low Power Electronics and Design (ISLPED), pp.121-126, 1-3 Aug. 2011

[8] E.Chen, D.Apalkov, Z.Diao, A.Driskill, Smith, D. Drust, D.Lottis, "Advances and future prospects of Spin transfer Torque Random Access Memory "*In IEEE transaction on* Magnetics, 46(6), June 2010

[9] K.L.Wang, J.G. Alzante, and P.K.Amiri, "Low-Power Non-Volatile Spintronic Memory: STT-RAM and Beyond," *In: Proceeding of* Journal *of Physics D: Applied Physics*, vol, 46, no.7 January 2013

[10] W.G.Wang and C.L.Chien, "Voltage-Induced Switching in Magnetic Tunnel Junctions with Perpendicular Magnetic Anisotropy," *In: Proceeding of Journal of Physics D: Applied Physics*, vol, 46, no, 7, January 2013

[11] Sturt S.P.Parkin, "Spintronics Materials and Device: Past, present and future" *In: Proceeding of* Electronic Device Meeting, 2004. IDEM technical digest. IEEE International Volume, Issue, 13-15 pp: 903-906, Dec, 2004

[12] M.Hosomi et.al, "A Novel nonvolatile memory with Spin Torque Transfer Magnetization Switching: Spin-RAM "In *IEEE International Electronic Device Meeting Technical Digest*, Dec 5, 2005 pages: 459-462

[13] W.Kim et al., "Extended Scalability of Perpendicular STT-MRAM Towards sub-20nm MTJ Node, " *In Electronics Devices Meeting (IDEM),2011 IEEE International*, pp.24.11-24.14, December 2011

[14] Y.Higo et al., "Thermal Activation Effect on Spin Transfer Switching in Magnetic Tunnel junctions," *In: Proceeding of Applied Physics Letters*, vol.87, no.8, pp.082502, 2005

[15]G.Binash, P.Grunberg, F. Saurenbach et al., "Enhanced magneto-resistance in layered magnetic structures with anti-ferromagnetic interlayer exchange*," In: Proceeding of Physics. Rev*, B 39, 4828-4830, 1989