Low-Power MRAM for Nonvolatile Electronics: Electric Field Control and Spin-Orbit Torques

Invited Paper

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***Abstract*— We review recent results and discuss challenges and prospects of nonvolatile magnetic random access memory (MRAM). In particular, we will focus on recent developments in magnetoelectric memory (MeRAM), where electric field control is used to replace existing current-controlled write mechanisms to achieve lower power dissipation and higher density. We will discuss scaling trends and prototype crossbar MeRAM demonstrations. We will also discuss the use of spin-orbit torque (SOT) effects for writing with reduced switching currents.**

***Index Terms*—Spintronics, MRAM, STT-RAM, Magnetic Tunnel Junctions, Nonvolatile Memory, MeRAM, SOT-MRAM.**

I. Introduction

Magnetic Random Access Memory using the spin transfer torque effect (STT-MRAM) provides nonvolatile storage of information [1-4], high speed [5-9] (better than DRAM and comparable to some SRAMs), low energy dissipation compared to existing nonvolatile memories (in particular NAND Flash) [7, 8, 10], and high endurance [2, 4, 8].

Nonetheless, STT-MRAM development currently faces a challenge in reducing the write current required for switching the magnetic bits. High switching currents result in both large cell areas due to the large width of access transistors, hence limiting the density, as well as large energy dissipation. This problem gets more significant as one scales STT-MRAM to smaller bit dimensions. Hence, the development of new magnetic tunnel junction (MTJ) material structures with lower switching current densities, and/or the utilization of novel physical mechanisms of writing information that are not based on currents, is critical to the success of MRAM, to enable it to go beyond niche applications and address a broader market.

This paper will focus on two of these possibilities: (i) Using electric field control, rather than current control to switch magnetic memory bits, provides a possibility to dramatically reduce both power dissipation and bit area of MRAM. We will review the recent developments and challenges of this type of magnetoelectric RAM (MeRAM), based on the voltage-controlled magnetic anisotropy (VCMA) effect. (ii) Spin-orbit interaction in nanostructures can also be engineered to create new possibilities for ultralow-power switching via current-induced spin-orbit torques (SOTs), such as the spin Hall effect.

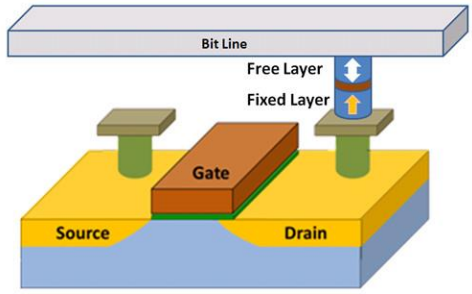

Fig. 1. Schematic illustration of a 1T-1MTJ MRAM cell. Switching of the free layer can be accomplished via STT and/or VCMA effects.

II. STT Switching Current Challenges

STT-MRAM typically uses a 1 Transistor - 1 MTJ (1T-1MTJ) cell structure (see Fig. 1), where a CMOS transistor is used as a select device, and drives the write currents through the bit. Opposite bits of information are written using currents of opposite directions. The bit consists of an MTJ, where information is stored as the relative orientation of a magnetic free layer with respect to a magnetic pinned layer. At scaled technology nodes, the magnetization of both films needs to be perpendicular (i.e. out of plane) for thermal stability, due to the built-in magnetic anisotropy of the material or interface, as opposed to using in-plane shape to define the stable bit directions, which is not scalable below ~30 nm.

Due to the current-controlled 1T-1MTJ structure, the cell area of STT-MRAM is defined by the size of its access transistor, which in turn is proportional to the write current of the magnetic bit. Hence, reduction of the switching current I_c is key to STT-MRAM development. In addition to the switching current, retention time (i.e. nonvolatility) is a key performance parameter, which is determined by the energy barrier E_b between the two magnetic states of the free layer. Typical values of E_b for 10 years retention in a 1 Mbit array are ~60kT, but the required E_b may be larger depending on array size and operating temperature.

For nonvolatile memory, reduction of the switching current generally has to be performed at a constant retention time, and hence for true scalability of STT-MRAM the ratio I_c / E_b has to be minimized. However, for STT-based switching of perpendicularly-magnetized MTJs, the ratio I_c / E_b is largely set by fundamental physical constants and material parameters with a limited tuning range (in particular by magnetic

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damping) [11-13]. This is disadvantageous for scaling. It is worth noting, however, that a number of recent works have suggested a deviation from this rule due to sub-volume excitation effects during switching [14, 15], however further study is needed to understand these effects and their scaling.

The value of I_c / E_b, when combined with the current drive capability of transistors at a given technology node, determines the bit density and hence the application space of STT-MRAM (see Fig. 2). Achieving scalability to below 10 nm (i.e. enabling DRAM-like cell sizes of ~6F2 at F < 10 nm) would require a much smaller scaling parameter of I_c / E_b than presently available, necessitating improvements in material and device design.

Alternatively, in order to provide for an improved scaling scenario, as well as to reduce the energy dissipation associated with the current-induced write mechanism, one can use non-STT write mechanisms for magnetic memory bits that can replace or complement the STT-based approach used in current-controlled MTJs.

III. VCMA Switching for Voltage-Controlled MeRAM

The interfacial voltage-controlled magnetic anisotropy (VCMA) effect [16, 17] has created new possibilities for voltage-controlled MeRAM devices. The free layer material in these structures is designed to have a perpendicular magnetic anisotropy, which can be modulated by voltage, hence allowing for voltage-induced switching of the magnetization. VCMA structures also offer readout via the tunneling magnetoresistance (TMR) effect. Since the manipulation of the free layer magnetization in these devices is performed via voltage (rather than current), the device can be designed to minimize ohmic losses. We refer to such a device as a voltage-controlled magnetoelectric tunnel junction (VMTJ or MEJ), to distinguish it from regular MTJs which primarily use the STT effect, although both effects can in principle be present in the same device.

The VCMA effect can be utilized to switch magnetic tunnel junctions. Switching is accomplished through the modification of perpendicular anisotropy when the voltage is applied. Two general strategies have been demonstrated for switching:

(i) Resonant (precessional) MeRAM: In this type of writing, application of a voltage pulse sets the free layer magnetization into a precessional motion [18, 19]. It can be very fast (< 1 ns) and is bidirectional. Both switching directions can be realized by the same pulse amplitude and width, but to achieve control over the switching direction a pre-read step is required. Due to the high speed and no need for STT (hence high device resistance), the switching can be very low energy (<10 fJ/bit). We have demonstrated this type of purely VCMA-induced switching in fully perpendicular nanoscale MEJs with very wide write windows with low error and speeds < 1 ns, resulting in robust switching. Note that both switching directions are realized by the same pulse shape and polarity, unlike in STT switching. A wide write pulse window for optimized devices enables reliable writing of information.

(ii) Thermally activated MeRAM: This type of switching is based on the lowering of the energy barrier in the free layer, combined with thermal activation. VCMA can be combined

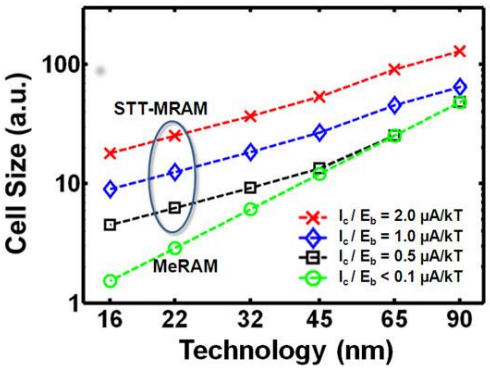

Fig. 2. Effect of the scaling parameter I_c / E_b on the scaling behavior of MRAM. Dramatic reduction of I_c / E_b, e.g. by using the VCMA effect can result in an improved scaling behavior, by allowing for the use of minimum sized transistors across technology nodes.

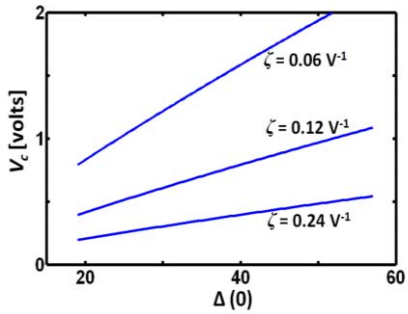

Fig. 3. MeRAM switching voltage as a function of the thermal stability factor (Δ = E_b / kT), for different values of the VCMA parameter ζ, which represents the relative change of the magnetic anisotropy per unit voltage applied to the device [23].

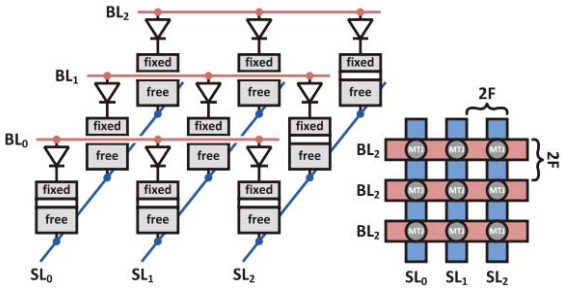

Fig. 4. Schematic illustration of crossbar MeRAM arrays, enabled by the unipolar VCMA switching characteristics [22].

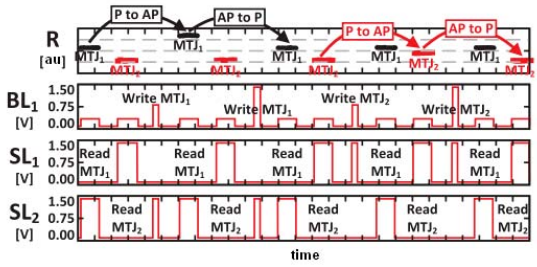

Fig. 5. Measured waveforms demonstrating individual read and writing of bits in a crossbar MeRAM structure [22].

with STT in this strategy to create control over the switching direction. Different voltage pulse amplitudes of the same polarity will switch the device in opposite directions (i.e. write opposite bits of information into it) in this case, thereby allowing for bidirectional switching. Note that, as with precessional switching, the same polarity of voltage is used for switching in both directions in this case. Details and experimental results of such devices are presented in [20-22].

The unipolar voltage-controlled behavior in both of these scenarios (as opposed to the bipolar STT behavior where opposite current polarities are used to write opposite bits of information) is a distinguishing feature of VCMA-based magnetic memory bits. It provides a unique opportunity for realization of crossbar arrays using diodes as access devices, thereby additionally increasing the density by ~2x compared to the traditional 1T-1MTJ architecture used for STT-MRAM, as described in section V.

IV. MeRAM Scaling

In a manner similar to the case of STT-MRAM, we can define the switching voltage V_c for a MeRAM bit, with the associated scaling parameter V_c / E_b which needs to be minimized [23]. Unlike STT-based devices, however, a constant- E_b scaling rule for VCMA devices does not necessarily put a constraint on the size of the access transistors, since currents during writing of MeRAM cells can be substantially smaller than in STT-MRAM. Hence, VCMA devices can potentially allow for minimum-sized transistors to be used down to smaller technology nodes. A similar scaling advantage is possible in terms of energy efficiency.

Successful realization of these potential advantages will require additional development and innovations in the design of improved MeRAM bits. In particular, it is important to maximize the VCMA effect (i.e. reduce V_c) through materials optimization, while maintaining high TMR for readout. A sufficient margin will have to be maintained between different write voltages and the breakdown voltage of the devices. This will require reducing the V_c / E_b ratio from the present ~ 30 mV/kT to < 10 mV/kT to maintain compatibility with CMOS read/write circuitry and typical MgO breakdown voltages of ~1 V. It should be noted, however, that MeRAM can potentially also offer improved performance in terms of breakdown voltage and reliability, due to its increased dielectric barrier thickness compared to traditional STT-MRAM. The tradeoff between switching voltage and thermal stability for MeRAM is illustrated in Fig. 3, showing the calculated critical switching voltage as a function of the thermal stability factor for a perpendicular magnetic bit.

V. MeRAM Crossbar Arrays

The use of transistors in STT-MRAM is necessary due to its purely current-controlled write mechanism, where currents of opposite polarities are needed to write different bits of information. In principle, however, crossbars are the densest memory arrays possible, and hence the realization of a diode-controlled memory device for crossbar arrays can greatly increase the density and scalability of the overall memory. This is enabled by MeRAM's unipolar write voltage. Additionally, the crossbar architecture allows for 3D stacking of multiple diode-MEJ memory layers in the CMOS back-end-of-line (BEOL) fabrication steps, potentially further increasing the effective density.

Figure 4 shows the schematic and layout view of such a high-density crossbar memory array using voltage-controlled MEJs. Parasitic currents ultimately limit the performance and the maximum size of the memory array. By placing the memory arrays directly over the array decoders and sense-amplifiers, a very high cell efficiency can be achieved. Figure 5 shows experimental waveforms demonstrating the functionality of the crossbar memory array.

VI. Spin-Orbit Torque MRAM

A second strategy to address the switching current challenges of STT-MRAM is to reduce the required write current by using spin-orbit torques, e.g. in spin Hall effect induced switching. A second advantage of this approach is that it separates read and write paths of the memory device, hence potentially improving reliability. However it results in a three-terminal device representing the memory bit.

It has been demonstrated that a current flowing through a metallic layer with large spin-orbit coupling, such as Ta or W adjacent to a CoFeB free layer, can generate a spin current into

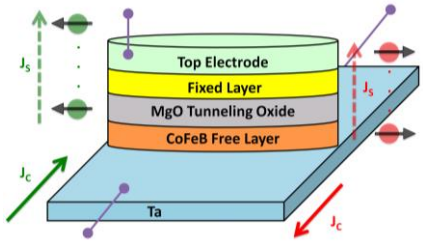

Fig. 6. Schematic of a SOT device, with a high spin-orbit-coupling metal layer passing the horizontal write current, integrated with an MTJ structure for readout via a separate vertical read path [12].

the MTJ free layer, which is large enough to induce switching in the device [24, 25]. The device structure is a three-terminal device (see Fig. 6), where the electrical current flowing in the lateral conductor induces a spin current through the MTJ bit on top of it. The direction of the current controls the injected spin polarization and therefore, the switching direction.

SOT based devices can be integrated into a MeRAM array similar to the one shown in Fig. 4, to enable combined SOT and VCMA switching. In terms of switching energy, the smaller switching current due to the SOT mechanism flows through a low-resistance metallic wire (e.g. a Ta wire as compared to a resistive MTJ), leading to smaller switching energy levels than in traditional STT devices.

While the initial demonstrations of SOT-induced switching were performed on in-plane magnetized layers, recent experiments have focused on the demonstration of switching in perpendicular devices, which are needed for scaling below ~30 nm. Due to the fact that the direction of spins injected into the free layer in response to currents in the high-spin-orbit-coupling metal is in-plane, additional in-plane symmetry breakings are needed in the device in order to enable deterministic switching of perpendicular magnetization via

SOTs. This was initially demonstrated by applying an in-plane external magnetic field to the device [26-28], and more recently was also demonstrated without applying any external fields [29].

VII. Summary and Conclusions

Voltage-controlled MeRAM utilizing the VCMA effect can provide improved energy efficiency, density, and scalability compared to current-controlled STT-MRAM. The success of this approach will depend on the realization of high voltage sensitivity (i.e. VCMA effect) while maintaining high TMR. SOT devices provide another avenue for reduction of switching current to save energy and improve reliability in SOT-MRAM structures. Both VCMA and SOT effects can in principle be combined into the same crossbar architecture, thereby providing major advantages over traditional STT-MRAM in terms of density and 3D stacking capability.

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