Non-volatile Spin-Transfer Torque RAM (STT-RAM): Data, Analysis and Design Requirements for Thermal Stability

A. Driskill-Smith, S. Watts, V. Nikitin, D. Apalkov, D. Druist, R. Kawakami, X. Tang, X. Luo, A. Ong, E. Chen

Grandis, Inc., 1123 Cadillac Court, Milpitas, California 95035, U.S.A.
Email: alexander.driskill-smith@grandisinc.com; Tel: +1 (408) 945-2160; Fax: +1 (408) 945-2161

Abstract

The thermal stability of STT-RAM is measured by multiple techniques and compared with theory. The read disturb rate is found to be determined by the standby thermal stability, but the error rate at target read currents is higher than expected. The implication for the design of 1 Gb STT-RAM is that 10 year room temperature data retention as well as 1000 FIT read disturb error rate requires thermal stability of greater than 75.

Keywords: STT-RAM, spintronics, spin transfer torque

Introduction

STT-RAM (Spin-Transfer Torque Random Access Memory) is a fast (<10 ns), scalable, durable, non-volatile memory technology that is easily embedded in standard CMOS processes. An STT-RAM memory cell consists of an access transistor and a magnetic tunnel junction (MTJ) storage element (Fig. 1). In this paper, we present a detailed analysis of thermal stability measurements obtained from STT-RAM chips. We measure the thermal stability of STT-RAM by multiple techniques – the dependence of write current on pulse-width, switching probability distribution fitting, read disturb probability, and magnetic measurements – and compare the results with the thermal stability parameter expected from spin-transfer torque theory. We also establish the implications of our data and analysis on the design requirements for a 1 Gb STT-RAM.

Write Current Density and Scalability

STT-RAM is an inherently scalable memory technology. For a fixed MTJ design, write current scales linearly with device area (Fig. 2). As the device size shrinks, thermal stability for in-plane STT-RAM can be maintained by adjusting the thickness of the MTJ free layer or device aspect ratio [1]. The write current density J_{c0} can also be reduced at a fixed device size without impacting device thermal stability through MTJ material engineering. For example, average J_{c0} can be reduced from 2–4 MA/cm^2 for conventional, bottom pinned single MTJ (BMTJ) devices [2] to close to 1 MA/cm^2 through the use of partial perpendicular anisotropy (Advanced BMTJ) [3]

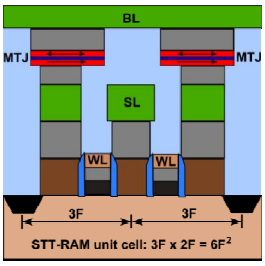

Figure 1. Cross-section through two STT-RAM unit cells with integrated CMOS. The minimum area of a single-level STT-RAM cell is 6 F^2 for both in-plane and perpendicular MTJ magnetization. Even smaller effective unit cell areas are projected for multi-level cells.

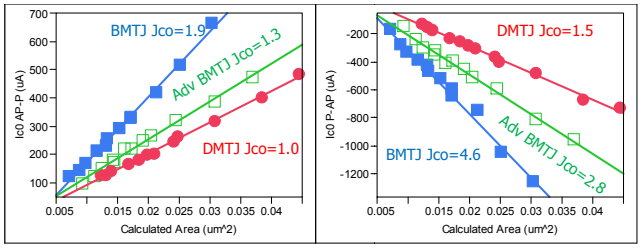

Figure 2. STT-RAM write current scalability. Write current I_{c0} (for both write directions, AP-P and P-AP) versus device area for three different MTJ structures that have the same free layer thickness and thermal stability at 90 nm. Each point is the median value of more than 100 devices.

and dual barrier MTJ (DMTJ) devices [4]. The DMTJs shown in Fig. 2 with adequate thermal stability at 90 nm should be scalable to enable stable 6 F^2 cells at the 32 nm technology node and beyond without any modification to the material set.

Thermal Stability Data and Analysis

The thermal stability of an STT-RAM bit is given by the ratio Δ of the energy required to flip a single bit to the thermal energy. The switching probability distribution of an STT-RAM bit at a given pulse duration can be fit with the conventional distribution function from spin transfer torque theory [5], where the two fitting parameters are the critical switching current I_{c0} and the thermal stability factor Δ. In the low current regime, the slope of the logarithm of switching probability versus I_c/I_{c0} is directly proportional to Δ. From the same theory, I_{c0} and Δ for STT-RAM devices can be estimated by fitting the median switching currents across a range of pulse widths. We will denote measurements of Δ from magnetic characterization as Δ_H, measurements of Δ from single pulse duration full switching probability distribution fits and from the median switching current versus pulse width as Δ_I, and estimates of Δ from the switching probability in the low current regime as Δ_{RD} (read disturb).

Our MTJ materials and device structures have been integrated into 256 kbit STT-RAM test chips based on a 4-level metal, 90 nm CMOS process. The test chip includes a 14 kb test

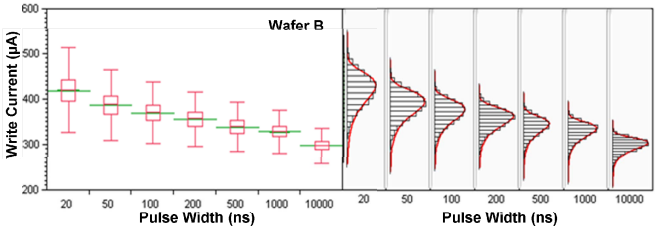

Figure 3. Write current distribution versus pulse width for a single bit. The data are obtained from 15,000 repeats at each pulse width from a single bit on Wafer B. In the right panel, the distributions are fit (red curve) with the conventional distribution function.

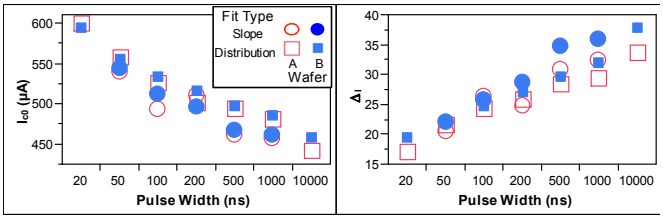

Figure 4. Write current (I_{c0}) and thermal stability (Δ_I) fit parameters versus pulse width for Wafers A and B. The data are median values across multiple bits obtained from distribution fits (squares) and from 3-point write current versus pulse width slope fits (circles).

array in which each cell can be directly connected to an I/O pad, bypassing the sense amplifier. This allows the switching current distribution to be measured very accurately for each bit in the test array. A typical measurement of a single, conventional BMTJ device with 15,000 repeats is shown in Fig. 3. The J_{c0} is approximately 3 MA/cm^2. As the pulse width is reduced, the median write current increases and the distribution width increases.

Our measurements result in very different estimates of thermal stability in the low ($I/I_{c0}<0.5$) and high current ($I/I_{c0}>0.5$) regimes. For two wafers featuring different STT-RAM device structures, we plot in Fig. 4 the median fit results over 20 to 30 bits from both the switching distribution data at a fixed pulse duration as well as the local slope of the median switching current versus pulse duration from three adjacent points. While the devices from the two wafers have similar switching currents, the STT-RAM device in wafer A has a thinner free layer and should therefore have a significantly smaller thermal stability factor Δ, as confirmed by extensive magnetic device characterization (Table 1). However, the values of Δ obtained from both current switching methods give much smaller estimates of Δ, and, remarkably, Fig. 4 shows only a small difference in Δ between the two wafers. Moreover, both the I_{c0} and Δ fit parameters depend on pulse width, with I_{c0} increasing at smaller pulse widths and Δ decreasing. There are several mechanisms that can explain this deviation from the theory [6], but they are beyond the scope of this paper.

We further examine the write error rates from the switching distributions for single bits from each wafer at three different pulse widths (Fig. 5). The slope of the high current tail is expected to be determined by Δ, and we again find a discrepancy with the expected behavior: the curves from the wafers at a particular pulse width are parallel, with possible exception at long pulse widths.

The read disturb data at 20 ns pulse width does reveal a difference between the two wafers, as shown in Fig. 6, where data from 20 to 30 bits are included for each wafer. At currents

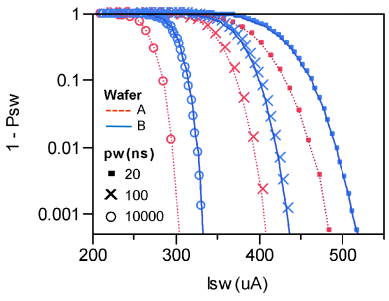

Figure 5. Write error probability versus write current for Wafers A and B. The data are obtained from the single-bit switching distributions at each pulse width.

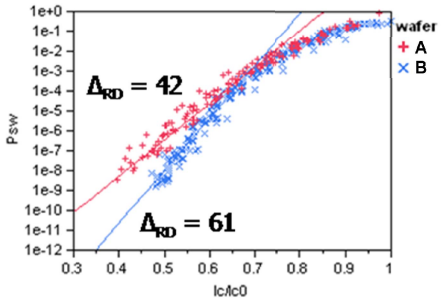

Figure 6. Read disturb probability versus normalized write current for multiple bits from Wafers A and B. The slopes at low current slopes yield Δ_{RD} directly.

Table 1. Comparison of free layer thickness (FL), magnetic anisotropy field (Hk), and thermal stability factors Δ_H, Δ_I and Δ_{RD} for Wafers A and B.

Wafer	FL (nm)	H_k (Oe)	Δ_H	Δ_I	Δ_{RD}
A	1.7	170	40	32	42
B	2.2	240	65	36	61

above 65% of I_{c0}, the switching probabilities are similar for the two wafers, but at low currents, the two wafers show dramatically different results. The values of Δ_{RD} obtained from the slope of the low current tail are much higher than those obtained from the fits at higher currents and in better agreement with the values expected from magnetic characterization.

STT-RAM Design Implications and Conclusions

A summary of our findings is shown in Table 1. We find that both I_{c0} and Δ obtained from conventional fits to the switching data have unexpected dependencies on the pulse width, not explained by simple theory [5]. In particular, the Δ obtained in this way does not scale with device parameters as expected, and does not agree with the measured magnetic properties of the device. However, the Δ_{RD} obtained at lower current conditions in read disturb measurements does agree well with magnetic measurement and with calculated shape-induced anisotropy of the magnetic bit cell.

Our findings indicate that the design specifications for STT-RAM need to consider both low and high-current thermal stabilities. Although the read disturb rate is determined by the standby thermal stability, we find that the extra curvature at high currents shifts the error rate at target read currents higher than expected based on the standard model [7]. Thus, higher thermal stability will be needed to meet the FIT target for read operation. We conclude that for 1 Gb STT-RAM, a 10 year room temperature data retention as well as 1000 FIT read disturb error rate requires Δ of 75, well within the achievable margin with present technology.

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