PCAMAP, NG2, VALENTINE CPU BOARD

Table 1 PCAMAP History

PCA-MAP REV	PCA NUMBER AND REVISION	ECO/CUP	DATE	HW VER.	ENGINEER	REASON/PURPOSE OF CHANGE
-02	73-19882-02_05		03/10/20		Daniel Hoang	P2B Proto
-02	73-19882-03_05		05/06/20		Daniel Hoang	P3A Proto Release
-02	73-19882-04_06		08/05/20		Daniel Hoang	P3B Proto Release
-03	73-19882-04_09		10/26/20		Daniel Hoang	P3C Proto Release

1.0 Purpose

1.1 This document is to be used to assemble 73-19882-04.

1.2 This document provides electronic identification and programming instructions.

1.3 This document defines the instructions required to rework from a previous version or revision, if any.

2.0 Manufacturing Assembly Instructions

2.1 Parts required:

2.1.1 General

2.1.1.1 This assembly is designed for **Pb-free** solder paste reflow processing.

2.1.1.2 Unless otherwise noted below, install all parts per the current revision of assembly drawing 60-103694-04 and bill of materials 73-19882-04.

2.1.1.3 Verify that the fab number of the bare PCB is 28-14428-04. This information is normally located on the solder (bottom) side of the PCB. If this information is not correct, either you have the wrong PCB or this is not the correct assembly procedure. Do not proceed until you have the correct material and documentation. Unless otherwise instructed by Cisco, do not begin the assembly processing of this board unless all the components, called out on the BOM above, are present.

2.1.1.4 Refer to relevant and latest active Cisco Deviations if any.

2.2 Assembly Steps and Procedures:

2.2.1 General

2.2.1.1 Ensure that all LEDs and connectors are installed flush with PCB surface and aligned straight with respect to their silkscreens. Pay particular attention to board edge connectors.

2.2.1.2 Make sure for paste in hole reflow target assembly through hole parts using solder pre-forms, solder paste stencil provision is provided following Cisco ME's direction. Refer EDCS-778627.

2.2.1.3 **Past-in-hole (PIH)**

2.2.1.3.1 The following CPNs are to be assembled using the PIH process.

2.2.1.3.2 Verify that the CPNs support the PIH process.

2.2.1.3.3 Make sure for paste in hole reflow target assembly thru-hole parts using solder preforms (CPN 54-100121-01), solder paste stencil provision is provided following Cisco ME's direction. Refer EDCS-778627

2.2.1.4 **Wave solder**

2.2.1.4.1 The following CPNs are to be assembled using the wave solder process.

2.2.1.4.2 TBD

2.2.1.5 **Cooling cap/Heat shielding**

2.2.1.5.1 The following CPNs are to be assembled with cooling cap/heat shielding placed over them.

2.2.1.5.2 TBD

2.2.1.6 **Post Soldering Heat Sink Installation**

2.2.1.6.1 With PCB backplane connectors facing away, and the front panel I/O connectors facing toward you, the air-flow direction is from right to left.

2.2.1.6.2 When installing adhesive-backed heat sinks, verify the fins are parallel to this airflow direction and the component surface is free of any contamination or solvents. Refer to mechanical assembly drawings 62- p/n under respective 68- level BOM for details.

2.2.1.6.3 For cross-cut fin heat sinks, make sure the wider gap is parallel to the air-flow direction.

2.2.1.6.4 MUST remove glue protection film if present from heat sinks, before installing heatsinks.

2.2.2 Label Placement

2.2.2.1 Refer to the Cisco specifications for labels and printing requirements found on the BOM for each label part number. DO NOT use the part number and revision from the drawing itself or from this assembly procedure. Label the bill of materials assembly number and revision in the PCA area provided per the assembly drawing. Note: CAD artwork specified label locations supersede locations specified in label specification documents. Contact the Cisco PE if clarification is required for label placement.

2.2.2.2 Ensure the following board marking and labeling are present:

2.2.2.2.1 PASS stamp for appropriate test processes.

2.2.2.2.2 Inspection/QA stamps

2.2.2.2.3 PCA barcode S/N Label

2.2.2.2.4 Current PCA P/N, Version and Revision as indicated on the BOM.

2.2.2.2.5 Any applicable Deviation Labels

2.2.3 Mechanical Assembly

2.2.3.1 Press in connectors should be mounted flush with the board surface and endcaps used to protect exposed pins

2.2.3.2 All screws and standoffs should be tightened to required torque outlined in assembly drawings.

2.2.4 PCB and Assembly Defect Repair:

2.2.4.1 Unless otherwise noted, all jumpers (30 ga wire min) are to be installed on the component side of the board.

2.2.4.2 Jumper connections are to be used as a reference for jumper wire end points only and do not define routing paths.

2.2.4.3 All wires should be routed around ICs and tacked to the PCB using glue or tape at intervals of 1.5" or less. Wires should not touch IC legs or other component pins except at end points.

2.2.4.4 All rework must meet or exceed latest revisions of IPC-7711 and IPC-7721 Class 3.

2.2.5 Component Packages using ExposedPad™ technology:

2.2.5.1 For those components using ExposedPad™ technology or some variation thereof, a minimum of 50% solder coverage is required after reflow. The coverage is to be verified using X-ray.

2.3 Test Requirements

2.3.1 X-ray shall be used (as a minimum requirement) to verify solder joints on all of the BGA packages present on the board. Additionally, In Circuit testing (ICT) shall be performed on the board to ensure solder joint quality and bad component identification. For defects found using both tests, the board shall be fixed and the rework recorded by serial number and archived for future reference.

2.3.2 X-ray energy reduction Cu shields should be used for the discrete memory components to reduce the X-ray power dosage to the parts to prevent damages per Standard Operating Procedures (SOP) from Cisco ME.

2.4 Solder Paste Requirements

2.4.1 Solder dots should be placed on the mounting holes and ICT test points copper according to the gerber data. Do NOT put solder paste on the TOP side PCBA mounting holes. Gerber data has this taken care, however ensure that the stencil is built and verified accordingly.

2.4.2 Do NOT exceed the max time over liquidous as specified for respective solder paste being used from the specs. Have the temperature profile reviewed and approved by Cisco ME.

2.4.3 Must use No-Clean Assembly Process.

2.5 Locations where NO MIX AVL Vendor parts are permitted:

2.5.1 Do NOT use mix vendor memory, DC-DC bricks and XTR parts.

2.5.2 Following table shows BOM reference designator locations where NO MIX AVL Vendor rule must be applied.

Table 2 DO NOT USE MIX AVL VENDOR PARTS:

Do NOT MIX AVL Group#	Group RefDes	Cisco PN on BOM
1		
2		
3		
4		
5		
6		

3.0 Programming Instructions:

3.1 Reference the NG IDPROM Specification EDCS-11492349 to program the IDPROM.

3.2 The SERIALNUM field is filled in from the scan of a bar code label that is applied by the CM at the time of manufacturing the modules. The format of the string to be scanned is outlined in the latest revision of specification 95-1766-01.

3.3 The CRC checksum is determined during ICT or during manufacturing test. The algorithm is specified in document EDCS-11525173. **The area from location 0x004 to 0x1FF is to be used to calculate the CRC checksum.**

3.4 Due to the TLV specification, address offsets and extra 00 values will not necessarily be the same after reprogramming at functional test. The address offsets and data shown in the table are only valid for ICT programming.

3.5 The MAC address is assigned at the time the assembly is tested in manufacturing.

3.6 These parameters only reside on this PCA. In terms of IDPROM content, this PCA is the master/active card in the system.

3.7 Default Calibration Data Value is 0x00. This field may be re-purposed for HW traceability e.g, Specific location Memory vendor pending MFG-ENG agreement.

3.8 Device Values Data to represent specific hw_change bits for proto builds based on ENG or MFG PE agreement table value. This field is to be programmed with 0x00 when there is no requirement for proto builds. At production release (A0) this field will be reset to 0x00 unless new MFG-ENG agreement is established.

3.9 Program unused bytes with 0x00 (null).

3.10 This 5th deviation entry is to be used as a HW tracking for prototype boards ONLY. At production release this field will be removed. There is no change to the software common code for this purpose.

3.11 Chassis SN programmed at system test.

3.12 U38 is the location of EEPROM Chip 16-2242-02 (64 Kbit) on CPU BOM 73-19882-04_xx.

Table 3: SPROM for Ref Des U38

Start Add	Data Length (bytes)	Description	HEX Data	Data Type	Human Readable Data
00	2	CRC	00 00	HEX	0x00 {see paragraph 3.3}
02	1	Version	04	HEX	0x04
03	1	Compatibility Byte	FF	HEX	0xFF
04	1	Controller Family ID	48	HEX	0x48
05	2	Controller Family Data	00 45	HEX	0x0045
07	1	Controller Type ID	40	HEX	0x40
08	2	Controller Type Data	06 B2	HEX	0x06B2 {see paragraph 3.6}
0A	1	PCA Serial Number ID	C1	HEX	0xC1

Start Add	Data Length (bytes)	Description	HEX Data	Data Type	Human Readable Data
0B	1	PCA Serial Number Length	8B	HEX	0x8B
0C	11	PCA Serial Number Data	30 30 30 30 30 30 30 30 30 30 30	TXT	{see paragraph 3.2 programmed by ICT}
17	1	PCA Part Number ID	E2	HEX	0xE2
18	1	PCA Part Number Length	46	HEX	0x46
19	2	PCA Part Number Data (commodity)	00 49	DEC	{73-19882-04}73
1B	3	PCA Part Number Data (base)	00 4D AA	DEC	19882
1E	1	PCA Part Number Data (version)	04	DEC	04
1F	1	PCA Revision ID	8A	HEX	0x8A
20	4	PCA Revision Data	30 39 00 00	TXT	09
24	1	Deviation Number ID	88	HEX	0x88
25	4	Deviation Number Data	00 00 00 00	DEC	0
29	1	Deviation Number ID	88	HEX	0x88
2A	4	Deviation Number Data	00 00 00 00	DEC	0
2E	1	Deviation Number ID	88	HEX	0x88
2F	4	Deviation Number Data	00 00 00 00	DEC	0
33	1	Deviation Number ID	88	HEX	0x88
34	4	Deviation Number Data	00 00 00 00	DEC	0
38	1	Deviation Number ID	88	HEX	0x88
39	4	Deviation Number Data	00 00 00 00	DEC	0x00 {See paragraph 3.10}
3D	1	Manufacturing Test Data ID	C4	HEX	0xC4
3E	1	Manufacturing Test Data Length	08	HEX	8
3F	8	Manufacturing Test Data	00 00 00 00 00 00 00 00	HEX	0x00
47	1	Calibration Data ID	86	HEX	0x86
48	4	Calibration Data	00 00 00 00	HEX	0x00 {See paragraph 3.7}
4C	1	Hardware Version ID	41	HEX	0x41
4D	1	Hardware Version Data Major (proto=00; A0 = start at 01)	00	DEC	0
4E	1	Hardware Version Data Minor (proto=/> 00; A0 = reset/start at 00)	04	DEC	4
4F	1	Device Values ID	C9	HEX	0xC9
50	1	Device Values Length	08	HEX	0x08
51	8	Device Values Data	00 00 00 01 E1 20 21 1C	HEX	0x00 00 00 01 E1 20 21 1C
59	422	Unused TLV space	{Filled with "FF"}	FIL	0xFF
1FF	1	TLV Data End Byte	{Filled with "FF"}	FIL	0xFF
200		Reserved for future use (must start at 0x200 address)	{Filled unused with "00"}	FIL	0x00

4.0 PCA Rework:

4.1 N/A

5.0 References

5.1 EDCS-643205 PCAMAP Standardization Document
5.2 EDCS-605019 PCA Assembly Best Practices and Guidelines
5.3 EDCS-7000160 ECO Process & Tools Procedure
5.4 EDCS-7003900 Revision Version Policy
5.5 EDCS-7003340 BOM Structure Policy
5.6 EDCS-231946 Cisco UDI Compliance Specification
5.7 EDCS-231945 Unique Device Identifier (UDI) Policy
5.8 EDCS-7024110 CLEI Code Process