PCAMAP, NG2 1RU BASE BOARD, OPEN PID

Table 1 PCAMAP History

PCA-MAP REV	PCA NUMBER AND REVISION	ECO/CUP	DATE	HW VER.	ENGINEER	REASON/PURPOSE OF CHANGE
-02	73-20560-01_03		12/09/2020	0.0	Daniel Hoang	P4A OPEN - proto release
-03	73-20560-01 03		1/12/2021	0.0	Kevin To	Fix the hw minor version
-04	73-20560-01_03		02/03/2021		Kevin To	Bump up hw mior revision for ST.2 rework

1.0 Purpose

1.1 This document is to be used to assemble 73-20560-01.

1.2 This document provides electronic identification and programming instructions.

1.3 This document defines the instructions required to rework from a previous version or revision, if any.

2.0 Manufacturing Assembly Instructions

2.1 Parts required:

2.1.1 General

2.1.1.1 This assembly is designed for **Pb-free** solder paste reflow processing.

2.1.1.2 Unless otherwise noted below, install all parts per the current revision of assembly drawing 60-103687-05 and bill of materials 73-20560-01.

2.1.1.3 Verify that the fab number of the bare PCB is 28-14425-05. This information is normally located on the solder (bottom) side of the PCB. If this information is not correct, either you have the wrong PCB or this is not the correct assembly procedure. Do not proceed until you have the correct material and documentation. Unless otherwise instructed by Cisco, do not begin the assembly processing of this board unless all the components, called out on the BOM above, are present.

2.1.1.4 Refer to relevant and latest active Cisco Deviations if any.

2.2 Assembly Steps and Procedures:

2.2.1 General

2.2.1.1 Ensure that all LEDs and connectors are installed flush with PCB surface and aligned straight with respect to their silkscreens. Pay particular attention to board edge connectors.

2.2.1.2 Minimum soldermask features: BGA package sites with 0.8 mm pitch and below need to be inspected for adequate soldermask dam (measured soldermask web width should be 3 mils minimum). The sampling plan should be per the Mil-STD-10 5D, AQL of 1% for normal inspection (Typical PCB Lot sizes are 26-50).

2.2.1.3 Past-in-hole (PiH)

2.2.1.3.1 The following CPNs are to be assembled using the PiH process. Proper size and quantity of preformed solder blocks is an option to achieve the desired hole fill result.

2.2.1.3.2 Verify that the following CPNs 29-2327-02, 29-103805-01 support the PiH process.

2.2.1.3.3 Make sure for paste in hole reflow target assembly thru-hole parts using solder preforms (CPN 54-100121-01), solder paste stencil provision is provided following Cisco ME's direction. Refer EDCS-778627

2.2.1.4 **Special Pre-SMT Assembly Instruction**

2.2.1.4.1 All thru-hole pins must meet or exceed hole-fill requirements as defined in document 95-9123-01 (PTH Solder Fill Minimum Acceptance Criteria)

2.2.1.4.2 Although hand-place PiH component is acceptable, the machine automation placement is preferable due to its accuracy that can reduce the impact of solder paste volume control.

2.2.1.5 **Wave solder**

2.2.1.5.1 The following CPNs are to be assembled using the wave solder process.

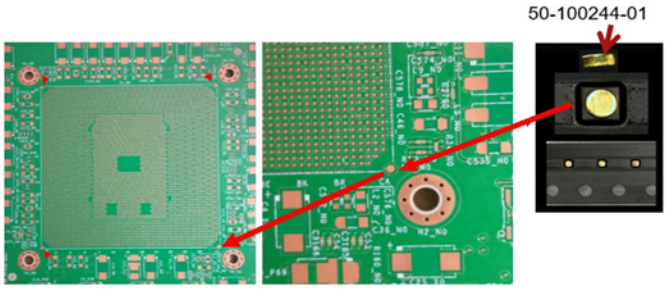
2.2.1.5.2 TBD

2.2.1.6 **Cooling cap/Heat shielding**

2.2.1.6.1 The following CPNs are to be assembled with cooling cap/heat shielding placed over them.

2.2.1.6.2 TBD

2.2.1.7 Ensure the ASIC at U1_N0 location has spacer blocks installed at 4 corners, CSB1, CSB2, CSB3, CSB4, as shown in picture below



2.2.1.8 **Post Soldering Heat Sink Installation**

2.2.1.8.1 Refer to heat sink installation drawings at 68-level BOM.

2.2.1.8.2 With PCB backplane connectors facing away, and the front panel I/O connectors facing toward you, the air-flow direction is from right to left.

2.2.1.8.3 When installing adhesive-backed heat sinks, verify the fins are parallel to this airflow direction and the component surface is free of any contamination or solvents. Refer to mechanical assembly drawings 62- p/n under respective 68- level BOM for details.

2.2.1.8.4 For cross-cut fin heat sinks, make sure the wider gap is parallel to the air-flow direction.

2.2.1.8.5 MUST remove glue protection film if present from heat sinks, before installing heatsinks.

2.2.2 Label Placement

2.2.2.1 Refer to the Cisco specifications for labels and printing requirements found on the BOM for each label part number. DO NOT use the part number and revision from the drawing itself or from this assembly procedure. Label the bill of materials assembly number and revision in the PCA area provided per the assembly drawing. Note: CAD artwork specified label locations supersede locations specified in label specification documents. Contact the Cisco PE if clarification is required for label placement.

2.2.2.2 Ensure the following board marking and labeling are present:

2.2.2.2.1 PASS stamp for appropriate test processes.

2.2.2.2.2 Inspection/QA stamps

2.2.2.2.3 PCA barcode S/N Label

2.2.2.2.4 Current PCA P/N, Version and Revision as indicated on the BOM.

2.2.2.2.5 Any applicable Deviation Labels

2.2.3 Mechanical Assembly

2.2.3.1 Press in connectors should be mounted flush with the board surface and endcaps used to protect exposed pins

2.2.3.2 All screws and standoffs should be tightened to required torque outlined in assembly drawings.

2.2.4 PCB and Assembly Defect Repair:

2.2.4.1 Unless otherwise noted, all jumpers (30 ga wire min) are to be installed on the component side of the board.

2.2.4.2 Jumper connections are to be used as a reference for jumper wire end points only and do not define routing paths.

2.2.4.3 All wires should be routed around ICs and tacked to the PCB using glue or tape at intervals of 1.5" or less. Wires should not touch IC legs or other component pins except at end points.

2.2.4.4 All rework must meet or exceed latest revisions of IPC-7711 and IPC-7721 Class 3.

2.2.5 Component Packages using ExposedPad™ technology:

2.2.5.1 For those components using ExposedPad™ technology or some variation thereof, a minimum of 50% solder coverage is required after reflow. The coverage is to be verified using X-ray.

2.3 Test Requirements

2.3.1 X-ray shall be used (as a minimum requirement) to verify solder joints on all of the BGA packages present on the board. Additionally, In Circuit testing (ICT) shall be performed on the board to ensure solder joint quality and bad component identification. For defects found using both tests, the board shall be fixed and the rework recorded by serial number and archived for future reference.

2.3.2 X-ray energy reduction Cu shields should be used for the discrete memory components to reduce the X-ray power dosage to the parts to prevent damages per Standard Operating Procedures (SOP) from Cisco ME.

2.4 Solder Paste Requirements

2.4.1 Solder dots should be placed on the mounting holes and ICT test points copper according to the gerber data. Do NOT put solder paste on the TOP side PCBA mounting holes. Gerber data has this taken care, however ensure that the stencil is built and verified accordingly.

2.4.2 Do NOT exceed the max time over liquidous as specified for respective solder paste being used from the specs. Have the temperature profile reviewed and approved by Cisco ME.

2.4.3 Must use No-Clean Assembly Process.

2.5 Locations where NO MIX AVL Vendor parts are permitted:

2.5.1 Do NOT use mix vendor memory, DC-DC bricks and XTR parts.

2.5.2 Following table shows BOM reference designator locations where NO MIX AVL Vendor rule must be applied.

Table 2 DO NOT USE MIX AVL VENDOR PARTS:

Do NOT MIX AVL Group#	Group RefDes	Cisco PN on BOM
1		
2		
3		
4		
5		
6		

3.0 Programming Instructions:

3.1 Reference the NG IDPROM Specification EDCS-11492349 to program the IDPROM.

3.2 The SERIALNUM field is filled in from the scan of a bar code label that is applied by the CM at the time of manufacturing the modules. The format of the string to be scanned is outlined in the latest revision of specification 95-1766-01.

3.3 The CRC checksum is determined during ICT or during manufacturing test. The algorithm is specified in document EDCS-11525173. **The area from location 0x004 to 0x1FF is to be used to calculate the CRC checksum.**

3.4 Due to the TLV specification, address offsets and extra 00 values will not necessarily be the same after reprogramming at functional test. The address offsets and data shown in the table are only valid for ICT programming.

3.5 The MAC address is assigned at the time the assembly is tested in manufacturing. **{Within the block the 32MSB should be the same; unique to baseboard}**

3.6 These parameters only reside on this PCA. In terms of IDPROM content, this PCA is the master/active card in the system.

3.7 Default Calibration Data Value is 0x00. This field may be re-purposed for HW traceability e.g, Specific location Memory vendor pending MFG-ENG agreement.

3.8 Device Values Data to represent specific hw_change bits for proto builds based on ENG or MFG PE agreement table value. This field is to be programmed with 0x00 when there is no requirement for proto builds. At production release (A0) this field will be reset to 0x00 unless new MFG-ENG agreement is established.

3.9 Program unused bytes with 0x00 (null).

3.10 This 5th deviation entry is to be used as a HW tracking for prototype boards ONLY. At production release this field will be removed. There is no change to the software common code for this purpose.

3.11 Chassis SN programmed at system test.

3.12 IDPROM is the location of EEPROM Chip 16-2242-02 (64 Kbit) on Churchill MB BOM 73-20560-01.

Table 3: SPROM for Ref Des IDPROM

Start Add	Data Length (bytes)	Description	HEX Data	Data Type	Human Readable Data
00	2	CRC	00 00	HEX	0x00 {see paragraph 3.3}
02	1	Version	04	HEX	0x04
03	1	Compatibility Byte	FF	HEX	0xFF
04	1	Controller Family ID	48	HEX	0x48
05	2	Controller Family Data	00 45	HEX	0x0045
07	1	Controller Type ID	40	HEX	0x40
08	2	Controller Type Data	06 B1	HEX	0x06B1 {see paragraph 3.6}

Start Add	Data Length (bytes)	Description	HEX Data	Data Type	Human Readable Data
0A	1	PID (UDI Product ID) ID	CB	HEX	0xCB
0B	1	PID (UDI Product ID) Length	92	HEX	0x92
0C	18	PID (UDI Product ID) Data	38 32 30 31 2D 33 32 46 48 2D 4F 00 00 00 00 00 00 00	TXT	8201-32FH-O {see paragraph 3.6}
1E	1	VID (UDI Product ID) ID	89	HEX	0x89
1F	4	VID (UDI Product ID) Data	56 30 30 00	TXT	V00 {see paragraph 3.6}
23	1	UDI Product Description ID	DA	HEX	0xDA
24	1	UDI Product Description Length	BF	HEX	0xBF
25	63	UDI Product Description Data	43 69 73 63 6F 20 38 32 30 30 20 53 65 72 69 65 73 20 33 32 78 34 30 30 47 20 51 53 46 50 44 44 20 31 52 55 20 46 69 78 65 64 20 53 79 73 74 65 6D 20 77 2F 48 42 4D 2C 4F 70 65 6E 20 53 57	TXT	Cisco 8200 Series 32x400G QSFPDD 1RU Fixed System w/HBM,Open SW {see paragraph 3.6}
64	1	Chassis Serial Number ID	C2	HEX	0xC2
65	1	Chassis Serial Number Length	8B	HEX	0x8B
66	11	Chassis Serial Number Data	00 00 00 00 00 00 00 00 00 00 00	TXT	{see paragraph 3.11}
71	1	Top Assembly Number ID	87	HEX	0x87
72	1	TAN Commodity Code	44	DEC	{68-7409-01}68 {see paragraph 3.6}
73	2	TAN Base Number	1C F1	DEC	7409 {see paragraph 3.6}
75	1	TAN Version	01	DEC	01 {see paragraph 3.6}
76	1	Top Assembly Revision ID	8D	HEX	0x8D
77	4	Top Assembly Revision Data	30 32 00 00	TXT	02 {see paragraph 3.6}
7B	1	PCA Serial Number ID	C1	HEX	0xC1
7C	1	PCA Serial Number Length	8B	HEX	0x8B
7D	11	PCA Serial Number Data	00 00 00 00 00 00 00 00 00 00 00	TXT	{see paragraph 3.2 programmed by ICT}
88	1	PCA Part Number ID	E2	HEX	0xE2
89	1	PCA Part Number Length	46	HEX	0x46
8A	2	PCA Part Number Data (commodity)	00 49	DEC	{73-20560-01}73
8C	3	PCA Part Number Data (base)	00 50 50	DEC	20560
8F	1	PCA Part Number Data (version)	01	DEC	01
90	1	PCA Revision ID	8A	HEX	0x8A

Start Add	Data Length (bytes)	Description	HEX Data	Data Type	Human Readable Data
91	4	PCA Revision Data	30 33 00 00	TXT	03
95	1	CLEI Code ID	C6	HEX	0xC6
96	1	CLEI Code Length	8A	HEX	0x8A
97	10	CLEI Code Data	55 4E 41 53 53 49 47 4E 45 44	TXT	UNASSIGNED {see paragraph 3.6}
A1	1	ECI Code ID	EB	HEX	0xEB
A2	1	ECI Code Length	86	HEX	0x86
A3	6	ECI Code Data	45 43 49 31 32 33	TXT	ECI123 {see paragraph 3.6}
A9	1	Deviation Number ID	88	HEX	0x88
AA	4	Deviation Number Data	00 00 00 00	DEC	0
AE	1	Deviation Number ID	88	HEX	0x88
AF	4	Deviation Number Data	00 00 00 00	DEC	0
B3	1	Deviation Number ID	88	HEX	0x88
B4	4	Deviation Number Data	00 00 00 00	DEC	0
B8	1	Deviation Number ID	88	HEX	0x88
B9	4	Deviation Number Data	00 00 00 00	DEC	0
BD	1	Deviation Number ID	88	HEX	0x88
BE	4	Deviation Number Data	00 00 00 00	DEC	0 {See paragraph 3.10}
C2	1	Manufacturing Test Data ID	C4	HEX	0xC4
C3	1	Manufacturing Test Data Length	08	HEX	8
C4	8	Manufacturing Test Data	00 00 00 00 00 00 00 00	HEX	0x00
CC	1	Calibration Data ID	86	HEX	0x86
CD	4	Calibration Data	00 00 00 00	HEX	0x00 {See paragraph 3.7}
D1	1	Base MAC Address ID	C3	HEX	0xC3
D2	1	Base MAC Address Length	06	HEX	0x06
D3	6	Base MAC Address Data	00 00 00 00 00 00	HEX	0x00 {see paragraph 3.5}
D9	1	MAC Block Size ID	43	HEX	0x43
DA	2	MAC Block Size Data {Unique 32MSB requirement}	02 00	DEC	512
DC	1	Hardware Version ID	41	HEX	0x41
DD	1	Hardware Version Data Major (proto=00; A0 = start at 01)	00	DEC	0
DE	1	Hardware Version Data Minor (proto=/> 00; A0 = reset/start at 00)	29	DEC	41
DF	1	Estimated Power Consumption ID	D7	HEX	0xD7
E0	1	Estimated Power Consumption Length	44	DEC	68

Start Add	Data Length (bytes)	Description	HEX Data	Data Type	Human Readable Data
E1	4	Est. Pwr Cons Data [x 0.01W]	00 00 00 00	DEC	0
E5	1	Device Values ID	C9	HEX	0xC9
E6	1	Device Values Length	08	HEX	0x08
E7	8	Device Values Data	82 E0 00 08 28 00 00 00	HEX	0x82 E0 00 08 28 00 00 00 {See paragraph 3.8}
EF	272	Unused TLV space	{Filled with "FF"}	FIL	0xFF
1FF	1	TLV Data End Byte	{Filled with "FF"}	FIL	0xFF
200		Reserved for future use (must start at 0x200 address)	{Filled unused with "00"}	FIL	0x00

4.0 PCA Rework:

4.1 N/A

5.0 References

5.1 EDCS-643205 PCAMAP Standardization Document
5.2 EDCS-605019 PCA Assembly Best Practices and Guidelines
5.3 EDCS-7000160 ECO Process & Tools Procedure
5.4 EDCS-7003900 Revision Version Policy
5.5 EDCS-7003340 BOM Structure Policy
5.6 EDCS-231946 Cisco UDI Compliance Specification
5.7 EDCS-231945 Unique Device Identifier (UDI) Policy
5.8 EDCS-7024110 CLEI Code Process