Table 1 PCAMAP History

PCA-MAP REV	PCA NUMBER AND REVISION (73-BBBB-VV_RR)	ECO/CUP	DATE	HW VER.	ENGINEER	REASON/PURPOSE OF CHANGE
A0	73-20128-04_A0	EA590474	08/25/2021	1.0	rikwong	Production release

1.0 Purpose

1.1 This document is to be used to assemble 73-20128-04.

1.2 This document provides electronic identification and programming instructions.

1.3 This document defines the instructions required to rework from a previous version or revision, if any.

2.0 Manufacturing Assembly Instructions

2.1 Parts required:

2.1.1 General

2.1.1.1 Unless otherwise noted below, install all parts per the current revision of assembly drawing **60-104039-04** and bill of materials **73-20128-04**.

2.1.1.2 Verify that the fab number of the bare PCB is **28-14606-04**. This information is normally located on the solder (bottom) side of the PCB. If this information is not correct, either you have the wrong PCB or this is not the correct assembly procedure. Do not proceed until you have the correct material and documentation. Unless otherwise instructed by Cisco, do not begin the assembly processing of this board unless all the components, called out on the BOM above, are present.

2.1.2 **Part Changes Not in Schematic**

2.1.2.1 NONE

2.1.3 Part Changes Not in BOM

2.1.3.1 NONE

2.2 Assembly Steps and Procedures:

2.2.1 General

2.2.1.1 PWB flatness: Flatness should be verified on BGA package sites of 47.5mm and above per the requirements on the fabrication drawing. 10% of the boards per PCB lot should be tested. Any out of specification measurement would require a 100% sampling response prior to assembly (This measurement may be performed by the PWB supplier at the Contract Manufacturer).

2.2.1.2 Minimum soldermask features: BGA package sites with 0.8 mm pitch and below need to be inspected for adequate soldermask dam (measured soldermask web width should be 3 mils minimum). The sampling plan should be per the Mil-STD-10 5D,AQL of 1% for normal inspection (Typi al PCB Lot sizes are 26-50).

2.2.1.3 **LCCC's:** Component stand-off height is critical. Stand-off height is a function of pad paste volume. The minimum stand-off height is >= 0.0015". Optimal stand-off height is 0.0025". Stencil apertures should be 1:1 to the PCB pad soldermask opening. Use a stencil thickness of 0.006". All LCCC solder paste deposits must be measured (AOI/SVS) to insure that they are the same (within 10% of each other) to prevent significant component tilt after assembly.

2.2.1.4 Post Soldering Heat Sink Installation

2.2.1.4.1 With PCB backplane connectors facing away, and the front panel I/O connectors facing toward you, the air-flow direction is from FRONT TO BACK OR BACK TO FRONT.

2.2.1.4.2 When installing adhesive-backed heat sinks, verify the fins are parallel to this airflow direction and the component surface is free of any contamination or solvents.

2.2.1.4.3 For cross-cut fin heat sinks, make sure the wider gap is parallel to the air-flow direction.

2.2.1.5 Ensure that all LEDs and connectors are installed flush with PCB surface and aligned straight with respect to their silkscreens. Pay particular attention to board edge connectors.

2.2.2 Label Placement

2.2.2.1 Refer to the Cisco specifications for labels and printing requirements found on the BOM for each label part number. DO NOT use the part number and revision from the drawing itself or from this assembly procedure. Label the bill of materials assembly number and revision in the PCA area provided per the assembly drawing. Note: CAD artwork specified label locations supersede locations specified in label specification documents. Contact the Cisco EPE if clarification is required for label placement.

2.2.3 Mechanical Assembly

2.2.3.1 Press in connectors should be mounted flush with the board surface and end caps used to protect exposed pins

2.2.3.2 Connectors are press-fit please process after SMT reflow.

2.2.3.3 It may be necessary to mask the screw mounting holes on the bottom side of the board. The holes are designed in order to minimize solder pickup. No solder is allowed on the screw mounting holes.

2.2.3.4 All screws and standoffs should be tightened to required torque outlined in 95-5874-01

2.2.3.5 Follow assembly instructions outlined in **62-110042-01**.

2.2.4 PCB and Assembly Defect Repair:

2.2.4.1 Unless otherwise noted, all jumpers (30 ga wire min) are to be installed on the component side of the board.

2.2.4.2 Jumper connections are to be used as a reference for jumper wire end points only and do not define routing paths.

2.2.4.3 All wires should be routed around ICs and tacked to the PCB using glue or tape at intervals of 1.5" or less. Wires should not touch IC legs or other component pins except at end points.

2.2.4.4 All rework must meet or exceed latest revision of IPC-R-700 Class 2.

2.3 Test Requirements

2.3.1 X-ray shall be used (as a minimum requirement) to verify solder joints on all of the BGA packages present on the board. Additionally, In Circuit testing (ICT) (if Available) shall be performed on the board to ensure solder joint quality and bad component identification. For defects found using both tests, the board shall be fixed and the rework recorded by serial number and archived for future reference.

3.0 Programming Instructions

3.1 Programmable Devices Data

3.1.1 See Table 1 for the programmable data information. If the pre-programmed image in the devices is not the same as those listed in the table, then the images are to be updated to match those listed in the table.

3.1.2 The files for the 17-level images can be found in EMCO.

3.1.3 The programmable table shows the firmware that is pre-programmed on the PCBA. The firmware may be upgraded during manufacturing tests. Please look up the latest specification 95-xxxxxx-xx for the minimum firmware required for customer shipment. The firmware listed in 95-xxxxxx-xx is the minimum required firmware for compatibility with the customer software. The 95 specification will be available at the time of the product's –A0 release.

3.1.4

Table 1 – Coastal Fog MB A0 BOM Pre-programmable Data

Image Desc	Ref Des	Part Number	Filename
PLD,PROG,LATTICE, TOR, UTOPIAS, CPLD, QSFP POWER CONTROL	U1_C4	17-15260-02	Utopias_pwr_en_imp_0_v3.jed
PLD,PROG,LATTICE, TOR, Kriek, CPLD, 12QSFP and 3 SFP	U1_C3	17-15268-01	Kriek1_imp_0_V2.jed
IC,LINEAR,PWR_CONTROLLER,IR35215, Retimer VRM, COASTAL FOG	U1_RR	17-15793-03	17-15793-03-00_RT_MTK_3+2_120A_OCP 08042021.mic
PROG,FLASH,TOR,MIROM,COASTAL FOG, v11	U38	17-15982-02	mi_coastal_fog_v11_swap.rpd
PROG,TIMING,SYNTHESIZER, 800MHz,LMK05318,COASTAL FOG	U4	17-16391-02	LMK05318_Coastal_Fog_R4-I2C-Program-Only.txt
PLD,PROG,LATTICE, TOR, CALGARY, CPLD	U1_C1,U1_C2	17-12430-01	Calgary1_imp_0_v2.jed
INSBU: IC,LINEAR, PWR SEQ, PWR_CONTROLLER,Q3V3R, Utopias	U1_Q3V3R	17-15549-02	17-15549-02_Utopias_QSFPDD.MIC
PROG,PWR SEQ,IR35215,QUADPEAKS AVDD VRM,COASTAL FOG	U1_QA	17-15988-01	17-15988-01-00_QP_AVDD_2+1.mic
PROG,PWR SEQ,QUADPEAKS DVDD VRM,COASTAL FOG	U1_QD	17-15989-02	17-15989-01-00_QP_DVDD_14+0.mic

Table 2 – Coastal Fog MB A0 Shipping Firmware Data

N9K-C9332D-GX2B Coastal Fog	Image file 5/21/2020	Image version / date
BUILD	Pilot	
MI-FPGA (for P3 only)	08/22/21: mi_coastal_fog_v13_swap.rpd.spi (P3)	0x20210819 (P3)
CPLD0	06/30/2020: 42992 May 21 06:55 calgary1_imp_0_v2.bin (diag)	00c20002
CPLD1	06/30/2020: 42992 May 21 06:55 calgary1_imp_0_v2.bin (diag)	00c20002
CPLD2	06/30/2020: 42992 Jun 4 02:15 kriek1_imp_0_V2.bin (diag)	00cc0002
CPLD3	06/30/2020: 42992 May 21 06:56 utopias_pwr_en_imp_0_v4.bin	0xd30004
PWR_SA_DVDD VRM (U1_UD)	05/24/21: 36711 May 20 15:00 BRING_UP_ONLY_17-15989-03-01_QP_DVDD_16+0.txt	17-15989-03 (PPLT-2A+)
PWD_SA_AVDD VRM (U1_QA)	06/30/20: 36755 Jun 30 04:57 17-15988-01-00_QP_AVDD_2+1.txt	17-15988-01
Retimer VRM (U1_RR)	09/10/21: 17-15793-03-00_RT_MTK_3+2_120A_OCP.txt (E2 retimer)	17-15793-03
VRM (U1_Q3V3R)	05/24/2021: 36758 Jun 15 16:11 17-15549-02_Utopias_QSFPDD.txt (diag) 05/24/2021: 19231 Jun 15 16:12 17-15549-02_Utopias_QSFPDD.MIC	17-15549-02
Clock OSCTI	14793 Jun 8 16:27 LMK05318_Coastal_Fog_R4-I2C-Program-Verify.txt (bundle in diag)	
TOR Diag image	09/10/2021: diag-tor2-x86_64-09072021-01	

PlinyH (CPU board)	Image file	Image version / date
BUILD	Pilot	
BIOS	06/27/2021: 16777216 Jul 12 23:57 hewittlake-plinyh-g13-bios-v1.8.bin	v1.08
IO-FPGA PROM	08/22/21: io_pliny_h_dual_image_signed_v11.bin.spi	0x20210806
Aikido	09/17/2020: AKFPGA: espi_plinyst_090920_dv11.bin (Aikido TAM LIB Version : 3-5-1 Aikido Core FW Version : 6.0.5 Aikido Working Bitstream FW Version : 11)	
CPU_VRM (2+1) (U1_VR)	06/30/20: 36756 Jun 30 04:58 17-15985-01-Hewitt-Lake_CPU_VCCIN_VCCSCSUS_2+1.txt	17-15985-01
MEM_VRM (1+1) (U1_MV)	06/30/20: 36756 Jun 30 04:58 17-15986-01-Hewitt-Lake_Mem_P1V05C-1+1_Delayed_Enable.txt	17-15986-01

4.0 SPROM Programming Instruction

4.1 Reference the XXX-PROM Programming Document used to program XXX-PROM

Block #	**Offset**	**Range**	Block Size (Bytes)
1	0x0	0x0 – 0x9F	160
2	0xA0	0xA0 – 0x106	103
3	0x107	0x107 – 0x14D	71

Block # 1 -
Common Block

Byte address		item	Value (decimal/hex)	comment
(hex)	(dec)			
0-1	0-1	block signature	0xabab	0xabab
2	2	block version	3	3
3	3	block length	160	160
4-5	4-5	block checksum		see section on checksum
6-7	6-7	SPROM size	65535	65535 (64k Bytes)
8-9	8-9	block count	3	
0A-0B	10-11	FRU major type	0x6002	See FRU section
0C-0D	12-13	FRU minor type	0	See FRU section
0E-21	14-33	OEM string	Cisco Systems, Inc.	Cisco Systems, Inc.
22-35	34-53	product number	N9K-C9332D-GX2B	
36-49	54-73	serial number		
4A-59	74-89	part number	73-20128-04	
5A-5D	90-93	part revision	**A0**	
5E-71	94-113	mfg deviation	0	used by manufacturing
72-73	114-115	hw rev major	**1**	
74-75	116-117	hw rev minor	**0**	
76-77	118-119	mfg bits	0	
78-79	120-121	eng bits	0	
7A-89	122-137	snmp OID	0.0.0.0.0.0.0.0	Default = 0.0.0.0.0.0.0.0 (software will have its own table, no update plan)
8A-8B	138-139	power consumption	-12500	centiAmp, 999W (12V)
8C-8F	140-143	RMA failure code	0-0-0-0	0
90-9B	144-155	CLEI code	**CMM6510ARA**	
9C-9F	156-159	VID	**V01**	Version ID Default = V01

Block #2 -

Byte offset		item	Value (decimal/hex)	comment
(hex)	**(dec)**			
0-1	0-1	block signature	0x6002	0x6002
2	2	block version	2	2
3	3	block length	103	103
4-5	4-5	block checksum		see section on checksum
6-D	6-13	feature bits	0	
E-15	14-21	hw changes bits	0x10	0x10 Ring E2 ASIC
16-17	22-23	card index	21188	
18-1D	24-29	MAC base		Auto-generated

1E-1F	30-31	MAC length	142	*142(= #ports(32*4)+2+12)*
20	32	EOBC connections	0	
21	33	EPLD num	0	
22-3F	34-63	EPLD versions	0	uint16*15 or uint8*30
40-4F	64-79	Port info	2-34;7-1	type-num; type-num;...
50-51	80-81	SRAM size	0	in kB
52-61	82-97	8 temp sensor info (major/minor)	60/42	1.Intake temp sensor
			80/70	2 Exhaust temp sensor
			90/80	3:X86 Processor
			110/100	4:CPU VRM
			120/80	5: ASIC
			110/100	6. DVDD VRM
			-128/-128	N/A
			-128/-128	N/A
62-63	98-99	max connector power	12500	centiAmp
64-65	100-101	cooling requirement	210	cfm, see Cooling Req Section
66	102	ambient temperature	55	degrees Celsius

Block #3 -
Sensor Block

Byte offset		item	Value (decimal/hex)	comment
(hex)	(dec)			
0-1	0-1	block signature	0x6008	0x6008
2	2	block version	1	1
3	3	block length	71	71
4-5	4-5	block checksum		see section on checksum
6	6	number of valid sensors	0	# of valid sensors in his block
7 - 46	7 - 70	32 temp sensor info (major/minor)	-128/-128	NA
			-128/-128	NA
			-128/-128	NA
			-128/-128	NA
			-128/-128	NA
			-128/-128	NA
			-128/-128	NA
			-128/-128	Sensor instances 15 - 39

5.0 PCA Rework

References

5.1 EDCS-643205 PCAMAP Standardization Document
5.2 EDCS-605019 PCA Assembly Best Practices and Guidelines
5.3 EDCS-7000160 ECO Process & Tools Procedure
5.4 EDCS-7003900 Revision Version Policy
5.5 EDCS-7003340 BOM Structure Policy
5.6 EDCS-231946 Cisco UDI Compliance Specification
5.7 EDCS-231945 Unique Device Identifier (UDI) Policy
5.8 EDCS-7024110 CLEI Code Process