

3604A, 3624A FAMILY 4K (512 × 8) HIGH-SPEED PROM

	3604A-2 3624A-2	3604A 3624A	3604AL
Max. T _A (ns)	60	70	90
Max. ICC(mA)	170	170	130/25*

*Standby Current When The Chip is Deselected.

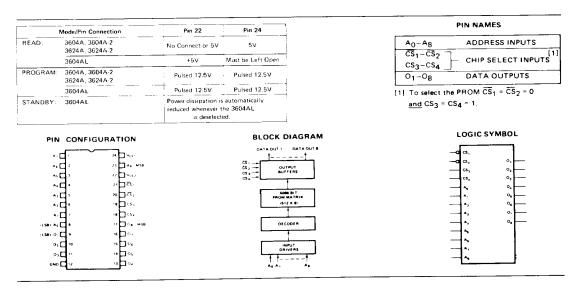
- Fast Access Time
 --60ns Max (3604A-2, 3624A-2)
- Low Standby Power Dissipation
 (3604AL) --32μW/Bit Max
- Open Collector (3604A)
 or Three State (3624A)
 Outputs

- Four Chip Select Inputs For Easy Memory Expansion
- Polycrystalline Silicon Fuse
 For Higher Reliability
- Hermetic 24 Pin DIP

The Intel® 3604A/3624A are 4096-bit bipolar PROMs organized as 512 words by 8 bits. The fast second generation 3604A/3624A replaces its Intel predecessor, the 3604/3624. Higher speed PROMs, the 3604A-2/3624A-2, are now available at 60 ns. All 3604A/3624A specifications, except programming, are the same as or better than the 3604/3624. Once programmed, the 3604A/3624A are interchangeable with the 3604/3624

The PROMs are manufactured with all outputs initially logically high. Logic low levels can be electrically programmed in selected bit locations. Both open collector and three-state outputs are available. Low standby power dissipation can be achieved with the 3604AL. The standby power dissipation is approximately 20% of the active power dissipation.

The 3604A/3624A are available in a hermetic 24-pin dual in-line package. These PROMs are manufactured with the time-proven polycrystalline silicon fuse technology.



PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions

Absolute Maximum Ratings*

Temperature Under Bias	-65°C to +125°C
Storage Temperature	-65°C to +160°C
Output or Supply Voltages	-0.5V to 7 Volts
All Input Voltages	1.6 to 5.5V
Output Currents	100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for $V_{CC} = +5.0V) \pm 5\%$, $T_A = 0$ °C to +75°C

		Limits					
Symbol	Parameter	Min.	Typ. ^[1]	Max.	Unit	Test Conditions	
İFA	Address Input Load Current		-0.05	-0.25	mA	V _{CC} = 5.25V, V _A = 0.45V	
IFS	Chip Select Input Load Current		-0.05	-0.25	mA	$V_{CC} = 5.25V, V_S = 0.45V$	
I _{RA}	Address Input Leakage Current		1	40	μΑ	$V_{CC} = 5.25V, V_A = 5.25V$	
I _{RS}	Chip Select Input Leakage Current			40	μΑ	V _{CC} = 5.25V, V _S = 5.25V	
V _{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V _{CC} = 4.75V, I _A = -10 mA	
V _{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	$V_{CC} = 4.75V$, $I_S = -10 \text{ mA}$	
V _{OL}	Output Low Voltage		0.3	0.45	V	V _{CC} = 4.75V, I _{OL} = 15 mA	
I _{CEX}	Output Leakage Current			100	μΑ	V _{CC} = 5.25V, V _{CE} = 5.25V	
I _{CC1}	Power Supply Current (3604A, 3604A-2, 3624A, and 3624A-2)		130	170	mA	$V_{CC1} = 5.25V, V_{A0} \rightarrow V_{A8} = 0V,$ $\overline{CS}_1 = \overline{CS}_2 = 0V, CS_3 = CS_4 = 5.25V$	
I _{CC2}	Power Supply Current (3604AL) Active		100	130	mA	$V_{CC2} = 5.25V$, $V_{CC1} = Open$ $\overline{CS}_1 = \overline{CS}_2 = 0.45V$, $CS_3 = CS_4 = 2.4V$	
	Standby		15	25	mA	$\overline{\text{CS}}_1 = \overline{\text{CS}}_2 = 2.5\text{V}$	
VIL	Input "Low" Voltage			0.85	V	V _{CC} = 5.0V	
V _{IH}	Input "High" Voltage	2.0			V	V _{CC} = 5.0V	

3624A FAMILY ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
lol	Output Leakage for High Impedance Stage			100	μΑ	$V_O = 5.25 \text{V or } 0.45 \text{V},$ $V_{CC} = 5.25 \text{V}, \overline{CS}_1 = \overline{CS}_2 = 2.4 \text{V}$
¹ sc ^[2]	Output Short Circuit Current	-20	-25	-70	mA	V _O = 0V, V _{CC} = 4.75V
V _{OH}	Output High Voltage	2.4			٧	I _{OH} = -2.4mA, V _{CC} = 4.75V

NOTES: 1. Typical values are at 25°C and at nominal voltage.

2. Unmeasured outputs are open during this test.

A. C. Characteristics $V_{CC} = +5V \pm 5\%$, $T_A = 0^{\circ}C$ to $+75^{\circ}C$

SYMBOL	PARAMETER	MAXII	NUM LIMIT	S (ns)	UNIT	TEST CONDITIONS	
STRIBOL		3604A-2 3624A-2	3604A 3624A	3604AL			
t _{A++} , t _A t _{A+-} , t _{A-+}	Address to Output Delay	60	70	90	ns	$\overline{CS}_1 = \overline{CS}_2 = V_{1L}$ and $CS_3 = CS_4 = V_{1H}$ to Select the PROM	
t _{S++}	Chip Select to Output Delay	30	30	30	ns	to delect the trioin	
t _S	Chip Select to Output Delay	30	30	120	ns		

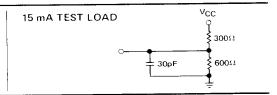
Capacitance (1) T_A = 25°C, f = 1 MHz

SYMBOL		LIMITS		UNIT	TEST CONDITIONS	
	PARAMETER	TYP.	MAX.	UNII	TEST CONDITIONS	
CINA	Address Input Capacitance	4	10	pF ;	V _{CC} = 5V	V _{IN} = 2.5V
C _{INS}	Chip-Select Input Capacitance	6	10	pF	V _{CC} = 5V	V _{IN} = 2.5V
C _{OUT}	Output Capacitance	7	15	pF	V _{CC} = 5V	V _{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz



Waveforms

