1. Support for Additional Instructions:
   * New instructions:
     + jalr (Jump and Link Register)
     + lui (Load Upper Immediate)
     + auipc (Add Upper Immediate to PC)
     + ecall (Environment Call)
2. PCTargetSrc Control Signal:
   * A new output PCTargetSrc has been added to the maindec module and propagated through the pipeline stages (Controller, Datapath).
3. Modified ALUControl Width:
   * The ALUControl signal in the aludec module is now 4 bits wide
4. Changes in maindec Logic:
   * The controls logic in maindec is now 14 bits wide to accommodate the new PCTargetSrc signal.
   * The case statement in maindec includes entries for the new instructions (jalr, lui, auipc, ecall) and sets the appropriate control signals for them.
5. funct3M Signal:
   * A new signal funct3M has been added and passed between modules (top, riscv, datapath, dmem).
6. Modification to dmem Module:
   * The dmem module now accepts funct3M as an input.
7. ALUSrc Width Change:
   * The ALUSrc signal in the controller module is now logic [1:0].
8. mux2 Instance in datapath:
   * The mux2 instance for srcbmux in the datapath now has a width of #(32), explicitly defining the width.