Digital Design and Computer Architecture

Lab 5: Adventure Game 2 [PRELAB and IN-LAB ASSIGNMENT]

0. Introduction

Total points assigned to ALL lab 5 assignments- 30 points

1. Lab 5 is a system Verilog implementation of Lab 4. There are some minor changes and hence "2" in the title.
2. You need to upload your design to the Terasic board and play the game in real time!
3. Remember to adapt your design from Lab 4 so that the NEW modifications are taken into consideration.
4. This is the prelab assignment for Lab 5 which is be worth certain points (TBD). Lab 4 assignment is directly also part of the preparation for Lab 5.
5. There is an in-lab assignment which is worth certain points (TBD).
6. We recommend you first read the workflow section at the end of this document so that you are familiar with what are the expectations and requirements of this lab.

7. To learn about system Verilog, you can study Chapter 4 of the course textbook. This chapter will be a helpful reference for this lab assignment.

1. Design, Schematic and Simulation

[Picking up from where Lab 4 left off]

Changes to the game design requirements

1. The Dragon's Den is now in the **SOUTH-EAST direction** from the Rapid River in Lab 5 instead of the East direction as in Lab 4. This means that both South and East direction need to be asserted simultaneously to make the hero go from the Rapid River to the Dragon's Den.
2. The room states in the Room FSM need to persist, until a legal direction input (or reset) is asserted. Here legal direction means a direction that can directly lead to another room from the current room. For example, the only legal direction from Cave of Cacophony is East, while for Twisty Tunnel both West and South are legal directions
3. Note that for the Dragon's Den you do not need to make the persistence assumption because by design the hero will automatically end up in either the Victory Vault or the Grievous Graveyard, depending on whether they have the Vorpal Sword.
4. Just like the Room FSM there is a persistence requirement for the Sword FSM. Once the Vorpal Sword output is asserted, it needs to persist until reset is asserted.

The Approach

1. Start Quartus and create a new project named "lab05_xx" (where xx are your initials).
2. **[TIP]** In system Verilog, always make sure that the file name for your module matches your module name.
3. Just like Lab 4, Lab 5 also uses a hierarchical design. You will first design a D-Flip Flop in system Verilog. Then you will design the Room FSM and Sword FSM in system Verilog, both of which will use the D-Flip Flop module that you designed previously. Now using these two FSM modules, you will design the Game module.
4. You can reuse the Boolean equations that you derived in Lab 4, but remember to modify them so that the changes described in the previous section are taken care of.

The Design [Prelab report portion of this assignment; worth 2 points; due in the week of 10/10/2022 before coming in for Lab 5]

1. First, design a module for D-Flip Flop in system Verilog.
2. **[TIP]** This module will use the following basic structure-

```
module d_ff (input logic d, clk,
             output logic q);

            always @ (posedge clk) begin
            //your own module definition
            end

endmodule
```

3. Once you are done, make this module as the top-level design and verify it works as expected using simulation waveforms. You can use a manually generated clock signal for the simulation.
4. Now, design the Room FSM module in system Verilog.
5. **[TIP]** This module will use the following basic structure-

```
module room (input logic clk, n, s, e, w, v, reset,
            output logic s6, win, s5, d, s4, s3, sw, s2, s1, s0);

            //one instance of D-Flip Flop for each room state

endmodule
```

6. Now make this module as the top-level design and verify it using simulation waveforms. Again, use a manually generated clock.
7. Next step is to design the Sword FSM module.
8. **[TIP]** This module will use the following basic structure-

```
module sword (input logic sw, reset, clk,
            output logic v);

            //one instance of D-flip flop to store sword FSM state

endmodule
```

9. Again, make this module as the top-level design. Using simulation waveforms, verify that it works as expected.
10. Now you are ready to define the Game module. This module will use an instance of Room FSM module and another instance of Sword FSM module.
11. **[TIP]** This module will use the following basic structure-

```
module game(input logic clk, n, s, e, w, reset,
      output logic s6, win, s5, d, s4, s3, sw, s2, s1, s0, v);

      //one instance of Room FSM module
      //one instance of Sword FSM module

endmodule
```

12. Make the game module as the top-level design. Use simulation waveforms to verify that it works as expected.
13. Check the "What to turn in" section for prelab assignment to know what type of waveforms you need to include in your report.

Uploading your design to the board [In-Lab report portion of this Assignment; worth 8 points; due in the week of (TBD) after completing Lab 5 in-lab sessions]

1. Once you are confident that the game module works as per the design requirements, you can go ahead and upload it to the Terasic Board.
2. First, you need to make the pin assignments. Use your experience from Lab 1 and Lab 2 to make appropriate pin assignments.
3. Note that for the clock input, you will be using the onboard clock available on the Terasic Board. Use the Terasic Board user manual on Canvas to find where this clock is located.
4. After making the pin assignments, compile your project. Make sure game module is set as top-level design.
5. Once the compilation completes successfully, upload your design to the Terasic board using the "programmer" from the Toolbar.
6. Now, play the game on the board.
7. Once you are confident that it works as expected, have a TA check your design (optional).

2. What to Turn In

2.1. For the Prelab Report

- **Due date-**Lab 5 prelab report is due in the week of TBD before coming in for Lab 5
- **Points assigned to prelab Assignment -** Certain points (TBD) for Lab 5 come from the prelabassignment report submission.
- **Contents of the Prelab report-**

You must submit an electronic copy of the following items (in the indicated order, and each part clearly labeled) via Canvas. Submit it to the Lab 5 Prelab Assignment. All items should all be included in a single file (.pdf).

1. Please indicate how many hours you spent on this lab**.** This will be helpful for calibrating the workload for the upcoming labs.
2. An image of the code you wrote for your D-Flip Flop module.
3. An image of the code you wrote for your Room FSM module.
4. An image of the code you wrote for your Sword FSM module.
5. An image of the code you wrote for your Game module.
6. A Google Drive (or similar cloud storage) link to a zipped version of your entire Quartus project folder for Lab 5. This should include all system Verilog (.sv) files for each of the modules and all the waveform (.vwf) files. **Please make sure that last edited date is visible on this cloud link and that the last edited date does not cross the in-lab assignment due date. Failure to do so will result in penalty towards your total Lab 5 score.**
7. Two images of your simulation waveforms: one that shows you playing the game and winning (entering "Victory Vault"), and another that shows an example of losing the game (entering the "Grievous Graveyard"). **Your signals must be printed in the following order: `clk`, `n`, `s`, `e`, `w`, `r`, `win`, `d`, $s_6 \ldots s_0$, `sw`, `v`.**

2.2. For the In-lab Report

- **Due date-** Lab 5 in-lab report is due in the week of (TBD), after completing the in-lab session for Lab 5
- **Points assigned to in-lab Assignment-** Certain points (exact number TBD) for Lab 5 come from the in-lab assignmentreport submission.
- **Contents of the In-lab report-**

  You must submit an electronic copy of the following items (in the indicated order, and each part clearly labeled) via Canvas. Submit it to the Lab 5 In-lab Assignment. All items should all be included in a single file (.pdf).

  1. To the pdf document from your prelab assignment, just add a section for the in-lab assignment.
  2. Please indicate how many hours you spent on this assignment**.** This will be helpful for calibrating the workload for the upcoming labs.
  3. Include a table indicating how you assigned the pins for each of the inputs and outputs of the game. This should help us understand your pictures of the code working on the board.

4. Take at least 5 pictures of the game working on the board. Include these pictures in the report and in each picture, indicate what stage of the game is shown by indicating the room that the hero is in.

2.3. For the mandatory assessment

- **Due date-** Lab 5 assessments will be performed over two weeks (week of TBA and week of TBA). Assessment slots will be assigned through a google sign-up sheet on a first-come-first-served basis.
- **Points assigned to mandatory assessment-** Certain points (TBA) for Lab 5 assignment come fromthe mandatory assessment.
- **Contents of the mandatory assessment-**

  Exact questions for the assessment will be revealed to you at your assigned slot. To give you an idea, here is an outline of what you might be asked. You will be required to make certain changes to your design in a rapid-fire manner. A few examples of such "changes"-

  1. Changes in the definition of certain modules that you created
  2. Changes in the pin assignments so that input/output is assigned to a different hardware on the board.
  3. Changes in the output requirements.
  4. Or something else along these lines.

  The idea is to ask the student to make a few random changes to their game design and see how they respond.

3. Workflow for Lab 5

You are expected to work on the system Verilog design for Lab 5 as a prelab assignment. This is crucial because during the in-lab session you will only have time to adapt and run your code on the board. This in turn is crucial because you will have an on-board assessment the following week that will require you to make changes to your design on the board in a rapid-fire manner.

Note that you must plan to be present in-person for the mandatory Lab 5 assessment during both the weeks. We can't guarantee what slot you will get in the sign-up sheet and if you are not able to attend for any undocumented reasons, then we would not be able to help. You will simply be marked absent for the assessment.