Digital Design and Computer Architecture

Lab 2: D FLIP-FLOP [IN-LAB ASSIGNMENT]

0. Introduction

Total points assigned to ALL lab 2 assignments- 10 points

In this lab you will design a simple D flip-flop on Quartus. Along the way, you will learn how to use the Altera field-programmable gate array (FPGA) tools to enter a schematic, simulate your design, and download your design onto a chip.

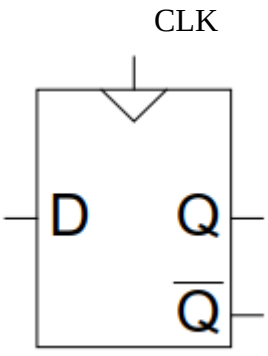
After completing the lab, you are required to turn in something from each part, as a lab report. Refer to the "What to Turn In" section at the end of every handout to check what are the submission requirements for each prelab assignment or in-lab assignment.

If you haven't already done so, go through the Lab 2 Prelab assignment and read all three instruction sets.

This lab is essentially similar to lab 1, so feel free to go back to Lab 1 instruction files anytime you need help.

0.1. Background

The objective of this lab is to design, simulate, and implement a D flip-flop:



Remember the working principle of D flip-flop: on the edge of the clock (when ***CLK* rises from 0 → 1**), *D* passes through to *Q*

0.2. Quartus installation

We want students to be well prepared at home so that they have more time to work on FPGA board during lab section. Therefore, students are required to install Quartus on their PC and complete assignments involving Quartus for the prelab assignment.

Using the following link to download Quartus Lite version 17.0:

Windows:
https://www.intel.com/content/www/us/en/software-kit/669557/intel-quartus-prime-lite-edition-design-software-version-17-0-for-windows.html

After downloading, unzip the file, open the folder and run the setup file (Windows Batch File).

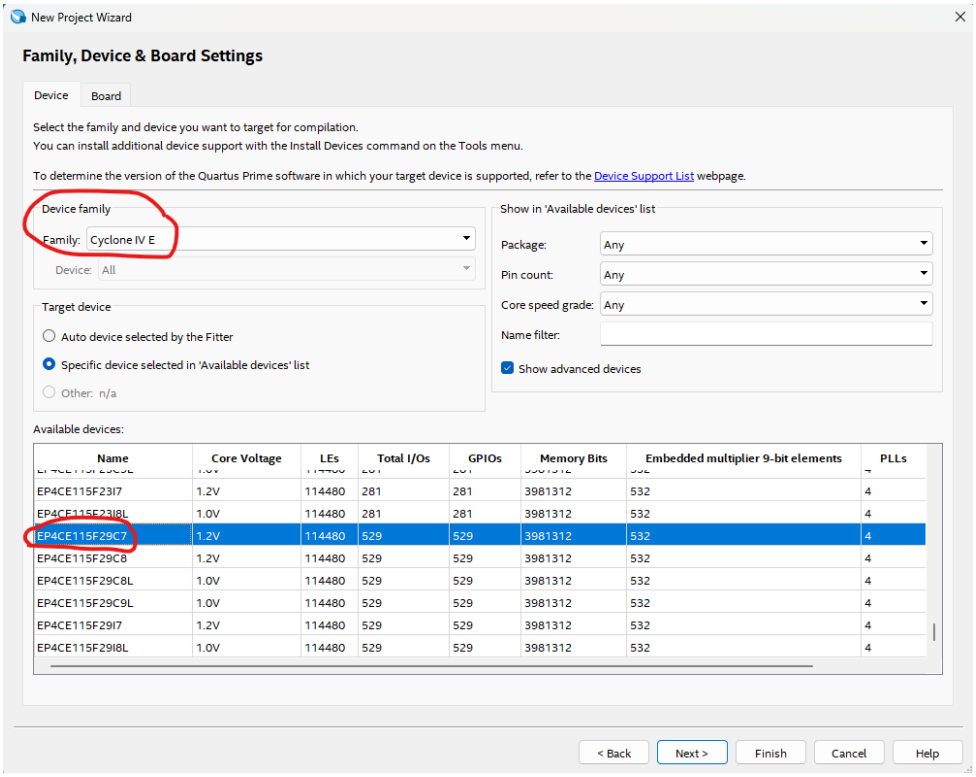
Linux:
https://www.intel.com/content/www/us/en/software-kit/669553/intel-quartus-prime-lite-edition-design-software-version-17-0-for-linux.html

If for some reason that doesn't work, you can use ECE lab computers remotely via https://vlab.rutgers.edu/

1. Design Implementation

After having install Quartus on your personal PC, you can either work on your own PC or use one of the ECE lab PCs.
Once you have logged into a system that works, create your Quartus Project for lab 2.

Make sure you pick the correct device and device family as follows:

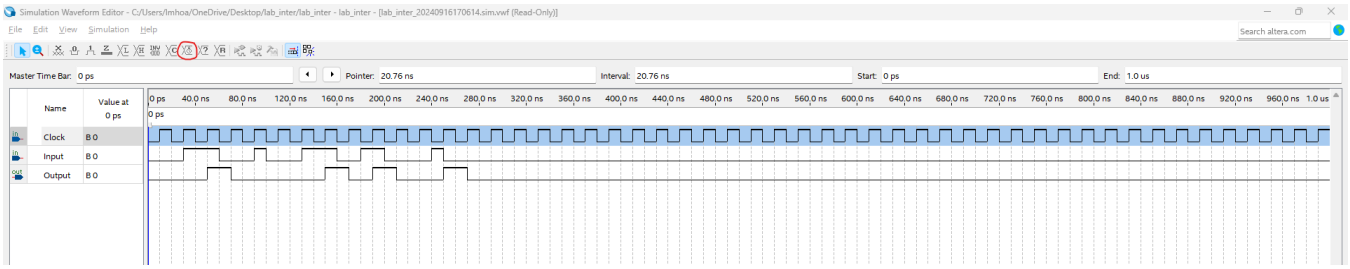


1. Once you have created a new project, go ahead and open a new file for Block Diagram design.
2. In this file, pick the D flip-flop logic gate from the library of available gates and place it on the canvas. D flip-flop can be found at **Symbol tool → (Libraries) primitives → storage → dff**.
3. Next pick an input port and place one for each of the two input ports of the dff gate. Also place an output port for the output from the dff gate.
4. Once you have placed all the ports and gates on the canvas, go ahead and save your design.
5. After saving your design, you need to compile your design.

2. Simulation

To create a clock signal for CLK input of dff, use the **Overwrite Clock** button. The you can pick the period as 10 or 20 nano seconds (ns)

A sample simulation:



3. What's next?

Run your design on your assigned FPGA board following instructions as in lab 1.

4. What to Turn In

Points assigned to In-lab Assignment- some points (to be defined) for Lab 2 come from In-lab assignment report submission

You must submit an electronic copy of the following items via Canvas. Submit to the Lab2 In-lab Assignment. These should all be included in a single "pdf" file. Be sure to label each section and organize them in the following order. Messy or disorganized labs will lose points.

1. Please use ECE Lab Report Cover Page (can be found in the Files Tab on canvas).

2. Please indicate how many hours you spent on this lab. This will be helpful for calibrating the workload for the upcoming Lab assignments.

3. Picture of your schematic design (if you already have this picture from your Prelab work, you can reuse it)

4. Picture of simulation waveform (if you already have this picture from your Prelab work, you can reuse it)

5. Include pictures of the code running properly on the board

Some Quartus Tips

- Make sure you don't have any spaces, and symbols like "-" in any of your folder or file names.
- Some CAD tools are case sensitive and others are case insensitive. Never use two different capitalizations of the same signal because some tools may treat them as different signals while others may treat them as the same signal. The easiest solution is to be consistent in your choice of capitalization.