MCA-103 Computer Organization & Architecture   L   T
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Course Objectives:
To introduce the fundamental concepts of digital computer organization and architecture. To develop a basic understanding of the building blocks of a digital computer system. To enable understanding of how these building blocks are organized together to architect a digital computer system. To enable understanding of how various functional units of a digital computer system interacts to meet the processing requirements of the user.

UNIT – I

Digital Logic Circuit: Digital Computers, Logic Gates, Boolean Algebra, Map Simplification, Combinational Circuits, Flip Flops, Sequential Circuits
Digital Components& Data Representation: Decoders, Multiplexers, Registers, Shift Registers, Binary Counters, Memory Units, Data Types, Complements, Fixed Point Representation, Floating Point Representation, Other Binary Codes, Error Correction Codes

UNIT – II

Register Transfer and Micro-operations: Register Transfer Language, Register transfer, Bus and Memory Transfer –Three State Bus Buffer, Memory Transfer; Arithmetic Micro-operations – Binary Adder, Binary Adder-Subtractor, Binary Incrementer, Arithmetic Circuit; Logic Micro-operations, Shift Micro-operations, Arithmetic Logic Shift Unit.
Basic Computer Organization: Instruction codes – Stored Program Organization, Indirect Address; Computer Registers – Common Bus System; Computer Instructions – Instruction Set Completeness; Timing and Control; Instruction Cycle – Fetch and Decode, Determine the Type of Instruction, Register-Reference Instructions; Memory Reference Instructions; Input-Output and Interrupt, Complete Computer Description, Design of Basic Computer, Design of Accumulator Logic

UNIT – III

Programming the Basic Computer: Machine Language, Assembly Language, Introduction to Assembler, Program Loops, Programming Arithmetic and Logic Operations
Micro programmed Control: Control Memory, Address Sequencing – Conditional Branching, Mapping of Instructions, Subroutines, Micro program Example – Computer Configuration, Microinstruction Format, Symbolic Microinstructions, Fetch Routine, Symbolic Micro program, Binary Micro program, Design of Control Unit – Micro program Sequencer
Central Processing Unit: Introduction, General Register Organization, Stack Organization – Register Stack, Memory Stack, Reverse Polish Notation, Evaluation of Arithmetic Expressions, Instruction Formats – Three-, Two-, One- and Zero-Address

Instructions, Addressing Modes, Data Transfer and Manipulation, Program Control – Status Bit Conditions, Conditional Branch Instructions, Subroutine Call and Return, Program Interrupt, Types of Interrupt, RISC & CISC Characteristics, Overlap Register Window

UNIT – IV

Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processors

Computer Arithmetic – Addition and Subtraction, Multiplication Algorithms, Division Algorithms, Floating Point Arithmetic Operations, Decimal Arithmetic Unit and Operations

Input-Output Organization: Peripheral Devices, Input-Output Interface, Modes of Transfer – Programmed I/O, Interrupt-Driven I/O, Priority Interrupt, Direct Memory Access (DMA), Input-Output Processor (IOP), Serial Communication

Memory Organization: Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory, Virtual Memory, Memory Management Hardware

Text Book:
1. Computer System Architecture, by M. Morris Mano, Third Edition. 2007. Low Price Edition. Pearson Education

Reference Books:
1. Computer Architecture and Organization, by John P. Hayes. Third Edition. 2017. McGraw Hill Publication.
2. Computer Organization and Architecture: Designing for Performance, by William Stallings. Tenth Edition. 2016. Pearson Education India.

Course Outcomes:

By the end of the course, Students will be able to
CO 1: Explain the working of arithmetic, logic and shift units in a computer system
CO 2: Elucidate the role of instruction set and instruction cycle in program execution
CO 3: Explain concept of interrupts and their handling
CO 4: Elucidate significance of stack and instruction formats
CO 5: Explain various mode of data transfer between memory and I/O devices
CO 6: Elucidate organization and operation of – main memory, auxiliary memory, associative memory and cache memory

Note: In each theory paper, nine questions are to be set. Two questions are to be set from each Unit and candidate is required to attempt one question from each unit. Question number nine will be compulsory, which will be of short answer type with 5-10 parts, out of the entire syllabus. In all, five questions are to be attempted.