Combinational Logic Design: Part 5: 4-Bit Priority Encoder

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1 Introduction

A priority encoder is a combinational circuit that converts multiple binary inputs into a smaller number of outputs, with priority given to the highest-order active input. In this project, we design and implement a 4-bit priority encoder in Verilog HDL, where input D[3] has the highest priority and D[0] has the lowest.

2 Design Description

The 4-bit priority encoder takes 4 input lines (D[3:0]) and produces:

- A 2-bit binary output (Y[1:0]) representing the highest priority active input
- A valid output (V) that indicates when at least one input is active

2.1 Truth Table

D3	D2	D1	D0	Y1	Y0	V
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

Table 1: Priority encoder truth table (X = don't care)

3 Verilog Implementation

```
`timescale 1ns/1ps

module priority_encoder_4bit (
    input [3:0] D,
    output reg [1:0] Y,
    output reg V
);

always @(*) begin
    V = 1'b1;
    casex(D)
        4'b1xxx: Y = 2'b11; // Highest priority (D3)
        4'b01xx: Y = 2'b10; // D2
        4'b001x: Y = 2'b01; // D1
        4'b0001: Y = 2'b00; // D0
```

```
        default: begin
            Y = 2'b00;
            V = 1'b0;       // No valid input
        end
    endcase
end

endmodule
```

4 Test Bench

```
`timescale 1ns/1ps

module tb_priority_encoder_4bit;
    reg [3:0] D;
    wire [1:0] Y;
    wire V;

    // Instantiate the priority encoder
    priority_encoder_4bit uut (
        .D(D),
        .Y(Y),
        .V(V)
    );

    initial begin
        // Initialize inputs
        D = 4'b0000;

        // Test all possible input combinations
        #10 D = 4'b0000;
        #10 D = 4'b0001;
        #10 D = 4'b0010;
        #10 D = 4'b0011;
        #10 D = 4'b0100;
        #10 D = 4'b0101;
        #10 D = 4'b0110;
        #10 D = 4'b0111;
        #10 D = 4'b1000;
        #10 D = 4'b1001;
        #10 D = 4'b1010;
        #10 D = 4'b1011;
        #10 D = 4'b1100;
        #10 D = 4'b1101;
        #10 D = 4'b1110;
        #10 D = 4'b1111;

        // Additional test cases
        #10 D = 4'b0000;
        #10 D = 4'b0010;
        #10 D = 4'b0100;
        #10 D = 4'b1000;
        #10 $finish;
    end

    initial begin
        $monitor("Time = %0t, D = %b, Y = %b, V = %b",
                 $time, D, Y, V);
    end

endmodule
```

5 Conclusion

- The 4-bit priority encoder was successfully designed and implemented in Verilog HDL.
- The design correctly prioritizes the highest-order active input and provides both the encoded output and a valid signal.
- The test bench verifies all possible input combinations, ensuring the design meets the specified requirements.

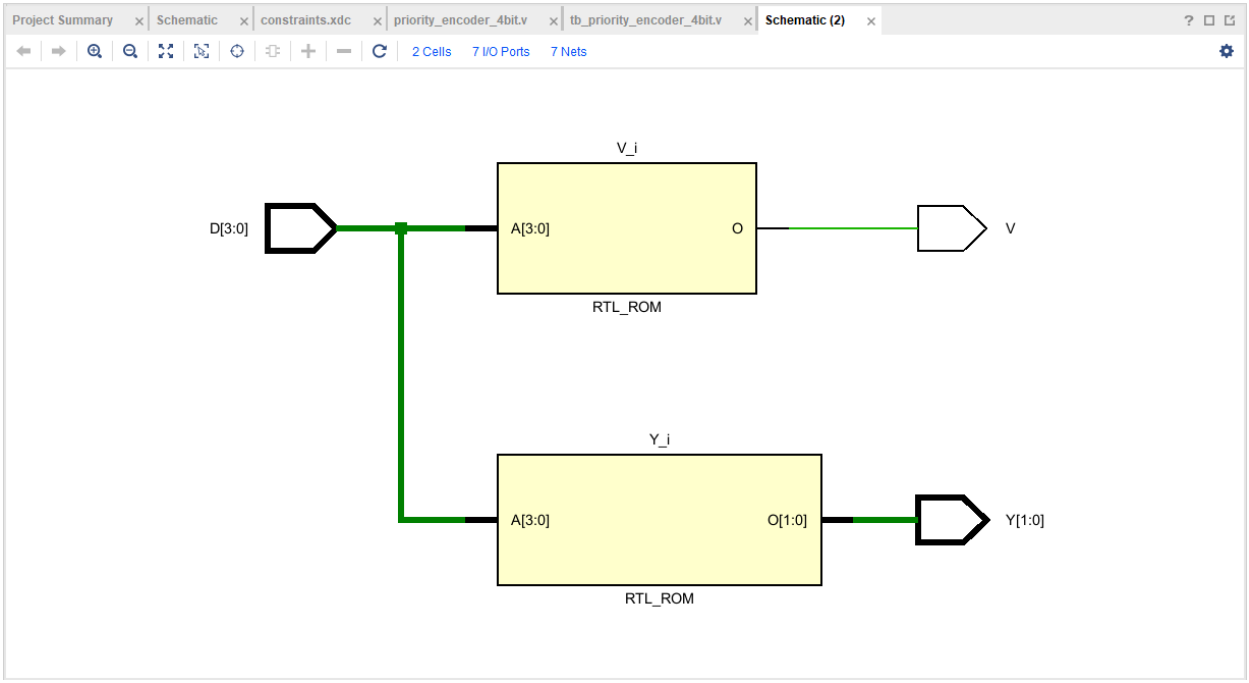

Figure 1: schematic

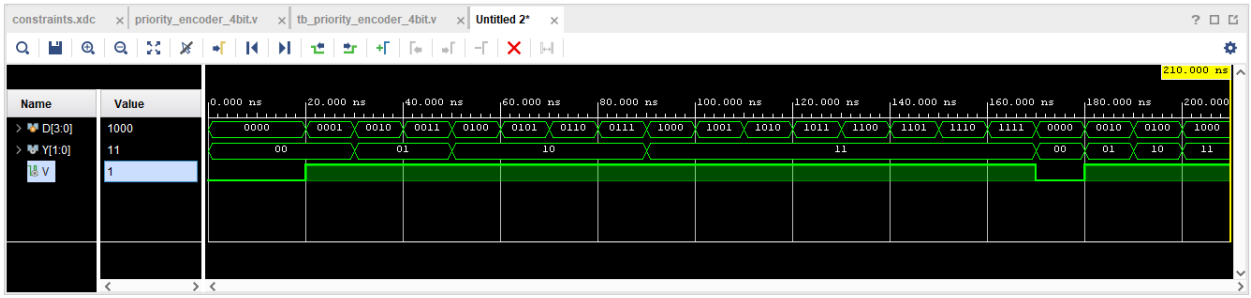

Figure 2: waveform