Combinational Logic Design: Part 3: 3-bit Even Parity Generator

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1 Introduction

A parity generator is a combinational circuit that generates the parity bit for a given set of data bits. In this project, I design a 3-bit even parity generator that produces a parity bit to make the total number of 1s in the 4-bit output (3 data bits + 1 parity bit) even. This type of circuit is commonly used in digital systems for error detection.

2 Design Description

2.1 Specifications

- Input: 3-bit data (A, B, C)
- Output: 1-bit even parity (P)
- Function: P = XOR of all input bits

Truth Table:

A	B	C	P
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

3 Verilog Implementation

```
`timescale 1ns / 1ps
module parity_gen(
    input wire A, B, C,     // 3-bit input
    output wire P           // Parity bit output
);

    assign P = A ^ B ^ C;  // XOR operation for even parity

endmodule
```

Listing 1: 3-bit Even Parity Generator Verilog Code

4 Test Bench Design

- Test all 8 possible input combinations (000 to 111)
- Verify output parity bit matches expected values
- Include delay between test cases for clear waveform observation
- Display both inputs and output in simulation

```
`timescale 1ns / 1ps

module tb_parity_gen;
    // Inputs
    reg A, B, C;
    // Outputs
    wire P;

    // Instantiate the Unit Under Test (UUT)
    parity_gen uut (
        .A(A), .B(B), .C(C), .P(P)
    );

    initial begin
        // Initialize Inputs
        A = 0; B = 0; C = 0;

        // Wait 100 ns for global reset
        #100;

        // Stimulus
        A=0; B=0; C=0; #100; // P=0
        A=0; B=0; C=1; #100; // P=1
        A=0; B=1; C=0; #100; // P=1
        A=0; B=1; C=1; #100; // P=0
        A=1; B=0; C=0; #100; // P=1
        A=1; B=0; C=1; #100; // P=0
        A=1; B=1; C=0; #100; // P=0
        A=1; B=1; C=1; #100; // P=1

        #100 $finish;
    end

    initial begin
        $monitor("Time=%0t A=%b B=%b C=%b P=%b",
                 $time, A, B, C, P);
    end
endmodule
```

Listing 2: Test Bench for 3-bit Even Parity Generator

5 Conclusion

- Verified correct operation through exhaustive test bench
- The design uses minimal logic (just XOR gates) for efficient implementation
- Can be extended to larger bit widths by cascading more XOR gates

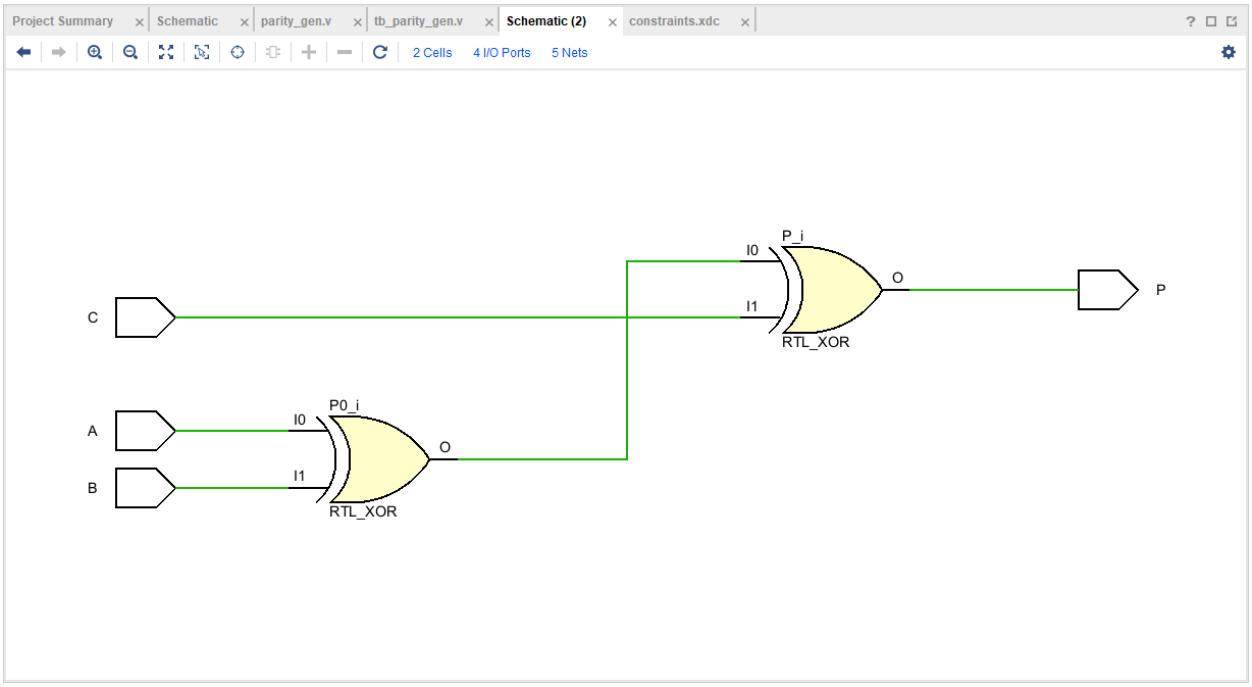

Figure 1: schematic

Figure 2: waveform