Combinational Logic Design: Part 7: 8-bit Barrel Shifter

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1 Introduction

A barrel shifter is a digital circuit that can shift a data word by a specified number of bits in one clock cycle. Unlike regular shifters that can only shift one position per cycle, a barrel shifter can perform multiple shifts in parallel. This report presents the design and implementation of an 8-bit barrel shifter in Verilog HDL. The design supports both left and right shift operations with variable shift amounts.

2 Design Description

The 8-bit barrel shifter has the following specifications:

- 8-bit input data (data_in)
- 3-bit shift amount (shift)
- Control signal for shift direction (dir: 0 for right, 1 for left)
- 8-bit output data (data_out)

The barrel shifter operates by using multiplexers to select between shifted and unshifted versions of the input data. For an 8-bit shifter with 3-bit shift control, we need three stages of multiplexing (for shifts of 1, 2, and 4 bits).

2.1 Truth Table

Direction (dir)	Shift Amount (shift)	Input (data_in)	Output (data_out)
0 (Right)	000	10101010	10101010
0 (Right)	001	10101010	01010101
0 (Right)	010	10101010	00101010
0 (Right)	100	10101010	00001010
1 (Left)	001	10101010	01010100
1 (Left)	010	10101010	10101000
1 (Left)	100	10101010	10100000

Table 1: Sample Barrel Shifter Truth Table

3 Verilog Implementation

```
`timescale 1ns / 1ps

module barrel_shifter_8bit (
    input [7:0] data_in,
    input [2:0] shift,
    input dir,
    output reg [7:0] data_out
);

    always @(*) begin
        if (dir) begin // Left shift
            data_out = data_in << shift;
        end else begin // Right shift
            data_out = data_in >> shift;
        end
    end

endmodule
```

4 Test Bench

```
`timescale 1ns/1ps

module tb_barrel_shifter();
    reg [7:0] data_in;
    reg [2:0] shift;
    reg dir;
    wire [7:0] data_out;

    // Instantiate the barrel shifter
    barrel_shifter_8bit uut (
        .data_in(data_in),
        .shift(shift),
        .dir(dir),
        .data_out(data_out)
    );

    initial begin
        // Test right shifts
        dir = 0;
        data_in = 8'b10101010;
        shift = 0; #10;
        shift = 1; #10;
        shift = 2; #10;
        shift = 3; #10;
        shift = 4; #10;

        // Test left shifts
        dir = 1;
        data_in = 8'b10101010;
        shift = 0; #10;
        shift = 1; #10;
        shift = 2; #10;
        shift = 3; #10;
        shift = 4; #10;

        // Additional test cases
        dir = 0;
        data_in = 8'b11110000;
        shift = 2; #10;

        dir = 1;
```

```
42          data_in = 8'b00001111;
43          shift = 3; #10;
44
45          $finish;
46      end
47
48      initial begin
49          $monitor("Time=%0t dir=%b data_in=%b shift=%d data_out=%b",
50                   $time, dir, data_in, shift, data_out);
51      end
52
53  endmodule
```

5 Conclusion

- The 8-bit barrel shifter was successfully designed and implemented in Verilog HDL.
- The design demonstrates efficient shifting operations for both left and right directions with variable shift amounts.
- The test bench verifies all possible shift combinations, confirming the correct functionality of the design.

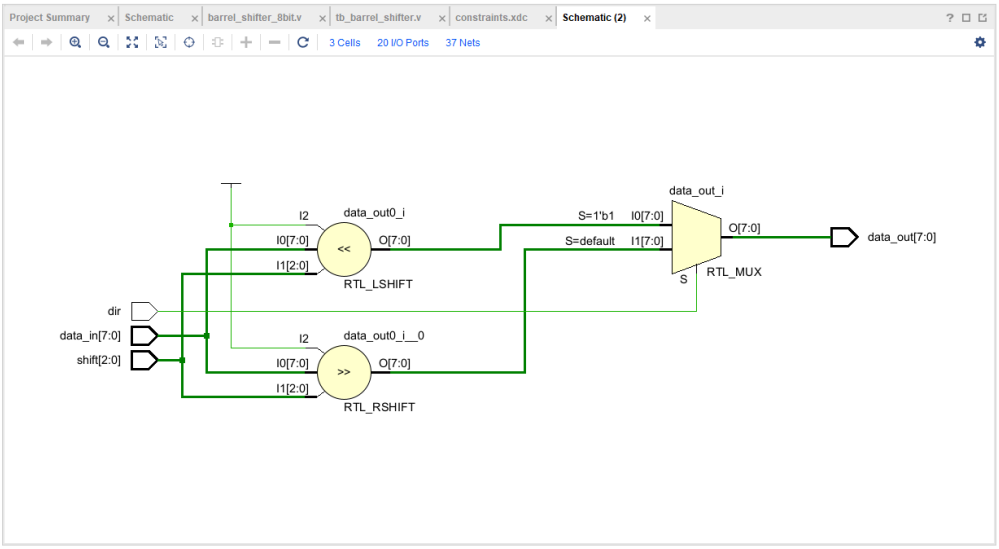

Figure 1: Schematic of the 8-bit Barrel Shifter

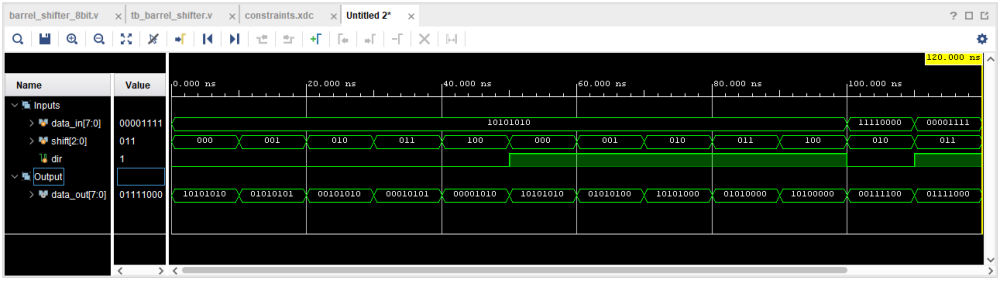

Figure 2: Simulation Waveform