

REVISION HISTORY

DATE:	DESCRIPTION	REVISION
Jaunary . 2014	Created	1.0

Page 1: Revision History

Page 2: KSZ8795/8765 Switch

Page 3: Transformer, LED and RJ45 for Port1 to 4

Page 4: Port 5 with Gigabit PHY KSZ9031RNX

Page 5: Power & Reset

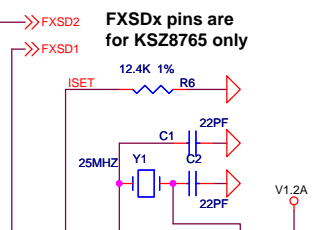
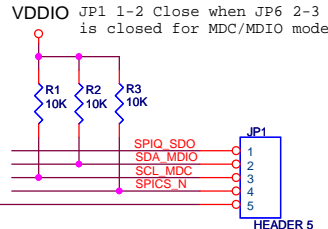
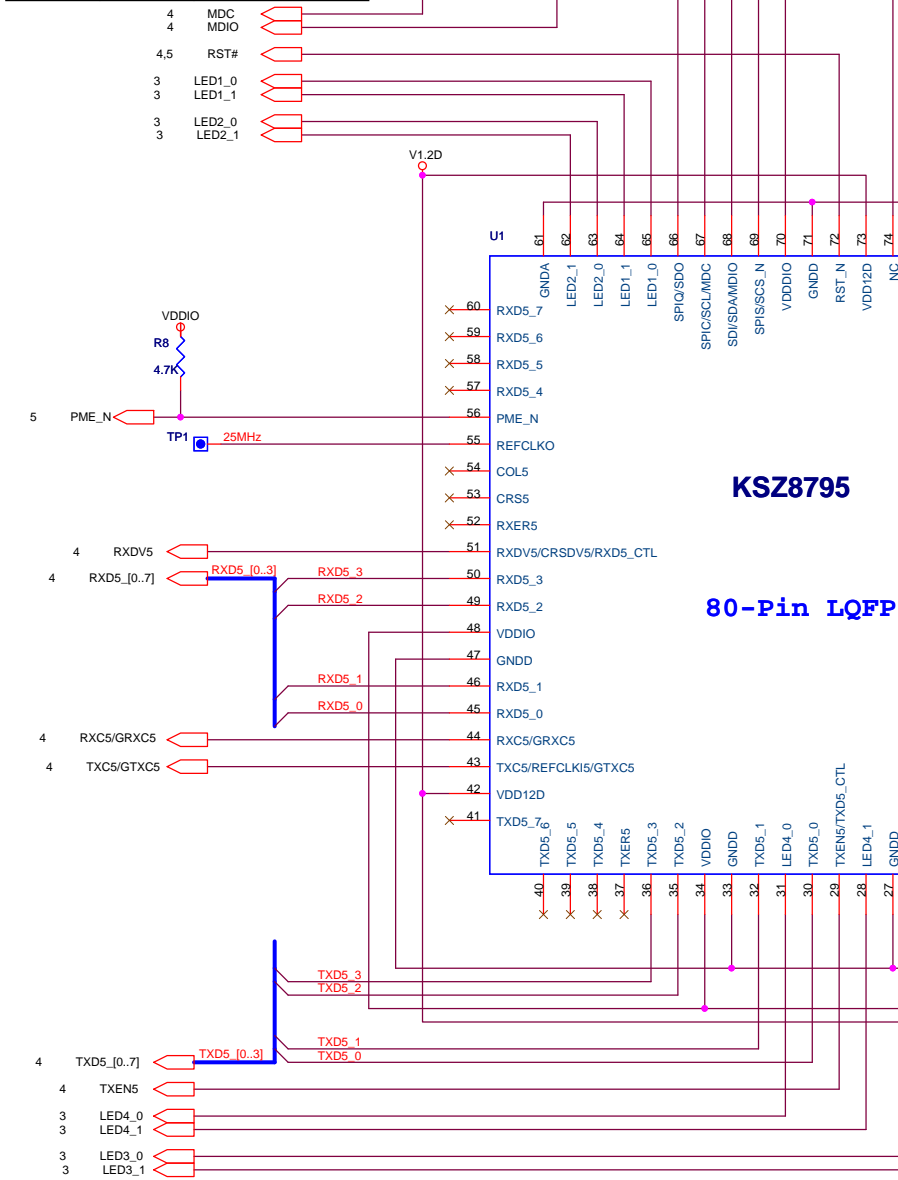
KSZ8795CLX Reference Design Schematics



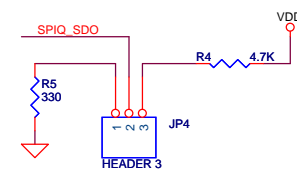
CONFIDENTIAL & PROPRIETARY

Title		
KSZ8795 Reference Schematics		
Size	Document Number	Rev
	Revision History	1.0
Date:	Friday, January 24, 2014	Sheet 1 of 5

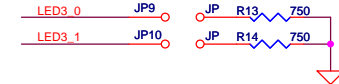
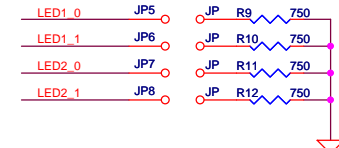
JP2	JP3	Description
1-2 Close	1-2 Close	8795 SPI, MIIM (Default)
2-3 Close	2-3 Close	External MIIM



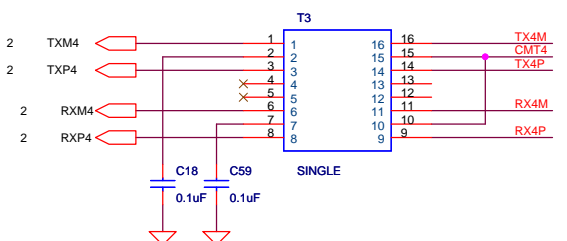
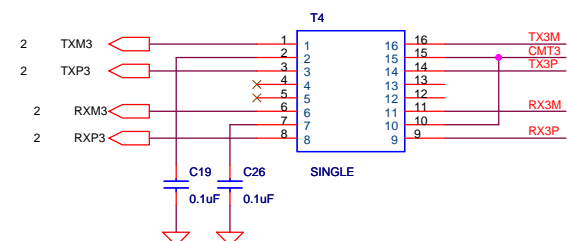
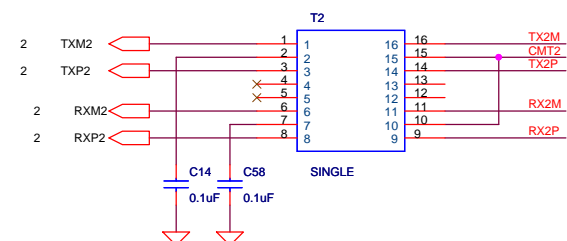
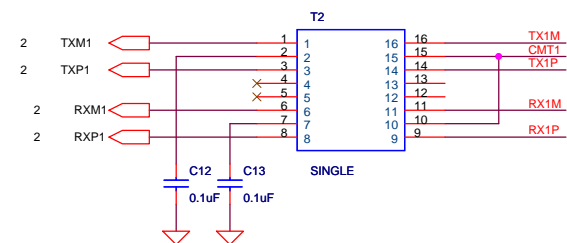
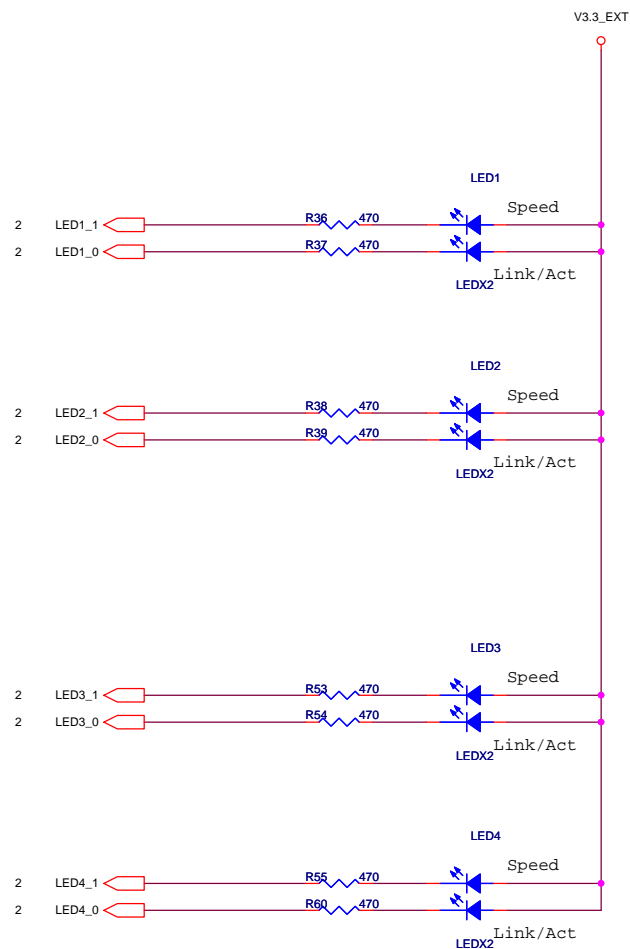
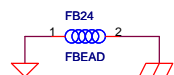
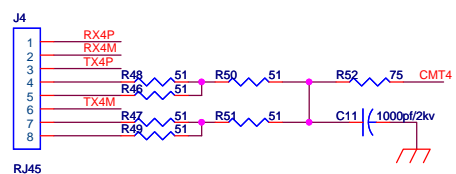
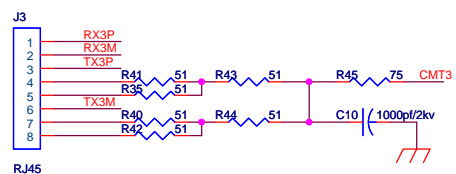
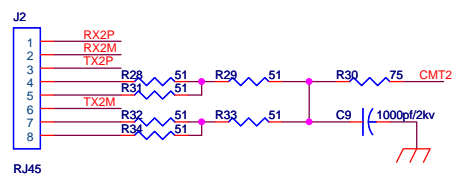
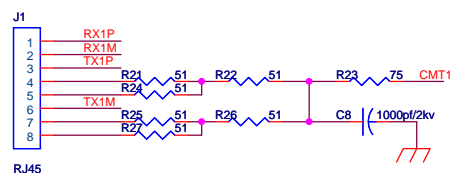
Jumpers	1-2 Closed	2-3 Closed
JP4(SPIQ_SDO)	SPI Slave Mode	MDC/MDIO Mode and JP1 1-2 is Closed too



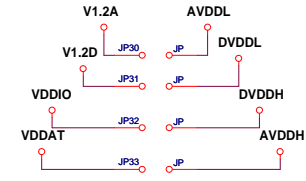
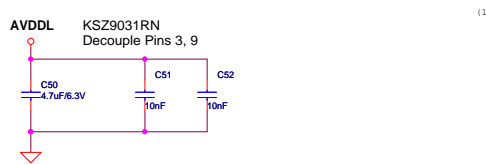
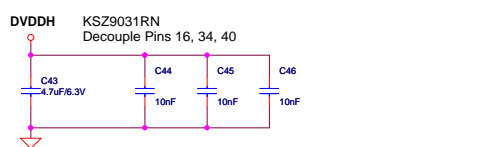
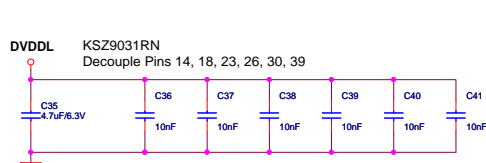
Jumpers	Open (Default)	Closed
JP5(LED1_0)	Open: Gbps mode on port 5	Close: 10/100Mbps on port 5
JP6(LED1_1)	Open: Device clock source from OSC 25MHz in RMII normal mode	Close: Device clock source from SW5-RMII TXC5 in RMII normal mode
JP7(LED2_0)	Open: REFCLKO pin 25MHz Output Enable	Close: REFCLKO pin 25 Mhz output is disabled
JP8(LED2_1)	Open: SW5-MII in MAC mode, SW5-RMII in Clock mode	Close: SW5-MII in PHY mode, SW5-RMII in Normal mode



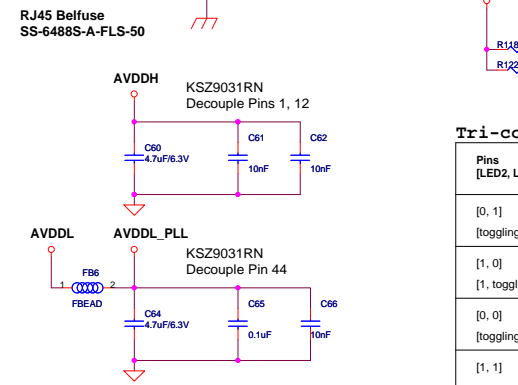
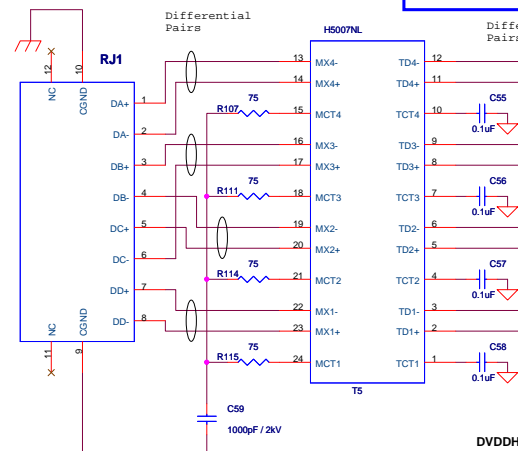
JP10	JP9	SW5-GMAC Mode
Close	Close	MII Mode
Close	Open	RMII
Open	Close	GMII
Open	Open	RGMII (Default)



Pulse H1102
TDK TLA_6T718A
YCL PT163020
Transpower HB726
DELTA LF8505
Bel Fuse S558-5999-U7
(or using a quad transformer H1164NL)



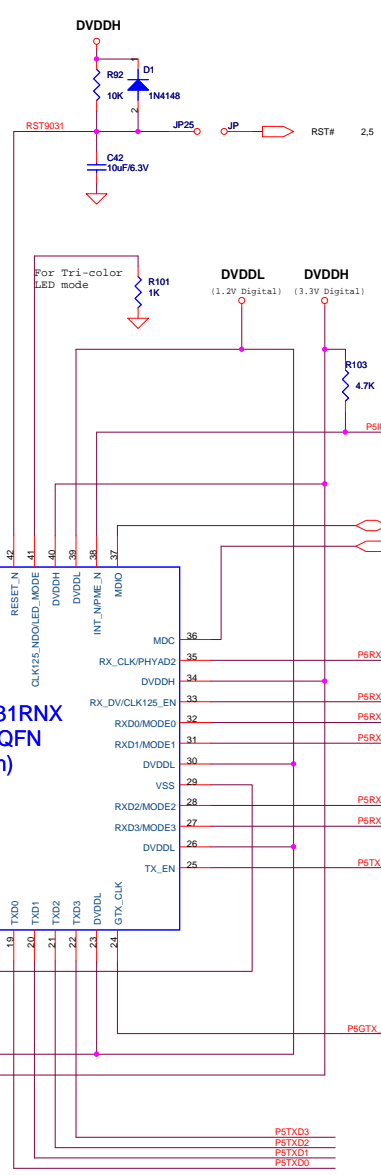
Port 5 Giga Port



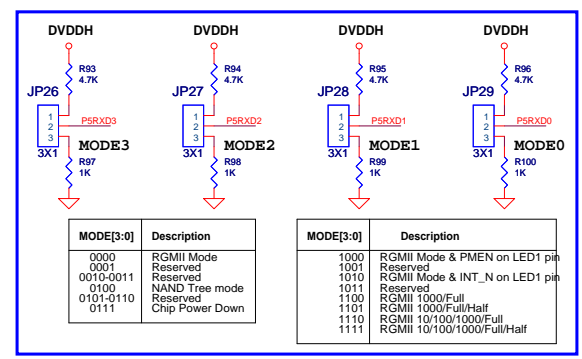
Tri-color Dual LED Mode

Pins [LED2, LED1]	Description	Dual LED Color
[0, 1] [toggling, 1]	Solid Color : 1G Link Blinking : Activity (RX, TX)	Green
[1, 0] [1, toggling]	Solid Color : 100M Link Blinking : Activity (RX, TX)	Red
[0, 0] [toggling, toggling]	Solid Color : 10M Link Blinking : Activity (RX, TX)	Orange
[1, 1]	Link off	None

KSZ9031RXN
48-Pin QFN
(7x7mm)
P-GND

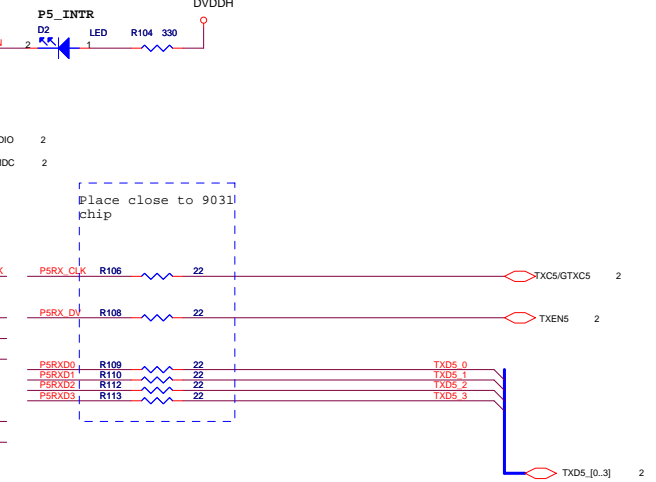


Strapping Pins for MODE Selection

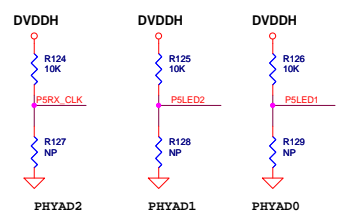
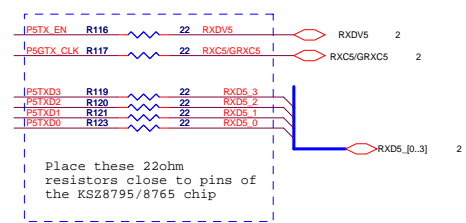


MODE[3:0]	Description
0000	RGMII Mode
0001	Reserved
0010-0011	Reserved
0100	NAND Tree mode
0101-0110	Reserved
0111	Chip Power Down

MODE[3:0]	Description
1000	RGMII Mode & PMEN on LED1 pin
1001	Reserved
1010	RGMII Mode & INT_N on LED1 pin
1011	Reserved
1100	RGMII 1000/Full
1101	RGMII 1000/Full/Half
1110	RGMII 10/100/1000/Full
1111	RGMII 10/100/1000/Full/Half



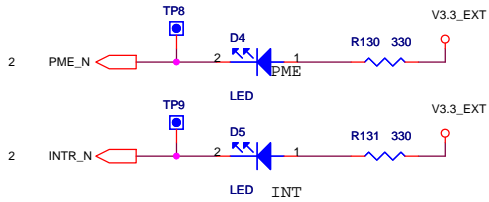
Traces of TX group and RX group should be Equal length individually between KSZ9031 to KSZ8795/8765 device



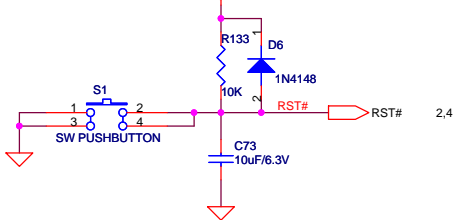
PHY address bits [4:3] are always set to "00"

Strapping PHY Address PHYAD[2:0] = 7 (111) for Port 5

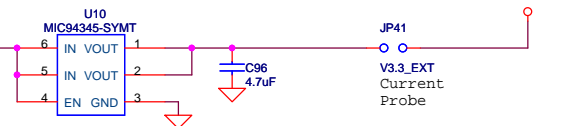
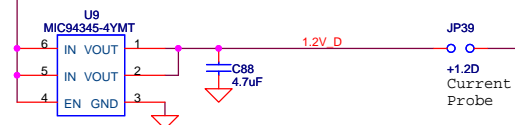
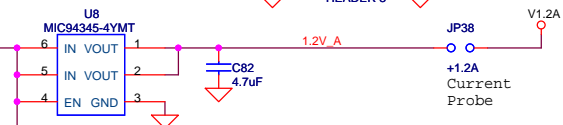
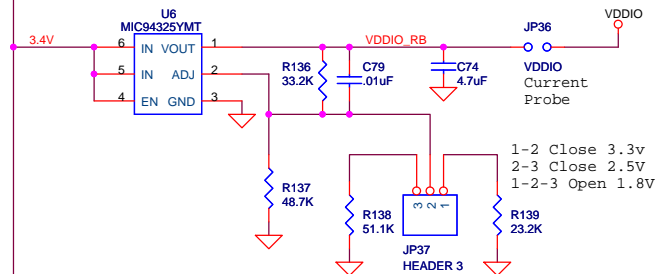
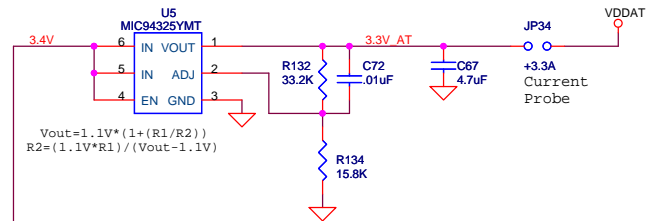
Title KSZ8795 DEMO BOARD		
Size C	Document Number Port 5 to GPHY KSZ9031	Rev 1.0
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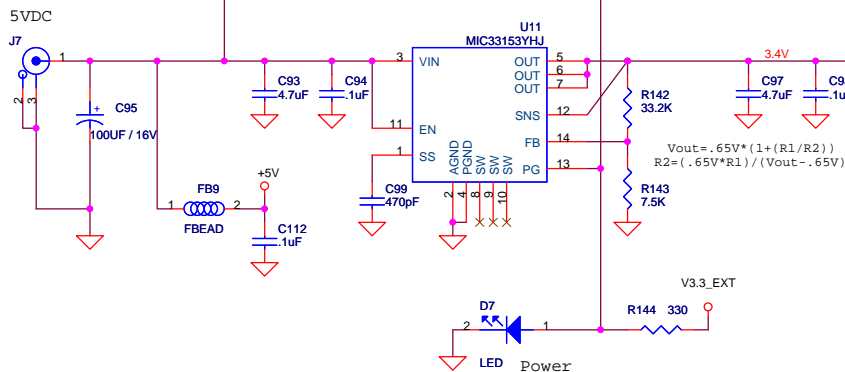
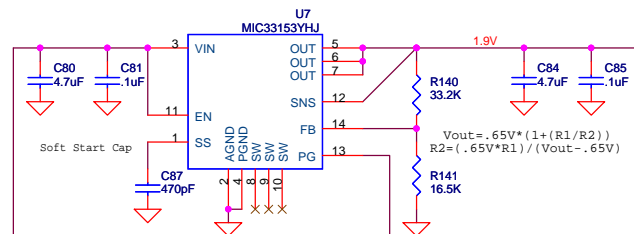
VDDIO



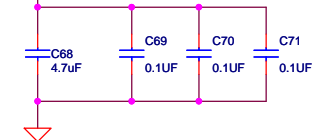
Micrel 500mA LDO with Ripple Blocker,
>50dB PSRR from DC to 100MHz.
Used on this EVB for demonstration purposes.
Not necessary on customer designs if bulk rails are
available. Ripple Blocker can be thought of as a very
good ferrite bead.



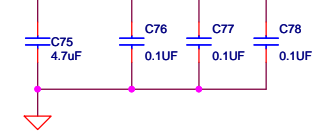
Micrel 4MHz Hyper Light Load
Buck with internal Inductor



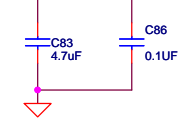
VDDAT Decouple Device Pin 4, 17 and 76
for VDDAT 3.3V analog power



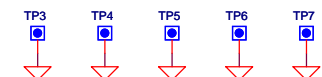
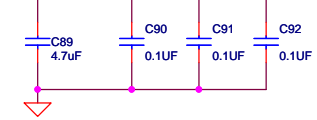
VDDIO Decouple Device Pins 36, 52 and 71
for VDDIO digital power



V1.2A Decouple Device Pin 3
VDD12A for analog 1.2V



V1.2D Decouple Device Pin 28, 46 and 74
for VDD12D for digital 1.2V



Title		
KSZ8795 DEMO BOARD		
Size	Document Number	Rev
	Power, reset, decouple cap and others	1.0
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