SPECIFICATION FOR LCM Module

MODULE No:	KD013QVFMD007
CUSTOMER:	

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Part. No	Part. No KD013QVFMD007		REV	V1.0	Page 1 of 30
	常备库存	长期供	货	支持小量	品种齐全

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Revision History

Date	Rev. No.	Page	Summary
2022.01.15	V1.0	ALL	FIRST ISSUE

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	常备库存	长 期 供	货	支持小量	品 种 齐 全
	Stock For Sale	Long Time s	supply	NO MOQ	In Full Range



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* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorpho us silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Pan el, driver circuit,back-light unit. The resolution of a 1.28 " TFT-LCD contains 240x240 pixels, and can display up to 65K/262K colors.

* Features

General Information	Specification	– Unit	Note
Items	Items Main Panel		Note
Display area(AA)	32.4(H)*32.4(V) (1.28 inch)	mm	
Driver element	TFT active matrix	-	
Display colors	65K/262K	colors	
Number of pixels	240(RGB)*240	dots	
Pixel arrangement	RGB vertical stripe	-	
Pixel pitch	0.135(H)*0.135(V)	mm	
Viewing angle	ALL	o'clock	
Controller IC	GC9A01	-	
	8/9/16/18bit MCU		
LCM Interface	3/4SPI+16/18BIT RGB	-	
	3/4 LINE SERIAL		
Display mode	Transmissive /Normally Black	-	
Operating temperature	-20~+70	°C	
Storage temperature	-30∼+80	$^{\circ}$ C	

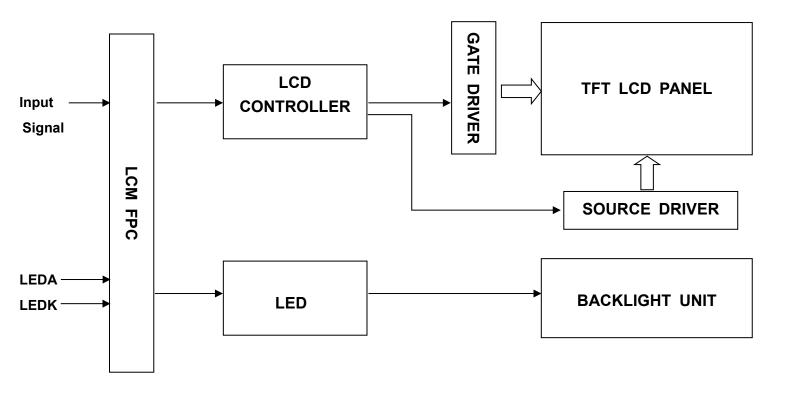
* Mechanical Information

	ltem	Min.	Тур.	Max.	Unit	Note
Madela	Horizontal(H)	-	35.6	-	mm	
Module size	Vertical(V)	-	37.74	-	mm	
Size	Depth(D)	-	1.58	-	mm	
	Weight	-	3	-	g	

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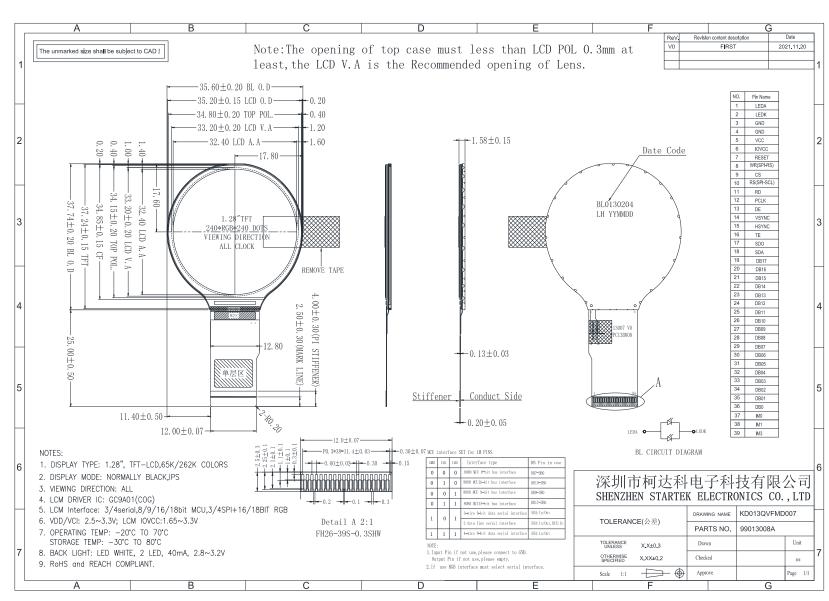
1. Block Diagram



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Outline dimension



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3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	LEDA	Anode pin of backlight	Р
2	LEDK	Cathode pin of backlight	Р
3	GND	Ground.	Р
4	GND	Ground.	Р
5	VCC	Supply voltage (2.5-3.3V).	Р
6	IOVCC	Supply voltage (1.65-3.3V).	Р
7	RESET	This signal will reset the device and must be applied to properly initialize the chip.	I
8	WR(SPI-RS)	-Write enable in MCU parallel interface. - Display data/command selection pin in 4-line serial interface. - Second Data lane in 2 data lane serial interface. -If not used, please fix this pin at IOVCC or GND.	I
9	CS	Chip select input pin ("Low" enable). Fix this pin at IOVCC or GND when not in use.	I
10	RS(SPI-SCL)	-Display data/command selection pin in parallel interfaceThis pin is used to be serial interface clock. DC='1': display data or parameter. DC='0': command dataIf not used, please fix this pin at IOVCC or GND.	I
11	RD	Serves as a read signal and MCU read data at the rising edge. Fix this pin at IOVCC or GND when not in use.	I
12	PCLK	Dot clock signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.	I
13	DE	Data enable signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.	I
14	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.	I
15	HSYNC	Line synchronizing signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.	I
16	TE	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this	I

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		pin is low. If not used, open this pin.	
17	SDO	The data is output on the falling edge of the SCL signal.	0
17	300	If not used, let this pin open.	
18	SDA	The data is latched on the rising edge of the SCL signal.	I/O
10	SDA	If not used, please fix this pin at IOVCC or DGND level	1/0
		18-bit parallel bi-directional data bus for MCU system and RGB	
19-36	DB17-DB0	interface mode .	I/O
		Fix to GND level when not in use	
37	IM0	MPU Parallel interface bus and serial interface select If use RGB	
38	IM1	Interface must select serial interface.	ı
39	IM3	Fix this pin at IOVCC and GND.	

MCU interface SET for IM PINS.

IM3	IM1	IMO	Interface type	DB Pin in use
0	0	0	8080 MCU 8-bit bus interface	DB7-DB0
0	1	0	8080 MCU16-bit bus interface	DB15-DB0
0	0	1	8080 MCU 9-bit bus interface	DB8-DB0
0	1	1	8080 MCU18-bit bus interface	DB17-DB0
1	1 0 1		3-wire 9-bit data serial interface	SDA:In/Out
1			2 data line serial interface	SDA:In/Out,DCX:In
1	1	1	4-wire 8-bit data serial interface	SDA:In/Out

NOTE:

- 1. Input Pin if not use, please connect to GND. Output Pin if not use, please empty.
- 2. If use RGB interface must select serial interface.

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	Stock For Sale	Long Time s	supply	NO MOQ	In Full Range



4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Тур.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0	600	800			(1)(2)
Response time	Rising Falling	$T_{R+}T_{F}$	Normal viewing angle		30	35	msec	(1)(3)
Color Gar	nut	S(%)		40	45		%	*
		Wx		0.2581	0.2981	0.3381		(1)(4)
	White	W _Y		0.2803	0.3203	0.3603		CA-
		R _X		0.5731	0.6131	0.6531		310
Color Filter	Red	R _Y		0.3198	0.3598	0.3998		
Chromacicity		G _X		0.3077	0.3477	0.3877		
	Green	G _Y		0.5325	0.5725	0.6125		
		B _X		0.1083	0.1483	0.1883		
	Blue	B _Y		0.0414	0.0814	0.1214		
		ΘL		80	85			(1)(4)
	Hor.	ΘR		80	85			
Viewing angle	.,	ΘU	CR>10	80	85			
	Ver.	ΘD		80	85			
Option View D	irection			ALL				

^{*}The data comes from the LCD specification.

Measuring Condition

Measuring surrounding : dark room Ambient temperature : 25±2_°C

15min. warm-up time.

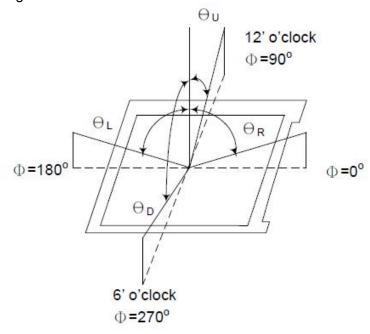
Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

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	常备库存	长期供	货	支持小量	品种齐全
	Stock For Sale	Long Time s	supply	NO MOQ	In Full Range

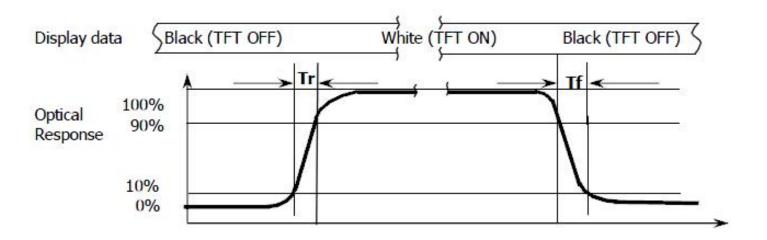


Note (1): Definition of Viewing Angle:



Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

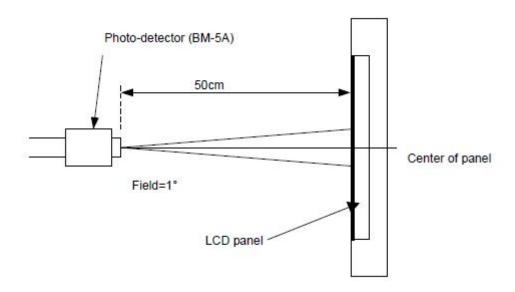
Note (3): Response Time



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Note (4): Definition of optical measurement setup



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	常备库存	长期供	货	支持小量	品 种 齐 全
	Stock For Sale	Long Time s	supply	NO MOQ	In Full Range



5. Electrical Characteristics

5.1 Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VCC/VCI	-0.3	4.6	V	Note1
Digital interface supple Voltage	IOVCC	-0.3	4.6	V	
Operating temperature	T _{OP}	-20	+70	°C	
Storage temperature	T _{ST}	-30	+80	°C	

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Тур.	Max.	Unit	Note
Digital Supply Voltage	VCC/VCI	2.5	2.8	3.3	V	
Digital interface supple Voltage	IOVCC	1.65	2.8	3.3	V	
Normal mode Current consumption	IDD		6	12	mA	
Level input veltere	V _{IH}	0.7*IOVCC		IOVCC	V	
Level input voltage	V _{IL}	GND		0.3*IOVCC	V	
Lovel output valtage	V _{ОН}	0.8*IOVCC		IOVCC	V	
Level output voltage	V _{OL}	GND		0.2*IOVCC	V	

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	常备库存	长期供	货	支持小量	品种齐全
	Stock For Sale	Long Time s	supply	NO MOQ	In Full Range



5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 2 chips LED

constant current driving method is suggested.

Item	Symbol	Min.	Тур.	Max.	Unit	Note
Forward Current	I _F	30	40		mA	
Forward Voltage	V _F	2.8		3.2	V	
LCM Luminance	LV	600	650		cd/m2	Note3
LED life time	Hr	50000			Hour	Note1,2
Uniformity	Avg	80			%	Note3

Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

Ta=25±3 °C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at

Ta=25°C and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The

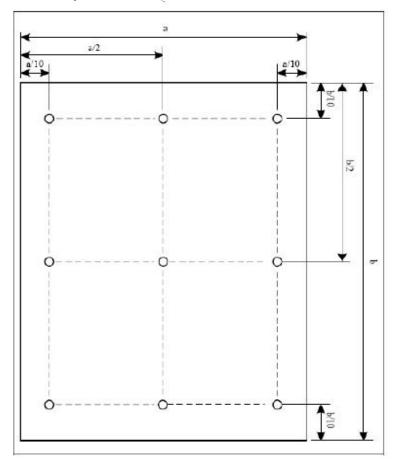
LEDA • LEDK

BL CIRCUIT DIAGRAM

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	常备库存	长 期 供	货	支持小量	品种齐全
	Stock For Sale	Long Time s	supply	NO MOQ	In Full Range



Note (3) Luminance Uniformity of these 9 points is defined as below:



Uniformity = $\frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$

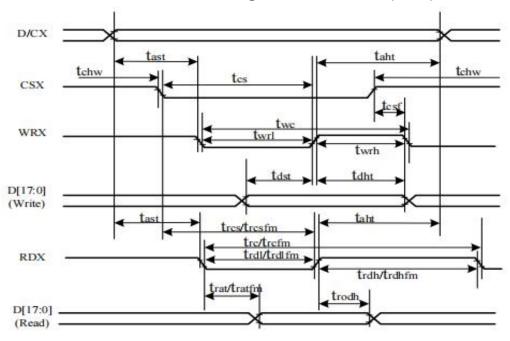
 $Luminance = \frac{Total \ Luminance \ of \ 9 \ points}{9}$

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	常备库存	长 期 供	货	支持小量	品种齐全
	Stock For Sale	Long Time s	vlague	NO MOQ	In Full Range



6. AC Characteristic

6.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080)



Signal	Symbol	Parameter	min	ma x	Uni t	Description
DCV	tast	Address setup time	0	-	ns	
DCX	taht	Address hold time(Write/Read)	0	-	ns	
9	tchw	CSX "H" pulse width	0	0-00	ns	
	tes	Chip Select setup time(Write)	15	140	ns	
CSX	tres	Chip Select setup time(Read ID)	45	121	ns	
	tresfm	Chip Select setup time(Read FM)	355		ns	
	tcsf	Chip Select Wait time (Write/Read)	10	1570	ns	
	twc	Write Cycle	66	-	ns	
WRX	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
DDV/FM	trefm	Read Cycle (FM)	380	1576	ns	
RDX(FM	trdhfm	Read Control H duration(FM)	180	-	ns	
)	trdlfm	Read Control L duration(FM)	200	-	ns	
	trc	Read Cycle (ID)	160	-	ns	
RDX(ID)	trdh	Read Control H pulse duration	90	-	ns	
	trdl	Read Control L pulse duration	70	-	ns	
D[17:0],	tdst	Write data setup time	10	-	ns	For maximum
D[15:0],	tdht	Write data hold time	10	-	ns	CL=30pF

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	常备库存	长 期 供	货	支持小量	品 种 齐 全
	Stock For Sale	Long Time s	supply	NO MOQ	In Full Range

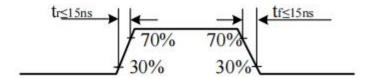
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D[8:0],	trat	Read access time		40	ns	For minimum
D[7:0]	tratfm	Read access time	- -	340	ns	CL=8pF
	trod	Read output disable time	20	80	ns	

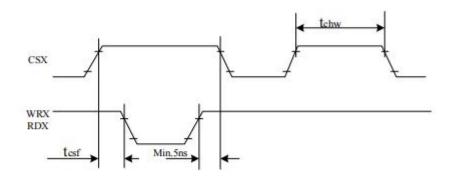
Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

Figure 91.



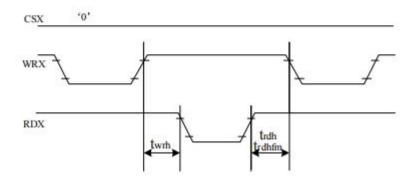
CSX timings:

Figure 92.



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals. Write to read or read to write timings:

Figure 92.



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

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	常备库存	长期供	货	支持小量	品种齐全
	Stock For Sale	Long Time s	supply	NO MOQ	In Full Range



6.2 Display Serial Interface Timing Characteristics (3-line SPI system)

Figure 97.

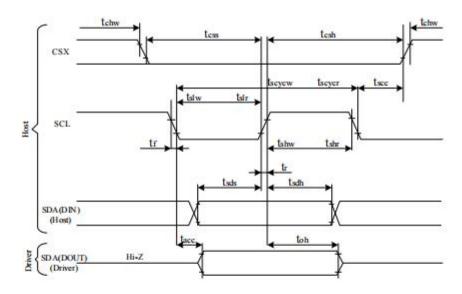
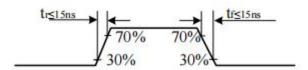


Table47.

Signal	Symbol	Parameter	min	max	Uni t	Description
	tscycw	Serial Clock Cycle (Write)	10		ns	
	tshw	SCL "H" Pulse Width (Write)	5	-	ns	
e.c.i	tslw	SCL "L" Pulse Width (Write)	5	(*)	ns	
SCL	tscycr	Serial Clock Cycle (Read)	150	950	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	140	ns	
SDA/SDI	tsds	Data setup time (Write)	5	3.00	ns	
(Input)	tsdh	Data hold time (Write)	5	950	ns	
SDA/SD0(Outp	tacc	Access time (Read)	10		ns	
	tscc	SCL-CSX	10	950	ns	
CSX	tchw	CSX "H" Pulse Width	10	-	ns	
	tess		20		ns	
	tesh	CSX-SCL Time	40	3.00	ns	

Note: Ta = 25 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, VSSA=VSSC=0V Figure 98.



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	Stock For Sale	Long Time s	supply	NO MOQ	In Full Range



6.3 Display Serial Interface Timing Characteristics (4-line SPI system)

Figure98.

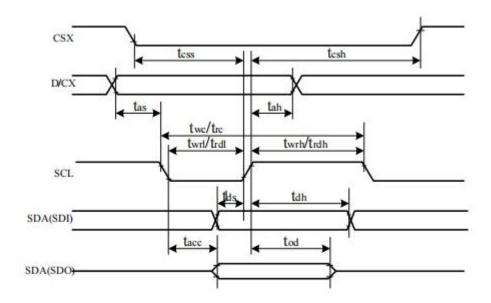
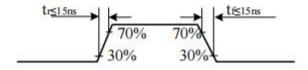


Table48.

Signal	Symbol	Parameter	min	max	Unit	Description
CEV	tess	Chip select time (Write)	20	2	ns	- 1111
CSX	tcsh	Chip select hold time (Read)	40	-	ns	
	twc	Serial Clock Cycle (Write)	10	-	ns	
	twrh	SCL "H" Pulse Width (Write)	5	-	ns	
CCI	twrl	SCL "L" Pulse Width (Write)	5	-	ns	
SCL	tre	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL "H" Pulse Width (Read)	60	-	ns	
	trdl	SCL "L" Pulse Width (Read)	60	-	ns	
DICV	tas	D/CX setup time	10	12	ns	
D/CX	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA/SDI	tds	Data setup time (Write)	5	15	ns	
(Input)	tdh	Data hold time (Write)	5	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	17	ns	

Note: Ta = 25 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V Figure99.



Part. No	KD013QVFI	MD007	REV	V1.0	Page 18 of 30
	常备库存	长期供	货	支持小量	品种齐全
	Stock For Sale	Long Time s	supply	NO MOQ	In Full Range



6.4 Parallel 18/16/6-bit RGB Interface Timing Characteristics Figure 100.

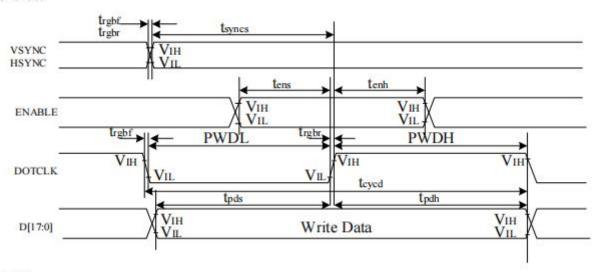


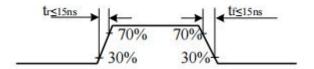
Table49.

Signal	Symbol Parameter		min	ma x	Uni t	Description	
VSYNC/HSYN	tsyncs	VSYNC/HSYNC setup time	15	121	ns	e 10	
C	tsynch	VSYNC/HSYNC hold time	15	(*)	ns]	
DE	tens	DE setup time	15	-	ns	1	
DE	tenh	DE hold time	15	-	ns		
DUTAN	tpos	Data setup time	15	121	ns	18/16-bit bus	
D[17:0]	tpdh	Date hold time	15	(*)	ns	RGB interface	
	PWDH	DOTCLK high-level period	15	-	ns	mode	
	PWDL	DOTCLK low-level period	15	2.1	ns		
DOTCLK	tcycd	DOTCLK cycle time	100	-	ns		
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time		15	ns		
VSYNC/HSYN	tsyncs	VSYNC/HSYNC setup time	15	- 1	ns		
C	tsynch	VSYNC/HSYNC hold time	15	-	ns		
DE	tens	DE setup time	15	-	ns		
DE	tenh	DE hold time	15	-	ns	15 25	
DELEGI	tpos	Data setup time	15	121	ns	Chal DCD	
D[17:0]	tpdh	Date hold time	15	-	ns	6-bit bus RGB	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	interface mode	
	PWDL	DOTCLK low-level pulse period	15	121	ns		
	tcycd	DOTCLK cycle time	100	(+)	ns	1	
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns		

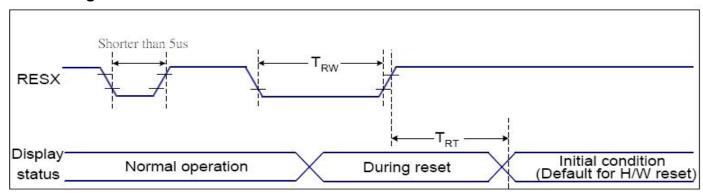
Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

Part. No	KD013QVFMD007		REV	V1.0	Page 19 of 30
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6.4 Reset Timing Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
2	TRW	Reset pulse duration	10	-	us
RESX	TRT	Docat agned	(27)	5 (Note 1, 5)	ms
	IKI	Reset cancel		120 (Note 1, 6, 7)	ms

Notes:

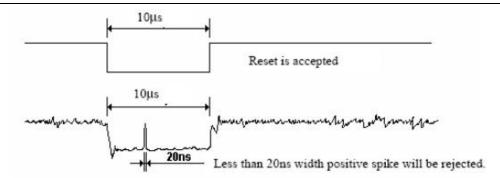
- The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
 - 2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

- 3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.
 - 4. Spike Rejection also applies during a valid reset pulse as shown below:

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	Stock For Sale	Long Time s	supply	NO MOQ	In Full Range





- 5. When Reset applied during Sleep In Mode.
- 6. When Reset applied during Sleep Out Mode.
- It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for
 120msec.

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7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

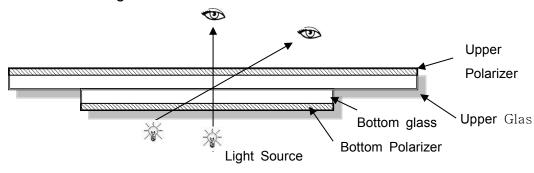
Temperature : 25±5°C

Humidity: 65%±10%RH

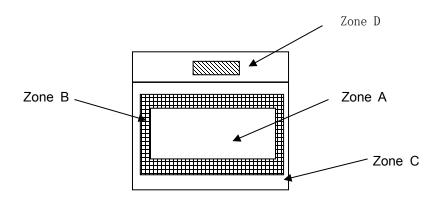
Viewing Angle: Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



7.1.2 Definition



Zone A: Effective Viewing Area(Character or Digit can be seen)

Zone B: Viewing Area except Zone A

Zone C: Outside (Zone A+Zone B) which can not be seen after assembly by customer

Zone D: IC Bonding Area

Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

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7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class $\, {\rm II} \,$ AQL:

Major defect	Minor defect		
0.65	1.5		

LCD: Liquid Crystal Display , LCM: Liquid Crystal Module,

No	Items to be inspected	Criteria	Classification of defect s
1	Functional defects	 No display, Open or miss line Display abnormally, Short Backlight no lighting, abnormal lighting. etc 	Major
2	Missing Components and etc		aje:
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed, deformation and etc	
4	Color tone	Color unevenness, refer to limited sample	
5	Spot/Line defect	Light dot,Dim spot,(Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	Minor
6	Soldering appearance	Good soldering, Peeling off is not allowed and etc.	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

Note1: a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

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7.1.4 Criteria (Visual)

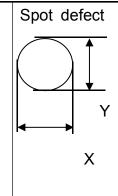
Number	Items	Criteria(mm)				
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height	(1) The edge of LCD broken					
L: Length of IT O,		X Y Z				
T: Height of LCD		≤3.0mm				
	(2)LCD corner broken	X Y Z ≤3.0mm ≤L ≤T				
	(3) LCD crack	Crack Not allowed				

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2.0

SHENZHEN STARTEK ELECTRONIC TECHNOLOGY CO., LTD



j light dot (black/white spot , pinhole, stain, etc.)					
Zone	ole Qty				
Size (mm)	А	В	С		
Ф≤0.15	Φ≤0.15 Ignore				
0.15<Φ≤0.25	3(distance ≥ 6mm)	Ignore			
0.25<Φ≤0.4	2(distance ≥ 6mm)	igi	iore		
Ф>0.4 0					
② Dim spot (light leakage、dent、dark spot, etc)					

Φ=(X+Y)/2

E Biiii opot (iigiit	loanagor doner dant op	01, 010,	
Zone	Acceptat	ole Qty	
Size (mm)	Α	В	С
⊅<0.15	lanoro		

Φ≤0.15 Ignore 0.15<Φ≤0.25 3(distance ≥ 6mm) 0.25<Φ≤0.4 2(distance ≥ 6mm) Φ>0.4 0

3 Polarizer accidented spot

A		
Α	С	
Igno		
2(distance ≥ 6mm)		Ignore
0		
	A Igno	Acceptable Qty A B Ignore 2(distance ≥ 6mm) 0

4 Polarizer Bubble

Zone	Acceptable Qty			
Size (mm)	АВ		С	
Ф≤0.2	Ignore			
0.2<Φ≤0.4	3(distance≧6mm)		Ignore	
Ф>0.4	0		_	

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	常备库存	长期供	货	支持小量	品种齐全

Stock For Sale Long

Long Time supply

支持小量 NO MOQ 品种齐全 In Full Range

Ignore



SHENZHEN SIA	KIEK EL	ECTRONIC TECHNOLOG	GY CO., LI	
3.0 LCD Pixel defect	Pixel bad po	ints		
	Item	Zone A	Acceptable Qt	
		Random	N≤2	
	Bright dot	2 dots adjacent	N≤0	
		3 dots adjacent	N≤0	
		Random	N≤2	
	Dark dot	2 dots adjacent	N≤0	
		3 dots adjacent	N≤0	
	Distance	 Minimum Distance Between Bright dots. Minimum Distance Between dark dots Minimum Distance Between dark and bright dot. 	5mm	
	Total bright	N≤4		
	Note:	1		
	 A) Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern. B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture. C) 2 dot adjacent = 1 pair = 2 dots Picture: 			
	2 dot adj	acent 2 dot adjacer	nt	
	2 dot adjace	nt (vertical) 2 dot adjacer	nt (slant)	

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	Line defect (LCD					
	/Polarizer backlight bla	Width(mm)	Length(m	Acce	ptable Q	ety
	ck/white line, scratch,	vvidtri(i1ii11)	m)	Α	В	С
4.0	stain)	Ф≤0.03	Ignore	Ignore	!	
4.0		0.03 <w≤0.04< td=""><td>L≤3.0</td><td>N≤2</td><td></td><td>Ignore</td></w≤0.04<>	L≤3.0	N≤2		Ignore
	W: width, L: length	0.04 <w≤0.05< td=""><td>L≤2.0</td><td>N≤1</td><td></td><td></td></w≤0.05<>	L≤2.0	N≤1		
	N : Count	W>0.05		Define as spo	t defect	
	Electronic Componen	, ,				
5.0	ts SMT.	smatch, The positive and negative polarity opposite				
6.0	Display color& Brigh	Color: Measuring the color coordinates, The measurement standard according to the datasheet or samples.				
	tness.	2. Brightness: Measuring the brightness of White screen, The meas urement standard according to the datasheet or Samples.				
7.0	LCD Mura/Waving/	Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.				
	Hot spot					

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed

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	Stock For Sale	Long Time s	supply	NO MOQ	In Full Range



8. Reliability Test Result

ltem	Condition	Inspection after test
High Temperature Operating	70°C,96H	
Low Temperature Operating	-20°C, 96HRS	
High Temperature Storage	80°C, 96HR	
Low Temperature Storage	-30°C, 96HR	Inspection after 2~4hours storage at room temperature,
High Temperature & High		the sample shall be free from
Humidity Operating		defects:
-10°C 30 min ← +60°C 30 min		1.Air bubble in the LCD;
, ,	Change time:5min 20CYC.	2.Non-display;
	C=150pF, R=330,5points/panel	3.Missing segments/line;
ESD test	Air:±8KV, 5times; Contact:±6KV, 5 times;	4.Glass crack;
	(Environment: 15°C~35°C, 30%~60%).	5.Current IDD is twice higher
	Frequency range:10~55Hz, Stroke:1.5mm	than initial value.
Vibration (Non-operation)	Sweep:10Hz~55Hz~10Hz 2 hours for each direction of	
	X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm(MEDIUM BOX)	

Remark:

- 1. The test samples should be applied to only one test item.
- 2. Sample size for each test item is 5~10pcs.
- 3. For Damp Proof Test, Pure water(Resistance $> 10M\Omega$) should be used.
- 4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
- 6. The color fading mura of polarizing filter should not care.

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9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.
- Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.
- If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
- Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.

9.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.
- It is highly recommended to store the module with temperature from 0 to 35 $\,^\circ\mathbb{C}\,$ and relative humidity of less than 70%
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
- In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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	Stock For Sale	Long Time s	supply	NO MOQ	In Full Range



10. Packing

----TBD-----

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	常备库存	长期供	货	支持小量	品 种 齐 全

Stock For Sale

Long Time supply NO MOQ

In Full Range