SN74AUP1G14 Low-Power Single Schmitt-Trigger Inverter

1 Features

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Low Static-Power Consumption (I_{CC} = 0.9 µA Maximum)
- Low Dynamic-Power Consumption (C_{pd} = 4.4 pF Typical at 3.3 V)
- Low Input Capacitance (C_I = 1.5 pF Typical)
- Low Noise – Overshoot and Undershoot <10% of V_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Includes Schmitt-Trigger Inputs
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- t_{pd} = 4.9 ns Maximum at 3.3 V

2 Applications

- AV Receivers
- Smartphones
- Blu-ray Players and Home Theaters
- DVD Recorders and Players
- Desktop or Notebook PCs
- Embedded PCs
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Portable Media Players
- Smoke Detectors
- Solid State Drive (SSD): Enterprise
- High-Definition (HDTV)
- Tablets: Enterprise
- Audio Docks: Portable
- DVR and DVS

3 Description

The AUP family is TI's premier solution to the industry's low power needs in battery-powered portable applications. This family assures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see *AUP – The Lowest-Power Family* and *Excellent Signal Integrity*).

This device functions as an independent gate with Schmitt-trigger inputs, which allows for slow input transition and better switching-noise immunity at the input.

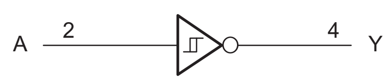
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

Device Information(1)

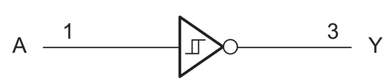
PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AUP1G14DBV	SOT-23 (5)	2.90 mm x 1.60 mm
SN74AUP1G14DCK	SC70 (5)	2.00 mm x 1.25 mm
SN74AUP1G14DRL	SOT (5)	1.60 mm x 1.20 mm
SN74AUP1G14DRY	SON (6)	1.45 mm x 1.00 mm
SN74AUP1G14DSF	SON (6)	1.00 mm x 1.00 mm
SN74AUP1G14DPW	X2SON (5)	0.80 mm x 0.80 mm
SN74AUP1G14YFP	DSBGA (4)	0.76 mm x 0.76 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic) (DBV, DCK, DRL, DRY, DSF, DPW, and YZP Packages)



Logic Diagram (Positive Logic) (YFP Package)



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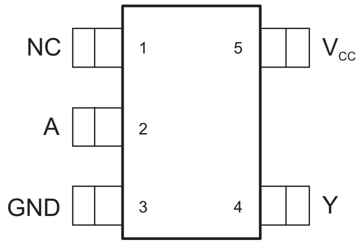
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

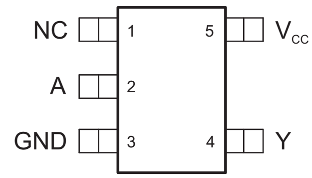
Changes from Revision I (May 2010) to Revision J	**Page**
• Added DPW (X2SON) package	1
• Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Deleted *Ordering Information* table, see *Mechanical, Packaging, and Orderable Information* section at the end of the data sheet	1
• Changed formatting of YFP package pinout drawing	3
• Deleted YZP package from data sheet	3
• Added Junction temperature, T_J in *Absolute Maximum Ratings*	4

5 Pin Configuration and Functions

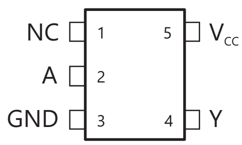
DBV Package
5-Pin SOT-23
Top View



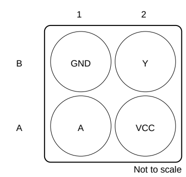
DCK Package
5-Pin SC70
Top View



DRL Package
5-Pin SOT
Top View



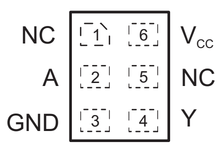
YFP Package
4-Pin DSBGA
Bottom View



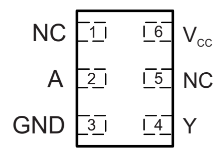
N.C. – No internal connection.

See mechancial drawings for dimensions.

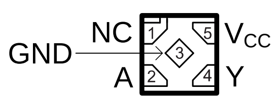
DRY Package
6-Pin SON
Top View



DSF Package
6-Pin SON
Top View



DPW Package
5-Pin X2SON
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	DBV, DCK, DRL, DPW	DRY, DSF	YFP		
A	2	2	A1	I	Logic Input
GND	3	3	B1	—	Ground
N.C.	1	1, 5	—	—	No internal connection
V_{CC}	5	6	A2	—	Positive Supply
Y	4	4	B2	O	Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4.6	V
V_I	Input voltage[2]		–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		–0.5	4.6	V
V_O	Voltage range applied to any output in the high or low state[2]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 0.8 V		–20	µA
		V_{CC} = 1.1 V		–1.1	mA
		V_{CC} = 1.4 V		–1.7	
		V_{CC} = 1.65 V		–1.9	
		V_{CC} = 2.3 V		–3.1	
		V_{CC} = 3 V		–4	
I_{OL}	Low-level output current	V_{CC} = 0.8 V		20	µA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to assure proper device operation. See *Implications of Slow or Floating CMOS Inputs*.

6.4 Thermal Information

THERMAL METRIC (1)		SN74AUP1G14							UNIT
		DRY (SON)	DSF (SON)	YFP (DSBGA)	DPW (X2SON)	DBV (SOT-23)	DCK (SC70)	DRL (SOT)	
		6 PINS	6 PINS	4 PINS	5 PINS	5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	347.8	386.2	179.3	489.2	289.1	325.1	324.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	237.7	192.9	2.8	226.3	213.7	229.1	156.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	210.6	242.2	58.3	352.9	123.0	123.2	172.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	64.4	28.9	1.1	38.2	104.5	96.3	21.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	210.6	241.9	58.6	352.1	122.3	122.4	173.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	150.8	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive-going input threshold voltage	T_A = 25°C	0.8 V	0.3		0.6	V
		T_A = –40°C to +85°C					
		T_A = 25°C	1.1 V	0.53		0.9	
		T_A = –40°C to +85°C					
		T_A = 25°C	1.4 V	0.74		1.11	
		T_A = –40°C to +85°C					
		T_A = 25°C	1.65 V	0.91		1.29	
		T_A = –40°C to +85°C					
		T_A = 25°C	2.3 V	1.37		1.77	
		T_A = –40°C to +85°C					
		T_A = 25°C	3 V	1.88		2.29	
		T_A = –40°C to +85°C					
V_{T-}	Negative-going input threshold voltage	T_A = 25°C	0.8 V	0.1		0.6	V
		T_A = –40°C to +85°C					
		T_A = 25°C	1.1 V	0.26		0.65	
		T_A = –40°C to +85°C					
		T_A = 25°C	1.4 V	0.39		0.75	
		T_A = –40°C to +85°C					
		T_A = 25°C	1.65 V	0.47		0.84	
		T_A = –40°C to +85°C					
		T_A = 25°C	2.3 V	0.69		1.04	
		T_A = –40°C to +85°C					
		T_A = 25°C	3 V	0.88		1.24	
		T_A = –40°C to +85°C					

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	T_A = 25°C		0.8 V	0.07		0.5	V
		T_A = –40°C to +85°C						
		T_A = 25°C		1.1 V	0.08		0.46	
		T_A = –40°C to +85°C						
		T_A = 25°C		1.4 V	0.18		0.56	
		T_A = –40°C to +85°C						
		T_A = 25°C		1.65 V	0.27		0.66	
		T_A = –40°C to +85°C						
		T_A = 25°C		2.3 V	0.53		0.92	
		T_A = –40°C to +85°C						
		T_A = 25°C		3 V	0.79		1.31	
		T_A = –40°C to +85°C						
V_{OH}		I_{OH} = –20 µA	T_A = 25°C	0.8 V to 3.6 V	V_{CC} – 0.1			V
			T_A = –40°C to +85°C					
		I_{OH} = –1.1 mA	T_A = 25°C	1.1 V	0.75 × V_{CC}			
			T_A = –40°C to +85°C		0.7 × V_{CC}			
		I_{OH} = –1.7 mA	T_A = 25°C	1.4 V	1.11			
			T_A = –40°C to +85°C		1.03			
		I_{OH} = –1.9 mA	T_A = 25°C	1.65 V	1.32			
			T_A = –40°C to +85°C		1.3			
		I_{OH} = –2.3 mA	T_A = 25°C	2.3 V	2.05			
			T_A = –40°C to +85°C		1.97			
		I_{OH} = –3.1 mA	T_A = 25°C		1.9			
			T_A = –40°C to +85°C		1.85			
		I_{OH} = –2.7 mA	T_A = 25°C	3 V	2.72			
			T_A = –40°C to +85°C		2.67			
		I_{OH} = –4 mA	T_A = 25°C		2.6			
			T_A = –40°C to +85°C		2.55			
V_{OL}		I_{OL} = 20 µA	T_A = 25°C	0.8 V to 3.6 V			0.1	V
			T_A = –40°C to +85°C					
		I_{OL} = 1.1 mA	T_A = 25°C	1.1 V			0.3 × V_{CC}	
			T_A = –40°C to +85°C					
		I_{OL} = 1.7 mA	T_A = 25°C	1.4 V			0.31	
			T_A = –40°C to +85°C				0.37	
		I_{OL} = 1.9 mA	T_A = 25°C	1.65 V			0.31	
			T_A = –40°C to +85°C				0.35	
		I_{OL} = 2.3 mA	T_A = 25°C	2.3 V			0.31	
			T_A = –40°C to +85°C				0.33	
		I_{OL} = 3.1 mA	T_A = 25°C				0.44	
			T_A = –40°C to +85°C				0.45	
		I_{OL} = 2.7 mA	T_A = 25°C	3 V			0.31	
			T_A = –40°C to +85°C				0.33	
		I_{OL} = 4 mA	T_A = 25°C				0.44	
			T_A = –40°C to +85°C				0.45	
I_I	A input	V_I = GND to 3.6 V	T_A = 25°C	0 V to 3.6 V			0.1	µA
			T_A = –40°C to +85°C				0.5	
I_{OFF}		V_I or V_O = 0 V to 3.6 V	T_A = 25°C	0 V			0.2	µA
			T_A = –40°C to +85°C				0.6	
ΔI_{OFF}		V_I or V_O = 0 V to 3.6 V	T_A = 25°C	0 V to 0.2 V			0.2	
			T_A = –40°C to +85°C				0.6	

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
I_{CC}	V_I = GND or (V_{CC} to 3.6 V) I_O = 0	T_A = 25°C	0.8 V to 3.6 V			0.5	µA
		T_A = –40°C to +85°C				0.9	
ΔI_{CC}	V_I = V_{CC} – 0.6 V I_O = 0	T_A = 25°C	3.3 V			40	µA
		T_A = –40°C to +85°C				50	
C_I	V_I = V_{CC} or GND	T_A = –40°C to +85°C	0 V		1.5		pF
		T_A = –40°C to +85°C	3.6 V				
C_O	V_O = GND	T_A = –40°C to +85°C	0 V		2.5		pF

6.6 Switching Characteristics: C_L = 5 pF

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 2 and Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	A	Y	V_{CC} = 0.8 V	T_A = 25°C		16.3		ns
			V_{CC} = 1.2 V ± 0.1 V	T_A = 25°C	4.2	6.9	11.7	
				T_A = –40°C to +85°C	0.9		15	
			V_{CC} = 1.5 V ± 0.1 V	T_A = 25°C	3.7	5.2	8.4	
				T_A = –40°C to +85°C	1.7		10.7	
			V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	3.3	4.4	6.9	
				T_A = –40°C to +85°C	1.9		8.5	
			V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	2.8	3.5	4.8	
				T_A = –40°C to +85°C	1.8		6.1	
			V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	2.5	3	4	
				T_A = –40°C to +85°C	1.7		4.9	

6.7 Switching Characteristics: C_L = 10 pF

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 2 and Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	A	Y	V_{CC} = 0.8 V	T_A = 25°C		18.4		ns
			V_{CC} = 1.2 V ± 0.1 V	T_A = 25°C	4.6	7.9	13.4	
				T_A = –40°C to +85°C	1.3		16.7	
			V_{CC} = 1.5 V ± 0.1 V	T_A = 25°C	4	6	9.6	
				T_A = –40°C to +85°C	2.2		11.8	
			V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	3.6	5	7.9	
				T_A = –40°C to +85°C	2.4		9.5	
			V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	3.2	4	5.5	
				T_A = –40°C to +85°C	2.3		6.8	
			V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	2.9	3.5	4.6	
				T_A = –40°C to +85°C	2.1		5.6	

6.8 Switching Characteristics: C_L = 15 pF

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 2 and Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	A	Y	V_{CC} = 0.8 V	T_A = 25°C		20.1		ns
			V_{CC} = 1.2 V ± 0.1 V	T_A = 25°C	5.5	8.7	14	
				T_A = –40°C to +85°C	2.5		17.3	
			V_{CC} = 1.5 V ± 0.1 V	T_A = 25°C	4.7	6.7	10	
				T_A = –40°C to +85°C	3		12.5	
			V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	4.2	5.6	8.3	
				T_A = –40°C to +85°C	3		10.1	
			V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	3.6	4.5	5.9	
				T_A = –40°C to +85°C	2.7		7.4	
			V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	3.3	3.9	5	
				T_A = –40°C to +85°C	2.5		6.1	

6.9 Switching Characteristics: C_L = 30 pF

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 2 and Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	A	Y	V_{CC} = 0.8 V	T_A = 25°C		25.7		ns
			V_{CC} = 1.2 V ± 0.1 V	T_A = 25°C	7.4	11.2	17.1	
				T_A = –40°C to +85°C	4.5		20.5	
			V_{CC} = 1.5 V ± 0.1 V	T_A = 25°C	6.1	8.5	12.3	
				T_A = –40°C to +85°C	4.6		14.7	
			V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	5.4	7.2	10.3	
				T_A = –40°C to +85°C	4.1		12	
			V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	4.7	5.7	7.4	
				T_A = –40°C to +85°C	3.7		8.8	
			V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	4.2	5	6.2	
				T_A = –40°C to +85°C	3.5		7.3	

6.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	0.8 V	4	pF
			1.2 V ± 0.1 V	4	
			1.5 V ± 0.1 V	4.1	
			1.8 V ± 0.15 V	4.1	
			2.5 V ± 0.2 V	4.3	
			3.3 V ± 0.3 V	4.4	

6.11 Typical Characteristics

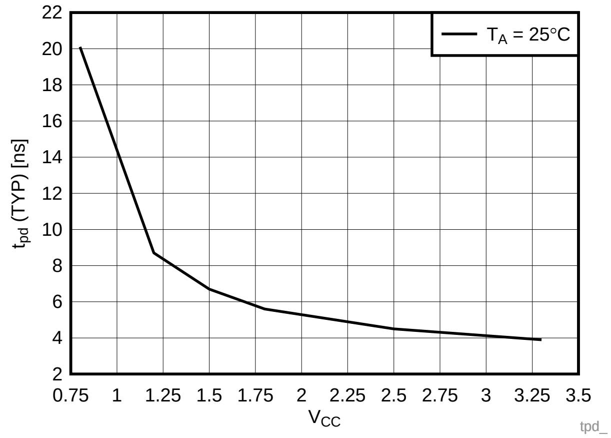
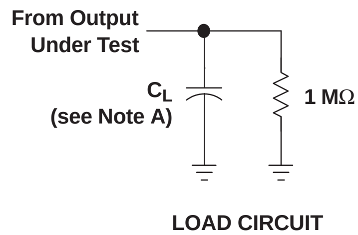


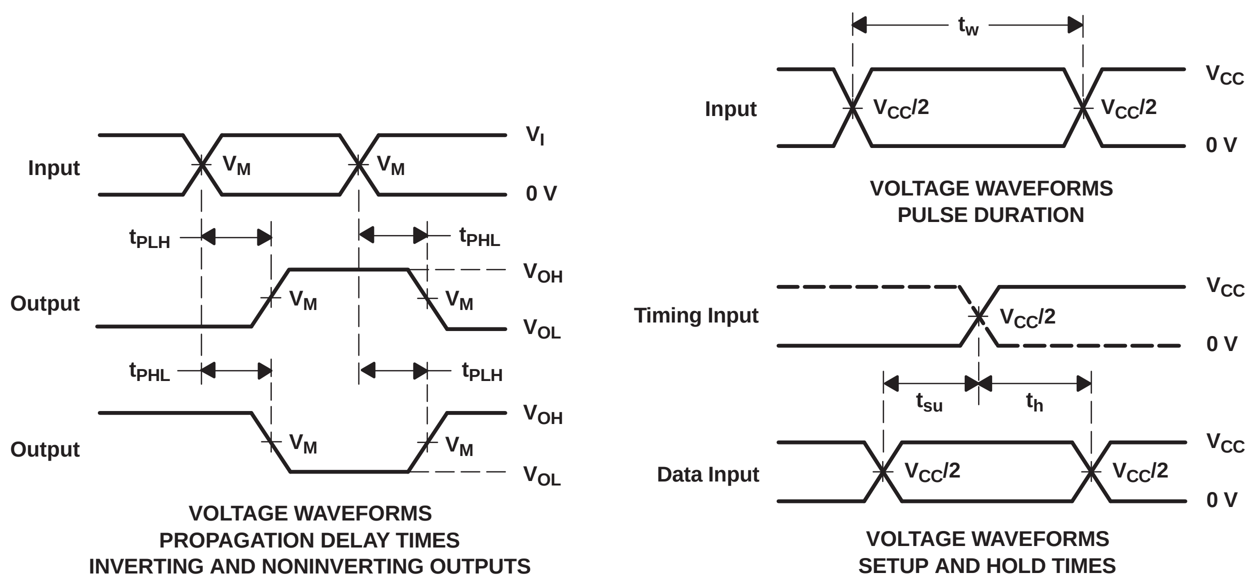
Figure 1. Typical Propagation Delay vs. Supply Voltage (C_L = 15 pF

7 Parameter Measurement Information

7.1 (Propagation Delays, Setup and Hold Times, and Pulse Width)



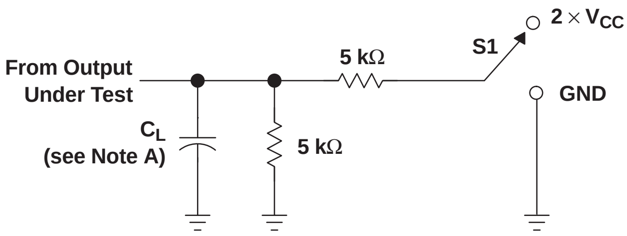
	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit And Voltage Waveforms

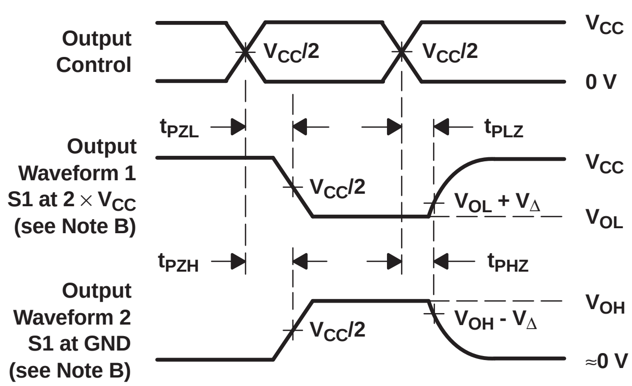
7.2 (Enable and Disable Times)



LOAD CIRCUIT

TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit And Voltage Waveforms

8 Detailed Description

8.1 Overview

This device functions as an independent gate with Schmitt-trigger inputs, which allows for slow input transition and better switching-noise immunity at the input.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

8.2 Functional Block Diagrams

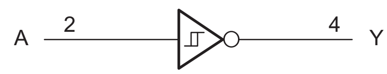


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**Figure 4. Logic Diagram (Positive Logic)
(DBV, DCK, DRL, DRY, DSF, DPW, and YZP Packages)**

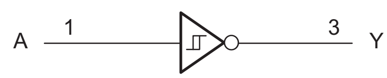

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**Figure 5. Logic Diagram (Positive Logic)
(YFP Package)**

8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* table must be followed at all times.

8.3.2 Schmitt-Trigger Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using ohm's law ($R = V \div I$).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, see *Understanding Schmitt Triggers*.

Feature Description (continued)

8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

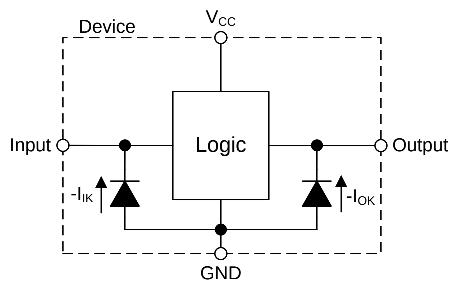


Figure 6. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics* table.

8.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Absolute Maximum Ratings* table.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74AUP1G14.

Table 1. Function Table

INPUT A	OUTPUT Y
H	L
L	H

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Mechanical input elements, such as push buttons or rotary knobs, offer simple ways to interact with electronic systems. Typically, these elements have recoil or bouncing, where the mechanical element makes and breaks contact multiple times during human interaction. This bouncing can cause one or more repeated signals to be passed, triggering multiple actions when only a single input was intended. One potential solution to mitigating these multiple inputs is by utilizing a Schmitt-trigger to create a debounce circuit. Figure 7 shows an example of this solution.

9.2 Typical Application

The input due to the push button switches multiple times, causing the output of a non Schmitt-trigger device to trigger multiple times, while the Schmitt-trigger input device with RC delay limits the output pulse to a single pulse desired by the user. The separated positive and negative input voltage threshold values prevent multiple triggers from occurring, see the *Electrical Characteristics* table for V_{T+}, V_{T-}, and V_{hys} values.

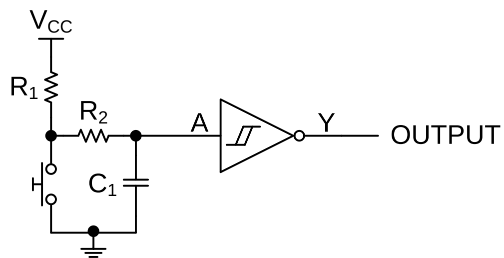


Figure 7. Push Button Debounce Circuit Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The drive strength also creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   – For specified high and low levels, see (V_{T+} and V_{T-}) in the *Electrical Characteristics* table.
   – Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the *Recommended Operating Conditions* table at any valid V_{CC}.
2. Recommended Output Conditions:
   – Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.

Typical Application (continued)

9.2.3 Application Curves

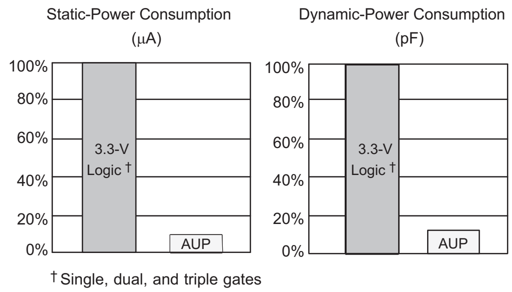


Figure 8. AUP – The Lowest-Power Family

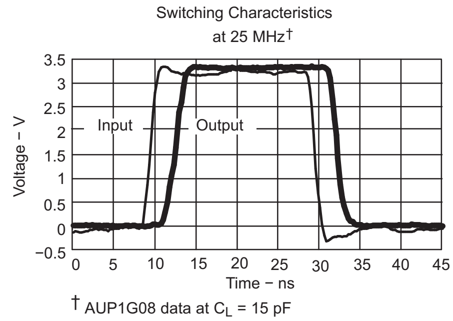


Figure 9. Excellent Signal Integrity

10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

Even low data rate digital signals can contain high-frequency signal components due to fast edge rates. When a printed-circuit board (PCB) trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 10 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

An example layout is given in Figure 11 for the DPW (X2SON-5) package. This example layout includes a 0402 (metric) capacitor and uses the measurements found in the example board layout appended to this end of this datasheet. A via of diameter 0.1 mm (3.973 mil) is placed directly in the center of the device. This via can be used to trace out the center pin connection through another board layer, or it can be left out of the layout

11.2 Layout Example

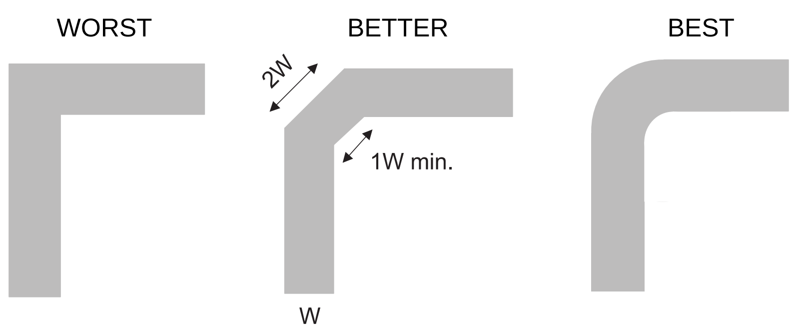


Figure 10. Trace Example

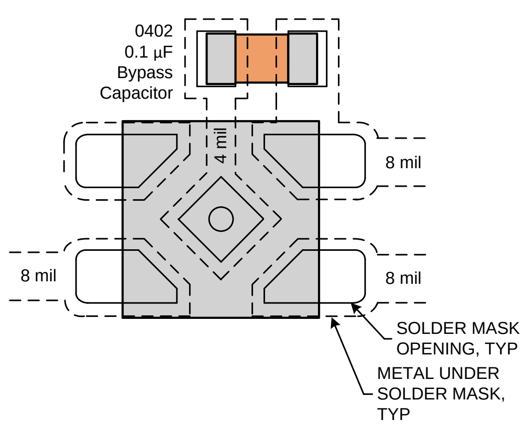


Figure 11. Example Layout With DPW (X2SON-5) Package

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1G14DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H14R	Samples
SN74AUP1G14DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H14R	Samples
SN74AUP1G14DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HF5, HFF, HFK, HF R)	Samples
SN74AUP1G14DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HF5, HFF, HFK, HF R)	Samples
SN74AUP1G14DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HF5, HFK, HFR)	Samples
SN74AUP1G14DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BZ	Samples
SN74AUP1G14DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(HF7, HFR)	Samples
SN74AUP1G14DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HF	Samples
SN74AUP1G14DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HF	Samples
SN74AUP1G14YFPR	ACTIVE	DSBGA	YFP	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		HF N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

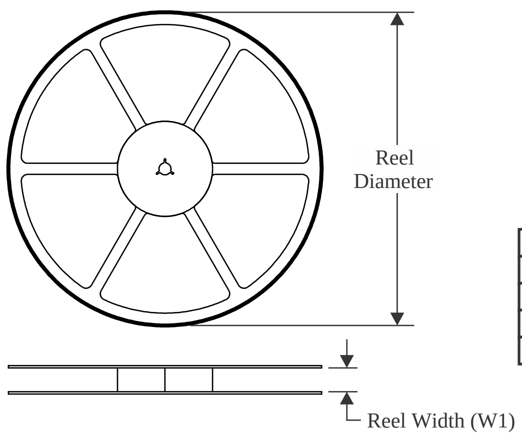
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

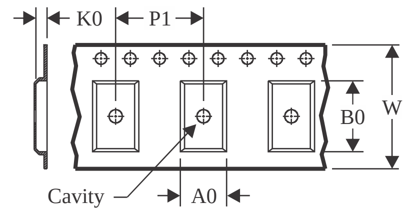
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

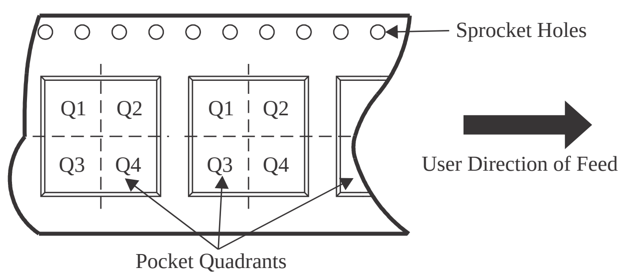


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

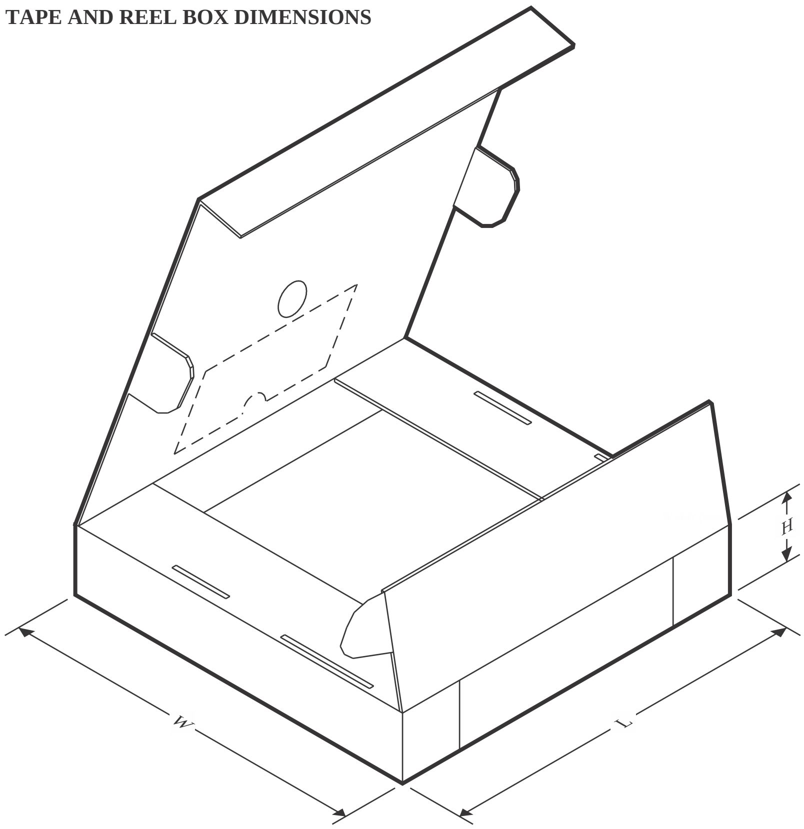
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

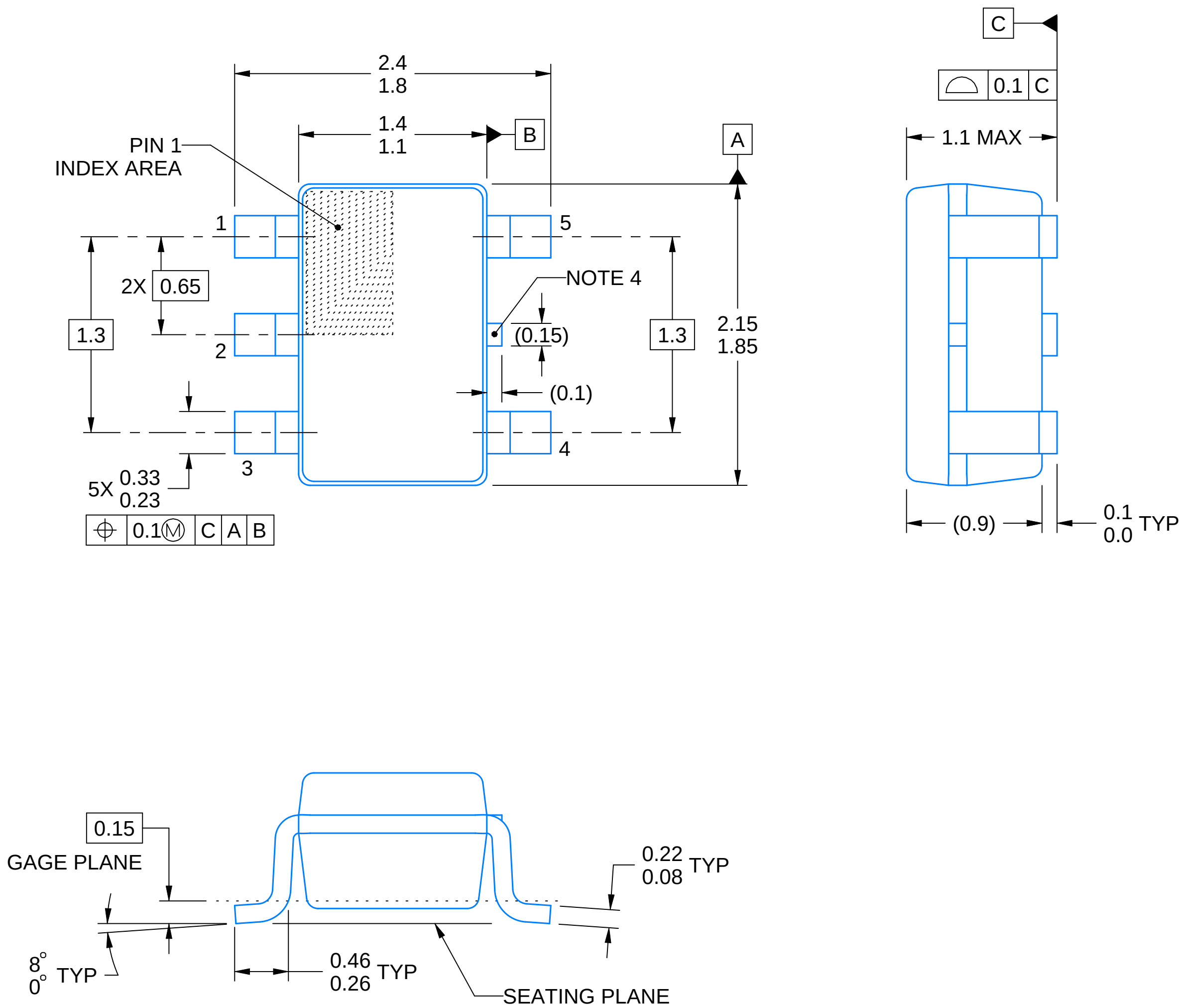
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G14DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G14DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G14DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G14DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G14DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G14DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74AUP1G14DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G14DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G14DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G14YFPR	DSBGA	YFP	4	3000	178.0	9.2	0.89	0.89	0.58	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

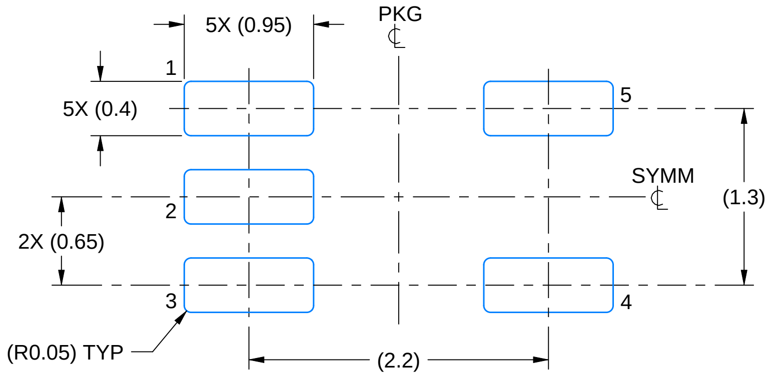
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G14DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G14DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G14DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G14DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74AUP1G14DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G14DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74AUP1G14DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G14DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G14DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP1G14YFPR	DSBGA	YFP	4	3000	220.0	220.0	35.0



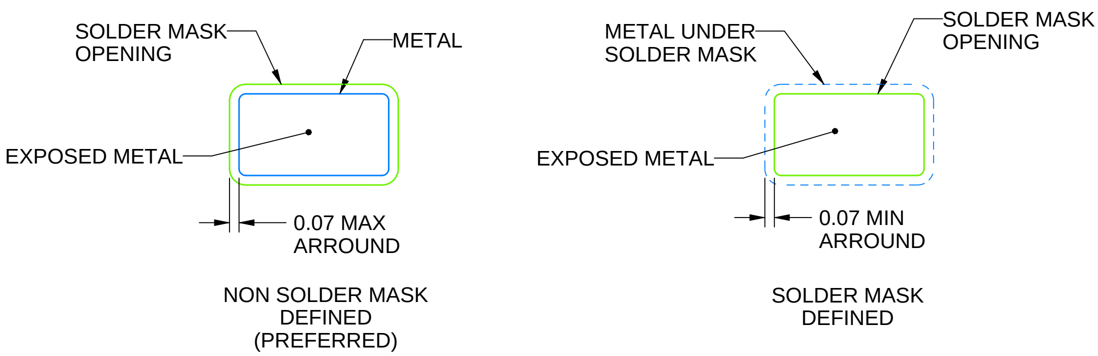
4214834/C 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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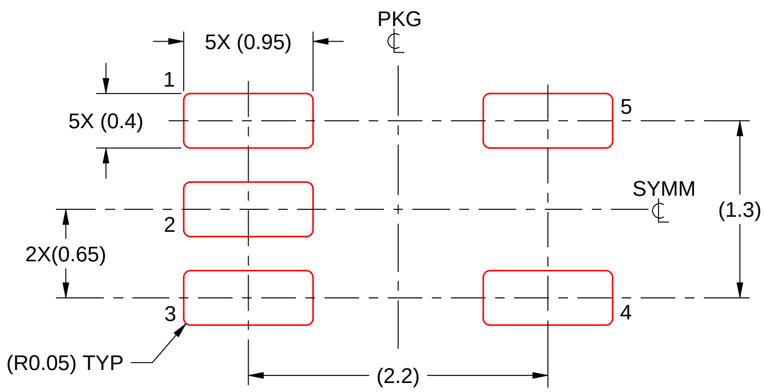
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



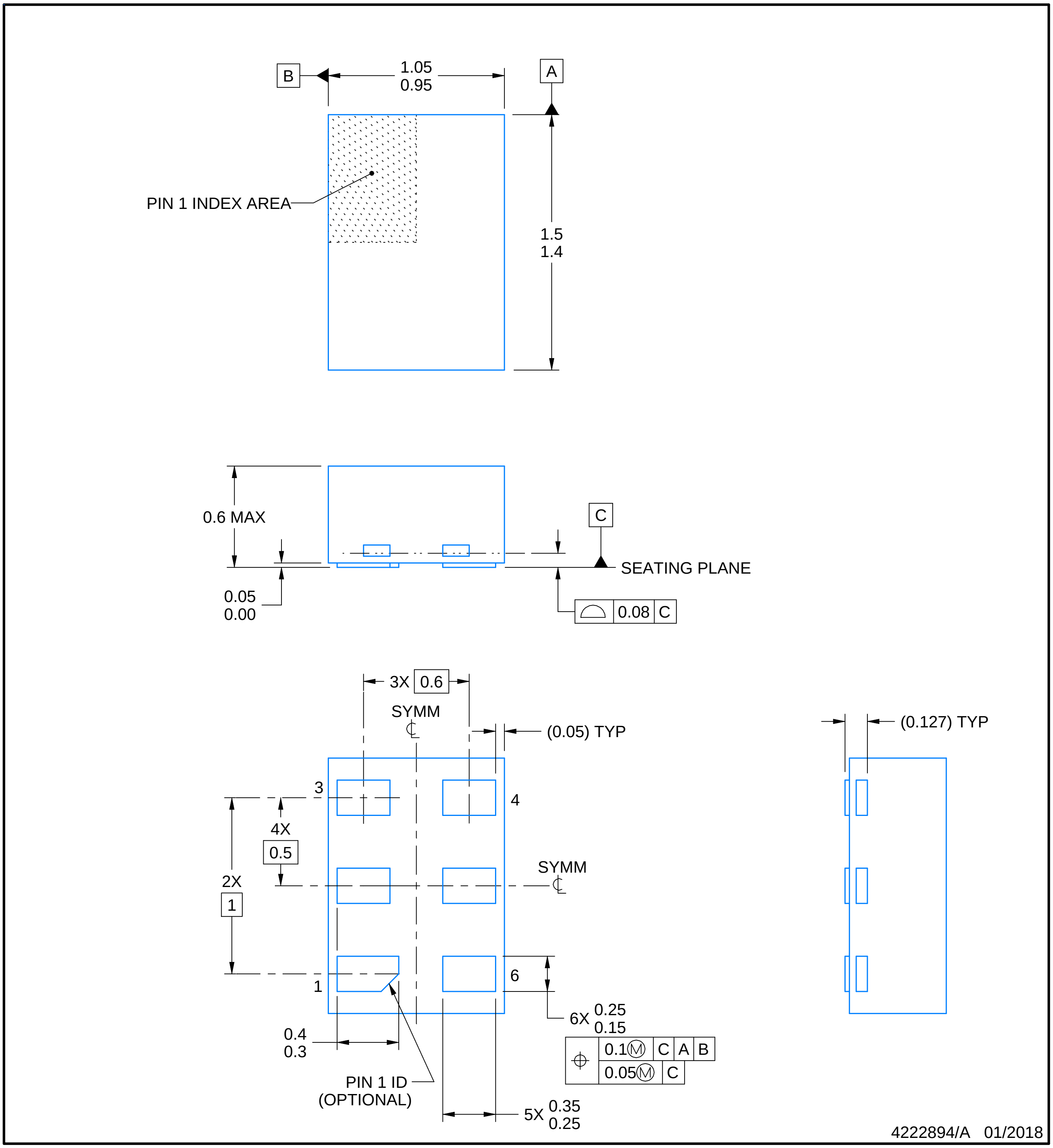
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/C 03/2023

NOTES: (continued)

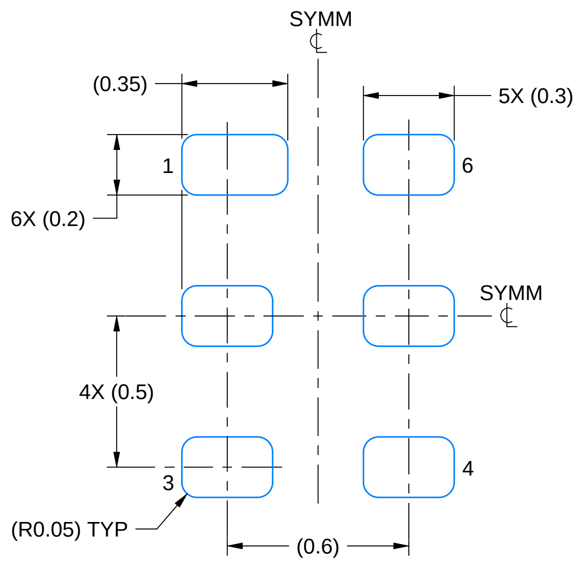
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

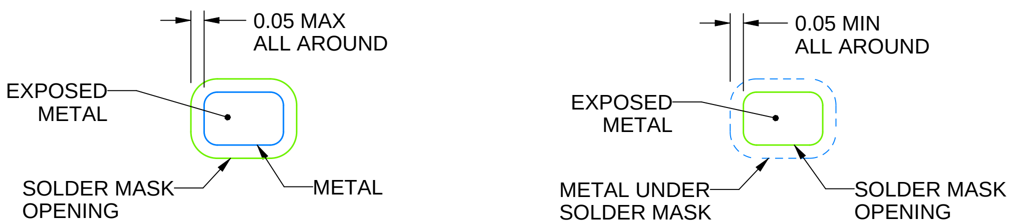


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



NON SOLDER MASK
DEFINED

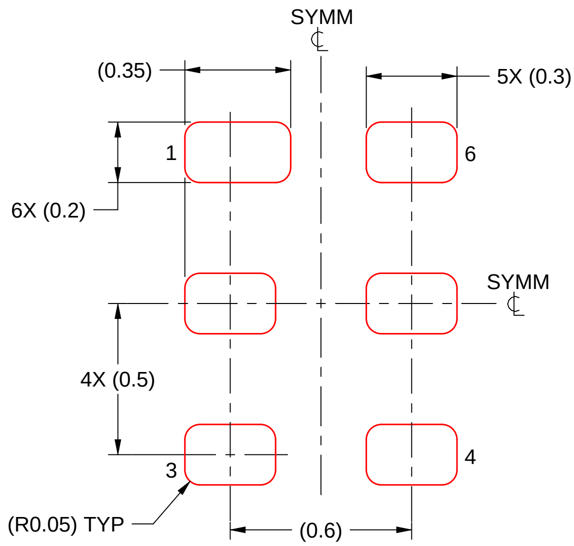
SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

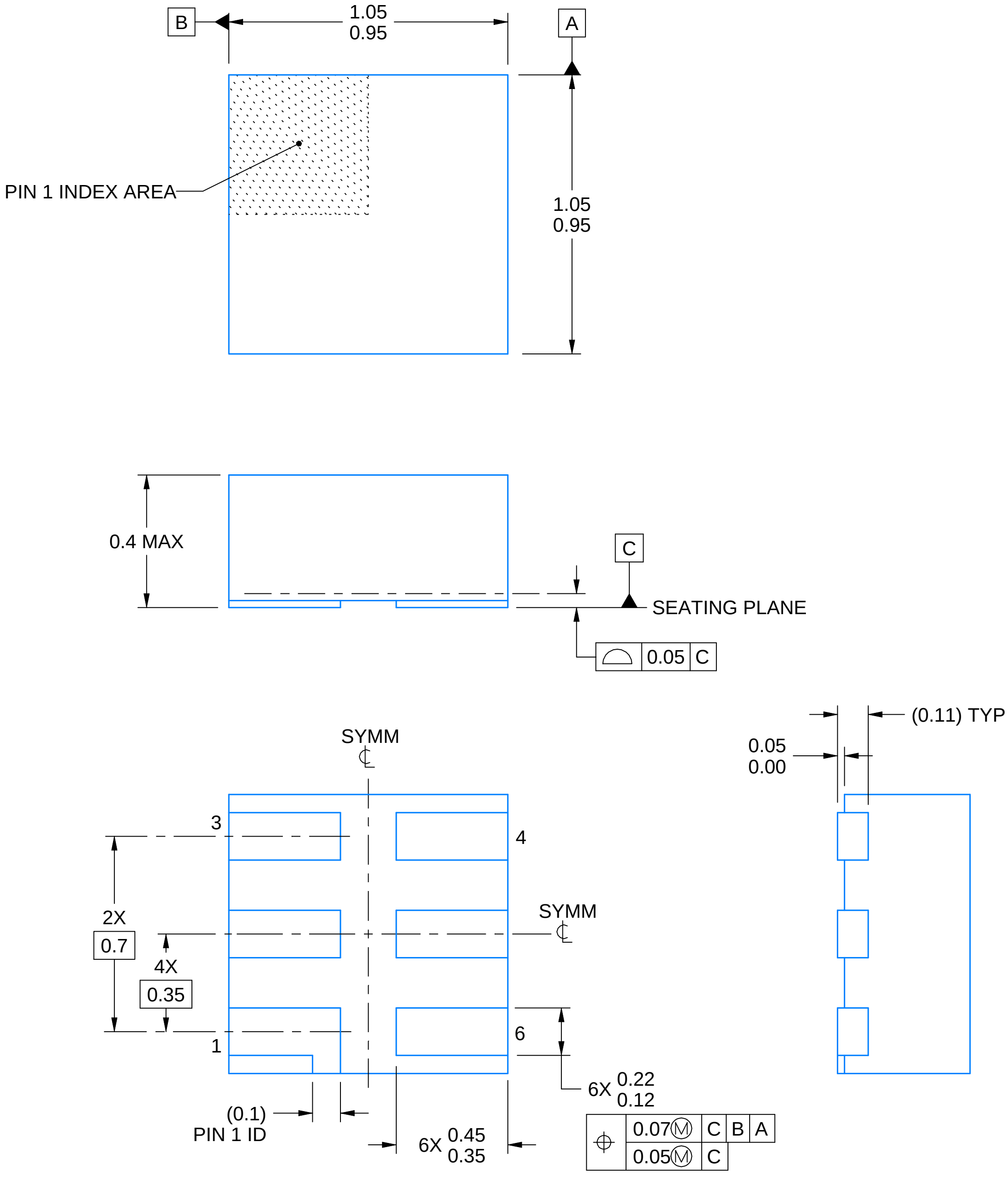
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

X2SON - 0.4 mm max height

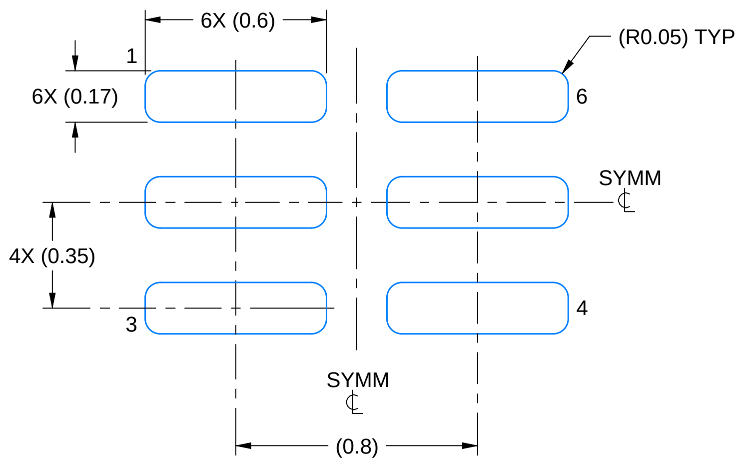
PLASTIC SMALL OUTLINE - NO LEAD



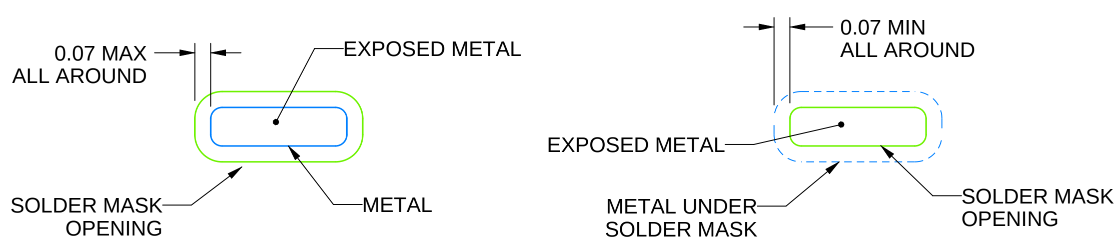
4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



NON SOLDER MASK
DEFINED

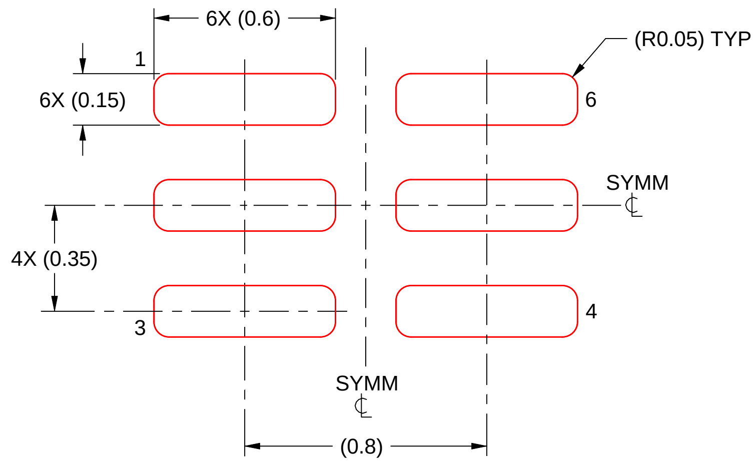
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



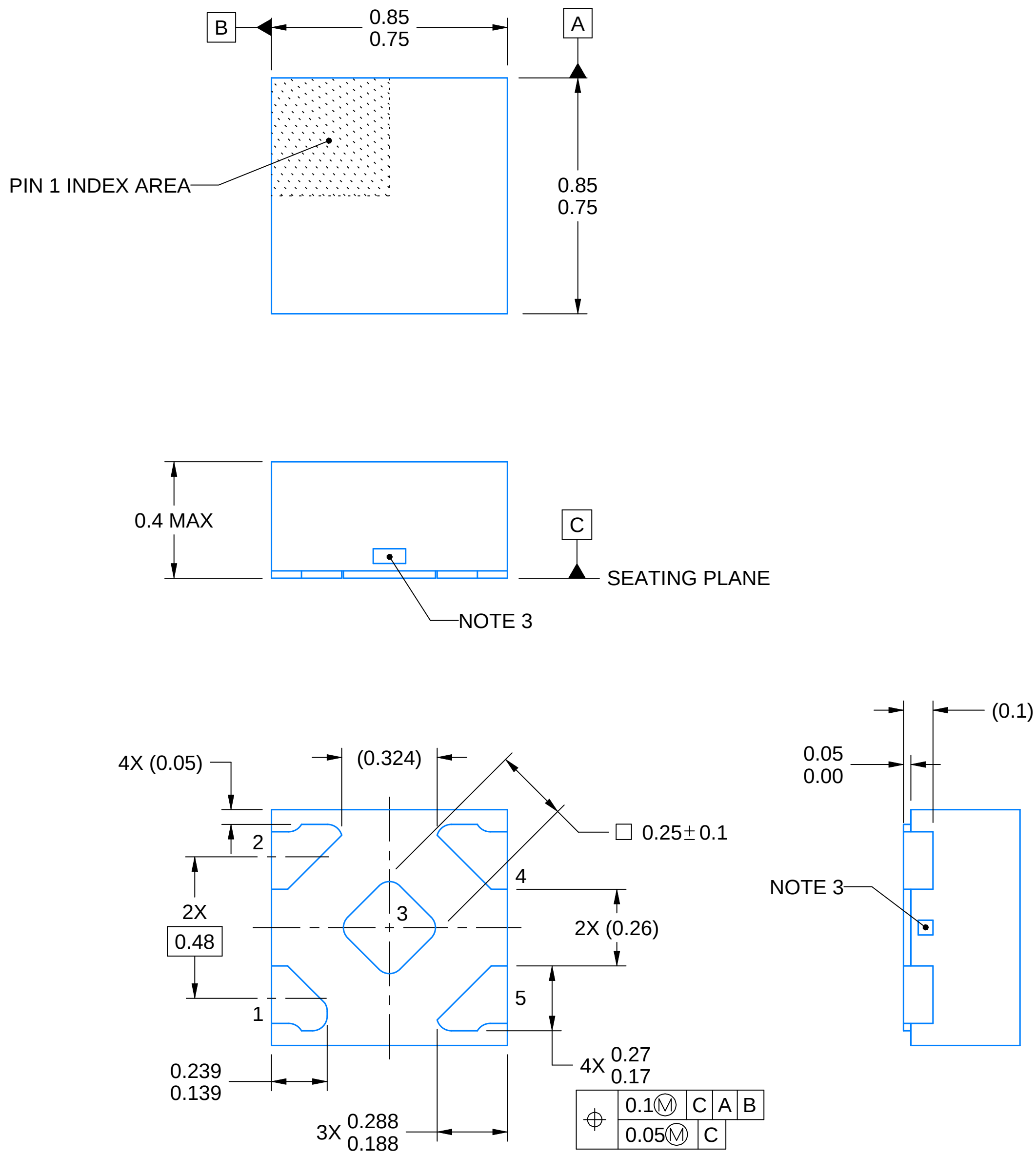
SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

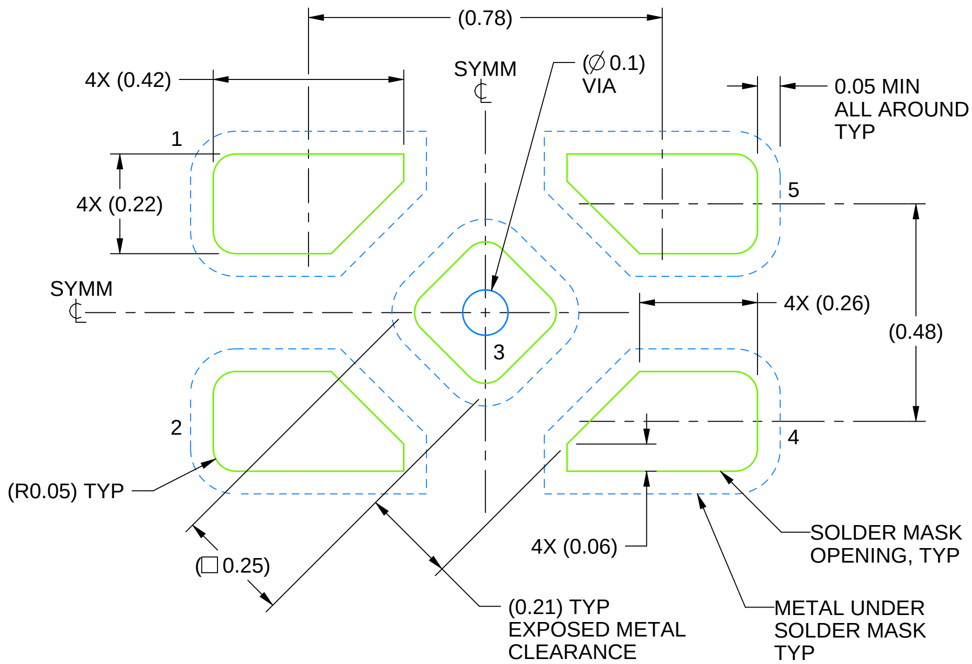
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

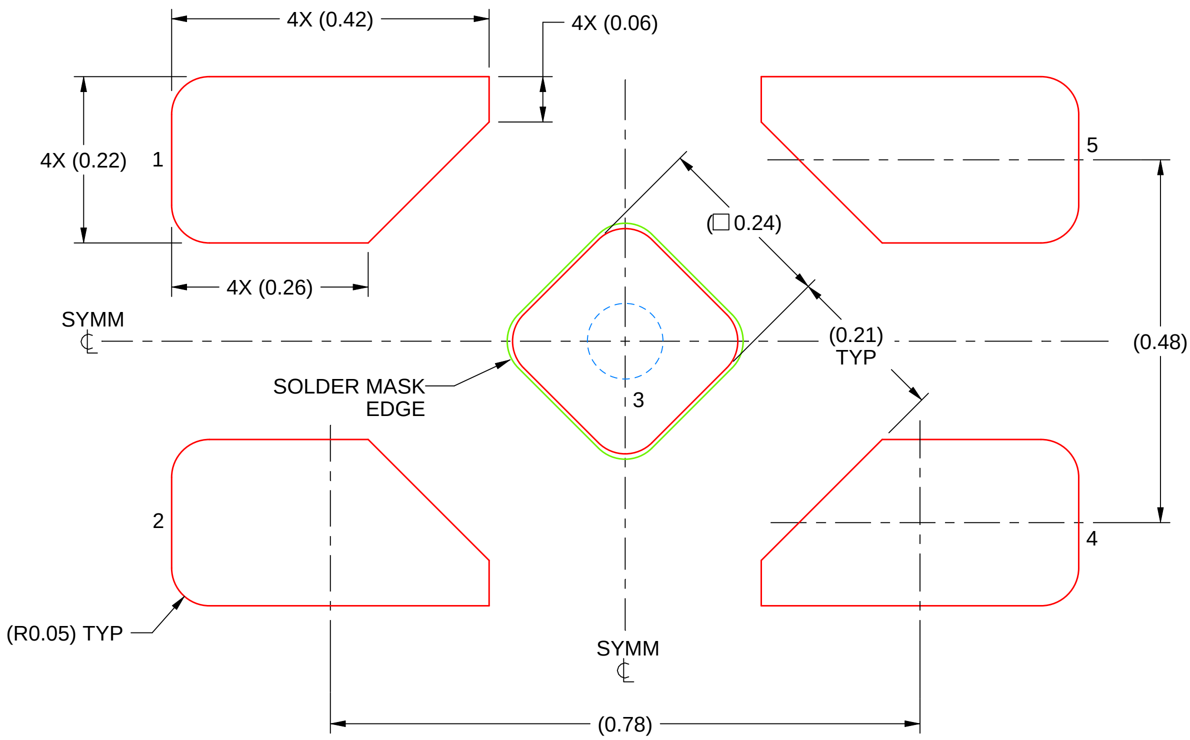


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



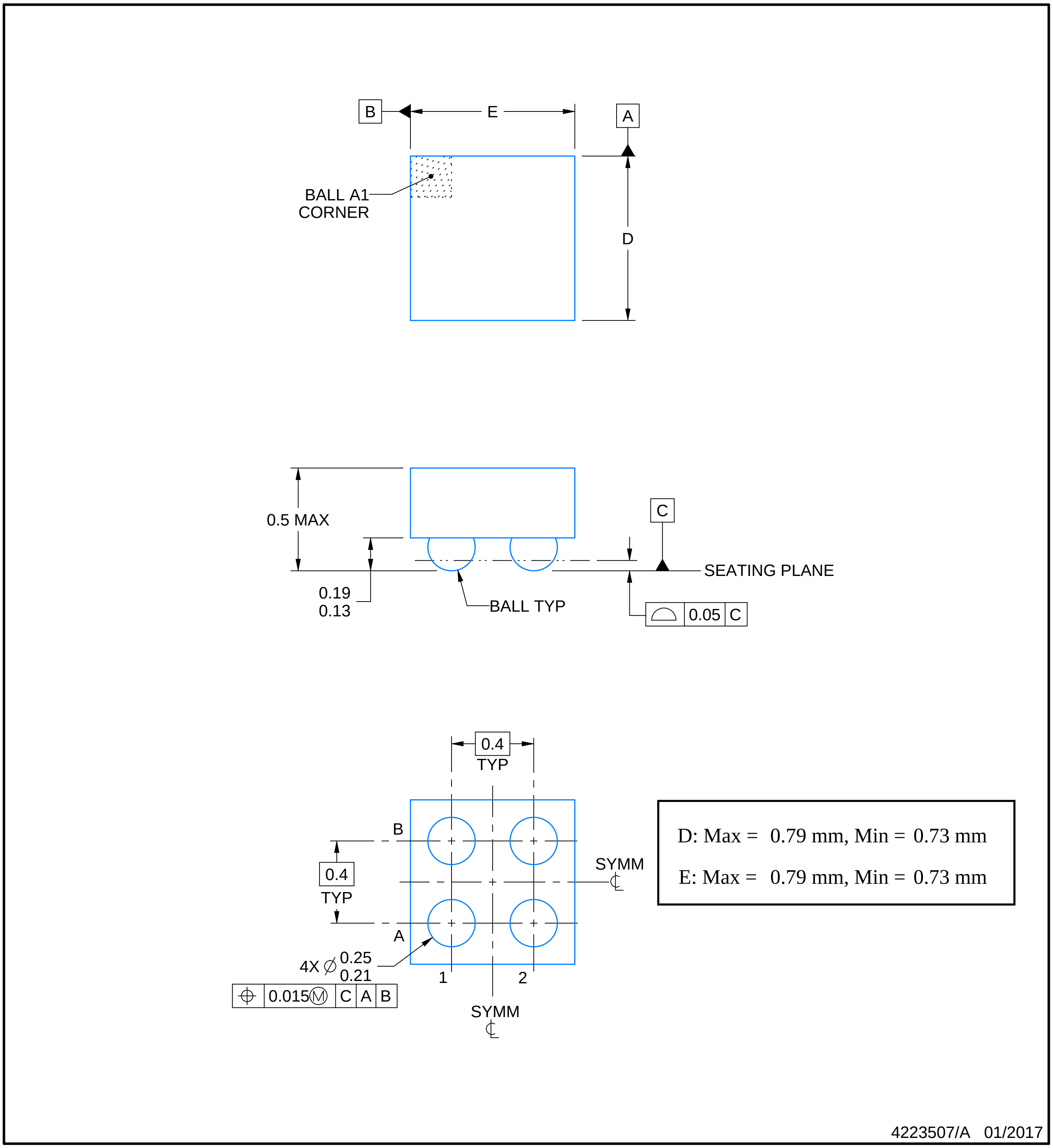
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

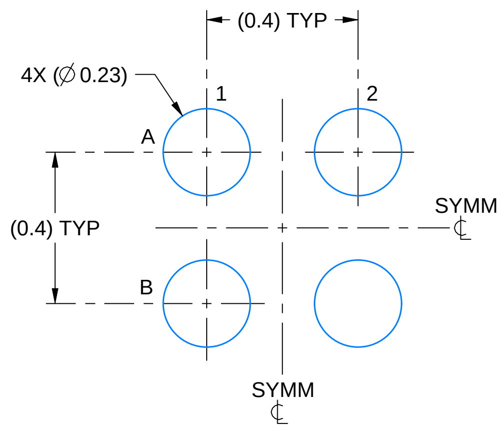
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

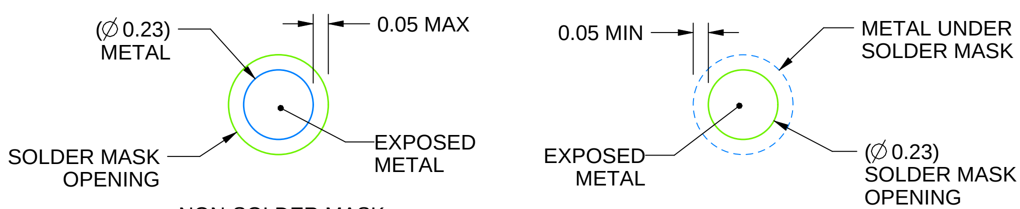


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



NON-SOLDER MASK
DEFINED
(PREFERRED)

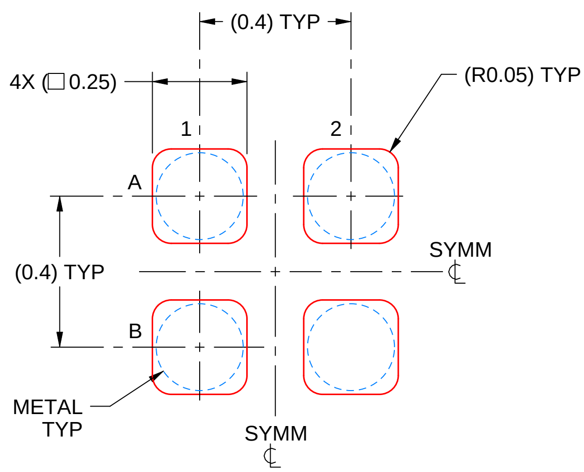
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4223507/A 01/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

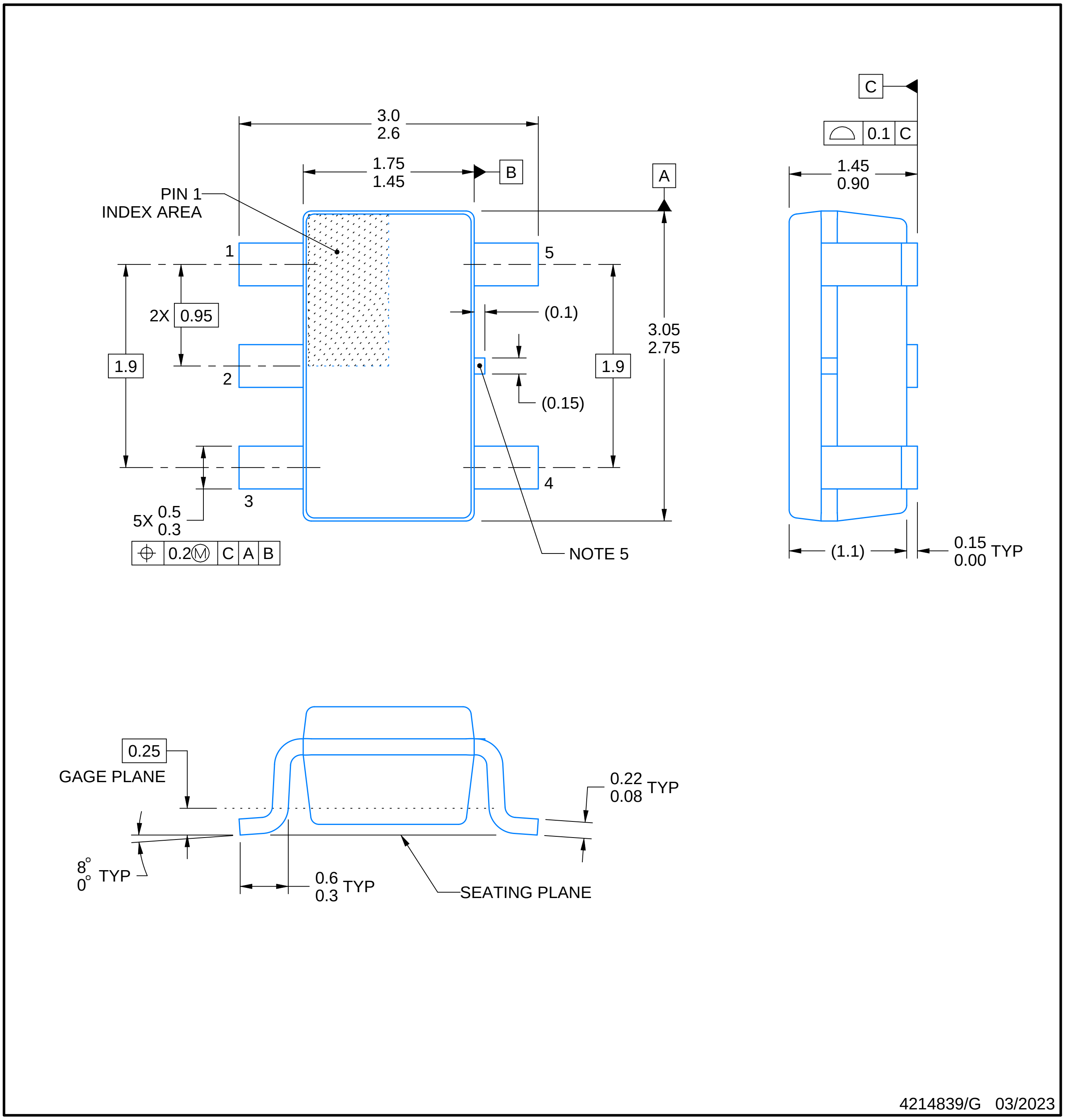


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223507/A 01/2017

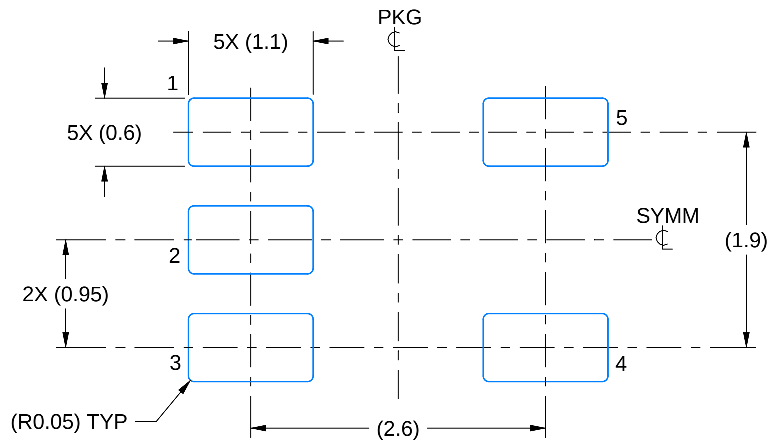
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

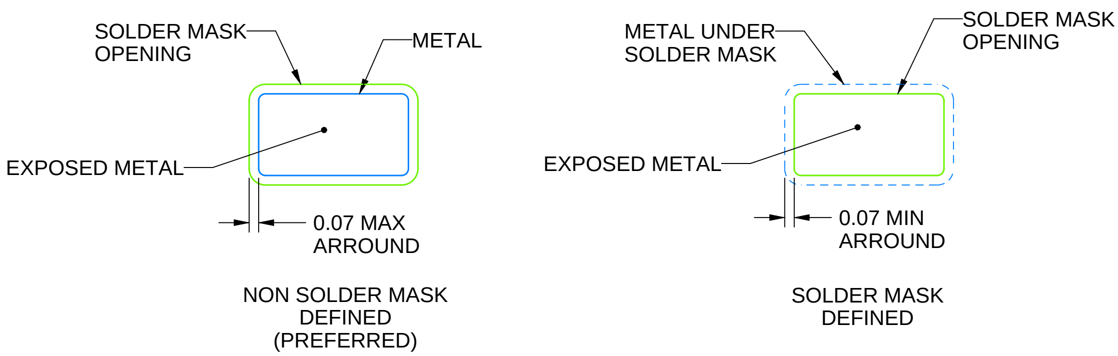


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

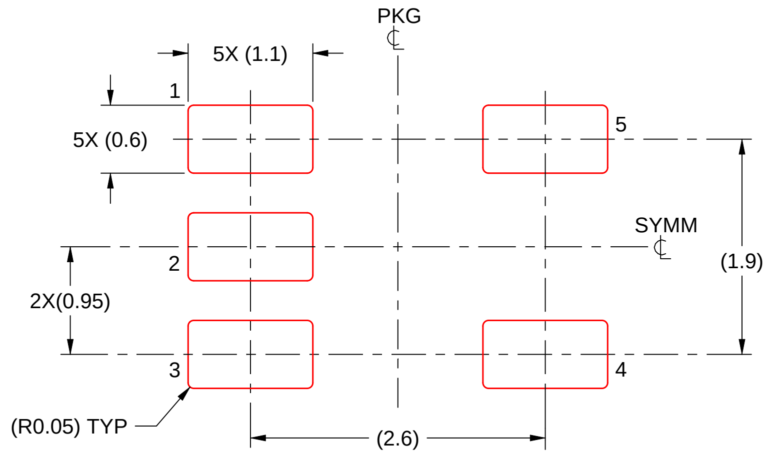


SOLDER MASK DETAILS

4214839/G 03/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

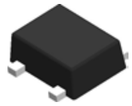


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/G 03/2023

NOTES: (continued)

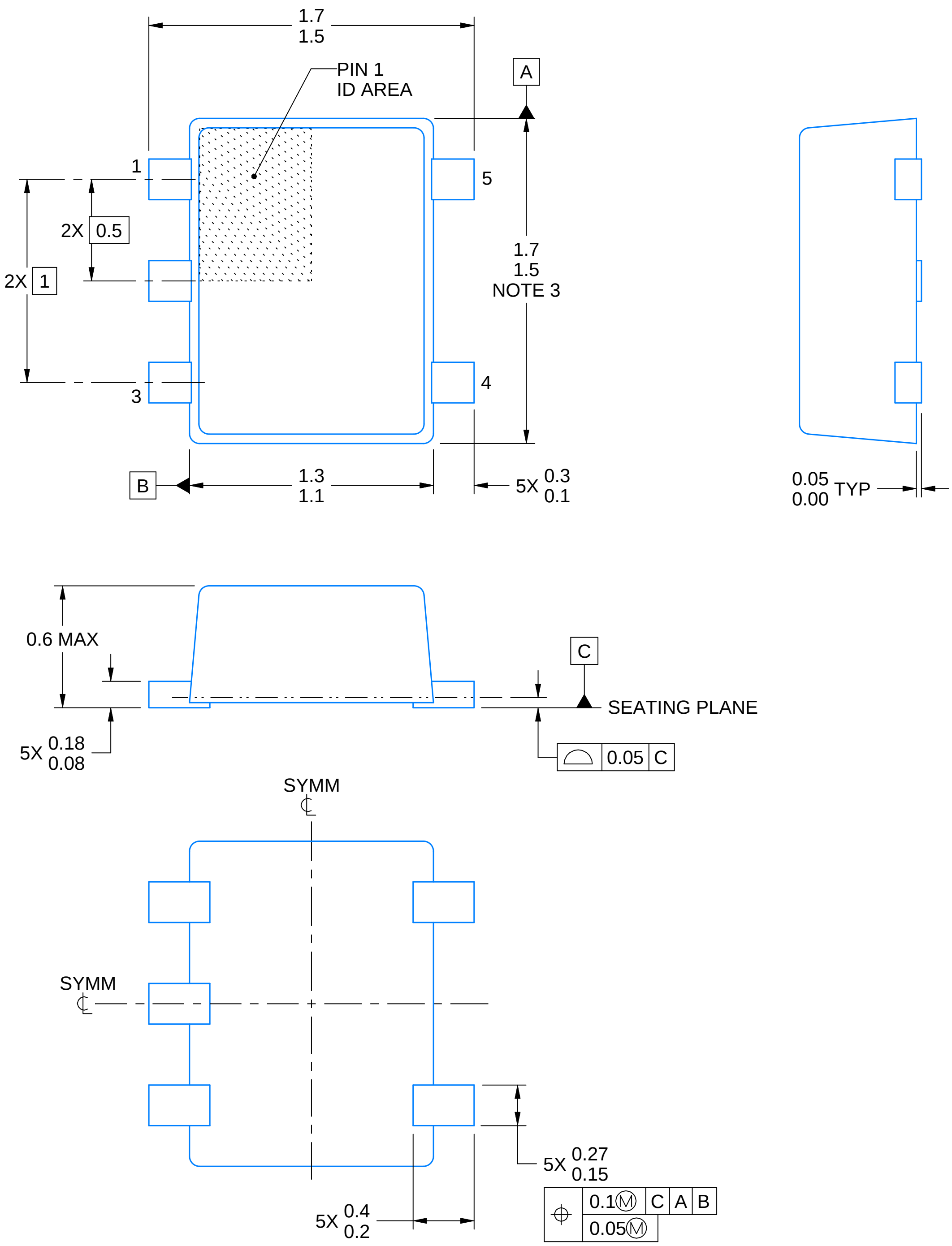
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

SOT - 0.6 mm max height

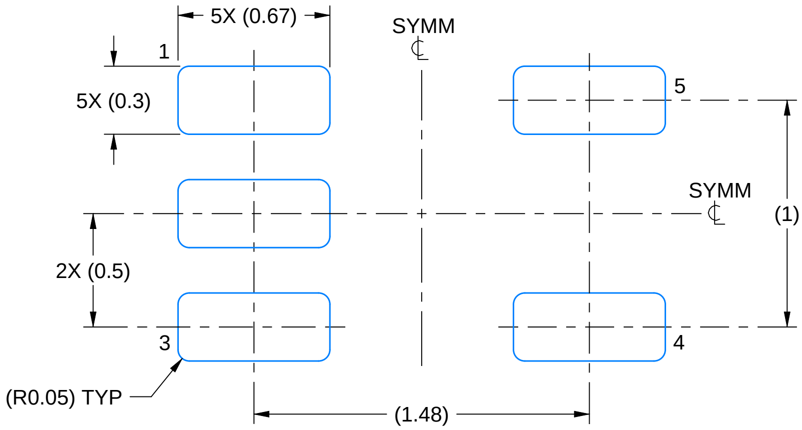
PLASTIC SMALL OUTLINE



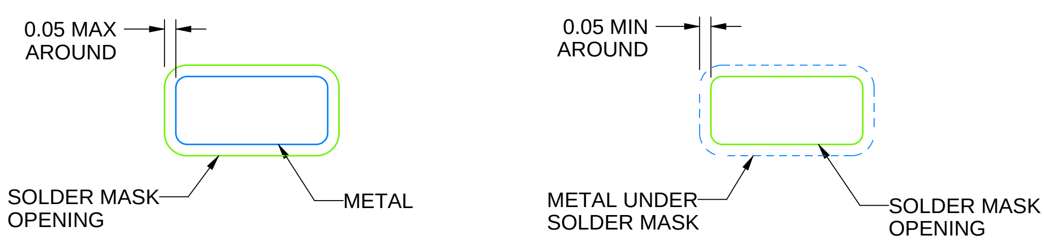
4220753/B 12/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X



NON SOLDER MASK
DEFINED
(PREFERRED)

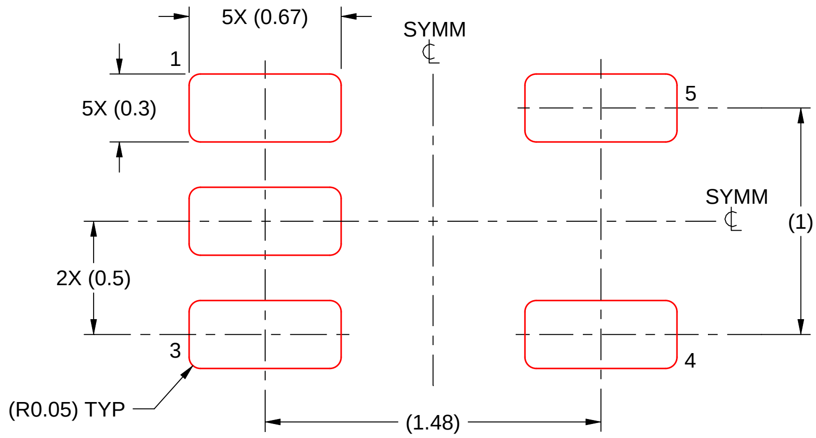
SOLDER MASK
DEFINED

SOLDERMASK DETAILS

4220753/B 12/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/B 12/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265