Project ECE 5460/6460:
Effect of Diameter Variation in CNTs

-Tasnuva Tarannum Tithi
-Divya Desiraju.

Introduction:

CMOS scaling has for the past four decades offered improved performance from one technology node to the next. However, as device scaling moves into the 32 nm node and beyond, there exist significant technology challenges[1].

Currently two of the most important challenges are:
1.the considerable increase of standby power dissipation and
2.the increasing variability in device characteristics (affecting circuit/system reliability)[1]

The international technology roadmap for semiconductors (ITRS) has identified seven postsilicon innovations that are likely candidates of the post-silicon CMOS era, with Carbon-based Nanoelectronics being recommended as the "Beyond CMOS" technology for accelerated development[1]

Introduction to CNT:

Carbon nanotubes (CNTs) are considered as one of the most promising new devices. CNFET avoid most of the fundamental limitations for traditional silicon devices.

(CNTs) offer unique mechanical and electronic properties:

- The potential for molecular scale electronics[1].
- Ability to conduct as either metal or semiconductor depending on chirality[1].
- CMOS fabrication process and infrastructure can be reused, as the operation principle and device structure are similar to CMOS devices.
- CNFET has the best experimentally demonstrated device current carrying ability till date.
- Carrier scattering along the channel is small.
- Conduction band and valence band have symmetrical band structures that lead to more balanced current drive for complementary circuits.
- In addition to the electrical properties carbon nanotube FETs are less sensitive to many process parameter variations compared to conventional MOSFETs [1].

Motivation:

Although every process parameter variation drastically affects the conventional MOSFET performance, it is found that nanowire/nanotube FETs are significantly less sensitive to many process parameter variations due to their inherent device structures and geometric properties [2].

The Schottky barrier (SB) at the contacts of a CNFET plays a crucial role in determining the performance of the device [8]. The height of the SB between a CNT and its metal contact depends on several material parameters, such as the metal contact work function, the environment to which the device is exposed, and the diameter of the nanotube[8]. There can be many sources of variation and it is desirable to study how they affect the device.In our project, we have simulated halfadder circuit to simulate the effect of diameter variation on CNFET based circuits.

About CNTs:

Physical Structure of CNTs:

CNTs are graphene sheets rolled up in to a cylinder. There are three distinct ways in which a graphene sheet can be rolled into a tube. That gives rise to three types of CNTs.

1. Armchair
2. zig-zag
3. Chiral

Armchair and zigzag structure can be obtained by rolling up the graphene sheet in along one of the symmetry axis. As in the case of chiral CNTs, the equivalent atoms of each unit cell are aligned on a spiral.
Again, if there is only one layer of graphene sheet is rolled to make a CNT, then it is called a single walled carbon nanotube (SWCNT), and if there are more than one layer of grapheme sheet rolled then it is called a multi walled CNT (MWCNT)[4][5].

Mechanical Properties of CNTs:

Steady progress has been made in exploring the mechanical properties and potential applications of two types of CNTs. Single-walled carbon nanotubes (SWCNT) and multi-walled carbon nanotubes (MWCNT). The measured specific tensile strength of a single layer of a multi-walled carbon nanotube can be as high as 100 times that of steel, and the graphene sheet (in-plane)

is as stiff as diamond at low strain. These mechanical properties motivate further study of possible applications for lightweight and high strength materials. Composite materials reinforced by either SWCNT or MWCNT have been fabricated and significant enhancement in mechanical properties has been recently reported [6][7].

Effect of process parameter variation:

MOSFETs and CNFETs both use lithography technique and, hence, will experience similar parametric variations . However, their impact on the electrostatic characteristics (mainly drive current and capacitance) of these devices will be different[2]. The impact of different parameters on the Ion and Cg for MOSFET and CNFET are summarized in table-1[2].

Parameter Variation	**Effect on MOSFET Ion**	**Effect on MOSFET Cg**	**Effect on CNTFET Ion**	**Effect on CNTFET Cg**
Leff	Strong	Strong	Null	Weak
tox	Strong	Strong	Weak	Weak
W	Strong	Strong	Null	Strong
Dopant Fluctuation	Strong	Weak	X	X
D	X	X	Strong	Weak

Table1: Effect of variation in different parameters in case of MOSFET and CNFET.X : not considered.

From table-1, we see that CNFETs are significantly less sensitive to variations in any geometry-related process parameters than conventional MOSFET devices. Effective channel length, oxide thickness, dopant fluctuation etc, when varied show weak influence on the gate capacitance and drive current of CNFETs. **The process parameter that when varying affects CNFETs the most is the diameter**.

While ever-increasing difficulty in controlling process parameter variations may become the ultimate limiting factor for conventional MOSFET devices in

future technologies, carbon nanotube and nanowire devices can conveniently overcome this bottleneck, as CNFET devices are far less sensitive to process variations compared to MOSFET devices [2].

Effect of Diameter variation in a half adder circuit:

We simulate a half adder circuit with CNTFET having different chiralities (m,n). In this study we focus on the worst cases or corners, when all the transistors have a larger or smaller diameter than the typical. Tube diameters are varied to within ±10% of a 1.51nm diameter which corresponds to a typical chirality of (19, 0).

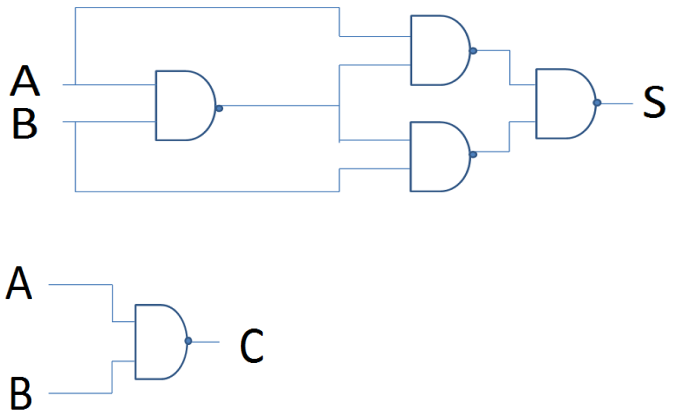

Figure1: Half adder circuit

Simulation:

We use HSPICE simulations to simulate our half adder. The technology used is 32nm technology. To simulate different diameters, we change the chirality (m,n). The diameters can be found from the equation:

$D = \frac{\sqrt{3}a}{\pi} * \sqrt{mn + m^2 + n^2}$ [3].

Where *a* = 0.142 nm is the interatomic distance between each carbon atom and its neighbor. We change the chirality of the CNT (value of m and n) to simulate for different diameters. The simulation evaluates the effect of diameter variability on performance for diameter values of 1.659nm, 1.51nm (typical), and 1.379nm with chiralities of (14, 10), (19, 0) and (15, 4),respectively.

The I–V characteristics of the CNTFET are similar to MOSFET's. The threshold voltage is defined as the voltage required to turn ON transistor. The threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half bandgap that is an inverse function of the diameter.
i.e.

$$Vth \approx \frac{Eg}{2e} = \frac{\sqrt{3}}{3}\frac{aV\pi}{eDcnt}$$ [3].

Where a = 2.49 °A is the carbon to carbon atom distance, $V\pi$ = 3.033 eV is the carbon π–π bond energy in the bonding model, e is the unit electron charge, and DCNT is the CNT diameter [3].

We calculate average power, threshold voltage Vth and delay for the half adder output s (sum) and c (carry). We also calculate the power delay product for s and c. The findings are summarized in Table-2:

D (nm)	Vth (v)	Avg Power (W)	Delay(s) (ms)	Delay(c) (ms)	PDP (s)
1.37	0.315	1.003	5.9	1.66	5.9 E-3
1.51	0.285	1.008	4.48	1.305	4.5 E-3
1.659	0.260	1.029	3.99	1.175	4.015 E-3

Table 2: Simulated results from 32nm technology CNFET based half adder circuit.

HSPICE CODE used for simulation:

```
**************************************************
*For optimal accuracy, convergence, and runtime
**************************************************
.options POST
.options AUTOSTOP
```

```
.options INGOLD=2     DCON=1
.options GSHUNT=1e-12 RMIN=1e-15
.options ABSTOL=1e-5  ABSVDC=1e-4
.options RELTOL=1e-2  RELVDC=1e-2
.options NUMDGT=4     PIVOT=13
.param   TEMP=27
**************************************************
*Include relevant model files
**************************************************
.lib 'CNFET.lib' CNFET
**************************************************
*Beginning of circuit and device definitions
**************************************************
*Supplies and voltage params:
.param Supply=0.9
.param Vg='Supply'
.param Vd='Supply'
*Some CNFET parameters:
.param Ccsd=0      CoupleRatio=0
.param m_cnt=1     Efo=0.6
.param Wg=0        Cb=40e-12
.param Lg=32e-9    Lgef=100e-9
.param Vfn=0       Vfp=0
.param m=14        n=10
.param Hox=4e-9    Kox=16

**************************************************************
**********
* Define power supply
**************************************************************
**********
Vd1 Vdd Gnd Vd
Vs1 Vss Gnd 0
Vg1 Vgg Gnd Vg
Vsub Sub Gnd 0
VA A Gnd 0 0 PULSE(0 'Supply' 0 0.01p 0.01p 1n 2n)
VB B Gnd 0 0 PULSE(0 'Supply' 0 0.01p 0.01p 2n 4n)

**************************************************************
**************
*Sub-Circuits
**************************************************************
**********
.subckt halfadd A B S C Vdd Gnd
```

```
X1 R1 A Vdd Vdd PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X2 R1 B Vdd Vdd PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X3 R1 A 1 Gnd NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X4 1 B Gnd Gnd NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X5 R2 A Vdd Vdd PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X6 R2 Q1 Vdd Vdd PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X7 R2 A 2 Gnd NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X8 2 R1 Gnd Gnd NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X9 R3 B Vdd Vdd PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X10 R3 R1 Vdd Vdd PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X11 R3 B 3 Gnd NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X12 3 R1 Gnd Gnd NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X13 S R2 Vdd Vdd PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X14 S R3 Vdd Vdd PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X15 S R2 4 Gnd NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
```

```
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X16 4 R3 Gnd Gnd NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X17 5 A Vdd Vdd PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X18 5 B Vdd Vdd PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X19 5 A 6 Gnd NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X20 6 B Gnd Gnd NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X21 C 5 Vdd Vdd PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
X22 C 5 Gnd Gnd NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-
9  n1=m  n2=n  tubes=3
.ends

**********************************************************************
**********
* Main Circuits
**********************************************************************
**********
* implement halfadder
Xhalfa A B S C Vdd Gnd halfadd
**********************************************************************
**********
* Measurements
**********************************************************************
**********
.TRAN 1p 10n
*.tran STEP=1p STOP=10n sweep wn lin 5 1.0
*.meas tran tplh_A1Bf trig V(A) td=1ns val='Vdd/2' cross=1
*+ targ V(S) td=1ns val='Vdd/2' cross=1
.meas tran avgpower AVG power from=1ns to=10ns
.meas tran peakpower MAX power from=1ns to=10ns
.end
```

Waveforms generated in synopsis custom waveview for the circuits corresponding to 3 different diameters:

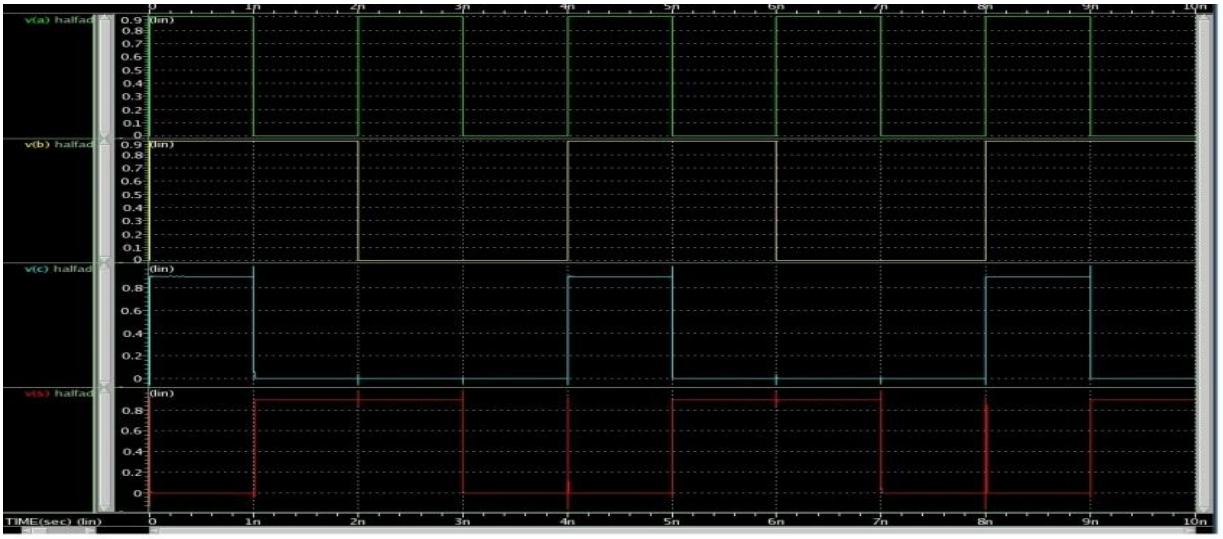

Fig 2a)

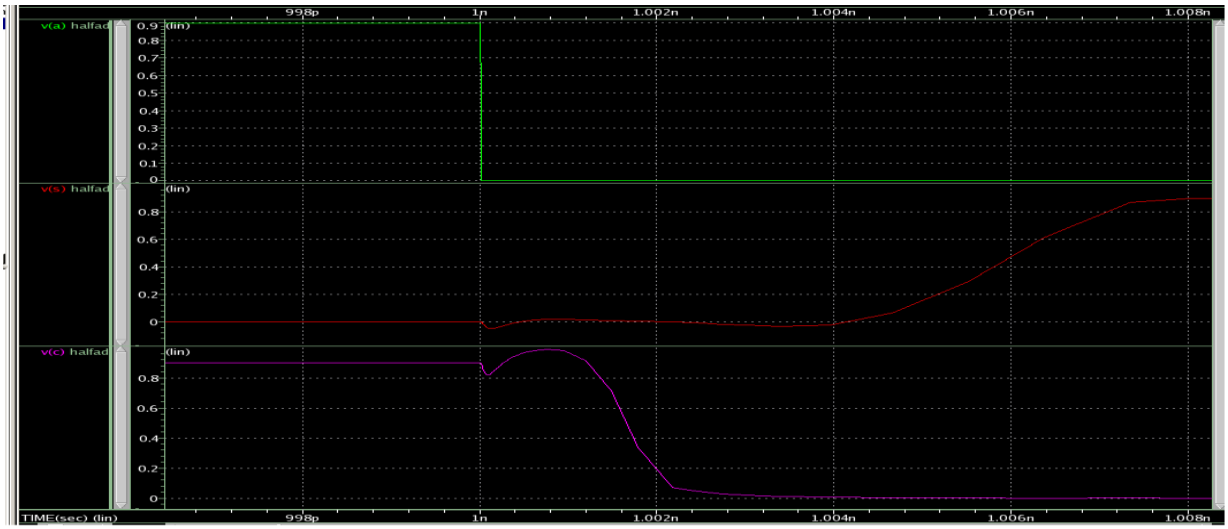

Fig 2b)

Figure 2: Input and output waveforms for CNTFET half adder with chirality (15,4) and diameter 1.37nm.

Output delay for Sum,S= 5.9 ms
Output delay for Carry, C=1.66ms

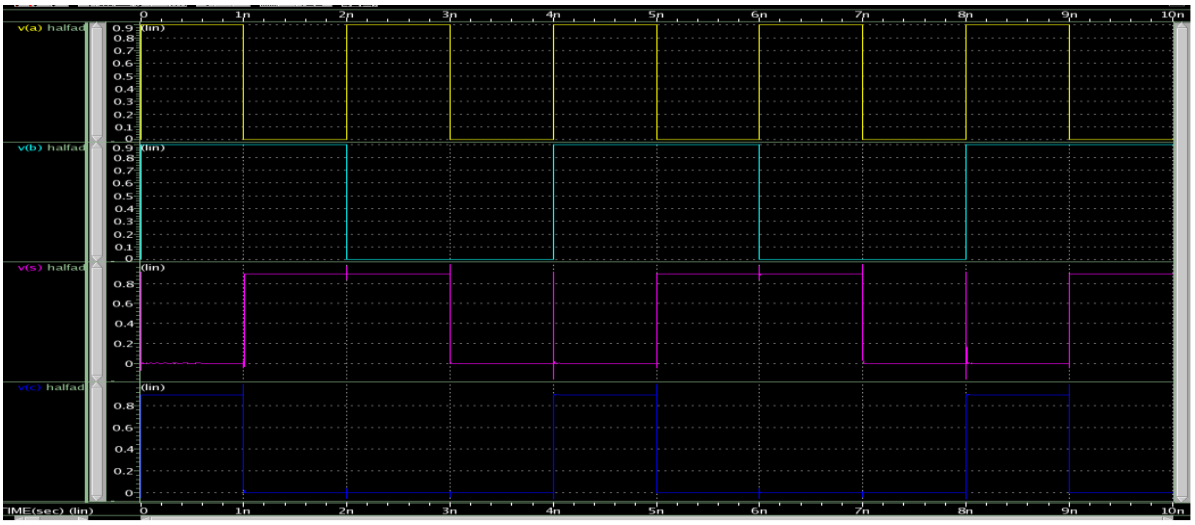

Fig 3a)

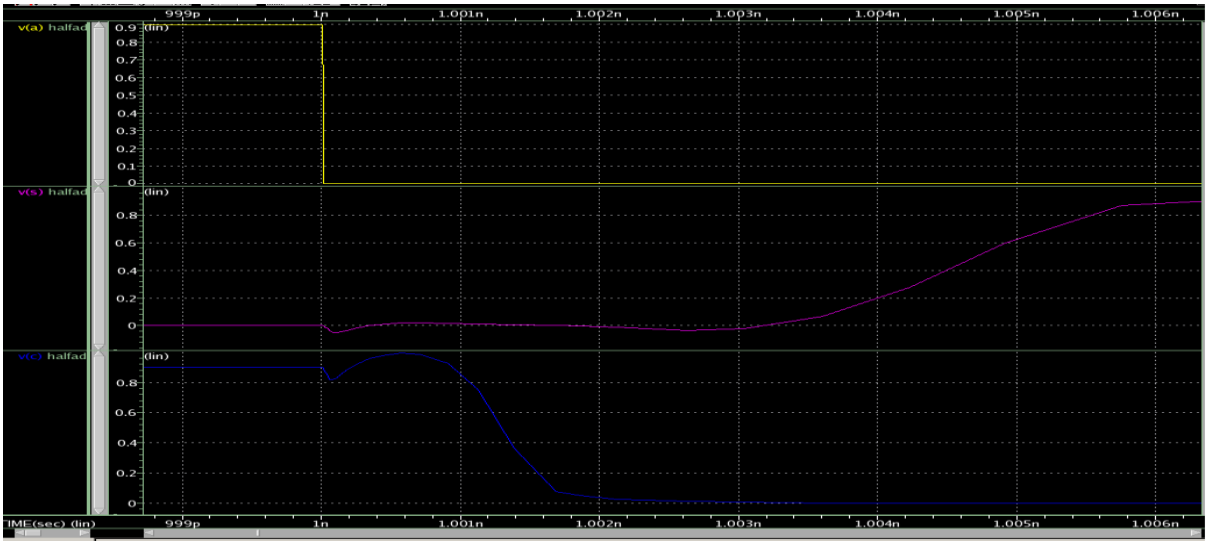

Fig 3b)

Figure 3: Input and output waveforms for CNTFET half adder with chirality (19,0) and diameter 1.51nm.

Output delay for Sum,S= 4.48 ms
Output delay for Carry, C= 1.305 ms

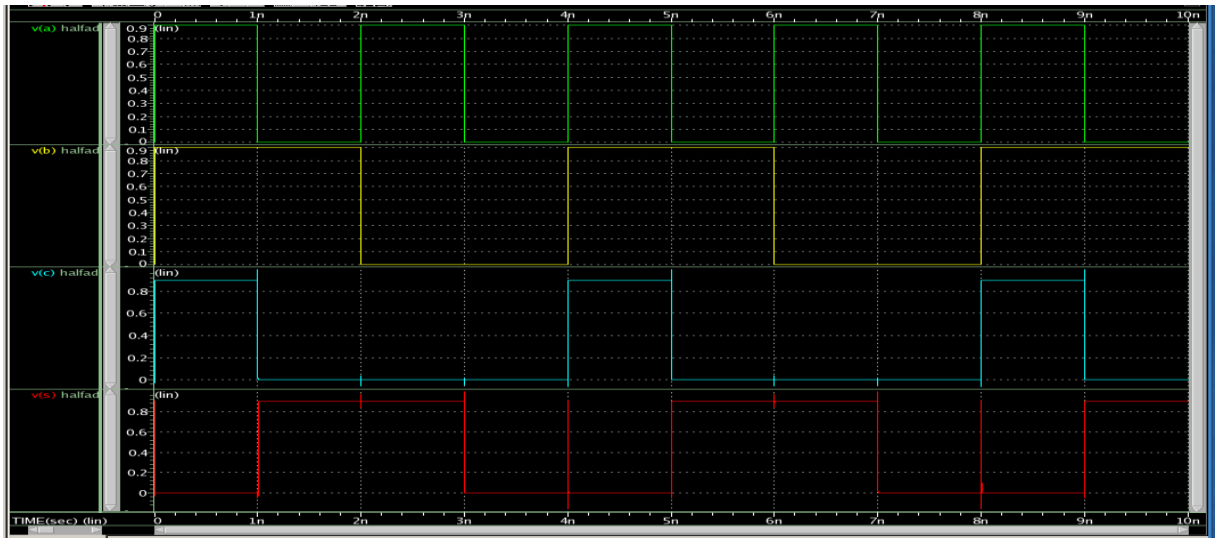

Fig 4a)

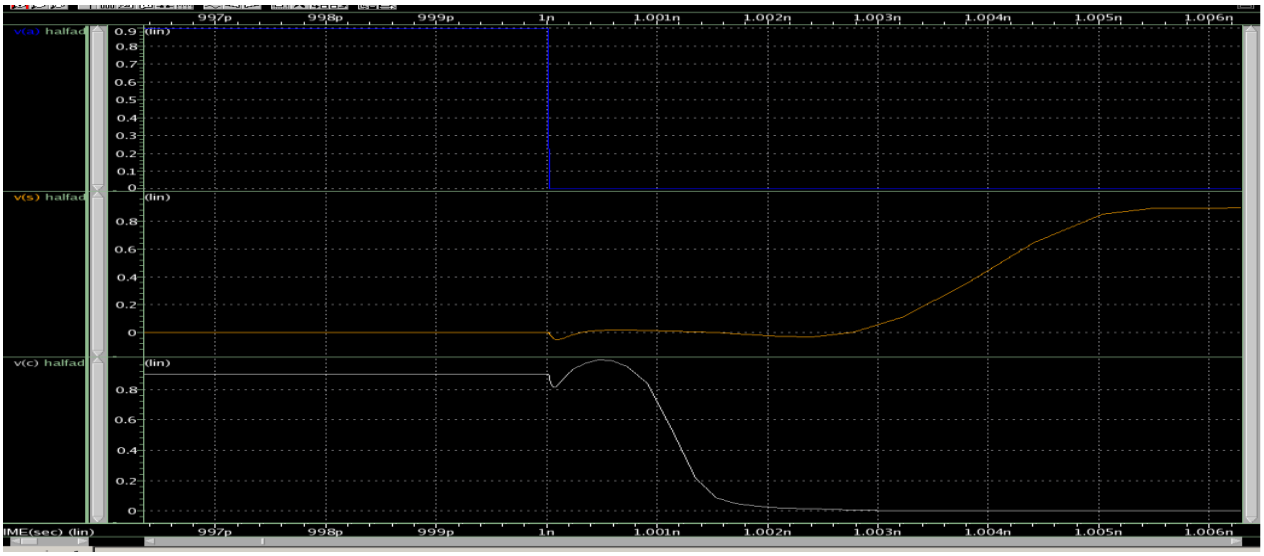

Fig 4b)

Fig 4: Input and output waveforms for CNTFET half adder with chirality (14,10) and diameter 1.659nm.

Output delay for Sum,S= 3.99 ms
Output delay for Carry, C= 1.175 ms

Observation:

From the simulated results we see that, for IC implementation, large-diameter nanotube is desirable for its low contact resistance and enhanced mobility. However, the off-current *I*off associated with such devices will be higher.

Solution to **diameter** Variation
Chemical vapor deposition (CVD) is a promising method of producing SWCNTs. It offers:

- versatile control
- the possibility of scaling-up.

REFERENCES:

[1] **Performance of CNFET SRAM Cells under Diameter Variation Corners** Zhe Zhang, Yanmin Liu, Jabulani Nyathi and José G. Delgado-Frias School of Electrical Engineering and Computer Science, Washington State University
{zzhang, yliu, jabu, jdelgado}@eecs.wsu.edu
[2] **Impact of a Process Variation on Nanowire and Nanotube Device Performance** Bipul C. Paul, *Senior Member, IEEE*, Shinobu Fujita, *Member, IEEE*, Masaki Okajima,Thomas H. Lee, *Member, IEEE*, H.-S. Philip Wong, *Fellow, IEEE*, and Yoshio Nishi, *Fellow, IEEE*
[3] **CNTFET-Based Design of Ternary Logic Gates and Arithmetic Circuits** Sheng Lin*, Student Member, IEEE*, Yong-Bin Kim*, Senior Member, IEEE*, and Fabrizio Lombardi*, Fellow, IEEE*
[4] http://www.personal.reading.ac.uk/~scsharip/tubes.htm
[5] Wikipedia.
[6] **Mechanical properties of carbon nanotubes: theoretical predictions and experimental measurements** Rodney S. Ruoff , Dong Qian , Wing Kam Liu
[7] **Molecular design of strong single-wall carbon nanotube/ polyelectrolyte multilayer composites, Nature Materials 1 (2002) 190–194.** A.A. Mamedv, N.A. Kotov, M. Prato, D.M. Guldi, J.P. Wicksted, A. Hirsch,
[8] **Effect of Diameter Variation in a Large Set of Carbon Nanotube Transistors Yu-Chih Tseng,* Kinyip Phoa, David Carlton, and Jeffrey Bokor** Department of Electrical Engineering and Computer Sciences, UniVersity of California at Berkeley, Berkeley, California 94720