

A decorative graphic consisting of blue circuit lines with circular nodes, extending horizontally from the left and right sides of the central text box.

# KECCAK-BASED BITCOIN MINER DESIGN PROJECT B

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## PROBLEM SPECIFICATION

- What is Bitcoin Mining?
- Challenges of SHA3-256 in Hardware
- Why use Keccak (SHA3-256)

# WHAT IS BITCOIN MINING?

- The process of finding a numeric *nonce* that, when combined with a block's header data and hashed, produces a hash value below a target threshold
- Miners iterate over nonces, hashing the 80-byte block header
  - checking if the resulting hash is sufficiently small
- This ensures that finding a valid block is *computationally hard*



# CHALLENGES OF SHA3-256 IN HARDWARE

- The SHA3-256 algorithm involves 64 rounds per hash
  - Bitcoin uses a double hash, thus 128 rounds total
- Fully unrolling and pipelining all 64 rounds can yield one hash result per clock cycle
  - Doing this for double-hash doubles resource usage
- Hardware Bitcoin miners often split work:
  - Pre-compute the first SHA-256 of the static part of the block header
  - Repeatedly compute the second SHA-256 for each nonce in hardware

# WHY USE KECCAK (SHA3-256)?

- Keccak (the core of SHA-3) is explored here as an alternative hash function for mining.
- Keccak was designed for efficiency in hardware:
  - *“Thanks to its symmetry and chosen operations, [Keccak’s] design is well-suited for ultra-fast hardware implementations and the exploitation of pipelining”.*
- Can achieve at least **4×** the performance of comparable SHA-2 implementations at roughly similar power consumption
- This Project is designed to investigate FPGA acceleration of the Bitcoin mining algorithm

```
Keccak[r, c, d](M){
```

*Initialization and padding:*

$S[x, y] = 0,$   $\forall (x, y) \text{ in } (0 \dots 4, 0 \dots 4)$

$P = M \parallel 0x01 \parallel \text{byte}(d) \parallel \text{byte}\left(\frac{r}{8}\right) \parallel 0x01 \parallel 0x00 \parallel \dots \parallel 0x00$

*Absorbing phase:*

$\forall \text{ block } P_i \text{ in } P$

$S[x, y] = S[x, y] \oplus P[x + 5y],$   $\forall (x, y) \text{ such that } (x + 5y) < \left(\frac{r}{w}\right)$

$S = \text{Keccak} - f[r + c](S)$

*Squeezing phase:*

$Z = \text{empty string}$

*while output is requested*

$Z = Z \parallel S[x, y],$   $\forall (x, y) \text{ such that } (x + 5y) < \left(\frac{r}{w}\right)$

$S = \text{Keccak} - f[r + c](S)$

*return Z*

```
}
```

Input: message M

1. Pad M with multi-rate padding (delimit M with 0x06 and 0x80)

2. Break padded M into blocks of r bits

3. Initialize 1600-bit state to zero

4. For each block:

XOR block into the first r bits of state

Apply Keccak-f[1600] permutation

5. Output first 256 bits of state (truncate or continue permutation for longer output)

## ALGORITHM TO BE INVESTIGATED (BITCOIN MINING WITH KECCAK)

Designated as SHA3 by NIST in 2015, Keccak is a secure hash algorithm known for its radically different algorithmic approach to previous hash algorithms (SHA-1, SHA-2).

It is invulnerable to many attacks which could compromise previous algorithms and allows arbitrary-length input.

It is used by Ethereum as its new core algorithm.



## PROJECT AIMS

- Functional Hardware Miner
- Accelerated Hash Computation
- FPGA Capability Showcase?
- Performance Comparison & Analysis



# THE FLOW OF MINING

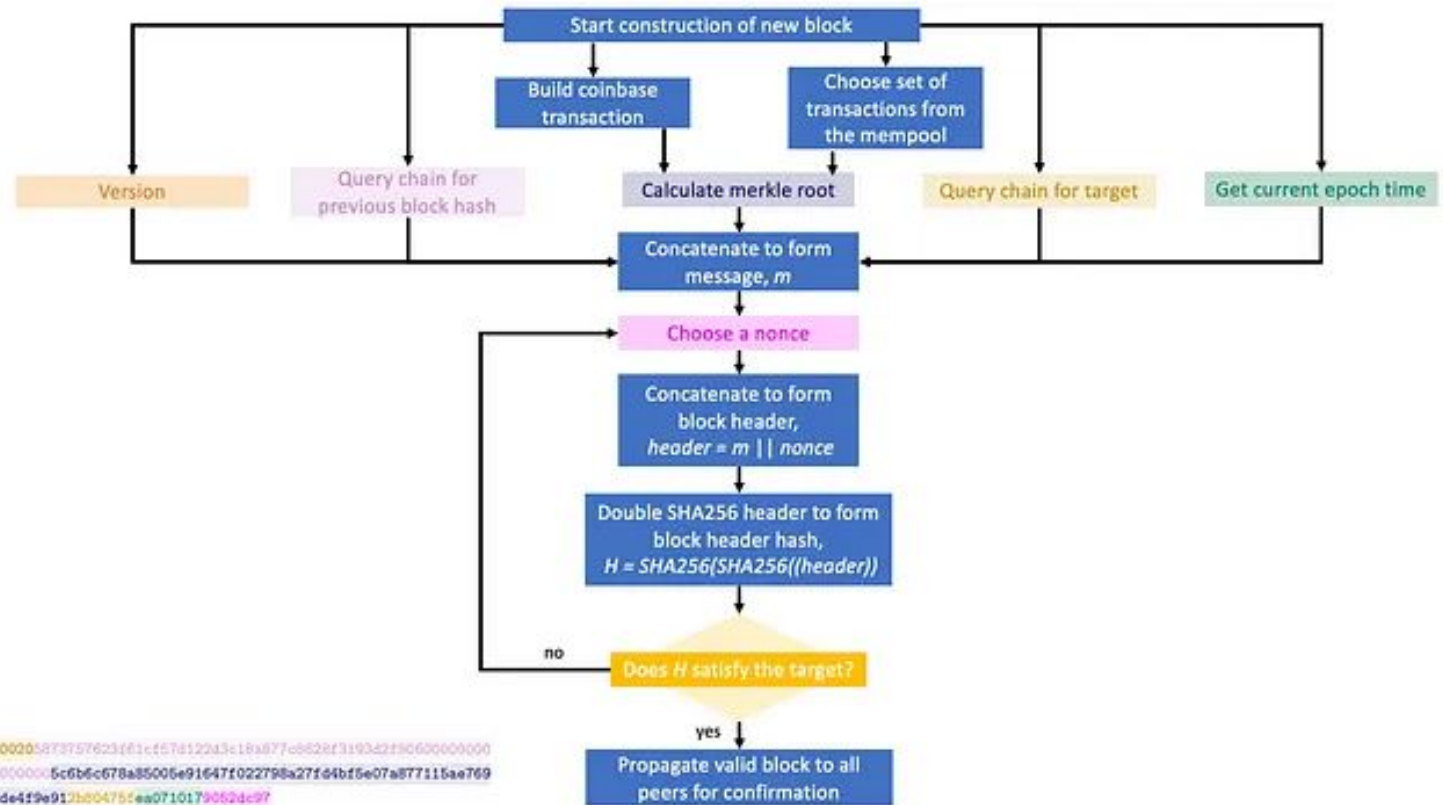
The process of mining in a blockchain network is essentially a competition of hashing.

For the sake of demonstration, we will ignore the computations of

- Merkle roots
- Queries of previous block hash
- Version sync

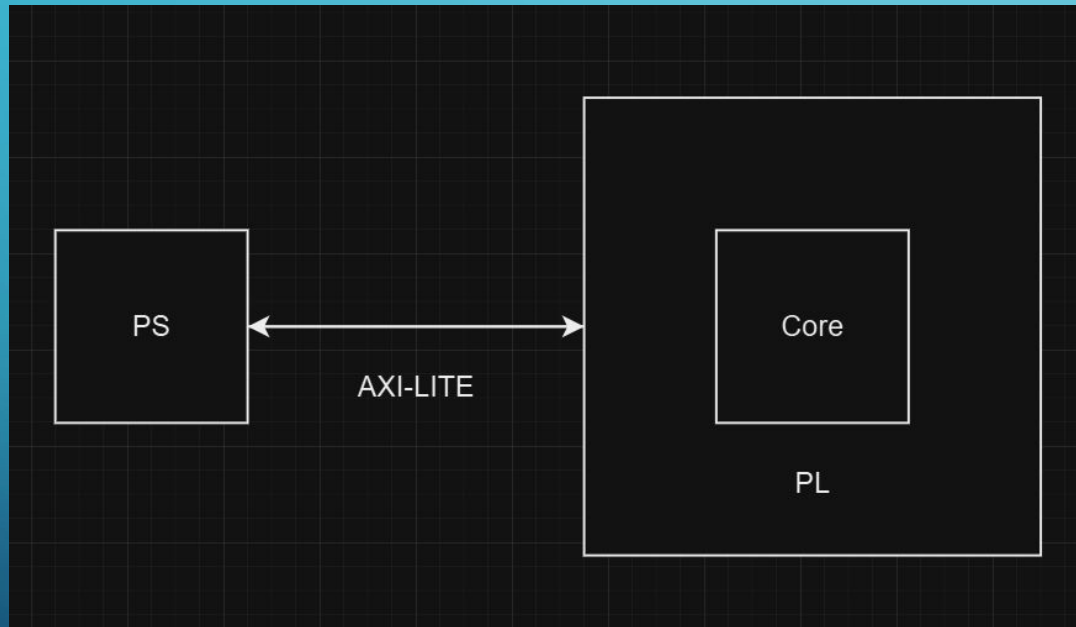
We are interested in accelerating the Keccak algorithm as the core hash over a fixed header.

Name	Type	Bytes	Description
version	int32_t	4	Version number
previous hash	char[32]	32	Hash of the previous block header in internal byte order
merkle root	char[32]	32	Merkle root of the transactions included in the block formatted in internal byte order
time	uint32_t	4	Epoch timestamp of the block
bits	uint32_t	4	Encodes the network target difficulty
nonce	uint32_t	4	Dedicated number to be updated to generate unique hashes





# FUNCTIONAL HARDWARE MINER

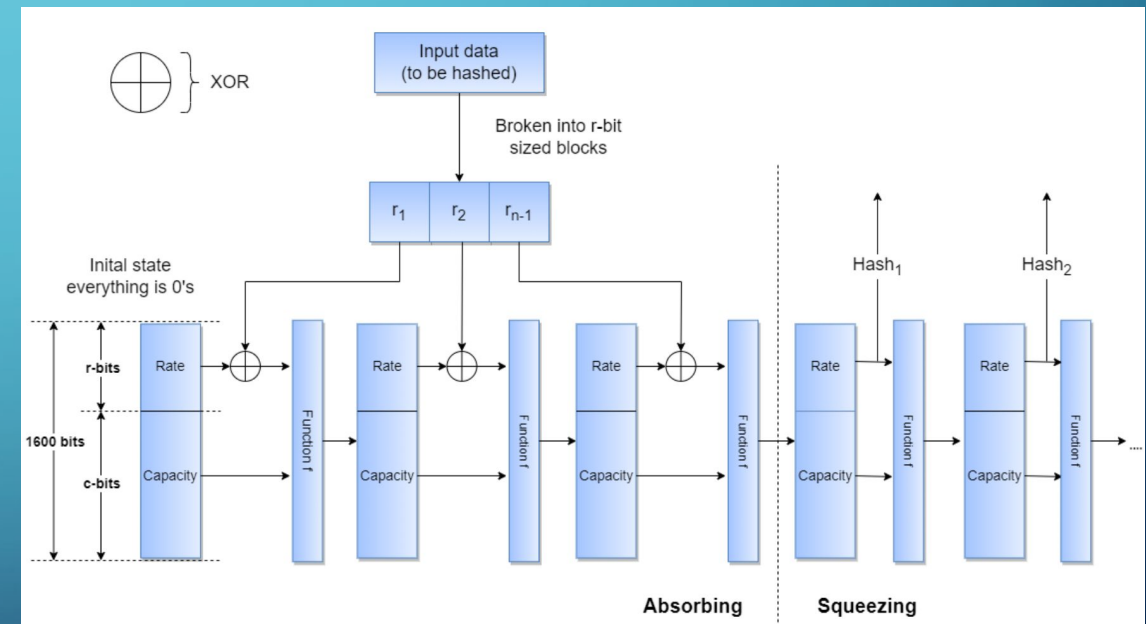


- This project uses a simple AXI-Lite interface for communication between PS and PL
- The PS contains a predefined target value to evaluate the mining result
- A nonce from the block is sent to PL via AXI-Lite
- The core processes the nonce, and the result is sent back to the PS
- The PS then compares the result with the target:
  - If the result  $\geq$  target, then PS sends it back for the next iteration
  - If the result  $<$  target, then valid nonce is found

# ACCELERATED HASH COMPUTATIONS

## Keccak Function Overview:

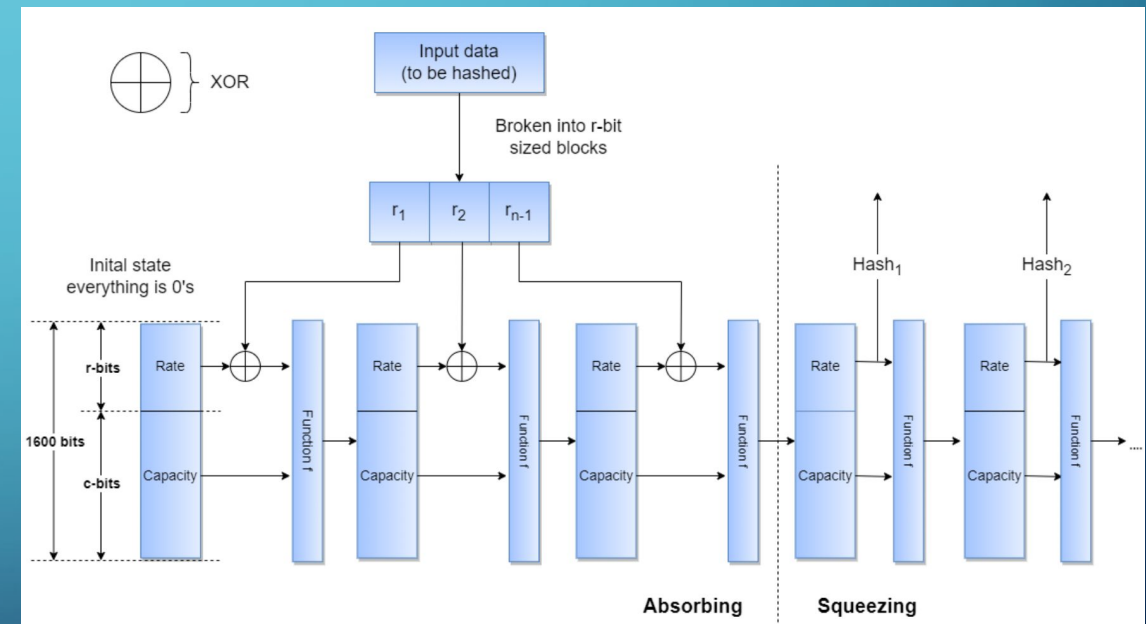
- Initial State:
  - A 1600-bit internal state initialized to all zeros, split into
    - r bits (Rate): interfaces with input and output
    - c bits (Capacity): Provides cryptographic strength



# ACCELERATED HASH COMPUTATIONS

## Absorbing Stage

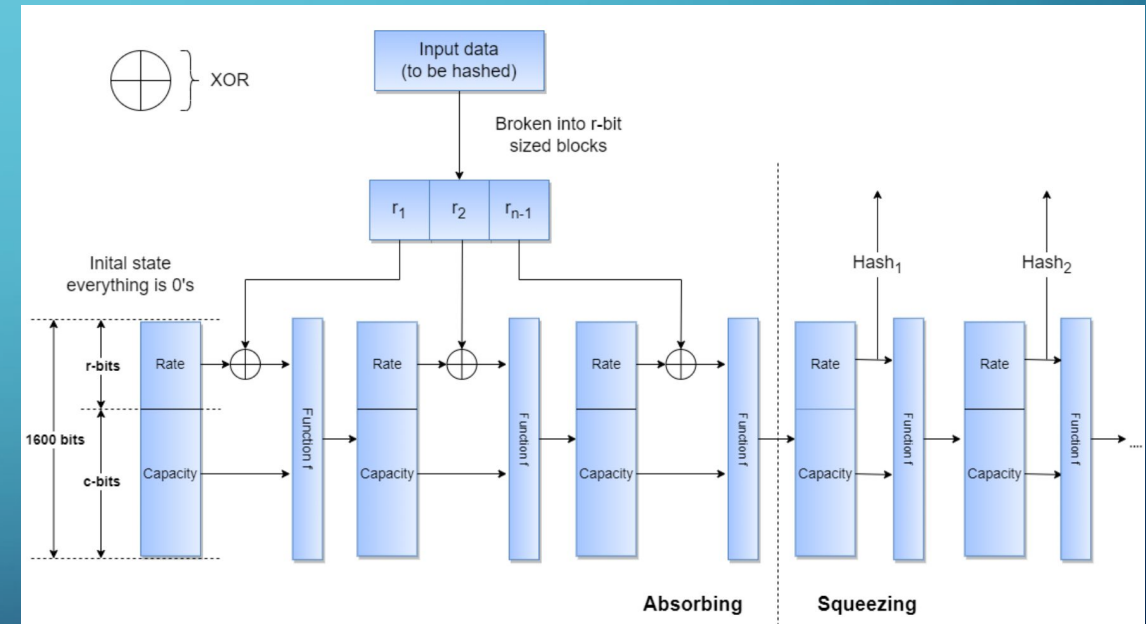
- Input data is divided into  $r$ -bit blocks
- Each block is processed in XOR operation into the rate portion of the state
- The entire state is updated via the Keccak permutation function  $f$
- Repeated until all input blocks are absorbed



# ACCELERATED HASH COMPUTATIONS

## Squeezing Stage

- Output is extracted from the rate portion as Hash1, Hash2...
- If more output is needed, apply  $f$  again and extract more bits
- Continues until desired hash length is reached



# Keccak-f

24 rounds of 5 steps:

- Theta: mix bits within columns
- Rho: rotate bits within lanes
- Pi: rearrange lanes spatially
- Chi: non-linear substitution
- Iota: XOR round constant

```
1 # Theta
2 ``py
3 C[x] = A[x][0] ⊕ A[x][1] ⊕ A[x][2] ⊕ A[x][3] ⊕ A[x][4]
4 D[x] = C[x-1] ⊕ ROT(C[x+1], 1)
5 A[x][y] ← A[x][y] ⊕ D[x]
6 ``
7
8 # Rho
9 ``py
10 A[x][y] ← ROT(A[x][y], r[x][y])
11 ``
12
13 # Pi
14 ``py
15 A'[x][y] = A[(x + 3y) mod 5][x]
16 ``
17
18 # Chi
19 ``py
20 A[x][y] ← A[x][y] ⊕ ((¬A[x+1][y]) ∧ A[x+2][y])
21 ``
22
23 # Iota
24 ``py
25 A[0][0] ← A[0][0] ⊕ RC[round_index]
26 ``
```

```
-- pi
i3001: for y in 0 to 4 generate
  i3002: for x in 0 to 4 generate
    i3003: for i in 0 to 63 generate
      --pi_out(y)(x)(i) ≤ pi_in((y + 2*x) mod 5)((4*y)+x) mod 5)(i);
      pi_out((2*x+3*y) mod 5)(0*x+1*y)(i) ≤ pi_in(y)(x)(i);
    end generate;
  end generate;
end generate;
```



# PERFORMANCE COMPARISON & ANALYSIS

- **Bandwidth of the write:** sustained input with randomized file.
- **Latency of the algorithm:**
  - Theoretical performance comparison with synthesis / implementation reports (against other hardware-based implementation);
  - Realtime performance comparison with burst writes
- **Efficiency:** task-time power monitoring on both PS and PL
  - Combined with bandwidth, obtain H/s performance comparables



# Hardware Optimization Strategies

## Pipelining & Unrolling

- Implement a **two-stage pipelined architecture**: Theta ( $\theta$ ) step — high delay path, Rho, Pi, Chi, Iota — lower delay logic
- This division reduces the **critical path**, improving max clock frequency and trying to achieve an  $II = 1$ .
- Additional **inter-round pipeline registers** allow higher throughput, allowing to produce multiple hashes at once.
- Partial **loop unrolling** (e.g. factor of 2) using VHDL generate enables parallel round execution while balancing area usage
- These techniques follow the optimization approach from **Sideris et al. (2023)**

## Bitwise Logic Parallelism

- Keccak's XOR, AND, and rotation operations map efficiently to FPGA logic
- Minimal interdependencies between rounds allow concurrent evaluation
- Optimized datapaths reduce synthesis and timing pressure

## Static Input & RC Optimization

- Fixed 80-byte header simplifies control and eliminates runtime padding
- **Simplified 7-bit Round Constant (RC)** replaces full 64-bit table  
→ Reduces Iota step logic from 64 XORs to just 7 XORs

## AXI-Lite Control Integration

- Lightweight **memory-mapped interface** connects PL (hash core) to PS
- Enables runtime control: trigger hashing, retrieve results
- The nonce will be handled inside the VHDL core to improve hashing efficiency.

# PROJECT PLAN & TIMELINE

## **Week 7 - Research**

Review Bitcoin mining & Keccak-256 algorithm. Define scope, VHDL flow, assign roles.

## **Week 8 - VHDL Core**

Refine Keccak-256 miner core in VHDL for PL. Set up simulation and testbench.

## **Week 9 - System Integration**

Wrap core with AXI Interface (Lite), add PS logic, test hashing rounds.

## **Week 10 - Testing & Presentation**

Simulate full flow and present final results.



# RISKS & CONTINGENCIES

## Timing Closure Issues

- **Risk:** Pipelined Keccak core may not meet timing at target frequency
- **Contingency:** Reduce pipeline depth or unroll factor; adjust placement constraints

## Excessive Resource Usage

- **Risk:** Full unrolling or deep pipelining may exceed available slices/LUTs
- **Contingency:** Scale back unrolling; optimize datapath and control logic

## AXI-Lite Integration Bugs

- **Risk:** Communication failures between PS and PL (e.g., unresponsive core)
- **Contingency:** Use Vivado ILA to debug; validate AXI signals before full integration

## Incorrect Hash Output

- **Risk:** Hardware hash doesn't match Keccak reference output
- **Contingency:** Compare against NIST vectors; test round-by-round in simulation

# ROLES OF TEAM MEMBERS

**Felix** : Working on the Keccak core design, optimizing and documentation.

**Desmond** : Focusing on debugging the VHDL core for hashing and simulation testing.

**Jack** : Working on system integration, PS-PL coordination and hardware testing.

**Thenuja** : Contributing to optimization strategy, PS–PL coordination and documentation.

The background is a solid blue gradient. In the corners, there are decorative white line art elements resembling circuit boards or neural networks, with lines and small circles connecting them.

# THANK YOU!

## Q & A