

# COMP3601 Baseline Project Quickstart

## Overview

Every student will receive a baseline FPGA project package consisting of:

- Pre-flashed Petalinux image with configured software and example bitstreams on SD card
- Kria KV260 and power supply, ethernet cable, USB cable
- UNSW CSE Design Project A/B PMOD board
- Adafruit I2S MEMS microphone

This guide describes the steps for students to get started on the project.

## Prerequisites

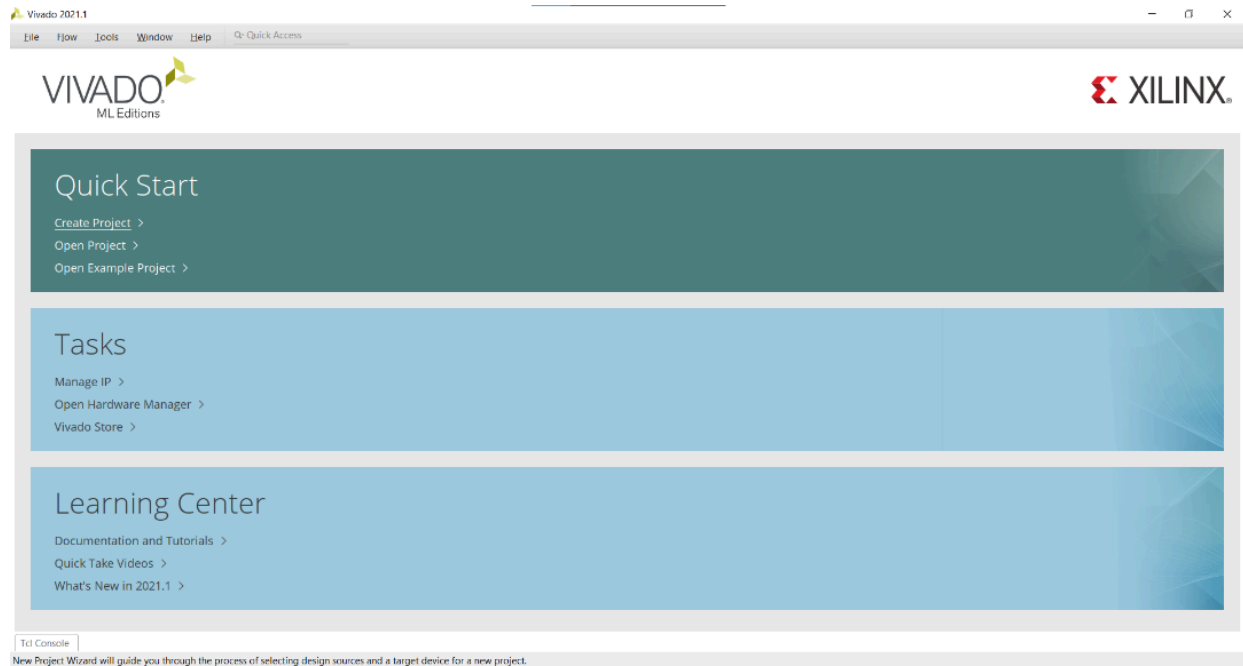
The software you should have installed before starting:

- Vitis Vivado 2021.1
    - During installation, you need to choose to install the full Vitis package as it will be needed later in this course.
  - If Ubuntu: minicom, if Windows: Putty
-

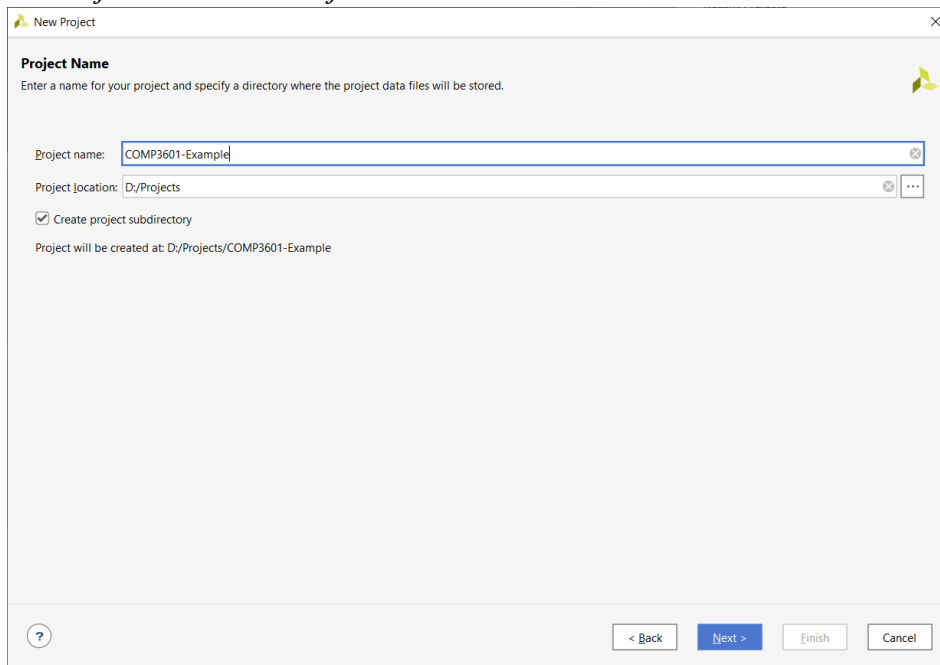
# Hardware Project Setup

## Creating a new project in Vivado

1. Open Vivado. Click on *Create Project* and click *Next*.

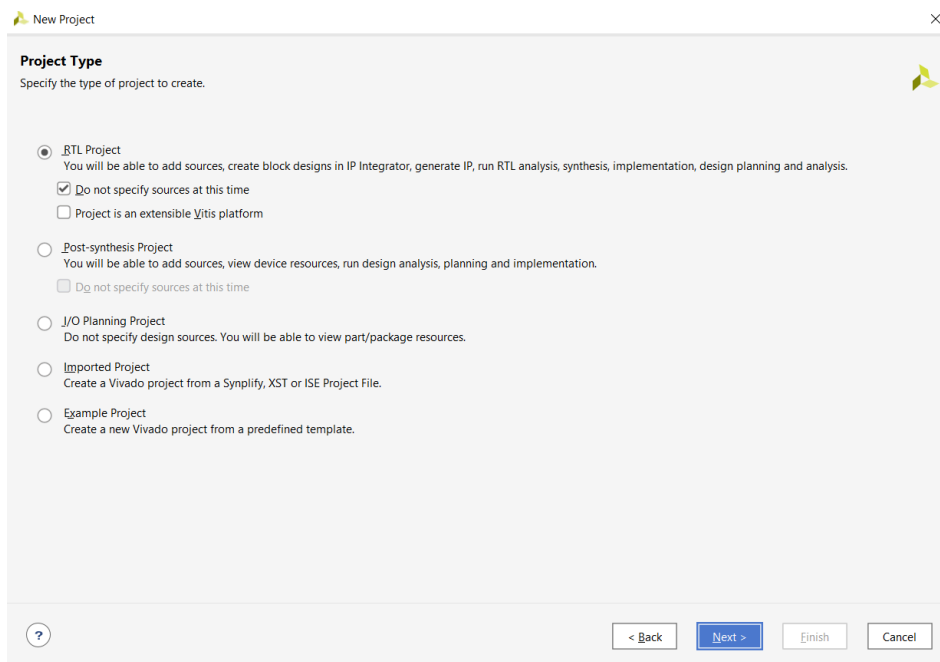


2. Set *Project name* and *Project location* and click *Next*.



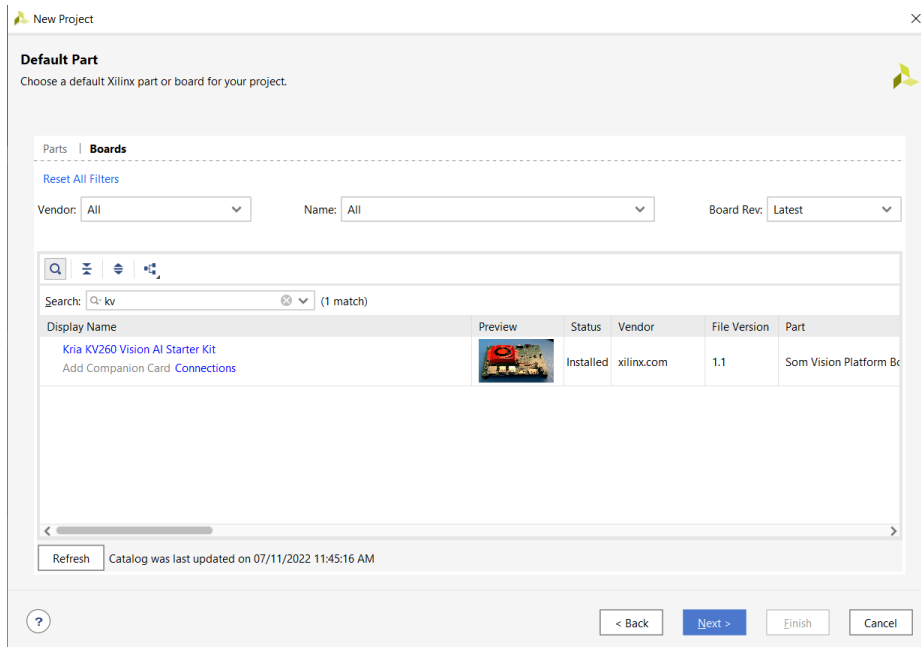
The screenshot shows the 'New Project' dialog box with the title bar 'New Project'. The main heading is 'Project Name'. Below it, a subtitle reads: 'Enter a name for your project and specify a directory where the project data files will be stored.' There are two input fields: 'Project name:' with the text 'COMP3601-Example' and 'Project location:' with the text 'D:/Projects'. Below these fields, there is a checked checkbox labeled 'Create project subdirectory' and a line of text stating 'Project will be created at: D:/Projects/COMP3601-Example'. At the bottom of the dialog, there are four buttons: '< Back' (disabled), 'Next >' (active/highlighted), 'Finish' (disabled), and 'Cancel' (disabled). A help icon (?) is located in the bottom left corner.

3. Select *RTL Project*. We will add the sources later so tick *Do not specify sources at this time*. Click *Next*.



The screenshot shows the 'New Project' dialog box with the title bar 'New Project'. The main heading is 'Project Type'. Below it, a subtitle reads: 'Specify the type of project to create.' There are five radio button options: 1. 'RTL Project' (selected): 'You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.' It has two sub-options: a checked checkbox 'Do not specify sources at this time' and an unchecked checkbox 'Project is an extensible Vitis platform'. 2. 'Post-synthesis Project': 'You will be able to add sources, view device resources, run design analysis, planning and implementation.' It has an unchecked checkbox 'Do not specify sources at this time'. 3. 'J/O Planning Project': 'Do not specify design sources. You will be able to view part/package resources.' 4. 'Imported Project': 'Create a Vivado project from a Synplify, XST or ISE Project File.' 5. 'Example Project': 'Create a new Vivado project from a predefined template.' At the bottom of the dialog, there are four buttons: '< Back' (disabled), 'Next >' (active/highlighted), 'Finish' (disabled), and 'Cancel' (disabled). A help icon (?) is located in the bottom left corner.

- In the *Default Part* section, click on the **Boards** tab and type "kv" in the search bar. Select **Kria KV260 Vision AI Starter Kit** and click *Next*.

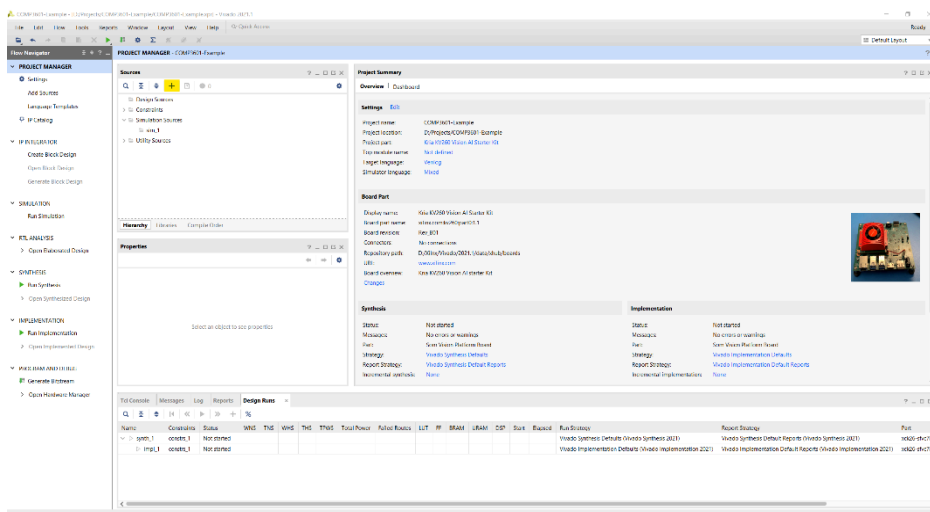


- Click *Finish* to create your project.

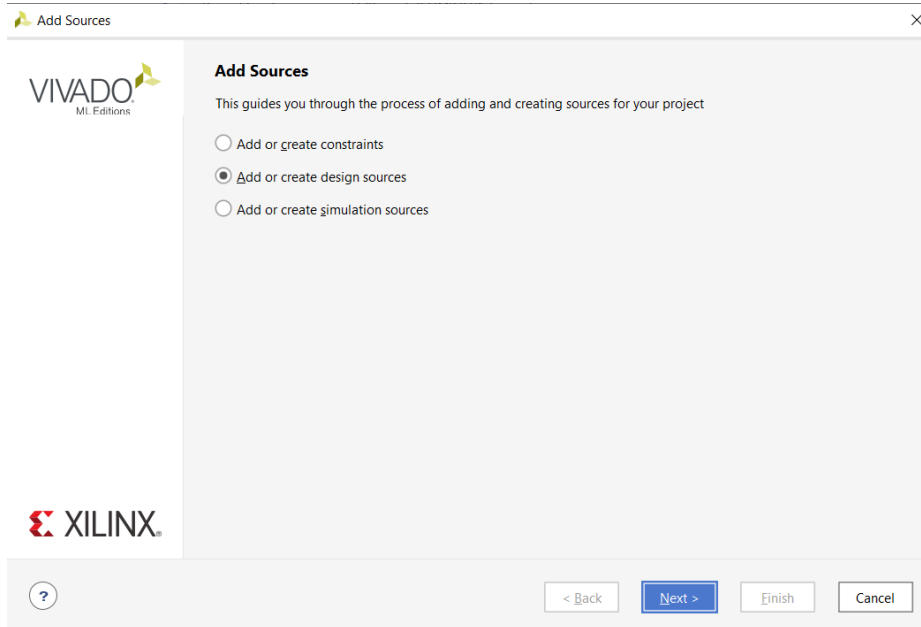
Make sure the *Project part* shows **Kria KV260 Vision AI Starter Kit**.

## Adding constraints to the project

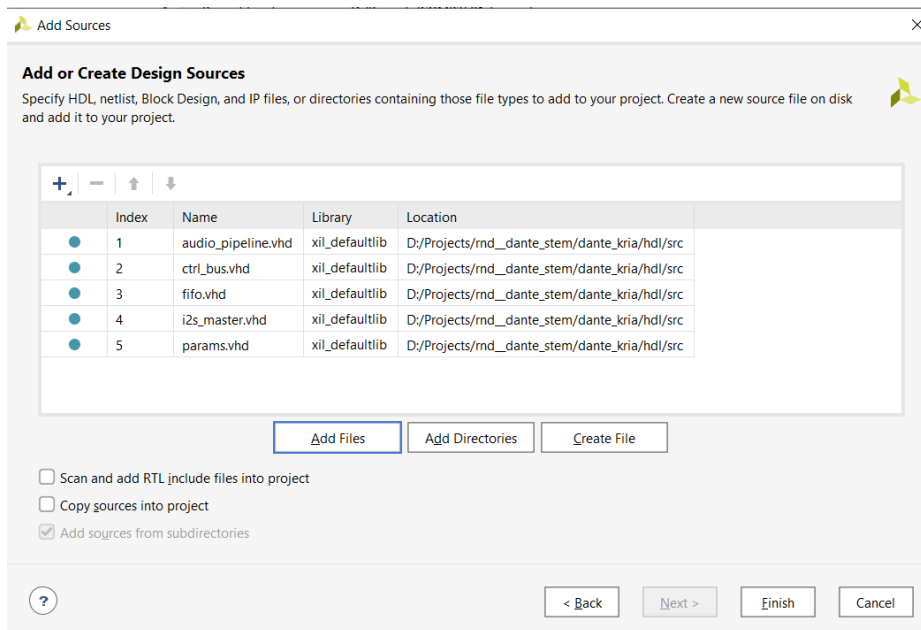
- In the *Project Manager*, click on + in the *Sources* window.



2. Select *Add or create design sources* and click *Next*.

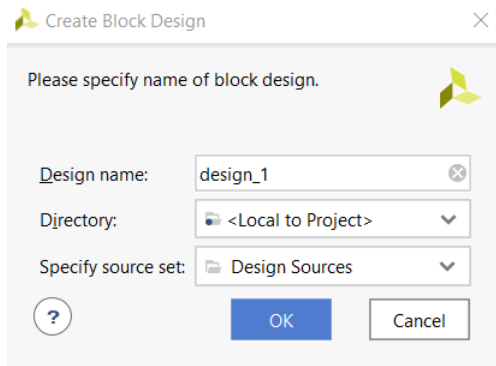


3. Add the HDL design files from Teams. Click *Finish* when done.
  1. Note: We provide i2s\_master.vhd and fifo.vhd files, but these are only skeletons. You'll need to finish them off!

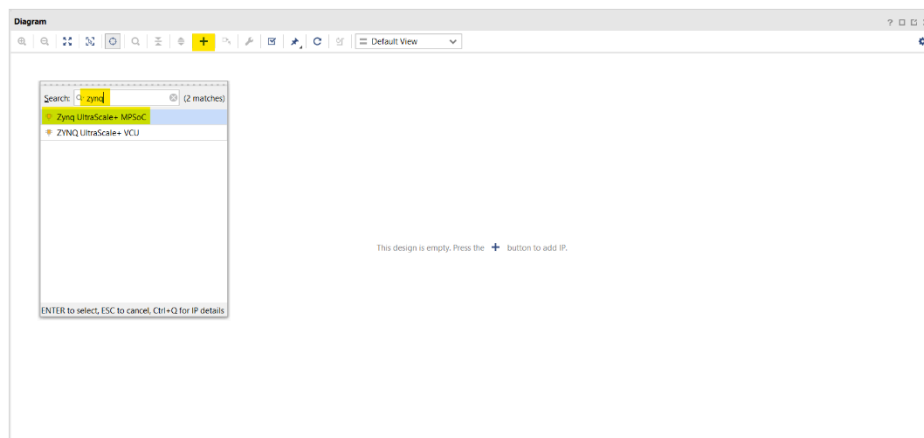


4. Add the constraint file for the Kria board into the project by choosing *Add or create constraints* in *Add sources*. Click *Finish* when done.

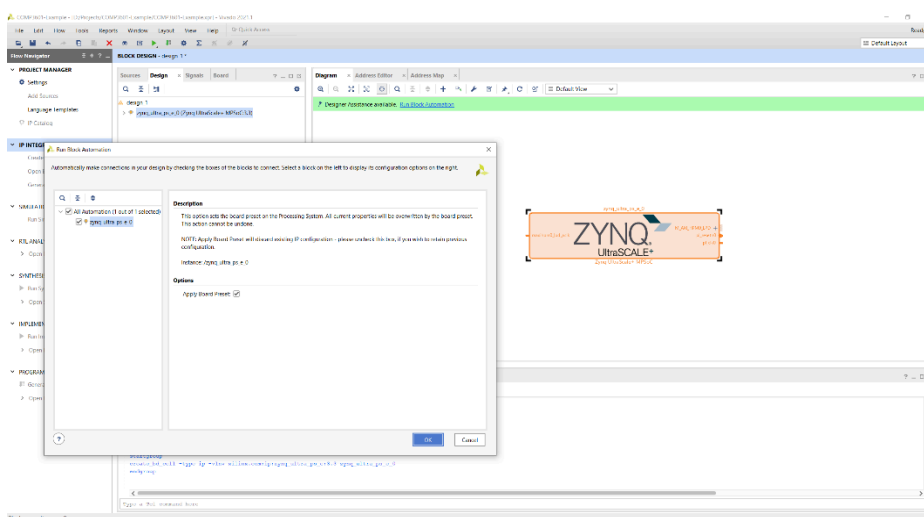




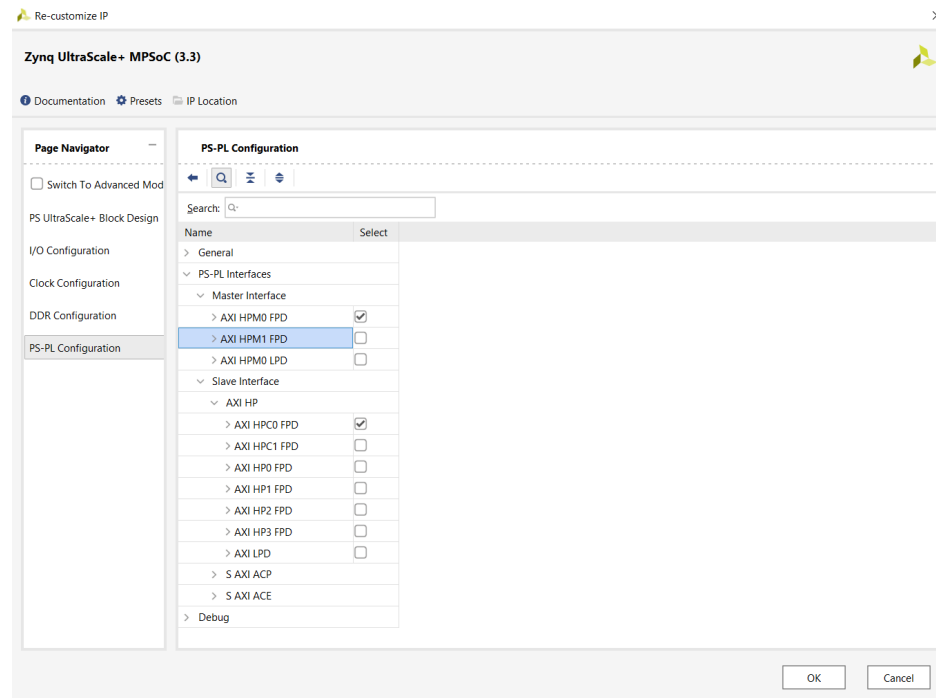
3. An empty *Diagram* should show up. Click on + and search for “zynq”. Double click on *Zynq UltraScale+ MPSoC* to add the IP into your block design.



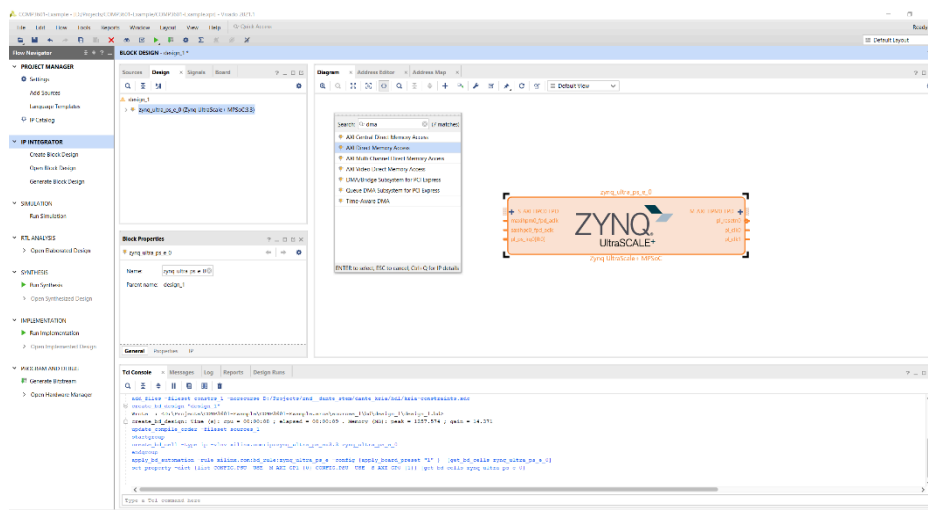
4. Click on *Run Block Automation* and click *OK* which will apply the Kria AI Starter Kit preset to the Zynq device.



5. Double click on the Zynq MPSoC IP and navigate to *PS-PL Configuration* → *PS-PL Interfaces* and do the following configurations:
  1. *Master Interface* → Untick *AXI HPM1 FPD*
  2. *Slave Interface* → Enable *AXI HPC0 FPD*

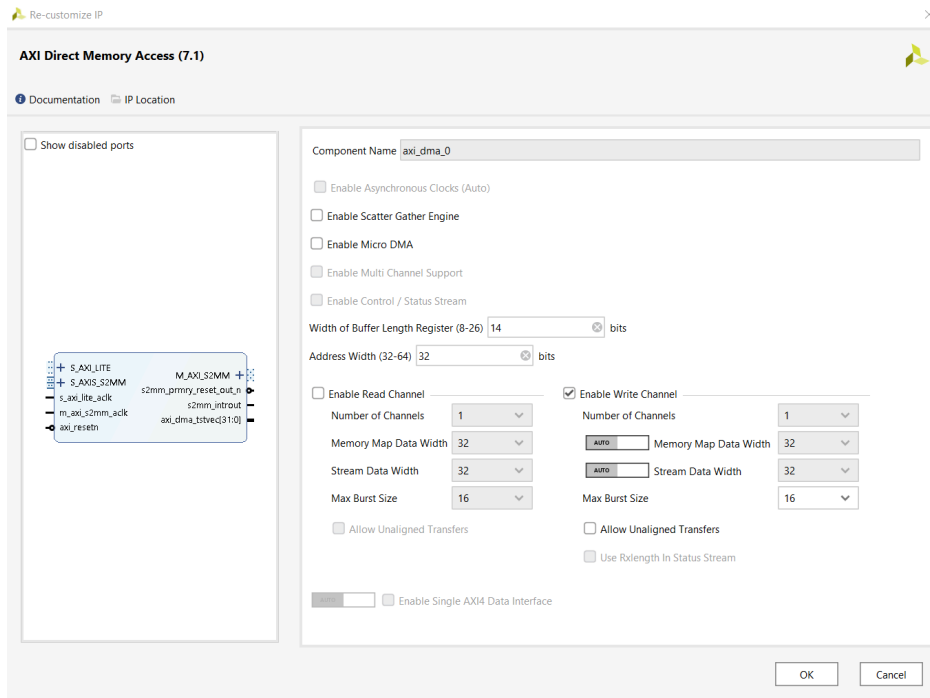


6. Click on +, search for “dma” and double click on *AXI Direct Memory Access* to add the IP into your block design.

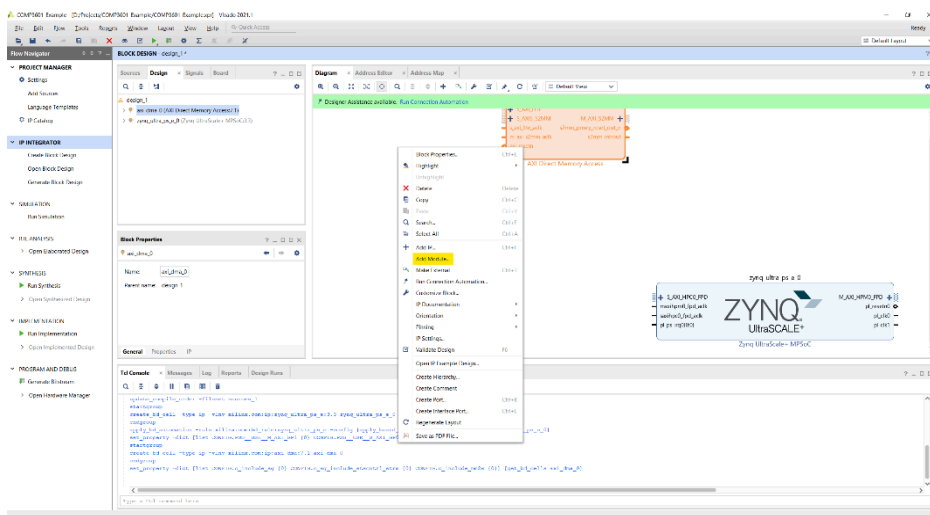


7. Double click on the DMA device and untick *Enable Scatter Gather Engine* and *Enable Read Channel*. Click *OK*.

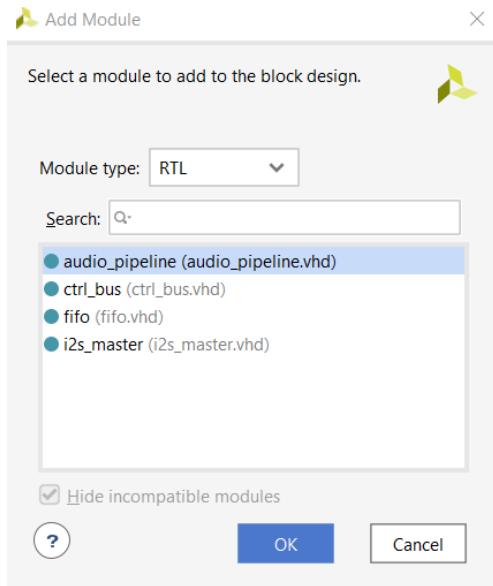




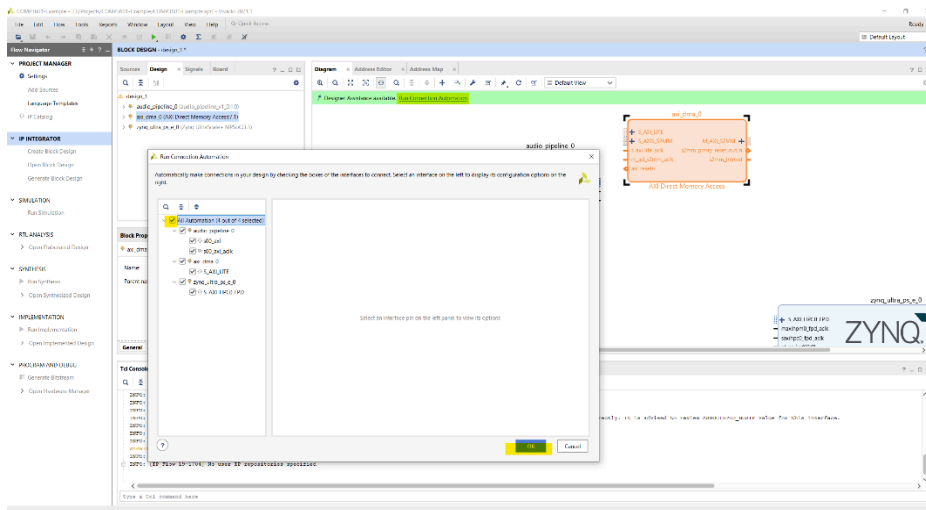
8. Right-click on the diagram and select *Add Module*.



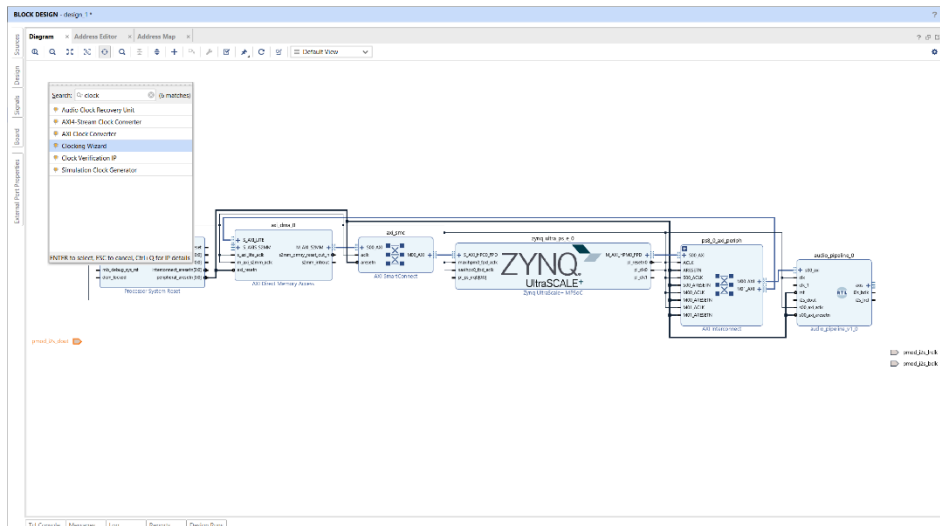
9. Select *audio\_pipeline* and click *OK*.



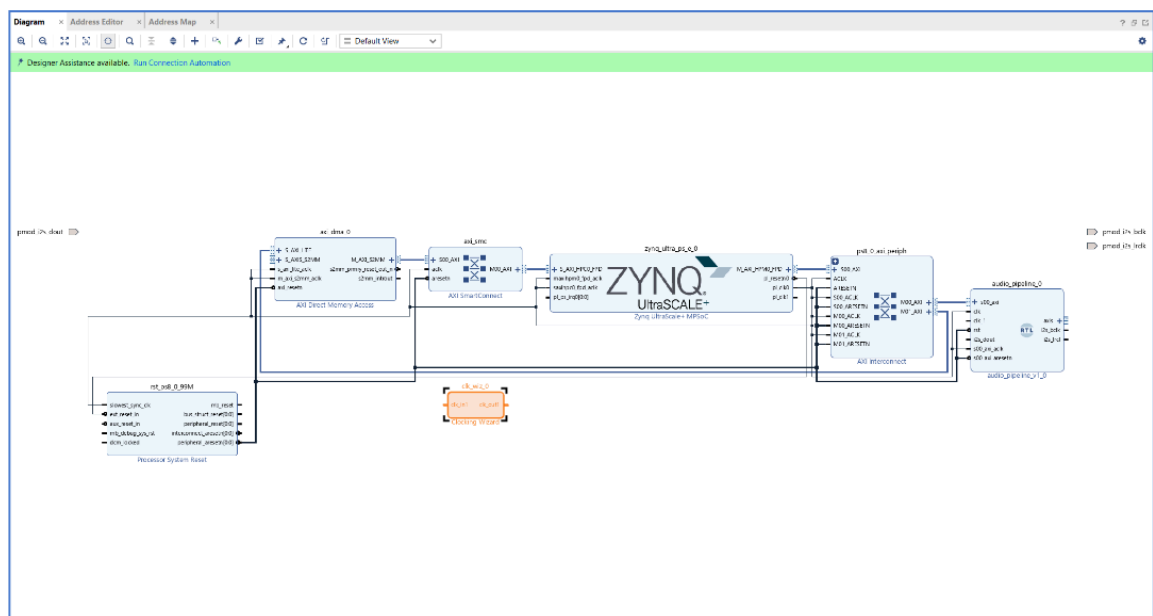
10. Click on *Run Connection Automation* and tick on all boxes to let the IP Integrator connect and add the required interconnect IPs between the HDL module and the Zynq device.



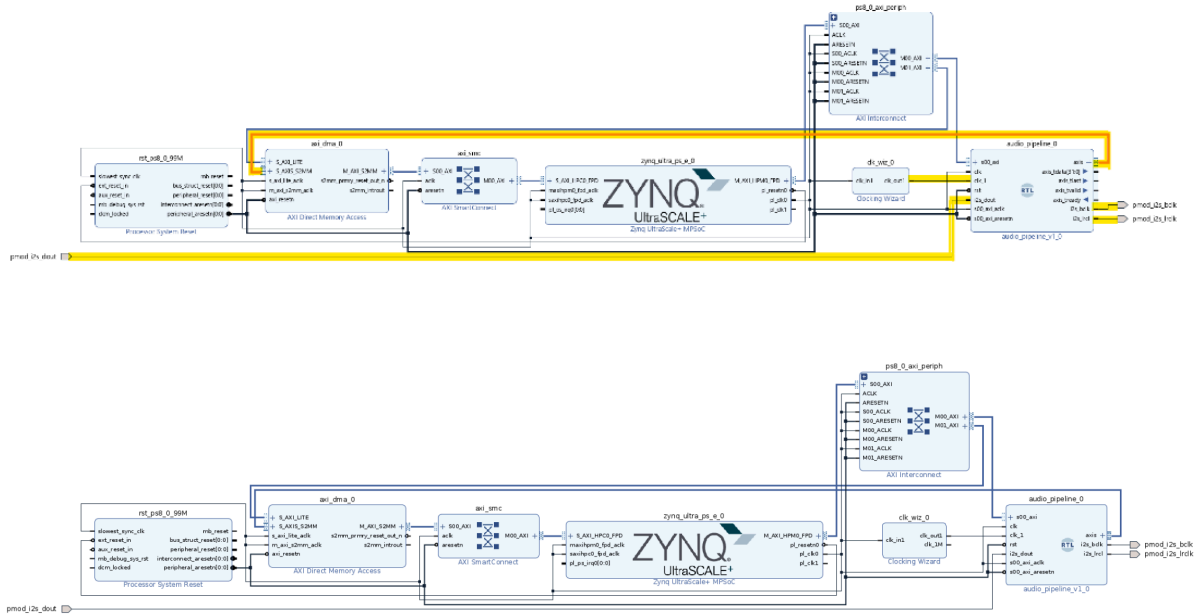
11. Right-click on the diagram and select *Create Port*. Add the following ports:
  1. pmod\_i2s\_lrcclk; *Output; Other*
  2. pmod\_i2s\_bclk; *Output; Other*
  3. pmod\_i2s\_dout; *Input; Other*
12. Click on + to add another IP and search for “clocking wizard”. Double click to add the IP to your block design.



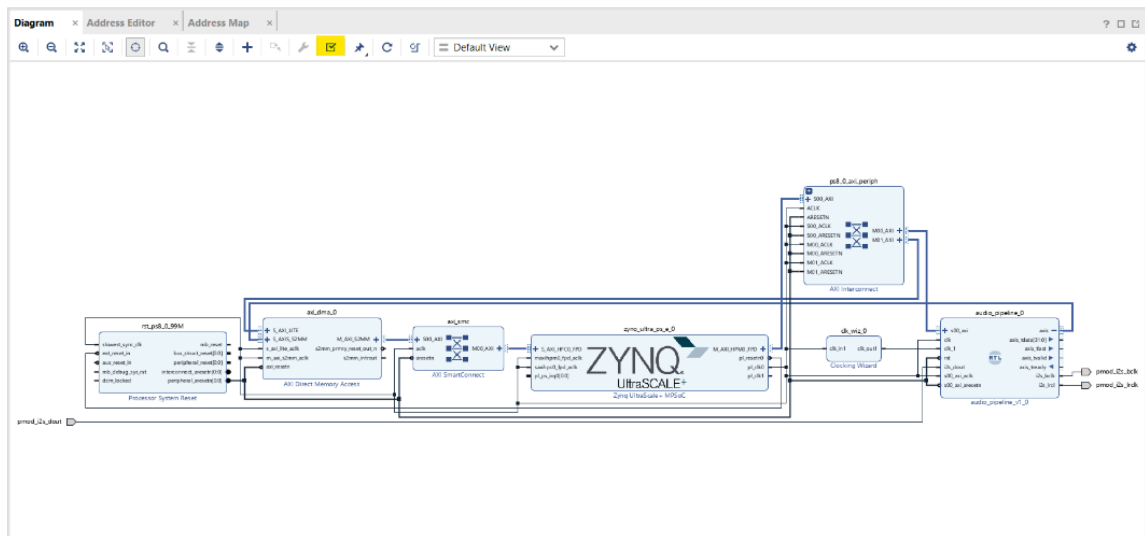
13. Double click on the clocking wizard IP and navigate to the *Output Clocks* tab.
  1. Set the *clk\_out1* clock to a requested **49.152MHz** frequency.
  2. Scroll down and under *Enable Optional Inputs / Outputs for MMCM/PLL* untick the *reset* and *locked* ports.
  3. Click *OK* to finish the configuration.
14. At this point your diagram should look like this:



15. Connect the ports on the audio\_pipeline\_0 IP to the corresponding pins which should look like the following diagram:



16. Validate the block design by clicking on the ticked-box icon.



17. Under the *Sources* tab, right-click on the design\_1.bd block design and click *Create HDL Wrapper*. Select *Let Vivado manage wrapper and auto-update* and click *OK*.

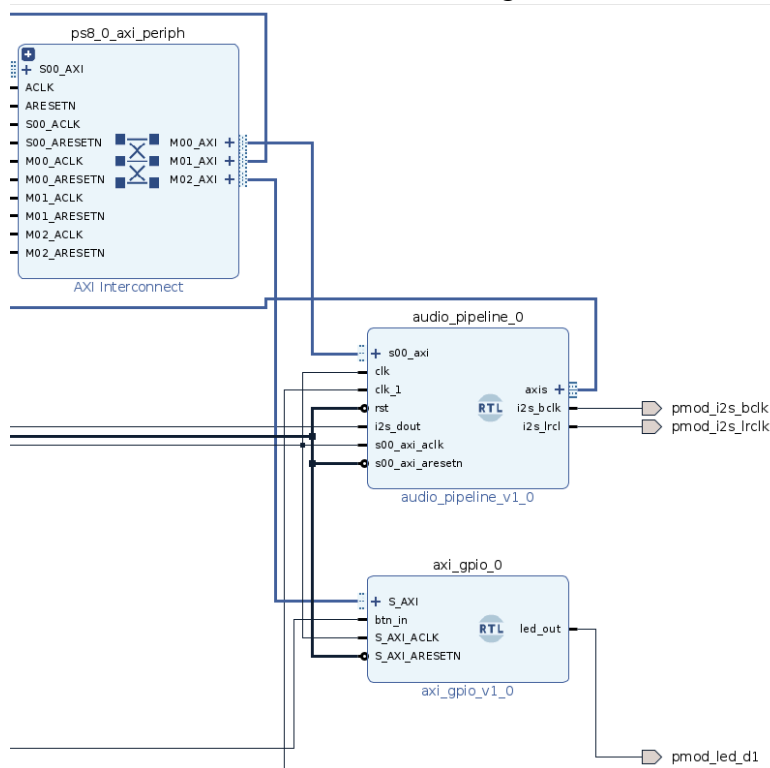
18. Go to the *Address Editor* tab and make sure that under Network 1, the /audio\_pipeline\_0/s00\_axi has address 0x00\_A001\_0000 and

/axi\_dma\_0/S\_AXI\_LITE has the address 0x00A000\_0000

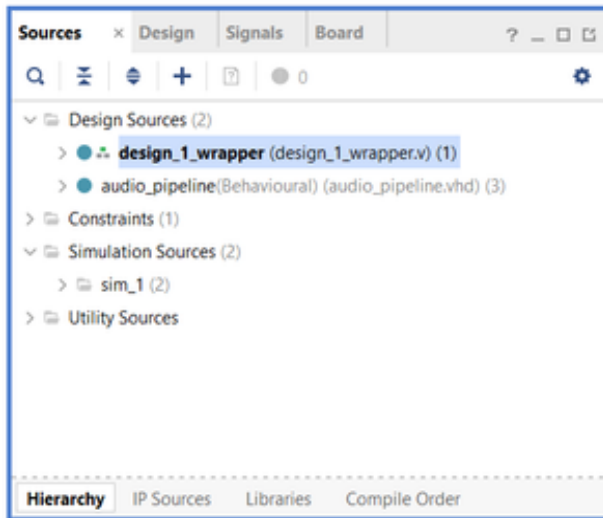
Name	Interface	Slave Segment	Master Base Address	Range	Master High Address
Network 0					
axi_dma_0					
axi_dma_0/Data_S2MM (32 address bits : 4G)					
/zynq_ultra_ps_e_0/SAXIGP0	S_AXI_HPC0_FPD	HPC0_QSPI	0xC000_0000	512M	0xDFFF_FFFF
/zynq_ultra_ps_e_0/SAXIGP0	S_AXI_HPC0_FPD	HPC0_DDR_LOW	0x0000_0000	2G	0x7FFF_FFFF
Excluded (2)					
/zynq_ultra_ps_e_0/SAXIGP0	S_AXI_HPC0_FPD	HPC0_DDR_HIGH			
/zynq_ultra_ps_e_0/SAXIGP0	S_AXI_HPC0_FPD	HPC0_LPS_OCM	0xFF00_0000	16M	0xFFFF_FFFF
Network 1					
/zynq_ultra_ps_e_0					
/zynq_ultra_ps_e_0/Data (39 address bits : 0x00A0000000 [ 256M ], 0x0400000000 [ 4G ], 0x1000000000 [ 224G ])					
/audio_pipeline_0/s00_axi	s00_axi	reg0	0x00_A001_0000	64K	0x00_A001_FFFF
/axi_dma_0/S_AXI_LITE	S_AXI_LITE	Reg	0x00_A000_0000	64K	0x00_A000_FFFF

19. Note: If you want to integrate your button and LED from M2, you can also do that.

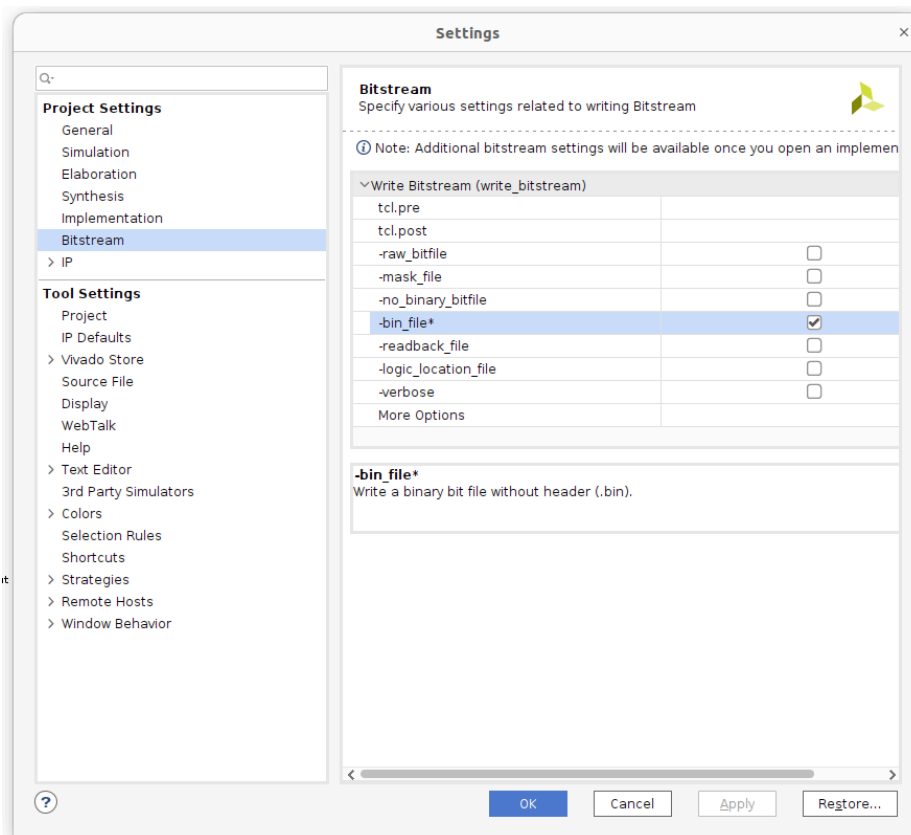
1. They should have the address 0x00\_A002\_0000
2. Add another “Master interface” to the AXI interconnect
3. Join the new Master port to the port on your axi\_gpio module
4. It should look something like this:



20. Right-click on the *design\_1\_wrapper* and click on *Set as Top*. Now the *design\_1\_wrapper* should be bold and on the top in *Design Sources*.



21. On the *Flow Navigator* tab, click on *Settings* under the *PROJECT MANAGER*. If you want the HDL wrapper you created to be in VHDL set the *Target Language* to VHDL. In *Bitstream*, enable `-bin_file` so that generating bitstream will give you a .bin version of the bitstream which will be needed for the Kria board (for advanced projects).



20. Note that you can try include your LED blinking code module as well, and add another clock output from the clocking wizard...

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## Building the project

1. Remember it won't actually work until you've finished the i2s\_master.vhd file and the fifo.vhd file.
2. In the *Flow Navigator* window, click on *Run Synthesis* and launch the synthesis tasks.
3. Once the synthesis has been completed, click on *Run Implementation* to run implementation tasks.
4. Once the implementation has been completed, click on *Generate Bitstream* to generate the .bit and .bin bitstream files. (The files will be located at <vivado-project-location>/design\_1.runs/impl1/ under the name design\_1\_wrapper.bit and design\_1\_wrapper.bin)
5. Click on *File* → *Export* → *Export Hardware*. Click *Next* and select *Include bitstream*. Set the xsa filename and choose your location to export the file to. Click *Next* and click *Finish* to complete your export.

## Running custom AXI hardware on Kria

1. Using the instructions from earlier, first “activate” the built-in AXI image using `xmutil unloadapp && xmutil loadapp comp3601-i2s-axi` via the serial port.
  - a. The LED should start blinking to indicate the app is loaded.
2. Do not unload this app before proceeding!
3. You will **always** need to do this before proceeding as the comp3601-i2s-axi sets up both a memory map for the session *and* a placeholder FPGA bitstream.
4. We will then replace the FPGA bitstream, but not the memory map, with vivado's hardware manager.
5. Open the Hardware Manager and download your code following the steps in labs 1/2.

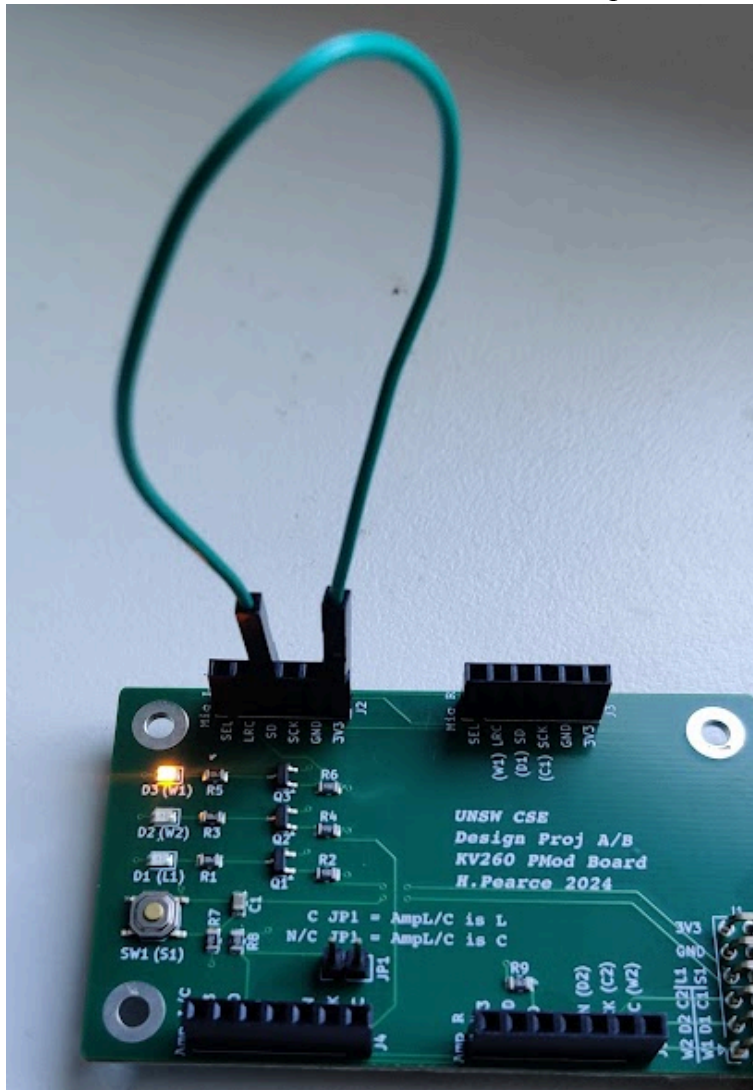
## Testing your custom AXI hardware on the Kria

1. Run the software code. We provide two binaries which you can use for debugging:
  1. These are found at /comp3601/resources/sample\_bin on the Kria

```
root@xilinx-k26-starterkit-2021_1:/comp3601/resources/sample_bin# ls
ctrl_bus_test  sample256
```

2. The sample256 binary will transfer 256 samples for each transaction and performs 10 transfers in total.

3. The `ctrl_bus_test` binary interfaces with the control bus of the module and tries to write `0xdeadbeef` to all the registers. Read-only registers will not be overwritten.
2. You can test your hardware by using the `sample256` application
  1. Run `chmod +x sample256` to make the program executable
    1. (First use only)
    2. Run `./sample256`
3. It will print a long series of numbers which reflect the values captured from the data input of the microphone
  1. You can do a simple test using a wire
  2. Connect SD to 3V3 and run `sample256` - all captures should be 1s



3. e.g.

Frame 9:

```

11111111 11111111 11111011 11011100 -> [3831]: 3ffff (100p)
11111111 11111111 11000111 11011100 -> [3832]: 3ffff (100p)
11111111 11111111 11100111 11011100 -> [3833]: 3ffff (100p)
11111111 11111111 11010111 11011100 -> [3834]: 3ffff (100p)

```

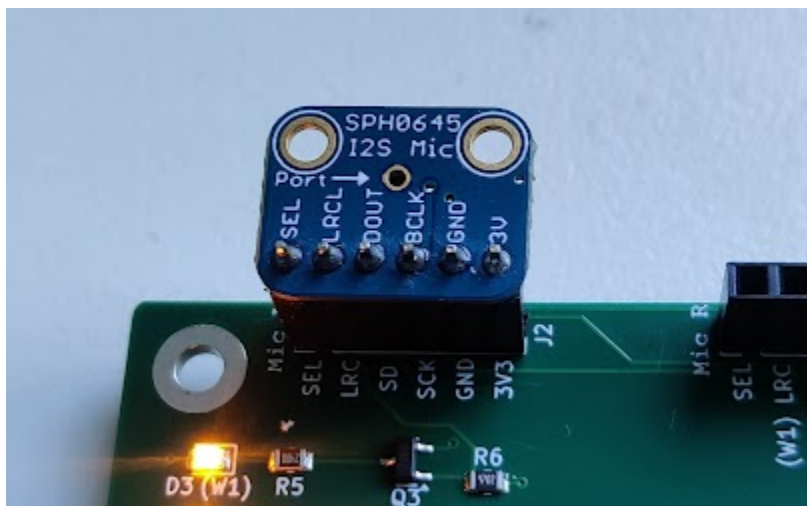


- Now repeat, but connect SD to GND - all captures should now be 0s

Frame 9:

```
00000000 00000000 00100100 11101001 -> [9673]: 00 (0p)
00000000 00000000 00010100 11101001 -> [9674]: 00 (0p)
00000000 00000000 00110100 11101001 -> [9675]: 00 (0p)
00000000 00000000 00001100 11101001 -> [9676]: 00 (0p)
```

- Now repeat, but plug the microphone in - all captures should be “random” values (actually the snapshots of audio at the instant the program ran).



Frame 9:

```
10001101 01001111 10010101 10001001 -> [9322]: 1f2b1 (48p)
00000000 00000000 00110101 10001001 -> [9323]: 00 (0p)
01110101 01001111 10001101 10001001 -> [9324]: 1f2ae (48p)
00000000 00000000 00101101 10001001 -> [9325]: 00 (0p)
01110101 01001111 10011101 10001001 -> [9326]: 1f2ae (48p)
```

You're now ready to continue developing the project on your own! Investigate writing software to replicate the sample256 program, and then try and save that to audio .wav files!

We provide some sample code (incomplete) at /comp3601/resources/app on the FPGA image. The image is set up for you to be able to develop on it directly (self-hosted) using gcc, or you can program your PC and download the programs using Vitis.

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## Appendix: Generating device tree overlay files for the custom HW modules

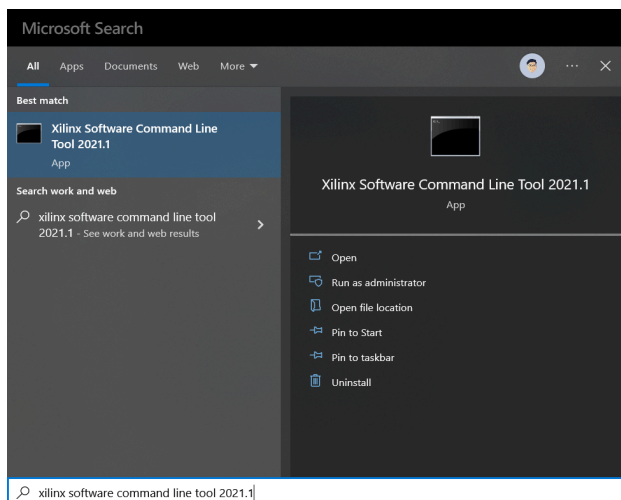
Up to this point we have had you using a pre-defined interface in the comp3601-i2s-axi module. However, this only defines three memory mapped components (the AXI stream, the AXI audio controller, and the AXI gpio button and LED). If you want to define further components or customize the map, these instructions describe what to do:

For the Petalinux image to recognise the interfaces between the Zynq MPSoC and PL hardware, we need device tree overlays to describe the interfaces.

1. Obtain the DTG tool from Xilinx's repo  

```
git clone https://github.com/Xilinx/device-tree-xlnx
cd device-tree-xlnx
git checkout xlnx_rel_v2021.1
```
2. Obtain the DTC tool if not obtained:  

```
sudo apt install dtc
# or
git clone https://git.kernel.org/pub/scm/utils/dtc/dtc.git
cd dtc
make
export PATH=$PATH:/<path-to-dtc>/dtc
```
3. In Windows, click Start and search for "Xilinx Command Line Tool 2021.1".



On Ubuntu, you will source the settings.sh file from your Vivado install directory then open xsct, e.g

```
$ source /tools/Xilinx/Vivado/2021.1/settings64.sh
$ xsct
```

4. Change the directory to the location where the exported XSA file is located. (using PowerShell/Linux commands E.g. ls, pwd, cd)

5. Run the following commands to generate the device tree file for the module which will generate the DTS file (human readable)

```
hsi open_hw_design <design_name.xsa>
hsi set_repo_path <path to device-tree-xlnx repository>
hsi create_sw_design device-tree -os device_tree -proc psu_cortexa53_0
hsi set_property CONFIG.dt_overlay true [hsi::get_os]
hsi generate_target -dir my_dts
hsi close_hw_design [current_hw_design]
```

6. (On windows) Open a WSL terminal, navigate to the location of the `my_dts` directory generated from the previous step and compile the `.dtsi` file into `.dtbo` using DTC (wsl); on Ubuntu just navigate to the right directory and ensure that `dtc` is on your PATH.

7. 

```
cd <path-to>/my_dts
dtc -@ -O dtb -o pl.dtbo pl.dtsi
```

At this point, you have generated the two files needed to run your custom hardware module on the Kria board, including:

- **pl.dtbo** located at `<path-to-vivado-project>/my_dts/pl.dtbo`
- **design\_1\_wrapper.bin** at `<path-to-vivado-project>/design_1.runs/impl1/design_1_wrapper.bin`

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## Running custom hardware on Kria

### Loading the firmware to Kria

Once the above steps are completed, you should have the `pl.dtbo` and `design_1_wrapper.bin` files ready.

1. `scp` these files to the `/lib/firmware/xilinx/<your-app-name>/` directory on the kria board with the naming convention of `<your-app-name>.dtbo` and `<your-app-name>.bit.bin`.
2. Create a `shell.json` file in the `/lib/firmware/xilinx/<your-app-name>/` directory. Paste the following snippet into the `shell.json` file.

```
{
    "shell_type": "XRT_FLAT",
    "num_slots": "1"
}
```

With the app name of `audio-i2s-dbg`, `/lib/firmware/xilinx/audio-i2s-dbg` should look like this:

```
xilinx-k26-starterkit-2021_1:~$ tree /lib/firmware/xilinx/audio-i2s-dbg
/lib/firmware/xilinx/audio-i2s-dbg
|-- audio-i2s-dbg.bit.bin
|-- audio-i2s-dbg.dtbo
`-- shell.json
```

```
0 directories, 3 files
```

### Loading the module onto the FPGA

4. Run `xmutil listapps` to list out the available hardware (your list may differ)

```
xilinx-k26-starterkit-2021_1:/home/petalinux# xmutil listapps
```

Type	#slots	Accelerator Active_slot	Base
		audio-i2s-dbg	audio-i2s-dbg
XRT_FLAT	0	-1	
		audio-i2s	audio-i2s
XRT_FLAT	0	-1	
		kv260-dp	kv260-dp
XRT_FLAT	0	0,	

Socket 9 closed by client

5. **Unload the default kv260-dp app with** `xmutil unloadapp`.

```
xilinx-k26-starterkit-2021_1:/home/petalinux# xmutil unloadapp
DFX-MGRD> daemon removing accel at slot 0
```

```
DFX-MGRD> Removing accel kv260-dp from slot 0
```

```
Accelerator successfully removed.
Socket 9 closed by client
```

6. **Assuming that audio-i2s-dbg is the name of your project, you then load the audio-i2s-dbg app with** `xmutil loadapp audio-i2s-dbg`

```
xilinx-k26-starterkit-2021_1:/home/petalinux# xmutil loadapp
audio-i2s-dbg
DFX-MGRD> daemon loading accel audio-i2s-dbg
```

```
DFX-MGRD> Successfully loaded base design.
```

```
Accelerator loaded to slot 0
Socket 6 closed by client
```

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## Appendix: writing software: Environment Setup

What you'll need:

- sdk.sh: SDK for cross-compilation.

1. Install the SDK by running the self-extracting .sh file. You can download this from Teams.

```
$ ./sdk.sh
PetaLinux SDK installer version 2021.1
=====
Enter target directory for SDK (default: /opt/petalinux/2021.1): <>
You are about to install the SDK to "/data/opt/petalinux". Proceed [Y/n]?
Y
Extracting
SDK.....
.....
.....done
Setting it up...done
SDK has been successfully set up and is ready to be used.
Each time you wish to use the SDK in a new shell session, you need to
source the environment setup script e.g.
$ .
/data/opt/petalinux/environment-setup-cortexa72-cortexa53-xilinx-linux
```

2. Once the SDK is installed, on every new terminal that you wish to build software for the Kria board, run the following command to set the cross-compilation environment.

```
.
<path-to-SDK-installation>/environment-setup-cortexa72-cortexa53-xilinx-l
inux
```

3. Check if the environment is set with `echo $CC`. The following output means the cross-compilation environment has been successfully set.

```
aarch64-xilinx-linux-gcc -mcpu=cortex-a72.cortex-a53 -march=armv8-a+crc
-fstack-protector-strong -D_FORTIFY_SOURCE=2 -Wformat -Wformat-security
-Werror=format-security
--sysroot=/data/opt/petalinux/sysroots/cortexa72-cortexa53-xilinx-linux
```

4. In the software example code, run `make` and transfer the binary to the Kria board (e.g. using a USB drive or `scp` command) and run with the hardware module loaded.
5. Use the code in `app/src` on Teams. Read what has been provided to you, understand it, and then your first step should be to try to replicate the functionality of the `sample256` example program.
6. For the basic requirements, you must save sampled audio as a `.wav` file.