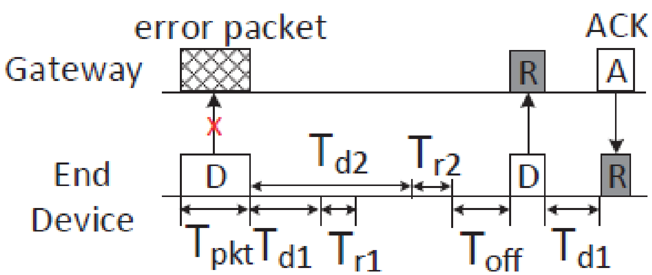
LiteNap: Downclocking LoRa Reception [INFOCOM 20]

Xianjin Xia, Yuanqing Zheng and Tao Gu

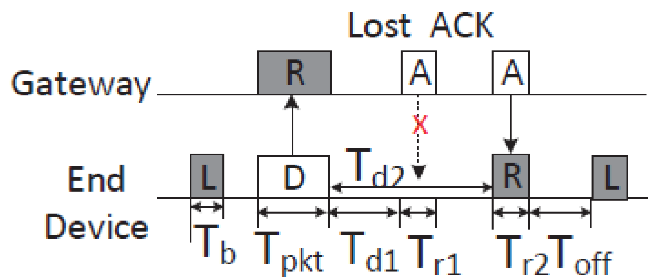
The Hong Kong Polytechnic, RMIT University

Motivation

- Improving energy efficiency in LoRaWAN
  - Duty cycle



(a) LoRaWAN Class A.



(b) LoRaWAN Class B.

- Reducing clock-rate can also reduce energy consumption

Modes		Enabled Components	Current Draw
Active	Transmit	MCU + TX Chains	20∼120 mA*
	Receive	MCU + RX Chains	11.5 mA
	Standby	MCU (disabled RF & PLL)	1.6∼1.8 mA
Sleep		Circuit	0.2∼1.5 μA

*The current draw varies with respect to the transmission power of 7∼20 dBm.

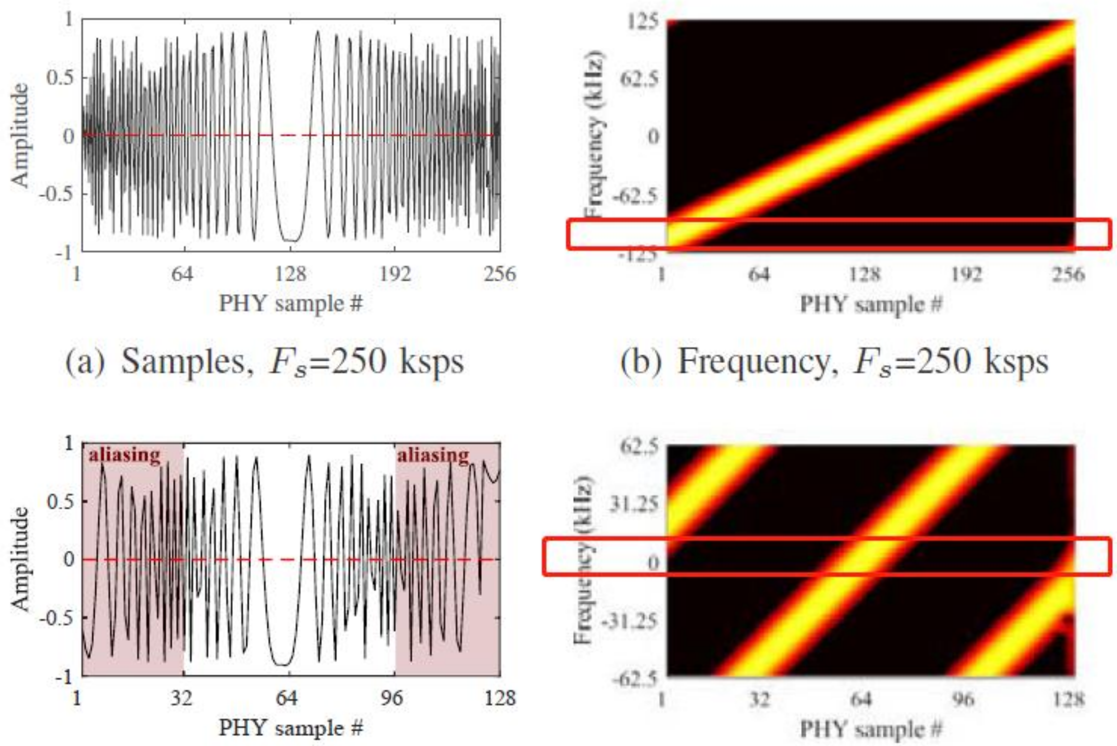
supply voltage

Power consumption ← $P \propto V^2 f$ → **Clock-rate(MCU/ADC)**

  - **High SER. Due to** Nyquist sampling theorem

Issues when reducing sampling rate

- ❑ **Frequency is changed when reducing sampling rate**
  - **SF=8, BW=250kHz。Fs=250kHz. (-125k~125k)**
  - **Symbol 0(-125kHz) -> Symbol 127 (0Hz)，Fs=125k**

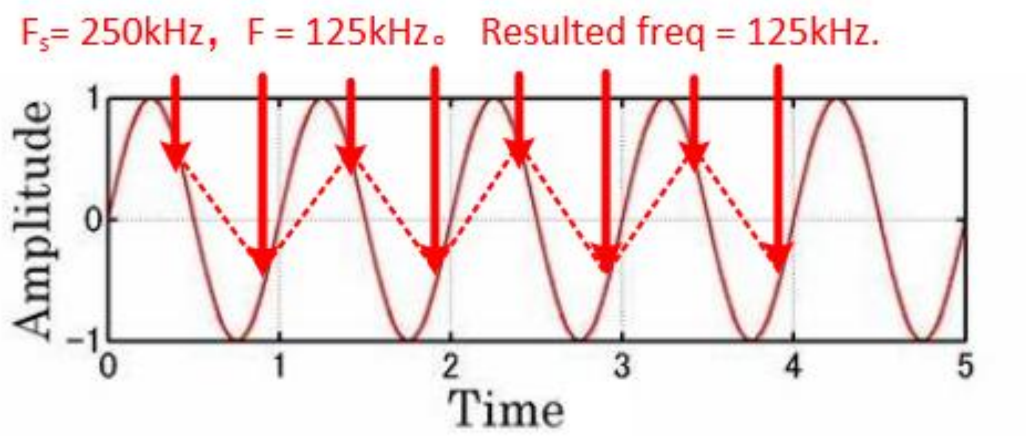


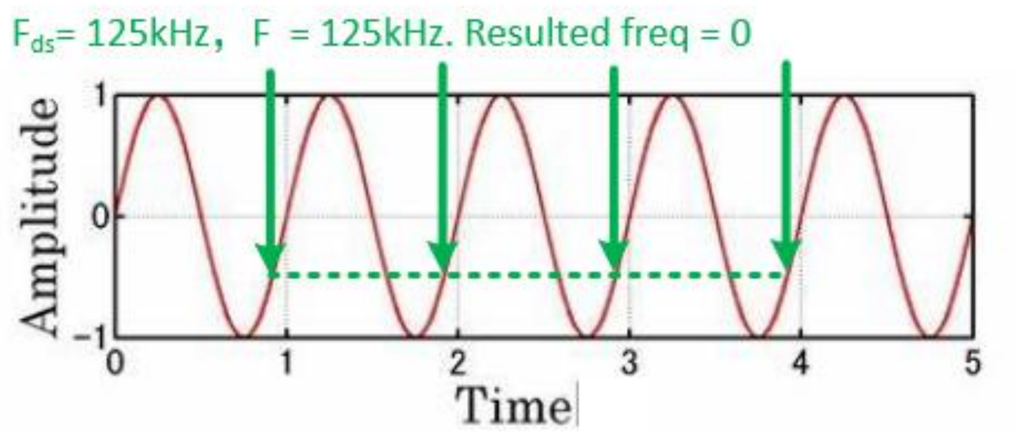
(a) Samples, F_s=250 ksps (b) Frequency, F_s=250 ksps

(c) Samples, F_s=125 ksps (d) Frequency, F_s=125 ksps

Issues when reducing sampling rate

- Specific example for the first frequency in chirp.
  - Target=125k
  - Fs=250k
  - Fds=125k

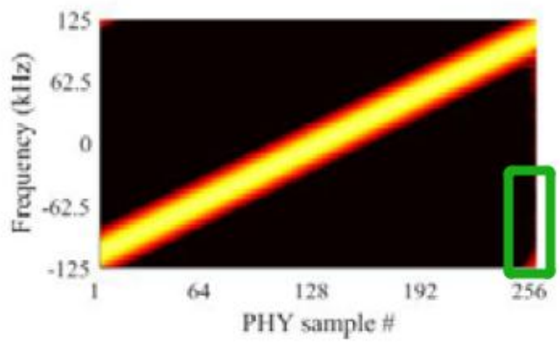




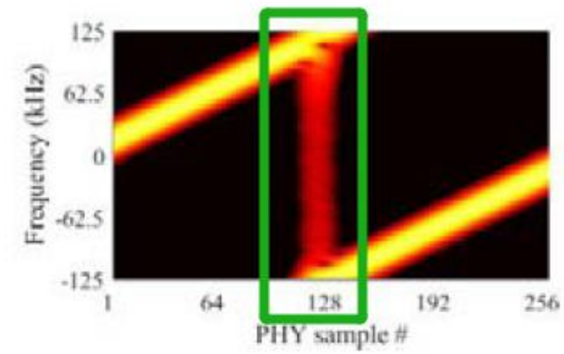
- **Problem:**
  - ***How to resolve the ambiguity caused by frequency aliasing due to undersampling***

Observation

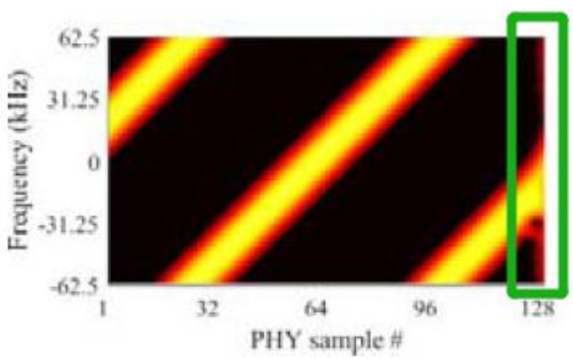
- **Frequency leakage when frequency suddenly changes from its maximum to minimum**
  - **Symbol#0. (a)at 256, (c) at 128 has leakage**
  - **Symbol#127. (b) at 128, (d) at 64 has leakage**



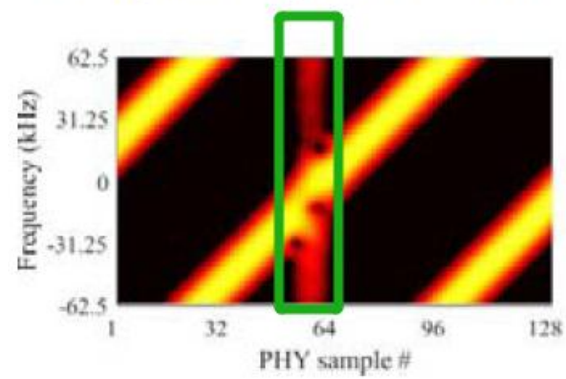
(a) Original chirp of symbol #0



(b) Original chirp of symbol #127



(c) Aliased chirp of symbol #0

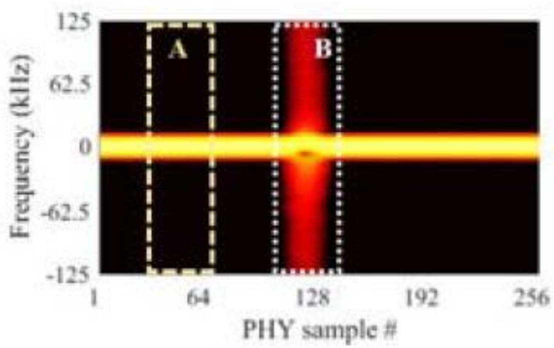


(d) Aliased chirp of symbol #127

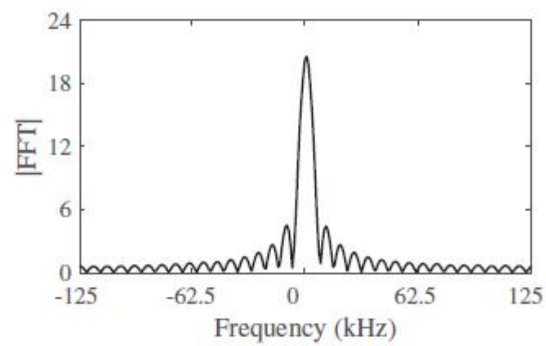
Approach one-frequency based

- **Key idea:**
  - **Detecting the leakage offset**
  - **Mapping the offset to the real symbol.**

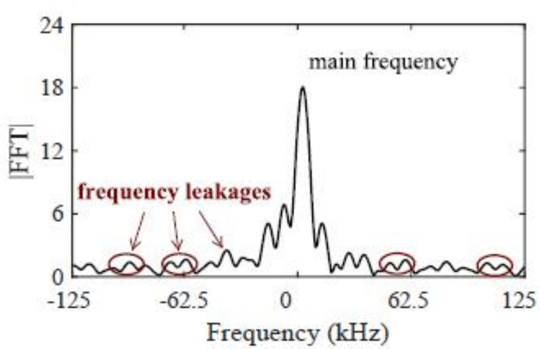
The original SF and BW are known. And down-clock to save energy.



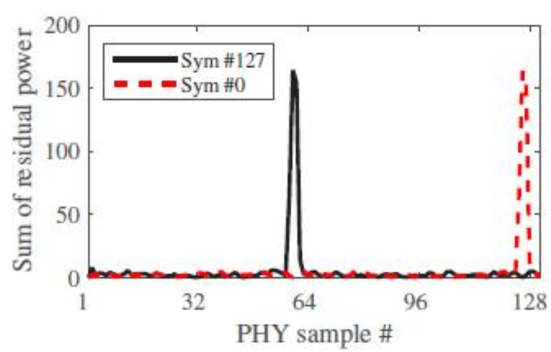
(a) Dechirped signal, F_s=250 ksps



(b) FFT of window A



(c) FFT of window B



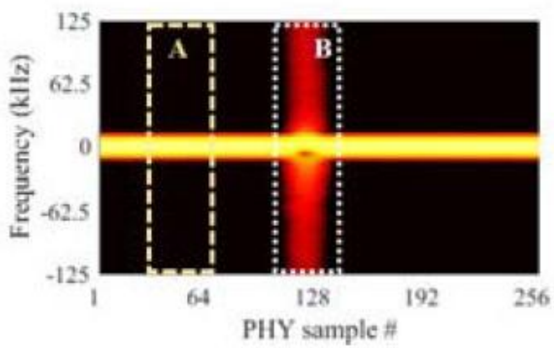
(d) Detected Loc. of freq. leakage

1. Moving window.
2. Difference of adjacent FFT.
3. Sum all the amplitude.

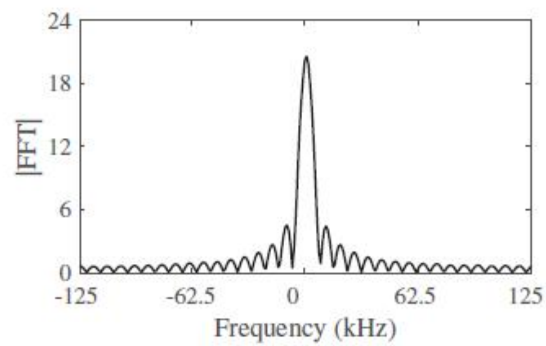
Approach one-frequency based

- **Key idea:**
  - **Detecting the leakage offset**
  - **Mapping the offset to the real symbol.**

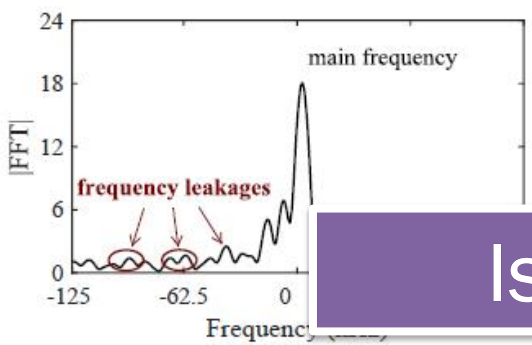
The original SF and BW are known. And down-clock to save energy.

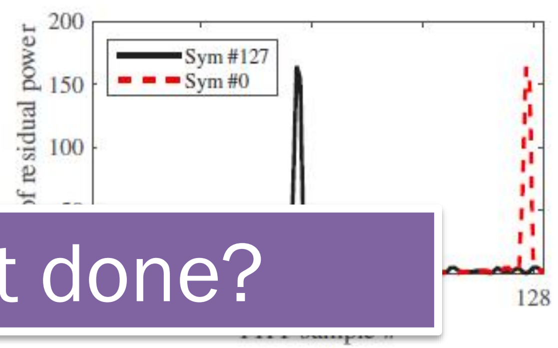


(a) Dechirped signal, F_s=250 ksps



(b) FFT of window A





Is it done?

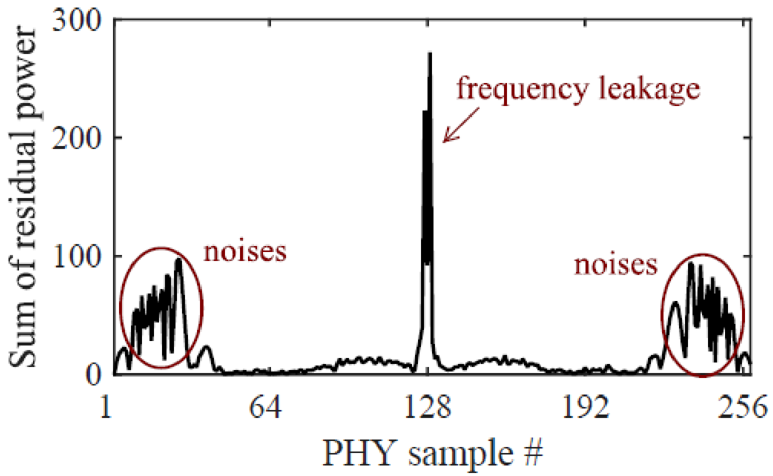
(c) FFT of window B

(d) Detected Loc. of freq. leakage

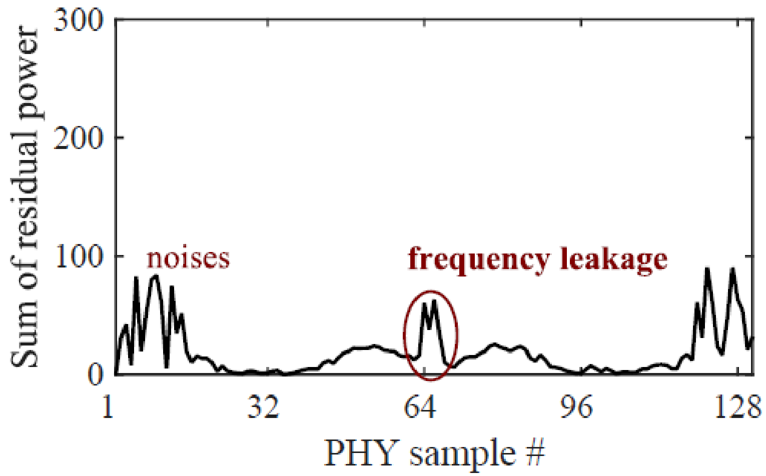
1. Moving window.
2. Difference of adjacent FFT.
3. Sum all the amplitude.

Approach one-frequency based

- **Unreliable** when there are noise.



(a) Detected freq. leakage (D=1)



(b) Detected freq. leakage (D=2)

Need to find another robust approach.

LiteMAP – Phase based approach

- **Frequency leakages are essentially caused by the *phase jitters***
  - Introduced by the hardware of LoRa modem.
  - **Aka**. Adding phase to change frequency.
  - Changing phase to modulate frequency switch.

$$\boxed{\text{a frequency shift keying } s(t) = Acos(2\pi(f \pm \Delta f)t)}$$

$$\boxed{\text{phase shift keying of } s(t) = Acos(2\pi f t \pm \Phi(t)), \text{ where } \Phi(t) = 2\pi \Delta f t.}$$

LiteMAP – Phase based approach

- **Received signal considering phase jitter**

$$R_{jit}(t, f_{sym}) = S(t, \boxed{f_{sym}}) \cdot \boxed{e^{j\varphi(t)}},$$

Phase jitter

Symbol initial frequency

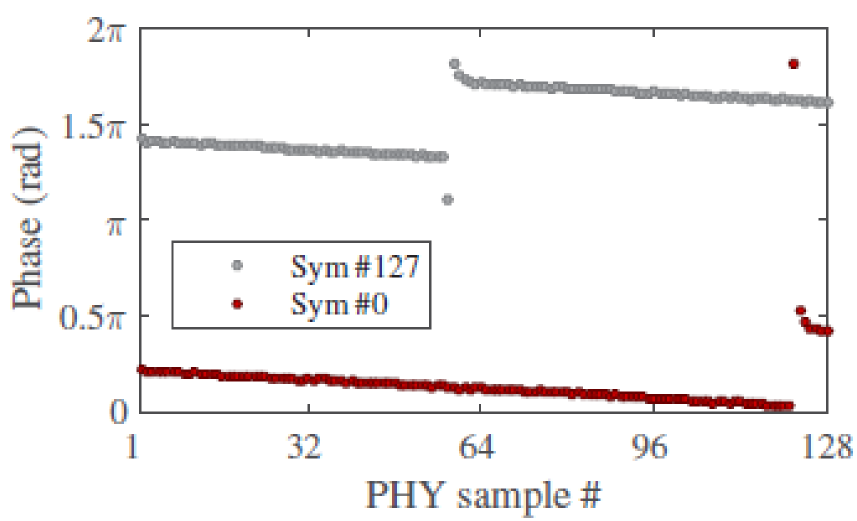
- **1. Obtain f_{alias} according to received signal.**
- **2. nBW/D is integer and is one. Rest fi(t) and f_{cfo}.**

$$\begin{aligned} & R_{jit}(t, f_{sym}) \cdot S^{-1}(t, f_{alias}) \\ \approx \; & h(t) e^{j2\pi\Delta f_{cfo} t} \underline{S(t, f_{sym}) e^{j\varphi(t)}} \cdot S^{-1}(t, f_{alias}) \\ = \; & h(t) \underbrace{e^{j2\pi\Delta f_{cfo} t}}_{\text{Carrier Frequency Offset (deal with preamble)}} \cdot \underbrace{e^{j2\pi(n\frac{BW}{D})t}}_{\text{integer}} \cdot e^{j\varphi(t)} \end{aligned}$$

$$\boxed{f_{sym} = f_{alias} + n\frac{BW}{D},}$$

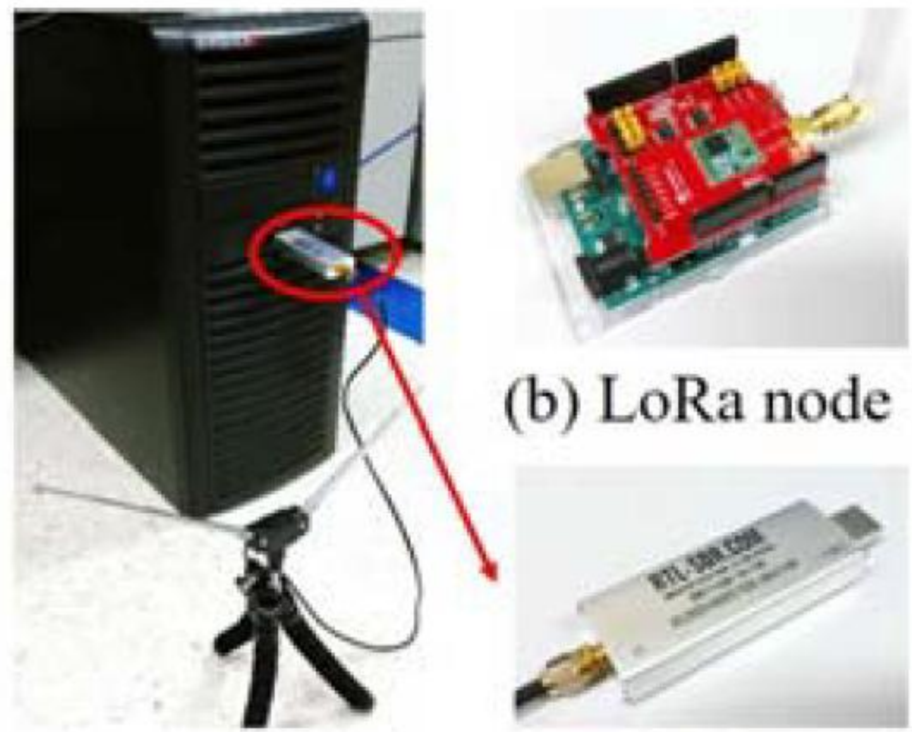
Carrier Frequency
Offset
(deal with preamble)

integer



Evaluation

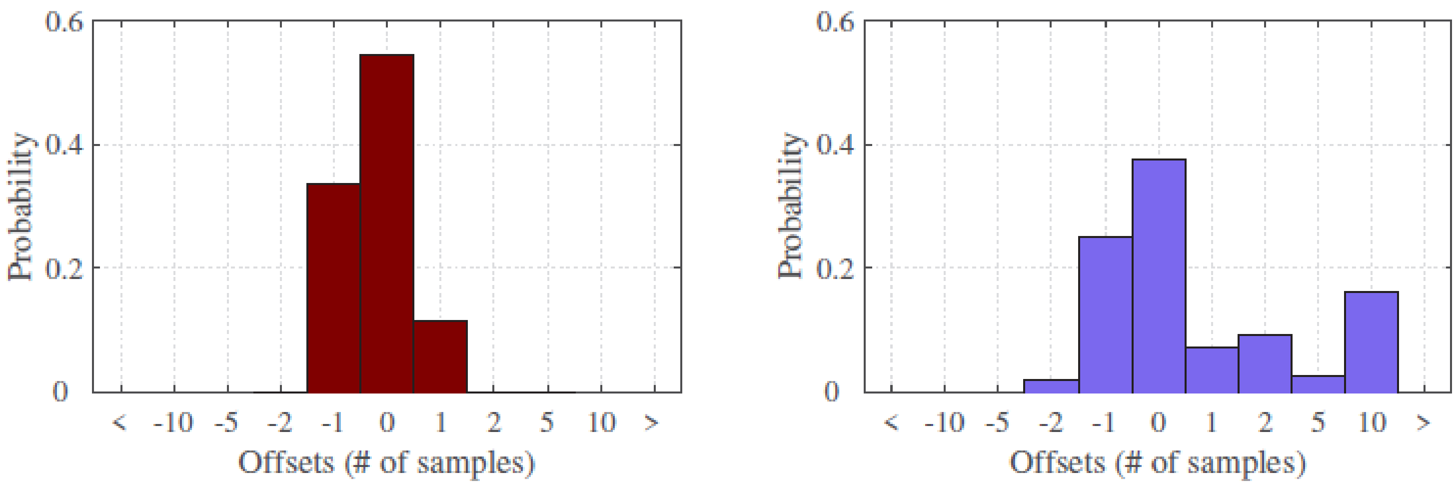
- Base station: PC + RTL-SDR
- LoRa node: Dragino LoRa shield
  - Settings:
    - *SF*=8, *BW*=250 kHz and coding rate *CR*=4/5.
  - RTL-SDR
    - Low sampling rates.



(a) Base station (b) LoRa node (c) RTL-SDR

Fingerprint extraction

- Phase-based is more robust than frequency-based



(a) Phase-based approach (b) Frequency-based approach

Fig. 12. Histogram of offsets (in # of PHY samples) between the extracted fingerprints and the ideal locations under the downclocking factor of D=8.

Packet reception performance

- 1,000 packets (payload: 22 Bytes).
- **Can be reduced to 1/8 Nyquist-rate.**
- Poor (<5dB) and Good (≥5dB) SNRs.

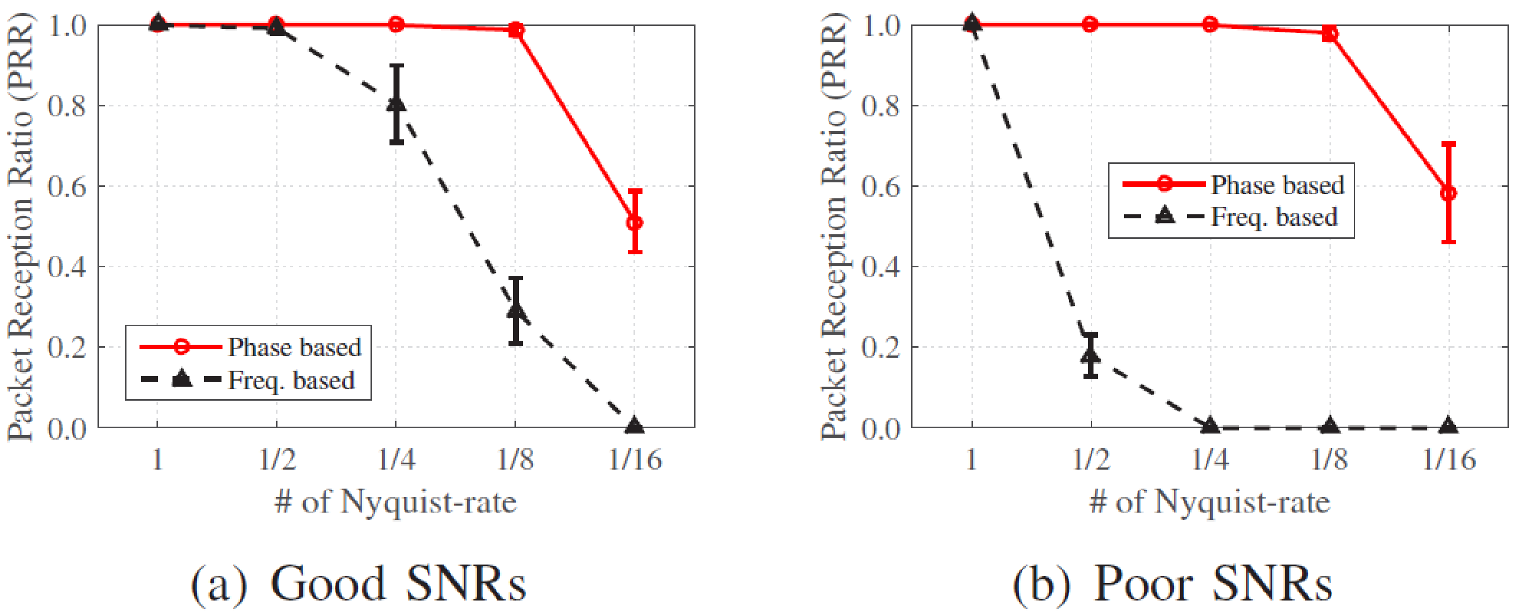
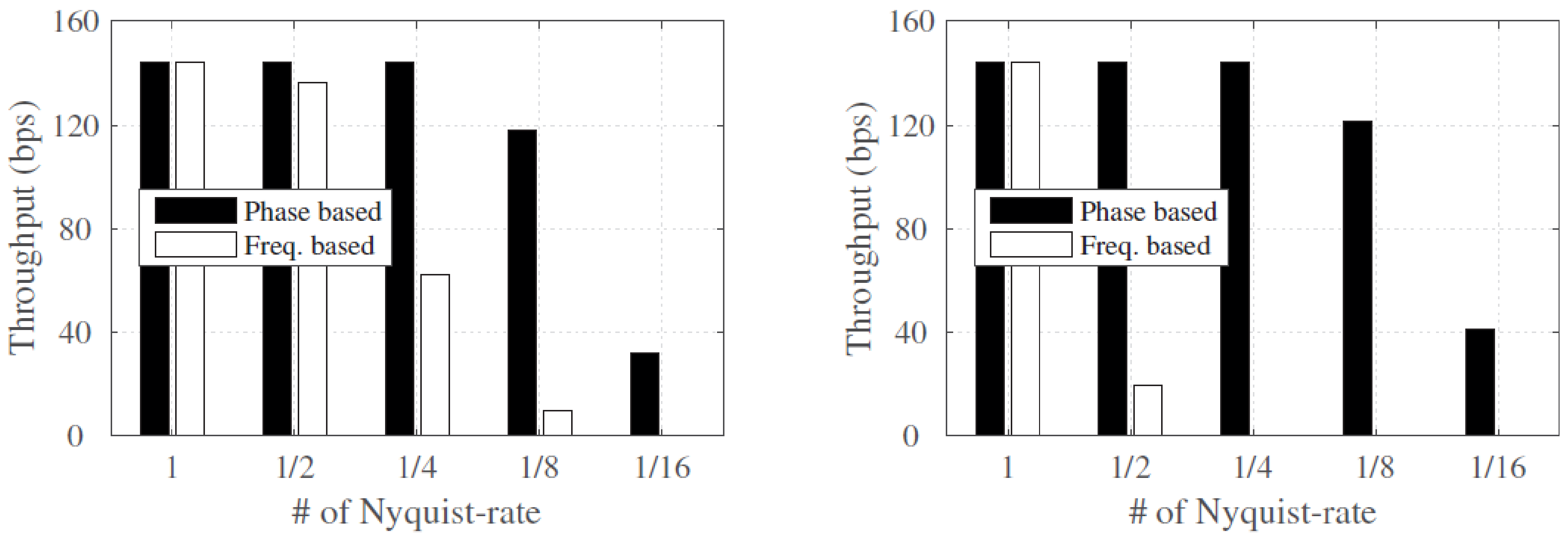


Fig. 13. Impacts of downclocking on Packet Reception Ratio (PRR).

Throughput performance

- 85% of the throughput of full sampling rate. (Phase-based)



(a) Good SNRs (b) Poor SNRs

Fig. 14. Impacts of downclocking on throughput.

Energy saving

- (payload: 22 Bytes) with a duty-cycle of 2%.
- Consumption reduced by 56.6%. with 1/8 Nyquist-rate.

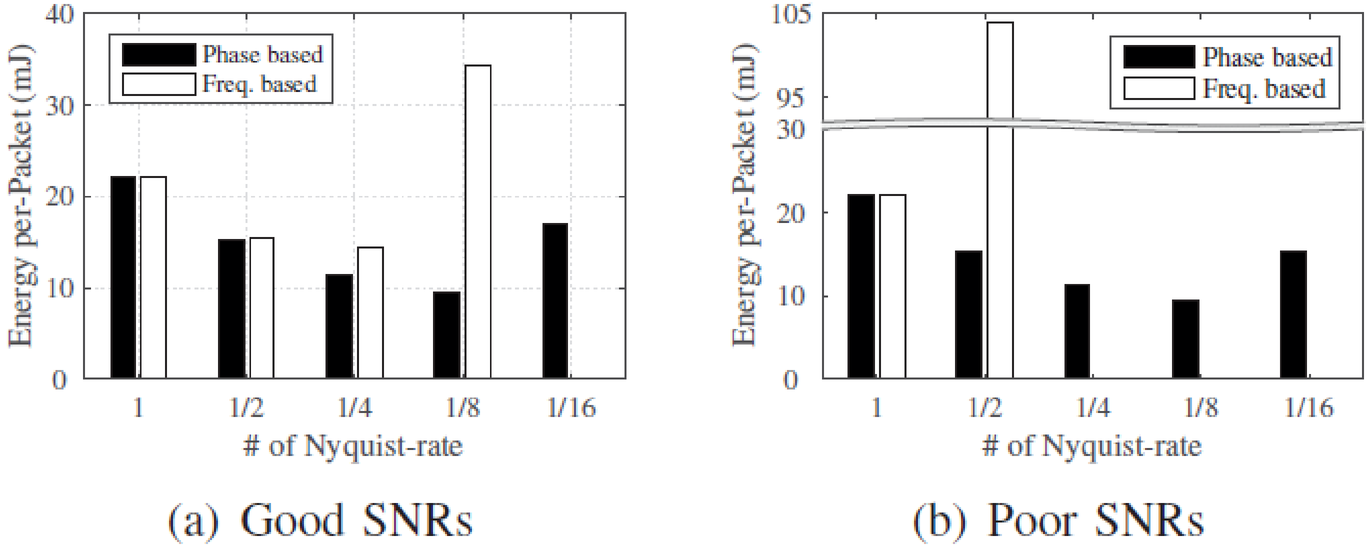


Fig. 16. Per-packet energy consumption under different downclocking factors. For the frequency-based approach, since no packets are correctly received in the cases of D=16 in good SNRs and D=4, 8, 16 in poor SNRs (see Fig.13), the corresponding results are absent.

Energy saving

❑ Power characteristics

TABLE II

POWER CHARACTERISTICS OF DOWNCLOCKED LORA RECEPTION.

Downclocking factors	***D*=1**	***D*=2**	***D*=4**	***D*=8**	***D*=16**
Transmit power (mW)	66.00	66.00	66.00	66.00	66.00
Receive power (mW)	37.95	24.67	17.08	13.28	11.39
Standby power (mW)	5.94	3.86	2.67	2.08	1.78
Packet on-air time	35.84 $\sim$ 46.08 (ms)				
LoRaWAN on-duty time*	3 (s)				

*on-duty time = TX Win + 2×RX Win + RX Delays(idle waiting).

Conclusion

- **Improve the energy efficiency of LoRa by enabling sub-Nyquist sampling and packet decoding**
- **Frequency leakage within a chirp can serve as a fingerprint to uniquely identify a symbol**
- **Results show that a down-clock receiver can reduce power consumption by up to 50%, while achieving comparable packet reception performance of a fullclock receiver in good channel conditions.**

$$f = n_c \frac{BW}{D} + f_{alias}$$

- **Future:**
  - Downclock decoding in WiFi OFDM (QAM)?
    - A(10), B(20), C(30,) D(40), E(50), F(60). (Fs=120Hz)
    - -20, -10, 0, 10, 20, 0. (Fs=60Hz, D=2) A,B,D,E, C+F
    - -10, 0, 10, 0, 10, 0. (Fs=30Hz, D=3) A, C+E, B+D+F,

Thanks!