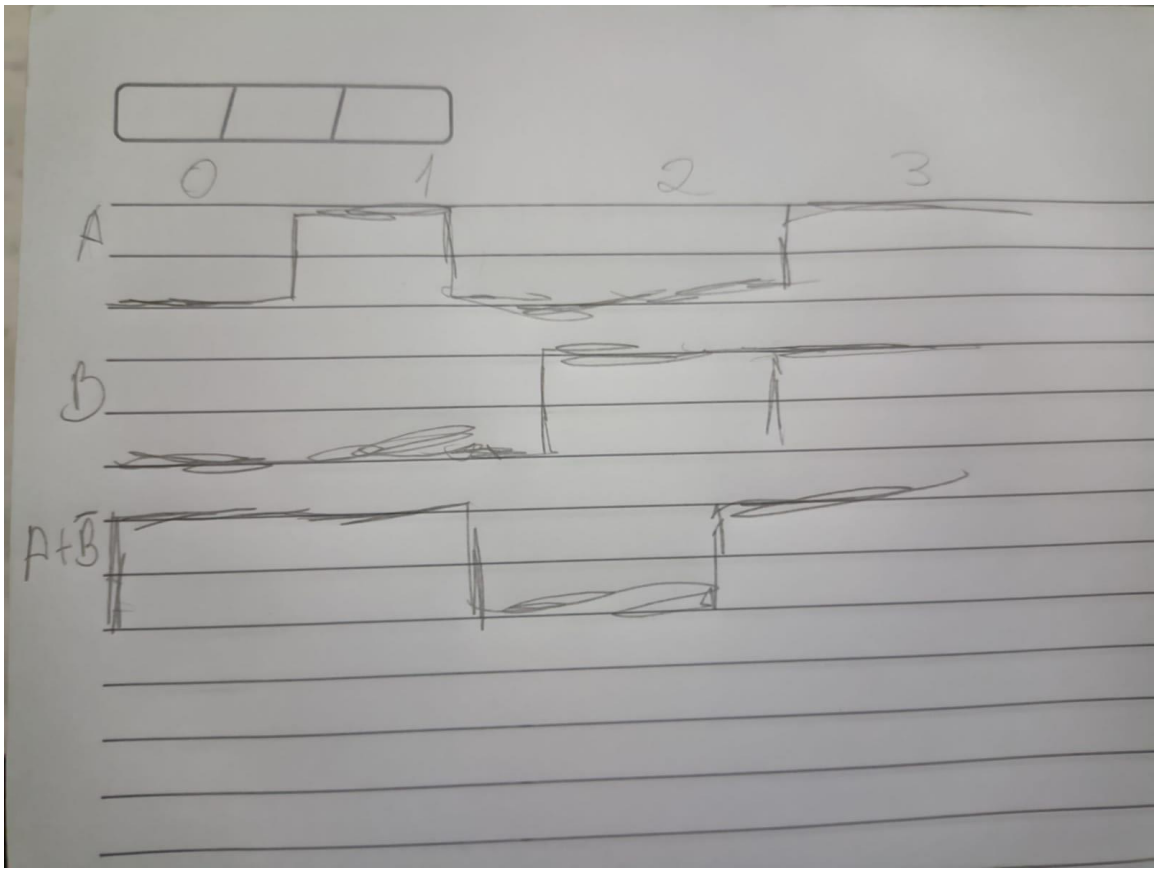
1.

```
library IEEE;
use IEEE.std_logic_1164.all;

entity ent is
port(
        a: in std_logic;
   b: in std_logic;
   c: in std_logic;
   d: in std_logic;
   s1: out std_logic;
   s2: out std_logic;
   s3: out std_logic;
   s4: out std_logic
);
end ent;

architecture arc of ent is
begin
        process(a , b , c , d) is
   begin
        s1 <= a or (not b);
      s2 <= (a or (not b)) and c or d;
      s3 <= (a or (not b)) and (c or d);
      s4 <= (a or (not b)) and not(c or (a and d));
   end process;
end arc;
```

2.



3.

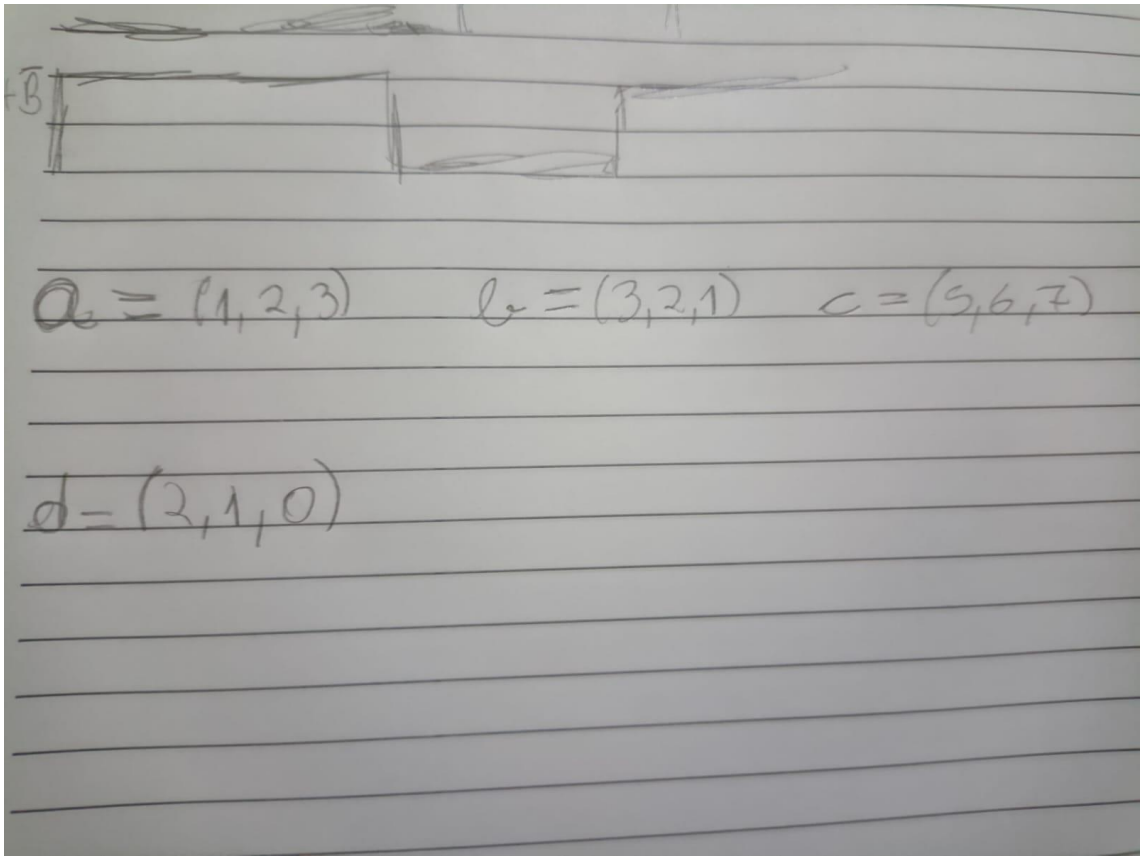
```
library IEEE;
use IEEE.std_logic_1164.all;

entity ent is
port(
   a: in bit_vector;
   b: in bit_vector;
   c: in bit_vector
);
end ent;

architecture arc of ent is
```

begin

4.



7. ENTITY corret_1 IScapa_1ra

PORT (a, b, c, d : IN BIT;

s : OUT BIT_VECTOR (5 DOWNTO 0));

END corret_1;

ARCHITECTURE teste OF corret_1 IS

BEGIN

s(0) <= (a AND b) OR (c AND d); -- opcao 1

--s(0) <= a AND (b OR c) AND d; -- opcao 2

s(1) <= (a NOR b) NOR c; -- opcao 1

--s(1) <= a NOR (b NOR c); -- opcao 2

```
  s(2) <= (a AND  b) OR c;        -- opcao 1
--s(2) <=  a AND  (b OR c);       -- opcao 2

  s(3) <= NOT (a AND b) NAND c;   -- correta
  s(4) <= a XOR  b XOR c;         -- correta
END teste;
```