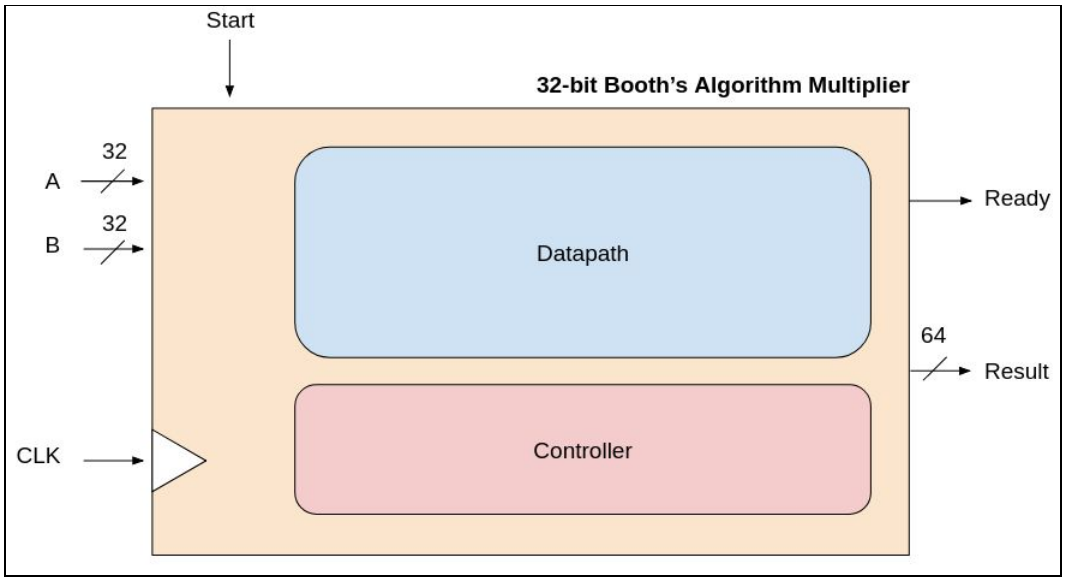
ASSIGNMENT 6

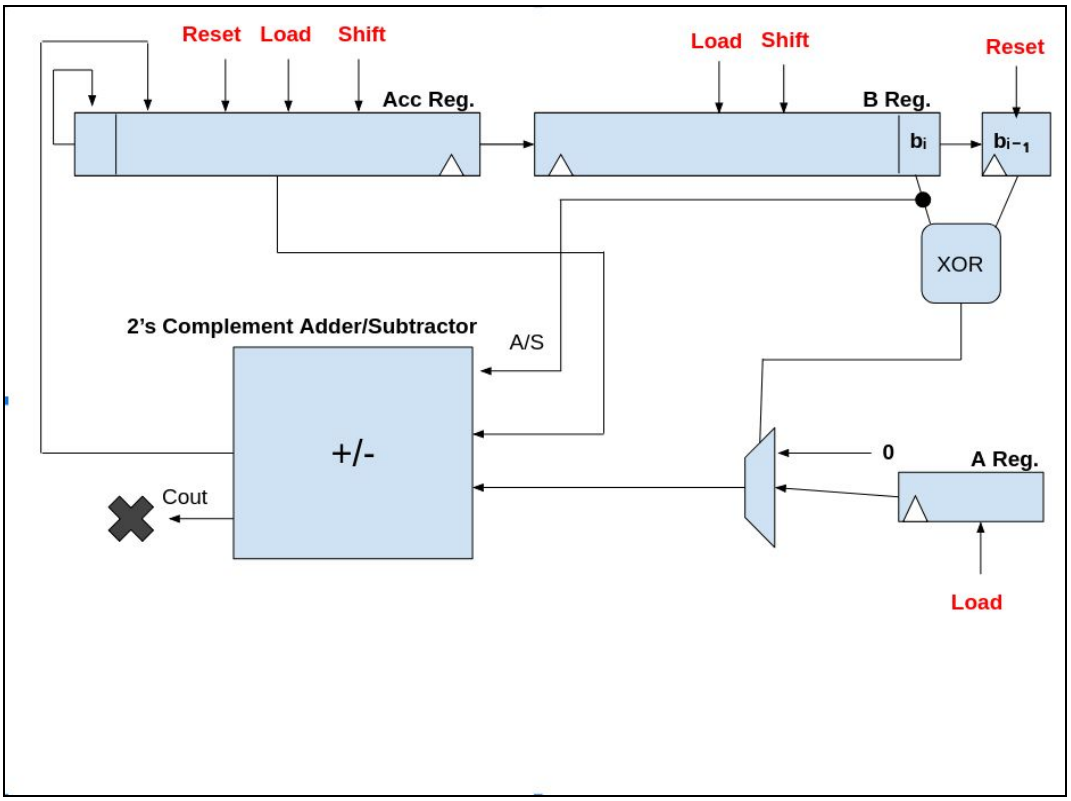
32-bit Booth's Algorithm Multiplier (Part 1: Datapath Circuit):

Diagram of the inputs and outputs of the final Booth's algorithm multiplier:



For this lab, you will be designing only the Datapath circuit for the Booth's algorithm multiplier. The next lab will cover the design of the controller for the circuit. For this lab, refer to the picture below for a reminder of what the datapath of Booth's algorithm looks like. Implement all of the blue modules shown in the figure below. Also add the extra functions (shown in red) to each of the modules that contain them.

Diagram of the Datapath portion of Booth's algorithm multiplier:



The extra functions (shown in red) will come into play for part 2 in next week's lab. Here are a list of the modules that I need to see implemented:

- 2's Complement Adder/Subtractor
- The Acc. Reg (This is a 32-bit shift register that shifts *arithmetically* to the right)
- The B Reg (This is a 32-bit shift register that shifts to the right)
- Bi-1 Reg (This is just a 1-bit D Flip Flop)
- 2-1 MUX
- A Reg (this is a regular 32-bit register)

Write testbenches for each module to verify that each module works correctly.
NOTE: The white triangles represent clock (CLK) input.

Lab Assignment:
Design the Datapath elements of the Booth's algorithm multiplier in Verilog. Create a testbench to test your design for various input combinations. In your **compressed zip file**, provide Verilog code for each module, test bench code, and timing diagram.

Due Date: Deliverables—Mar. 5 11:59pm (submit on BlackBoard)
Demo---Mar. 6 (during lab class)