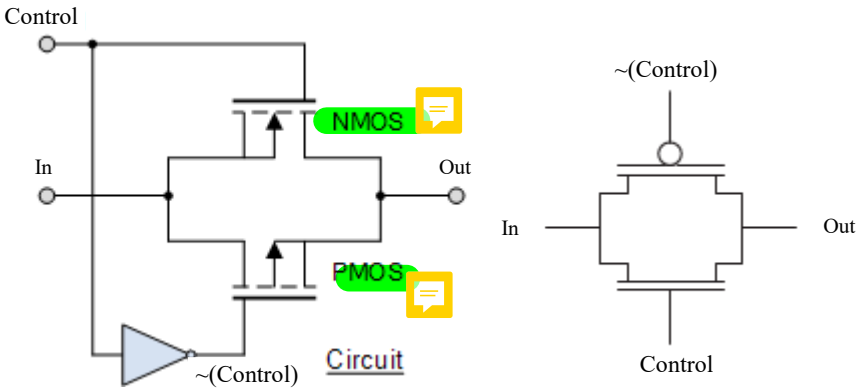
EE 4513 – Fall 2019
Lab Assignment #7

Objective:

To learn and implement the layout of simple sequential circuits using standard cells and verify their functionality.

Tasks:

1. Draw the layout of a Transmission Gate (Also known as a C – switch) and verify its functionality.



(a) (b)

Figure 1: (a) Schematic of a Transmission Gate. (b) Typical symbol of transmission gate

2. Using C-switches and inverters create the layout of a positive edge triggered D Flip Flop and verify the functionality. Follow the schematic of a D-Flip Flop given below.

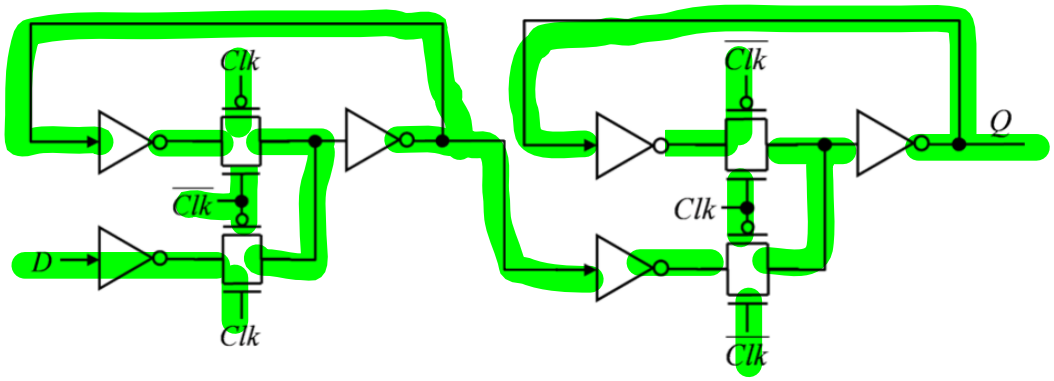


Figure 2: Schematic of A positive edge triggered D Flip Flop using transmission gates and inventers.

Report:

You should turn in a report containing the following items:

1. A description of the layout you created, and any challenges faced.
2. Snapshots of layouts and the corresponding simulation waveforms.