Fall 2019

EE 4513 – Introduction to VLSI Design

Lab Assignment # 8

In this lab assignment,

1. You are required to design: (i) 64 x 64 Array Multiplier
(ii) 16-bit synchronous up/down (selectable) counter

2. Once you have written the Verilog code of your design and completed the behavioral simulation (for example, using Vivado), synthesize your code to generate the netlist using Cadence RTL Compiler (RC).

3. Then, use the Cadence Encounter platform to generate the GDS2 layout of your design. Verify your design for connectivity, and geometry violations.

Turn in report, which includes the following: -

1. The directory path (in Linux) where you worked on and created the multiplier and counter. Work on the two designs in separate directory.
2. Simulation waveforms for your multiplier and counter
3. Physical Layout snapshot of your design
4. Snapshots of portions of the connectivity and geometry verification reports, showing any violations, if present.
5. Schematic of your design (can be seen by clicking Tools -> Schematic Viewer)
6. Report Your Timing Analysis (Slew, Delay, Arrival...etc) and Total Area from your RTL compiler for your design.
7. Snapshot of the message showing successful generation of GDS2 layout
8. Try to optimize your design in the Verilog (efficient /structured code) and post a conclusion for your design.

Note: -

1. Once you have logged in, you can make a new directory called **lab8hw** using the **mkdir** command (**mkdir lab8hw**) in the terminal. Then change over to the created directory using **cd lab8hw.** Inside this directory, make two new directories called "**multiplier**" and "**counter**" using the **mkdir** command. Use these two directories to create the layout of the respective Verilog modules that you will be making in this assignment. Provide the path of these two directories in the report.