Daniel Yeum

Report:

You should turn in a report containing the following items: -

1. Design approach adopted.

   I used multiple copies of basic gates like the AND and NAND gates. This was so that in the complex gates I could use those single copies for ease of build, and if I needed to change a specific part of just that gate I could edit it, without changing the original. By running simulations for each gate I reduced any debug time and made sure one part was working as I made my way up to the 8-bit Full Adder. There were some errors, however, I think they were all fixed and the output was shown to be correct.

2. Snapshots of layouts and the corresponding simulation waveforms. Also, include the final gate-level schematic for each part mentioned above.

1. Create the layout for a 2 input XOR gate using Virtuoso. Use the 2 input NAND cell from your library to create the 2 input XOR cell. Use the diagrams below as a guideline. Verify the functionality of the XOR cell for all input combinations using the built-in simulation tool.

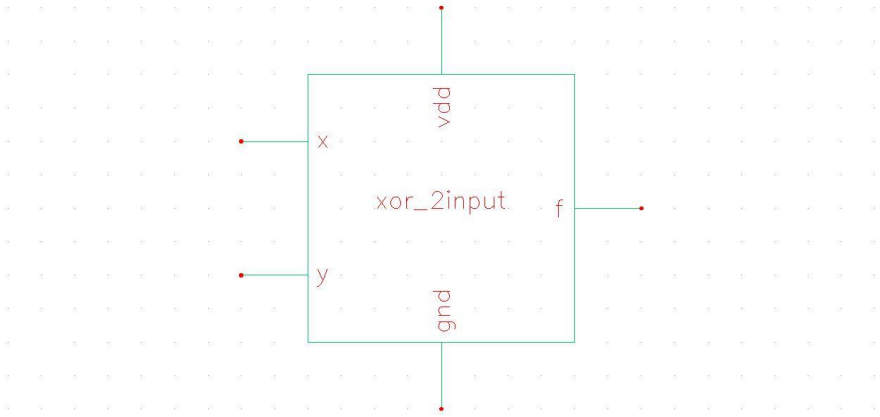


Figure 1: 2-input XOR Symbol

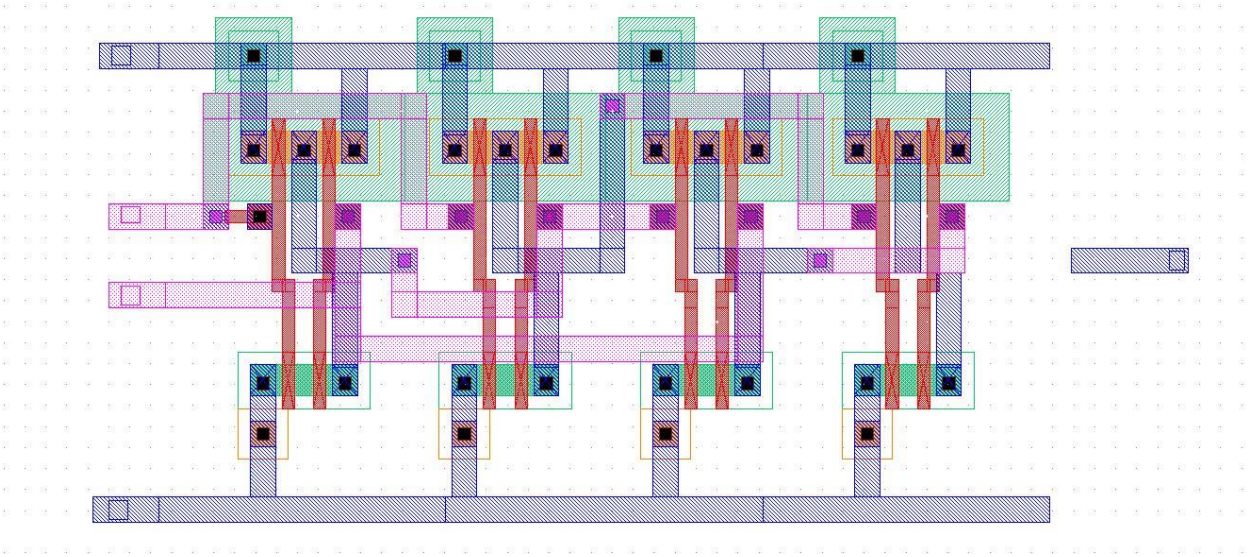


Figure 2: 2-input XOR layout

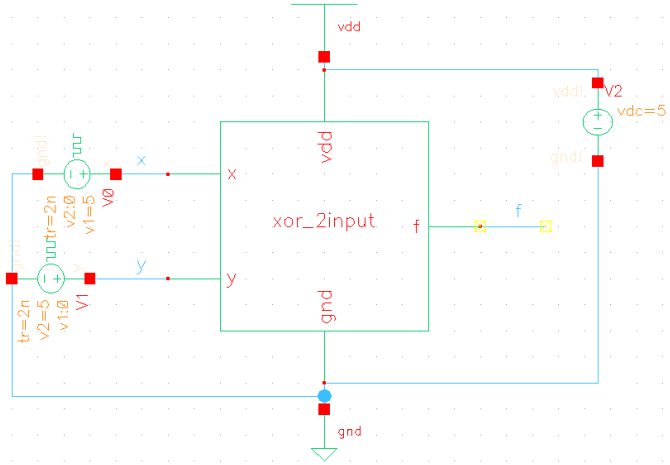


Figure 3: 2-input XOR Schematic

Figure 4: 2-input XOR Simulation

2. Using the 2 input XOR cell you created in Step 1 and other basic cells from your library, draw the layout for a Full Adder. Verify for functionality.

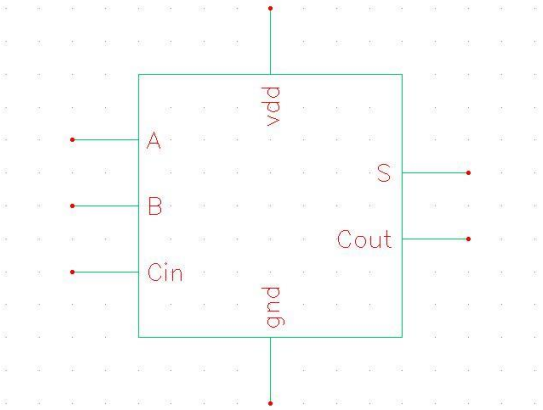


Figure 5: 1-bit Full Adder Symbol

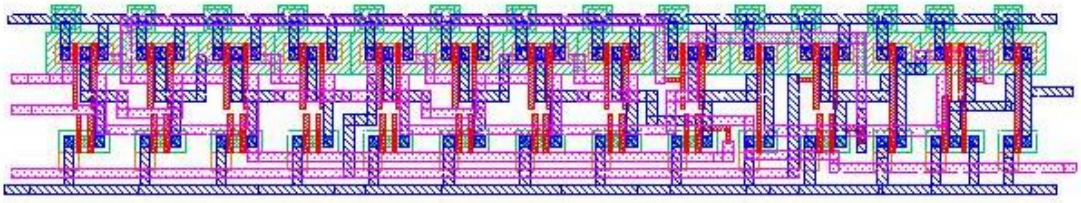


Figure 6: 1-bit Full Adder Layout

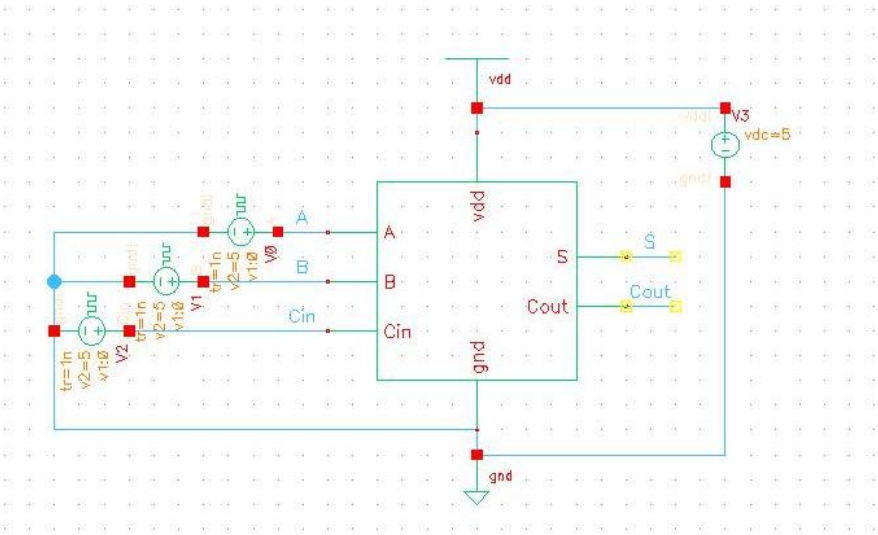


Figure 7: 1-bit Full Adder Schematic

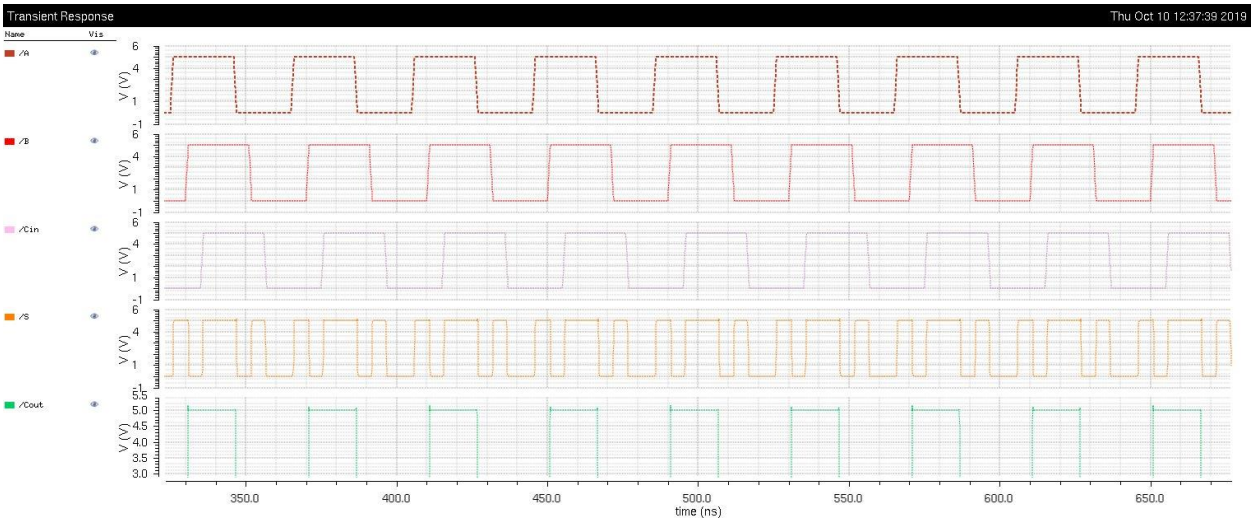


Figure 8: 1-bit Full Adder Simulation

3. Using 8 such FAs (from Step 2) design an 8-bit adder.

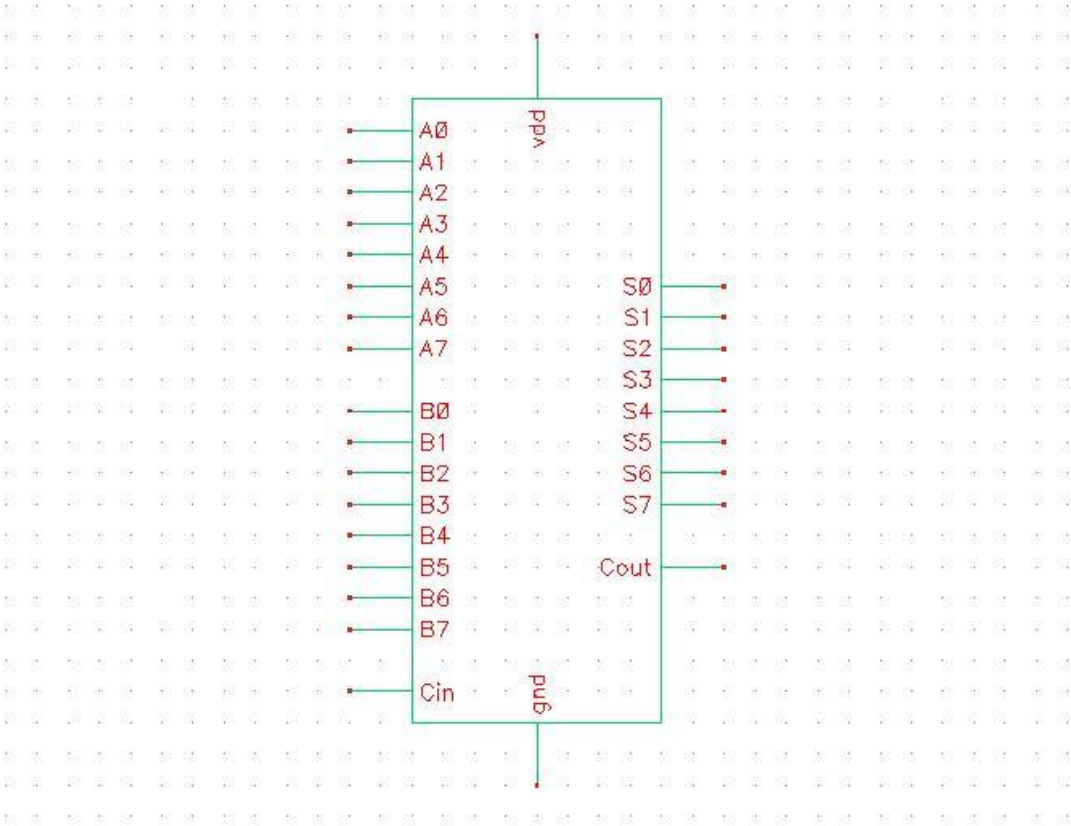


Figure 9: 8-bit Full Adder Symbol

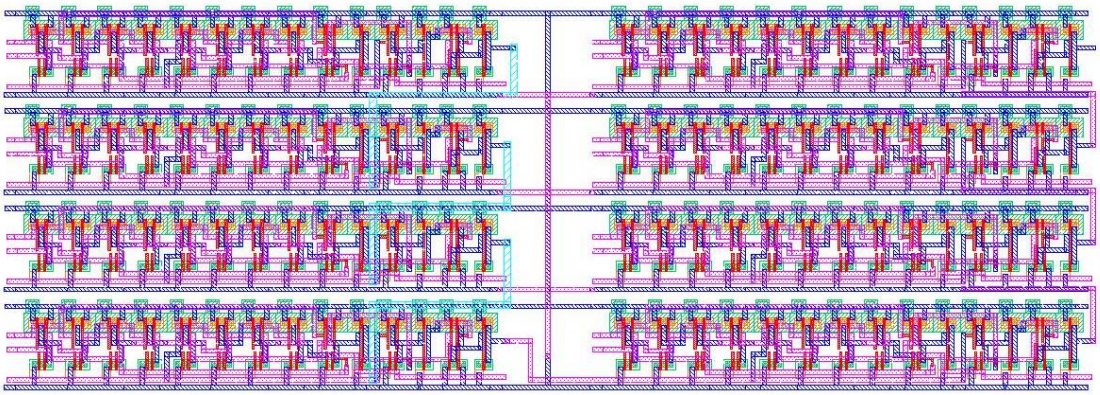


Figure 10: 8-bit Full Adder Layout

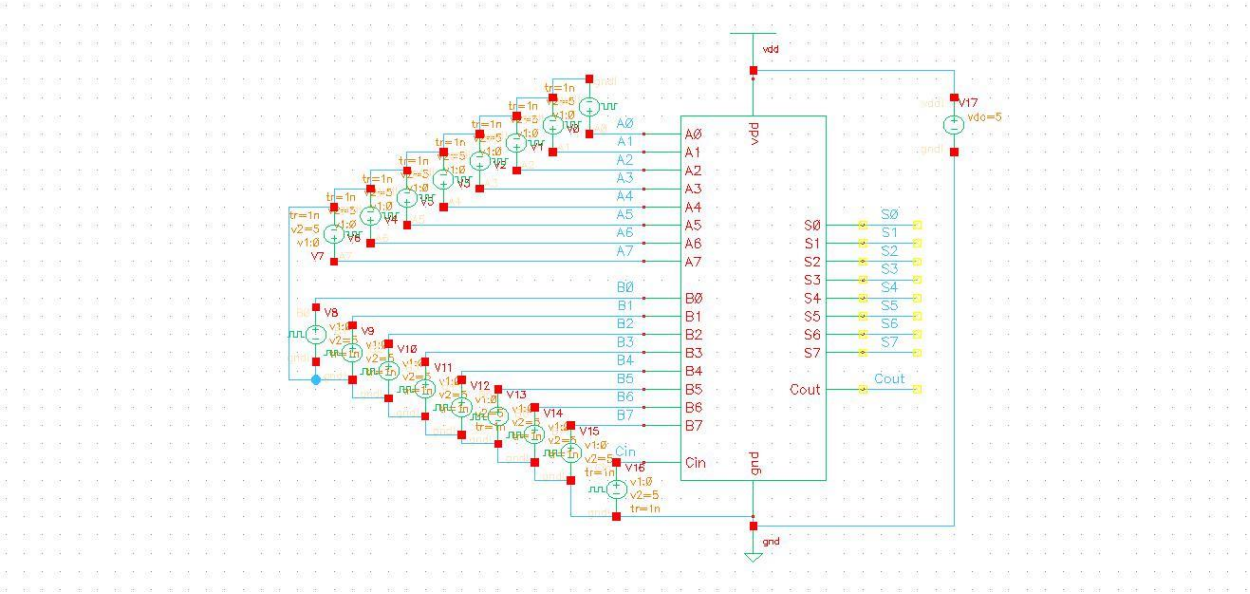
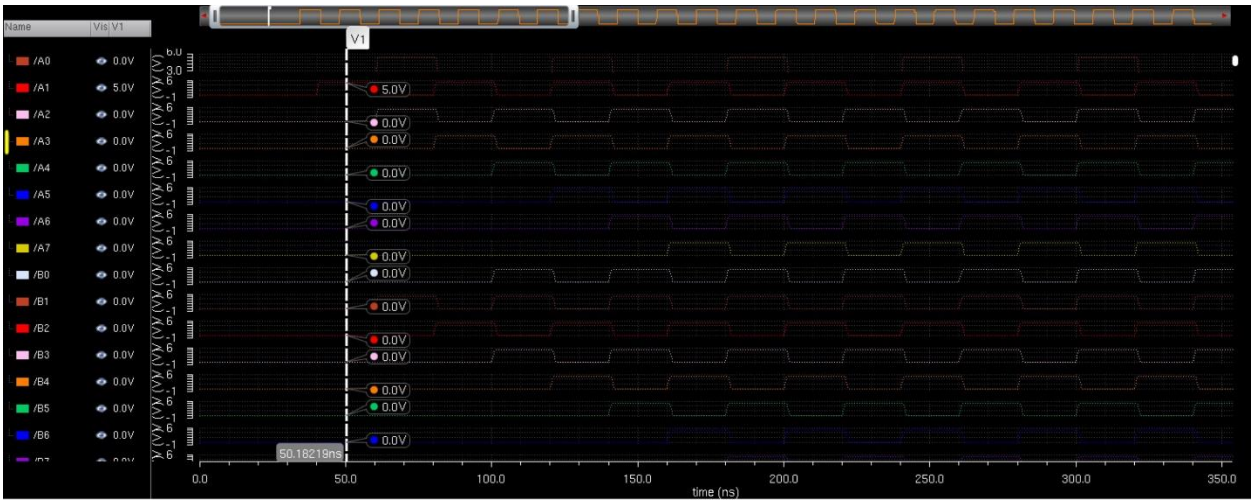
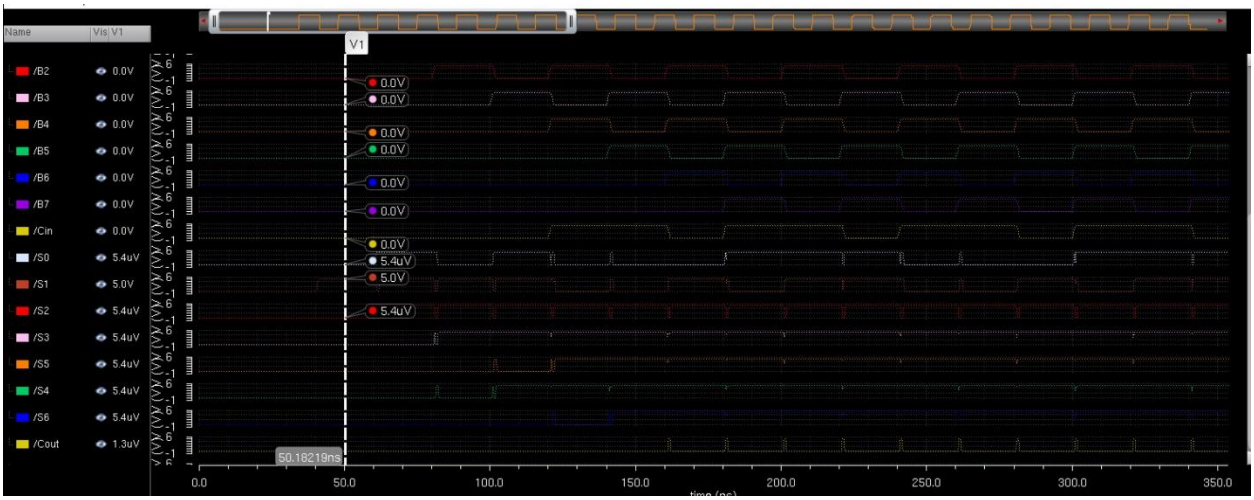
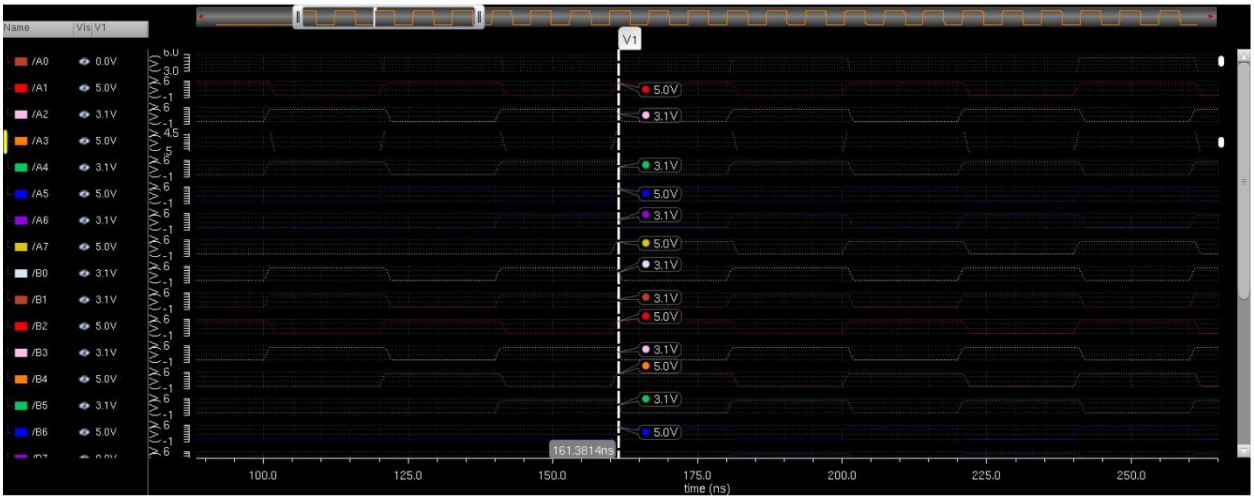


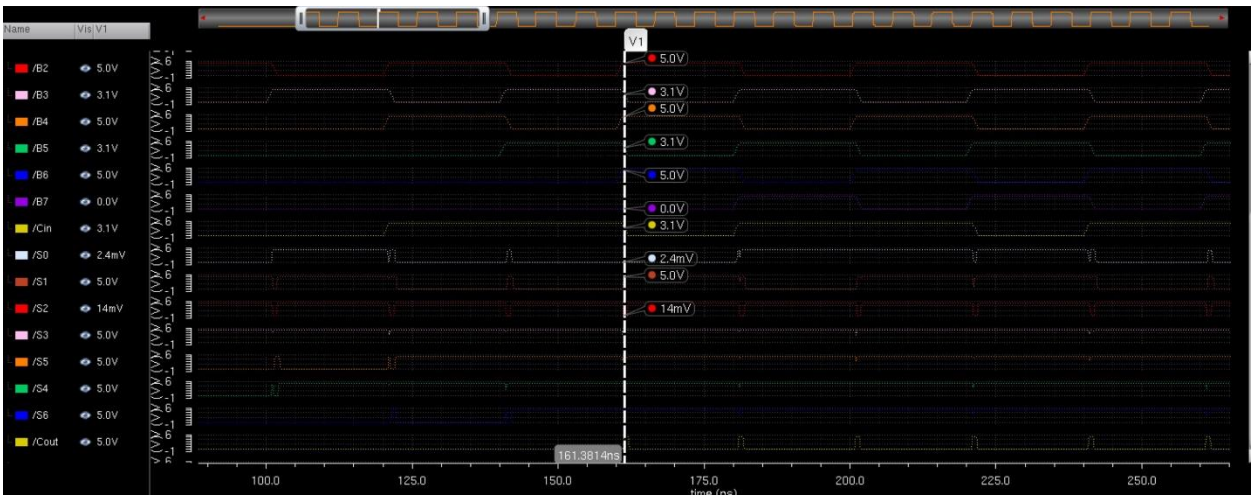
Figure 11: 8-bit Full Adder Schematic

4. Verify the functionality of the 8-bit adder using SPICE for at least four different input combinations. Also indicate the worst-case delay for your layout.




Name
Vis
V1
/B2 0.0V
/B3 0.0V
/B4 0.0V
/B5 0.0V
/B6 0.0V
/B7 0.0V
/Cin 0.0V
/S0 5.4uV
/S1 5.0V
/S2 5.4uV
/S3 5.4uV
/S5 5.4uV
/S4 5.4uV
/S6 5.4uV
/Cout 1.3uV
50.18219ns
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0


Name
Vis
V1
/A0 0.0V
/A1 5.0V
/A2 3.1V
/A3 5.0V
/A4 3.1V
/A5 5.0V
/A6 3.1V
/A7 5.0V
/B0 3.1V
/B1 3.1V
/B2 5.0V
/B3 3.1V
/B4 5.0V
/B5 3.1V
/B6 5.0V
161.3814ns
100.0
125.0
150.0
175.0
200.0
225.0
250.0
time (ns)


Name
Vis
V1
/B2 5.0V
/B3 3.1V
/B4 5.0V
/B5 3.1V
/B6 5.0V
/B7 0.0V
/Cin 3.1V
/S0 2.4mV
/S1 5.0V
/S2 14mV
/S3 5.0V
/S5 5.0V
/S4 5.0V
/S6 5.0V
/Cout 5.0V
161.3814ns
100.0
125.0
150.0
175.0
200.0
225.0
250.0