Daniel Yeum

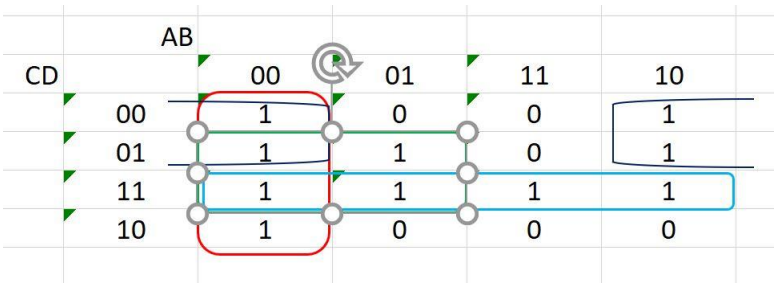
EE 5193 FPGA and Verilog HDL

Assignment 1

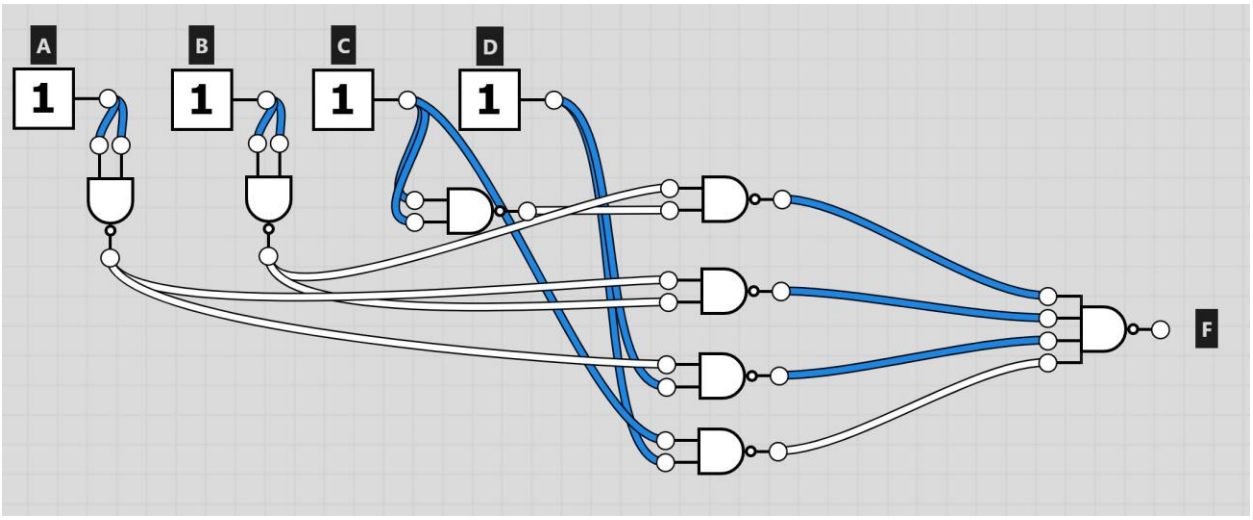
Due on 11th June, by 6.00 PM

1. a. Minimize the four-variable logic function using Karnaugh map and realize it with NAND gates.

$f(A,B,C,D)= \Sigma m(0,1,2,3,5,7,8,9,11,15)$



F = B'C' + A'B' + A'D + CD



b. Minimize the logic function in POS form.

F' = (BD' + ABC' + ACD')'

F = (B' + D)(A' + B' + C)(A' + C' + D)

2. Design a Gray-to-Decimal code converter using 8:1 multiplexers and NAND gates.

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		Gray	Code			Decimal			
	g3	g2	g1	g0	d3	d2	d1	d0	
0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0	2
2	0	0	1	0	0	0	1	1	3
6	0	1	1	0	0	1	0	0	4
7	1	1	1	0	0	1	0	1	5
5	0	1	0	1	0	1	1	0	6
4	0	1	0	0	0	1	1	1	7
12	1	1	0	0	1	0	0	0	8
13	1	1	0	1	1	0	0	1	9

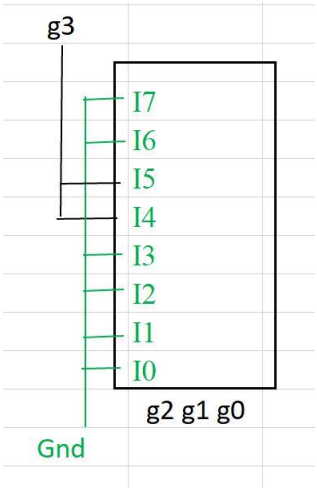
$$D3 = \Sigma m(12, 13)$$

$$D2 = \Sigma m(4, 5, 6, 7)$$

$$D1 = \Sigma m(2, 3, 4, 5)$$

$$D0 = \Sigma m(1, 2, 4, 7, 13)$$

d3				g2g1g0				
	000	001	010	011	100	101	110	111
g3' (0)	0	1	2	3	4	5	6	7
g3 (1)	8	9	10	11	12	13	14	15
	I0	I1	I2	I3	I4	I5	I6	I7



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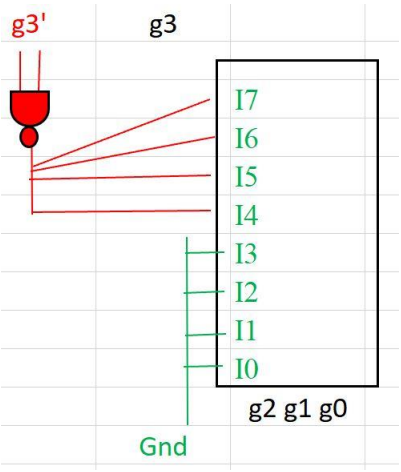
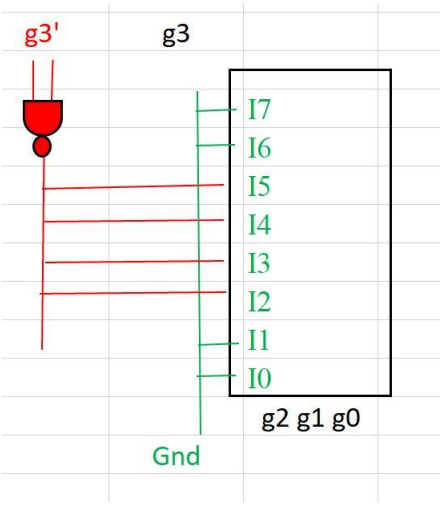
d2				g2g1g0				
	000	001	010	011	100	101	110	111
g3' (0)	0	1	2	3	4	5	6	7
g3 (1)	8	9	10	11	12	13	14	15
	I0	I1	I2	I3	I4	I5	I6	I7



d1				g2g1g0				
	000	001	010	011	100	101	110	111
g3' (0)	0	1	2	3	4	5	6	7
g3 (1)	8	9	10	11	12	13	14	15
	I0	I1	I2	I3	I4	I5	I6	I7



d0				g2g1g0				
	000	001	010	011	100	101	110	111
g3' (0)	0	1	2	3	4	5	6	7
g3 (1)	8	9	10	11	12	13	14	15
	I0	I1	I2	I3	I4	I5	I6	I7

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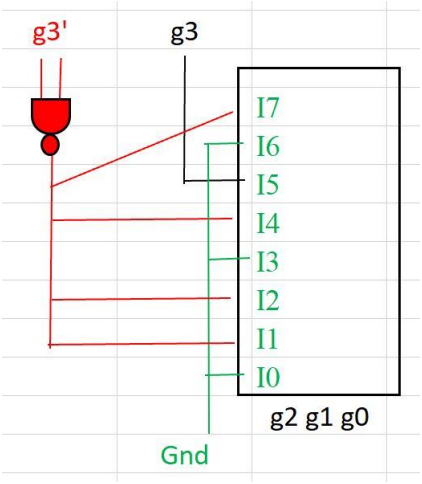
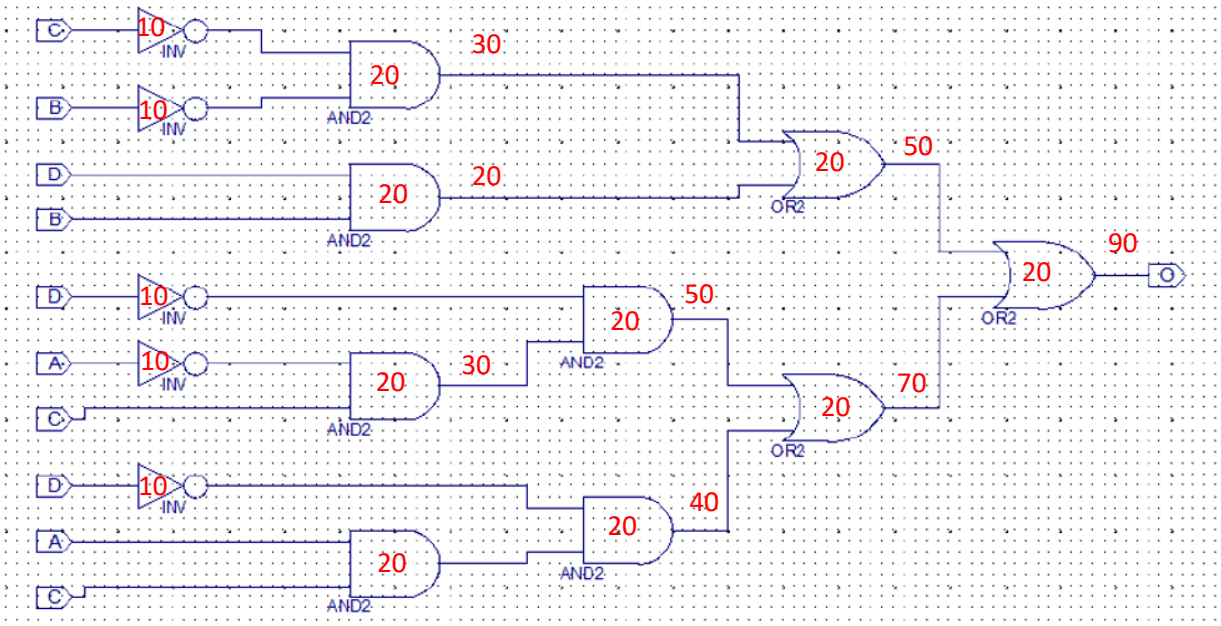


3. Consider the following circuit where the propagation delay of logic gates in the circuit are:

NOT=10ns, AND=20ns, OR=20ns.



a. Draw a truth table for the given circuit. Draw a Karnaugh map using the truth table and derive a sum of product (SOP) expression for the results.

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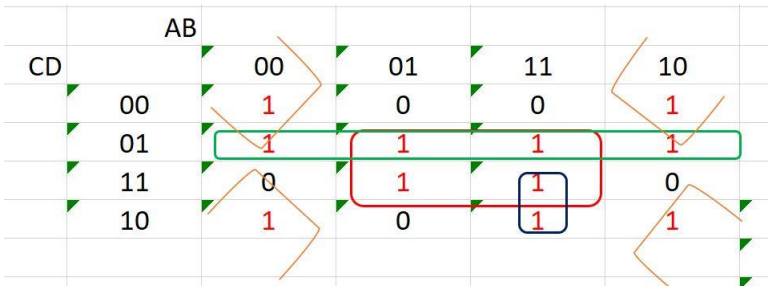

F = C'D + BD + B'D' + ABC

b. Describe advantages and disadvantages of your SOP expression vs the given circuit.

There are unaccounted hazards in my circuit. Advantage is that the circuit is minimized.

c. If the given circuit is used as combinational logic within a clocked system, what is the maximum clock speed of the system? Will the maximum clock speed change if circuit of the SOP expression is used instead?

Max clock speed is 90ns. 50ns with SOP circuit, the max clock speed changes.