

Fall 2019

EE 4513 – Introduction to VLSI Design

Lab 5 - Cadence Layout Assignment

In this assignment, you need to do the following: -

1. Create the layouts for a 3-input NAND gate and a 3-input NOR gate using Virtuoso. Verify their functionality for all input combinations using the built-in simulation tool.
2. Design and Simulate the circuit below in Virtuoso following the procedures in 1.

Turn in a report, which includes the following: -

1. Neat transistor level circuit schematics of the 3-input NAND gate, 3-input NOR gate and the circuit above, which you will be using to develop your layout. Also, mention the total number of transistors in each circuit.
2. The layout files for each circuit.
3. The waveforms for each circuit, showing all input combinations and their corresponding outputs.

=====3-input NAND Schematic=====

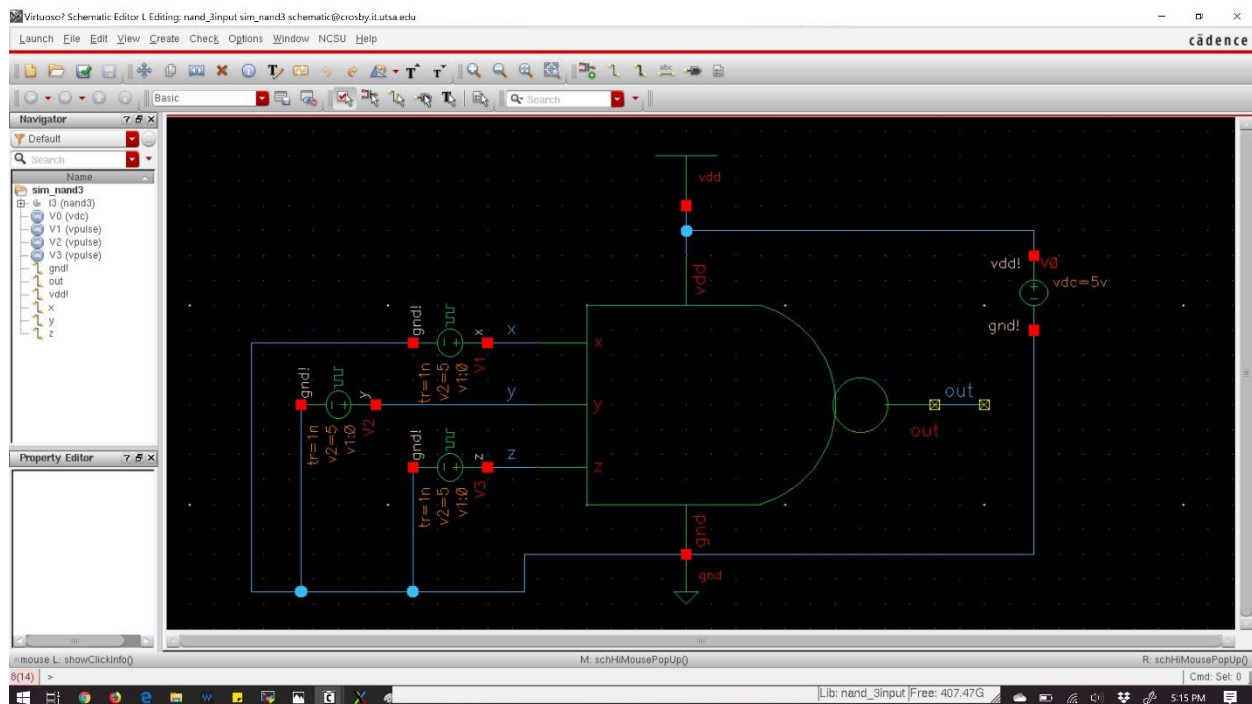


Figure 1: 3-input NAND schematic

3-input NOR Schematic

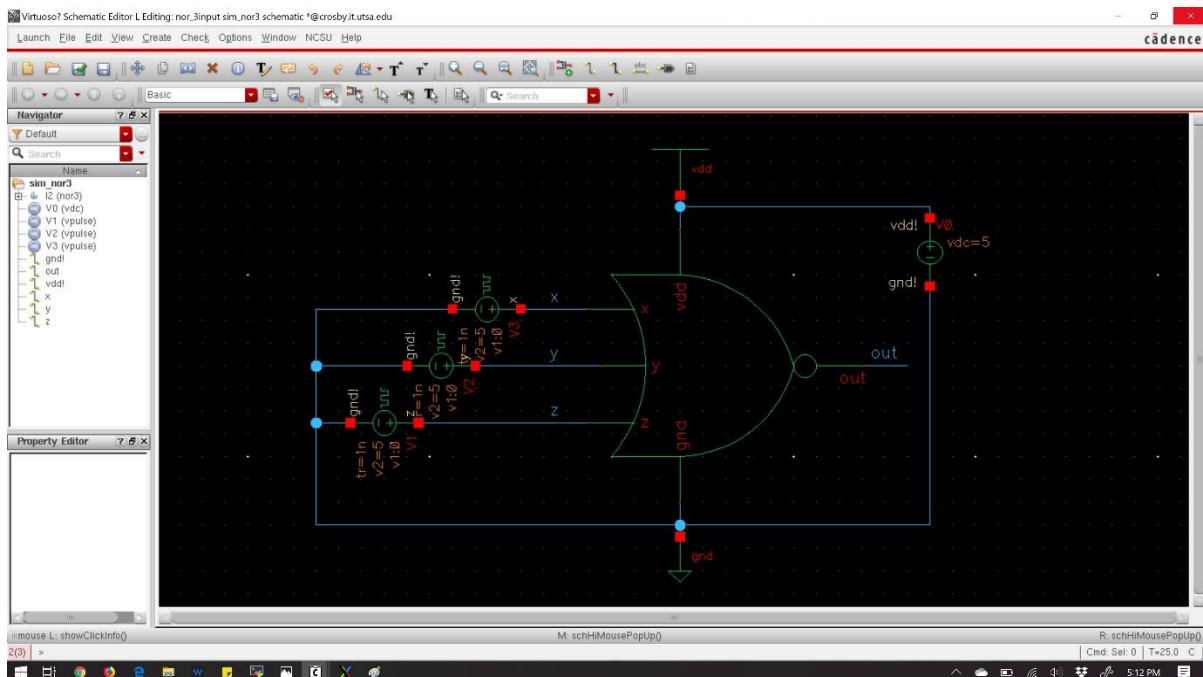


Figure 2: 3-input NOR

Complex Circuit Schematic

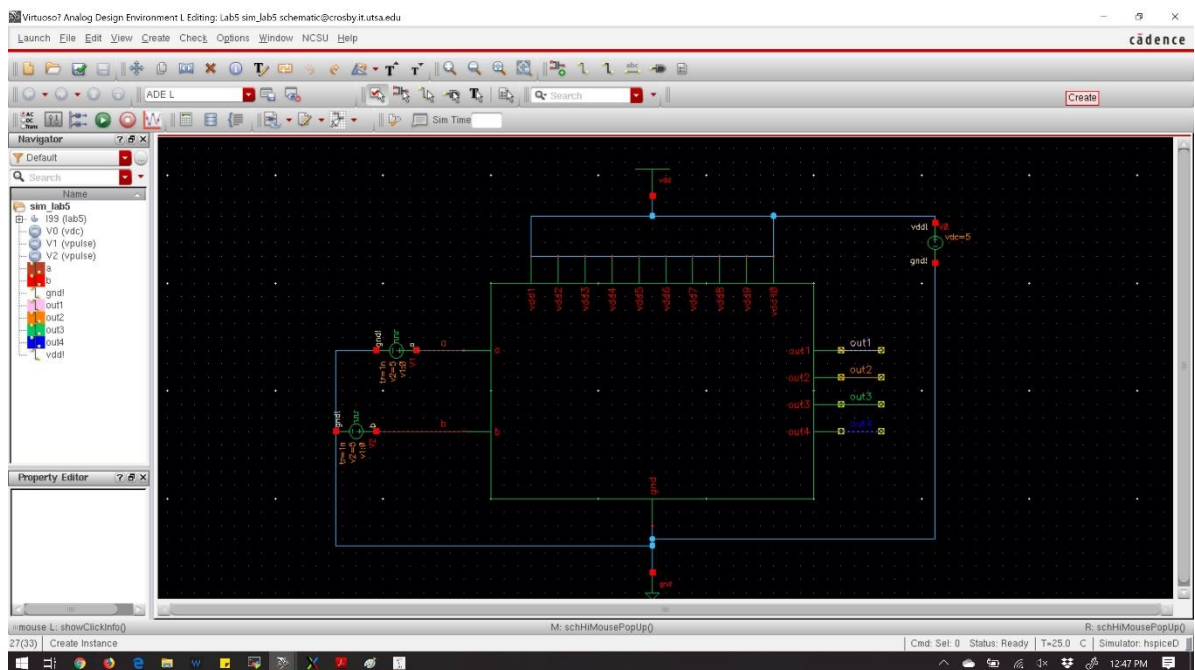


Figure 3: Full circuit schematic

3-input NAND Layout File

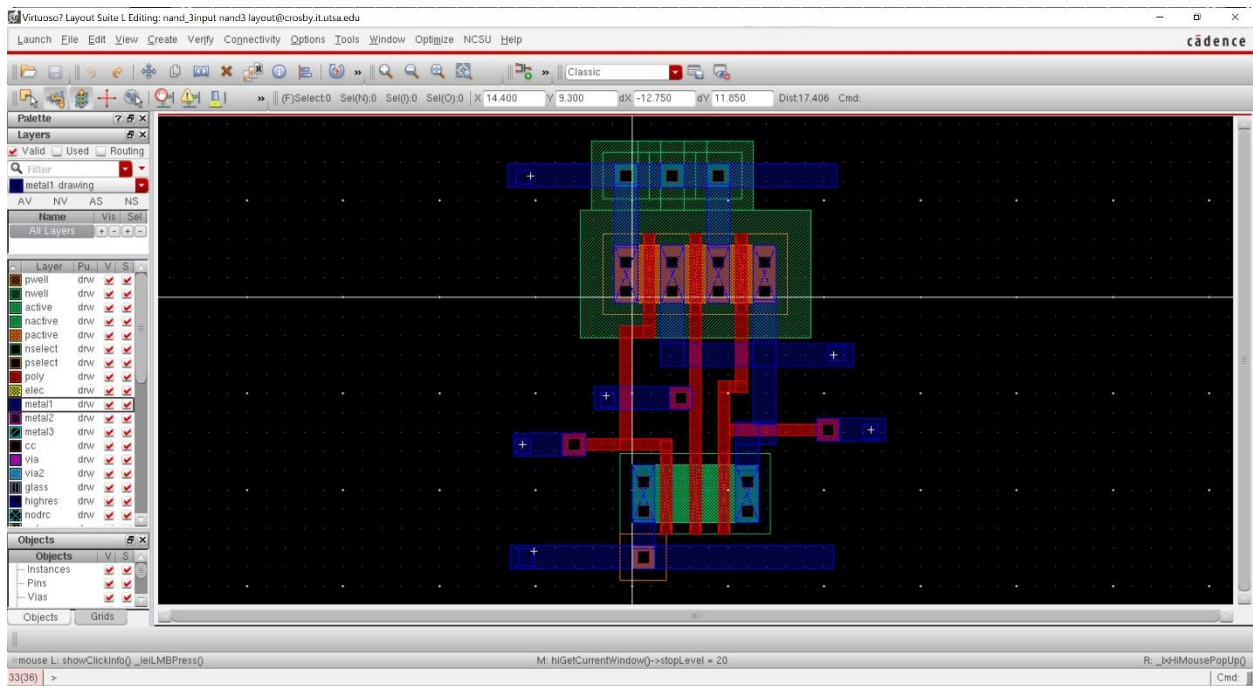


Figure 4: 3-input NAND Layout

3-input NOR Layout File

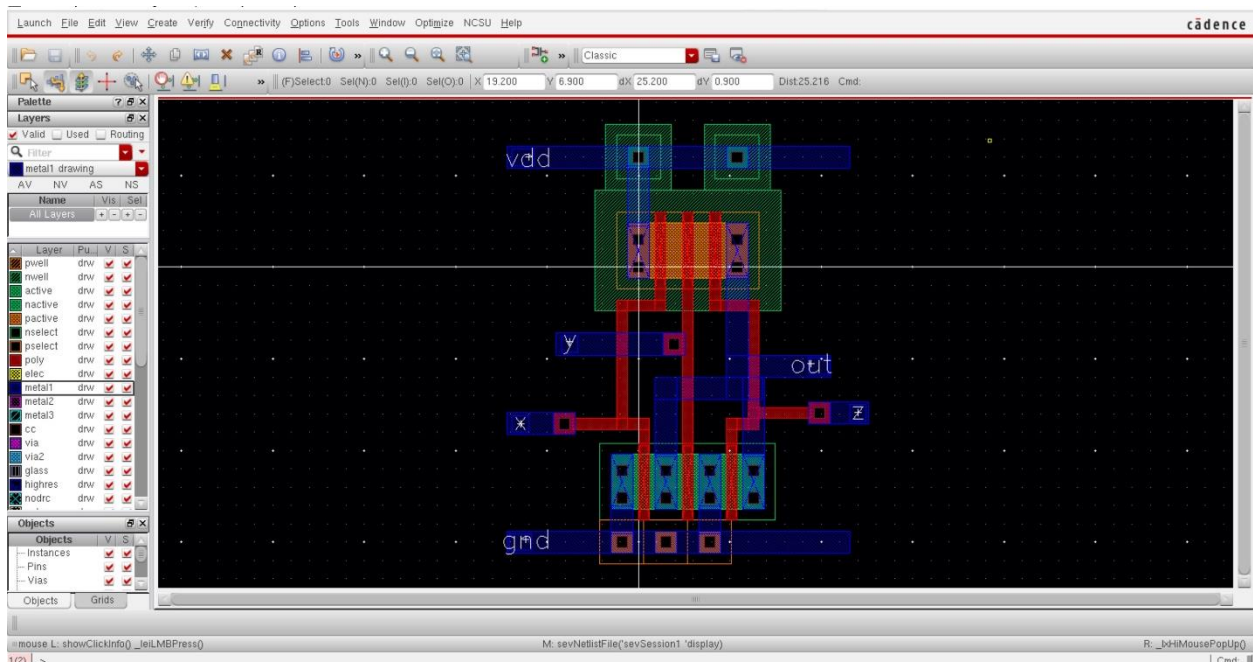


Figure 5: 3-input NOR layout

=====Complex Circuit Layout File=====

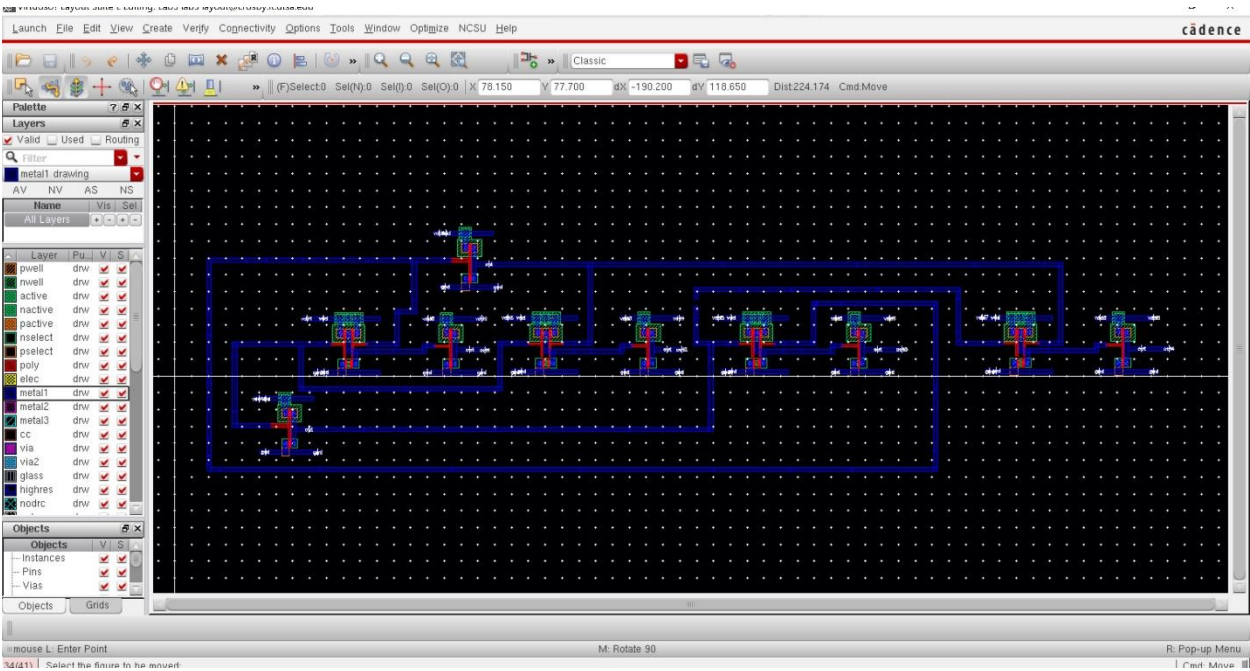


Figure 6: Full Circuit Layout

=====3-input NAND Waveform=====

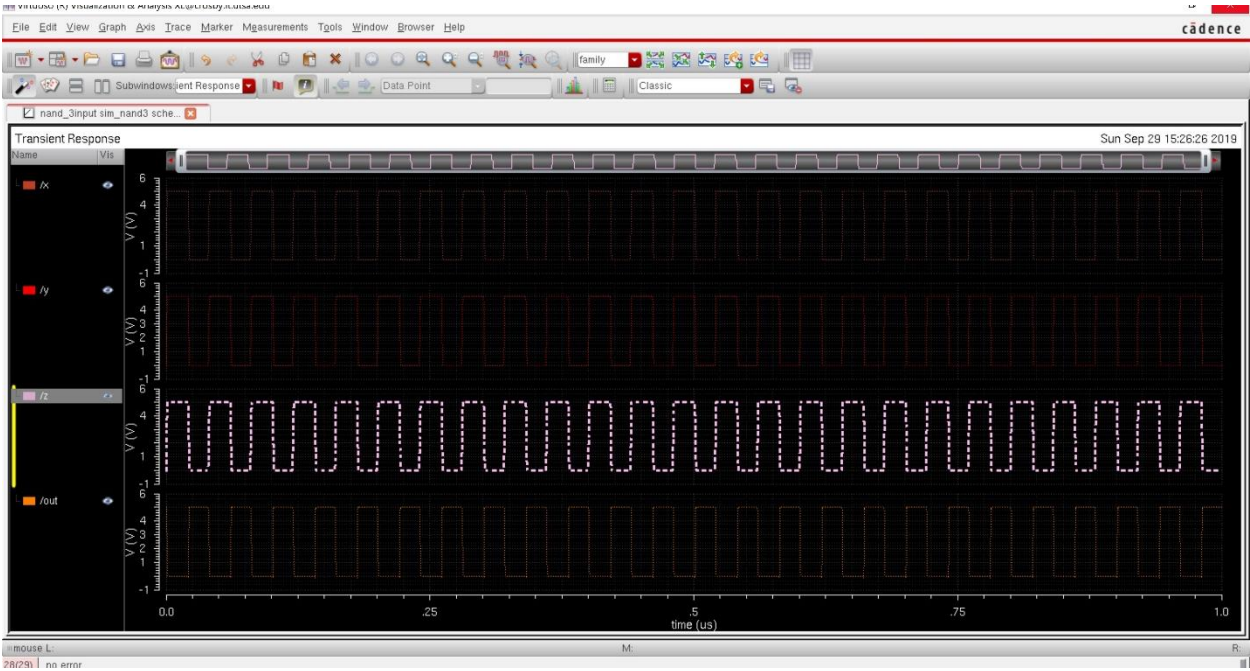


Figure 7: 3-input NAND waveform

=====3-input NOR Waveform=====

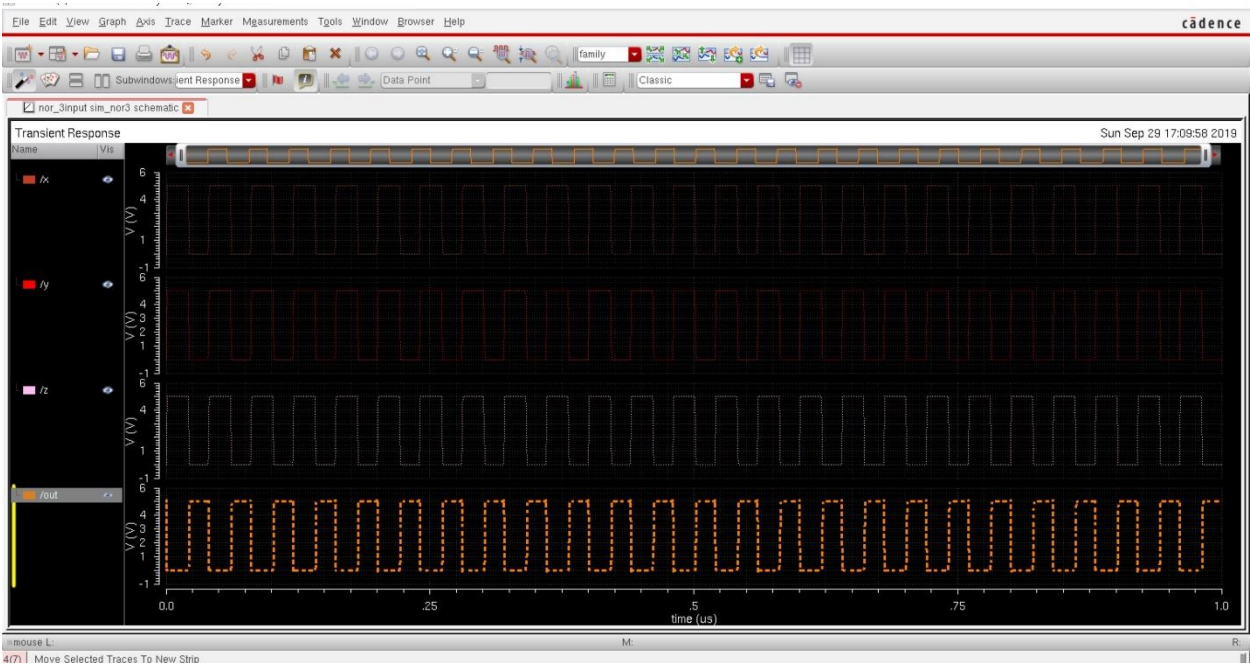


Figure 8: 3-input NOR Waveform

=====Complex Circuit Waveform=====



Figure 9: Full circuit waveform

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1. Neat transistor level circuit schematics of the 3-input NAND gate, 3-input NOR gate and the circuit above, which you will be using to develop your layout. Also, mention the total number of transistors in each circuit.

For the 3-input NAND gate and the 3-input NOR gate, a total of six transistors were required for each circuit.

The complex circuit required a total of 28 transistors to complete.