Fall 2019: EE 4513 Introduction to VLSI Design

Lab 6: Cadence Layout Lab Assignment

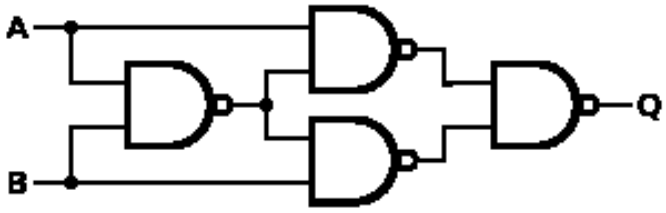
Objective:

To implement the layout of combinational circuits using standard cells and verify their functionality.

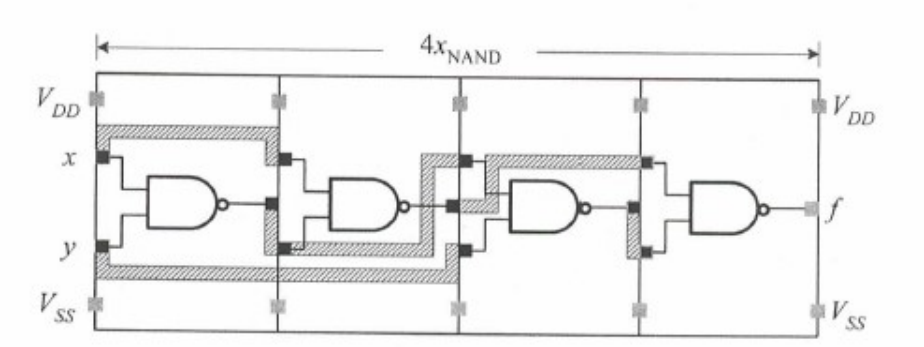
Tasks:

Following are the tasks that you are required to perform:-

1. Create the layout for a 2 input XOR gate using Virtuoso. Use the 2 input NAND cell from your library to create the 2 input XOR cell. Use the diagrams below as a guideline. Verify the functionality of the XOR cell for all input combinations using the built in simulation tool.



NAND- NAND Realization of XOR function



2 input XOR cell constructed from four two-input NAND cells

2. Using the 2 input XOR cell you created in Step 1 and other basic cells from your library, draw the layout for a Full Adder. Verify for functionality.

3. Using 8 such FAs (from Step 2) design an 8-bit adder.

4. Verify the functionality of the 8 bit adder using SPICE for at least four different input combinations. Also indicate the worst-case delay for your layout.

Report:

You should turn in a report containing the following items: -

1. Design approach adopted.
2. Snapshots of layouts and the corresponding simulation waveforms. Also, include the final gate-level schematic for each part mentioned above.