Lab Project (20 points)

Group Assignment: By each board. One report per group. Each student should show their contribution to the project

Due: Tuesday 23rd by end of class. No electronic submission.

20% for the demonstration. 10% delay penalty.

Design a16-bit Arithmetic Logic Unit.

(a) A hierarchical design approach for 16-bit ALU using a Full Adders (16-bit), Multiplier (16-bit), Full Subtractor (16-bit), and shift right A register. You may use the modules developed for prior homework.

Write a top-level module for 16-bit ALU and synthesize your design.

| S0 | S1 | ALU - Operation |
|---|---|---|
| 0 | 0 | Addition |
| 0 | 1 | Subtraction |
| 1 | 0 | Multiplication |
| 1 | 1 | Shift Right |

(b) Write a test bench to verify your ALU design and simulate the waveforms in Xilinx ISE simulator.

(c) Implement the design and download to the FPGA Board. SW switches 1 and 2 should represent S0, and S1. Use SW switch 4 as Reset. GPIO LEDs should be used to indicate the ALU-Operation called.

(d) Store initial values in memory. Display answers in seven-segment display units.

(e) Multiply 16 bit numbers. The answer will be 32-bits.

The report should include the cover page, the problem statement, explanation of your approaches including the reuse of previously developed modules, a block diagram, ASM charts, Verilog codes used, and the waveforms screen-prints. Print both sides of paper. Code font size 10.

State problems encountered at simulation and implementation stages and how they were resolved.