EE5193 FPGA and Verilog HDL

Assignment 2

Due date: Thursday 27th June 2019

1. a. Design an instruction decoder using the gate level constructs and test using Xilinx simulator.
   b. Design and simulate the Behavioral Model for the instruction decoder.
   The report should include the Verilog codes and simulation waveforms for the design.

Mnemonic	Address mode	Op-code[3:0]	Control[13:0]
LDA	Immediate	0000	00_0000_0000_0001
	Memory	1000	00_0001_0000_0000
STA	Memory	0001	00_0000_0000_0010
ADD	Immediate	0010	00_0000_0000_0100
	Memory	1010	00_0010_0000_0000
SUB	Immediate	0011	00_0000_0000_1000
	Memory	1011	00_0100_0000_0000
MUL	Immediate	0100	00_0000_0001_0000
	Memory	1100	00_1000_0000_0000
SWAP	Immediate	0101	00_0000_0010_0000
PAUSE	Immediate	1101	01_0000_0000_0000
JC	Memory	0110	00_0000_0100_0000
JV	Memory	0111	00_0000_1000_0000
JZ	Memory	1111	10_0000_0000_0000

Approach:

a. Generate the truth table for the given inputs and outputs

b. Drawing the K-Maps for the obtained truth tables

c. Gate level implementation for the expressions obtained

d. A test bench

e. Simulation

f. Design the Behavioral model

g. simulate using a test bench.

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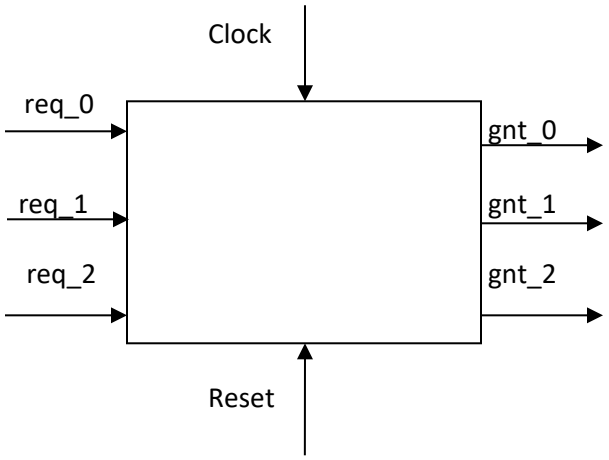
2. Design an arbiter in Verilog and test using Xilinx simulator.
   When only req_0 is asserted, gnt_0 is asserted. Similarly when only req_1 is asserted, gnt_1 is asserted and when only req_2 is asserted, gnt_2 is asserted.
   When both req_0 and req_1 are asserted then gnt_0 is asserted, otherwise when both req_1 and req_2 are asserted then gnt_1 is asserted.
   For all other combinations, gnt_2 will be asserted.
   The arbiter has three inputs and three outputs as shown in the diagram below.



(a) Arbiter circuit

   The report should include the state diagrams, the Verilog codes and simulation waveforms for the design.

You may be requested to demonstrate your work at the time of submission.