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Xzd304

EE 4513 Intro to VLSI Design

EE 4513 – Fall 2019 Lab Assignment #7

Report:

You should turn in a report containing the following items:

1. A description of the layout you created, and any challenges faced.

   The C-Switch took some time to understand before I began creating the layout, I wanted to make sure I understood the design and behavior. What confused me slightly was the diagram in the lab instructions was not correct because the schematic had the pmos and nmos sides on the flipped to the wrong sides, along with the inverter. Once I understood this and the design, I was able to create a working simulation with the right outputs.

   The D Flip-Flop was relatively straight forward, what helped me in the design was to split the design in two parts (latch view) and focus on making the connections in the first part before connecting the second latch side of the D Flip-Flop.

2. Snapshots of layouts and the corresponding simulation waveforms.

Objective:

To learn and implement the layout of simple sequential circuits using standard cells and verify their functionality.

Tasks:

1. Draw the layout of a Transmission Gate (Also known as a C – switch) and verify its functionality.

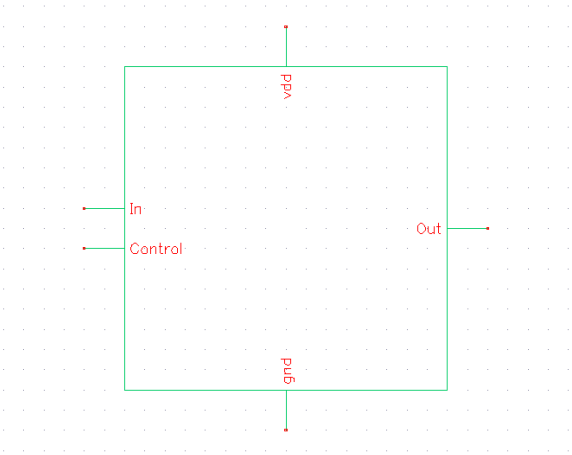

Figure 1: C-Switch Symbol

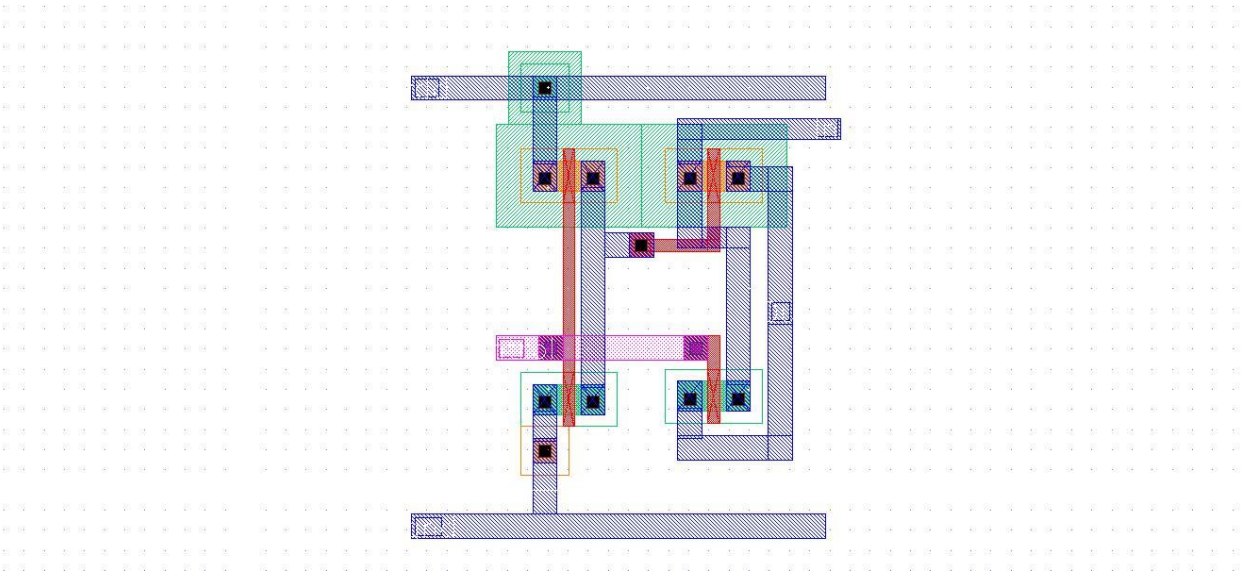

Figure 2: C-Switch Layout

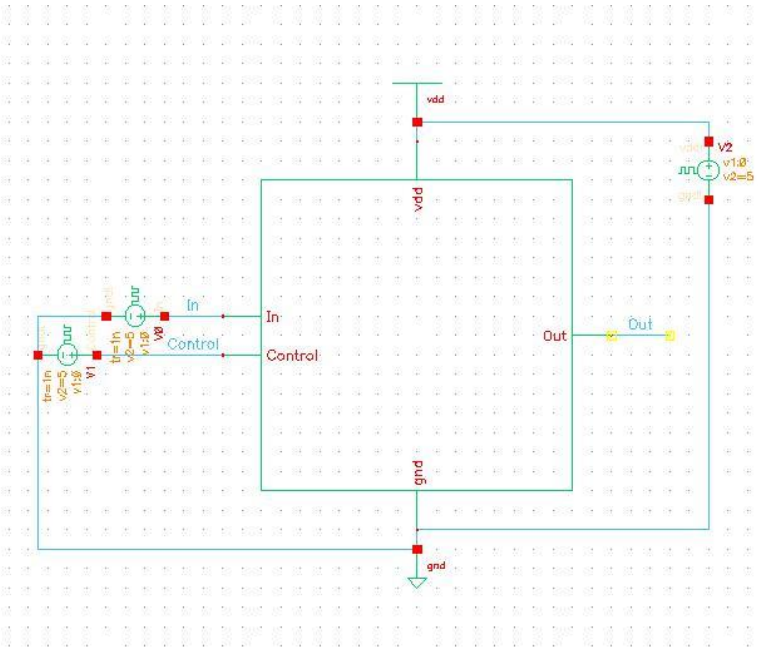

Figure 3: C-Switch Schematic

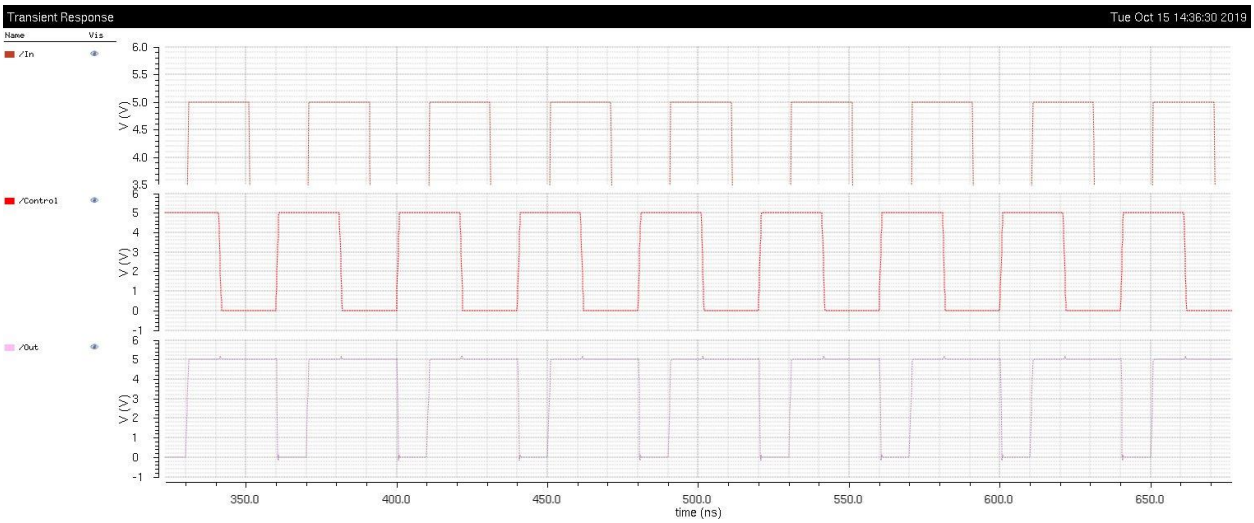

Figure 4: C-Switch Simulation

2. Using C-switches and inverters create the layout of a positive edge triggered D Flip Flop and verify the functionality.

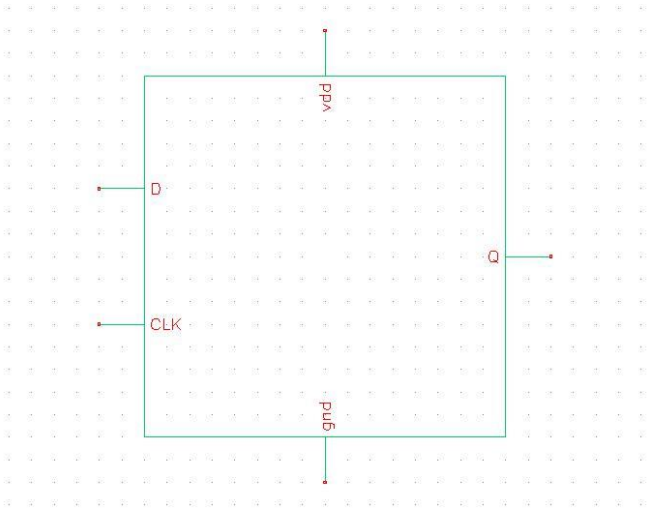

Figure 5: D-FF Symbol

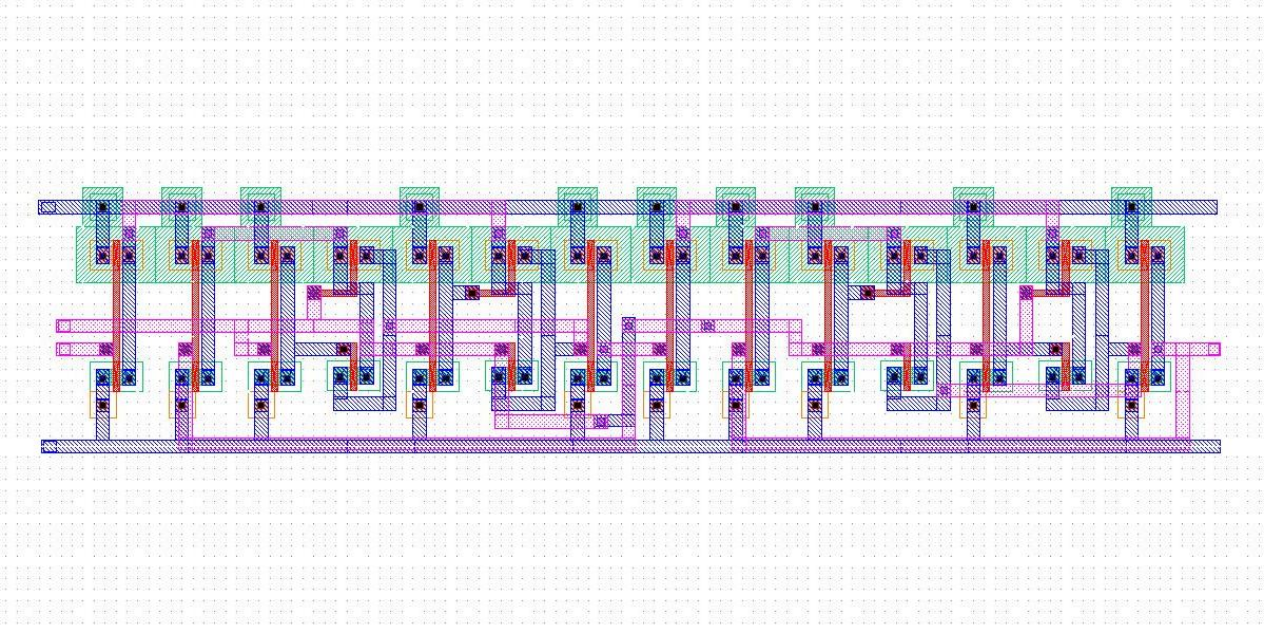

Figure 6: D-FF Layout

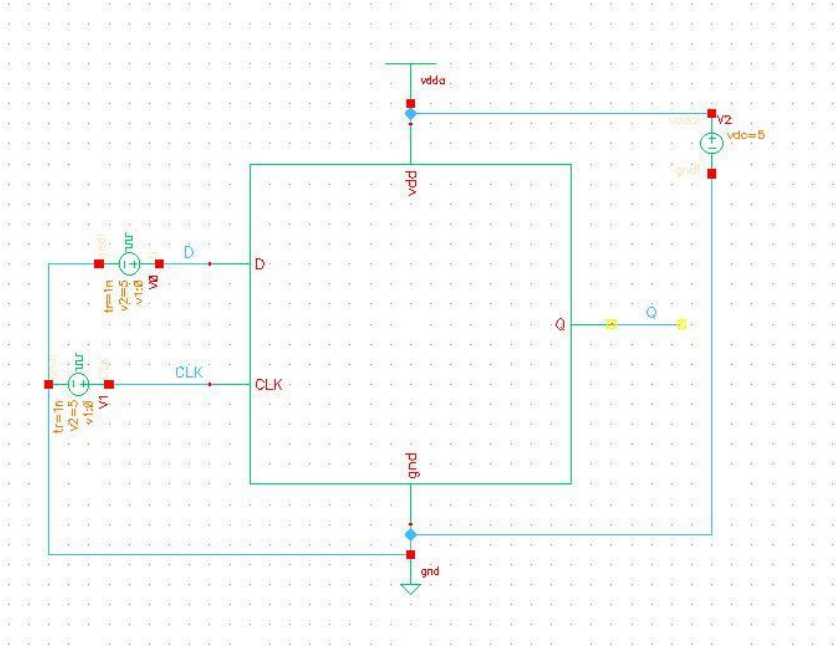

Figure 7: D-FF Schematic

Figure 8: D-FF Simulation