Fall 2019

EE 4513 – Introduction to VLSI Design

Lab Assignment 9

1. Implement the Multiply-Add-Fused (MAF) Functional Unit shown in Figure 1

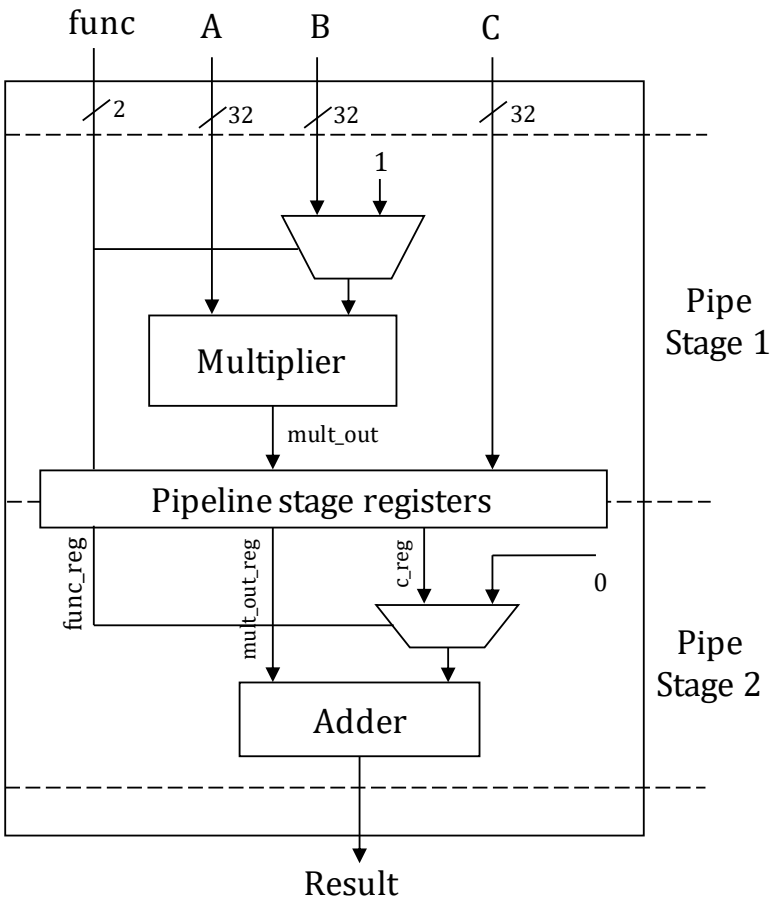

Figure 1: Fused Mult-Add Functional Unit

Table 1: Control signal for function and computation in the pipe stages

Function	Pipe Stage 1	Pipe Stage 2	Desired Output
00	A × B	(A × B) + 0	A × B
01	A × 1	(A × 1) + C	A + C
10	A × B	(A × B) + C	(A × B) + C
11	Don't Care	Don't Care	Don't Care

2. Once you have completed the behavioral simulation (for example, using Xilinx Vivado), synthesize your code to generate the netlist using Cadence RTL Compiler (RC).

3. Then, use the Cadence Encounter platform to generate the schematic and GDS2 layout of your design. Verify your design for connectivity, and geometry violations.

Turn in report, which includes the following: -

1. The directory path (in Linux) where you worked on and created the MAF unit
2. Verilog Code and Simulation waveforms for your MAF unit
3. Physical Layout snapshot of your design
4. Snapshots of portions of the connectivity and geometry verification reports, showing any violations, if present.
5. Schematic of your design (can be seen by clicking Tools -> Schematic Viewer)
6. Report Your Timing Analysis (Slew, Delay, Arrival...etc) and Total Area from your RTL compiler for your design.
7. Snapshot of the message showing successful generation of GDS2 layout
8. Try to optimize your design in the Verilog (efficient /structured code) and post a conclusion for your design.

Note: -

Once you have logged in, you can make a new directory called **lab9hw** using the **mkdir** command (**mkdir lab9hw**) in the terminal. Then change over to the created directory using **cd lab9hw.** Inside this directory, make a new directory called "**maf_unit**" using the **mkdir** command. Use this directory to create the layout of the Verilog module required in this assignment. Provide the path of this directory in the report.