Fall 2019

EE 4513 – Introduction to VLSI Design

Lab Assignment # 10

In this lab assignment,

1. You are required to design: (i) IEEE Single Precision Floating Point Adder.

2. Once you have completed the behavioral simulation (for example, using Vivado), synthesize your code to generate the netlist using Cadence RTL Compiler (RC).

3. Then, use the Cadence Encounter platform to generate the schematic and GDS2 layout of your design. Verify your design for connectivity, and geometry violations.

Turn in report, which includes the following: -

1. The directory path (in Linux) where you worked on and created the FP unit
2. Verilog Code and Simulation waveforms for your FP unit
3. Physical Layout snapshot of your design
4. Snapshots of portions of the connectivity and geometry verification reports, showing any violations, if present.
5. Schematic of your design (can be seen by clicking Tools -> Schematic Viewer)
6. Report Your Timing Analysis (Slew, Delay, Arrival...etc) and Total Area from your RTL compiler for your design.
7. Snapshot of the message showing successful generation of GDS2 layout
8. Try to optimize your design in the Verilog (efficient /structured code) and post a conclusion for your design.

Note: -

1. Once you have logged in, make a new directory called **lab10**. For example, if your account is abc.123, then upon login you will be taken to a directory with the same name. This is **your** home directory (not to be confused with another directory with the name 'home'). To view the path of this directory, use the 'pwd' command. Then make the 'lab10' directory by using the **mkdir** command (**mkdir lab10**). Then change over to the lab10 directory using **cd lab10.** All the files related to this assignment should be in this directory. You must use the same names as mentioned here.
2. In your report, you should clearly mention the file names that you choose for the various reports that are generated (verification, GDS2 etc.) while using Encounter.