NG-MEDIUM SPACE

NX1H35AS
Datasheet

V1.0.12

July 2025

Table of Content

1 Important information

This datasheet applies exclusively to the NG-MEDIUM FPGA referenced **NX1H35AS**.

For previous silicon versions (NX1H35S), please refer to the previous datasheets versions.

2 Summary

Radiation Tolerance

- Radiation hardening by design in configuration memories and registers.
- SEL immune up to LET > 60MeV.cm^2/mg.
- Device Configuration SER < 1.70 10^{-4}/day (GEO)
- Total ionizing dose > 100Krads.
- Embedded EDAC for user memory mitigation.
- Embedded configuration memory scrubbing.
- Fast automatic memory configuration repair.
- Embedded bitstream integrity check (CMIC).

Main Features

- 65 nm STm C65-SPACE process technology.
- 4-Input Look-up tables.
- Lut expender to support up to 16 bits boolean functions.
- High performance carry chains.
- Advanced interconnect network to support random logic and coarse grain block functions.
- DSP Blocks for complex arithmetic operations.
- User memories with variable width and depth.
- 5 configuration modes: JTAG, Parallel 8 bits, Parallel 16 bits, Serial dump bus, Space Wire.
- Integrated Space Wire interface available for user applications.
- Dedicated lowskew distribution network for clock, reset and load enable signals.
- On-chip thermal monitoring capability.

Input / Output Features

- Multiple I/O powering support from 1.8V to 3.3V
- Cold sparing support.
- Programmable output drive to support multiple industry standards.
- Embedded logic to support DDR2 and DDR3.
- 800 Mbps I/O support.
- LVDS compatible mode.
- All pins support 2000V of ESD-HBM.
- Embedded logic to support Space Wire Data Strobe encoding.
- Programmable delay lines on all pins.
- Programmable resistive termination.

3 Features

The NG-MEDIUM device (NX1H35AS) is a Radiation Hardened By Design Sram-based FPGA manufactured on STM C65 Space process with following resources.

3.1 Resources

Device	NX1H35AS
Capacity	
Equivalent System Gates	4 400 000
ASIC Gates	550 000
Modules	
Register	32256
LUT-4	34272
Carry	8064
Embedded RAM	-
Core RAM Blocks (48K-bits)	56
Core RAM Bits (K = 1024)	2688 K
Core Register File Blocks (64 x 16-bits)	168
Core Register File Bits	116 K
Embedded DSP	112
Clocks	24
Embedded Serial Link	
SpaceWire 400Mbps	1
I/Os	
I/O Banks	13
User I/Os	-
LGA-625 & CGA-625	374
CQFP-352	192
FG-625	374
I/O PHYSICAL INTERFACES	-
DDR/DDR2	16
SpaceWire	16

3.2 Electrical Specifications

Symbol	Parameter	Value	Units
V_{core}	Nominal core voltage	1.2	V
VDDIO	Nominal I/O voltage	1.8 or 2.5 or 3.3	V
VDD2V5A	Nominal auxiliary analog voltage	2.5	V

3.3 Operating Conditions

Parameter	Value	Units
Temperature Range	-55 to +125	°C
Power Supply Tolerance	±10	%V_{cc}

3.4 Radiation Performance

All resources are protected against radiation.

- Configuration Memory Cells are built with dedicated RH layout to guarantee a very low probability of soft-errors,
- User Register and DFF are also built with RH layout,
- Register files and Embedded Dual-Port RAM are protected with ECC.
- Clock tree has double redundancy
- Remaining critical logic blocks are triplicated.

Hereafter Orbital upset rates calculated with I96 (Solar min, 100mils shielding, 2µm sensitive volume thickness),

Total Ionizing Dose	100Krads Tested up to 300Krads
Heavy ions Latch Up susceptibility @ 125°C, 1.32V	LET > 60MeV.cm^2/mg
Configuration Memory SEU @ 25°C, 1.08V	GEO SER < 2.1 10^{-4}/day/device LEO SER < TBD
Embedded RAM + EDAC SEU/SET @ 25°C, 1.08V	GEO SER < 2,16 10^{-11}/day/bit LEO SER < 2,20 10^{-12}/day/bit
DFF SEU/SET @ 25°C, 1.08V	GEO SER < 1.80 10^{-9}/day LEO SER < 1.22 10^{-14}/day
Bitstream Management SEFI @ 25°C, 1.08V	GEO SER < TBD LEO SER < TBD

On top of that, even the SER's versus various orbits are very low, the bitstream is verified with an integrated scrubber controller named CMIC.

3.5 Configuration

The NX1H35AS are configured by loading the bitstream into internal configuration memory using one of these following modes:

- JTAG,
- Slave Parallel 8bits, 16bits
- Slave SpaceWire, compliant ECSS-E-ST-50-12C link,
- Master SPI, compliant with SPI JESD68.01,
- Master Dump.

Hereafter the NG-MEDIUM configuration modes table:

MODE[3:0]	CLK	Configuration mode
0b0000	Internal OSC	Master Serial
0b0001	Internal OSC	JTAG Only
0b0010	Internal OSC	Master SPI
0b0011	Internal OSC	Master SPI + Vcc
0b0100	Internal OSC	Slave Spacewire
0b0101	Internal OSC	Reserved
0b0110	Internal OSC	Slave Parallel 8
0b0111	Internal OSC	Slave Parallel 16
0b1000	External	Master Serial
0b1001	External	Reserved
0b1010	External	Master SPI
0b1011	External	Master SPI + Vcc
0b1100	External	Slave Spacewire
0b1101	External	Reserved
0b1110	External	Slave Parallel 8
0b1111	External	Test Mode

Table 1: Configuration mode

When MODE[3]='0', a 50MHz internal oscillator is used as Bitstream Manager clock. Otherwise, user must provide an external clock.

MODE pins must be static and changed only when RST_N is asserted.

JTAG is always usable but can be used for memory configuration only in slave modes (all but Master Serial / Master Serial SPI / Master Serial SPI + Vcc modes).

This NX1H35AS bitstream size depends on the application size (configuration) and the number of user Core RAM and Core Register File to be initialized.

Maximum configuration[1] (100%):	6.735Mb
Medium configuration[1] (70%):	4.714Mb
Small configuration (50%)	3.367Mb
D-Flip-Flop initialization (32 256):	0.033Mb (1.02b/DFF)
Core RAM initialization (56):	5.505Mb (98.30Kb/RAM)
Core Register File initialization (168):	0.258Mb (3.07Kb/2RFB)
Configuration Memory Integrity Check:	0.022Mb

The maximum bitstream size is 6.735 + 0.033 + 5.505 + 0.258 + 0.022 = 12.553Mb

Most applications do not require to initialize all instances. A typical bitstream is less than 8Mb.

[1] These figures are just estimations. The actual size can be determined only by running the mapping software.

3.6 Configuration Memory Integrity Check (CMIC)

The CMIC is an embedded engine performing automatic verification and repair of the configuration memory.

A CMIC reference memory is initialized during the bit stream download process with reference data computed by the software.

Once the initialization is done, the CMIC engine can be periodically activated to perform the following sequence:

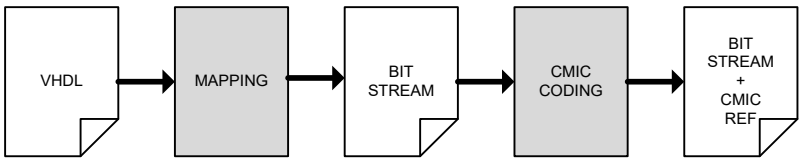
1. Read configuration data
2. Calculate signature
3. Compare the signature with CMIC reference
4. If a mismatch is detected:
    a. Calculate faulty address (BAD @) and faulty bit location
    b. Read DATA[BAD @]
    c. Repair flipped bit
    d. Write DATA[BAD @]

The CMIC period can be set by the user. The minimum period is 5.3 ms and the maximum 65 days. The configuration memory scan takes 4ms.

The CMIC reference memory is protected by ECC.

The CMIC does not need to access the external NVRAM when performing checks and repairs at run time. When a faulty bit is detected, the repair process is launched automatically and a notification signal is generated. This signal can be used by external means to manage this situation at system level.

CMIC Reference Generation



When the bit stream is downloaded from an external NVRAM, the bit stream data is sent to the configuration memory and the CMIC reference data is stored in special RAM protected with ECC.

4 Functional Description

4.1 Device Architecture

The NG-MEDIUM FPGA (NX1H35AS) is based on NanoXplore patented interconnect architecture offering the highest logic density as well as high efficiency mapping. Application mapping is supported by NanoXplore tools based on proprietary algorithms tailored to the interconnect topology.

The device is composed of a central fabric embedding the programmable logic, RAM and DSP blocks, and peripheral I/O buffers. The fabric is covered with a grid of high level functional blocks interleaved with interconnect structures providing routing resources to realize the connections within the fabric and to the peripheral I/O buffers. The programmable logic resources are arranged in a hierarchical structure called a TILE with a specific local interconnect network. The I/O buffers are arranged into multiple banks. Each bank has its own I/O buffer supply voltage.

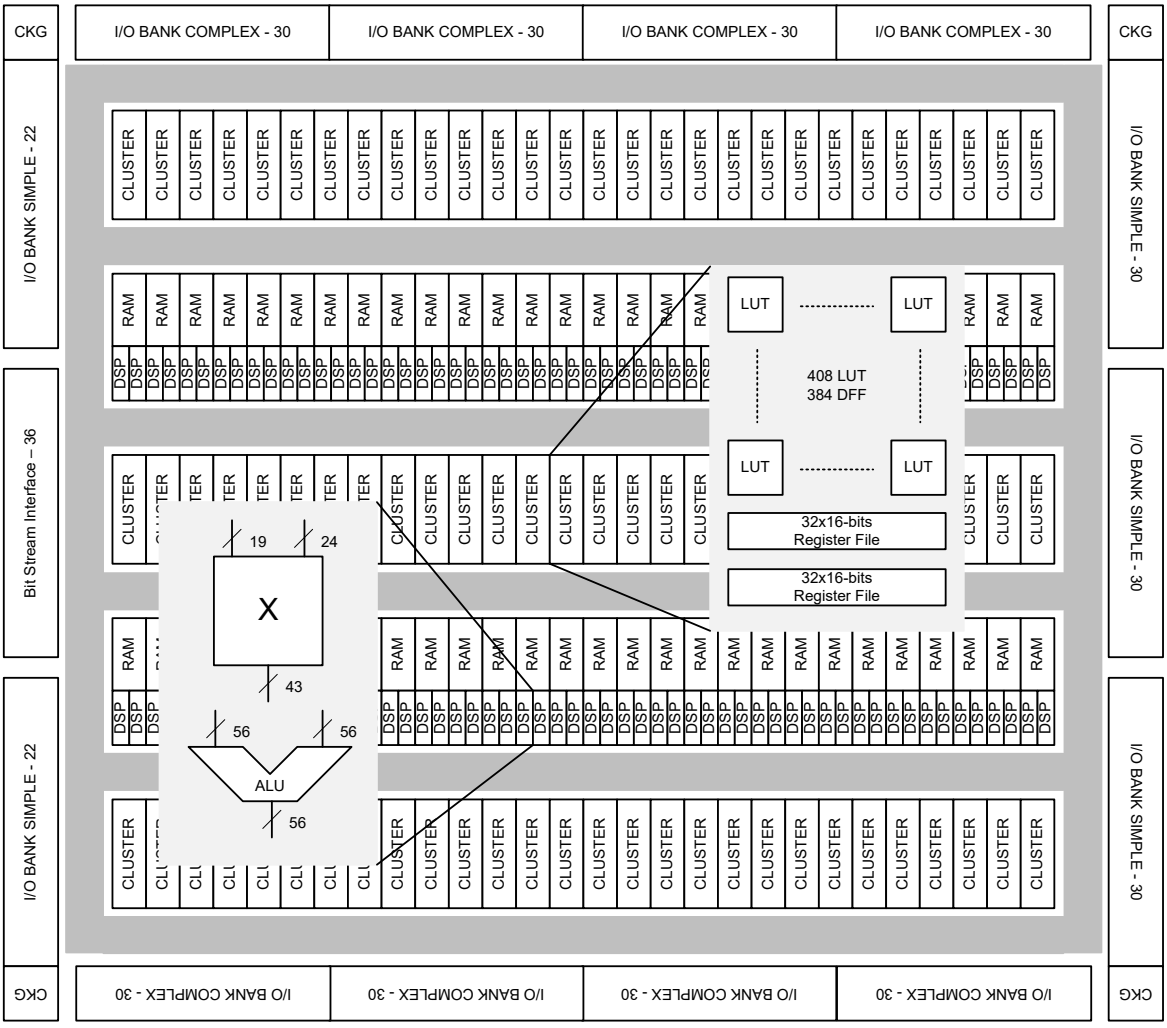


Figure 1: Device Floor Plan

NX1H35AS die features :

- 5 “Simple” I/O Banks B0, B1, B6, B7 and B8
- 8 “Complex” I/O Banks B2, B3, B4, B5, B9, B10, B11 and B12
- 1 “Service” configuration bank Prog
- 4 PLL clock generators CG0, CG1, CG2 and CG3

- LUTs
- Flip-flops
- 36 Kbit internal RAM blocks
- DSPs

4.2 Device Features

4.2.1 TILE

384 LUT
24 X-LUT
96 Carry Logic
384 DFF
2 Register File 64*16bits

Table 2: TILE logic resources

4.2.1.1 LUT & DFF

The random logic is implemented with 4 inputs look up tables (LUT). The LUT output signal can be optionally stored in a register (Figure 2). The terminals I1, I2, I3, I4, and OUT are connected to the TILE interconnect network. The inputs RST, LE, CLK1, CLK2 SYS1 and SYS2 are connected to the TILE low skew network.

To support wide boolean equations, a group of four LUT can provide four inputs directly to a fifth X-LUT without routing through the interconnect network (Figure 3). One TILE contains 384 LUT and 24 X-LUT.

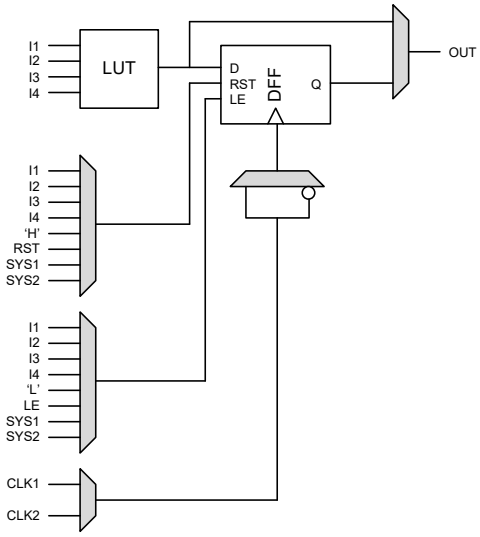


Figure 2: LUT and DFF Diagram

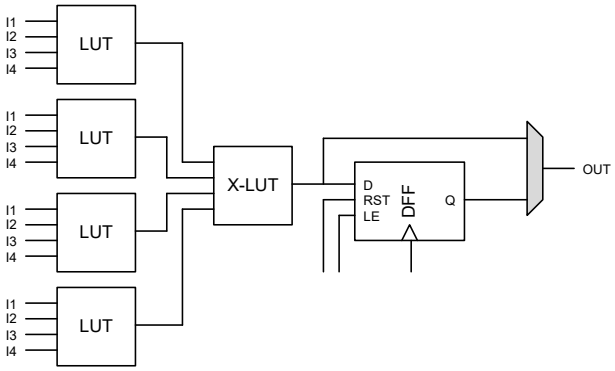


Figure 3: X-LUT and DFF Diagram

Four inputs and one output truth table • realizes any 1 to 4-inputs Boolean function
X-LUT Configuration • realizes up to 16-inputs Boolean function
Optional register on output • 1 bit edge sensitive flip-flop (DFF) • Programmable synchronous / asynchronous reset • Programmable positive / negative clock edge • Programmable Load enable
DFF Initialization by bit stream

Table 3: LUT & DFF Features

4.2.1.2 Carry Logic

Arithmetic operators requiring a carry propagation can be implemented with a hard wired carry logic. In order to accelerate the carry propagation through wide operators, a 4-bits carry look ahead circuit is added in the carry propagation path. Versatile arithmetic operators can be implemented by combining the carry logic with LUT and DFF.

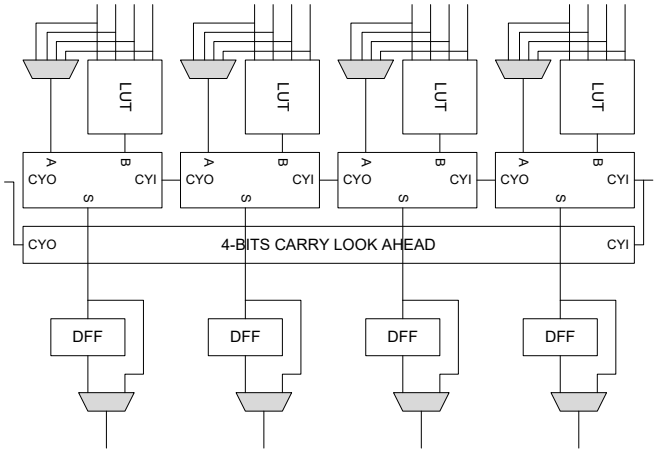


Figure 4: Carry Chain Diagram

Combines one LUT with carry propagation logic
Fast 4 bits carry look ahead acceleration
Up to 96 bits chains

Table 4: Carry Logic Features

4.2.1.3 Register File

Small memory blocks can be implemented with a 64 x 16-bits register file array. It is inserted between the LUT and DFF. The DFF can be bypassed or used as an optional output pipe line register. The inputs CLK1 and CLK2 are connected to the TILE low skew network.

A hardware SECDED EDAC function generates the ECC bits on the input port and performs error correction and detection on the output port. The EDAC bits are stored in extra memory bits which are not accessible to the user application.

Synchronous Simple Dual Port SRAM
64 x 16-bits words
One synchronous read only port
One synchronous write only port
Optional pipe-line output register
Programmable positive / negative clock edge
Initialization by bit stream
Embedded SECDED EDAC

Table 5: Register File Features

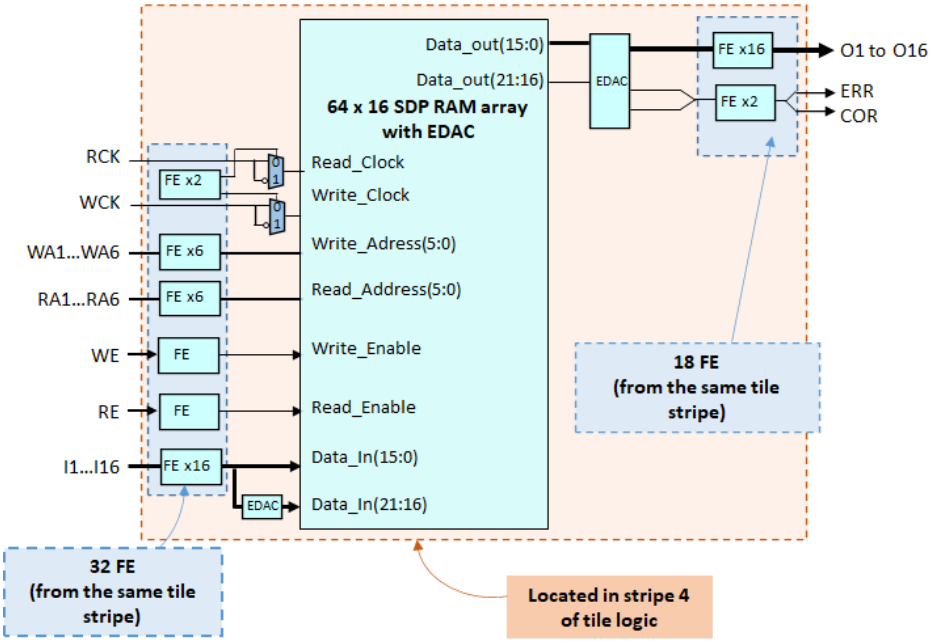


Figure 5: Register File simplified diagram

4.2.2 Memory

The memory block is a true dual-port synchronous 48K-bits SRAM. The memory is configurable and supports various modes of operation. Each port can perform a read or write operation. The data can be protected by a hardware SECDED EDAC. This EDAC function can be bypassed. The ECC signature is computed during the write cycle and checked during the read cycle.

An optional feature is the Read Repair mode. When this mode is enabled and a correctable error is detected during the read cycle, then the memory array is updated with the corrected data/ECC value.

With EDAC: • 2048 x 1-bit • 2048 x 2-bits • 2048 x 6-bits • 2048 x 9-bits • 2048 x 18-bits
Without EDAC: • 49152 x 1-bit • 24576 x 2-bits • 12288 x 4-bits • 6144 x 8-bits • 1024 x 12-bits • 2048 × 24-bits
Programmable positive / negative clock edge
Optional pipe-line output register
Initialization by bit stream
Embedded EDAC
Automatic repair mode

Table 6: Memory Features

Read Cycle:

When the memory is enabled in a memory read cycle (CSx = 1 and Wex = 0), the address is stored on the rising memory clock (CLKMEMx) edge, and data appears at the output bus after the access time. The chronogram is shown on the Figure 6. The optional output pipeline registers are available in all memory configurations. These registers are clocked by CLKREGx signals, which may be different from the main memory clock signals CLKMEMx. The memory pipeline register may be forced to zero by asserting the synchronous RSTx signal. Both memory clocks and register clocks may have individually configured polarity. The presence of output pipeline registers is determined independently for each port.

Write Cycle:

When the memory is enabled in a memory write cycle (ENBx = 1 and WEx = 1), the address is stored and data is written to the memory on the rising edge of the memory clock (CLKMEMx). **During a write access DOUT maintains the output previously generated by a read operation.**

Note: Simultaneous write by both ports of a same memory location or simultaneous read/write are not allowed.

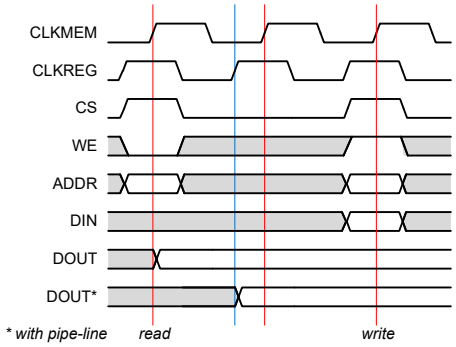


Figure 6: Read and Write Timings

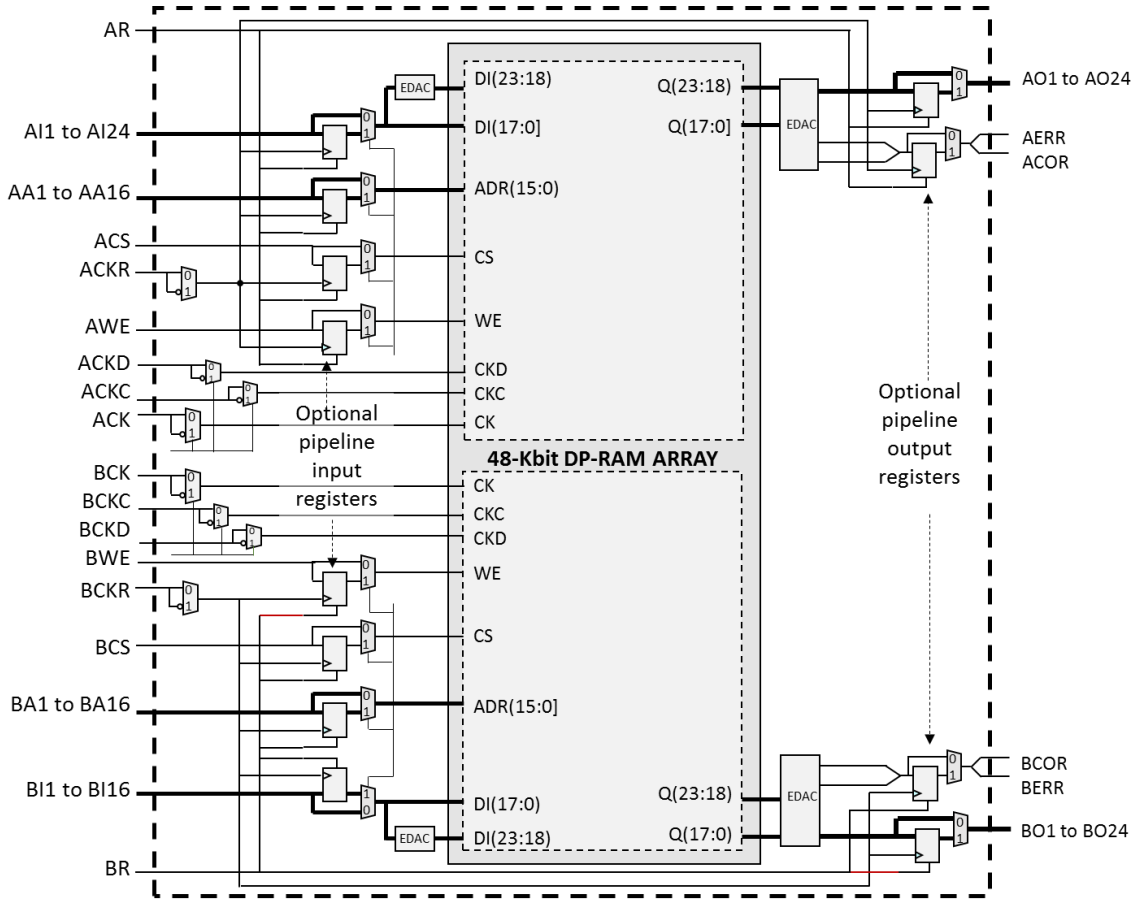


Figure 7: RAM block simplified internal diagram

4.2.3 DSP

The DSP can implement arithmetic computations such as multiply, multiply-add/subtract, multiply-accumulate, and arithmetic wire shift for higher precision calculation. The ability to cascade multiple DSP allows for users to achieve high performance algorithms such as FIR with a minimum of fabric resource usage.

A single DSP (Figure 8) has a 19×24 multiplier, a 56-bit arithmetic unit (ALU), an 18-bit pre adder (ADD) and several pipe-line registers (PR). Two adjacent DSP can be combined to support 24 x 24 multiplications. The DSP can be configured to operate in unsigned or signed mode. When in signed mode, all operands format is two's complement format.

19x24 signed / unsigned multiplier
56-bit arithmetic and logic unit
18-bit pre adder (19-bit result)
Programmable Pipeline stages
Possibility to cascade up to 56 DSP blocks
Support for Higher order 24x30 multiply
Signed (two's complement) or unsigned mode
Among Single DSP operations: • 18 x 24-bit Multiplication: Z[35:0] = A[23:0] x B[17:0] • 18 x 24-bit Multiplication and Addition: Z[55:0] = A[23:0] x B[17:0] + CZI[55:0] • 18 x 24-bit Multiplication and 56-bit Accumulation: Z[55:0] = (A[23:0] x B[17:0]) + CZO • 18-bit Pre-adder, Multiplication and 56-bit adder Multiplication and Addition with Pre-adder: Z[55:0] = A[23:0] * (B[17:0] + D[17:0]) + CZI[55:0] •
Among Multi DSP operations at full speed (~300 MHz) • 24 x 30-bit Multiplication (2 DSP blocks) Z[47:0] = A[23:0] * B[29:0] • 18 x 18-bit complex multiplier (4 DSP blocks) • Parallel N-tap FIR filter – non symmetric : N x DSP block • Parallel N-tap FIR filter – symmetric : N/2 DSP blocks

Table 7: DSP Features

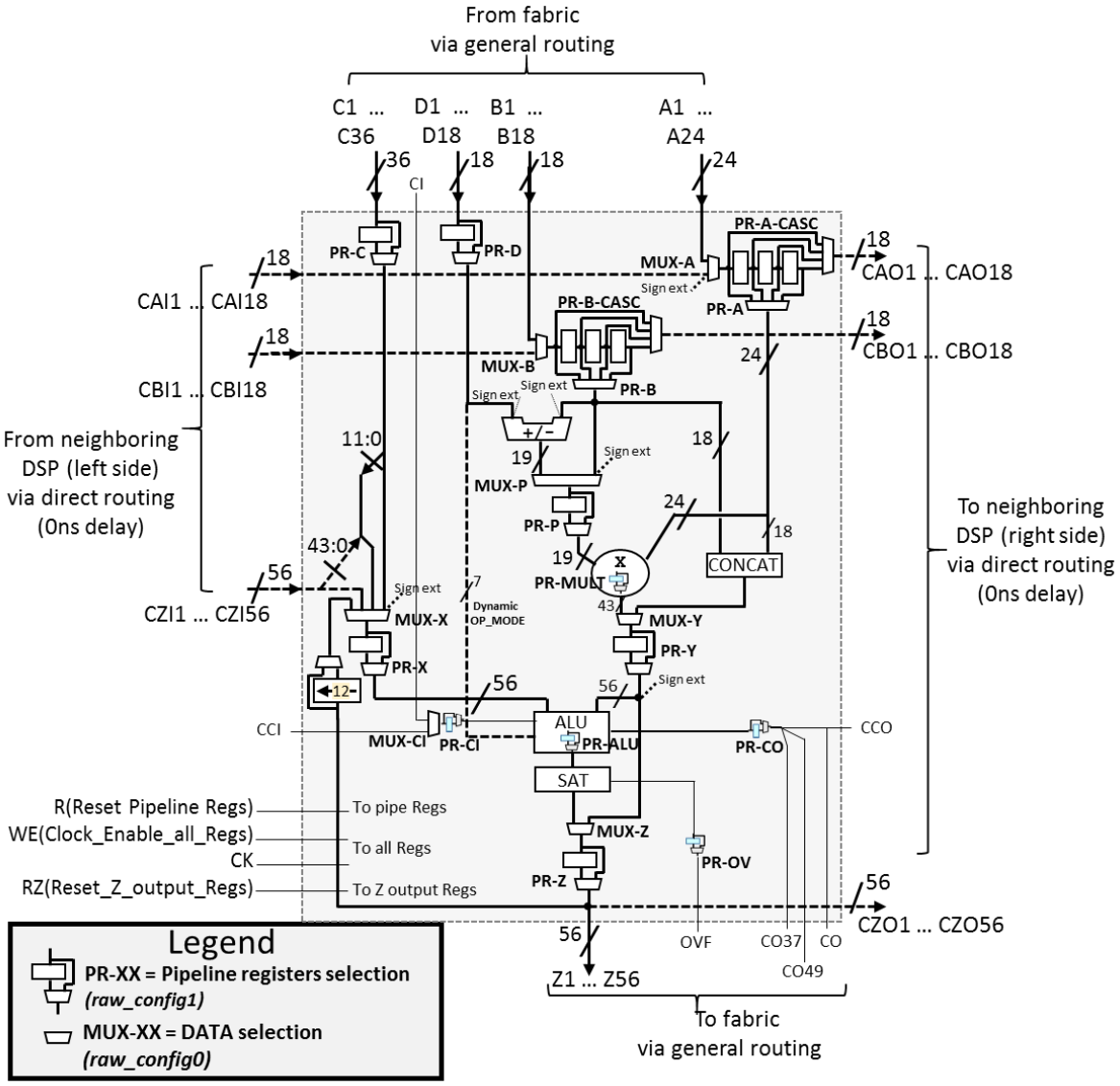


Figure 8: DSP simplified diagram

4.2.4 I/O Buffer

There are two types of I/O buffer: complex and simple.

An I/O buffer (IOB) provides input, output, and bidirectional interfaces. Each IOB can be configured to meet various voltage, current, and impedance configurations and supports cold sparing. The input and output path logic can be configured to provide various data and clocking interfaces with the fabric. Two adjacent IOB can be paired to form a differential buffer.

In complex I/O, a programmable resistor network provides both on-chip termination connected to an external voltage VTO, or a differential resistive termination between two paired IOBs.

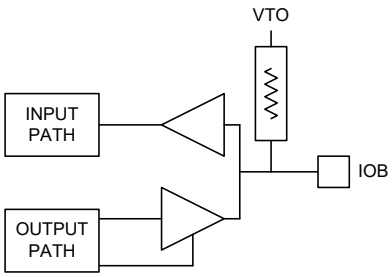


Figure 9: Single Ended complex IOB

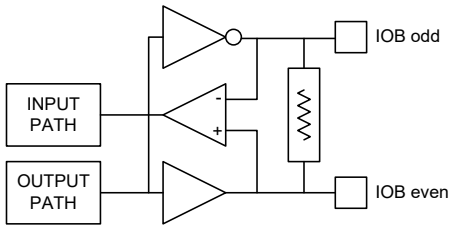


Figure 10: Differential complex IOB Pair

NX1H35AS user I/Os are assembled in pairs P/N. Each pair may be used as either a true differential signal or two unipolar signals.

NX1H35AS devices I/O banks support I/O standards as listed in Table 8.

Standard	Supply	Drive	Turbo	Max freq MHz or Mb/s	Special considerations	Notes
LVCMOS 3.3V	3.3 V	2–16 mA	Yes/No	200MHz		
LVCMOS 2.5V	2.5 V	2–16 mA	Yes/No	300MHz		
LVCMOS 1.8V	1.8 V	2–16 mA	Yes/No	300MHz		
SSTL 2.5V – I/II	2.5 V	8 mA / 16 mA	Yes/No	600Mb/s	Controlled Source Impedance	DDR
SSTL 1.8V – I/II	1.8V	8.6 / 13.4 mA	Yes/No	800Mb/s	Controlled Source Impedance	DDR

Standard	Supply	Drive	Turbo	Max freq MHz or Mb/s	Special considerations	Notes
HSTL 1.8V – I/II	1.8 V	8 / 16 mA	Yes	800Mb/s	Controlled Source Impedance	DDR
HSTL 1.8V – I/II	1.8 V	8 / 16 mA	No	400Mb/s	Controlled Source Impedance	DDR
LVDS 2.5V	2.5 V	3.5mA		800Mb/s		DDR

Table 8: IO Buffer Standard List

Each buffer has programmable delay lines on their input and output paths and can be combined with a register, shift registers and a CDC function to provide various types of data interface and clocking modes with the FABRIC. The following schematics illustrate the output, input and termination interfaces. The programmable delay line is used to align incoming or outgoing data with the external clocking environment and can be bypassed.

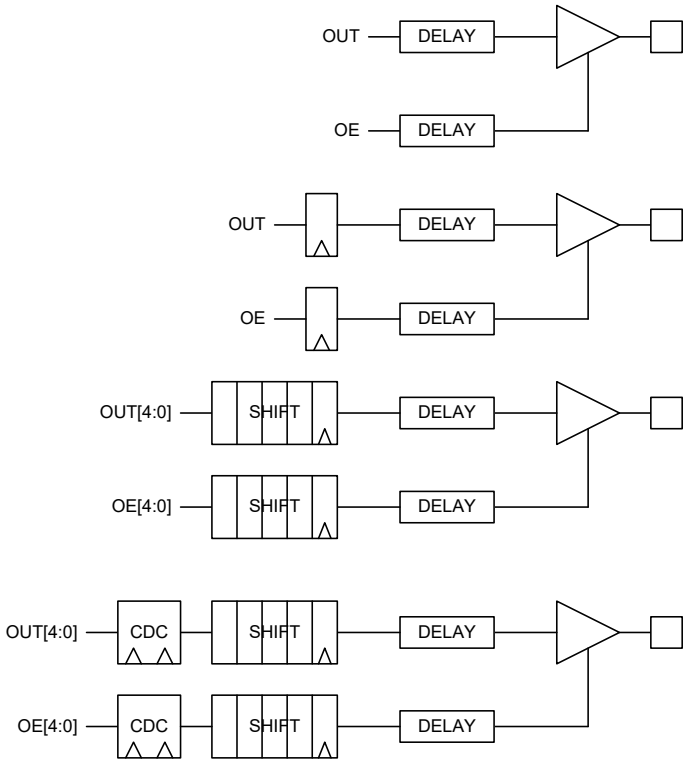


Figure 11: Output Path

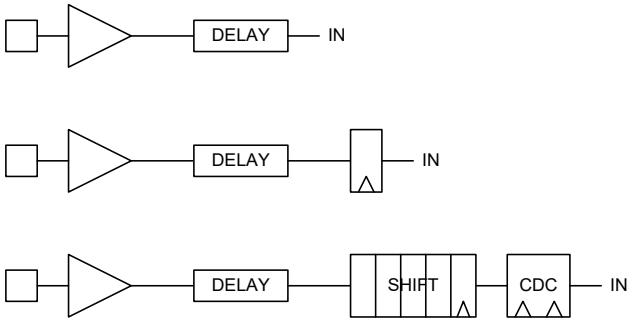


Figure 12 : Input Path

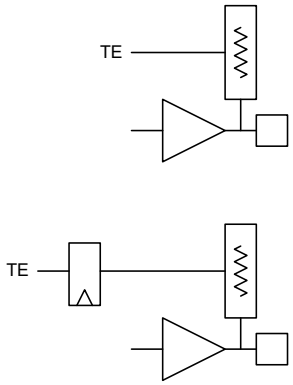


Figure 13: Termination Path

Programmable strength
Supports multiple voltage levels (1.8V – 3.3V)
Single ended operation
Differential operation
Programmable slew rate
Programmable pre-emphasis
Programmable resistive termination
External termination voltage
Programmable input level
Programmable input delay line
Programmable output delay line
Termination-enable control
Input register
Output register
Output-enable register
Termination-enable register

Table 9: IO Buffer Features

4.2.4.1 On-chip resistive termination

The programmable on-chip resistive termination network in a complex IOB is controlled through 4-bits control signal. This 4-bit value is assigned to the IOs within a NXpython script file for each IO requiring internal input impedance adaptation.

It can be used for both single-ended and differential input/output signals. Table 10 presents minimum and maximum resistance values at given VDDIO voltage when on-chip termination is activated.

In single-ended mode, the VTO pads of the IO banks using internal impedance adaptation must be connected to an external VTO voltage. VTO must be nominally set at VDDIO/2 and can be adjusted according to the range listed Table 11.

In differential termination mode, or if termination resistors are not used, VTO pads may be left unconnected.

	Code max [1111]		Code min [0001]	
VDDIO	**$Rtmax_{min}$ (Ω)**	**$Rtmax_{max}$ (Ω)**	**$Rtmin_{min}$ (Ω)**	**$Rtmin_{max}$ (Ω)**
1.8 V	78	92	31	33
2.5 V	92	108	34	38

Table 10 : On-chip termination resistance min and max values vs. VDDIO

Notes: Rtmin and Rtmax values cover ±10% variations on VDDIO, VTO and VDD2V5 supply voltages, -40 to 125C° temperature variations. Non-silicided poly resistance variations defined by foundry design rules are not taken into consideration.

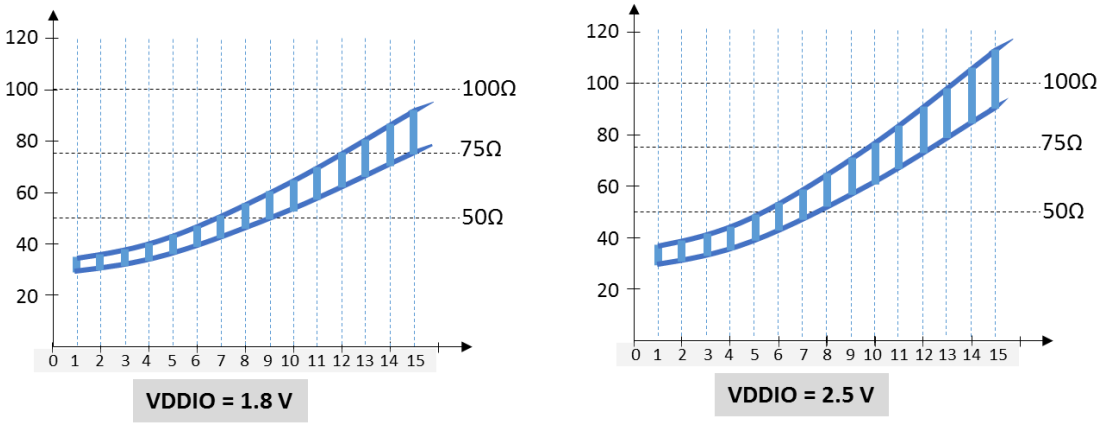


Figure 14: Impedance adaptation resistor values

VDDIO	VTO nom
1.8 V	0.9 V +/-5%
2.5 V	1.25 V +/-5%

Table 11: VTO range vs VDDIO

For VDDIO 1.8 V, on-chip termination can be activated for all pads in a given bank. In case of VDDIO 2.5 V, on-chip termination can be activated on maximum 11 due to the limitation on power supply rails.

4.2.4.2 Delay line

The delay lines are PVT compensated. Through calibration, maximum reachable delay is approximately between 7.3ns and 20 ns, where delay step of the 64-bits delay line varies approximately between 110ps and 310ps.

However, the delay step is set by default to 160 ps.
Accuracy of the delay tap is +/- 2% for the worst case.
The delay line can be bypassed.

The delay lines are PVT compensated and provide a programmable delay range with 64 steps of 160ps.

4.2.4.3 Weak Termination

By default, each I/O pad has a 30 KΩ pull-up with a precision of +/- 10KΩ. In addition, each user's I/Os can optionally have an additional 4KΩ with a precision of +/-2KΩ with the option Weak Termination set to Pull up. No pull-down or keeper is available on NG-MEDIUM I/Os.

4.2.4.4 Pre-Emphasis and Slew-rate control

Edge boost (pre-emphasis) mode can accelerate rising and falling edges up to 25% while stepped activation (slew control) mode can slow down by up to 40 % (Test case: half drive strength, 100MHz output, 6pf of load). It has to be noted that these numbers depend strongly on the chosen drive strength and the driven load. In the software, the user can set the output buffer to: "slow", "medium" or "fast".

4.2.5 IO Bank

An I/O Bank is composed of several IOB and supply pins forming a homogeneous structure sharing:

- A same IO power supply VDDIO
- A same resistive termination supply VTO (Only in complex IOB)

There are two types of IO banks with different functionalities detailed in

Table 12: Simple and Complex.

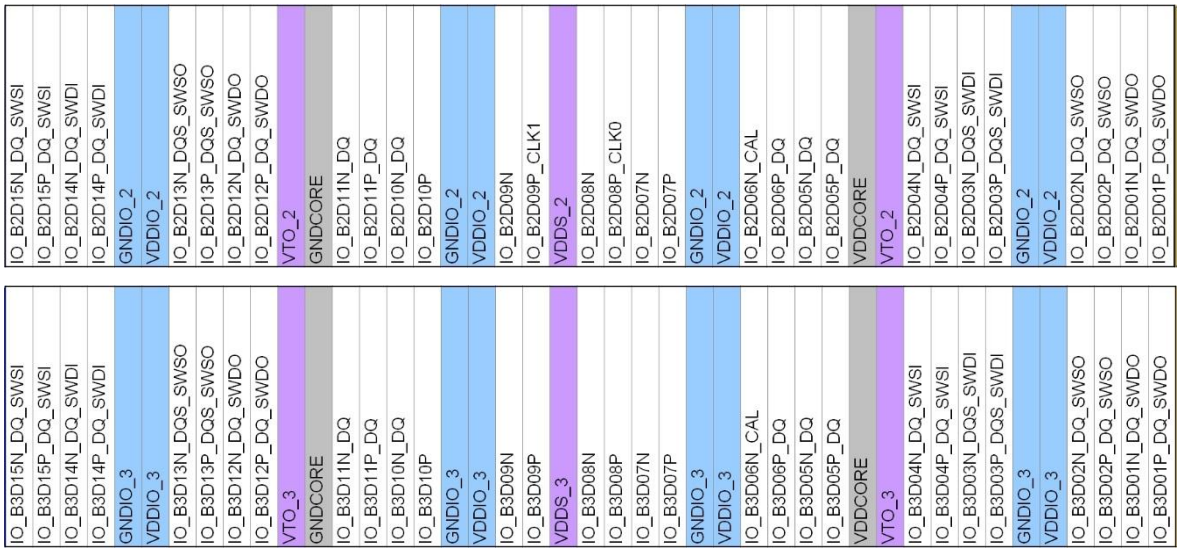
	Complex	Simple
Number of I/O Pads	30	30/22
Resistive termination	Yes	No
Differential	Yes	Yes
Delay line	Yes	Yes
Single DFF	Yes	Yes
CDC	Yes	No
Shift register	Yes	No
DDR	Yes	No
SpaceWire	Yes	No

Table 12: I/O bank Features

Simple I/O Banks present differential pairs allowing I/O supplies of 1.8V, 2.5V or 3.3V;

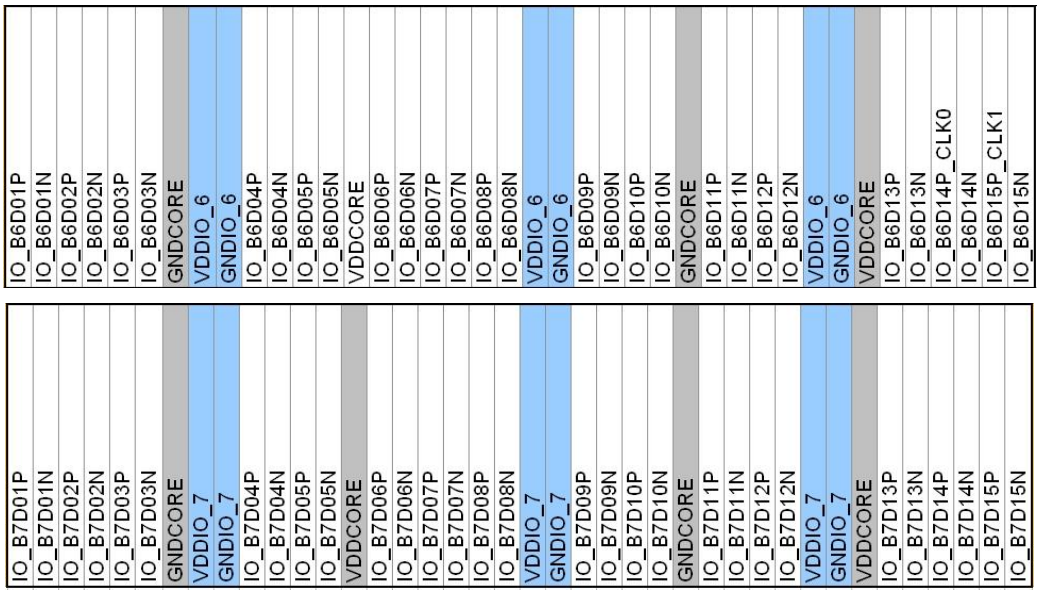
Complex I/O Banks present 15 differential pairs, allow the same I/O supplies of 1.8V, 2.5V or 3.3V, and offer additional features:

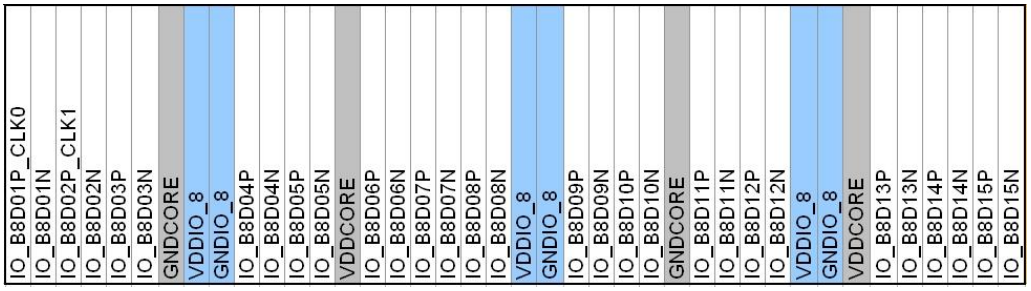
- DDR2 interface capability
- Controlled impedance termination capabilities
- SpaceWire interface capability



Note : I/O banks 2, 5, 9 and 12 have CLK functions; I/O banks 3, 4, 10 and 11 have no CLK functions

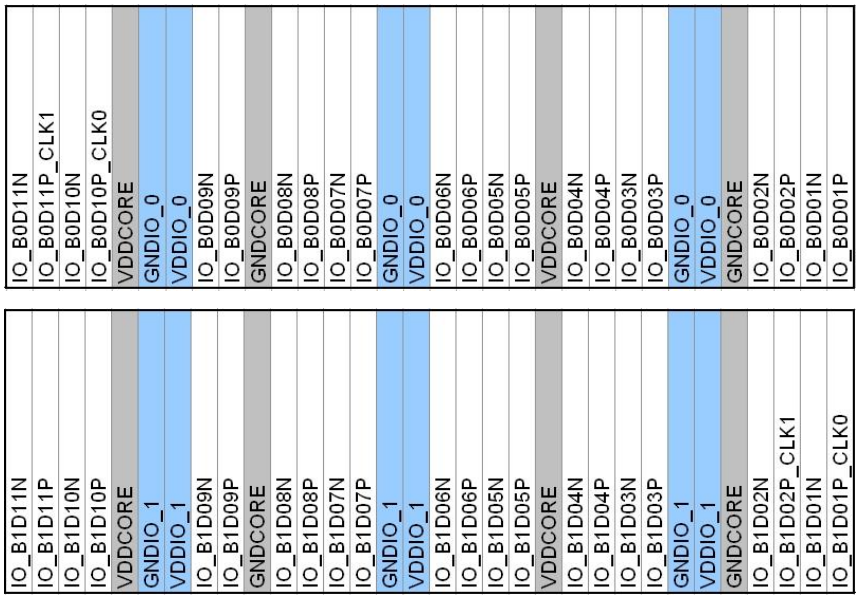
Figure 15: Complex IO Banks 2, 3, 4, 5, 9, 10, 11 and 12 – 30 I/Os





Note : I/O banks 6 and 8 differ only in CLK functions position. I/O bank 7 has no CLK functions

Figure 16 : Simple IO Banks 6, 7 and 8 – 30 I/Os



Note : I/O banks 0 and 1 differ only in CLK functions position.

Figure 17: Simple IO Banks 0 and 1– 22 I/Os

4.2.5.1 DDR Support

11 IOB can be combined to form a physical DDR bytelane (Figure 19) with 9 DQ (8 data, 1 data mask) and 2 DQS (differential strobe).

Each complex bank is able to host 2 bytelanes and command signals complying with the following mapping:

03P or 13P for DQSP pads.

03N or 13N for DQSN pads.

The DQ & DM pins forming a bytelane need to be located in the pins surrounding the corresponding DQS pads.

Clocks, commands and control pins may be located anywhere in banks connected to the same CKG than associated bytelanes. Some banks may be used only by commands pads.

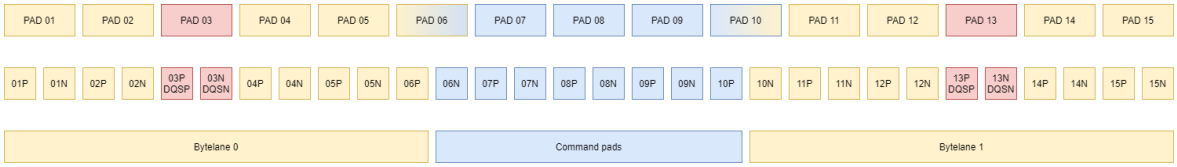


Figure 18: DDR bytelane mapping

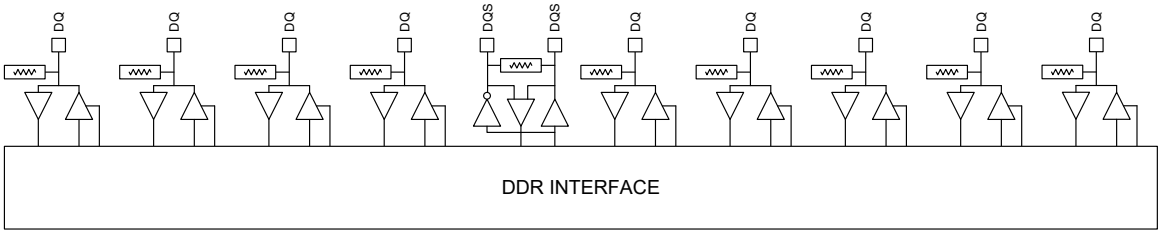


Figure 19: DDR Physical Interface

4.2.5.2 Space-Wire Support

IOB and dedicated Tx and Rx modules can be combined to implement a physical media access layer of a Space Wire interface (Figure 20).

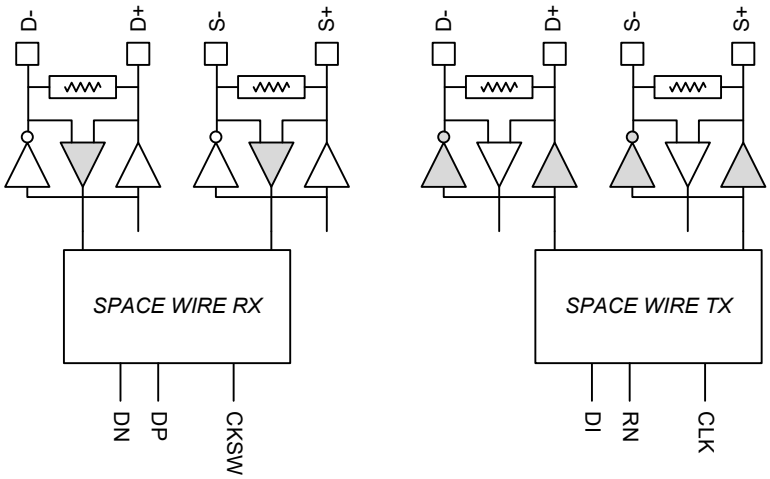


Figure 20: Space Wire Physical Interface

The SpaceWire Tx module receives the transmit clock (CLK), a reset input (RN) and the serial data input (DI) and generates the Data Strobe LVDS outputs. The Rx module receives the Data Strobe LVDS inputs and generates the data clock (CKSW) the positive edge data (DP) and the negative edge data (DN). The Tx and Rx chronograms are illustrated in Figure 21 and Figure 22.

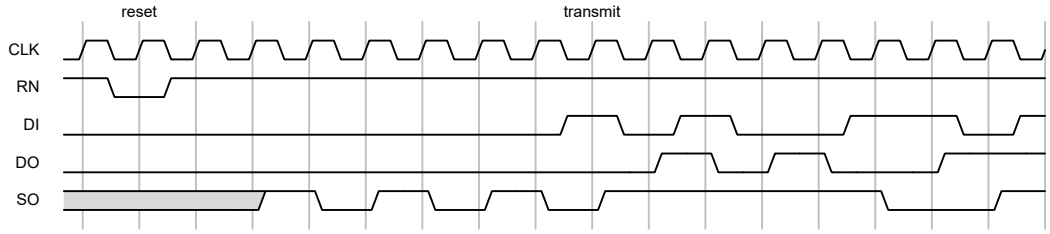


Figure 21: Space Wire Tx Chronogram

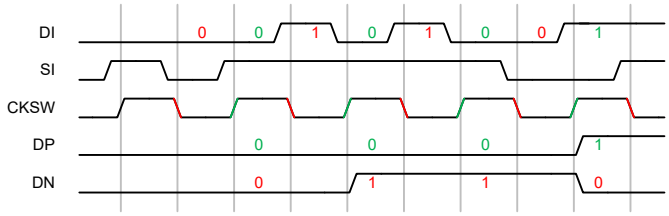


Figure 22: SpaceWire Rx Chronogram

4.2.6 Clock System

The clocking resources can manage various clocking schemes within the FABRIC or between the IOB and the FABRIC. Therefore, the clock distributions spans multiple non homogeneous resources. To achieve the required performance and minimize the skew, the clock distribution is split into several zones. Each zone has its own clock distribution coupled to adjacent IO banks to achieve complex clocking schemes between the periphery and the synchronous elements within the FABRIC.

4.2.6.1 Clock Tree Architecture

Figure 23 is illustrating the clock distribution architecture. There are three types of clock nets:

- Core clock CCK (red)
- Zone clock ZCK (grey)
- Bank clock BCK (green)

Each CKG receives source clocks from 4 BANK inputs (PAD) or 2 FABRIC signals (AUX_CLK).

The FABRIC provides 8 inputs to the CCK switch in order to propagate some internal generated signals to the clock distribution.

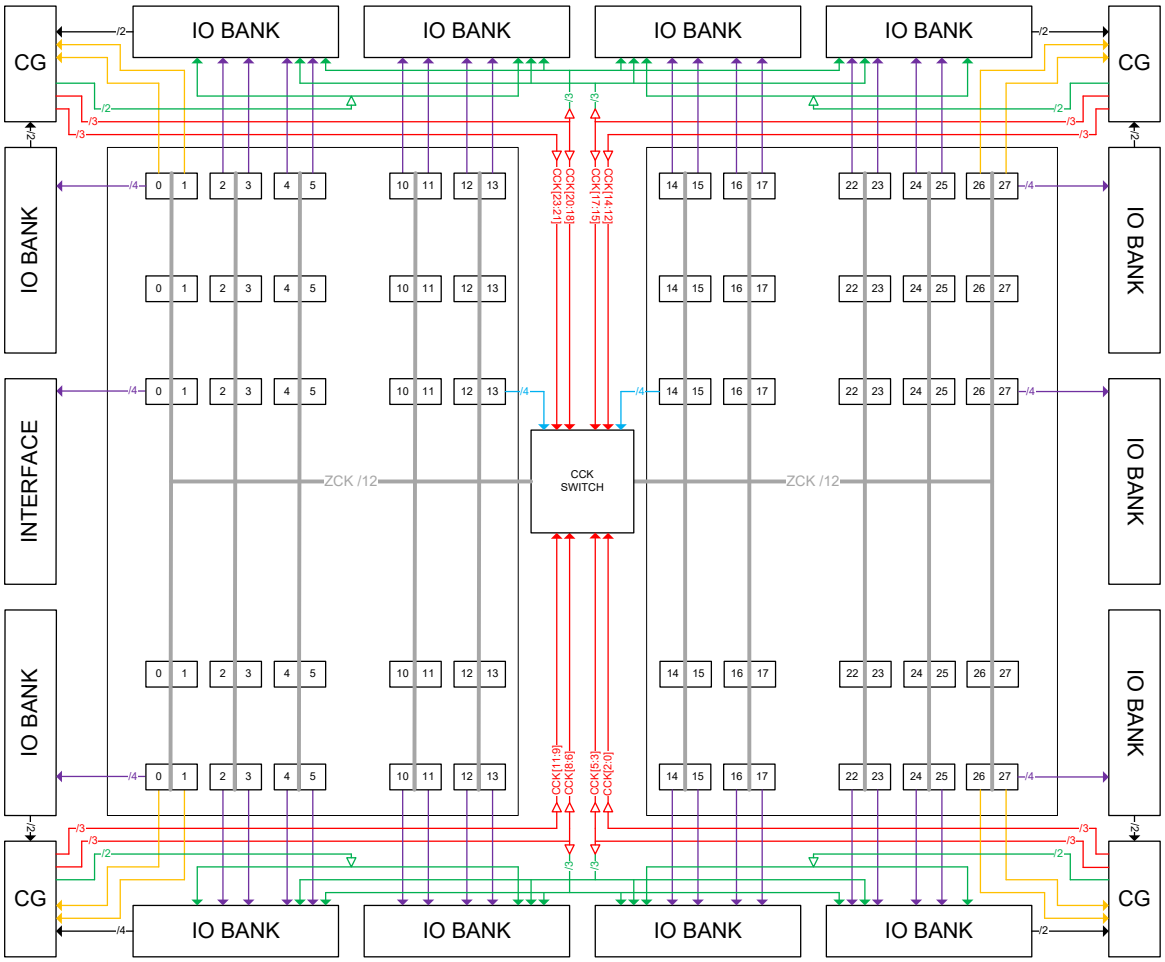


Figure 23: Clock Trees Architecture

4 x Clock Generators (CKG)
Each CKG provides 3 x CCK, 3 x CCK-BCK, 2 x BCK
Each CKG receives 2 x FABRIC inputs and 4x BANK inputs
2 x Clock Zones
12 x ZCK per Clock Zone

Table 13: Clock Distribution Features

4.2.6.2 Clock Generator

The Clock Generation is composed of the main blocks:

- Frequency dividers / Waveform generators (WFG)
- Delay lines

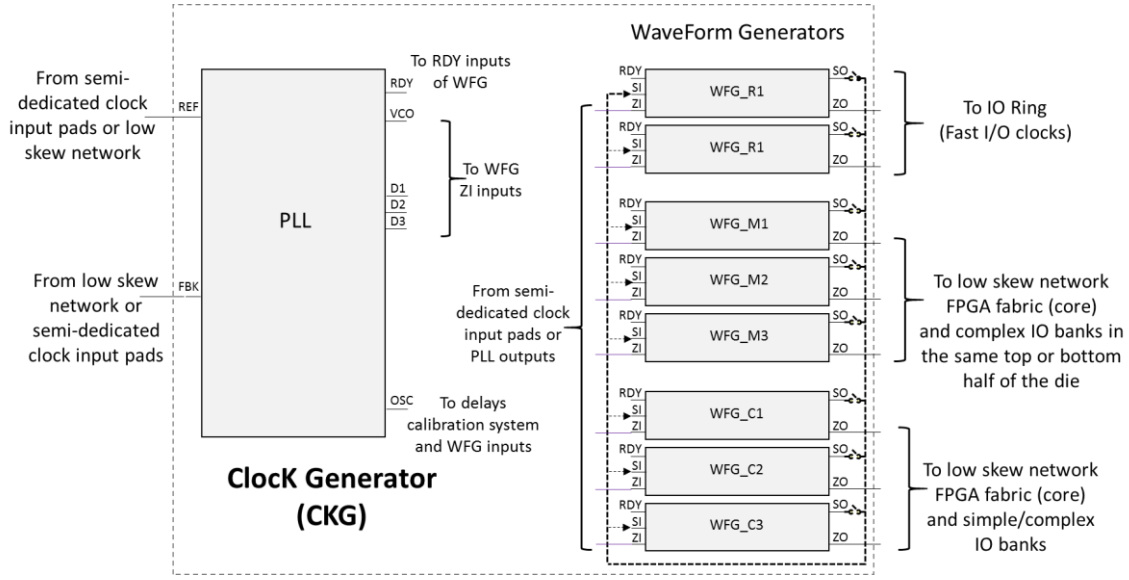


Figure 24: Clock Generator Architecture

Post-Scaler ratio: • 1 • 1/6 – 1/(128*6) ⇔ 1/(2**n * 6) with n=0…7
Waveform Generator ratio: • 1 • ½ – 1/16 ⇔ 1/n with n = 2, 3, …, 16 • Any waveform using 2 – 16 steps is allowed
Delay: 64 steps, 160ps / step

Table 14: Clock Generator Features

A detailed description of the WFG is available in the Library guide, and more information is available on the NG-MEDIUM Cookbook.

The following table summarizes the main PLL characteristics.

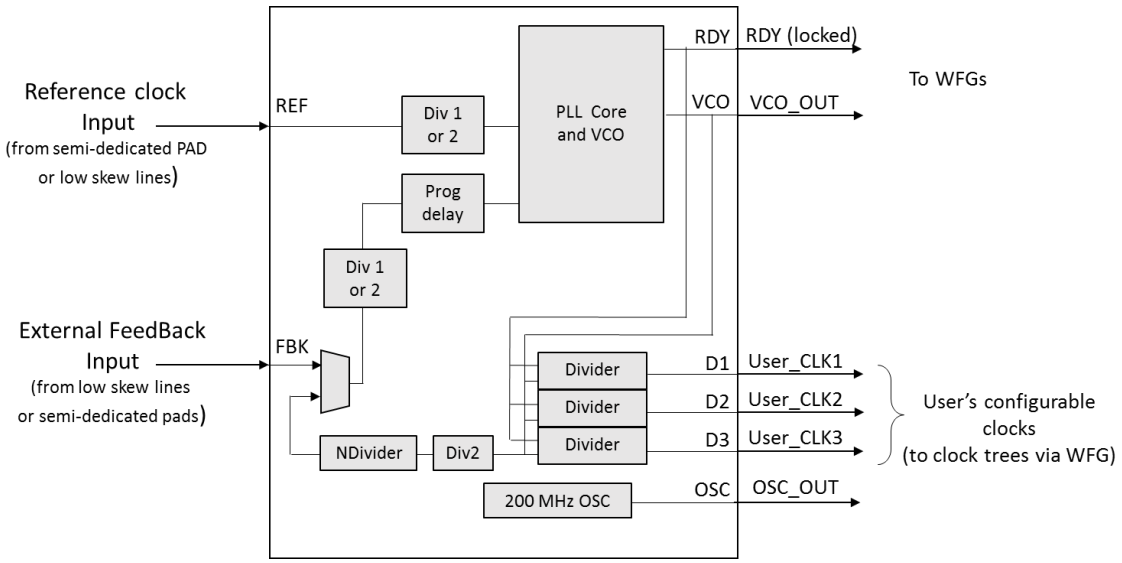


Figure 25: PLL Block Diagram

Pin Name	Direction	Description
REF	Input	Incoming clock to the PLL.
FBK	Input	Feedback clock to the PLL, when PLL's feedback loop is completed using external clock-tree. See PLL configuration in the nxLibrary_guide for NXmap3 document
VCO	Output	VCO output.
D1, D2, D3	Output	Divided clock outputs
OSC	Output	Internal 200 MHz oscillator +/- 10%
RDY	Output	Goes high when PLL is locked

Table 15: PLL Pin Description

Input frequency: 20 MHz – 200 MHz
VCO frequency: 200 MHz – 800 MHz
Output frequency: • VCO output : 200 MHz to 800 MHz (2 frequency ranges) • D1, D2 and D3 outputs : 1,6 MHz to 600 MHz • Loop single phase output (ndivout) = 20MHz to 200MHz range
Maximum power: 26 Mw
Maximum static phase error (clockin – extfbclk): +/- 200ps
Lock time: 100µs
Single period jitter: +/- 60ps @ clk* = 200MHz, REF = 20MHz
Cycle to cycle jitter: +/- 90ps @ clk* = 200MHz, REF = 20MHz
Long term jitter: +/- 330ps @ clk* = 200MHz, REF = 20MHz

Table 16: PLL Characteristics

4.3 Power supplies

4.3.1 NX1H35AS supplies definition

NX1H35AS devices require the following power supplies:

- VDD1V2	Core logic supply	1.2V ± 10%
- VDD2V5A	Auxiliary analog supply, static	2.5V ± 10%

Configuration bank supplies:

- VDDIO_SERVICE	Configuration bank supply	3.3V ± 10%
- VDD_LVDS	Configuration SpaceWire LVDS supply	2.5V ± 10%

If SpaceWire from the Service Bank is not used, VDD_LVDS can be grounded.

Simple I/O banks supplies:

- VDDIO_n	I/O banks supplies	1.8, 2.5 or 3.3V

Complex I/O banks supplies:

- VDDIO_n	I/O banks supplies	1.8, 2.5 or 3.3V
- VDDS_n	I/O termination switches supply	2.5 or 3.3V (*)
- VTO_n	Termination supplies	½ of VDDIO_n supply

(*) *VDDS_n switch voltage should be 3.3V if VDDIO_n=3.3V, else 2.5V. VDDS_n is subject to pollution from the terminated I/Os and should be separated from sensible power supplies.*

4.3.2 Absolute maximum ratings

Symbol	Description		Min	Max	Unit
VDD1V2	Core Logic Supply		-0,5	1,32	V
VDD2V5A	Auxiliary analog supply, static		-0,5	2,75	V
VDDIO_SERVICE	Configuration bank supply		-0,5	3,63	V
VDD_LVDS	Configuration LVDS supply		-0,5	2,75	V
VDDIO_0, VDDIO_1, VDDIO_2, VDDIO_3, VDDIO_4, VDDIO_5, VDDIO_6, VDDIO_7, VDDIO_8, VDDIO_9, VDDIO_10, VDDIO_11, VDDIO_12	Complex / Simple I/O bank supply	LVCMOS 3V3	-0,5	3,63	V
		LVCMOS 2V5	-0,5	2,75	V
		LVCMOS 1V8	-0,5	1,98	V
		SSTL 2V5	-0,5	2,75	V
		SSTL 1V8	-0,5	1,98	V
		HSTL 1V8	-0,5	1,98	V
		LVDS 2V5	-0,5	2,75	V
VDDS_0, VDDS_1, VDDS_2, VDDS_3, VDDS_4, VDDS_5, VDDS_6, VDDS_7, VDDS_8, VDDS_9, VDDS_10, VDDS_11, VDDS_12	I/O termination switch supply	VDDIO_* 3V3	-0,5	3,63	V
		VDDIO_* 2V5	-0,5	2,75	V
VTO_0, VTO_1, VTO_2, VTO_3, VTO_4, VTO_5, VTO_6, VTO_7, VTO_8, VTO_9, VTO_10, VTO_11, VTO_12	Termination supply	LVCMOS 3V3	-0,5	1,815	V
		LVCMOS 2V5	-0,5	1,375	V
		LVCMOS 1V8	-0,5	0,9	V
		SSTL 2V5	-0,5	1,375	V
		SSTL 1V8	-0,5	0,9	V
		HSTL 1V8	-0,5	0,9	V
		LVDS 2V5	-0,5	0,9	V

Table 17: Absolute maximum ratings

4.3.3 Bank supplies use cases

In case of unused bank, VDDIO_n, VTO_n and VDDS_n can be grounded.

For VDDIO 3.3V bank, singled-ended or differential termination modes are not allowed.

For others:

- VTO_n is needed only if singled ended with termination is used in the bank. Otherwise, it can be grounded or left floating.
- VDDS_n is needed if singled-ended or differential termination mode is used in the bank. It is recommended to power VDDS_n even if VTO_n is powered but termination function is not used. Please see Table 18 for different cases.

Single-ended with termination	Differential	VDDIO_n	VTO_n	VDDS_n	**Note**
Yes	-	1.8V	0.9V	2.5V	
No	Yes	1.8V	Grounded or Floating	2.5V	1
No	No	1.8V	Grounded or Floating	Grounded or 2.5V	2
Yes	-	2.5V	1.25V	2.5V	
No	Yes	2.5V	Grounded or Floating	2.5V	1
No	No	2.5V	Grounded or Floating	Grounded or 2.5V	2
No	No	3.3V	Floating	Grounded or 3.3V	3

Table 18 - Termination supplies use cases

1. *If PAD is configured for differential signaling without using on-chip termination, it is recommended to keep VDDS_n at 2.5 V for high frequency signaling to reduce signal perturbation.*
2. *If VDDS is grounded, the termination buffer will be in cold-spare mode. In this mode there will be a small amount of current flowing from PAD to VTO during cold-spare activation when a transition occurs on the PAD (can be seen as an extra capacitive charge).*
3. *When PAD is configured for VDDIO 3.3 V, VDDS_n should be equal to VDDIO or grounded and VTO must be left floating in order to respect foundry reliability rules.*

4.3.4 Termination supplies definition and use cases

Single-ended with termination	Differential	VDDIO_n	VTO_n	VDDS_n	Note
Yes	-	1.8V	0.9V	2.5V	
No	Yes	1.8V	Grounded or Floating	2.5V	1
No	No	1.8V	Grounded or Floating	Grounded or 2.5V	2
Yes	-	2.5V	1.25V	2.5V	
No	Yes	2.5V	Grounded or Floating	2.5V	1
No	No	2.5V	Grounded or Floating	Grounded or 2.5V	2
No	No	3.3V	Floating	Grounded or 3.3V	3

(1) If PAD is configured for differential signaling without using on-chip termination, it is recommended to keep VDDS_n at 2.5 V for high frequency signaling in order to reduce signal perturbation.

(2) If VDDS is grounded, the termination buffer will be in cold-spare mode. In this mode there will be a small amount of current flowing from PAD to VTO during cold-spare activation when a transition occurs on the PAD (can be seen as an extra capacitive charge).

(3) When PAD is configured for VDDIO 3.3 V, VDDS_n should be equal to VDDIO or grounded and VTO has to be left floating in order to respect foundry reliability rules.

Table 19: Termination supplies use cases

4.3.5 Supplies Dependencies

VDD1V2 Core supply current is fully dependent on the downloaded application and working frequency.

VDDIO_n I/O supply current is fully dependent on the downloaded application, used I/O standard and working frequency.

VDD2V5A analog supply current is static.

VDD_SERVICE current is dependent on programming interface mode and activity.

Symbol	Parameter	Min	Typ	Max	Unit
IDD1V2	Quiescent* Core supply current	TBD	170	295	mA
IDD2V5A	Quiescent* VDD2V5A supply current	-	251	-	mA
IDD_SER	Quiescent* VDD_SERVICE supply current	TBD	20	TBD	mA

** Quiescent current is measured when the chip is turned on in safe-config mode without any design.*

4.3.6 PLL supplies use cases

In case of unused PLL, PLL power supplies can comply with the following table:

Power Supply	Expected Voltage
ASUBPLL	GND
AGNDPLL	GND
AVDDPLL	1.2 V
DVDDPLL	1.2 V

Table 20: PLL Pin Description

5 Device configuration

5.1 Purpose of NX1H35AS configuration

NX1H35AS chips are SRAM-based FPGAs. To achieve user-defined functionality their configuration bitstream must be downloaded first.

NX1H35AS chips are always accessible through JTAG, and also support several configuration modes, as a function of the state of MODE[3:0] pins sampled at power-up. RST_N is a dedicated input pin that allows to reset the configuration engine, and launches the configuration process after RST_N is released. (It can't be used to reset the FPGA user's logic).

In Slave Parallel 6 and Slave Parallel 16 modes, the configuration clock must be provided to the FPGA on the CLK dedicated input pin. Its frequency can range from 20 MHz to 50 MHz, in any case it must be strictly greater than twice the JTAG (TCK) frequency – if used.

MODE[3:0]	Configuration mode
0000 0x0	RESERVED
0001 0x1	RESERVED
0010 0x2	Master Serial SPI
0011 0x3	Master Serial SPI with Vcc control
0100 0x4	Slave SpaceWire
0101 0x5	RESERVED
0110 0x6	Slave Parallel 8
0111 0x7	Slave Parallel 16

Please refer to the NG-MEDIUM Configuration Guide for detailed and updated information

5.2 NX1H35AS chips prog interface pin list

The NX1H35AS presents 40 signal pins.

The user must provide the 4-bit MODE value to select the configuration mode. In addition, the internal configuration engine requires an external clock (CLK) and RST_N signal. RST_N must be asserted (low) during at least 50 CLK cycles. When RST_N is de-asserted, the configuration process starts according the MODE bits settings.

Depending on the selected configuration MODE, some prog bank pins are activated during the process. Some other remain as inputs with internal PullUp during the configuration process.

In addition, some prog bank pins can be used as auxiliary user's defined I/Os after completing the configuration.

The next table summarizes the list of pins that can be affected during the configuration process.

Grp	Name	I/O	Description
GLOBAL	MODE(3 :0)	I	Input pins sampled at power-up. MODE(3:0). They define the configuration mode to be used for NG-MEDIUM configuration
	CLK	I	Mandatory input clock for the NG-MEDIUM configuration engine. The frequency must be in the range 20 MHz to 50 MHz, and in any case strictly greater than twice the JTAG TCK frequency.
	RST_N	I	Mandatory input. When low, it resets the internal configuration engine. RST_N must be low at least during 50 CLK cycles to ensure a proper configuration engine reset. When RST_N goes high, the configuration starts after up to 50 CLK cycles.
	READY	O	Goes high when the configuration is complete (and the FPGA enters in user's mode)
	ERROR	O	Generates a high level pulse (during one CLK cycle) each time an error is encountered during the configuration.
Slave Parallel 8	CS_N	I	Active low Chip_Select input. Used in **Slave Parallel 8** mode. The master can write or read to/from the configuration engine when CS_N is low during a CLK rising edge.
	WE_N	I	Active low Write_Enable input. Used in **Slave Parallel 8** mode. The master can write to the configuration engine when both CS_N and WE_N are low during a CLK rising edge.
	DATA_OE	O	DATA_OE is an active high output used in **Slave Parallel 8**. After a master read request, DATA_OE goes high when the requested data is valid on D(7:0)
	D(7 :0)	I/O	8-bit data bus used in **Slave Parallel 8** mode to write the bitstream and/or read internal NG-MEDIUM internal state values
Master Serial SPI	D(8)	O	Used in **Master Serial SPI** and **Master Serial SPI with Vcc control**, as CS_N output to the external SPI Flash memory.
	D(9)	O	Used in **Master Serial SPI** and **Master Serial SPI with Vcc control**, as clock output to the external SPI Flash memory.
	D(10)	I	Used in **Master Serial SPI** and **Master Serial SPI with Vcc control**, as data input (MISO) from the external SPI Flash memory.
	D(11)	O	Used in **Master Serial SPI** and **Master Serial SPI with Vcc control**, as data output (MOSI) to the external SPI Flash memory (while writing a new bitstream into the SPI Flash.
	D(12)	I	Configured as input (with internal PullUp) during the configuration. Can be configured as,user's I/O available after completing the configuration.
	D(13)	I/O	Configured as input (with internal PullPup) during the configuration in **Master Serial SPI**
	D(14)	I/O	Configured as high level output during the configuration in **Master Serial SPI with Vcc control**.
	D(15)	I/O	Can be configured as,user's I/O available after completing the configuration.
SpaceWire	DIN_P	I	SpaceWire interface is available after completing the configuration in Master Serial SPI, Master Serial SPI with Vcc control or Slave Parallel 8 modes. If SpaceWire is used for the configuration, it can't be used for other purpose than the configuration.
	DIN_N	I	
	SIN_P	I	
	SIN_N	I	
	DOUT_P	O	
	DOUT_N	O	
	SOUT_P	O	
	SOUT_N	O	
JTAG	TCK	I	JTAG clock
	TMS	I	JTAG TMS
	TDI	I	JTAG TDI
	TRST_N	I	JTAG TRST_N
	TDO	O	JTAG TDO

6 Timing Characteristics

6.1 PLL Characteristics

Symbol	Parameter	Value	Units
Fin_min	Minimum Input frequency	20	MHz
Fin_max	Maximum Input frequency	200	MHz
FVCO_min	Minimum VCO frequency	200	MHz
FVCO_max	Maximum VCO frequency	800	MHz
Fout_vco_min	Minimum output frequency (VCO outputs)	200	MHz
Fout_vco_max	Maximum output frequency (VCO outputs)	800	MHz
Floop_vco_min	Minimum output frequency (Loop single phase output)	20	MHz
Floop_vco_max	Maximum output frequency (Loop single phase) output)	200	MHz
Tlock	PLL lock time	100	µs

6.2 DSP Timing Characteristics

Symbol	Description	Value	Units
Tby	Delay to bypass a pipeline register	TBD	ns
Ts	Setup time of a pipeline register	TBD	ns
Tq	Clock to pipeline register output delay	TBD	ns
TC->X	Delay between PRC and PRX	TBD	ns
TD->P	Delay between PRD and PRP	TBD	ns
TB->P	Delay between PRB and PRP	TBD	ns
TA->Y	Delay between PRA and PRY	TBD	ns
TP->Y	Delay between PRP and PRY	TBD	ns
TY->Z	Delay between PRY and PRZ	TBD	ns
TY->CO	Delay between PRY and PRCO	TBD	ns
TY->OV	Delay between PRY and PROV	TBD	ns
TX->Z	Delay between PRX and PRZ	TBD	ns
TX->CO	Delay between PRX and PRCO	TBD	ns
TX->OV	Delay between PRX and PROV	TBD	ns
TCI->Z	Delay between PRCI and PRZ	TBD	ns
TCI->CO	Delay between PRCI and PRCO	TBD	ns
TCI->OV	Delay between PRCI and PROV	TBD	ns
Fmax	Max. frequency with all registers used	333	MHz

6.3 DPRAM Timing Characteristics

Port mode		Data width max		ECC off			ECC on					
							Read Reapair off			Read Repair on		
Port0	Port1	Port0	Port1	Tset	Tacc	Tcyc	Tset	Tacc	Tcyc	Tset	Tacc	Tcyc
Read	Read	18	18	TBD	TBD	4	TBD	TBD	5	TBD	TBD	10
Read	Write	36	36	TBD	TBD	4	TBD	TBD	5	TBD	TBD	10
Read	Read/ Write	18	18/36	TBD	TBD	4	TBD	TBD	5	TBD	TBD	10
Write	Read	18	18	TBD	TBD	4	TBD	TBD	5	TBD	TBD	10
Write	Write	18	18	TBD	TBD	4	TBD	TBD	5	TBD	TBD	10
Write	Read/ Write	18	18	TBD	TBD	4	TBD	TBD	5	TBD	TBD	10
Read/ Write	Read	18/18	18	TBD	TBD	4	TBD	TBD	5	TBD	TBD	10
Read/ Write	Write	36/18	18	TBD	TBD	4	TBD	TBD	5	TBD	TBD	10
Read/ Write	Read/ Write	18/18	18	TBD	TBD	4	TBD	TBD	5	TBD	TBD	10
Read	-	36	-	TBD	TBD	4	TBD	TBD	5	TBD	TBD	10
Write	-	18	-	TBD	TBD	4	TBD	TBD	5	TBD	TBD	10
Read/ Write	-	36/18	-	TBD	TBD	4	TBD	TBD	5	TBD	TBD	10
-	Read	-	18	TBD	TBD	4	TBD	TBD	5	TBD	TBD	10
-	Write	-	36	TBD	TBD	4	TBD	TBD	5	TBD	TBD	10
-	Read/ Write	-	18/36	TBD	TBD	4	TBD	TBD	5	TBD	TBD	10

6.4 REGFILE Timing Characteristics

Port mode		ECC on		
Port 0	Port 1	Tset	Tacc	Tcyc
Read	Write	TBD	TBD	3.5

6.5 Fabric Timing Characteristics

Symbol	Parameter	Value	Units
Fmax	Maximum System frequency	250	MHz

Note: This value depends on the mapped application.

6.6 Configuration Timing Characteristics

Configuration start in Master SPI mode :

Master SPI mode configuration starts upon release of NG_MEDIUM RST_N input to its inactive state 1. SPI PROM clock is applied at its minimum frequency, and configuration starts after 3000 clocks (Typ. 1 mS).

Configuration start in Slave modes :

Configuration in slave modes may be started with a typical 10 µS delay after release of NG_MEDIUM RST_N input to its inactive state 1.

Configuration clock inputs:

Symbol	Parameter	Min	Typ	Max	Unit
TCKF	JTAG clock frequency		8		MHz
CLKF	Slave Parallel clock frequency	2 x TCKF		50	MHz
SpWF	Slave SpaceWire data rate			400	Mbit/S

Configuration clock outputs:

Symbol	Parameter	Min	Typ	Max	Unit
CLKbsm	Bistream manager main clock	20	50	50	MHz
DCKF	Master Serial Dump clock frequency		CLKbsm /N*		MHz
SPIF	Master SPI clock frequency		CLKbsm /N*		MHz

** Division factor is 2 ≤ N ≤ 17. Default factor is 17 and may be dynamically changed during bitstream download with values provided by the bitstream generation software*

7 I/O Interface Characteristics

7.1 General Description

I/O Absolute maximum ratings (VDDIO)	-0.33 to 3.66 V
Operating temperature	-55 to 125 °C

Table 21: DC Characteristics

Each pad of each I/O bank can be configured as input-only, output-only or input-output.

7.2 I/O Interface Standards DC/AC Specifications

	VDDIO (V)			Vref ([1]) (V) (Internally generated)			VTO (V)			
Standard	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**Standard Support**
LVCMOS 3V3	3.15	3.3	3.45	-	1.49	-	-	-	-	JESD8C.01
LVCMOS 2V5	2.375	2.5	2.625	-	1.25	-	-	-	-	JESD8-5
LVCMOS 1V8	1.71	1.8	1.89	-	0.9	-	-	-	-	JESD8-7
SSTL 2V5 class I/II	2.3	2.5	2.7	1.13	1.25	1.38	(VDDIO/2) -0.04	VDDIO/2	(VDDIO/2) +0.04	JESD8-9
SSTL 1V8 class I/II	1.7	1.8	1.9	0.838	0.9	0.969	(VDDIO/2) -0.04	VDDIO/2	(VDDIO/2) +0.04	JESD8-15
HSTL 1V8 class I/II	1.7	1.8	1.9	0.838	0.9	0.969	-	VDDIO/2	-	JESD8-6
LVDS 2V5	2.25	2.5	2.75	-	-	-	-	-	-	ANSI/TIA/EIA-644

[1] *Vref represents an internally generated reference voltage, which is generally equal to the half of VDDIO voltage and used as input buffer comparator reference voltage.*

Table 22: I/O Standard DC characteristics

	AC				DC						
Standard	**VIH(V)**	**VIL(V)**	**VOH(V)**	**VOL(V)**	**VIH([1]) (V)**	**VIL([1]) (V)**	**VOH([1]) (V)**	**VOL([1]) (V)**	**IOH (mA)**	**IOL (mA)**	Standard Support
LVCMOS 3V3	-	-	-		2	0.8	2.4	0.4	-2, -4, -8, -16	2, 4, 8, 16	JESD8C.01
LVCMOS 2V5	-	-	-	-	1.7	0.7	1.7	0.7			JESD8-5
LVCMOS 1V8	-	-	-	-	0.65*VDDIO	0.35*VDDIO	VDDIO-0.45	0.45			JESD8-7
SSTL 2V5 class I	Vref+0.31	Vref-0.31	VTO+0.6	VTO-0.6	Vref+0.15	Vref-0.15	Vt+0.6	Vt-0.6	-8.1	8.1	JESD8-9
SSTL 2V5 class II	Vref+0.31	Vref-0.31	VTO+0.8	VTO-0.8	Vref+0.15	Vref-0.15	Vt+0.8	Vt-0.8	-16.2	16.2	JESD8-9
SSTL 1V8 class I	Vref+0.25	Vref-0.25	VTO+0.6	VTO-0.6	Vref+0.125	Vref-0.125	Vt+0.6	Vt-0.6	-8.6	8.6	JESD8-15
SSTL 1V8 class II	Vref+0.25	Vref-0.25	VTO+0.6	VTO-0.6	Vref+0.125	Vref-0.125	Vt+0.6	Vt-0.6	13.4	13.4	JESD8-15
HSTL 1V8 class I	Vref+0.2	Vref-0.2	VDDIO-0.6	0.6	Vref+0.1	Vref-0.1	VDDIO-0.4	0.4	-8	8	JESD8-6
HSTL 1V8 class II	Vref+0.2	Vref-0.2	VDDIO-0.6	0.6	Vref+0.1	Vref-0.1	VDDIO-0.4	0.4	-16	16	JESD8-6

[1] *Compatibility with Jedec Standards is assured by design and configuration of IOs*

Table 23: I/O Single-Ended Standards AC/DC Input Output Specifications

	VICM (V) Input common mode			**VID (V) Input differential**	
Standard	**Min**	**Typ**	**Max**	**Min**	**Max**
LVDS 2V5[1]	0.75[(3)]	1.25[(3)]	1.7[(3)]	0.1	-

	VOD (V) [(2)] Output Differential			**V OCM (V) Output common mode**		
Standard	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
LVDS 2V5[(1)]	0.36	0.55	0.782	1.02	1.2	1.42

- *NG-MEDIUM IO PADS programmed as LVDS2V5 are "LVDS-compatible", therefore AC/DC specifications are different that standard support ANSI/TIA/EIA-644 specifications.*
- *For R termination 100 Ω under DC conditions.*
- *Under DC Condition*

Table 24: I/O Differential Standards AC/DC Input Output Specifications

Single-ended characterization of LVDS IO pads with 2mA of applied current charge used in qualification:

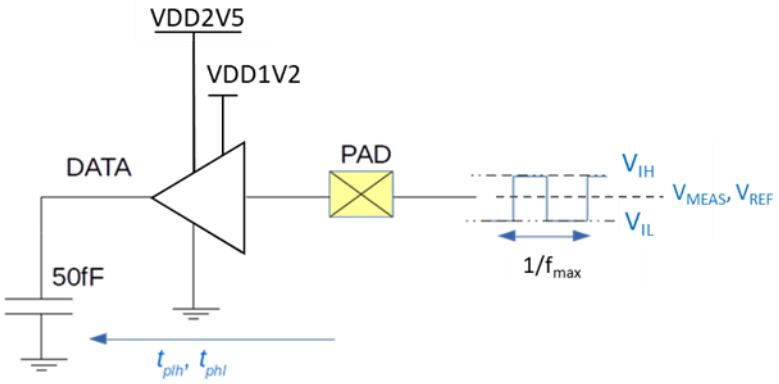
			Min	Typ	Max	
Low Level Output Voltage	V_{OL}	I_{OH} = 2 mA	-		0.7	V
High Level Output Voltage	V_{OH}	I_{OL} = 2 mA	1.7		-	V

Table 25: Single-ended characterization of LVDS IO pads used in qualification.

It has to be noted that the drive strength is programmable through configuration.

7.3 I/O Input/Output Switching Characteristics

7.3.1 Generic I/O Buffer Testbench



I/O Standard	V_{IL} [V]	V_{IH} [V]	V_{MEAS} [V] (1)	V_{REF} [V] (2)
LVCMOS 3.3V	0	3.3	1.5	-
LVCMOS 2.5V	0	2.5	1.25	-
LVCMOS 1.8V	0	1.8	0.9	-
SSTL 2.5V Class I/II	V_{REF}-0.75	V_{REF}+0.75	V_{REF}	1.25
SSTL 1.8V Class I/II	V_{REF}-0.5	V_{REF}+0.5	V_{REF}	0.9
HSTL 1.8V Class I/II	V_{REF}-0.5	V_{REF}+0.5	V_{REF}	0.9
LVDS 2.5	V_{REF}-0.125	V_{REF}+0.125	0 (3)	1.25

Notes :

(1) Input voltage level from which the measurements starts.

(2) This is the input voltage reference used for input signal generation.

(3) The value is given in differential input voltage.

Figure 26: Generic single-ended testbench for input buffer

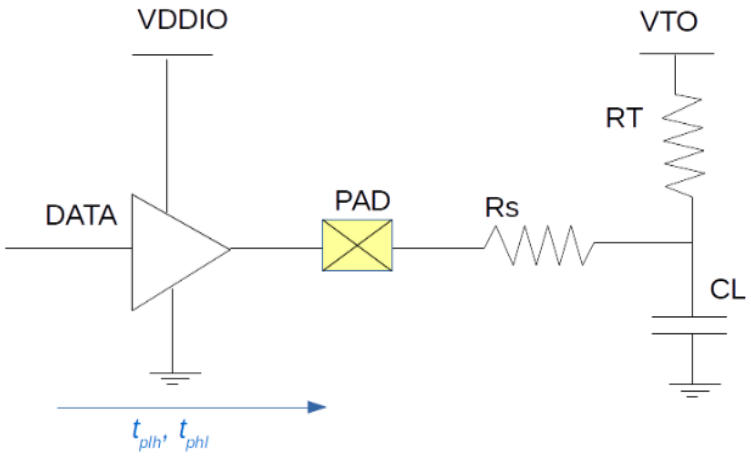


Figure 27: Generic testbench of Output Buffer for Single-ended AC loading

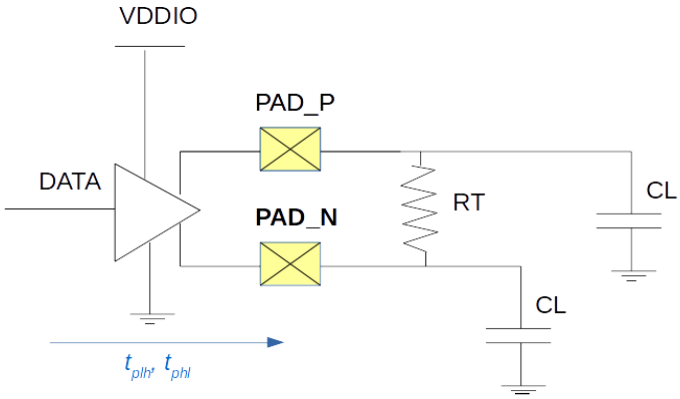


Figure 28: Generic testbench of Output Buffer for Differential AC loading

7.3.2 IO Input Buffer Switching Characteristics

Standard	tplh (1) (ns)	tphl (1) (ns)	trise (2) (ps)	tfall (2) (ps)	turbo	fmax (MHz)
LVCMOS 3V3	0.917	0.728	97.7	61.2	Yes	200
LVCMOS 3V3	2.50	1.90	98/6	61.4	No	100
LVCMOS 2V5	0.901	0.778	97.9	60.6	Yes	300
LVCMOS 2V5	2.72	2.04	97.4	61.4	No	150
LVCMOS 1V8	0.975	0.883	97.8	60.6	Yes	300
LVCMOS 1V8	2.78	2.58	97.2	61.7	No	150
LVCMOS 1V5	0.962	0.991	97.8	60.6	Yes	300
LVCMOS 1V5	2.61	2.99	98.3	62.1	No	150
SSTL 2V5	0.944	0.824	97.7	60.7	Yes	300
SSTL 1V8	0.935	0.818	97.7	60.6	Yes	400
HSTL 1V8	0.982	0.858	97.7	60.6	Yes	400
HSTL 1V5	0.973	0.892	97.7	60.6	Yes	400
LVDS 2V5	1.09	1.17	97.7	60.6	Yes	400
LVDS 2V5	3.11	2.77	97.3	61.9	No	100

Table 26: I/O Input Buffer Switching Characteristics

Simulation conditions:
*Worse-case operating conditions as VDD1V2O*0.9 V and -40C junction temperature.*
Worse-case packaging parasitic are considered.
PAD input signal changes between VIHACmin and VILACmax of the IO standard under test with a 50ps transition time.

*[1] tplh and tphl are defined as described in Figure 25. Timing reference for switching is Vref of the standard-under-test at input of the buffer and 0.5*VDD1V2 at output of the buffer.*
[2] trise and tfall are calculated as 20-80% transition time of data signal at the output of the input buffer divided by 0.6 to extrapolate to full swing.

7.3.3 Output Buffer Switching Characteristics

Standard	tplh [1] (ns)	tphl [1] (ns)	rising ramp (V/ns)	falling ramp (V/ns)	F_{max} for Cload (MHz)
LVCMOS 3V3 2mA	3.81	4.98	0.42	0.39	50
LVCMOS 3V3 4mA	2.6	3.04	0.81	0.77	100
LVCMOS 3V3 8mA	2.07	2.06	1.27	1.61	200
LVCMOS 3V3 16mA	1.75	1.76	3.22	3.39	300

LVCMOS 2V5 2mA	4.65	5.22	0.27	0.24	50
LVCMOS 2V5 4mA	3.02	3.14	0.52	0.48	100
LVCMOS 2V5 8mA	2.10	2.56	1.06	0.75	200
LVCMOS 2V5 16mA	1.80	1.85	2.32	1.74	300
LVCMOS 1V8 2mA	3.62	4.09	0.29	0.25	50
LVCMOS 1V8 4mA	2.92	3.07	0.43	0.38	100
LVCMOS 1V8 8mA	2.09	2.11	0.88	0.77	200
LVCMOS 1V8 16mA	1.82	1.72	1.94	1.88	300
SSTL2V5 class I	1.64	1.64	1.55	1.52	300
SSTL2V5 class II	1.49	1.51	2.76	2.39	300
SSTL1V8 class I	1.60	1.60	1.82	1.66	400
SSTL1V8 class II	1.53	1.52	1.81	1.63	400
HSTL1V8 class I	1.58	1.57	1.18	1.17	400
HSTL1V8 class II	1.47	1.51	1.14	1.07	400
LVDS 2V5 [2]	1.61	1.61	1.43	1.41	400

Table 27: Output Buffer Switching Characteristics

Notes:
Simulation conditions:
*Worse-case operating conditions as VDDIOnom*0.9 and 125C junction temperature. A worse-case packaging parasitic model is used. Output buffer input signal transition time is set as one tenth of the signal pulse width which varies with F_{max} and the duty cycle is 0.5. No parasitic nor transmission line effect due to board traces are considered in this characterization. Spice benches consider only RLC parasitic due to packaging and a resistive/capacitive load connected directly to PAD pin, for which values can be found in (reference to table 22 I/O standard termination specifications).*

*[1] tplh and tphl are defined as described in Figure 25 and Figure 27. Reference voltages for timing extractions are V_{ref} of Standard-under-test (Table 17) at output of the output buffer and 0.5*VDD1V2 at input of the output buffer.*
[2] Output signal reference voltage for timing extraction of LVDS 2V5 is 0V for differential output voltage.

7.3.4 IO Standard Termination Specifications

Standard	Rs (Ω)	RT (Ω)	CL (pF)	VT (V)
LVCMOS 3V3	-	-	5	0
LVCMOS 2V5	-	-	5	0
LVCMOS 1V8	-	-	5	0
SSTL 2V5 class I	25	50	5	1.25
SSTL 2V5 class II	25	25	5	1.25
SSTL 1V8 class I	20	50	5	0.9
SSTL 1V8 class II	20	25	5	0.9
HSTL 1V8 class I	-	50	5	0.9
HSTL 1V8 class II	-	25	5	0.9
LVDS 2V5	-	100	5	-

Table 28: I/O Standard Termination Specifications

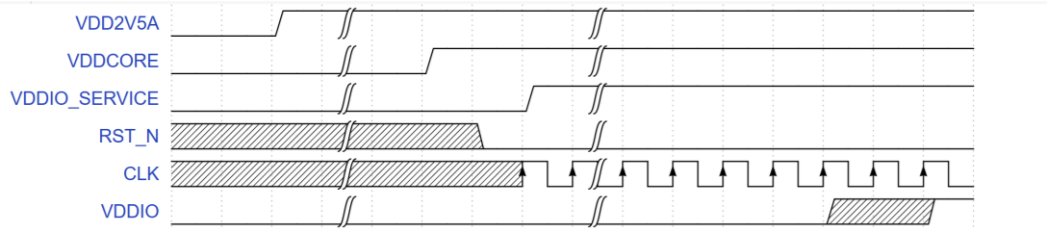
8 Power supplies sequencing

The recommended power-on sequencing follows:

- 2.5V VDD2V5A analog supply first
- 1.2V VDDCORE core supply, next
- VDDIO_SERVICE bank supplies next
- VDDIO_n IO Bank power supply last

Therefore VDD2V5A, VDDCORE and VDDIO_SERVICE power rails should be electrically isolated and powered before other power rails.
In cases where this sequence is not respected, transient glitches may appear on powered User IO Banks.

Figure 29 - NG-Medium Power-On Sequencing Requirements



s

Clock on CLK pin and active low reset signal on RST_N pin should be present

- before or after VDDIO_SERVICE power-up
- before User IO Banks VDDIO power-up

to guarantee the completion of power-on-reset and entry into safe configuration mode that will configure all I/Os as input until the end of the loading of the bitstream.

VDDS_n switch supply is required after device configuration, so it can be derived from the same base 2.5V supplies. It is not recommended to derive from VDD2V5A supply since it can cause interference with I/O signal state during power-up depending on VTO supply state

VTO_n terminations supplies are also necessary after device configuration. If needed by the application, they should thus be derived from the corresponding VDDIO_n supplies.

VDDLVDS SpaceWire I/Os supply has few interferences with other supplies, it can be derived from other 2.5V VDDIO_n Supplies.

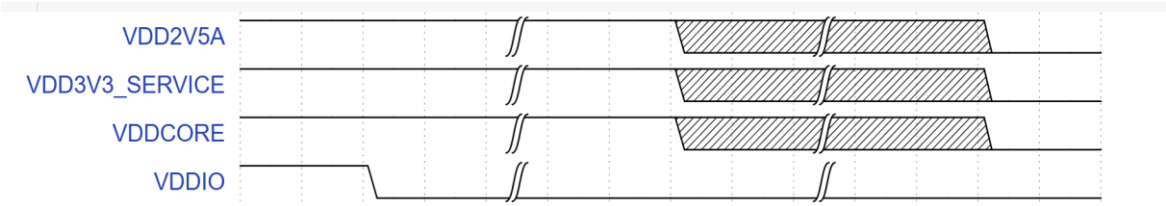
NOTE: There are no specific timing requirements while power-on sequencing. It is recommended to respect the above sequence with 80% level on each power supply before rising the next one and avoid long delays between the activation of successive power supplies.

Even if this recommendation is not respected, NG-MEDIUM will be successfully configured with loaded bitstream.

During power-off, it is recommended to first power-off User IO Bank supplies VDDIO to avoid any transient glitch on user I/Os.

NOTE: There are no specific timing requirements while power-off sequencing

Figure 30 - NG-Medium recommended power-off sequencing



9 Package Pin Assignment

The NG-MEDIUM FPGA (NX1H35AS) is packaged in Land-Grid Array 625 (LG625) package, Ceramic Column-Grid Array 625 (CG625) package and Ceramic Quad-Flat Package 352pins.

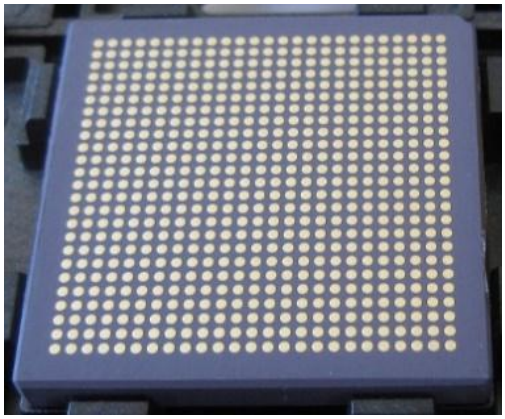


Figure 31: LGA625 picture

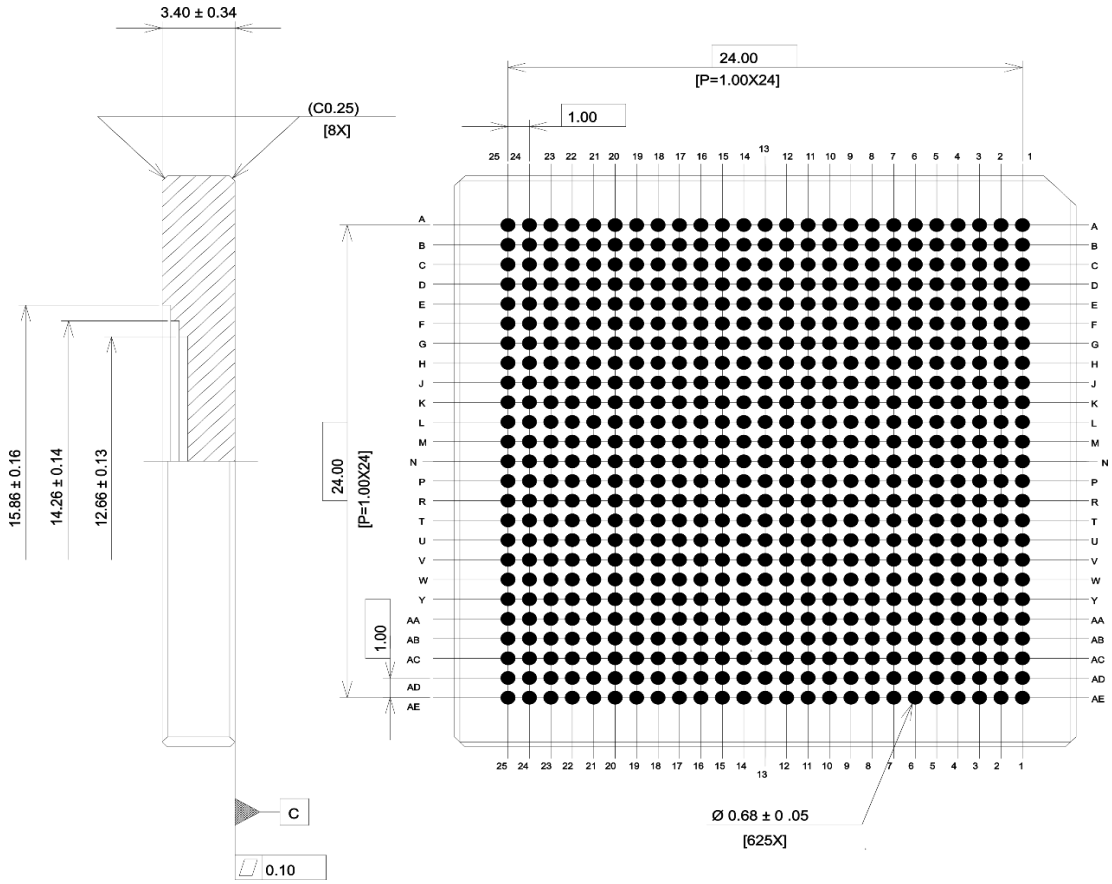


Figure 32: LGA625 mechanical outline

CCGA/CLGA625 package connects all the 374 die's user I/Os

Bank	Type	I/Os
0	Simple	22
2	Complex	30
4	Complex	30
6	Simple	30
8	Simple	30
9	Complex	30
11	Complex	30

Bank	Type	I/Os
1	Simple	22
3	Complex	30
5	Complex	30
7	Simple	30
10	Complex	30
12	Complex	30

Table 29: LGA/CGA 625 I/O banks

Bank	Pin Name	Pin Nbr	I/O	Description
0	IO_B0D11N	H7	I/O	
0	IO_B0D11P_CLK1	G6	I/O	
0	IO_B0D10N	J8	I/O	
0	IO_B0D10P_CLK0	J7	I/O	
-	VDDSENSE	N9		VDDCORE Sense return
0	GND	F2		Internal GND plane
0	VDDIO_0	F1		Bank0 I/O supply
0	IO_B0D09N	G5	I/O	
0	IO_B0D09P	G4	I/O	
-	GND	J12		Internal GND plane
0	IO_B0D08N	F3	I/O	
0	IO_B0D08P	G3	I/O	
0	IO_B0D07N	H6	I/O	
0	IO_B0D07P	H5	I/O	
-	GND	J2		Internal GND plane
0	VDDIO_0	J1		Bank0 I/O supply
0	IO_B0D06N	H4	I/O	
0	IO_B0D06P	H3	I/O	
0	IO_B0D05N	G2	I/O	
0	IO_B0D05P	G1	I/O	
-	VDDCORE	K12		Internal VDD1V2 plane
0	IO_B0D04N	K8	I/O	
0	IO_B0D04P	K7	I/O	
0	IO_B0D03N	J6	I/O	
0	IO_B0D03P	J5	I/O	
-	GND	K9		Internal GND plane
0	VDDIO_0	L9		Bank0 I/O supply
-	GND	J14		Internal GND plane
0	IO_B0D02N	J4	I/O	
0	IO_B0D02P	J3	I/O	
0	IO_B0D01N	H2	I/O	
0	IO_B0D01P	H1	I/O	
-	VDDCORE	K14		Internal VDD1V2 plane
-	GND	K13		Internal GND plane
-	VDD2V5A	A6		Internal VDD2V5A ring
Prog	GND	K2		Internal GND plane
Prog	DOUT_P	K4	O	Configuration Spacewire
Prog	DOUT_N	K3	O	Configuration Spacewire
-	GND	L10		Internal GND plane
Prog	SOUT_P	K6	O	Configuration Spacewire
Prog	SOUT_N	K5	O	Configuration Spacewire

Prog	DIN_P	L3	I	Configuration Spacewire
Prog	DIN_N	L2	I	Configuration Spacewire
-	VDDCORE	L11		Internal VDD1V2 plane
Prog	SIN_P	L5	I	Configuration Spacewire
Prog	SIN_N	L4	I	Configuration Spacewire
Prog	VDDLVDS	L1		2.5V LVDS supply (Space wire)
Prog	RST_N	L6	I	Hardware Reset input
Prog	MODE0	L8	I	Cfg Mode input
Prog	MODE1	L7	I	Cfg Mode input
Prog	MODE2	M8	I	Cfg Mode input
Prog	VDDIO_SERVICE	M7		3.3V Prog supply
-	GND	M6		Internal GND plane
Prog	MODE3	N8	I	Cfg Mode input
Prog	ERROR	N7	O	Cfg Error output
Prog	TCK	M5	I	JTAG Clock input
Prog	TRST	M4	I	Active-low JTAG Reset input
Prog	CLK	M3	I	SlavePar Clock input
Prog	TMS	M2	I	JTAG TMS input
Prog	TDI	M1	I	JTAG TDI input
Prog	TDO	N3	O	JTAG TDO output
Prog	VDDIO_SERVICE	N1		3.3V Prog supply
-	GND	N2		Internal GND plane
Prog	READY	N6	O	Cfg Ready output
Prog	D0	P5	I/O	SlavePar Data bit 0
Prog	D1	P4	I/O	SlavePar Data bit 1
Prog	D2	P3	I/O	SlavePar Data bit 2
Prog	D3	P2	I/O	SlavePar Data bit 3
Prog	D4	P1	I/O	SlavePar Data bit 4
Prog	D5	R5	I/O	SlavePar Data bit 5
Prog	D6	R4	I/O	SlavePar Data bit 6
Prog	VDDIO_SERVICE	N5		3.3V Prog supply
-	GND	N4		Internal GND plane
Prog	D7	R3	I/O	SlavePar Data bit 7
Prog	D8	P8	I/O	SlavePar Data bit 8
Prog	D9	P7	I/O	SlavePar Data bit 9
Prog	D10	P6	I/O	SlavePar Data bit 10
Prog	D11	R8	I/O	SlavePar Data bit 11
Prog	D12	R7	I/O	SlavePar Data bit 12
Prog	D13	R6	I/O	SlavePar Data bit 13
Prog	D14	T6	I/O	SlavePar Data bit 14
Prog	VDDIO_SERVICE	R1		3.3V Prog supply
-	GND	T2		Internal GND plane
Prog	D15	T5	I/O	SlavePar Data bit 15
Prog	CS_N	R2	I	SlavePar Chip Select input
Prog	WE_N	T4	I	SlavePar Write Enable input
Prog	DATA_OE	T3	O	SlavePar Data available output
-	VDD2V5A	A13		Internal VDD2V5A ring
-	VDDCORE	L13		Internal VDD1V2 plane
-	GND	L12		Internal GND plane
1	IO_B1D11N	T8	I/O	
1	IO_B1D11P	T7	I/O	
1	IO_B1D10N	U7	I/O	
1	IO_B1D10P	U6	I/O	
-	VDDCORE	L15		Internal VDD1V2 plane
-	GND	R9		Internal GND plane
1	VDDIO_1	T9		Bank1 I/O supply
1	IO_B1D09N	U4	I/O	
1	IO_B1D09P	U3	I/O	
-	GND	L14		Internal GND plane

1	IO_B1D08N	U5	I/O	
1	IO_B1D08P	V5	I/O	
1	IO_B1D07N	V4	I/O	
1	IO_B1D07P	V3	I/O	
-	GND	U2		Internal GND plane
1	VDDIO_1	U1		Bank1 I/O supply
1	IO_B1D06N	V2	I/O	
1	IO_B1D06P	V1	I/O	
1	IO_B1D05N	U8	I/O	
1	IO_B1D05P	V7	I/O	
-	VDDCORE	M10		Internal VDD1V2 plane
1	IO_B1D04N	V6	I/O	
1	IO_B1D04P	W5	I/O	
1	IO_B1D03N	W4	I/O	
1	IO_B1D03P	W3	I/O	
-	GND	Y2		Internal GND plane
1	VDDIO_1	Y1		Bank1 I/O supply
-	GND	L16		Internal GND plane
1	IO_B1D02N	W2	I/O	
1	IO_B1D02P_CLK1	W1	I/O	
1	IO_B1D01N	Y4	I/O	
1	IO_B1D01P_CLK0	Y3	I/O	
CG1	CG1_AGNDPLL	AA1		PLL1 Analog GND
CG1	CG1_AVDDPLL	AB1		PLL1 1.2V Analog Supply
CG1	CG1_ASUBPLL	AA2		PLL1 Substrate -> AGND
-	GND	T11		Internal GND plane
CG1	CG1_DVDDPLL	T10		PLL1 1.2V Digital Supply
-	GND	M9		Internal GND plane
-	VDDCORE	M12		Internal VDD1V2 plane
2	IO_B2D15N_DQ_SWSI	AD1	I/O	
2	IO_B2D15P_DQ_SWSI	AE1	I/O	
2	IO_B2D14N_DQ_SWDI	AC2	I/O	
2	IO_B2D14P_DQ_SWDI	AC3	I/O	
-	GND	W9		Internal GND plane
2	VDDIO_2	V9		Bank2 I/O supply
2	IO_B2D13N_DQS_SWSO	AA3	I/O	
2	IO_B2D13P_DQS_SWSO	AB3	I/O	
2	IO_B2D12N_DQ_SWDO	AA4	I/O	
2	IO_B2D12P_DQ_SWDO	Y5	I/O	
2	VTO_2	AD2		Bk2 Termination voltage
-	GND	M11		Internal GND plane
2	IO_B2D11N_DQ	W6	I/O	
2	IO_B2D11P_DQ	Y6	I/O	
2	IO_B2D10N_DQ	W7	I/O	
2	IO_B2D10P	Y7	I/O	
-	GND	AB2		Internal GND plane
2	VDDIO_2	AC1		Bank2 I/O supply
2	IO_B2D09N	V8	I/O	
2	IO_B2D09P_CLK1	W8	I/O	
2	VDDS_2	AE3		Bank2 Switch supply
2	IO_B2D08N	U9	I/O	
2	IO_B2D08P_CLK0	U10	I/O	
2	IO_B2D07N	Y8	I/O	
2	IO_B2D07P	AA8	I/O	
-	GND	AD3		Internal GND plane
2	VDDIO_2	AE2		Bank2 I/O supply
2	IO_B2D06N_CAL	AB4	I/O	
2	IO_B2D06P_DQ	AC4	I/O	
2	IO_B2D05N_DQ	AD4	I/O	

2	IO_B2D05P_DQ	AE4	I/O	
-	VDDCORE	M14		Internal VDD1V2 plane
2	VTO_2	AD5		Bk2 Termination voltage
2	IO_B2D04N_DQ_SWSI	AA5	I/O	
2	IO_B2D04P_DQ_SWSI	AB5	I/O	
2	IO_B2D03N_DQS_SWDI	AC5	I/O	
2	IO_B2D03P_DQS_SWDI	AC6	I/O	
-	GND	AD6		Internal GND plane
2	VDDIO_2	AE5		Bank2 I/O supply
2	IO_B2D02N_DQ_SWSO	AA6	I/O	
2	IO_B2D02P_DQ_SWSO	AB6	I/O	
2	IO_B2D01N_DQ_SWDO	AA7	I/O	
2	IO_B2D01P_DQ_SWDO	AB7	I/O	
-	VDD2V5A	A20		Internal VDD2V5A ring
3	IO_B3D15N_DQ_SWSI	AB8	I/O	
3	IO_B3D15P_DQ_SWSI	AC7	I/O	
3	IO_B3D14N_DQ_SWDI	AB9	I/O	
3	IO_B3D14P_DQ_SWDI	AC8	I/O	
-	GND	V13		Internal GND plane
3	VDDIO_3	W13		Bank3 I/O supply
3	IO_B3D13N_DQS_SWSO	AB10	I/O	
3	IO_B3D13P_DQS_SWSO	AC9	I/O	
3	IO_B3D12N_DQ_SWDO	AD9	I/O	
3	IO_B3D12P_DQ_SWDO	AE8	I/O	
3	VTO_3	AD8		Bk3 Termination voltage
-	GND	M13		Internal GND plane
3	IO_B3D11N_DQ	Y9	I/O	
3	IO_B3D11P_DQ	AA9	I/O	
3	IO_B3D10N_DQ	Y10	I/O	
3	IO_B3D10P	AA10	I/O	
-	GND	AD10		Internal GND plane
3	VDDIO_3	AD7		Bank3 I/O supply
3	IO_B3D09N	V10	I/O	
3	IO_B3D09P	W10	I/O	
3	VDDS_3	AE10		Bank3 Switch supply
3	IO_B3D08N	U11	I/O	
3	IO_B3D08P	V11	I/O	
3	IO_B3D07N	W11	I/O	
3	IO_B3D07P	Y11	I/O	
-	GND	AE7		Internal GND plane
3	VDDIO_3	AD13		Bank3 I/O supply
3	IO_B3D06N_CAL	AB11	I/O	
3	IO_B3D06P_DQ	AC10	I/O	
3	IO_B3D05N_DQ	AC11	I/O	
3	IO_B3D05P_DQ	AC12	I/O	
-	VDDCORE	M16		Internal VDD1V2 plane
3	VTO_3	AD12		Bk3 Termination voltage
3	IO_B3D04N_DQ_SWSI	AD11	I/O	
3	IO_B3D04P_DQ_SWSI	AE11	I/O	
3	IO_B3D03N_DQS_SWDI	AA11	I/O	
3	IO_B3D03P_DQS_SWDI	AB12	I/O	
-	GND	AE12		Internal GND plane
3	VDDIO_3	AE9		Bank3 I/O supply
3	IO_B3D02N_DQ_SWSO	Y12	I/O	
3	IO_B3D02P_DQ_SWSO	AA12	I/O	
3	IO_B3D01N_DQ_SWDO	V12	I/O	
3	IO_B3D01P_DQ_SWDO	W12	I/O	
-	VDD2V5A	K1		Internal VDD2V5A ring
4	IO_B4D15N_DQ_SWSI	Y13	I/O	

4	IO_B4D15P_DQ_SWSI	AA13	I/O	
4	IO_B4D14N_DQ_SWDI	AB13	I/O	
4	IO_B4D14P_DQ_SWDI	AC13	I/O	
-	GND	W14		Internal GND plane
4	VDDIO_4	Y14		Bank4 I/O supply
4	IO_B4D13N_DQS_SWSO	AC14	I/O	
4	IO_B4D13P_DQS_SWSO	AD14	I/O	
4	IO_B4D12N_DQ_SWDO	AD15	I/O	
4	IO_B4D12P_DQ_SWDO	AE15	I/O	
4	VTO_4	AE14		Bk4 Termination voltage
-	GND	M15		Internal GND plane
4	IO_B4D11N_DQ	AB15	I/O	
4	IO_B4D11P_DQ	AC15	I/O	
4	IO_B4D10N_DQ	W15	I/O	
4	IO_B4D10P	Y15	I/O	
-	GND	AA14		Internal GND plane
4	VDDIO_4	AB14		Bank4 I/O supply
4	IO_B4D09N	V14	I/O	
4	IO_B4D09P	V15	I/O	
4	VDDS_4	AE16		Bank4 Switch supply
4	IO_B4D08N	U15	I/O	
4	IO_B4D08P	U16	I/O	
4	IO_B4D07N	V16	I/O	
4	IO_B4D07P	W16	I/O	
-	GND	AE19		Internal GND plane
4	VDDIO_4	AD19		Bank4 I/O supply
4	IO_B4D06N_CAL	Y16	I/O	
4	IO_B4D06P_DQ	AA16	I/O	
4	IO_B4D05N_DQ	AA15	I/O	
4	IO_B4D05P_DQ	AB16	I/O	
-	VDDCORE	J13		Internal VDD1V2 plane
4	VTO_4	AD18		Bk4 Termination voltage
4	IO_B4D04N_DQ_SWSI	AC16	I/O	
4	IO_B4D04P_DQ_SWSI	AC17	I/O	
4	IO_B4D03N_DQS_SWDI	AD17	I/O	
4	IO_B4D03P_DQS_SWDI	AE18	I/O	
-	GND	AD16		Internal GND plane
4	VDDIO_4	AE17		Bank4 I/O supply
4	IO_B4D02N_DQ_SWSO	AA17	I/O	
4	IO_B4D02P_DQ_SWSO	AB17	I/O	
4	IO_B4D01N_DQ_SWDO	AB18	I/O	
4	IO_B4D01P_DQ_SWDO	AC18	I/O	
-	VDD2V5A	K25		Internal VDD2V5A ring
5	IO_B5D15N_DQ_SWSI	AB19	I/O	
5	IO_B5D15P_DQ_SWSI	AC19	I/O	
5	IO_B5D14N_DQ_SWDI	W17	I/O	
5	IO_B5D14P_DQ_SWDI	Y17	I/O	
-	GND	U17		Internal GND plane
5	VDDIO_5	V17		Bank5 I/O supply
5	IO_B5D13N_DQS_SWSO	Y18	I/O	
5	IO_B5D13P_DQS_SWSO	AA18	I/O	
5	IO_B5D12N_DQ_SWDO	V18	I/O	
5	IO_B5D12P_DQ_SWDO	W18	I/O	
5	VTO_5	AD21		Bk5 Termination voltage
-	GND	M17		Internal GND plane
5	IO_B5D11N_DQ	W19	I/O	
5	IO_B5D11P_DQ	Y19	I/O	
5	IO_B5D10N_DQ	AA19	I/O	
5	IO_B5D10P	AA20	I/O	

-	GND	AB24		Internal GND plane
5	VDDIO_5	AC25		Bank5 I/O supply
5	IO_B5D09N	AB20	I/O	
5	IO_B5D09P_CLK1	AC20	I/O	
5	VDDS_5	AE23		Bank52 Switch supply
5	IO_B5D08N	Y20	I/O	
5	IO_B5D08P_CLK0	Y21	I/O	
5	IO_B5D07N	AA21	I/O	
5	IO_B5D07P	AB21	I/O	
-	GND	AD20		Internal GND plane
5	VDDIO_5	AE21		Bank5 I/O supply
5	IO_B5D06N_CAL	AC21	I/O	
5	IO_B5D06P_DQ	AC22	I/O	
5	IO_B5D05N_DQ	AD22	I/O	
5	IO_B5D05P_DQ	AE22	I/O	
-	VDDCORE	N11		Internal VDD1V2 plane
5	VTO_5	AD24		Bk5 Termination voltage
5	IO_B5D04N_DQ_SWSI	AA22	I/O	
5	IO_B5D04P_DQ_SWSI	AB22	I/O	
5	IO_B5D03N_DQS_SWDI	AA23	I/O	
5	IO_B5D03P_DQS_SWDI	AB23	I/O	
-	GND	AD23		Internal GND plane
5	VDDIO_5	AE24		Bank5 I/O supply
5	IO_B5D02N_DQ_SWSO	AC24	I/O	
5	IO_B5D02P_DQ_SWSO	AC23	I/O	
5	IO_B5D01N_DQ_SWDO	AD25	I/O	
5	IO_B5D01P_DQ_SWDO	AE25	I/O	
-	GND	N10		Internal GND plane
-	VDDCORE	N13		Internal VDD1V2 plane
-	GND	T15		Internal GND plane
CG2	CG2_DVDDPLL	T16		PLL2 1.2V Digital Supply
CG2	CG2_ASUBPLL	AA24		PLL2 Substrate -> AGND
CG2	CG2_AVDDPLL	AB25		PLL2 1.2V Analog Supply
CG2	CG2_AGNDPLL	AA25		PLL2 Analog GND
6	IO_B6D15N	Y22	I/O	
6	IO_B6D15P_CLK1	Y23	I/O	
6	IO_B6D14N	W21	I/O	
6	IO_B6D14P_CLK0	W22	I/O	
6	IO_B6D13N	W23	I/O	
6	IO_B6D13P	W24	I/O	
-	VDDCORE	N15		Internal VDD1V2 plane
-	GND	T21		Internal GND plane
6	VDDIO_6	T20		Bank6 I/O supply
6	IO_B6D12N	V25	I/O	
6	IO_B6D12P	W25	I/O	
6	IO_B6D11N	V23	I/O	
6	IO_B6D11P	V24	I/O	
-	GND	N12		Internal GND plane
6	IO_B6D10N	V21	I/O	
6	IO_B6D10P	V22	I/O	
6	IO_B6D09N	V19	I/O	
6	IO_B6D09P	W20	I/O	
-	GND	T23		Internal GND plane
6	VDDIO_6	T24		Bank6 I/O supply
6	IO_B6D08N	U19	I/O	
6	IO_B6D08P	V20	I/O	
6	IO_B6D07N	T18	I/O	
6	IO_B6D07P	U18	I/O	
6	IO_B6D06N	R17	I/O	

6	IO_B6D06P	T17	I/O	
-	VDDCORE	P10		Internal VDD1V2 plane
6	IO_B6D05N	R18	I/O	
6	IO_B6D05P	R19	I/O	
6	IO_B6D04N	T19	I/O	
6	IO_B6D04P	U20	I/O	
-	GND	Y24		Internal GND plane
6	VDDIO_6	Y25		Bank6 I/O supply
-	GND	N14		Internal GND plane
6	IO_B6D03N	U21	I/O	
6	IO_B6D03P	U22	I/O	
6	IO_B6D02N	T22	I/O	
6	IO_B6D02P	U23	I/O	
6	IO_B6D01N	U24	I/O	
6	IO_B6D01P	U25	I/O	
-	VDD2V5A	T1		Internal VDD2V5A ring
6	IO_B7D15N	R20	I/O	
6	IO_B7D15P	R21	I/O	
6	IO_B7D14N	P18	I/O	
6	IO_B7D14P	P19	I/O	
6	IO_B7D13N	P20	I/O	
6	IO_B7D13P	P21	I/O	
-	VDDCORE	P12		Internal VDD1V2 plane
-	GND	L24		Internal GND plane
7	VDDIO_7	L25		Bank7 I/O supply
7	IO_B7D12N	P22	I/O	
7	IO_B7D12P	P23	I/O	
7	IO_B7D11N	P24	I/O	
7	IO_B7D11P	P25	I/O	
-	GND	N16		Internal GND plane
7	IO_B7D10N	N18	I/O	
7	IO_B7D10P	N19	I/O	
7	IO_B7D09N	N20	I/O	
7	IO_B7D09P	N21	I/O	
-	GND	R23		Internal GND plane
7	VDDIO_7	R22		Bank7 I/O supply
7	IO_B7D08N	N22	I/O	
7	IO_B7D08P	N23	I/O	
7	IO_B7D07N	N24	I/O	
7	IO_B7D07P	N25	I/O	
7	IO_B7D06N	M18	I/O	
7	IO_B7D06P	M19	I/O	
-	VDDCORE	P14		Internal VDD1V2 plane
7	IO_B7D05N	M20	I/O	
7	IO_B7D05P	M21	I/O	
7	IO_B7D04N	M22	I/O	
7	IO_B7D04P	M23	I/O	
-	GND	R24		Internal GND plane
7	VDDIO_7	R25		Bank7 I/O supply
-	GND	P9		Internal GND plane
7	IO_B7D03N	M24	I/O	
7	IO_B7D03P	M25	I/O	
7	IO_B7D02N	L22	I/O	
7	IO_B7D02P	L23	I/O	
7	IO_B7D01N	L20	I/O	
7	IO_B7D01P	L21	I/O	
-	VDD2V5A	T25		Internal VDD2V5A ring
8	IO_B8D15N	L17	I/O	
8	IO_B8D15P	L18	I/O	

8	IO_B8D14N	K19	I/O	
8	IO_B8D14P	L19	I/O	
8	IO_B8D13N	K20	I/O	
8	IO_B8D13P	K21	I/O	
-	VDDCORE	P16		Internal VDD1V2 plane
-	GND	F24		Internal GND plane
8	VDDIO_8	F25		Bank8 I/O supply
8	IO_B8D12N	K22	I/O	
8	IO_B8D12P	K23	I/O	
8	IO_B8D11N	H25	I/O	
8	IO_B8D11P	J24	I/O	
-	GND	P11		Internal GND plane
8	IO_B8D10N	J22	I/O	
8	IO_B8D10P	J23	I/O	
8	IO_B8D09N	J20	I/O	
8	IO_B8D09P	J21	I/O	
-	GND	K17		Internal GND plane
8	VDDIO_8	J25		Bank8 I/O supply
8	IO_B8D08N	H23	I/O	
8	IO_B8D08P	H24	I/O	
8	IO_B8D07N	H21	I/O	
8	IO_B8D07P	H22	I/O	
8	IO_B8D06N	J18	I/O	
8	IO_B8D06P	J19	I/O	
-	VDDCORE	R11		Internal VDD1V2 plane
8	IO_B8D05N	J16	I/O	
8	IO_B8D05P	J17	I/O	
8	IO_B8D04N	H19	I/O	
8	IO_B8D04P	H20	I/O	
-	GND	K24		Internal GND plane
8	VDDIO_8	K18		Bank8 I/O supply
-	GND	P13		Internal GND plane
8	IO_B8D03N	G24	I/O	
8	IO_B8D03P	G25	I/O	
8	IO_B8D02N	G21	I/O	
8	IO_B8D02P_CLK1	G22	I/O	
8	IO_B8D01N	F23	I/O	
8	IO_B8D01P_CLK0	G23	I/O	
CG3	CG3_AGNDPLL	E25		PLL3 Analog GND
CG3	CG3_AVDDPLL	D25		PLL3 1.2V Analog Supply
CG3	CG3_ASUBPLL	E24		PLL3 Substrate -> AGND
-	GND	K15		Internal GND plane
CG3	CG3_DVDDPLL	K16		PLL3 1.2V Digital Supply
-	GND	P15		Internal GND plane
-	VDDCORE	R13		Internal VDD1V2 plane
9	IO_B9D15N_DQ_SWSI	F22	I/O	
9	IO_B9D15P_DQ_SWSI	E23	I/O	
9	IO_B9D14N_DQ_SWDI	G20	I/O	
9	IO_B9D14P_DQ_SWDI	F21	I/O	
-	GND	B20		Internal GND plane
9	VDDIO_9	A21		Bank9 I/O supply
9	IO_B9D13N_DQS_SWSO	E22	I/O	
9	IO_B9D13P_DQS_SWSO	D23	I/O	
9	IO_B9D12N_DQ_SWDO	B25	I/O	
9	IO_B9D12P_DQ_SWDO	A25	I/O	
9	VTO_9	B21		Bk9 Termination voltage
-	GND	P17		Internal GND plane
9	IO_B9D11N_DQ	C23	I/O	
9	IO_B9D11P_DQ	C24	I/O	

9	IO_B9D10N_DQ	H18	I/O	
9	IO_B9D10P	G19	I/O	
-	GND	B23		Internal GND plane
9	VDDIO_9	A24		Bank9 I/O supply
9	IO_B9D09N	F20	I/O	
9	IO_B9D09P_CLK1	E21	I/O	
9	VDDS_9	A23		Bank9 Switch supply
9	IO_B9D08N	D22	I/O	
9	IO_B9D08P_CLK0	C22	I/O	
9	IO_B9D07N	D21	I/O	
9	IO_B9D07P	C21	I/O	
9	GND	D24		Internal GND plane
9	VDDIO_9	C25		Bank9 I/O supply
9	IO_B9D06N_CAL	B22	I/O	
9	IO_B9D06P_DQ	A22	I/O	
9	IO_B9D05N_DQ	H17	I/O	
9	IO_B9D05P_DQ	G18	I/O	
-	VDDCORE	R15		Internal VDD1V2 plane
9	VTO_9	B24		Bk9 Termination voltage
9	IO_B9D04N_DQ_SWSI	F19	I/O	
9	IO_B9D04P_DQ_SWSI	E20	I/O	
9	IO_B9D03N_DQS_SWDI	E19	I/O	
9	IO_B9D03P_DQS_SWDI	D20	I/O	
-	GND	F18		Internal GND plane
9	VDDIO_9	G17		Bank9 I/O supply
9	IO_B9D02N_DQ_SWSO	E18	I/O	
9	IO_B9D02P_DQ_SWSO	D19	I/O	
9	IO_B9D01N_DQ_SWDO	C19	I/O	
9	IO_B9D01P_DQ_SWDO	C20	I/O	
-	VDD2V5A	AE6		Internal VDD2V5A ring
10	IO_B10D15N_DQ_SWSI	H16	I/O	
10	IO_B10D15P_DQ_SWSI	G16	I/O	
10	IO_B10D14N_DQ_SWDI	F17	I/O	
10	IO_B10D14P_DQ_SWDI	E17	I/O	
-	GND	A19		Internal GND plane
10	VDDIO_10	A15		Bank10 I/O supply
10	IO_B10D13N_DQS_SWSO	D18	I/O	
10	IO_B10D13P_DQS_SWSO	C18	I/O	
10	IO_B10D12N_DQ_SWDO	A17	I/O	
10	IO_B10D12P_DQ_SWDO	A18	I/O	
10	VTO_10	B14		Bk10 Termination voltage
-	GND	R10		Internal GND plane
10	IO_B10D11N_DQ	J15	I/O	
10	IO_B10D11P_DQ	H15	I/O	
10	IO_B10D10N_DQ	G15	I/O	
10	IO_B10D10P	F16	I/O	
-	GND	B16		Internal GND plane
10	VDDIO_10	B13		Bank10 I/O supply
10	IO_B10D09N	F15	I/O	
10	IO_B10D09P	E16	I/O	
10	VDDS_10	A16		Bank10 Switch supply
10	IO_B10D08N	D16	I/O	
10	IO_B10D08P	D17	I/O	
10	IO_B10D07N	C17	I/O	
10	IO_B10D07P	B17	I/O	
-	GND	C14		Internal GND plane
10	VDDIO_10	B19		Bank10 I/O supply
10	IO_B10D06N_CAL	H14	I/O	
10	IO_B10D06P_DQ	G14	I/O	

10	IO_B10D05N_DQ	F14	I/O	
10	IO_B10D05P_DQ	E15	I/O	
-	VDDCORE	T12		Internal VDD1V2 plane
10	VTO_10	B18		Bk10 Termination voltage
10	IO_B10D04N_DQ_SWSI	D15	I/O	
10	IO_B10D04P_DQ_SWSI	C16	I/O	
10	IO_B10D03N_DQS_SWDI	B15	I/O	
10	IO_B10D03P_DQS_SWDI	A14	I/O	
-	GND	G13		Internal GND plane
10	VDDIO_10	H13		Bank10 I/O supply
10	IO_B10D02N_DQ_SWSO	D14	I/O	
10	IO_B10D02P_DQ_SWSO	C15	I/O	
10	IO_B10D01N_DQ_SWDO	F13	I/O	
10	IO_B10D01P_DQ_SWDO	E14	I/O	
-	VDD2V5A	AE13		Internal VDD2V5A ring
11	IO_B11D15N_DQ_SWSI	H12	I/O	
11	IO_B11D15P_DQ_SWSI	G12	I/O	
11	IO_B11D14N_DQ_SWDI	E13	I/O	
11	IO_B11D14P_DQ_SWDI	D13	I/O	
-	GND	A7		Internal GND plane
11	VDDIO_11	A9		Bank11 I/O supply
11	IO_B11D13N_DQS_SWSO	C12	I/O	
11	IO_B11D13P_DQS_SWSO	B12	I/O	
11	IO_B11D12N_DQ_SWDO	J11	I/O	
11	IO_B11D12P_DQ_SWDO	H11	I/O	
11	VTO_11	A12		Bk11 Termination voltage
-	GND	R12		Internal GND plane
11	IO_B11D11N_DQ	G11	I/O	
11	IO_B11D11P_DQ	F11	I/O	
11	IO_B11D10N_DQ	E11	I/O	
11	IO_B11D10P	D11	I/O	
-	GND	B10		Internal GND plane
11	VDDIO_11	B7		Bank11 I/O supply
11	IO_B11D09N	B11	I/O	
11	IO_B11D09P	A11	I/O	
11	VDDS_11	A10		Bank11 Switch supply
11	IO_B11D08N	C10	I/O	
11	IO_B11D08P	C11	I/O	
11	IO_B11D07N	E10	I/O	
11	IO_B11D07P	D10	I/O	
11	GND	C13		Internal GND plane
11	VDDIO_11	D12		Bank11 I/O supply
11	IO_B11D06N_CAL	D9	I/O	
11	IO_B11D06P_DQ	C9	I/O	
11	IO_B11D05N_DQ	B9	I/O	
11	IO_B11D05P_DQ	A8	I/O	
-	VDDCORE	T14		Internal VDD1V2 plane
11	VTO_11	B8		Bk11 Termination voltage
11	IO_B11D04N_DQ_SWSI	F10	I/O	
11	IO_B11D04P_DQ_SWSI	E9	I/O	
11	IO_B11D03N_DQS_SWDI	D8	I/O	
11	IO_B11D03P_DQS_SWDI	C8	I/O	
-	GND	E12		Internal GND plane
11	VDDIO_11	F12		Bank11 I/O supply
11	IO_B11D02N_DQ_SWSO	H10	I/O	
11	IO_B11D02P_DQ_SWSO	G10	I/O	
11	IO_B11D01N_DQ_SWDO	F9	I/O	
11	IO_B11D01P_DQ_SWDO	E8	I/O	
-	VDD2V5A	AE20		Internal VDD2V5A ring

12	IO_B12D15N_DQ_SWSI	G9	I/O	
12	IO_B12D15P_DQ_SWSI	F8	I/O	
12	IO_B12D14N_DQ_SWDI	H9	I/O	
12	IO_B12D14P_DQ_SWDI	G8	I/O	
-	GND	B3		Internal GND plane
12	VDDIO_12	A2		Bank12 I/O supply
12	IO_B12D13N_DQS_SWSO	H8	I/O	
12	IO_B12D13P_DQS_SWSO	G7	I/O	
12	IO_B12D12N_DQ_SWDO	C7	I/O	
12	IO_B12D12P_DQ_SWDO	C6	I/O	
12	VTO_12	B2		Bk12 Termination voltage
-	GND	R14		Internal GND plane
12	IO_B12D11N_DQ	E7	I/O	
12	IO_B12D11P_DQ	D7	I/O	
12	IO_B12D10N_DQ	D6	I/O	
12	IO_B12D10P	C5	I/O	
-	GND	B6		Internal GND plane
12	VDDIO_12	A5		Bank12 I/O supply
12	IO_B12D09N	F7	I/O	
12	IO_B12D09P_CLK1	E6	I/O	
12	VDDS_12	A3		Bank12 Switch supply
12	IO_B12D08N	B4	I/O	
12	IO_B12D08P_CLK0	A4	I/O	
12	IO_B12D07N	D5	I/O	
12	IO_B12D07P	C4	I/O	
12	GND	D2		Internal GND plane
12	VDDIO_12	C1		Bank12 I/O supply
12	IO_B12D06N_CAL	E5	I/O	
12	IO_B12D06P_DQ	D4	I/O	
12	IO_B12D05N_DQ	C2	I/O	
12	IO_B12D05P_DQ	C3	I/O	
-	VDDCORE	U12		Internal VDD1V2 plane
12	VTO_12	B5		Bk12 Termination voltage
12	IO_B12D04N_DQ_SWSI	B1	I/O	
12	IO_B12D04P_DQ_SWSI	A1	I/O	
12	IO_B12D03N_DQS_SWDI	E4	I/O	
12	IO_B12D03P_DQS_SWDI	D3	I/O	
-	GND	J10		Internal GND plane
12	VDDIO_12	J9		Bank12 I/O supply
12	IO_B12D02N_DQ_SWSO	F6	I/O	
12	IO_B12D02P_DQ_SWSO	F5	I/O	
12	IO_B12D01N_DQ_SWDO	F4	I/O	
12	IO_B12D01P_DQ_SWDO	E3	I/O	
-	GND	R16		Internal GND plane
-	VDDCORE	U14		Internal VDD1V2 plane
CG0	CG0_DVDDPLL	K10		PLL0 1.2V Digital Supply
-	GND	K11		Internal GND plane
CG0	CG0_ASUBPLL	E2		PLL0 Substrate -> AGND
CG0	CG0_AVDDPLL	D1		PLL0 1.2V Analog Supply
CG0	CG0_AGNDPLL	E1		PLL0 Analog GND
-	GND	T13		Internal GND plane
-	GND	U13		Internal GND plane
-	VDDCORE	N17		Internal VDD1V2 plane

Table 30: LGA/CGA 625 Pin-out

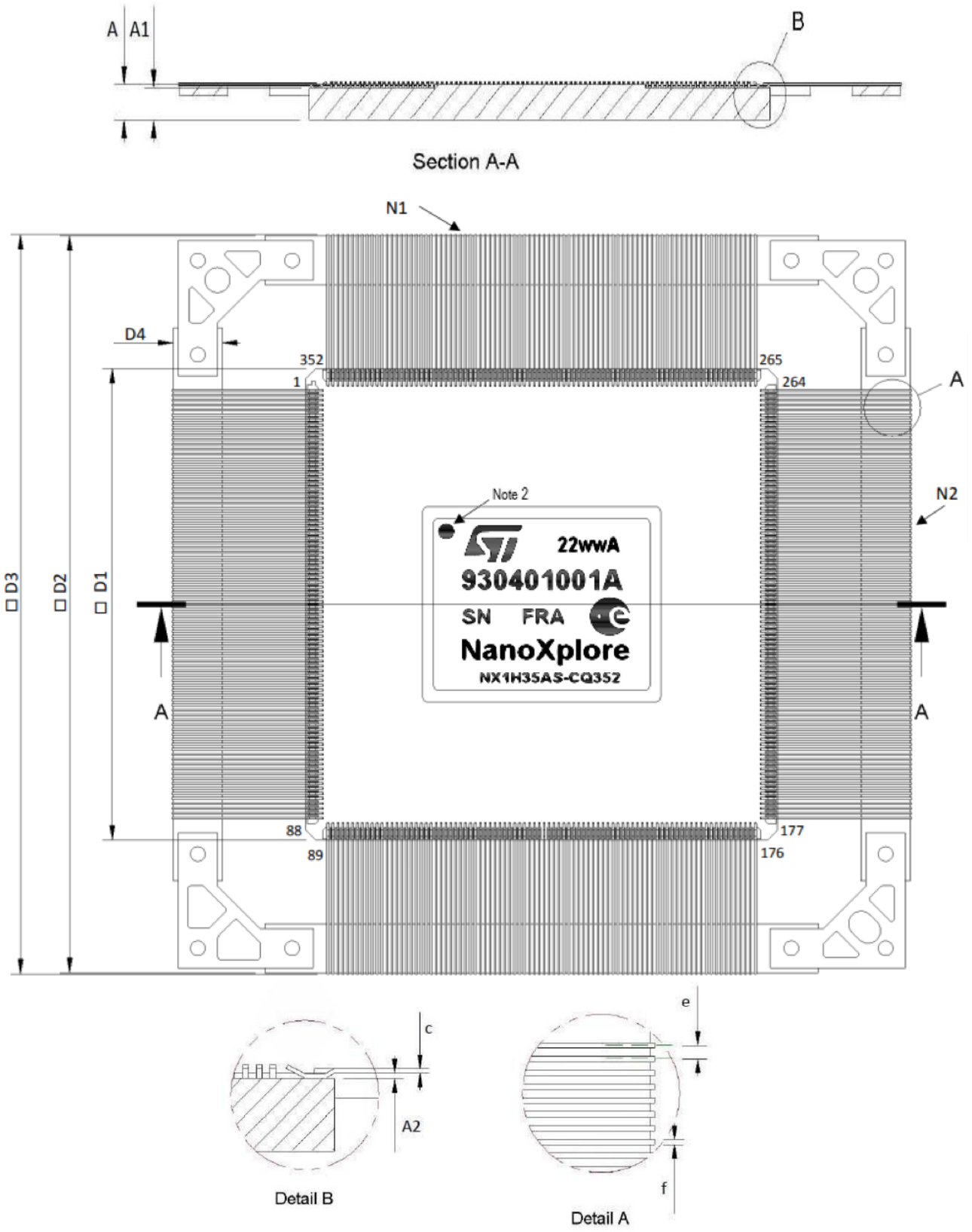


Figure 33: CQFP352 mechanical outline

Symbols	Dimensions mm		Notes
	Min	Max	
A	2.52	3.51	
c	0.1	0.17	
D1	47.67	48.33	1
D2	74.62	75.38	
D3	74.87	76.01	
D4	4.5	5.5	
e	0.5 BSC		
f			1
A1	0.17	0.24	
A2	2.37	2.87	1
N1	88 Leads		
N2	88 Leads		

NOTES:

1. **Applies to all leads.**
2. **Terminal identification is specified by reference to the index corner as shown.**

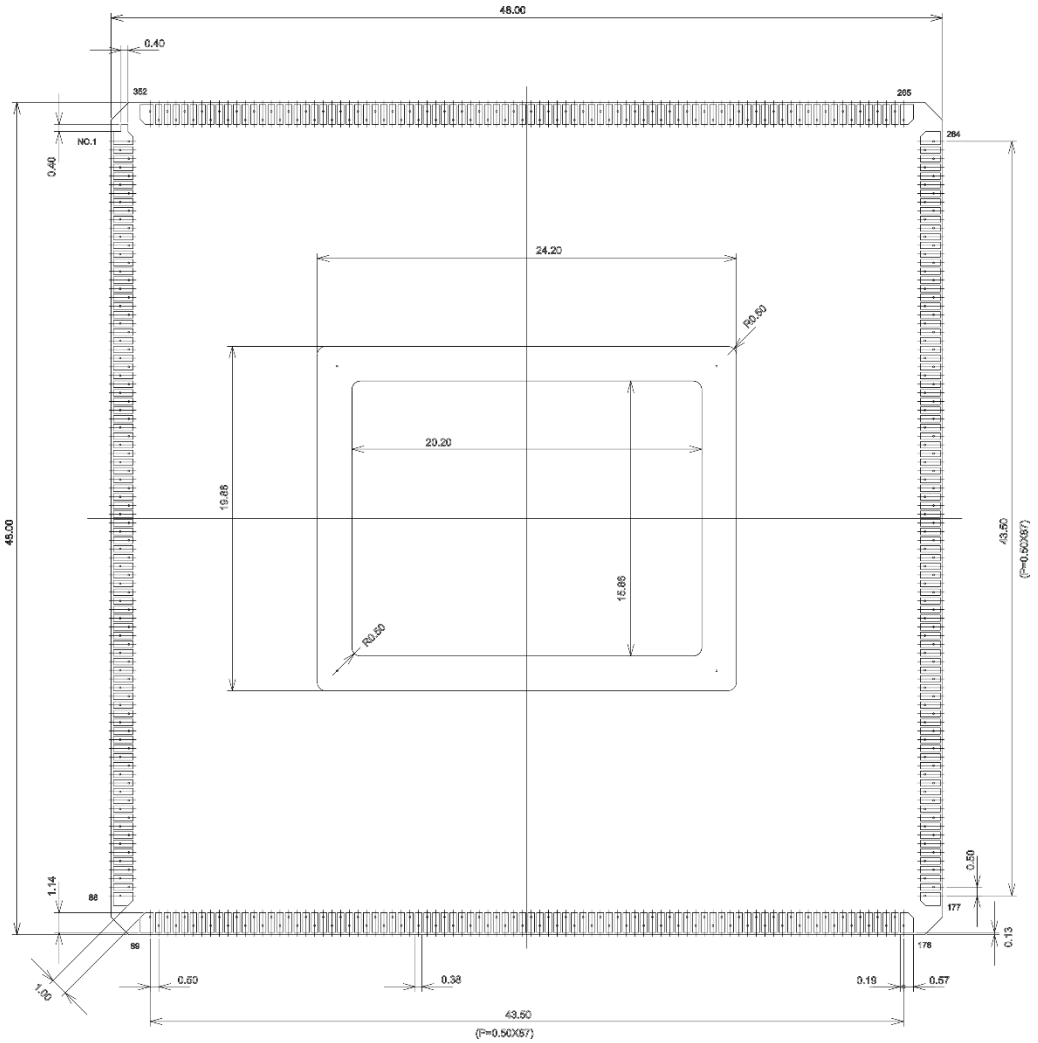


Figure 34: CQFP352 Preformed Leads (by Assembler)

CQFP352 package gives access to only 192 of the 374 die's user I/Os

Bank	Type	I/Os
0	Simple	14
2	Complex	30
4	Complex	-
6	Simple	22
8	Simple	24
9	Complex	30
11	Complex	-

Bank	Type	I/Os
1	Simple	12
3	Complex	-
5	Complex	30
7	Simple	-
10	Complex	-
12	Complex	30

Table 31: CQFP352 I/O banks

Bank	Pin Name	Pin Nbr	I/O	Description
0	IO_B0D11N	351	I/O	
0	IO_B0D11P_CLK1	352	I/O	
0	IO_B0D10N	1	I/O	
0	IO_B0D10P_CLK0	2	I/O	
-	VDDSENSE	3		VDDCORE Sense return
0	GND	4		Internal GND plane
0	VDDIO_0	5		Bank0 I/O supply
0	IO_B0D09N	6	I/O	
0	IO_B0D09P	7	I/O	
-	GNDCORE	8		Internal GND plane
0	IO_B0D08N	9	I/O	
0	IO_B0D08P	10	I/O	
0	IO_B0D07N	11	I/O	
0	IO_B0D07P	12	I/O	
0	VDDIO_0	13		Bank0 I/O supply
0	IO_B0D06N	14	I/O	
0	IO_B0D06P	15	I/O	
0	IO_B0D05N	16	I/O	
0	IO_B0D05P	17	I/O	
-	VDDCORE	18		Internal VDD1V2 plane
-	GND	19		Internal GND plane
-	VDD2V5A	20		Internal VDD2V5A ring
Prog	GND	21		Internal GND plane
Prog	DOUT_P	22	O	Configuration Spacewire
Prog	DOUT_N	23	O	Configuration Spacewire
-	GND	24		Internal GND plane
Prog	SOUT_P	25	O	Configuration Spacewire
Prog	SOUT_N	26	O	Configuration Spacewire
Prog	DIN_P	27	I	Configuration Spacewire
Prog	DIN_N	28	I	Configuration Spacewire
-	VDDCORE	29		Internal VDD1V2 plane
Prog	SIN_P	30	I	Configuration Spacewire
Prog	SIN_N	31	I	Configuration Spacewire
Prog	VDDLVDS	32		2.5V LVDS supply
Prog	RST_N	33	I	Hardware Reset input
Prog	MODE0	34	I	Cfg Mode input
Prog	MODE1	35	I	Cfg Mode input
Prog	MODE2	36	I	Cfg Mode input
-	GND	37		Internal GND plane
Prog	MODE3	38	I	Cfg Mode input
Prog	ERROR	39	O	Cfg Error output
Prog	TCK	40	I	JTAG Clock input

Prog	TRST	41	I	Active-low JTAG Reset input
Prog	CLK	42	I	SlavePar Clock input
Prog	TMS	43	I	JTAG TMS input
Prog	TDI	44	I	JTAG TDI input
Prog	TDO	45	O	JTAG TDO output
Prog	VDDIO_SERVICE	46		3.3V Prog supply
-	GND	47		Internal GND plane
Prog	READY	48	O	Cfg Ready output
Prog	D0	49	I/O	SlavePar Data bit 0
Prog	D1	50	I/O	SlavePar Data bit 1
Prog	D2	51	I/O	SlavePar Data bit 2
Prog	D3	52	I/O	SlavePar Data bit 3
Prog	D4	53	I/O	SlavePar Data bit 4
Prog	D5	54	I/O	SlavePar Data bit 5
Prog	D6	55	I/O	SlavePar Data bit 6
Prog	VDDIO_SERVICE	56		3.3V Prog supply
-	GND	57		Internal GND plane
Prog	D7	58	I/O	SlavePar Data bit 7
Prog	D8	59	I/O	SlavePar Data bit 8
Prog	D9	60	I/O	SlavePar Data bit 9
Prog	D10	61	I/O	SlavePar Data bit 10
Prog	D11	62	I/O	SlavePar Data bit 11
Prog	D12	63	I/O	SlavePar Data bit 12
Prog	D13	64	I/O	SlavePar Data bit 13
Prog	D14	65	I/O	SlavePar Data bit 14
-	GND	66		Internal GND plane
Prog	D15	67	I/O	SlavePar Data bit 15
Prog	CS_N	68	I	SlavePar Chip Select input
Prog	WE_N	69	I	SlavePar Write Enable input
Prog	DATA_OE	70	O	SlavePar Data available output
-	VDD2V5A	71		Internal VDD2V5A ring
-	VDDCORE	72		Internal VDD1V2 plane
-	GND	73		Internal GND plane
1	VDDIO_1	74		Bank1 I/O supply
1	IO_B1D06N	75	I/O	
1	IO_B1D06P	76	I/O	
1	IO_B1D05N	77	I/O	
1	IO_B1D05P	78	I/O	
-	VDDCORE	79		Internal VDD1V2 plane
1	IO_B1D04N	80	I/O	
1	IO_B1D04P	81	I/O	
1	IO_B1D03N	82	I/O	
1	IO_B1D03P	83	I/O	
-	GND	84		Internal GND plane
1	VDDIO_1	85		Bank1 I/O supply
-	GND	86		Internal GND plane
1	IO_B1D02N	87	I/O	
1	IO_B1D02P_CLK1	88	I/O	
1	IO_B1D01N	89	I/O	
1	IO_B1D01P_CLK0	90	I/O	
CG1	CG1_AGNDPLL	91		PLL1 Analog GND
CG1	CG1_AVDDPLL	92		PLL1 1.2V Analog Supply
-	GND	93		Internal GND plane
-	VDDCORE	94		Internal VDD1V2 plane
2	IO_B2D15N_DQ_SWSI	95	I/O	
2	IO_B2D15P_DQ_SWSI	96	I/O	
2	IO_B2D14N_DQ_SWDI	97	I/O	
2	IO_B2D14P_DQ_SWDI	98	I/O	
-	GND	99		Internal GND plane

2	VDDIO_2	100		Bank2 I/O supply
2	IO_B2D13N_DQS_SWSO	101	I/O	
2	IO_B2D13P_DQS_SWSO	102	I/O	
2	IO_B2D12N_DQ_SWDO	103	I/O	
2	IO_B2D12P_DQ_SWDO	104	I/O	
2	VTO_2	105		Bk2 Termination voltage
2	IO_B2D11N_DQ	106	I/O	
2	IO_B2D11P_DQ	107	I/O	
2	IO_B2D10N_DQ	108	I/O	
2	IO_B2D10P	109	I/O	
-	GND	110		Internal GND plane
2	VDDIO_2	111		Bank2 I/O supply
2	IO_B2D09N	112	I/O	
2	IO_B2D09P_CLK1	113	I/O	
2	VDDS_2	114		Bank2 Switch supply
2	IO_B2D08N	115	I/O	
2	IO_B2D08P_CLK0	116	I/O	
2	IO_B2D07N	117	I/O	
2	IO_B2D07P	118	I/O	
-	GND	119		Internal GND plane
2	VDDIO_2	120		Bank2 I/O supply
2	IO_B2D06N_CAL	121	I/O	
2	IO_B2D06P_DQ	122	I/O	
2	IO_B2D05N_DQ	123	I/O	
2	IO_B2D05P_DQ	124	I/O	
2	VTO_2	125		Bk2 Termination voltage
2	IO_B2D04N_DQ_SWSI	126	I/O	
2	IO_B2D04P_DQ_SWSI	127	I/O	
2	IO_B2D03N_DQS_SWDI	128	I/O	
2	IO_B2D03P_DQS_SWDI	129	I/O	
-	GND	130		Internal GND plane
2	VDDIO_2	131		Bank2 I/O supply
2	IO_B2D02N_DQ_SWSO	132	I/O	
2	IO_B2D02P_DQ_SWSO	133	I/O	
2	IO_B2D01N_DQ_SWDO	134	I/O	
2	IO_B2D01P_DQ_SWDO	135	I/O	
-	VDD2V5A	136		Internal VDD2V5A ring
-	GND	137		Internal GND plane
-	VDDCORE	138		Internal VDD1V2 plane
-	VDD2V5A	139		Internal VDD2V5A ring
-	GND	140		Internal GND plane
-	VDDCORE	141		Internal VDD1V2 plane
-	VDD2V5A	142		Internal VDD2V5A ring
5	IO_B5D15N_DQ_SWSI	143	I/O	
5	IO_B5D15P_DQ_SWSI	144	I/O	
5	IO_B5D14N_DQ_SWDI	145	I/O	
5	IO_B5D14P_DQ_SWDI	146	I/O	
-	GND	147		Internal GND plane
5	VDDIO_5	148		Bank5 I/O supply
5	IO_B5D13N_DQS_SWSO	149	I/O	
5	IO_B5D13P_DQS_SWSO	150	I/O	
5	IO_B5D12N_DQ_SWDO	151	I/O	
5	IO_B5D12P_DQ_SWDO	152	I/O	
5	VTO_5	153		Bk5 Termination voltage
5	IO_B5D11N_DQ	154	I/O	
5	IO_B5D11P_DQ	155	I/O	
5	IO_B5D10N_DQ	156	I/O	
5	IO_B5D10P	157	I/O	
-	GND	158		Internal GND plane

5	VDDIO_5	159		Bank5 I/O supply
5	IO_B5D09N	160	I/O	
5	IO_B5D09P_CLK1	161	I/O	
5	VDDS_5	162		Bank52 Switch supply
5	IO_B5D08N	163	I/O	
5	IO_B5D08P_CLK0	164	I/O	
5	IO_B5D07N	165	I/O	
5	IO_B5D07P	166	I/O	
-	GND	167		Internal GND plane
5	VDDIO_5	168		Bank5 I/O supply
5	IO_B5D06N_CAL	169	I/O	
5	IO_B5D06P_DQ	170	I/O	
5	IO_B5D05N_DQ	171	I/O	
5	IO_B5D05P_DQ	172	I/O	
5	VTO_5	173		Bk5 Termination voltage
5	IO_B5D04N_DQ_SWSI	174	I/O	
5	IO_B5D04P_DQ_SWSI	175	I/O	
5	IO_B5D03N_DQS_SWDI	176	I/O	
5	IO_B5D03P_DQS_SWDI	177	I/O	
-	GND	178		Internal GND plane
5	VDDIO_5	179		Bank5 I/O supply
5	IO_B5D02N_DQ_SWSO	180	I/O	
5	IO_B5D02P_DQ_SWSO	181	I/O	
5	IO_B5D01N_DQ_SWDO	182	I/O	
5	IO_B5D01P_DQ_SWDO	183	I/O	
-	GND	184		Internal GND plane
-	VDDCORE	185		Internal VDD1V2 plane
CG2	CG2_AVDDPLL	186		PLL2 1.2V Analog Supply
CG2	CG2_AGNDPLL	187		PLL2 Analog GND
6	IO_B6D15N	188	I/O	
6	IO_B6D15P_CLK1	189	I/O	
6	IO_B6D14N	190	I/O	
6	IO_B6D14P_CLK0	191	I/O	
6	IO_B6D13N	192	I/O	
6	IO_B6D13P	193	I/O	
-	VDDCORE	194		Internal VDD1V2 plane
-	GND	195		Internal GND plane
6	VDDIO_6	196		Bank6 I/O supply
6	IO_B6D12N	197	I/O	
6	IO_B6D12P	198	I/O	
6	IO_B6D11N	199	I/O	
6	IO_B6D11P	200	I/O	
-	GND	201		Internal GND plane
6	IO_B6D10N	202	I/O	
6	IO_B6D10P	203	I/O	
6	IO_B6D09N	204	I/O	
6	IO_B6D09P	205	I/O	
-	GND	206		Internal GND plane
6	VDDIO_6	207		Bank6 I/O supply
6	IO_B6D08N	208	I/O	
6	IO_B6D08P	209	I/O	
6	IO_B6D07N	210	I/O	
6	IO_B6D07P	211	I/O	
6	IO_B6D06N	212	I/O	
6	IO_B6D06P	213	I/O	
-	VDDCORE	214		Internal VDD1V2 plane
6	IO_B6D05N	215	I/O	
6	IO_B6D05P	216	I/O	
-	GND	217		Internal GND plane

-	VDD2V5A	218		Internal VDD2V5A ring
-	VDDCORE	219		Internal VDD1V2 plane
-	GND	220		Internal GND plane
-	VDD2V5A	221		Internal VDD2V5A ring
-	VDDCORE	222		Internal VDD1V2 plane
8	IO_B8D12N	223	I/O	
8	IO_B8D12P	224	I/O	
8	IO_B8D11N	225	I/O	
8	IO_B8D11P	226	I/O	
-	GND	227		Internal GND plane
8	IO_B8D10N	228	I/O	
8	IO_B8D10P	229	I/O	
8	IO_B8D09N	230	I/O	
8	IO_B8D09P	231	I/O	
-	GND	232		Internal GND plane
8	VDDIO_8	233		Bank8 I/O supply
8	IO_B8D08N	234	I/O	
8	IO_B8D08P	235	I/O	
8	IO_B8D07N	236	I/O	
8	IO_B8D07P	237	I/O	
8	IO_B8D06N	238	I/O	
8	IO_B8D06P	239	I/O	
-	VDDCORE	240		Internal VDD1V2 plane
8	IO_B8D05N	241	I/O	
8	IO_B8D05P	242	I/O	
8	IO_B8D04N	243	I/O	
8	IO_B8D04P	244	I/O	
-	GND	245		Internal GND plane
8	VDDIO_8	246		Bank8 I/O supply
-	GND	247		Internal GND plane
8	IO_B8D03N	248	I/O	
8	IO_B8D03P	249	I/O	
8	IO_B8D02N	250	I/O	
8	IO_B8D02P_CLK1	251	I/O	
8	IO_B8D01N	252	I/O	
8	IO_B8D01P_CLK0	253	I/O	
CG3	CG3_AGNDPLL	254		PLL3 Analog GND
CG3	CG3_AVDDPLL	255		PLL3 1.2V Analog Supply
-	GND	256		Internal GND plane
-	VDDCORE	257		Internal VDD1V2 plane
9	IO_B9D15N_DQ_SWSI	258	I/O	
9	IO_B9D15P_DQ_SWSI	259	I/O	
9	IO_B9D14N_DQ_SWDI	260	I/O	
9	IO_B9D14P_DQ_SWDI	261	I/O	
-	GND	262		Internal GND plane
9	VDDIO_9	263		Bank9 I/O supply
9	IO_B9D13N_DQS_SWSO	264	I/O	
9	IO_B9D13P_DQS_SWSO	265	I/O	
9	IO_B9D12N_DQ_SWDO	266	I/O	
9	IO_B9D12P_DQ_SWDO	267	I/O	
9	VTO_9	268		Bk9 Termination voltage
9	IO_B9D11N_DQ	269	I/O	
9	IO_B9D11P_DQ	270	I/O	
9	IO_B9D10N_DQ	271	I/O	
9	IO_B9D10P	272	I/O	
-	GND	273		Internal GND plane
9	VDDIO_9	274		Bank9 I/O supply
9	IO_B9D09N	275	I/O	
9	IO_B9D09P_CLK1	276	I/O	

9	VDDS_9	277		Bank9 Switch supply
9	IO_B9D08N	278	I/O	
9	IO_B9D08P_CLK0	279	I/O	
9	IO_B9D07N	280	I/O	
9	IO_B9D07P	281	I/O	
9	GND	282		Internal GND plane
9	VDDIO_9	283		Bank9 I/O supply
9	IO_B9D06N_CAL	284	I/O	
9	IO_B9D06P_DQ	285	I/O	
9	IO_B9D05N_DQ	286	I/O	
9	IO_B9D05P_DQ	287	I/O	
9	VTO_9	288		Bk9 Termination voltage
9	IO_B9D04N_DQ_SWSI	289	I/O	
9	IO_B9D04P_DQ_SWSI	290	I/O	
9	IO_B9D03N_DQS_SWDI	291	I/O	
9	IO_B9D03P_DQS_SWDI	292	I/O	
-	GND	293		Internal GND plane
9	VDDIO_9	294		Bank9 I/O supply
9	IO_B9D02N_DQ_SWSO	295	I/O	
9	IO_B9D02P_DQ_SWSO	296	I/O	
9	IO_B9D01N_DQ_SWDO	297	I/O	
9	IO_B9D01P_DQ_SWDO	298	I/O	
-	VDD2V5A	299		Internal VDD2V5A ring
-	GND	300		Internal GND plane
-	VDDCORE	301		Internal VDD1V2 plane
-	VDD2V5A	302		Internal VDD2V5A ring
-	GND	303		Internal GND plane
-	VDDCORE	304		Internal VDD1V2 plane
-	VDD2V5A	305		Internal VDD2V5A ring
12	IO_B12D15N_DQ_SWSI	306	I/O	
12	IO_B12D15P_DQ_SWSI	307	I/O	
12	IO_B12D14N_DQ_SWDI	308	I/O	
12	IO_B12D14P_DQ_SWDI	309	I/O	
-	GND	310		Internal GND plane
12	VDDIO_12	311		Bank12 I/O supply
12	IO_B12D13N_DQS_SWSO	312	I/O	
12	IO_B12D13P_DQS_SWSO	313	I/O	
12	IO_B12D12N_DQ_SWDO	314	I/O	
12	IO_B12D12P_DQ_SWDO	315	I/O	
12	VTO_12	316		Bk12 Termination voltage
12	IO_B12D11N_DQ	317	I/O	
12	IO_B12D11P_DQ	318	I/O	
12	IO_B12D10N_DQ	319	I/O	
12	IO_B12D10P	320	I/O	
-	GND	321		Internal GND plane
12	VDDIO_12	322		Bank12 I/O supply
12	IO_B12D09N	323	I/O	
12	IO_B12D09P_CLK1	324	I/O	
12	VDDS_12	325		Bank12 Switch supply
12	IO_B12D08N	326	I/O	
12	IO_B12D08P_CLK0	327	I/O	
12	IO_B12D07N	328	I/O	
12	IO_B12D07P	329	I/O	
12	GND	330		Internal GND plane
12	VDDIO_12	331		Bank12 I/O supply
12	IO_B12D06N_CAL	332	I/O	
12	IO_B12D06P_DQ	333	I/O	
12	IO_B12D05N_DQ	334	I/O	
12	IO_B12D05P_DQ	335	I/O	

12	VTO_12	336		Bk12 Termination voltage
12	IO_B12D04N_DQ_SWSI	337	I/O	
12	IO_B12D04P_DQ_SWSI	338	I/O	
12	IO_B12D03N_DQS_SWDI	339	I/O	
12	IO_B12D03P_DQS_SWDI	340	I/O	
-	GND	341		Internal GND plane
12	VDDIO_12	342		Bank12 I/O supply
12	IO_B12D02N_DQ_SWSO	343	I/O	
12	IO_B12D02P_DQ_SWSO	344	I/O	
12	IO_B12D01N_DQ_SWDO	345	I/O	
12	IO_B12D01P_DQ_SWDO	346	I/O	
-	GND	347		Internal GND plane
-	VDDCORE	348		Internal VDD1V2 plane
CG0	CG0_AVDDPLL	349		PLL0 1.2V Analog Supply
CG0	CG0_AGNDPLL	350		PLL0 Analog GND

Table 32: CQFP-352 Pin-out (Preliminary)

10 Ordering Information

9304010 01 A

Screening level :
. A : 300krad(Si)

Packaging :
. 01 : CQ352 (Ceramic Quad-Flat package 352 pins)
. 02 : LG625 (Ceramic Land-Grid array, 625 pins, 29x29mm body, 1,0mm pitch)

Detail Specification Reference :
9304/010 : ESCC Detail Specification Reference - FPGA matrix (named NG-MEDIUM)

NX1H35AS device and package combinations

Part Number	FPGA Matrix	Package	Temperature range	Quality level
930401001A	NX1H35AS	CQFP-352	-55°c to 125°c	ESCC9000
930401002A	NX1H35AS	CLGA-625	-55°c to 125°c	ESCC9000

Contact NanoXplore Marketing & Sales @ sales@nanoxplore.com for more information.

11 Glossary

Acronym	Description
ALU	Arithmetic Logic Unit
CG	Clock Generator
CGA	Column Grid Array
CMIC	Configuration Memory Integrity Check
CMOS	Complementary Metal Oxide Semiconductor
DDR	Double Data Rate
DFF	D-Flip Flop
DPRAM	Dual-Port Read Access Memory
DSP	Digital Signal Processor
ECC	Error Correction Circuit
EDAC	Error Detection And Correction
FPGA	Field Programmable Gate Array
HSTL	High-Speed Transceiver Logic
IOB	Input Output Block
LGA	Land Grid Array
LUT	Look-Up Table
LVCMOS	Low Voltage CMOS
LVDS	Low Voltage Differential Signal
CQFP	Multilayer Quad Flat Package
PCI	Peripheral Component Interconnect
PLL	Phase-Locked Loop
RH	Radiation Hardened
RHBD	Radiation Hardened By Design

SECDED	Single Error Detection, Double Error Detection
SEFI	Single-Event Functional Interrupt
SEL	Single-Event Latch-up
SER	Soft-Error Rate
SET	Single-Event Transient
SEU	Single-Event Upset
SpW Tx & Rx	SpaceWire Transceiver & Receiver
SSTL	Stub Series Terminated Logic

12 Revision history

The following table shows the revision history of the NX1H35S and NX1H35AS datasheet

Date	Version	Revision
2022-04-11	1.0	Initial NX datasheet
2022-04-21	1.0.1	Addition of DDR2 bytelane mapping
2022-05-04	1.0.2	Correction on VOD values for LVDS
2022-05-18	1.0.3	Add Single-ended characterization of LVDS IO pads
2022-05-19	1.0.4	Add configuration mode sections
2022-10-06	1.0.5	Part number ESCC9000
2022-10-14	1.0.6	Package description Updated
2023-01-02	1.0.7	Fix bitstream size estimation
2023-09-01	1.0.8	Clarify termination power supplies chapters
2024-01-08	1.0.9	Delay Line tap accuracy
2024-03-05	1.0.10	PLL information
2024-04-18	1.0.11	Add more details on power supplies sequencing chapter
2025-07-23	1.0.12	Clarification in Power Supplies – Bank supplies use cases Correction in Power supplies sequencing