Brave NG_Medium

(NX1H35S)

CLGA625 DevKit V3

User Guide

Revision	Date	Originator	Comments
1.04	09/17/2018	Christian Magne	DevKit V2 - > V3 evolution

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1 Introduction

1.1 Scope of the document

This document describes NanoXplore BRAVE/NX1H35 CLGA625 Development Kit, V3 board.

1.2 Applicable and Reference Document

1.2.1 Applicable and Reference Document (ADs)

1.2.2 Reference Documents (RDs)

2 Background and Objectives

2.1 General Background

The DevKit is a demonstration board for Brave NG_MEDIUM CLGA625 chip.

Board has been upgraded from V0 to V1 for 2 reasons:

- mechanical dimensions had to be increased to ease production : surface-mount connectors were too close to the board edge.
- FMC connector orientation was wrong.

Board has been upgraded from V1 to V2 in September 2017, with the following changes:

- Due to an early documentation error, SpaceWire I/Os distribution on complex banks were erroneous, so DevKit V1 SpaceWire performance won't reach the 400Mbit/S target. On DevKit V2, User1 and User2 SpaceWire connectors have access to the integrated SpaceWire-enhanced functions of the complex bank.
- The correction for the not-fully-asynchronous JTAG reset has been integrated (schottky diode providing a single JTAG clock pulse on RST_N rising edge).
- Calibration resistors have been added on 3 complex banks' D06N_CAL I/O.
- VDDSENSE voltage measurement has been added.
- Primary 12V input current measurement has been added.

Three V0 boards have been produced in November 2016, using 1st run NG_MEDIUM silicon.

Thirty V1 boards have been produced with 2nd run chips, after mask fix.

Board has been upgraded from V2 to V3 in June 2018, with the following changes :

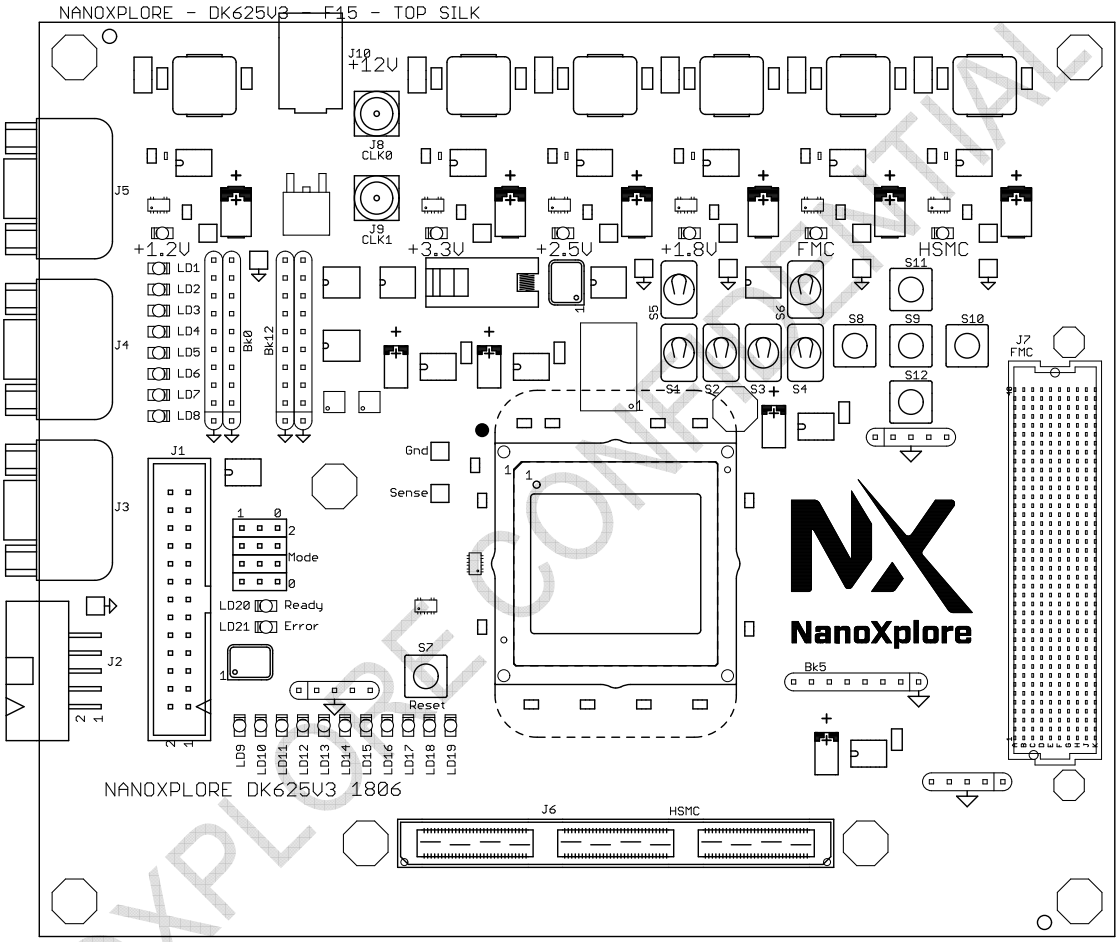
- A 4th jumper has been added for MODE3 mode pin.
- Four 0805 resistor footprints have been added to J3 Prog interface Spacewire inputs, for common-mode correction with current-mode LVDS outputs.

2.2 Objectives of the Document

3 DevKit board overview

3.1 Board geometry

Brave NG_MEDIUM CLGA625 DevKit V2 is a 153 x 130 mm board



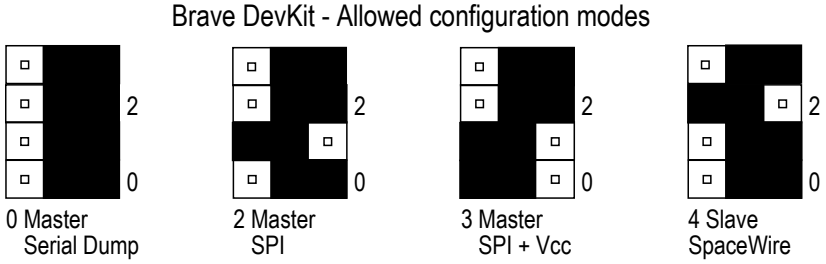
3.2 Board hardware overview

3.2.1 Configuration interfaces

The DevKit is an evaluation board to be used either interactively through JTAG, or standalone from an EEPROM board. The board configuration mode is thus selected by 4 on-board jumpers.

The JTAG connector receives a 26-pin ribbon cable from NanoXplore Angie USB-JTAG interface, providing:

- The 5 JTAG signals TRST-, TMS, TCK, TDI, TDO
- An I²C interface
- A target RST_N signal
- A connection to the mode bits, for readback and optionnal override



JTAG slave configuration is available in any other mode.

A 10-pin HE10 connector is provided to receive an EEPROM memory board (Atmel Dump Mode EEPROM or standard SPI EEPROM).

An optional SpaceWire connector allows SpaceWire configuration

3.2.2 Clocking options

Brave DevKit provides the following clocking options:

- Osc0 – U3 25MHz clock oscillator
- Osc1 – U4 Clam-shell socket for a user-supplied 2.5V 7x5mm clock oscillator
- Clk0 – J8 external SMA clock input
- Clk1 – J9 external SMA clock input

3.2.3 Supervision functions

The I²C interface is used for misc control and supervision functions.

- board identification: 24LC128 I²C serial identification EEPROM
- power supply voltages and current monitoring:
  two ADG728 I²C analog muxes
  one ADS1115 4-channel I²C ΔΣ A/D converter
- temperature measurement: LM73 I²C temp sensor

3.2.4 On-board devices

The board provides:

- a 128Mx16 DDR2 memory chip (Micron MT47H128M16RT)
- 6 switches
- 5 pushbuttons
- 19 LEDS
- a 2.5V, 7x5mm, 25 MHz clock oscillator
- a socket for a user-selected 2.5V, 7x5mm clock oscillator

3.2.5 Expansion connectors

The board provides:

- two optional user SpaceWire connectors
- one Altera HSMC mezzanine connector
- one VITA-57 FMC connector

3.3 Brave chip implementation

3.3.1 Socket capability

Brave DK625 DevKit board may be delivered with either a soldered chip or an Ironwood spring-pin clam-shell CLGA625 socket.

3.3.2 Banks repartition

All Brave I/Os are connected on the board.

Simple Banks 0 and 1 are 3.3V powered

Complex Banks 2, 3, 4 and 5 (J6 HSMC connector) are powered with HSMC supply, factory-set to 2.5V with VDD/2 termination voltage

Simple Banks 6, 7, 8 and Complex Bank 9 (J7 FMC connector) are powered with FMC supply, factory-set to 2.5V with VDD/2 termination voltage

Complex Banks 10 and 11 are 1.8V powered with VDD/2 termination voltage, and dedicated to the DDR2 memory chip and input switches

Complex Bank 12 is 2.5V powered with VDD/2 termination voltage, and handles both user SpaceWire connectors and the clock oscillators.

3.4 Detailed board features

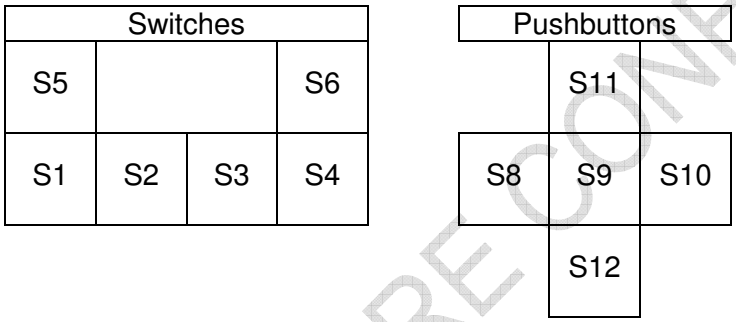
The user can find all the pads definition for NX1H35 development kit board DK625V2 in the provided NX1H35_EK_V2.py file.

3.4.1 User clocks

DK625 board clock sources				
Source	Voltage	Frequency	Signal	FPGA I/O
U3 oscillator	2.5V	25 MHz	OSC0	IO_B12D09P
U4 oscillator socket	2.5V	User def.	OSC1	IO_B12D08P
J8 ext SMA input	3.3V	User def.	CLK0	IO_B0D10P
J9 ext SMA input	3.3V	User def.	CLK1	IO_B0D11P

3.4.2 User input devices

Switches and pushbuttons use Bank10 I/Os (1.8V powered)



Switches				Pushbuttons		
Sw	Signal	FPGA I/O		Sw	Signal	FPGA I/O
S1	PA09	IO_B10D09P		S8	PA07	IO_B10D07P
S2	PA03	IO_B10D03P		S9	PA12	IO_B10D12P
S3	NA03	IO_B10D03N		S10	NA07	IO_B10D07N
S4	PA04	IO_B10D04P		S11	NA12	IO_B10D12N
S5	NA09	IO_B10D09N		S12	PA14	IO_B10D14P
S6	NA04	IO_B10D04N				

3.4.3 User LEDs

User LEDs – Banks 0 and 1						
LED	Signal	FPGA I/O		LED	Signal	FPGA I/O
1	LD1_N	IO_B0D01P		5	LD5_N	IO_B1D05P
2	LD2_N	IO_B0D03N		6	LD6_N	IO_B1D06N
3	LD3_N	IO_B0D03P		7	LD7_N	IO_B1D06P
4	LD4_N	IO_B1D05N		8	LD8_N	IO_B1D02N

User LEDs – Prog Bank (added on DK625V1 board)			
LED	Signal	FPGA I/O	Interface
9	LD9_N	D0	USER_D0
10	LD10_N	D1	USER_D1
11	LD11_N	D2	USER_D2
12	LD12_N	D3	USER_D3
13	LD13_N	D4	USER_D4
14	LD14_N	D5	USER_D5
15	LD15_N	D6	USER_D6
16	LD16_N	D7	USER_D7
17	LD17_N	CS_N	USER_CS_N
18	LD18_N	WE_N	USER_WE_N
19	LD19_N	DATA_OE	USER_DATA_OE

Note: Unlike standard FPGA I/Os, declared in pads dictionary, these LEDs are accessed through direct connections to the fabric, declared in interfaces dictionary.

3.5 Connectors pinouts

3.5.1 Flash expansion connector

J2 Serial PROM expansion connector				
Pin	Pad	Dump Mode	SPI Mode	SPI VCC Mode
1	D9	CLOCK	CLOCK	CLOCK
2	D12	RDY	Prog LED	Prog LED
3	GND	GND	GND	GND
4	D11	RST/OE	MOSI	MOSI
5	D13	SER_EN	-	Vcc0
6	VCC	VCC	VCC	Unused
7	D15	-	-	Vcc2
8	D14	Prog LED	-	Vcc1
9	D10	MISO	MISO	MISO
10	D8	CS_N	CS_N	CS_N

3.5.2 SpaceWire interfaces

J3 – Configuration SpaceWire connector – Prog Bank (2.5V)						
Pin	Signal	FPGA I/O		Pin	Signal	FPGA I/O
1	DINP	DIN_P		6	DINN	DIN_N
2	SINP	SIN_P		7	SINN	SIN_N
3	Shield					
4	SOUN	SOUT_N		8	SOUP	SOUT_P
5	DOUN	DOUT_N		9	DOUP	DOUT_P

J4 – User1 SpaceWire connector – Bank 12 (2.5V)						
Pin	Signal	FPGA I/O		Pin	Signal	FPGA I/O
1	U1DIP	IO_B12D03P		6	U1DIN	IO_B12D03N
2	U1SIP	IO_B12D04P		7	U1SIN	IO_B12D04N
3	Shield					
4	U1SON	IO_B12D02N		8	U1SOP	IO_B12D02P
5	U1DON	IO_B12D01N		9	U1DOP	IO_B12D01P

J5 – User2 SpaceWire connector – Bank 12 (2.5V)						
Pin	Signal	FPGA I/O		Pin	Signal	FPGA I/O
1	U2DIP	IO_B12D14P		6	U2DIN	IO_B12D14N
2	U2SIP	IO_B12D15P		7	U2SIN	IO_B12D15N
3	Shield					
4	U2SON	IO_B12D13N		8	U2SOP	IO_B12D13P
5	U2DON	IO_B12D12N		9	U2DOP	IO_B12D12P

On DevKit V2, User1 and User2 SpaceWire interfaces on J4 and J5 connectors have access to NanoXplore-specific enhanced functions (clock recovery xor and high speed shift registers), expecting the targeted 400Mbit/

3.5.3 HSMC interface

J6 - HSMC connector – Bank 1						
Pin	Signal	FPGA I/O		Pin	Signal	FPGA I/O
1	HTX7P	IO_B5D06P		2	HRX7P	IO_B5D02P
3	HTX7N	IO_B5D06N		4	HRX7N	IO_B5D02N
5	HTX6P	IO_B5D09P		6	HRX6P	IO_B5D04P
7	HTX6N	IO_B5D09N		8	HRX6N	IO_B5D04N
9	HTX5P	IO_B5D15P		10	HRX5P	IO_B5D10P
11	HTX5N	IO_B5D15N		12	HRX5N	IO_B5D10N
13	HTX4P	IO_B4D03P		14	HRX4P	IO_B5D13P
15	HTX4N	IO_B4D03N		16	HRX4N	IO_B5D13N
17	HTX3P	IO_B4D01P		18	HRX3P	IO_B4D04P
19	HTX3N	IO_B4D01N		20	HRX3N	IO_B4D04N
21	HTX2P	IO_B4D12P		22	HRX2P	IO_B4D05P
23	HTX2N	IO_B4D12N		24	HRX2N	IO_B4D05N
25	HTX1P	IO_B4D11P		26	HRX1P	IO_B4D06P
27	HTX1N	IO_B4D11N		28	HRX1N	IO_B4D06N
29	HTX0P	IO_B3D06P		30	HRX0P	IO_B3D10P
31	HTX0N	IO_B3D06N		32	HRX0N	IO_B3D10N
33	HSDA	IO_B1D02P		34	HSCL	IO_B1D08N
35	HTCK	IO_B1D03P		36	HTMS	IO_B1D07N
37	HTDO	IO_B1D03N		38	HTDI	IO_B1D07P
39	HCKO0	IO_B5D08N		40	HCKI0	IO_B5D08P

J6 - HSMC connector – Bank 2						
Pin	Signal	FPGA I/O		Pin	Signal	FPGA I/O
41	HD0P	IO_B3D05P		42	HD1P	IO_B3D03P
43	HD0N	IO_B3D05N		44	HD1N	IO_B3D03N
45	+3.3V	-		46	+12V	-
47	HD2P	IO_B3D04P		48	HD3P	IO_B3D13P
49	HD2N	IO_B3D04N		50	HD3N	IO_B3D13N
51	+3.3V	-		52	+12V	-
53	HD4P	IO_B3D09P		54	HD5P	IO_B3D15N
55	HD4N	IO_B3D09N		56	HD5N	IO_B3D15P
57	+3.3V	-		58	+12V	-
59	HD6P	IO_B2D01P		60	HD7P	IO_B2D07P
61	HD6N	IO_B2D01N		62	HD7N	IO_B2D07N
63	+3.3V	-		64	+12V	-
65	HD8P	IO_B2D03P		66	HD9P	IO_B2D04P
67	HD8N	IO_B2D03N		68	HD9N	IO_B2D04N
69	+3.3V	-		70	+12V	-
71	HD10P	IO_B2D09P		72	HD11P	IO_B2D10P
73	HD10N	IO_B2D09N		74	HD11N	IO_B2D10N
75	+3.3V	-		76	+12V	-
77	HD12P	IO_B2D08P		78	HD13P	IO_B2D15P
79	HD12N	IO_B2D08N		80	HD13N	IO_B2D15N
81	+3.3V	-		82	+12V	-
83	HD14P	IO_B5D07P		84	HD15P	IO_B5D11P
85	HD14N	IO_B5D07N		86	HD15N	IO_B5D11N
87	+3.3V	-		88	+12V	-
89	HD16P	IO_B5D12P		90	HD17P	IO_B5D14P
91	HD16N	IO_B5D12N		92	HD17N	IO_B5D14N
93	+3.3V	-		94	+12V	-
95	HD18P	IO_B4D08P		96	HD19P	IO_B4D02P
97	HD18N	IO_B4D08N		98	HD19N	IO_B4D02N
99	+3.3V	-		100	+12V	-

J6 - HSMC connector – Bank 3						
Pin	Signal	FPGA I/O		Pin	Signal	FPGA I/O
101	HD20P	IO_B4D10P		102	HD21P	IO_B4D07P
103	HD20N	IO_B4D10N		104	HD21N	IO_B4D07N
105	+3.3V	-		106	+12V	-
107	HD22P	IO_B4D09P		108	HD23P	IO_B4D13P
109	HD22N	IO_B4D09N		110	HD23N	IO_B4D13N
111	+3.3V	-		112	+12V	-
113	HD24P	IO_B3D01N		114	HD25P	IO_B4D15P
115	HD24N	IO_B3D01P		116	HD25N	IO_B4D15N
117	+3.3V	-		118	+12V	-
119	HD26P	IO_B3D02N		120	HD27P	IO_B4D14P
121	HD26N	IO_B3D02P		122	HD27N	IO_B4D14N
123	+3.3V	-		124	+12V	-
125	HD28P	IO_B3D08P		126	HD29P	IO_B3D07P
127	HD28N	IO_B3D08N		128	HD29N	IO_B3D07N
129	+3.3V	-		130	+12V	-
131	HD30P	IO_B3D11P		132	HD31P	IO_B3D12P
133	HD30N	IO_B3D11N		134	HD31N	IO_B3D12N
135	+3.3V	-		136	+12V	-
137	HD32P	IO_B2D02P		138	HD33P	IO_B3D14P
139	HD32N	IO_B2D02N		140	HD33N	IO_B3D14N
141	+3.3V	-		142	+12V	-
143	HD34P	IO_B2D06P		144	HD35P	IO_B2D11P
145	HD34N	IO_B2D06N		146	HD35N	IO_B2D11N
147	+3.3V	-		148	+12V	-
149	HD36P	IO_B2D05P		150	HD37P	IO_B2D12P
151	HD36N	IO_B2D05N		152	HD37N	IO_B2D12N
153	+3.3V	-		154	+12V	-
155	HD38P	IO_B2D14P		156	HD39P	IO_B2D13P
157	HD38N	IO_B2D14N		158	HD39N	IO_B2D13N
159	+3.3V	-		160	+12V	-

3.5.4 FMC interface

On the FMC interface connector,

- All SERDES I/O signals are unconnected
- All HBnn signals are unconnected
- Only LAnn and HAnn signals are available

J7 - FMC connector – A & B Columns						
Pin	Signal	FPGA I/O		Pin	Signal	FPGA I/O
A1	GND			B1		
A2				B2	GND	
A3				B3	GND	
A4	GND			B4		
A5	GND			B5		
A6				B6	GND	
A7				B7	GND	
A8	GND			B8		
A9	GND			B9		
A10				B10	GND	
A11				B11	GND	
A12	GND			B12		
A13	GND			B13		
A14				B14	GND	
A15				B15	GND	
A16	GND			B16		
A17	GND			B17		
A18				B18	GND	
A19				B19	GND	
A20	GND			B20		
A21	GND			B21		
A22				B22	GND	
A23				B23	GND	
A24	GND			B24		
A25	GND			B25		
A26				B26	GND	
A27				B27	GND	
A28	GND			B28		
A29	GND			B29		
A30				B30	GND	
A31				B31	GND	
A32	GND			B32		
A33	GND			B33		
A34				B34	GND	
A35				B35	GND	
A36	GND			B36		
A37	GND			B37		
A38				B38	GND	
A39				B39	GND	
A40	GND			B40		

J7 - FMC connector – C & D Columns						
Pin	Signal	FPGA I/O		Pin	Signal	FPGA I/O
C1	GND			D1	FPGC2M	IO_B1D04P
C2				D2	GND	
C3				D3	GND	
C4	GND			D4		
C5	GND			D5		
C6				D6	GND	
C7				D7	GND	
C8	GND			D8	FLA01P	IO_B6D08P
C9	GND			D9	FLA01N	IO_B6D08N
C10	FLA06P	IO_B6D10P		D10	GND	
C11	FLA06N	IO_B6D10N		D11	FLA05P	IO_B6D15P
C12	GND			D12	FLA05N	IO_B6D15N
C13	GND			D13	GND	
C14	FLA10P	IO_B6D09P		D14	FLA09P	IO_B6D04P
C15	FLA10N	IO_B6D09N		D15	FLA09N	IO_B6D04N
C16	GND			D16	GND	
C17	GND			D17	FLA13P	IO_B6D07P
C18	FLA14P	IO_B6D05P		D18	FLA13N	IO_B6D07N
C19	FLA14N	IO_B6D05N		D19	GND	
C20	GND			D20	FLA17P	IO_B7D15P
C21	GND			D21	FLA17N	IO_B7D15N
C22	FLA18P	IO_B7D10P		D22	GND	
C23	FLA18N	IO_B7D10N		D23	FLA23P	IO_B8D14P
C24	GND			D24	FLA23N	IO_B8D14N
C25	GND			D25	GND	
C26	FLA27P	IO_B8D05P		D26	FLA26P	IO_B8D03P
C27	FLA27N	IO_B8D05N		D27	FLA26N	IO_B8D03N
C28	GND			D28	GND	
C29	GND			D29	FTCK	IO_B1D01N
C30	FSCL	IO_B1D09P		D30	FTDI	IO_B1D01P
C31	FSDA	IO_B1D09N		D31	FTDO	IO_B1D11N
C32	GND			D32	+3.3V	
C33	GND			D33	FTMS	IO_B1D11P
C34	GA0 = GND			D34	FTRN	IO_B1D10P
C35	+12V			D35	GA1 = GND	
C36	GND			D36	+3.3V	
C37	+12V			D37	GND	
C38	GND			D38	+3.3V	
C39	+3.3V			D39	GND	
C40	GND			D40	+3.3V	

J7 - FMC connector – E & F Columns						
Pin	Signal	FPGA I/O		Pin	Signal	FPGA I/O
E1	GND			F1	FPGM2C	IO_B1D04N
E2	FHA01P	IO_B6D14P		F2	GND	
E3	FHA01N	IO_B6D14N		F3	GND	
E4	GND			F4	FHA00P	IO_B6D03P
E5	GND			F5	FHA00N	IO_B6D03N
E6	FHA05P	IO_B6D13P		F6	GND	
E7	FHA05N	IO_B6D13N		F7	FHA04P	IO_B7D11P
E8	GND			F8	FHA04N	IO_B7D11N
E9	FHA09P	IO_B6D02P		F9	GND	
E10	FHA09N	IO_B6D02N		F10	FHA08P	IO_B7D06P
E11	GND			F11	FHA08N	IO_B7D06N
E12	FHA13P	IO_B6D06P		F12	GND	
E13	FHA13N	IO_B6D06N		F13	FHA12P	IO_B7D04P
E14	GND			F14	FHA12N	IO_B7D04N
E15	FHA16P	IO_B7D14P		F15	GND	
E16	FHA16N	IO_B7D14N		F16	FHA15P	IO_B8D09P
E17	GND			F17	FHA15N	IO_B8D09N
E18	FHA20P	IO_B7D13P		F18	GND	
E19	FHA20N	IO_B7D13N		F19	FHA19P	IO_B7D05P
E20	GND			F20	FHA19N	IO_B7D05N
E21				F21	GND	
E22				F22		
E23	GND			F23		
E24				F24	GND	
E25				F25		
E26	GND			F26		
E27				F27	GND	
E28				F28		
E29	GND			F29		
E30				F30	GND	
E31				F31		
E32	GND			F32		
E33				F33	GND	
E34				F34		
E35	GND			F35		
E36				F36	GND	
E37				F37		
E38	GND			F38		
E39	VDDFMC			F39	GND	
E40	GND			F40	VDDFMC	

J7 - FMC connector – G & H Columns						
Pin	Signal	FPGA I/O		Pin	Signal	FPGA I/O
G1	GND			H1		
G2	FCLK1P	IO_B9D08P		H2	FPS_N	IO_B1D10N
G3	FCLK1N	IO_B9D08N		H3	GND	
G4	GND			H4	FCLK0P	IO_B9D09P
G5	GND			H5	FCLK0N	IO_B9D09N
G6	FLA00P	IO_B6D11P		H6	GND	
G7	FLA00N	IO_B6D11N		H7	FLA02P	IO_B6D12P
G8	GND			H8	FLA02N	IO_B6D12N
G9	FLA03P	IO_B7D03P		H9	GND	
G10	FLA03N	IO_B7D03N		H10	FLA04P	IO_B7D09P
G11	GND			H11	FLA04N	IO_B7D09N
G12	FLA08P	IO_B7D02P		H12	GND	
G13	FLA08N	IO_B7D02N		H13	FLA07P	IO_B8D08P
G14	GND			H14	FLA07N	IO_B8D08N
G15	FLA12P	IO_B8D10P		H15	GND	
G16	FLA12N	IO_B8D10N		H16	FLA11P	IO_B8D06P
G17	GND			H17	FLA11N	IO_B8D06N
G18	FLA16P	IO_B8D13P		H18	GND	
G19	FLA16N	IO_B8D13N		H19	FLA15P	IO_B8D07P
G20	GND			H20	FLA15N	IO_B8D07N
G21	FLA20P	IO_B8D04P		H21	GND	
G22	FLA20N	IO_B8D04N		H22	FLA19P	IO_B9D04P
G23	GND			H23	FLA19N	IO_B9D04N
G24	FLA22P	IO_B9D02P		H24	GND	
G25	FLA22N	IO_B9D02N		H25	FLA21P	IO_B9D15P
G26	GND			H26	FLA21N	IO_B9D15N
G27	FLA25P	IO_B9D12P		H27	GND	
G28	FLA25N	IO_B9D12N		H28	FLA24P	IO_B9D01P
G29	GND			H29	FLA24N	IO_B9D01N
G30	FLA29P	IO_B8D01P		H30	GND	
G31	FLA29N	IO_B8D01N		H31	FLA28P	IO_B9D05P
G32	GND			H32	FLA28N	IO_B9D05N
G33	FLA31P	IO_B8D02P		H33	GND	
G34	FLA31N	IO_B8D02N		H34	FLA30P	IO_B9D11P
G35	GND			H35	FLA30N	IO_B9D11N
G36	FLA33P	IO_B9D13P		H36	GND	
G37	FLA33N	IO_B9D13N		H37	FLA32P	IO_B9D14P
G38	GND			H38	FLA32N	IO_B9D14N
G39	VDDFMC			H39	GND	
G40	GND			H40	VDDFMC	

J7 - FMC connector – J & K Columns						
Pin	Signal	FPGA I/O		Pin	Signal	FPGA I/O
J1	GND			K1		
J2				K2	GND	
J3				K3	GND	
J4	GND			K4		
J5	GND			K5		
J6	FHA03P	IO_B7D12P		K6	GND	
J7	FHA03N	IO_B7D12N		K7	FHA02P	IO_B7D07P
J8	GND			K8	FHA02N	IO_B7D07N
J9	FHA07P	IO_B6D01P		K9	GND	
J10	FHA07N	IO_B6D01N		K10	FHA06P	IO_B7D08P
J11	GND			K11	FHA06N	IO_B7D08N
J12	FHA11P	IO_B8D12P		K12	GND	
J13	FHA11N	IO_B8D12N		K13	FHA10P	IO_B8D11P
J14	GND			K14	FHA10N	IO_B8D11N
J15	FHA14P	IO_B7D01P		K15	GND	
J16	FHA14N	IO_B7D01N		K16	FHA17P	IO_B8D15P
J17	GND			K17	FHA17N	IO_B8D15N
J18	FHA18P	IO_B9D10P		K18	GND	
J19	FHA18N	IO_B9D10N		K19	FHA21P	IO_B9D03P
J20	GND			K20	FHA21N	IO_B9D03N
J21	FHA22P	IO_B9D07P		K21	GND	
J22	FHA22N	IO_B9D07N		K22	FHA23P	IO_B9D06P
J23	GND			K23	FHA23N	IO_B9D06N
J24				K24	GND	
J25				K25		
J26	GND			K26		
J27				K27	GND	
J28				K28		
J29	GND			K29		
J30				K30	GND	
J31				K31		
J32	GND			K32		
J33				K33	GND	
J34				K34		
J35	GND			K35		
J36				K36	GND	
J37				K37		
J38	GND			K38		
J39				K39	GND	
J40	GND			K40		

3.5.5 Bank0 spare I/Os (3.3V supplied bank)

TP1 test point				TP2 test point		
Pin	Signal	FPGA I/O		Pin	Signal	FPGA I/O
1	GND			1	GND	
2	P006	IO_B0D06P		2	N006	IO_B0D06N
3	P007	IO_B0D07P		3	N007	IO_B0D07N
4	P005	IO_B0D05P		4	N005	IO_B0D05N
5	P009	IO_B0D09P		5	N009	IO_B0D09N
6	N001	IO_B0D01N		6	N011	IO_B0D11N
7	P008	IO_B0D08P		7	N008	IO_B0D08N
8	N010	IO_B0D10N		8	P002	IO_B0D02P
9	N002	IO_B0D02N		9	P004	IO_B0D04P
10	N004	IO_B0D04N		10		

3.5.6 Bank12 spare I/Os (2.5V supplied bank)

TP3 test point				TP4 test point		
Pin	Signal	FPGA I/O		Pin	Signal	FPGA I/O
1	GND			1	GND	
2	PC10	IO_B12D10P		2	NC10	IO_B12D10N
3	PC05	IO_B12D05P		3	NC05	IO_B12D05N
4	NC07	IO_B12D07N		4	PC07	IO_B12D07P
5	NC08	IO_B12D08N		5	NC09	IO_B12D09N
6	PC11	IO_B12D11P		6	NC11	IO_B12D11N
7	PC06	IO_B12D06P		7	NC06	IO_B12D06N
8	CAL0	Cal network 0		8	CAL1	Cal network 1
9	SVDD	Opt. 2.5V sup.		9	SVDD	Opt. 2.5V sup.
10	SVTT	Opt. Vterm		10	SVTT	Opt. Vterm

Note: IO_B12D06N is Calibration pin for complex bank 12.

3.5.7 Bank5 spare I/Os (HSMC supplied bank)

TP5 test point		
Pin	Signal	FPGA I/O
1	GND	
2	N503	IO_B5D03N
3	P503	IO_B5D03P
4	N501	IO_B5D01N
5	P501	IO_B5D01P
6	N505	IO_B5D05N
7	P505	IO_B5D05P
8	HVDD	Opt. HMC sup.