Introduction to Processors

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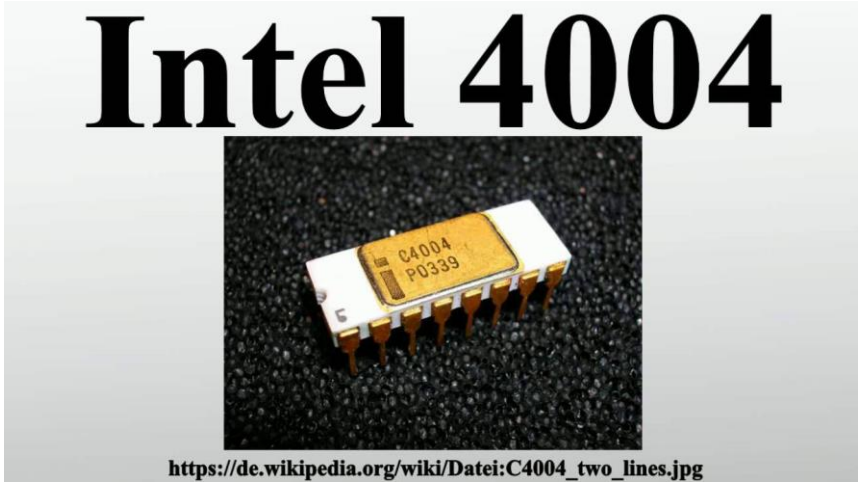
Outline for Lecture 1

- History in short
- Evolution of processors
- Technology Developments
- Performance parameters
- System on Chip

Primitive Microprocessor

- First integrated circuit in 1959, Fairchild Semiconductors
- Intel4004 first microprocessor (µP) invented 1971

Gordan Moore, Robert Noyce and Andrew Grove resigned from the Fair child semiconductors and started their own company: Integrated Electronics (Intel).



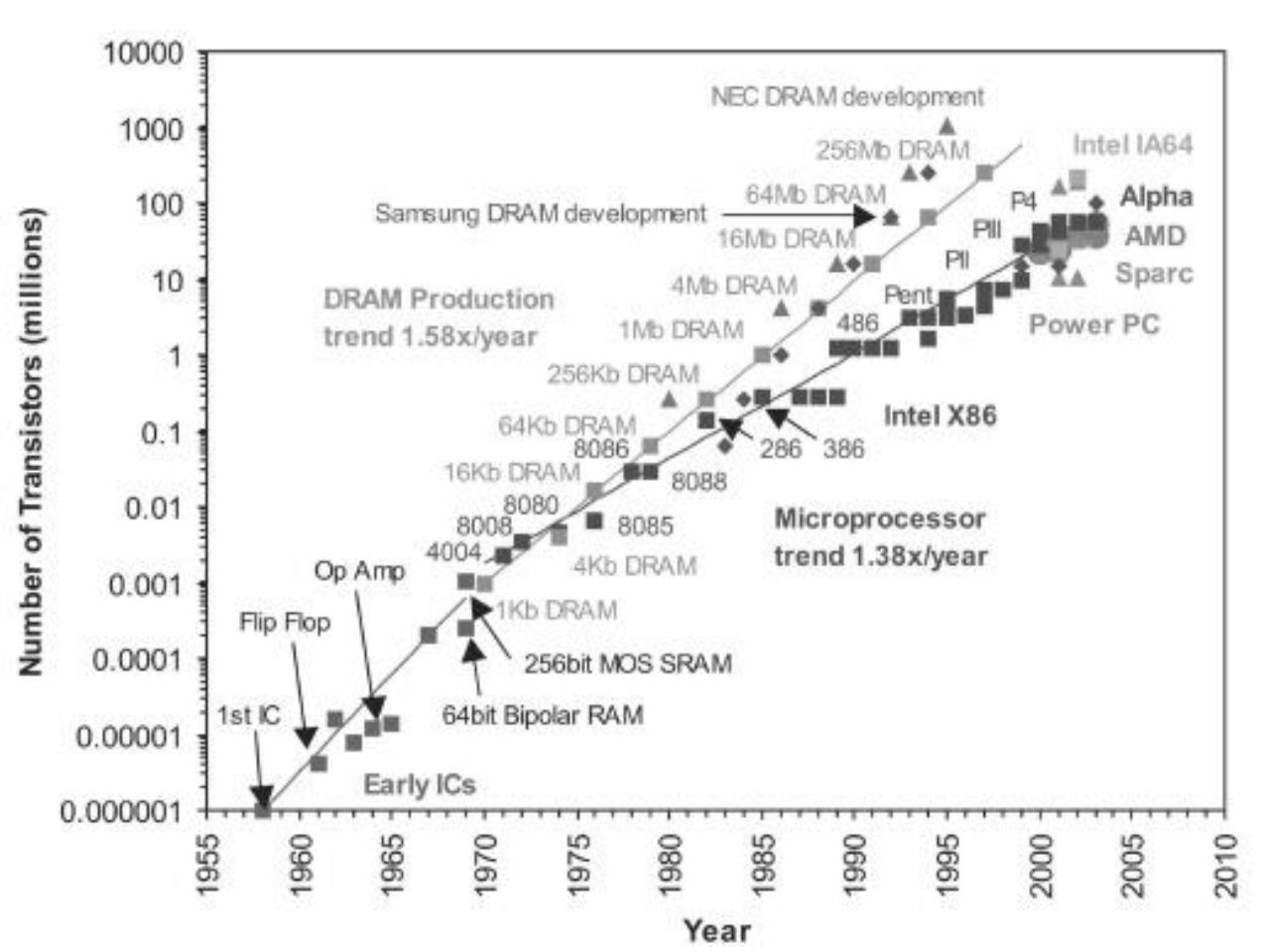
https://en.wikipedia.org/wiki/Intel_4004

Min. feature size	10 µm
Instruction set	4-bit BCD-oriented
Transistors	2300[1]
Data width	4
Address width	12 (multiplexed)
Successor	Intel 4040
Application	Busicom calculator, arithmetic manipulation
Package(s)	•16-pin DIP

Evolution

- Second generation μP: Intel 8008 was announced in 1974
- 8 bit -Intel 8080 and Motorola 6800 followed.
- Intel 8031 and Intel 8051 in 1980s
- Electrically erasable and programable (Flash) memories 1990s. A lot of μC from Atmel and Microchip use flash memories.
- Competitors for manufacturing μC : AVR (Alf, Vegard and Risc) and PIC (Microchip Technologies), Texas Instruments.....

Developments



Advances in optical lithography allow high resolutions during fabrication.

Moore's law I: the number of transistors on processor doubles approximately every 18 months. Component density was key target in 1960 and 1970.

Processor speed became important design Criterion in 1980.
Low Power consumption & low noise are the key design parameters now.

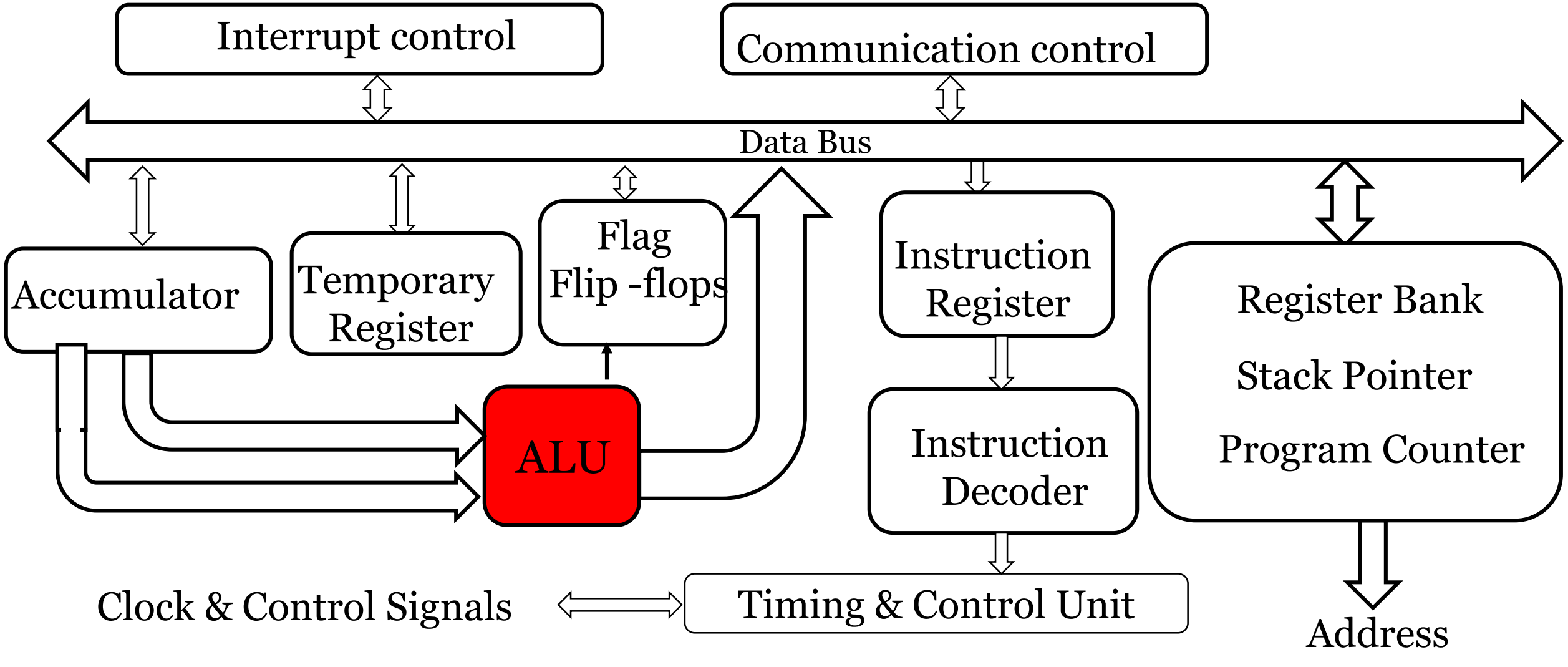
Mile Stojcev, Teufik Toki, Ivan Milentijevi " The limits of semiconductor technology and oncoming challenges in computer microarchitectures and architectures", *ELEC. ENERG*. vol.17, December2004,285-312.

Performance parameters

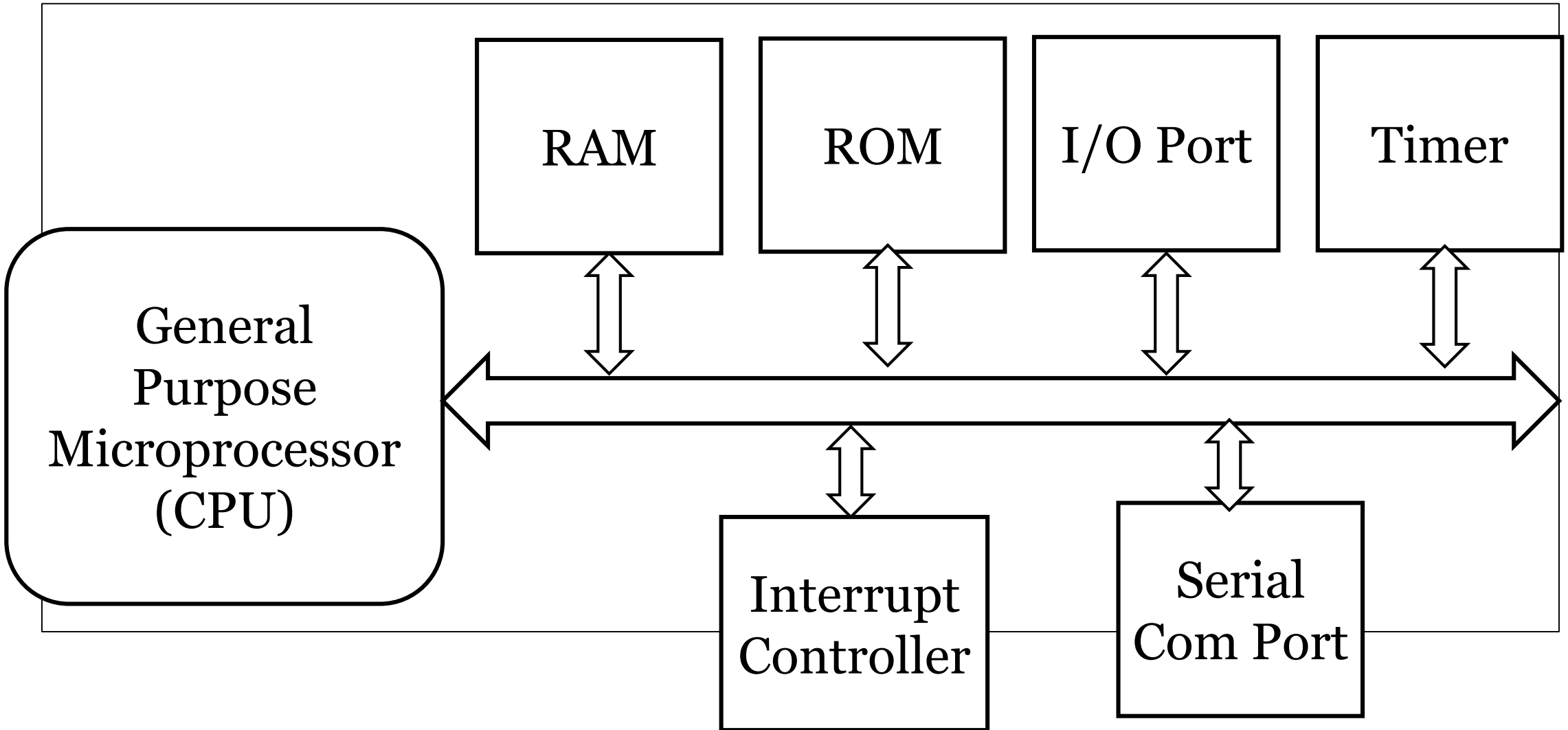
- Dhrystone MIPs(DMIPs)
- Processors are selected by assessing two parameters
  - Speed of processing
  - Width of data

Processor name	Speed of processing	Data bus width	Introduced on date	Minimum feature size
8086	5 to 10MHz	8 bits	June 1978	?
286	6 MHz	16 bits	Feb. 1982	?
Pentium II	233 MHz to 450 MHz	32 bits	May. 1997	?
Pentium III	450 MHz to 1.4 GHz	64 bits	Feb. 1999	?
Intel® Core i7	3.1 GHz	64 bits	Dec. 2009	?

Microprocessor (CPU)

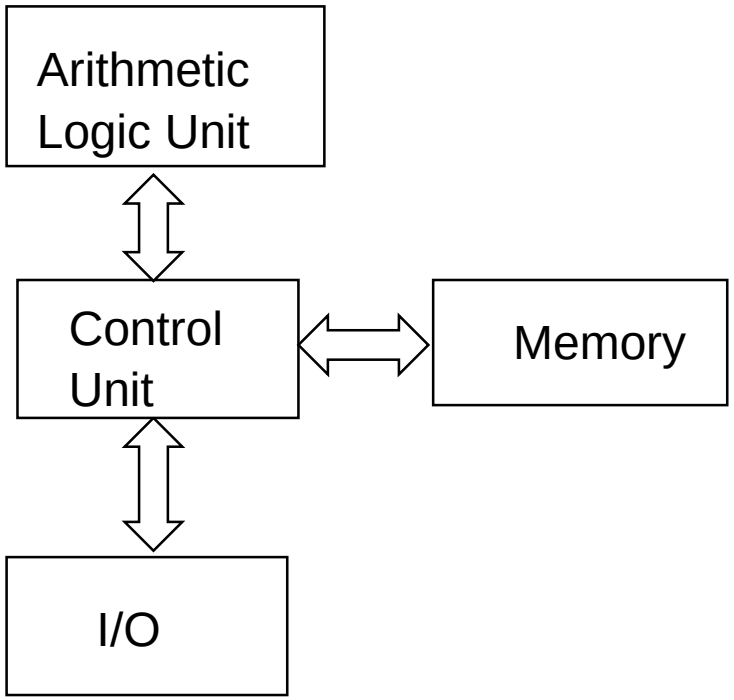


Evolution of Microcontrollers

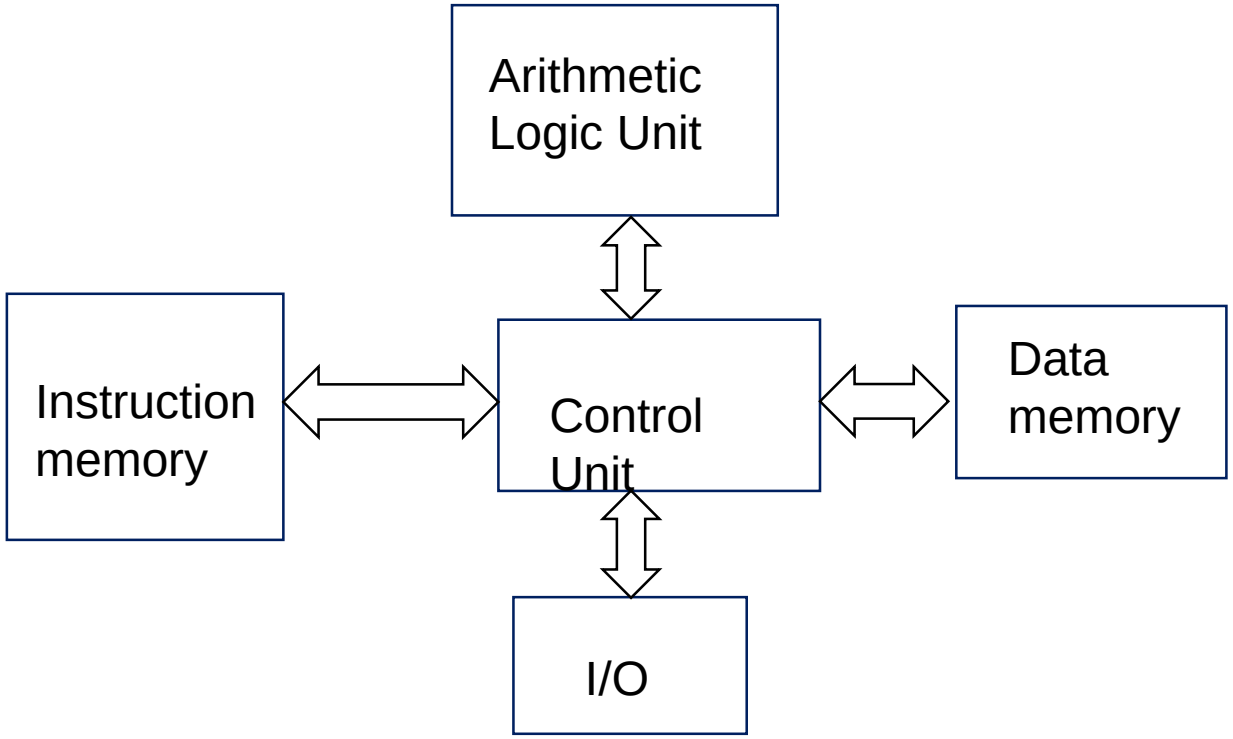


Hardware Architectures

Von Neumann or Princeton



Harvard Architecture



Instruction Set Architecture

- Reduced Instruction Set Computing (RISC)- less power consumption, less heat
- Load store Architecture (both operands & destinations must be on registers)
- Pipelining

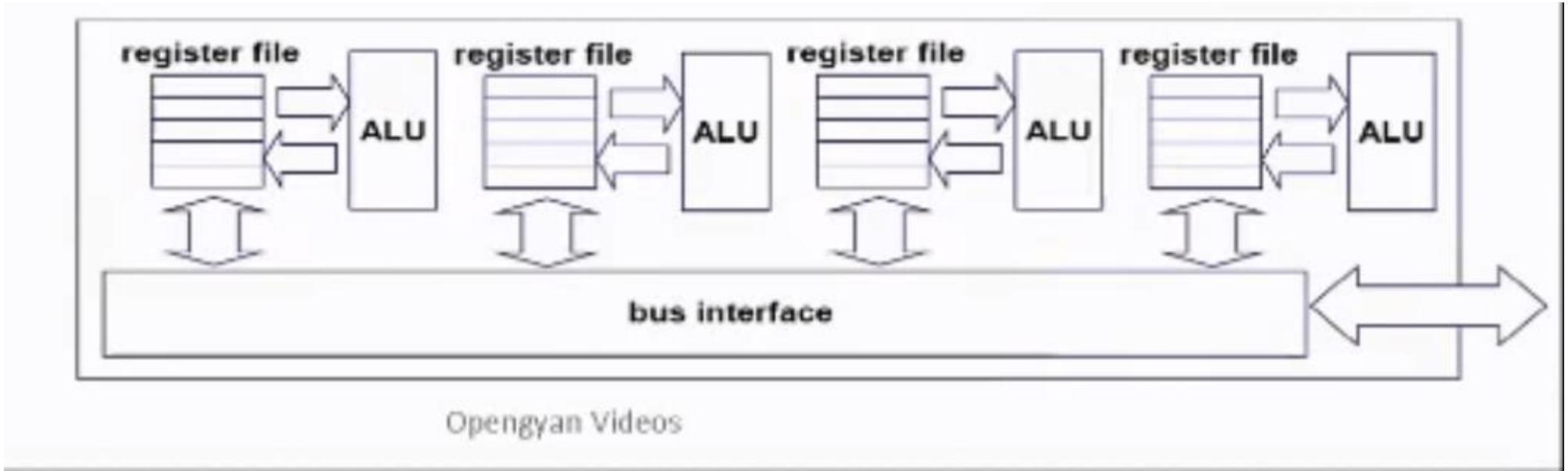
Clock cycle / Instr. No.	1	2	3	4	5	6	7
1	IF	ID	EX	MEM	WB		
2		IF	ID	EX	MEM	WB	
3			IF	ID	EX	MEM	WB
4				IF	ID	EX	MEM
5					IF	ID	EX

(IF = Instruction Fetch, ID = Instruction Decode, EX = Execute, MEM = Memory access, WB = Register write back).In the fourth clock cycle (the green column), the earliest instruction is in MEM stage, and the latest instruction has not yet entered the pipeline.

System on Chip SOC

- Raspberry pi 4 uses Broadcom BCM2711 SoC
- Arm A72 64 bit CPU running at 1.5 GHz , quad-core, 32 KB data + 48 KB instruction L1 cache per core, 1MB L2 cache.

What is advantage of multicore ? can run multiple instructions at the same time.



Multicore Processors

Advantages:

- Performance improvement

Disadvantages:

- Cost more than single core
- Does not have twice the efficiency, depends on program (single threaded may not need more parallelism).
- Faster battery drainage.
- Require better thermal management
- Multiple levels of cache required (at times upto L4)

Microarchitecture

Micro-architecture includes things like:

- Pipeline length and layout.
- Number and sizes of caches.
- Cycle counts for individual instructions.
- Which optional features are implemented.

Microarchitectures for Arm Cortex-A processors:

- Cortex-A8 is a single core, single-thread processor. **The entire processor is a PE.**
- Cortex-A53 is a multi-core processor, each core is a single thread. **Each core is PE.**
- Cortex-A65AE is a multi-core processor, each core has two threads. **Each thread is PE.**

Privileges

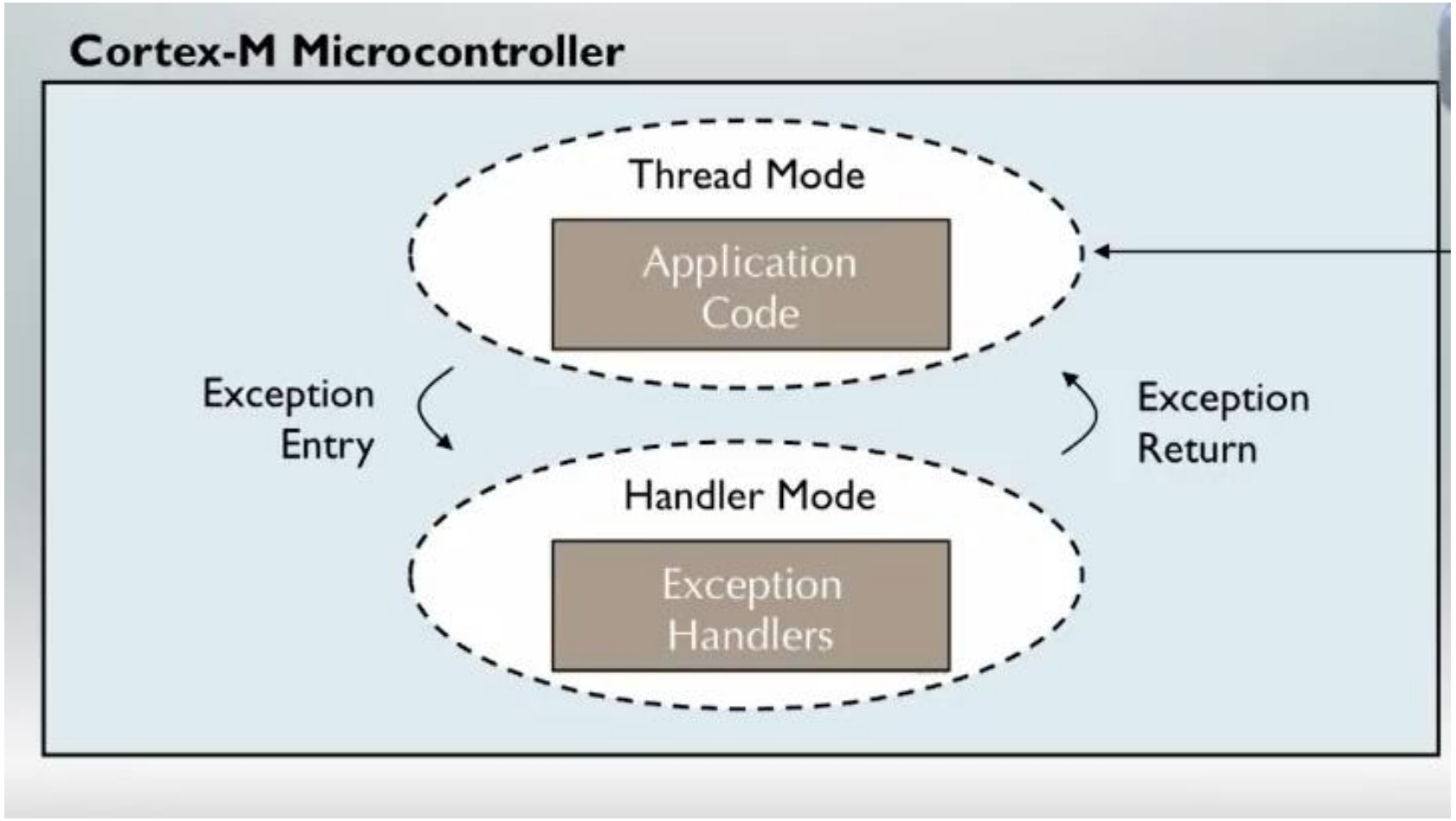
- Modern software expects to be split into different modules, each with a different level of access to system and processor resources.

  Types of Privileges:
  - Memory Privilege : MMU assigns privileges to r-w-x to software.
  - Processor resources: Higher Exception levels have the privilege to access registers that control lower levels

Exceptions

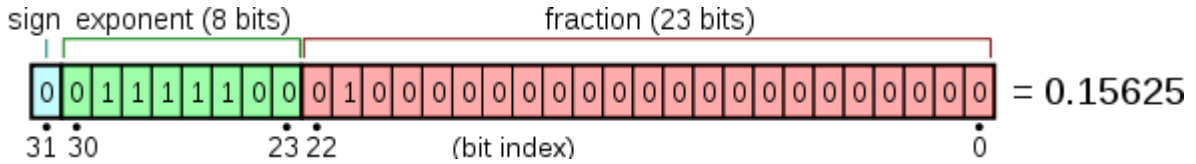
- Reset
- Undefined instruction
- Software Interrupt (SWI)
- Prefetch Abort
- Data Abort
- IRQ
- FIQ

Program Structure



Assignment

- Read IEEE 754 standard for representing floating point numbers.
- Convert binary numbers to decimal



- What is Dhrystone per second?
- Revise Digital Number Systems