CSE 460

VLSI LAB

ASSIGNMENT 05

Submitted by

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# Lab Assignment 05

Problem statement

Draw the circuit using the appropriate tool as taught in the lab and rectify all design errors (if any), submit the full screen screenshots of the design file and the simulation file **with proper discussion.**
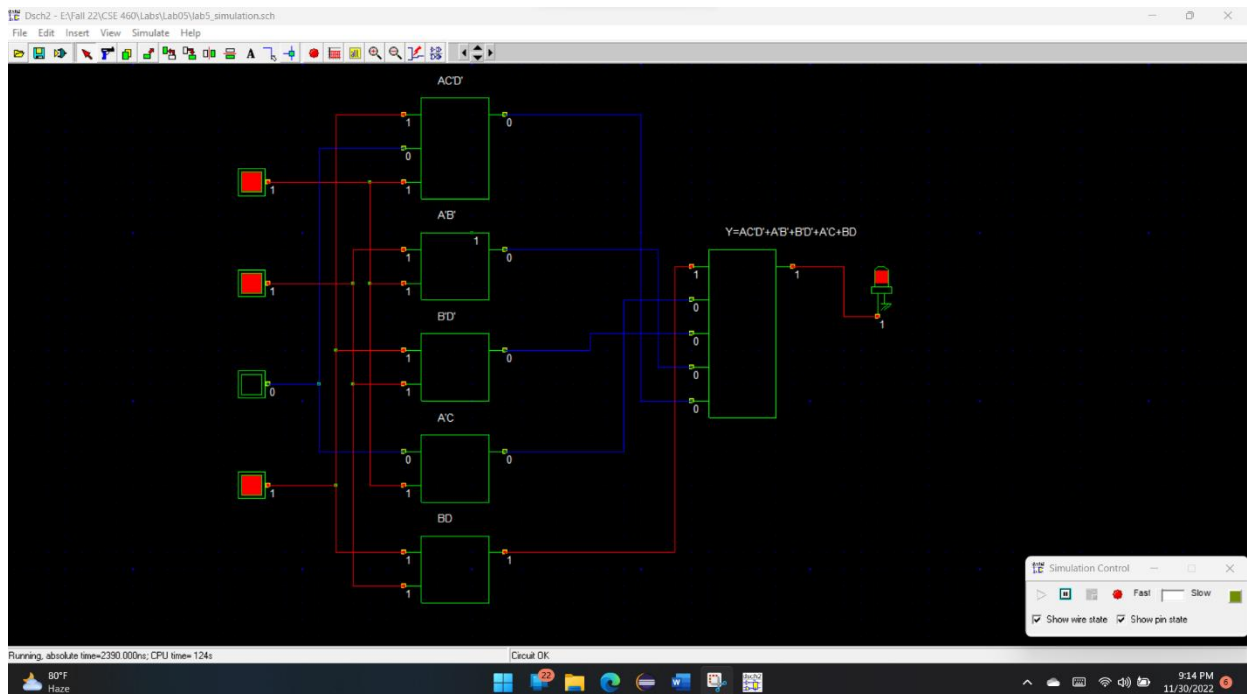
Problem:
Derive the Boolean logic expression from the following K-Map and implement the logic function using CMOS technology. You may use blocks/sub-circuits made using CMOS technology but cannot use readily available logic gates.

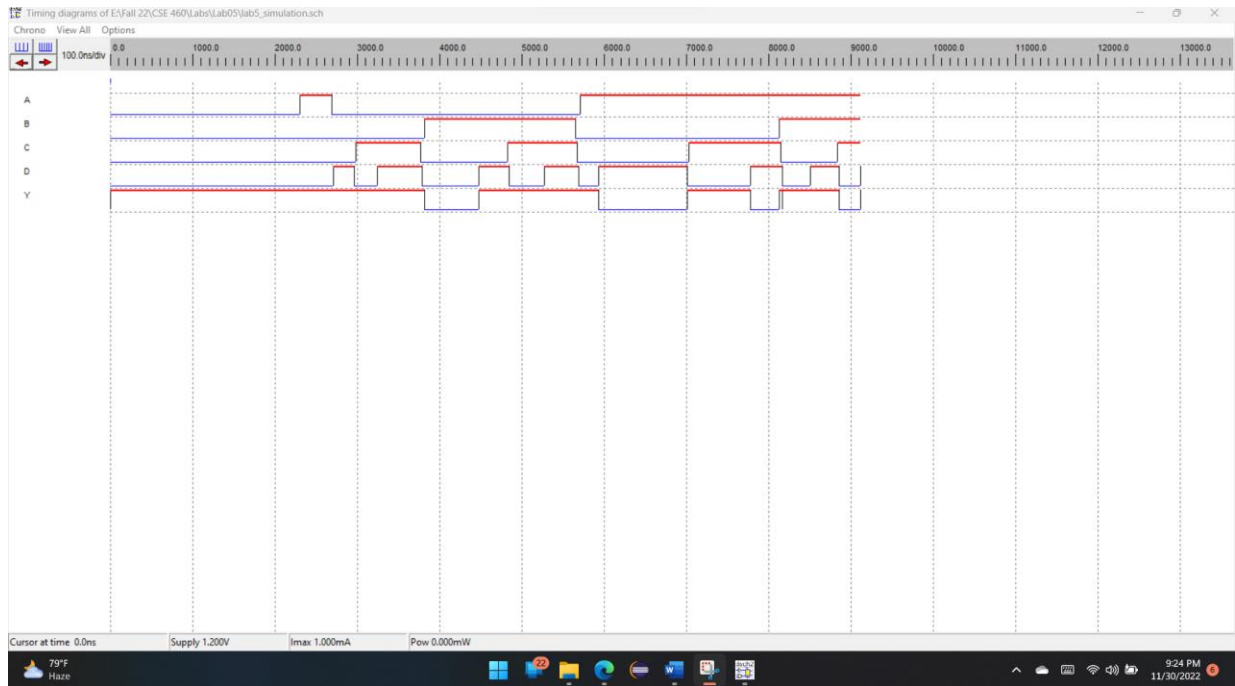| CD \ AB	00	01	11	10
00	1	0	1	1
01	1	d	d	0
11	d	d	1	0
10	1	1	0	1

Diagram
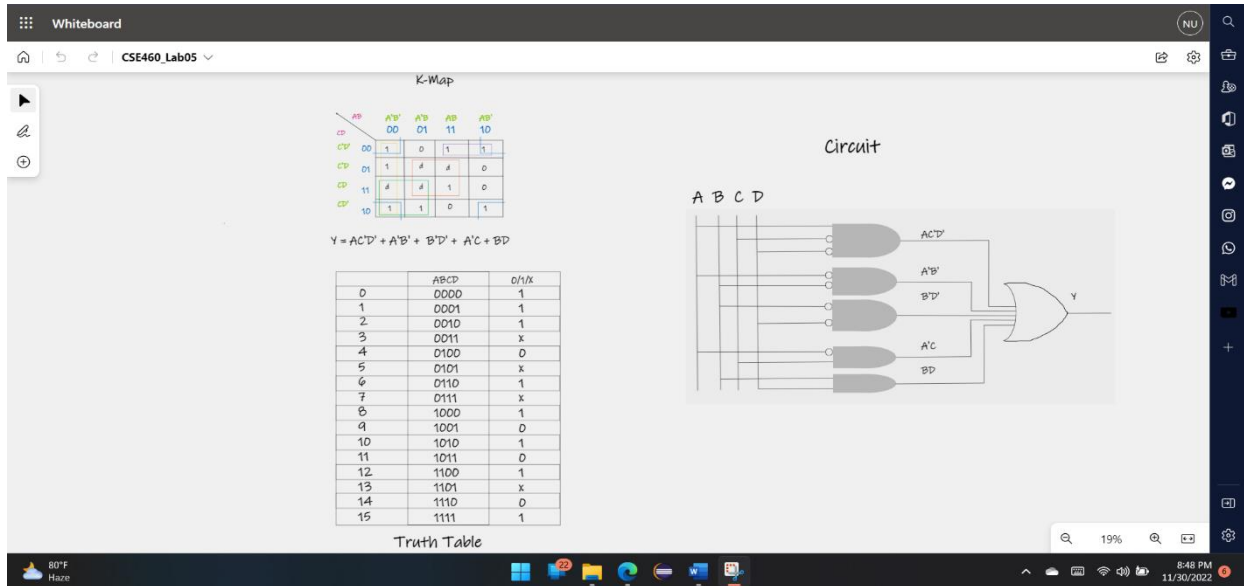
Simulation

Timing Diagram

Discussion

From the timing diagram if we compare it with the truth table, we can find that in between 2000ns-3000ns when A, B, C, D are low we get the output high. Also, when A is high and B, C, D are low we get high output at Y. Then again, when A, B, C are low, and D is high we get a high output at Y. Now if we look in between 4000ns to 5000ns, when our input A is low, B is high and other two inputs are low then we get a low output at Y. So, our timing diagram is completely representing the truth we've got.