General guidelines for good hardware description

1. Do not have more than one entity in one vhd file.
2. If you have multiple architectures per entity, they should all be in the same file.
3. The filename of a vhd file should be the same as the name of the entity in the file.
4. Entity names should be meaningful and complete. DO NOT USE SHORTHAND. Use only small case names.
5. Architecture names should be meaningful. Eg. use behavioural / structural / rtl etc. Use only small case names.
6. If you have some functions which you use; all these functions should be written in a file named as functions_projectname.vhd where project name is the name of your project.
7. If you have custom data types these should be written in a seperate file named as data_types_projectname.vhd
8. Name all signals meaningfully. DO NOT USE SHORT FORMS. Append the name with the bus width and the direction of the pin. eg. 16 bit address bus would be named as address_16_in. 32 bit databus would be named as data_bus_32_inout. All signal/pin names should be in small case.
9. Signal names should be named as name_signal. Variable names should be named as name_variable.
10. Code should be well structured in the text file. Use tabstop of 4 spaces.
11. Code should be well commented. A person who knows VLSI design but doesn't know VHDL should understand what hardware the code is describing.