

Project Report

Designing a P-MOSFET and showing its DC and AC (C_{gg} - V_{gs} ; C_{gs} - V_{gs} ; C_{gd} - V_{gs} and C_{ds} - V_{gs}) characteristics and analyzing the impact of varying substrate doping concentration and source/drain doping concentration on threshold voltage.

Channel Length: 80 nm, Oxide Thickness: 10 nm

Body Doping: $1 \times 10^{17} \text{ cm}^{-3}$, S/D Doping: $1 \times 10^{20} \text{ cm}^{-3}$

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Contents

Abstract	1
1 Introduction	2
2 Device Design and Simulation Setup	3
2.1 Device Structure	3
2.2 Simulation Environment	4
3 DC Characteristics	5
3.1 Transfer Characteristics (I_d - V_{gs})	5
3.2 Output Characteristics (I_d - V_{ds})	5
4 AC Characteristics	7
4.1 Gate Capacitance Components	7
4.2 Capacitance-Voltage Behavior	7
5 Impact of Doping Concentration on Threshold Voltage	9
5.1 Effect of Substrate Doping	9
5.2 Effect of Source/Drain Doping	9
6 Conclusion	11
References	12

Abstract

This project presents the design and simulation of a nanoscale P-channel Metal-Oxide-Semiconductor Field-Effect Transistor (P-MOSFET) with a channel length of 80 nm and an oxide thickness of 10 nm. The device is modeled using a p-type substrate doping concentration of $1 \times 10^{17} \text{ cm}^{-3}$ and heavily doped source/drain regions of $1 \times 10^{20} \text{ cm}^{-3}$. DC and AC analyses were carried out to obtain the transistor's current–voltage (I–V) and capacitance–voltage (C–V) characteristics, including $C_{gg}-V_{gs}$, $C_{gs}-V_{gs}$, $C_{gd}-V_{gs}$, and $C_{ds}-V_{gs}$.

The results show typical P-MOSFET behavior, with strong inversion occurring under negative gate bias. The threshold voltage (V_{th}) shifts significantly with substrate doping concentration due to changes in depletion charge, while source/drain doping primarily affects series resistance and junction characteristics. Increasing substrate doping leads to a higher magnitude of V_{th} , whereas reducing it lowers the threshold voltage. These results highlight the influence of doping on performance trade-offs in nanoscale PMOS device design.

Chapter 1

Introduction

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is the fundamental building block of modern integrated circuits. A P-channel MOSFET (P-MOSFET) operates with holes as the majority carriers and conducts when a negative gate-to-source voltage (V_{gs}) induces a strong inversion layer of holes in the channel.

As device dimensions shrink into the nanometer regime, parameters such as channel length, oxide thickness, and doping concentration play critical roles in determining threshold voltage, leakage current, and device speed. Proper control of these parameters is essential for achieving desired electrical characteristics.

This work focuses on designing a nanoscale P-MOSFET, analyzing both its DC and AC behavior, and studying how variations in substrate and source/drain doping affect the threshold voltage. Understanding these dependencies is crucial for optimizing device performance in low-power and high-speed CMOS circuits.

Chapter 2

Device Design and Simulation Setup

2.1 Device Structure

Table 2.1: Device Parameters

Parameter	Symbol	Value
Channel Length	L	80 nm
Gate Oxide Thickness	t_{ox}	10 nm
Body (Substrate) Doping	N_A	$1 \times 10^{17} \text{ cm}^{-3}$
Source/Drain Doping	N_D	$1 \times 10^{20} \text{ cm}^{-3}$
Channel Type	—	P-type
Gate Material	—	n ⁺ Poly-Si
Source/Drain Material	—	P ⁺ diffusion regions

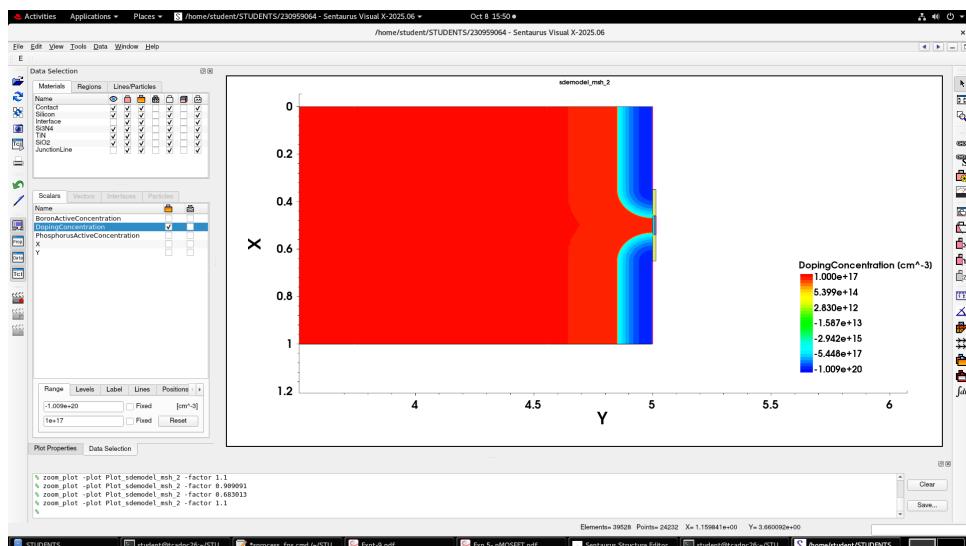


Figure 2.1: P-MOSFET after simulation using SDE

2.2 Simulation Environment

Simulations were performed using TCAD (*Synopsys Sentaurus*). The 2D structure of the P-MOSFET was defined, followed by doping profile creation, oxide definition, and electrode contacts.

Biasing conditions:

- DC analysis: $V_{ds} = -0.5$ V to -1 V, $V_{gs} = -1$ V
- AC analysis: Small-signal AC sweep at various gate voltages

Chapter 3

DC Characteristics

3.1 Transfer Characteristics (Id–Vgs)

The drain current (I_d) was plotted versus gate voltage (V_{gs}) at different drain voltages (V_{ds}). As V_{gs} becomes more negative, the inversion charge density in the channel increases, leading to a higher drain current.

Observations:

- The device turns ON when $V_{gs} < V_{th}$ (negative for PMOS).
- Subthreshold region shows exponential dependence of I_d on V_{gs} .
- Increasing V_{ds} enhances current until saturation.

3.2 Output Characteristics (Id–Vds)

The drain current (I_d) versus drain voltage (V_{ds}) for various V_{gs} values shows linear and saturation regions:

- Linear region: $I_d \propto V_{ds}$ for small $|V_{ds}|$.
- Saturation: Occurs when $|V_{ds}| > |V_{gs} - V_{th}|$.

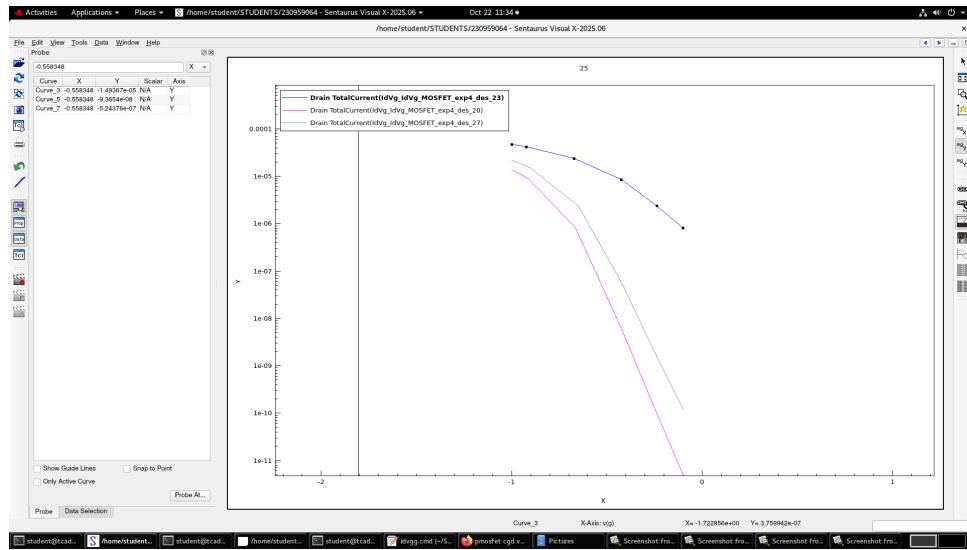


Figure 3.1: Id-Vgs Characteristics at different values of substrate and source-drain doping

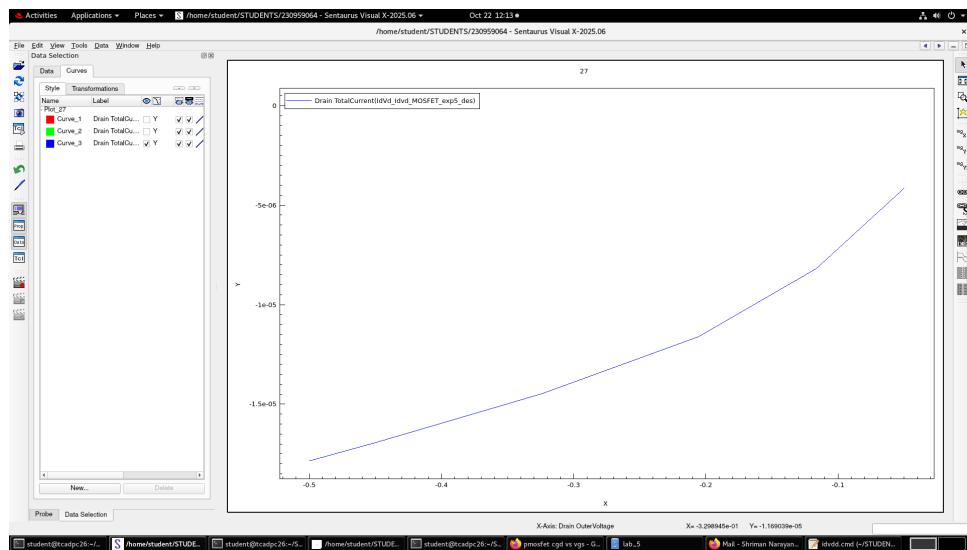


Figure 3.2: Id-Vds Characteristics

Chapter 4

AC Characteristics

4.1 Gate Capacitance Components

The total gate capacitance C_{gg} is given by:

$$C_{gg} = C_{gs} + C_{gd} \quad (4.1)$$

where C_{gs} is the gate-to-source capacitance, C_{gd} is the gate-to-drain capacitance, and C_{ds} is the drain-to-source capacitance (typically small).

4.2 Capacitance–Voltage Behavior

- At accumulation (positive V_{gs}), capacitances are dominated by oxide capacitance.
- In depletion, capacitances decrease as depletion width increases.
- In inversion, C_{gg} approaches C_{ox} again due to the formation of a conductive channel.
- C_{gd} decreases in saturation since the channel near the drain is pinched off.

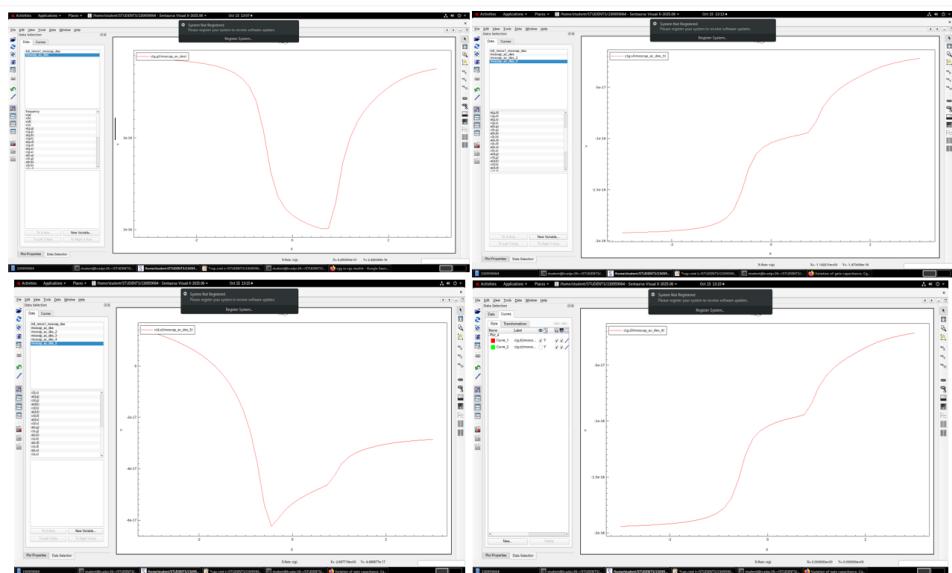


Figure 4.1: Top Left: C_{gg} vs V_{gs}; Top Right: C_{gs} vs V_{gs}; Bottom Right: C_{gd} vs V_{gs}; Bottom Left:C_{ds} vs V_{gs}

Chapter 5

Impact of Doping Concentration on Threshold Voltage

5.1 Effect of Substrate Doping

Increasing N_A increases ϕ_F and the depletion charge term, making V_{th} more negative.

Table 5.1: Variation of Threshold Voltage with Substrate Doping

Substrate Doping (N_A)	Source-Drain Doping	Threshold Voltage (V_{th})
$1 \times 10^{16} \text{ cm}^{-3}$	$1 \times 10^{20} \text{ cm}^{-3}$	-0.15 V
$1 \times 10^{17} \text{ cm}^{-3}$	$1 \times 10^{20} \text{ cm}^{-3}$	-0.70 V
$1 \times 10^{17} \text{ cm}^{-3}$	$1 \times 10^{21} \text{ cm}^{-3}$	-0.63 V

5.2 Effect of Source/Drain Doping

Increasing source/drain doping:

- Reduces contact resistance and improves current drive.
- Slightly modifies V_{th} via junction capacitance effects.
- Excessive doping can cause tunneling leakage.

Discussion The DC and AC results confirm expected PMOS operation. The threshold voltage depends strongly on substrate doping, while source/drain doping mainly affects

series resistance. Trade-offs exist between speed, leakage, and power consumption:

- Higher $N_A \rightarrow$ higher $|V_{th}|$ and lower leakage but slower switching.
- Lower $N_A \rightarrow$ faster switching but higher off-state leakage.

Chapter 6

Conclusion

A nanoscale P-MOSFET with 80 nm channel length and 10 nm oxide thickness was successfully designed and analyzed. DC and AC characteristics exhibit typical PMOS behavior with inversion under negative gate bias. Increasing substrate doping increases $|V_{th}|$, while higher source/drain doping enhances drive current and reduces series resistance. The study demonstrates how doping engineering can optimize PMOS performance for scaled CMOS technologies.

References

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3. Synopsys Sentaurus Device User Guide, Synopsys Inc.