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MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL
(A constituent unit of MAHE, Manipal)

I SEMESTER M.TECH (CSE) MIDTERM EXAMINATIONS OCT 2023

MIDTERM EXAMINATION

HIGH PERFORMANCE COMPUTING SYSTEMS [CSE 5116]

Date: 13-10-2023 Time: 10:30 AM – 12:30 PM Max. Marks: **30**

Instructions to Candidates:

- Answer ALL the questions

Q1. How do you recognize a parallel region in OpenMP, and how is it defined in code? **2M**

Q2. Interpret and explain the role of the directives required in OpenMP. Give examples of any two commonly used directives and their purposes. **3M**

Q3. Write and explain the routines of MPI with their arguments that provides point-to-point communication within a communicator. **3M**

Q4. Implement an MPI program using standard mode send and receive. The program consists of 2 processes. Process 0 sends a number and a text message to the receiver. Receiver in turn must receive this number and the text message. After this now let the receiver send the text message only back to the sender. Use the user-friendly statements where ever required in your program. **3M**

Q5. It is required for the root process to communicate a number to all its slaves. All processes (including the root) will add the number and send the total sum to the root process. Implement an efficient MPI program to meet the specification. **4M**

Q6. Interpret the use of threads, blocks, and grids in the context of CUDA? **3M**

Q7. Construct an efficient CUDA kernel to meet the following:
It is required to generate the sum of the squares of the principal diagonal elements of a given matrix A of size N X N. In your kernel use only the threadIdx to find the thread ID. **3M**

For Eg, if the given matrix A is of size 3 X 3:

$$\text{Matrix A} = \begin{matrix} 1 & 2 & 3 \\ 4 & 5 & 6 \\ 7 & 8 & 9 \end{matrix}$$

sum of the squares of the principle diagonal elements = 107 (i.e. $1^2 + 5^2 + 9^2 = 107$)

Q8. Construct the code of main ( ) function required to use the kernel you wrote in question number Q7. **4M**

Q9.

A) Sketch a specific block diagram and explain its architectural class scheme based on the multiplicity of instruction streams and data streams in which a parallel computer may execute distinct instructions and act on different data at the same time. **3M**

B) Differentiate the role of hardware and software in programmatic levels of parallel processing in parallel computer systems. **2M**