Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

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A Constituent Institution of Manipal University

I SEMESTER M.TECH (COMPUTER SCIENCE AND ENGINEERING)
END SEMESTER EXAMINATIONS, NOVEMBER 2017
HIGH PERFORMANCE COMPUTING SYSTEMS [CSE 5104]
REVISED CREDIT SYSTEM

Time: 3 Hours 23-11-2017 MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data, if any, may be suitably assumed.

1A. Starting from fundamental principles of processor bandwidth, memory bandwidth and I/O device bandwidth discuss how entire memory bandwidth is matched with the bandwidth sum of the processor and I/O devices to achieve a balanced system. **5M**

1B. Design a 2D mesh network of size 3 X 3 for a SIMD computer. In your design analyze all the possible data routing permutations. Can you deduce it to chordal ring network? If yes, draw the corresponding chordal ring network and if no, give the justification why can't it be deduced to chordal ring network. **3M**

1C. Draw a diagram of 5D hypercube network. In the network label your nodes in binary. Identify the node degree, network diameter and channel bisection width. **2M**

2A.

	1	**2**	**3**	**4**	**5**	**6**
S1	X				X	
S2			X			
S3		X		X		X

Fig. Q 2.A

For the Reservation Table given in Fig. Q 2.A

i) Determine latencies in the forbidden list, F and the collision vector, C.
ii) Draw the state transition diagram.
iii) List all simple cycles and Greedy cycles.
iv) Determine MAL.
v) Compute the efficiency of the pipeline and the corresponding throughput. **5M**

2B. With the block diagram discuss the basic structure of centralized shared memory multiprocessor system. **3M**

2C. Discuss the multiport memory organization in multiprocessor system. **2M**

3A. Write an MPI program to multiply two matrices. **5M**

3B. Write a parallel algorithm to sum n values using Shuffle-exchange SIMD model where n is the number of values to be added and p is the number of processors in the model. It is assumed that the each processor initially holds one of the values among n. **3M**

3C. For question 3B, assume Shuffle-exchange SIMD model with $n = p = 16$. Show how such addition happens using appropriate diagrams with suitable example. **2M**

4A. Write a kernel function which takes an array *A* with *N* (where *N* is multiple of 4) number of integer values as input. It modifies array *A* by swapping alternate elements (such as the elements at 0^{th} position with 2^{nd} position, 1^{st} with 3^{rd}, 4^{th} with 6^{th} , 5^{th} with 7^{th} and so on). **3M**

4B. Frame VLIW instructions for a VLIW processor for the following sequential instruction stream A. Draw a diagram showing how a VLIW based execution takes place in such system. Assume that the system has two Integer ALUs and one Floating point ALU. What difference is found on scheduling these VLIW instructions compared to the sequential scheduling? Discuss.

Instruction Stream A

```
add a, b, c
mul d, a, c
mul f, d, e
add a, f, g
fmul h, a, f
```

3M

4C. Write a convolution kernel in OpenCL that describes how each pixel will be influenced by its neighbors in a given image. **4M**

5A. Write down the important steps in implementation of OpenCL program with the supporting APIs. Just name the APIs in every steps. **4M**

5B. Write a kernel in CUDA to multiply two Matrices A and B of dimensions $M \times N$ and $N \times P$ resulting in Matrix C of dimension $M \times P$. Create P number of threads, and each column of the resultant matrix is to be computed by one thread. **3M**

5C. Give a diagram for mapping the memory model defined by OpenCL to the architecture of a GPU. **3M**