MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL
(A constituent unit of MAHE, Manipal)

I SEMESTER M.TECH. (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER EXAMINATIONS, DECEMBER - 2023

HIGH PERFORMANCE COMPUTING SYSTEMS [CSE 5116]

Date: 07/12/2023 [9:30 AM – 12:30 PM]

Time: 3 Hours

MAX. MARKS: 50

Instructions: Answer ALL the questions.

1A. Explain the use of reduction clause in OpenMP. Write an OpenMP program that reads an array. Further apply the use of this operator in the program to calculate the sum of all the elements in the array using parallelization. — **5M**

1B. Sketch a relevant block diagram to explain the concept of shared memory in symmetric multiprocessor systems. — **3M**

1C. Define the node degree and the network diameter metrics of a static interconnection network of SIMD computers. — **2M**

2A. Implement an MPI program to meet the following:
The master process initializes an array and then distributes an equal portion of that array to the other processes. After the other processes receive their portion of the array, they perform an addition operation to each array element. They also maintain a sum for their portion of the array. The master process does likewise with its portion of the array. An appropriate MPI call is used to collect the sums maintained by each process. Finally, the master process displays global sum of array elements. Assume that the number of elements is evenly divisible by number of processes. — **5M**

2B. Interpret and explain different built-in MPI reduction operators. Write the appropriate API in using any one of the MPI reduction operators. — **3M**

2C. Construct a skeleton part of the MPI program to show the possibility of occurrence of deadlock when using point to point communication routines. — **2M**

3A. Organize and list the steps in implementation of OpenCL program with the supporting APIs. Just name the APIs in every step. — **5M**

3B. Construct an OpenCL kernel for multiplying two matrices A and B of size $M \times N$ and $N \times P$. Each row of A has to be multiplied by a separate work item. — **5M**

4A. Implement a parallel algorithm to sum n values using Shuffle-exchange SIMD model where n is the number of values to be added and p is the number of processors in the model. It is assumed that each processor initially holds one of the values among n. — **4M**

4B. For question 4A, assume Shuffle-exchange SIMD model with $n = p = 8$. Demonstrate to show how such addition happens using appropriate diagrams with suitable example. — **3M**

4C. Discuss message passing and shared-memory models in the context of parallel programming models. — **3M**

5A. Design 8 × 8 baseline multistage network. Explain your design methodology.

4M

5B. Implement a kernel in CUDA to multiply two Matrices A and B of dimensions $M \times N$ and $N \times P$ resulting in Matrix C of dimension $M \times P$. Create P number of threads, and each column of the resultant matrix is to be computed by one thread.

5C. Describe what is meant by GPU computing?

4M

2M