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MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent institution of MAHE, Manipal)

I SEMESTER M.TECH. (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER EXAMINATIONS, NOV 2018

HIGH PERFORMANCE COMPUTING SYSTEMS [CSE 5104]

REVISED CREDIT SYSTEM
(27/11/2018)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. Name and discuss one of the parallel processing mechanism in which DMA operation is conducted on a cycle-stealing basis in uniprocessor system. **2M**

1B. Draw a nonlinear pipeline block diagram with its reservation table. In this pipeline, there exists a feedback connection from last stage to the first stage and also the linear connections between the stages S_i to S_{i+1} where $0< i < 3$. The input to the pipeline for the function evaluation begins at stage S_1.The evaluation time of a function by this pipeline is found to be 5 clock cycles and all successor stages must be used after each clock cycle. Find the forbidden list of avoided latencies F, collision vector C, the state transition diagram, all simple cycles, greedy cycles, constant cycles, MAL. **5M**

1C. Discuss the role of hardware and software in programmatic levels of parallel processing in parallel computer systems. **3M**

2A. Design an interconnection network for a SIMD computer having 16 nodes with the following routing functions where the address of a node shown is in binary. Also write the permutation cycles.

$$\beta_k\,(a_{n-1}\ldots a_{k+1}\;a_k\;a_{k-1}\;\ldots\;a_1\;a_0) = (a_{n-1}\ldots a_{k+1}\;a_0\;a_{k-1}\ldots a_1\;a_k)$$

5M

2B. Draw the cross point switch in a crossbar network and discuss its importance. **3M**

2C. What is symmetric shared memory multiprocessor? Draw its diagram and discuss its architecture. **2M**

3A. Write a parallel algorithm to sum *n* values in hypercube SIMD model. Given that $n = p$ where *n* is the number of values to be added and *p* is the number of processors in the model. What is the time complexity of your algorithm? **5M**

3B. Write an MPI program to add elements of an array using two processes. Use only point to point communication APIs in your program and use the user friendly statements wherever it is needed. **5M**

4A. There are three integer arrays A, B and C each of size 1024. Write an OpenCL kernel to find X and Y. Here X is an array containing the elements as sum of respective elements of A and B. Y is also an array containing the elements as the sum of respective elements of X and C.

In host program, assume there is already a platform id created named *platid*, a device id named *devid*, context *con* and command queue *cq*. Write the OpenCL API calls to create the buffers for X and Y. Also write the API call to invoke this kernel to meet the specified array size. **5M**

4B. Write an OpenCL kernel that takes a string S as input and one integer value N. Produce a string N times as follows in parallel:
Input: S = Kalam N = 4
Output String: KalamKalamKalamKalam
Note that each work-item copies same character from the Input N times to the required position in output string. **3M**

4C. Instruction stream A and stream B are given below:

Instruction Stream A	*Instruction Stream B*
add a, b, c	fadd a, b, c
mul d, b, e	fmul d, a, e
mul f, a, e	mul f, d, f
add a, d, g	add a, b, d
fmul h, a, f	fmul f, a, f

Show and explain how the execution resources are more effectively utilized in a system having two integer ALUs and one floating point ALU using Simultaneous Multithreading. **2M**

5A. Provide a visual for applying a convolution filter to a source image. Discuss on how you obtain the pixel values for filtered image. **2M**

5B. How will you calculate the threadId of each thread in CUDA for
i) 2D Grid of 1D Block
ii) 1D Grid of 1D Block **3M**

5C. Write a CUDA kernel to compute the value of Y for different values of X in the equation Y = mX + C where m is the slope of line and C is a constant. In your CUDA main program, show how to create 256 CUDA threads with one thread on each values of X. Pass the grid and block dimensions to the kernel using dim3 structure. Also include the CUDA code used to compute the time of execution of this kernel. **5M**