PHYSICS

Class XII

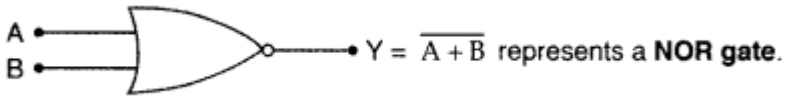
Chapter 14-Semiconductor Electronics Materials Devices and Simple Circuits

1 Mark Question

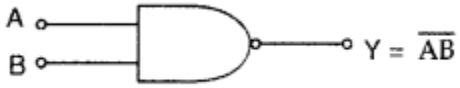
Question 1.
State the reason, why GaAs is most commonly used in making of a solar cell.
Answer:
GaAs is most commonly used in making of a solar cell because :
(i) It has high optical absorption (~ 104 cm^{-1}) .
(ii) It has high electrical conductivity.

Question 2.
Why should a photodiode be operated at a reverse bias?
Answer:
As fractional change in minority charge carriers is more than the fractional change in majority charge carriers, the variation in reverse saturation current is more prominent.

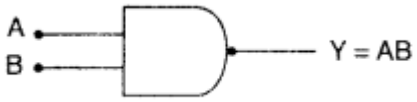
Question 3.
Give the logic symbol of NOR gate.
Answer:



Question 4.
Give the logic symbol of NAND gate.
Answer:



Question 5.
Give the logic symbol of AND gate.
Answer:



Question 6.
In a transistor, doping level in base is increased slightly. How will it affect
(i) collector current and
(ii) base current?
Answer:
Increasing base doping level will decrease base resistance and hence increasing base current, which results in a decrease in collector current.

Question 7.
What happens to the width of depletion layer of a p-n junction when it is
(i) forward biased,
(ii) reverse biased?
Answer:
(i) In forward biased, the width of depletion layer of a p-n junction decreases.
(ii) In reverse biased, the width of depletion layer of a p-n junction increases

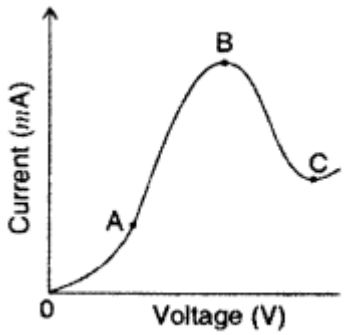
Question 8.
What is the difference between an H-type and a p-type intrinsic semiconductor?
Answer:

n-type semiconductor	*p-type semiconductor*
The electron density (n_e) is much greater than the hole density (n_h), *i.e.*, $n_e >> n_h$.	The hole density (n_h) is much greater than the electron density (n_e), *i.e*, $n_h >> n_e$.

Question 10.
How does the depletion region of a p-n junction diode get affected under reverse bias?
Answer:
Depletion region widens under reverse bias.

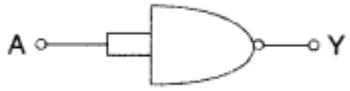
Question 11.
How does the width of depletion region of a p-n junction diode change under forward bias?
Answer:
The width of depletion region of a p-n junction

Question 12.
The graph shown in the figure represents a plot of current versus voltage for a given semi-conductor. Identify the region, if any, over which the semi-conductor has a negative resistance.



Answer:
Between the region B and C, the semiconductor has a negative resistance.

Question 13.
Write the truth table for a NAND gate as shown in the figure.



Answer:
Truth table for NAND gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Question 14.
What is the function of a photodiode?
Answer:
A photodiode is a special purpose p-n junction diode fabricated with a transparent window to allow light to fall on diode. It is operated under reverse bias.

Question 15.
Write the truth table for a NOT gate connectedA as shown in the figure.

Answer:
Truth Table

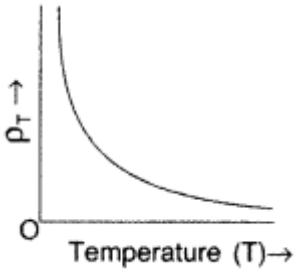
A	B	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$	$\overline{\overline{A}+\overline{B}} = A.B$
0	0	1	1	1	0
0	1	1	0	1	0
1	0	0	1	1	0
1	1	0	0	0	1

This combination acts as AND gate.

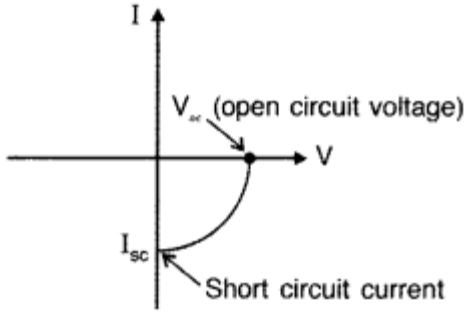
Question 16.
Write the truth table of a two point input NAND gate.
Answer:
Truth Table:

A	B	$Y = \overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

Question 17.
Show variation of resistivity of Si with temperature in a graph.
Answer:



Question 18.
Plot a graph showing variation of current versus voltage for the material GaAs.
Answer:
A Graph showing variation of current versus voltage for GaAs

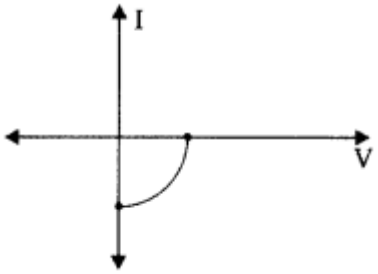


Question 19.
Draw the logic symbol of NAND gate and give its Truth Table.
Answer:
Symbol of NAND Gate
Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Question 20.
Identify the logic gate whose output equals 1 when both of its inputs are 0 each.
Answer:
NAND gate or NOR gate.

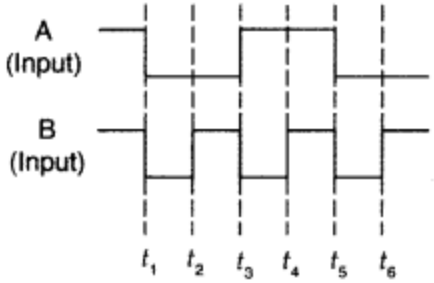
Question 21.
Name the junction diode whose I-V characteristics are drawn below:



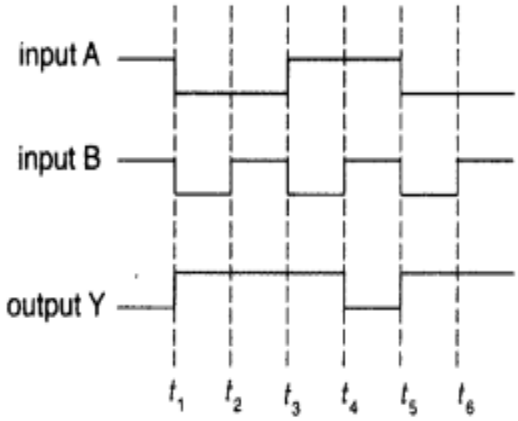
Answer:
Solar cell

2 Mark Question

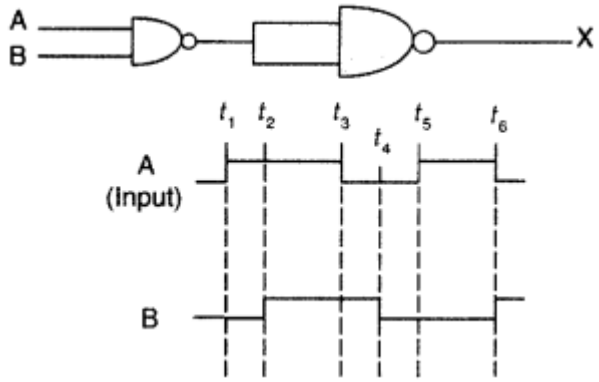
Question 1.
The given inputs A, B are fed to a 2-input NAND gate. Draw the output wave form of the gate.



Answer:



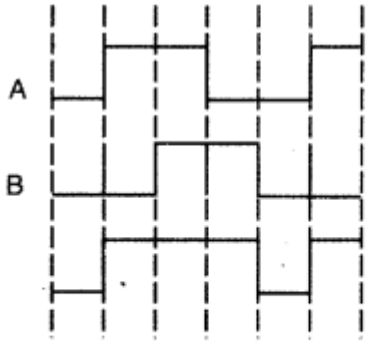
Question 2.
Draw the output wave form at X, using the given inputs A, B for the logic circuit shown below. Also identify the gate.



Answer:

A	B	$\overline{A.B} = Y_1$	$\overline{Y}_1 = X$
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

$\therefore$ The logic gate is *OR gate.*

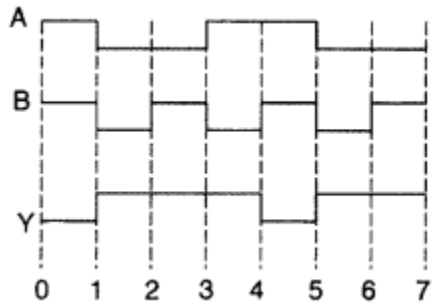


Output Waveform

Question 3.
If the output of a 2 input NOR gate is fed as both inputs A and B to another NOR gate, write down a truth table to find the final output, for all combinations of A, B.
Answer:
The truth table is:

A	B	$Y = \overline{A+B}$	$\overline{Y} = Y'$
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Question 4.
The following figure shows the input waveforms (A, B) and the output waveform (Y) of gate. Identify the gate, write its truth table and draw its logic symbol.



Answer:

Truth table is :

A	B	Y
1	1	0
0	0	1
0	1	1
1	0	1
1	1	0
0	0	1
0	1	1

Symbol

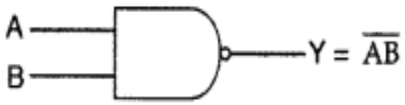
This truth table represents a *'NAND' gate.*

Question 5.
The output of a 2-input AND gate is fed to a NOT gate. Give the name of the combination and its logic symbol. Write down its truth table.

Answer:

Name : NAND gate.

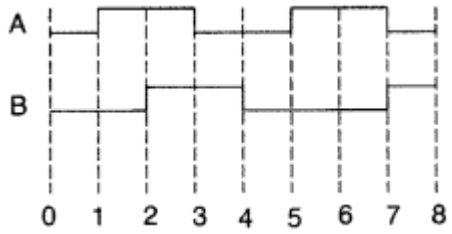
Its symbol is :



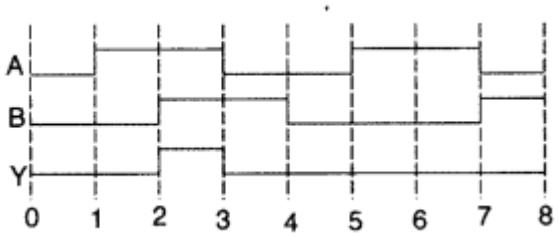
Truth table is :

A	B	$Y = \overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

Question 6.
(i) Sketch the output waveform from an AND gate for the inputs A and B shown in the figure.

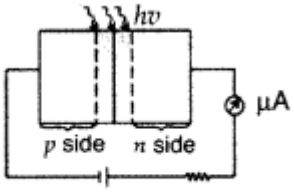


(ii) If the output of the above AND gate is fed to a NOT gate, name the gate of the combination so formed.
Answer:
(*i*)



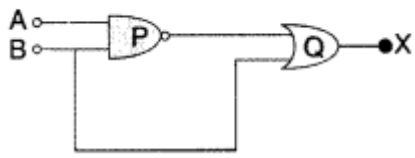
(ii) If this output of AND gate is fed to a NOT gate, the result will be a NAND gate.

Question 7.
Draw the circuit diagram of an illuminated photodiode in reverse bias. How is photodiode used to measure light intensity?
Answer:
A measurement of the change in the reverse. saturation current on illumination can give the values of light intensity because photocurrent is pro-portional to incident light intensity.



A reverse biased photodiode illuminated with light.

Question 8.
(i) Identify the logic gates marked P and Q in the given logic circuit.
(ii) Write down the output at X for the inputs A = 0, B = 0 and A = 1, B = 1.



Answer:

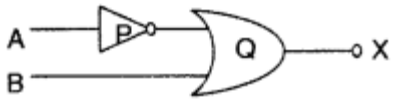
(i) P is NAND gate and Q is OR gate.

(ii)

A	B	$\overline{AB} = \overline{A} + \overline{B}$	$(\overline{A} + \overline{B}) + B$
0	0	1	1
1	1	0	1

Question 9.

(i) Identify the logic gates A marked P and Q B in the given logic circuit.



(ii) Write down the output at X for the inputs A = 0, B = 0 and A = 1, B = 1.

Answer:

(i) P is NOT gate

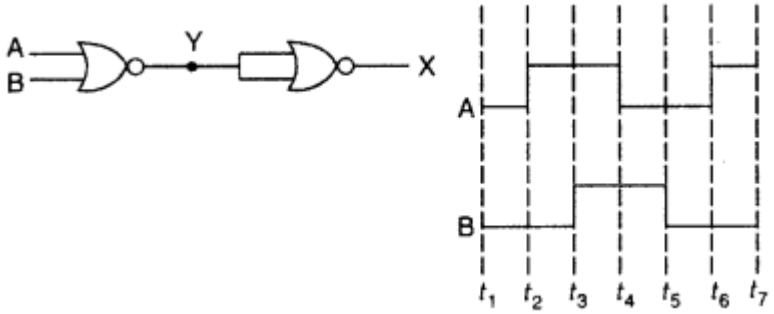
Q is OR gate

(ii)

Input		Output
A	B	$X = \overline{A} + B$
0	0	1
1	1	1

Question 10.

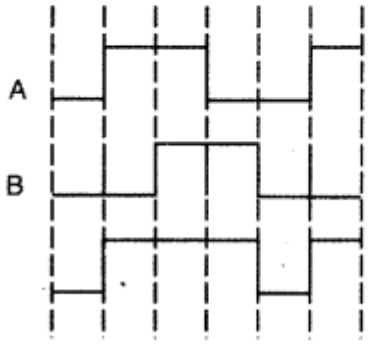
Draw the output wave form at X, using the given inputs A and B for the logic circuit shown below. Also, identify the logic operation performed by this circuit.



Answer:

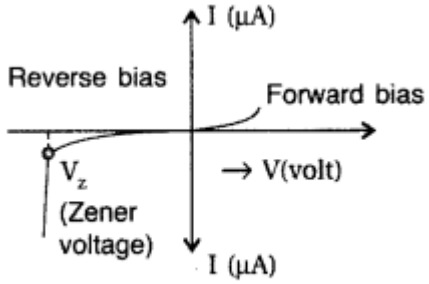
A	B	$\overline{A.B} = Y_1$	$\overline{Y}_1 = X$
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

$\therefore$ The logic gate is *OR gate.*



Output Waveform

Question 11.
Name the semiconductor device that can be used to regulate an unregulated dc power supply. With the help of I-V characteristics of this device, explain its working principle.
Answer:
Name : Zener diode is used to regulate an unregulated dc power supply.

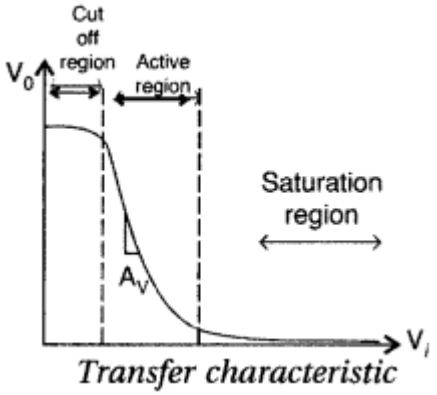


V-I charactertic

Working principle : When a zener diode is operated in the reverse break down region, the voltage across it remains practically constant (equal to the break down voltage V-I) for a large change in the reverse current.

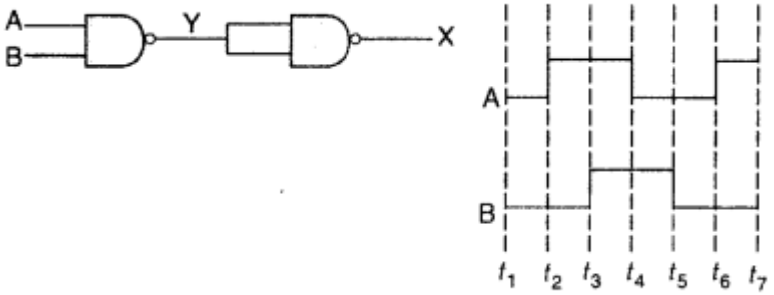
Question 12.
Draw the transfer characteristic curve of a base biased transistor in CE configuration. Explain clearly how the active region of the VD versus V, curve in a transistor is used as an amplifier.
Answer:
For using the transistor as an amplifier we will use the active region of the V0 vs. V, curve. The slope of the linear part of the curve represents the rate of change of the output with input. It is negative, that is why as input voltage of the CE amplifier increases its output voltage decreases and the output is said to be out of

phase with input.



Transfer characteristic

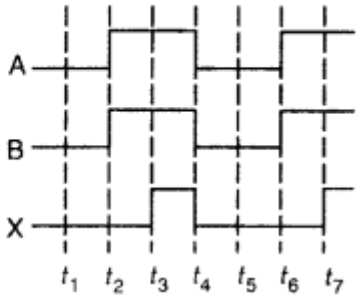
Question 13.
Draw the output waveform at X, using the given inputs A and B for the logic circuit shown below. Also, identify the logic operation performed by this circuit.



Answer:

Both are *NAND Gates.*
Truth table is :

Input		*Output*		
A	***B***	***Y = A.B***	***Y***	***X***
0	0	0	1	0
0	1	0	1	0
1	0	0	1	0
1	1	1	0	1



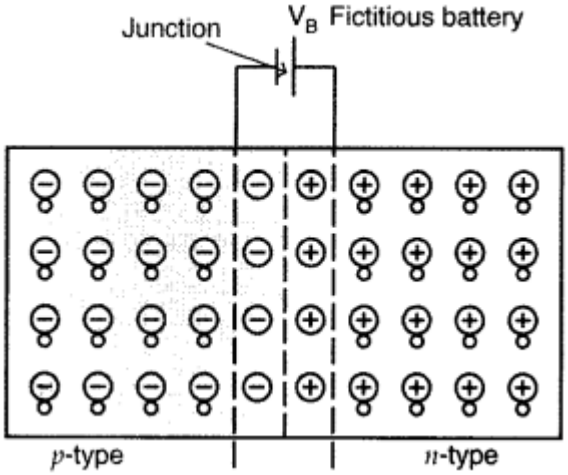
Question 14.
How is forward biasing different from reverse biasing in a pn junction diode?
Answer:
Forward biasing : If the positive terminal of a battery is connected to a p-side and the negative terminal to the 72-side, then the p-n junction is said to be forward biased. Here the applied voltage V opposes the barrier voltage VB. As a result of this

- the effective resistance across the p-n junction decreases.
- the diffusion of electrons and holes into the depletion layer which decreases its width.

Reverse biasing : If the positive terminal of a battery is connected to the 72-side and negative terminal to the p-side, then the p-n junction is said to be reverse biased.
The applied voltage V and the barrier potential V_B are in the same direction. As a result of this

- the resistance of the p-n junction becomes very large.
- the majority charge carriers move away from the junction, increasing the width of the depletion layer.

Question 15.
Explain how a depletion region is formed in a junction diode.
Answer:
As soon as a p-n junction is formed, the majority charge carriers begin to diffuse from the regions of higher concentration to the regions of lower concentrations. Thus the electrons from the n-region diffuse into the p-region and where they combine with the holes and get neutralised. Similarly, the holes from the p-region diffuse into the n-region where they combine with the electrons and get neutralised. This process is called electron-hole recombination.



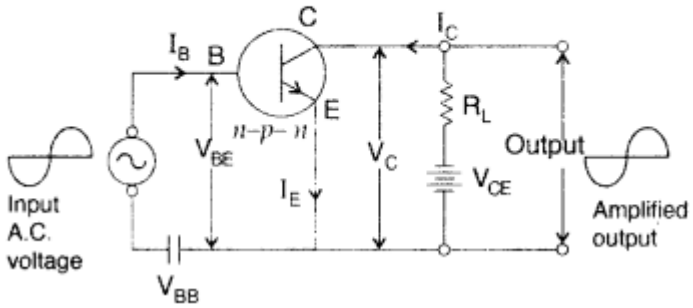
The p-region near the junction is left with immobile -ve ions and n-region near the junction is left with +ve ions as shown in the figure. The small region in the vicinity of the junction which is depleted of free charge carriers and has only immobile ions is called the depletion layer. In the depletion region, a potential difference VB is created, called potential barrier as it creates an electric field which opposes the further diffusion of electrons and holes.
(i) In forward biased, the width of depletion region is decreased.
(ii) In reverse biased, the width of depletion region is increased.

4 Mark Question

Question 1.
Draw the labelled circuit diagram of a common-emitter transistor amplifier. Explain clearly how the input and output signals are in opposite phase.
Answer:
The diagram shows the circuit diagram of a n-p-n trasistor as a CE amplifier. In this diagram it is evident that the base-emitter junction is forward biased whereas collector emitter junction is set to be reverse biased for an ideal operation as an amplifier. In absence of any input a.c. signal the p.d. between collector and emitter is given by

$$V_C = V_{CE} - I_C R_L$$

...where [V_{CE} is the voltage of battery V_{CE}) ...(*i*)



In the presence of an input a.c. signal, the forward biased voltage increases resulting in an increase in collector current I_C during the positive half cycle, which further decreases the V_C from equation (i) Whereas I_E and I_C both decrease during the negative half cycle as a result of reverse biasing of input section, the decrease in I_C increases the V_C. So the change in V_C during the positive and negative half input cycle results in a 180° phase difference between input and output.

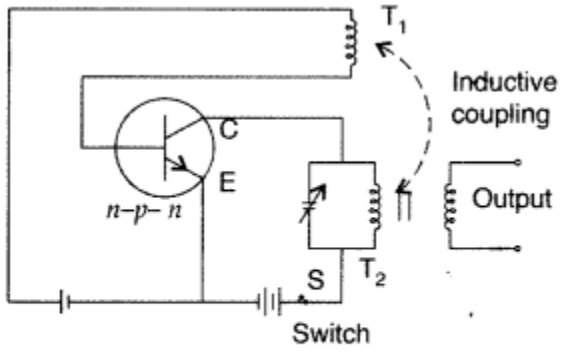
Question 2.

State briefly the underlying principle of a- transistor oscillator. Draw a circuit diagram showing how the feedback is accomplished by inductive coupling. Explain the oscillator action.

Answer:

Principle of transistor oscillator : "Sustained a.c. signals can he obtained from an amplifier circuit without any external input signal by giving a positive feedback to the input circuit through inductive coupling or RC/LC network."

Oscillator action : In an ideal n-p-n biased transistor, when input base emitters junction and output base collector junction are forward and reverse biased respectively, a high collector current I_C flows through the circuit. If in circuit switch S is on, this current I_C will start flowing in the emitter circuit through the inductive coupling between coils T_1 and T_2, which provides the +ve feedback output to input and hence make I_E maximum. In the absence of +ve feedback the IE thus decreases making the circuit back to its original state. This process continues and ocillations are produced.

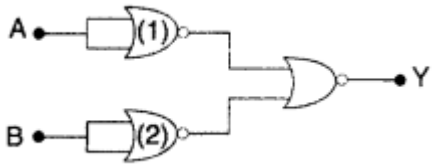


The f_R resonance frequency is thus given by

$$f = \frac{1}{2\pi\sqrt{LC}}$$

7 Marks Questions

Question 1.
The inputs A and B are inverted by using two NOT gates and their outputs are fed to the NOR gate as shown:
Analyse the action of the gates (1) and (2) and identify the logic gate of the complete circuit so obtained. Give its symbol and the truth table.



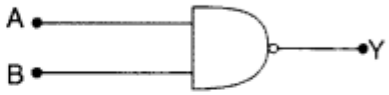
Answer:

The output $Y = \overline{\overline{A} + \overline{B}} = \overline{\overline{A}}.\overline{\overline{B}} = A.B$

(*i*) The gates (1) and (2) act as NOT gate (made from NOR gates).

(*ii*) The logic gate of the complete circuit is AND gate.

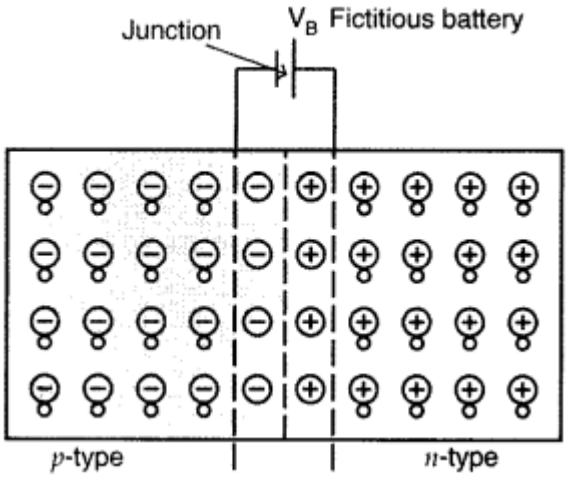
Symbol :



Truth table is

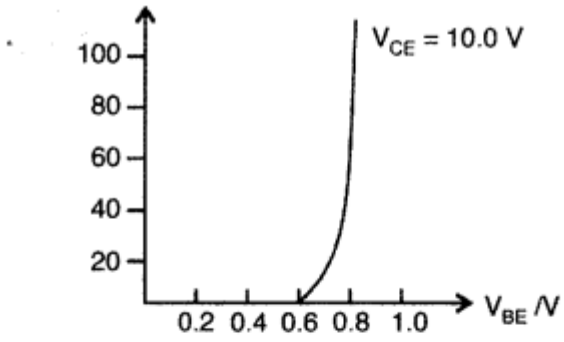
A	*B*	$Y = A.B$
0	0	0
0	1	0
1	0	0
1	1	1

Question 2.
With the help of a suitable diagram, explain the formation of depletion region in a p-n junction. How does its width change when the junction is
(i) forward biased, and
(ii) reverse biased?
Answer:
As soon as a p-n junction is formed, the majority charge carriers begin to diffuse from the regions of higher concentration to the regions of lower concentrations. Thus the electrons from the n-region diffuse into the p-region and where they combine with the holes and get neutralised. Similarly, the holes from the p-region diffuse into the n-region where they combine with the electrons and get neutralised. This process is called electron-hole recombination.

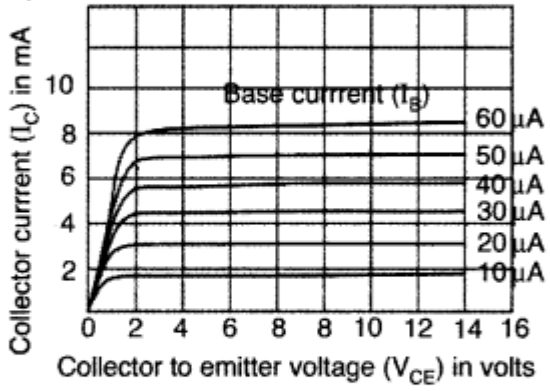


The p-region near the junction is left with immobile -ve ions and n-region near the junction is left with +ve ions as shown in the figure. The small region in the vicinity of the junction which is depleted of free charge carriers and has only immobile ions is called the depletion layer. In the depletion region, a potential difference VB is created, called potential barrier as it creates an electric field which opposes the further diffusion of electrons and holes.
(i) In forward biased, the width of depletion region is decreased.
(ii) In reverse biased, the width of depletion region is increased.

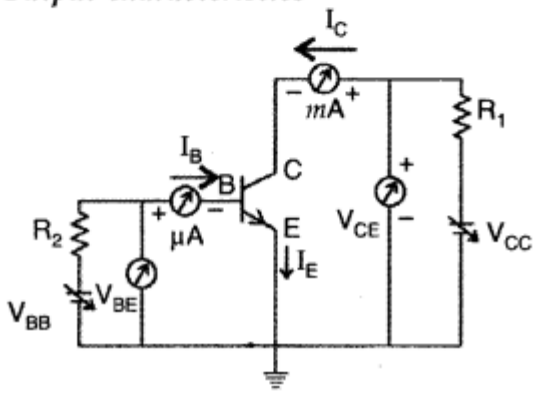
Question 3.
Give a circuit diagram of a common emitter amplifier using an n-p-n transistor. Draw the input and output waveforms of the signal. Write the expression for its voltage gain.
Answer:
(i) (a) Common emitter configuration of n-p-n transistor



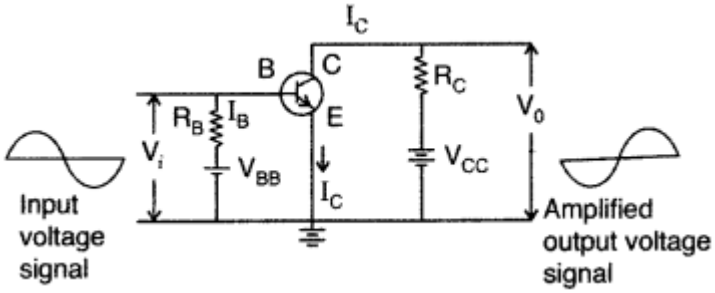
(b) Input characteristics



(c) Output characteristics



(ii) Transistor as an amplifier (C.E. configuration) : The circuit diagram of a common emitter amplifier using n-p-n transistor is given below :



The input (base-emitter) circuit is forward biased and the output circuit (collector- emitter) is reverse biased. When no a.c. signal is applied, the potential difference V_{CC} between the collector and emitter is given by

$$V_{CC} = V_{CE} + I_C R_C$$

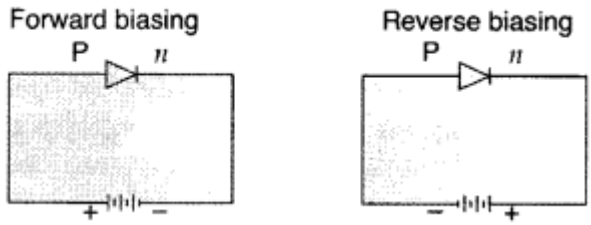
When an a.c. signal is fed to the input circuit, the forward bias increases during the positive half cycle of the

input. This results in increase in I_C and decreases in V_{CC}. Thus during positive half cycle of the input, the collector becomes less positive.

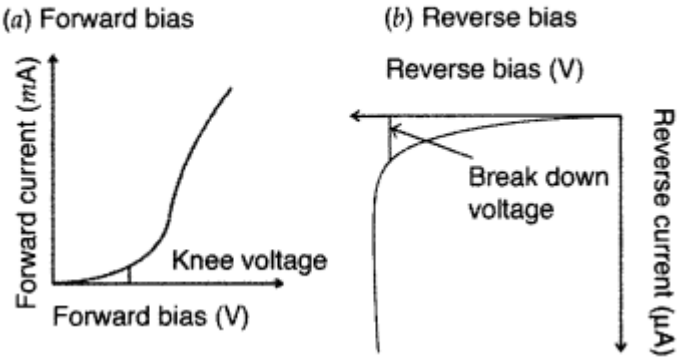
During the negative half cycle of the input, the forward bias is decreased resulting in decrease in I_E and hence I_C. Thus V_{CC} would increase making the collector more positive. Hence in a common-emitter amplifier, the output voltage is 180° out of phase with the input voltage.

$$A_V = \frac{V_0}{V_i} = \frac{I_C R_C}{I_B R_B} = \beta\left(\frac{R_C}{R_B}\right) \qquad \left[\because \beta = \frac{I_C}{I_B}\right.$$

Question 4.
(i) With the help of circuit diagrams, distinguish between forward biasing and reverse biasing of a p-n junction diode.
(ii) Draw V-I characteristics of a p-n junction diode in
(a) forward bias,
(b) reverse bias.
Answer:
(i)



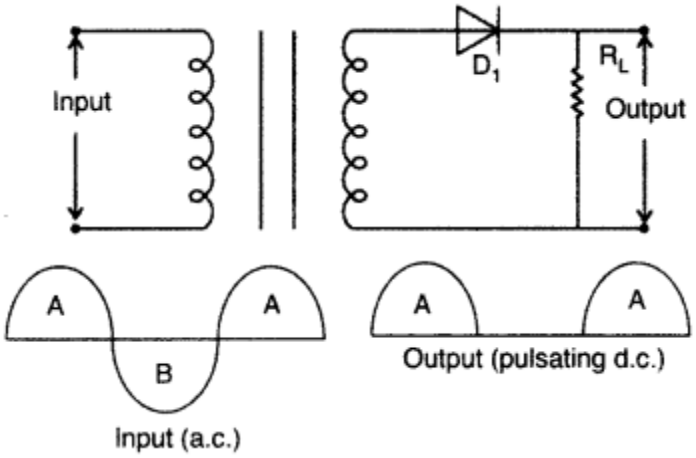
(ii) V-I characteristics of a p-n junction diode



Question 5.
Explain with the help of a circuit diagram how a zener diode works as a DC voltage regulator. Draw its I – V characteristics.

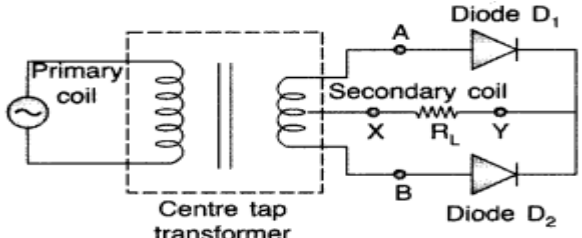
Answer:
Zener diode is fabricated by heavily doping both p and n-sides. Due to this, depletion region formed is very thin (< 10^{-6} n and the electric field of the junction is extremely high (~5×10^6 V / m) even for a small reverse bias voltage of 5 volts. It is seen that when the applied reverse bias voltage (V) reaches the breakdown voltage (Vz) of the Zener diode, there is a large change in the current. After the breakdown

voltage Vz, a large change in the current can be produced by almost insignificant change in the reverse bias voltage. In other words, Zener voltage remains constant even though current through the Zener diode varies over a wide range. This property of the Zener diode is used for regulating voltages so that they are constant.
Semiconductor diode as a half wave Rectifier : The junction diode D, supplies rectified current to the band during one half of the alternating input voltage and is always in the same direction. During the first half cycles of the alternating input voltage, junction diodes D_1 will conduct each permitting current to flow during one half cycle whenever its p-terminal is positive with respect to the n-terminal.

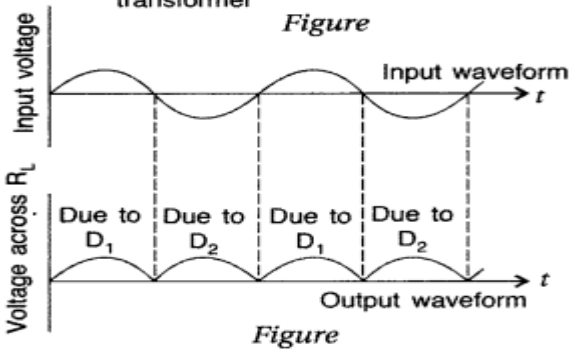


The resulting output current is a series of unidirectional pulses with alternate gaps.

Question 6.
Draw a labelled diagram of a full wave rectifier circuit. State its working principle. Show the input-output waveforms.
Answer:
p-n junction diode as full wave rectifier
A full wave rectifier consists of two diodes and special type of transformer known as centre tap transformer as shown in the circuit. The secondary of transformer gives the desired a.c. voltage across A and B.
During the positive half cycle of a.c. input, the diode D_1 is in forward bias and conducts current while D_2 is in reverse biased and does not conduct current. So we get an output voltage across the load resistor R_L.



Figure



Figure

During the negative half cycle of a.c. input, the diode D_1 is in reverse biased and does not conduct current

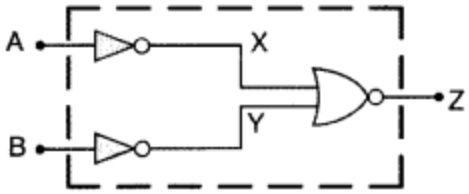
while diode D_2 in forward biased and conducts current. So we get an output voltage across the load resistor R_L.
NOTE: This is a more efficient circuit for getting rectified voltage or current.

Let $I = I_0 \sin wt$ be the input current to be rectified

$\therefore$ The average current $= \frac{2I_0}{\pi}$

Hence output voltage $= \frac{2I_0}{\pi} R_L$

Question 7.
You are given a circuit below. Write its truth table. Hence, identify the logic operation carried out by this circuit. Draw the logic symbol of the gate it corresponds to.



Answer:

The gate equivalent to the dotted box is *AND gate.*

Truth table :

Input		*Output*
A	*B*	*Y = A.B*
0	0	0
0	1	0
1	0	0
1	1	1

Logic symbol :

Fill in the blanks

1. What bonds are present in a semiconductor is ---------- **(Covalent)**

2. The number of electrons in the valence shell of a semiconductor is----------**(4)**

3. What happens to the forbidden energy gap of a semiconductor with the fall of temperature----------
(Increases)

Multiple choice questions

1. In a p-type semiconductor, the current conduction is due to

a. Holes
b. Atoms
c. Electrons
d. Protons

Answer: (a) Holes

Explanation: In a p-type semiconductor, the current conduction is due to holes.

2. What is the main function of a transistor?

a. Simplify
b. Amplify
c. Rectify
d. All of the above

Answer: (b) Amplify

Explanation: The main function of a transistor is to amplify.

3. In a semiconductor, what is responsible for conduction?

a. Electrons only
b. Holes only
c. Both electrons and holes
d. Neither electrons nor holes

Answer: (c) Both electrons and holes

Explanation: Both electrons and holes are responsible for conduction in a semiconductor.

4. What happens to the resistance of semiconductors on heating?

a. Increases
b. Decreases
c. Remains the same
d. First increases later decrease

Answer: (b) decreases

Explanation: The resistance of semiconductors decreases on heating.

5. In intrinsic semiconductors at room temperature, the number of electrons and holes are

a. Unequal
b. Equal
c. Infinite
d. Zero

Answer: (b) Equal

Explanation: In intrinsic semiconductors, the number of electrons and holes are equal.

6. Which of the following is not a universal gate?

a. NOT
b. AND
c. OR
d. NAND

Answer: (d) NAND

Explanation: NAND is not a universal gate.

7. A p-type semiconductor is

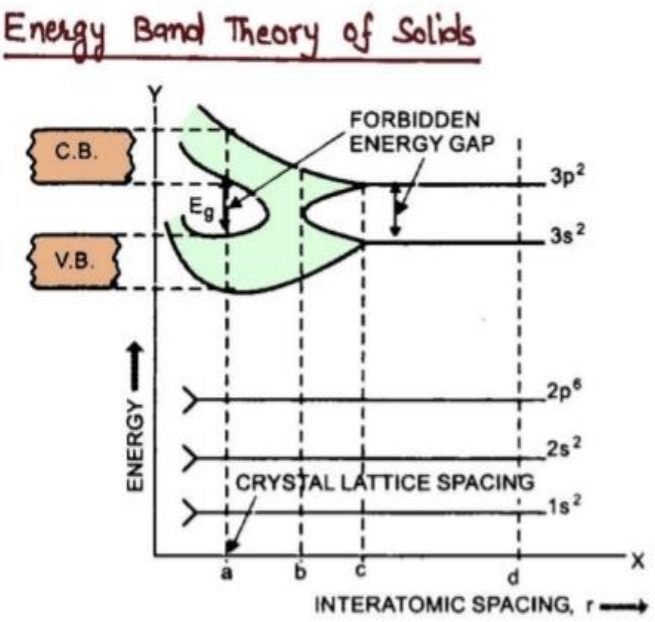
a. Positively charged
b. Negatively charged
c. Uncharged
d. None of the above

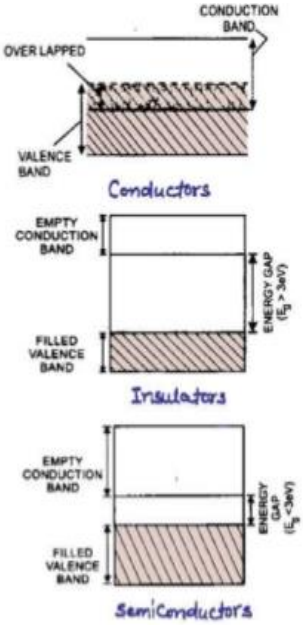
Answer: (c) Uncharged

Explanation: A p-type semiconductor is electrically neutral that is uncharged.

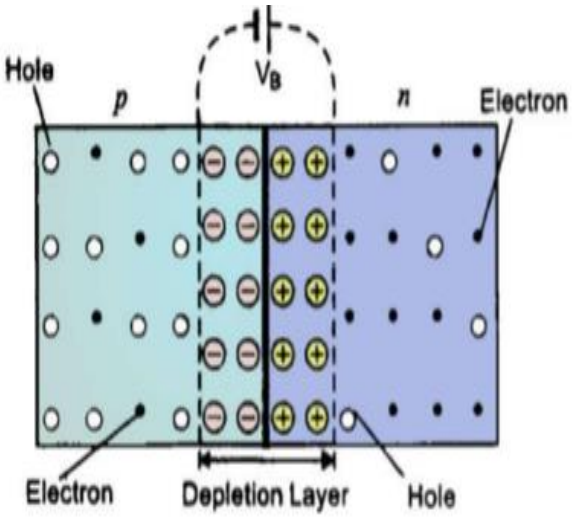
Diagrams

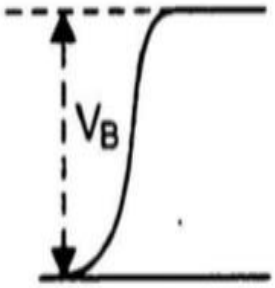
Energy Band Theory of Solids





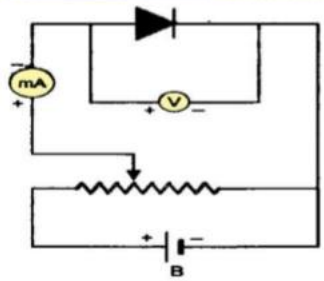
P-N JUNCTION

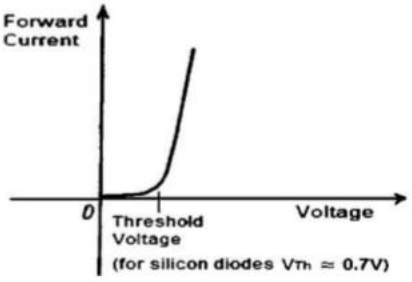




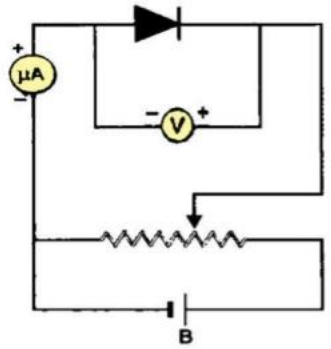
CHARACTERISTICS OF PN JUNCTION DIODE

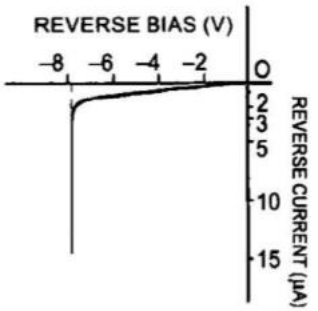
(i) Forward Characteristics



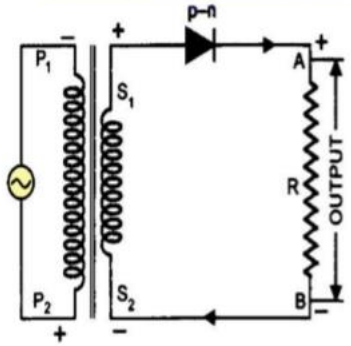


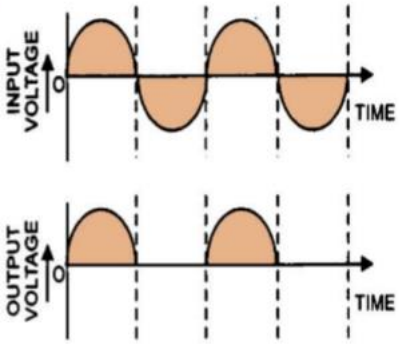
(ii) Reverse Characteristics



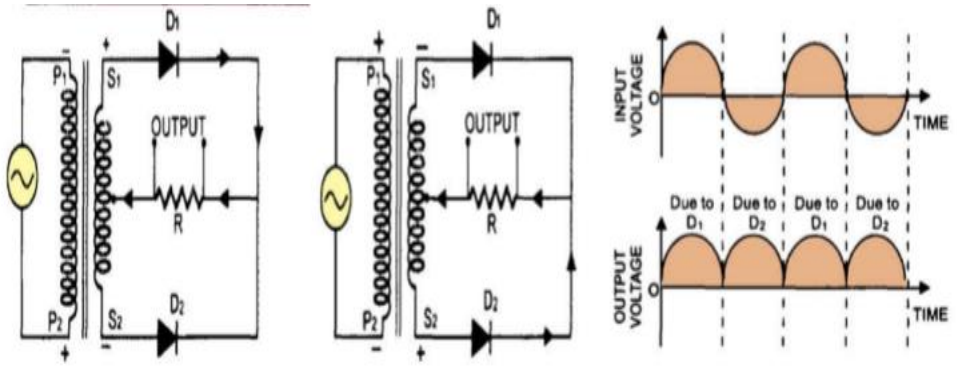


(1) HALF WAVE RECTIFIER

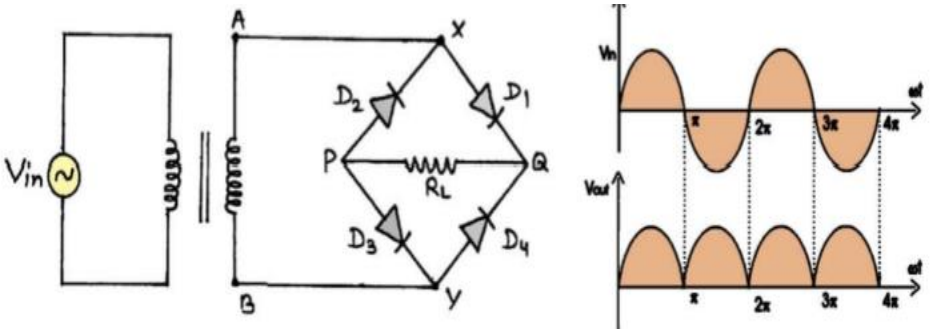




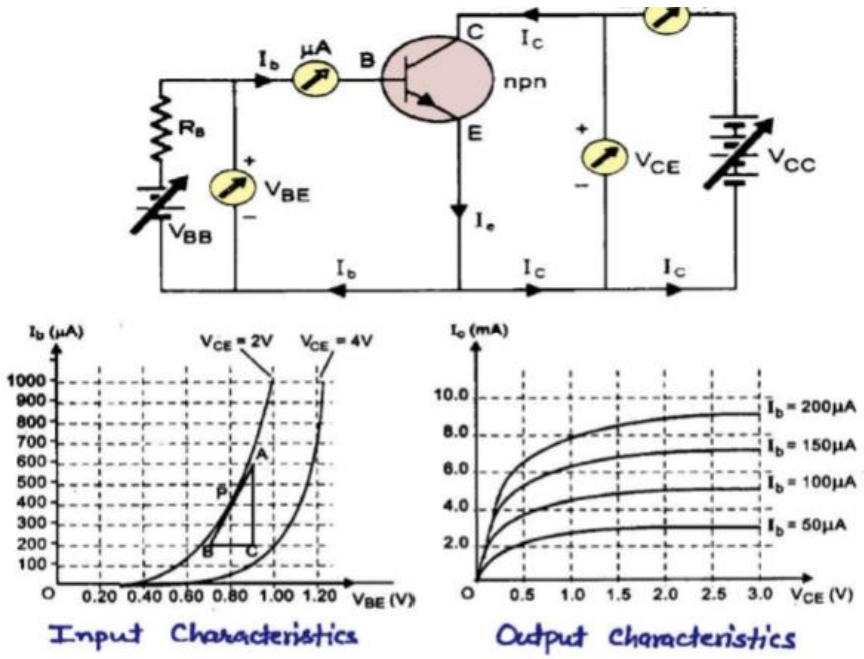
FULL WAVE RECTIFIER



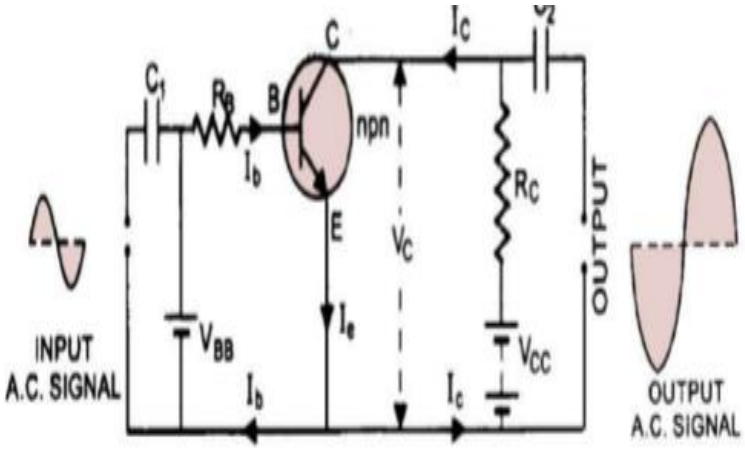
Full ware bridge Rectifier



COMMON EMITTER TRANSISTER CHARACTERISTICS



TRANSISTER AS COMMON EMITTER AMPLIFIER



SUMMARY

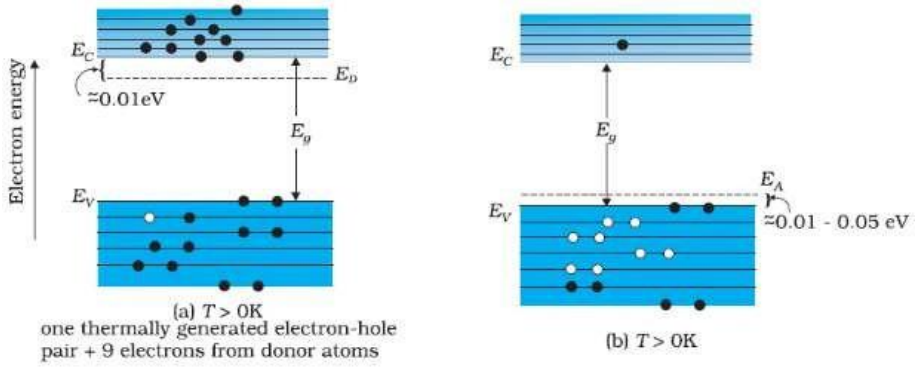
- **Intrinsic Semiconductor:**
  The pure semiconductors in which the electrical conductivity is totally governed by the electrons excited from the valence band to the conduction band and in which no impurity atoms are added to increase their conductivity are called intrinsic semiconductors and their conductivity is called intrinsic conductivity. Electrical conduction in pure semiconductors occurs by means of electron-hole pairs. In an intrinsic semiconductor,

  $$n_e = n_h = n_i$$

  where n_e = the free electron density in conduction band, n_h = the hole density in valence band, and n_i = the intrinsic carrier concentration.
- **Extrinsic Semiconductors:**
  A Semiconductor doped with suitable impurity atoms so as to increase its conductivity is called an extrinsic semiconductor.
- **Types of Extrinsic Semiconductors:**
  Extrinsic semiconductors are of two types
  i) n-type semiconductors
  ii) p-type semiconductors
- **n-type semiconductors:**
  The pentavalent impurity atoms are called donors because they donate electrons to the host crystal and the semiconductor doped with donors is called n-type semiconductor. In n-type semiconductors, electrons are the majority charge carriers and holes are the minority charge carriers. Thus,

  $$n_e >> n_h$$
- **p-type semiconductors:**
  The trivalent impurity atoms are called acceptors because they create holes which can accept electrons from the nearby bonds. A semiconductor doped with acceptor type impurities is called a p-type semiconductor. In p-type semiconductor, holes are the majority carriers and electrons are the minority charge carriers Thus,

  $$n_h >> n_e$$

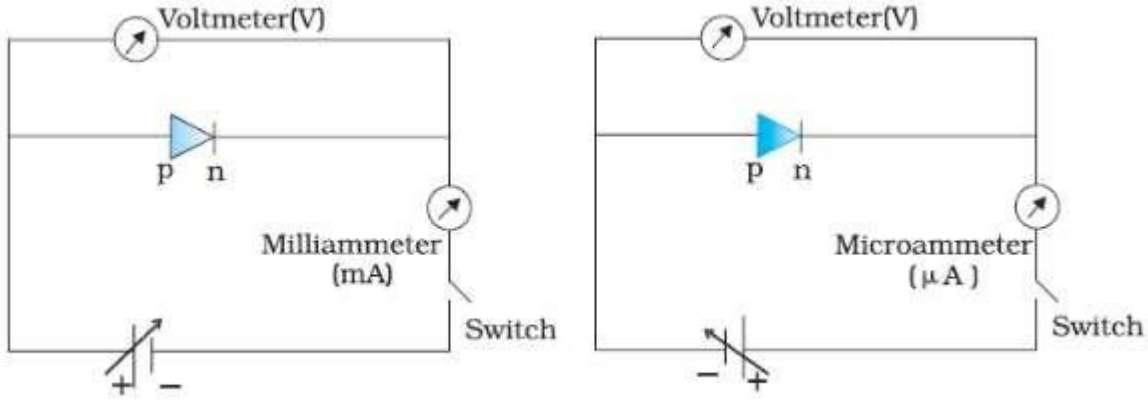


Energy Band Diagram of n-type semiconductor Energy band Diagram of p-type semiconductor

- **Holes:**
  The vacancy or absence of electron in the bond of a covalently bonded crystal is called a hole. A hole serves as a positive charge carrier.
- **Mobility:**
  a) The drift velocity acquired by a charge carrier in a unit electric field is called its electrical mobility and is denoted by μ .
  $$\mu = \frac{V_d}{E}$$
  b) The mobility of an electron in the conduction band is greater than that of the hole (or electron) in the valence band.
- **Electrical conductivity of a Semiconductor:**
  a) If a potential difference V is applied across a conductor of length L and area of cross-section A, then the total current I through it is given by,
  $$I = eA(n_e v_e + n_h v_h)$$
  where n_e and n_h are the electron and hole densities, and v_e and v_h are their drift velocities, respectively.
  b) If μ_h are the electron and hole mobilities, then the conductivity of the semiconductor will be,
  $$\rho = e(n_e \mu_e + n_h \mu_h)$$
  and the resistivity will be,
  $$\rho = \frac{1}{e(n_e \mu_e + n_h \mu_h)}$$
  c) The conductivity of an intrinsic semiconductor increases exponentially with temperature as,
  $$\sigma = \sigma_0 \exp\left(-\frac{E_g}{2k_B T}\right)$$
- **Forward Biasing of a pn-junction:**
  If the positive terminal of a battery is connected to the p-side and the negative terminal to the n-side, then the pn-junction is said to be forward biased. Both electrons and holes

move towards the junction. A current, called forward current, flows across the junction. Thus a pn-junction offers a low resistance when it is forward biased.

- **Reverse Biasing of a pn-junction:**
  If the positive terminal of a battery is connected to the n-side and negative terminal to the p-side, then pn-junction is said to be reverse biased. The majority charge carriers move away from the junction. The potential barrier offers high resistance during the reverse bias. However, due to the minority charge carriers a small current, called reverse or leakage current flows in the opposite direction. Thus junction diode has almost a unidirectional flow of current.



(a) Forward Bias: pn Junction (b) Reverse Bias: pn Junction

- **Action of a transistor:**
  When the emitter-base junction of an npn-transistor is forward biased, the electrons are pushed towards the base. As the base region is very thin and lightly doped, most of the electrons cross over to the reverse biased collector. Since few electrons and holes always recombine in the base region, so the collector current I_c is always slightly less then emitter current I_E.

$$I_E = I_C + I_B$$

  Where I_B is the base current.

- **Three Configurations of a Transistor:**
  A transistor can be used in one of the following three configurations:
  a) Common-base (CB) circuit.
  b) Common-emitter (CE) circuit.
  c) Common-collector (CC) circuit.

- **Current Gains of a Transistor:**
  Usually low current gains are defined:
  a) Common base current amplification factor or ac current gain α :
  It is the ratio of the small change in the collector current to the small change in the emitter current when the collector-base voltage is kept constant.

$$\alpha = \left[\frac{\delta I_C}{\delta I_E}\right]_{V_{CB}=\text{constant}}$$

b) Common emitter current amplification factor or ac current gain β :

It is the ratio of the small change in the collector current to the small change in the base current when the collector emitter voltage is kept constant.

$$\beta = \left[\frac{\delta I_C}{\delta I_B}\right]_{V_{CE}=\text{constant}}$$

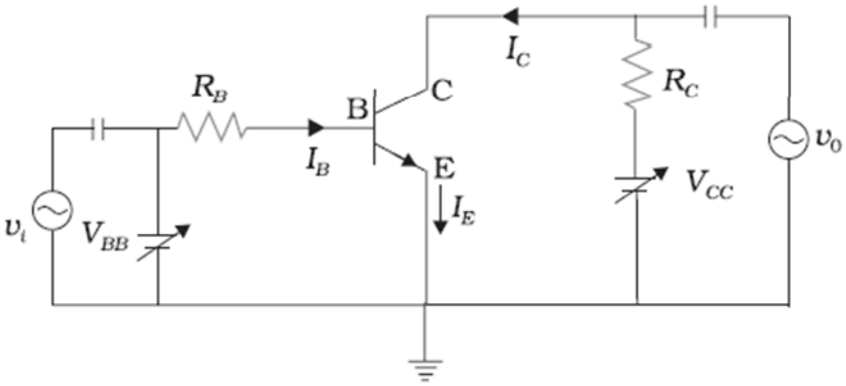
- **Relations between α and β :**

The current gains α and β are related as,

$$\alpha = \frac{\beta}{1+\beta} \quad \text{and} \quad \beta = \frac{\alpha}{1+\alpha}$$

- **Transistor as an amplifier:**

An amplifier is a circuit which is used for increasing the voltage, current or power of alternating form. A transistor can be used as an amplifier.



- **AC Current Gain:**

AC current gain is defined as,

$$\beta_{ac} \text{ or } A_i = \left[\frac{\delta I_C}{\delta I_B}\right]_{V_{CE}=\text{ constant}}$$

- **DC Current Gain:**

DC current gain is defined as,

$$\beta_{dc} = \left[\frac{I_C}{I_B}\right]_{V_{CE}=\text{ constant}}$$

- **Voltage Gain of an Amplifier:**

It is defined as,

$$A_v = \frac{V_0}{V_i} = \frac{\text{A small change in output voltage}}{\text{A small change in input voltage}}$$

$$A_V = \frac{\delta V_{CE}}{\delta V_{BE}}$$

$$A_V = \beta_{ac} \cdot \frac{R_{out}}{R_{in}} = A_i . A_r$$

i.e., Voltage gain = Current gain X Resistance gain

- **Power Gain of an Amplifier:**
  It is defined as,

$$A_p = \frac{\text{Output power}}{\text{Input power}} = \text{current x voltage gain}$$

  or

$$A_p = A_i . A_v = \beta_{ac}^2 . \frac{R_{out}}{R_{in}}$$

- **Logic Gate:**
  A logic gate is a digital circuit that has one or more inputs but only one output. It follows a logical relationship between input and output voltage.
- **Truth Table:**
  This table shows all possible input combination and the corresponding output for a logic gate.
- **Boolean Expression:**
  It is a shorthand method of describing the function of a logic gate in the form of an equation or an expression. It also relates all possible combination of the inputs of a logic gate to the corresponding outputs.
- **Positive and Negative Logic:**
  If in a system, the higher voltage level represents 1 and the lower voltage level represent 0, the system is called a positive logic. If the higher voltage represents 0 and the lower voltage level represents 1, then the system is called a negative logic.
- **OR Gate:**
  An OR gate can have any number of inputs but only one output. It gives higher output (1) if either input A or B or both are high (1), otherwise the output is low (0).

$$A + B = Y$$

  Which is read as 'A or B equals Y'.
- **AND gate:**
  An AND gate can have any number of inputs but only one output. It gives a high output (1) if inputs A and B are both high (1), or else the output is low (0). It is described by the Boolean expression.

$$A . B = Y$$

  Which is read as 'A and B equals Y'.
- **NOT Gate:**
  A NOT gate is the simplest gate, with one input and one output. It gives as high output (1) if the input A is low (0), and vice versa.
  Whatever the input is, the NOT gate inverts it. It is described by the Boolean expression:

$$\bar{A} = Y$$

  Which is read as 'not A equal Y'.

- **NAND (NOT+AND) gate:**
  It is obtained by connecting the output of an AND gate to the input of a NOT gate. Its output is high if both inputs A and B are not high. If is described by the Boolean expression.
  $$\overline{A.B} = Y \text{ or } \overline{AB} = Y$$
  Which is read as 'A and B negated equals Y'.
- **NOR (NOT+OR) Gate:**
  It is obtained by connecting the output of an OR gate to the input of a NOT gate. Its output is high if neither input A nor input B is high. It is described by the Boolean expression.
  $$\overline{A + B} = Y$$
  Which is read as 'A and B negated equals Y'.
- **XOR or Exclusive OR gate.** The XOR gate gives a high output if either input A or B is high but not when both A and B are high or low. It can be obtained by using a combination of two NOT gates, two AND gates and one OR gate. It is described by Boolean expression:
  $$Y = \overline{AB} + \overline{AB}$$
  The XOR gate is also known as difference gate because its output is high when the inputs are different.
- **Integrated Circuits:**
  The concept of fabricating an entire circuit (consisting of many passive components like R and C and active devices like diode and transistor) on a small single block (or chip) of a semiconductor has revolutionized the electronics technology. Such a circuit is known as Integrated Circuit (IC).