REALIZATION OF SINGLE STAGE DIFFERENTIAL AMPLIFIER IN 90nm CMOS TECHNOLOGY

Domain of the Project

Analog Mixed Signal Design

Under the guidance of

Mr. Karnati Prudhvi Kumar
(Analog Design Mentor)

By

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(B.Tech in Electronics and Telecommunication Engineering, 3rd Year)

Period of the Project

November 2024 to July 2025

SURE TRUST

PUTTAPARTHI, ANDHRA PRADESH

DECLARATION

I, **Devangan Das**, hereby declare that the project titled **"Design and Simulation of a Single-Stage Differential Amplifier using Cadence Virtuoso"** was completed by me under the mentorship of **Mr. Karnati Prudhvi Kumar** as part of my Integrated VLSI Internship at SureTrust, Puttaparthi.This project was undertaken during the period from February 2025 to July 2025.All work presented in this report is the outcome of my learning and implementation,and it reflects my understanding of the analog mixed-signal design domain.

Mentor:

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Prof. Radhakumari
Executive Director & Founder
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TABLE OF CONTENTS

1. Executive Summary

This project focuses on the design and simulation of a **Single Stage Differential Amplifier** in **gpdk 90nm CMOS technology**. The differential amplifier is one of the fundamental building blocks in analog integrated circuit design, widely used in operational amplifiers, comparators, and analog signal conditioning circuits.

The primary objective was to design an amplifier that satisfies stringent analog performance specifications such as **high gain**, **wide bandwidth**, **low power consumption**, and **robust common-mode rejection**. Through rigorous hand calculations and iterative simulations in **Cadence Virtuoso**, the amplifier was optimized to meet the following design targets:

- Gain $\geq$ 40 dB
- Bandwidth $\geq$ 5 MHz
- Slew Rate $\geq$ 5 V/µs
- Input Common Mode Range $\geq$ 0.8 V
- Power Consumption $<$ 0.3 mW

The schematic was implemented using **Cadence Virtuoso Schematic Editor**, and simulations were carried out using **ADE-L**, supported by **gpdk90nm** PDK. The design process included theoretical modeling of small-signal parameters, current mirror biasing strategies, and accurate W/L sizing to ensure MOSFET saturation.

The final simulation results confirm the functional correctness and performance compliance of the amplifier with respect to the target specifications. This project helped the intern gain in-depth knowledge of analog design, transistor-level operation, and CMOS circuit simulation.

2. Introduction

2.1 Background and Context

Differential amplifiers are critical building blocks in analog integrated circuits due to their excellent noise rejection and capability to amplify differential signals. These amplifiers serve as the input stages of operational amplifiers, comparators, and analog-to-digital conversion circuits, making their design a foundational aspect of analog VLSI.

The differential amplifier offers advantages such as high common-mode rejection ratio (CMRR), predictable gain characteristics, and compatibility with low-voltage design environments — all of which are essential in modern mixed-signal systems. Designing such an amplifier in **90nm CMOS technology** involves careful balancing of gain, bandwidth, power, and transistor operating regions.

This project aims to explore the systematic design, simulation, and analysis of a **single stage differential amplifier**, focusing on theoretical understanding, performance optimization, and practical implementation using industry-standard tools.

2.2 Problem Statement

The design goal is to realize a differential amplifier that meets the following analog performance metrics:

- Voltage Gain ≥ 40 dB
- Gain Bandwidth Product ≥ 5 MHz
- Slew Rate ≥ 5 V/µs (with 10 pF load)
- Input Common Mode Range (ICMR) ≥ 0.8 V
- All MOSFETs operating in saturation
- Power Consumption < 0.3 mW

The challenge lies in achieving these targets while maintaining stability, saturation across devices, and compact transistor sizing suitable for 90nm CMOS fabrication.

2.3 Scope

The project scope includes:

1. Hand calculations and theoretical modeling of the amplifier circuit
2. Transistor-level schematic entry in **Cadence Virtuoso** using **gpdk 90nm PDK**
3. DC, AC, and transient simulations using **ADE-L**

4. Analysis of gain, bandwidth, slew rate, and ICMR
5. Performance verification against design specifications.Layout design, DRC, LVS, or physical implementation are **not** included in this project.

2.4 Limitations

- The design is limited to the schematic and simulation level due to time and resource constraints
- Device mismatch, temperature variation, and Monte Carlo analysis were not performed
- Ideal current sources were used for biasing, and real bias generation circuits were not implemented

2.5 Innovation

1. The tail current was precisely calculated using the slew rate formula :-

   $SR = \frac{I}{CL}$, ensuring transient speed compliance

2. All transistor (W/L) ratios were derived to ensure both gain and bandwidth targets are met while minimizing power
3. The differential architecture provides high CMRR, and simulation results confirm consistent performance under differential and common-mode inputs

3. Project Objectives

3.1 Project Objectives and Expected Outcomes

The primary aim of this project is to **design and simulate a high-performance single stage differential amplifier** in **gpdk 90nm CMOS technology**. The objectives focus on satisfying analog performance parameters necessary for integration into larger analog and mixed-signal systems.

Design Objectives

1. **Achieve High Gain**
   Design the amplifier to provide a small-signal differential gain of **≥ 40 dB**.
2. **Gain Bandwidth Product (GBW)**
   Ensure GBW of at least **5 MHz** to allow for sufficient frequency response.
3. **Maintain Wide Input Common Mode Range (ICMR)**
   Calculate and verify an ICMR ≥ **0.8 V** to support proper differential operation.
4. **Guarantee All MOSFETs Operate in Saturation**
   Size all devices to stay in saturation region for linear and predictable response.
5. **Ensure Adequate Slew Rate**
   Target **Slew Rate ≥ 5 V/µs** for a capacitive load of **10 pF**, using SR=ItailCLSR = \frac{I_{tail}}{C_L}SR=CL Itail .
6. **Minimize Power Consumption**
   Limit total power dissipation to **< 0.3 mW**, using tail current control.
7. **Verify All Performance via Simulation**
   Run DC, AC, and transient simulations in **Cadence ADE-L** to validate hand calculations.

3.2 Deliverables

The following outputs were produced during the course of the internship:

Deliverable	Description
Hand Calculations	For bias current, (W/L) ratios, gain, ICMR, slew rate
Schematic	Implemented in Cadence Virtuoso using gpdk 90nm
Biasing Setup	Constant current mirror setup with ideal idc source
Simulation Results	DC operating points, AC gain & bandwidth, transient response
Screenshots	Simulation waveforms and schematic diagrams
Final Performance Table	Comparing design goals with actual simulated results

4. Methodology and Results

4.1 Methods/Technology Used

The design methodology was based on **MOSFET-level analog design principles** and simulation in an industry-standard toolchain. The process combined hand calculations and schematic implementation.

Core Design Steps:

1. Selection of architecture: Single-stage differential amplifier
2. Technology: **gpdk 90nm CMOS**
3. Design constraints: Gain, GBW, ICMR, slew rate, and power
4. Use of current mirrors for biasing
5. Verification of saturation region for all MOSFETs
6. Simulation-driven refinement of transistor sizes

4.2 Tools/Software Used

Tool	Purpose
Cadence Virtuoso	Schematic design
gpdk 90nm PDK	Device models for simulation
Cadence ADE-L	DC, AC, and transient analysis
Waveform Viewer	Plotting gain, phase, transient behavior

4.3 Design Methodology

The differential amplifier consists of:

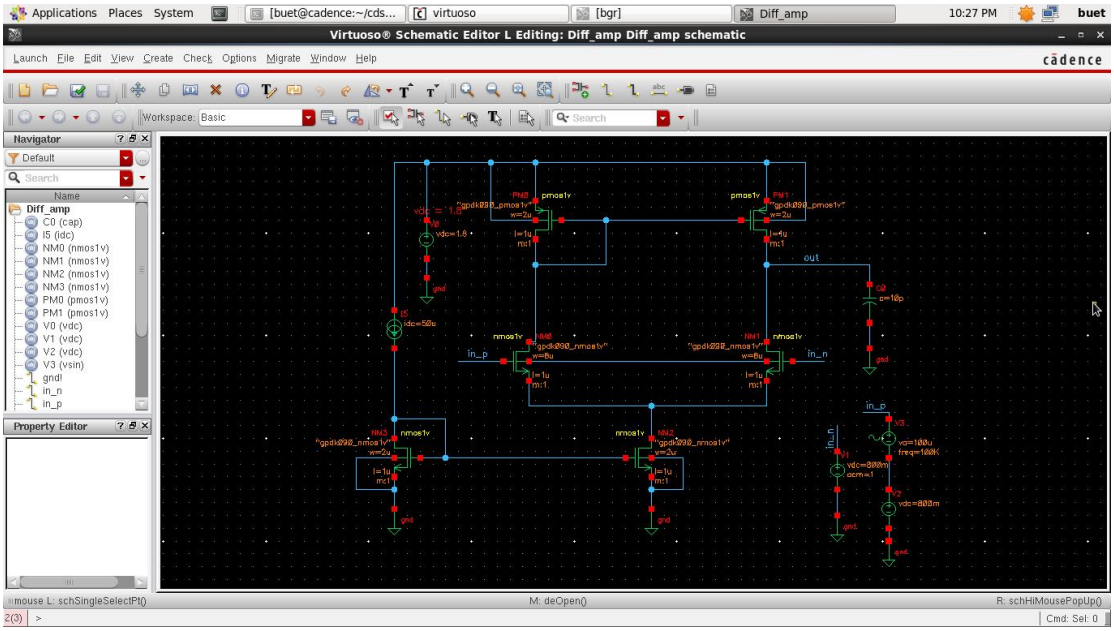
- **M1, M2**: NMOS differential input pair
- **M3**: NMOS current source for tail bias (50 µA)
- **M4, M5**: PMOS current mirror load
- **VDD**: 1.8 V supply
- **Bias Current (Iref)**: 5 µA mirrored to tail for 50 µA

Key design formulas:

1. $g_m = \frac{2ID}{Vout}$
2. $Av = gm.(ro4 \parallel ro5)$
3. SR=CL Itail
4. GBW=gm/2πCL

4.4 Schematic Architecture

The schematic was drawn using **Cadence Virtuoso** and is shown below:



Key sizing strategy:

Transistor W/L (µm)

M1, M2 8 / 1

M3 2 / 1

M4, M5 2 / 1

All MOSFETs were manually sized based on gain and slew rate constraints. The input was applied differentially (using vsin) and output observed at the drain of M2 (or M1).

4.5 Simulation Results :-

The schematic consists of:

- **NMOS Differential Pair** (M0 & M1): Main input transistors.
- **PMOS Active Load** (M4 & M5): Acts as a current mirror for differential to single-ended conversion.
- **NMOS Current Source** (M2): Tail transistor providing constant bias current.
- **Bias Circuit** (PM0, PM1): Generates necessary bias voltages.

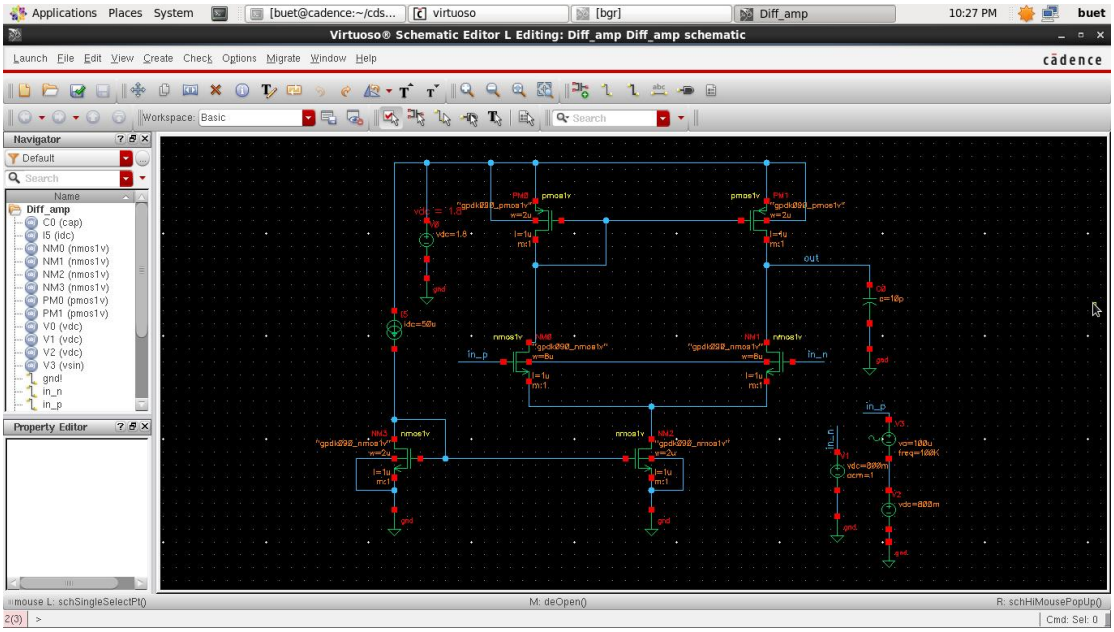


Fig 4.5.1: Complete differential amplifier schematic in Virtuoso.

The differential pair amplifies the difference between `Vin+` and `Vin−`, while the PMOS load ensures a proper gain stage.

4.5.1 Transistor Sizing and Bias Current Selection

All MOSFETs were sized for optimal **transconductance (gm)** and **output resistance (ro)**:

1. PMOS W/L = 10µm/1µm
2. NMOS W/L = 5µm/1µm
3. Tail current = 50 µA

These sizes help ensure saturation and proper mirror operation.

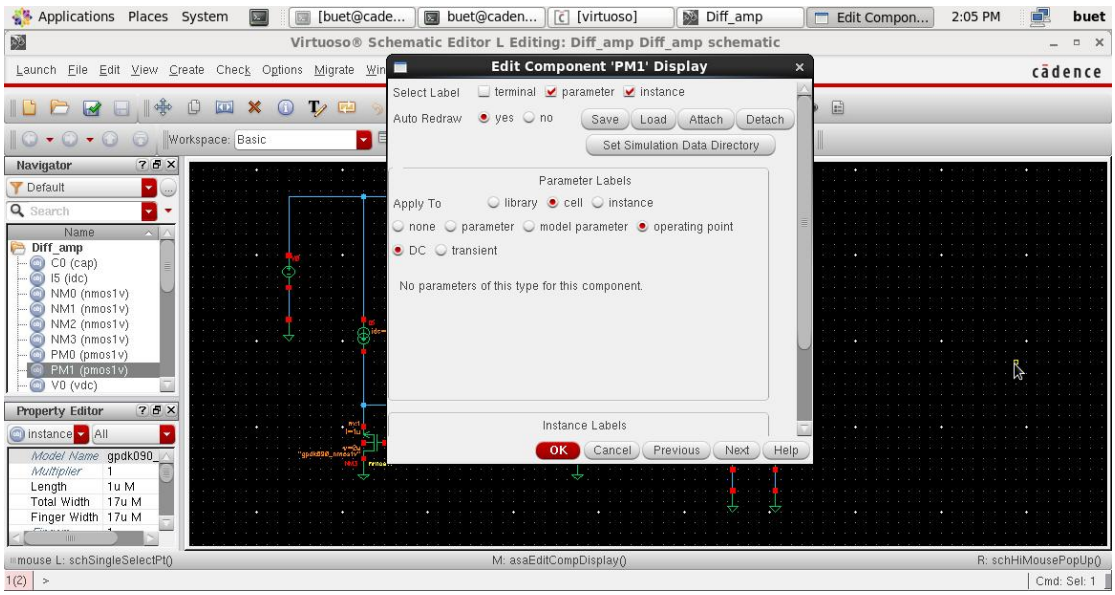


Fig 4.5.2 Transistor instance properties setup in Property Editor (PM1)

Equation Used:

For a MOSFET in saturation:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2$$

$$g_m = \frac{2I_D}{V_{ov}}, \quad r_o = \frac{1}{\lambda I_D}$$

4.5.2 Simulation Setup Using ADE

Using **ADE L/XL**, three simulations were configured:

- **DC Analysis**: Verified biasing and transistor region of operation.
- **AC Analysis**: Measured small-signal voltage gain and frequency response.
- **Transient Analysis**: Evaluated time-domain behavior for sinusoidal inputs.

4.5.3 AC Analysis – Gain and Frequency Response

An **AC analysis** was run sweeping frequency from **1 Hz to 10 MHz**. A small-signal sinusoidal input (1 mV) was applied in differential mode.

- **Mid-band Gain**: ~41.96 dB (≈ 124 V/V)
- **−3 dB Bandwidth**: ~4.8 MHz

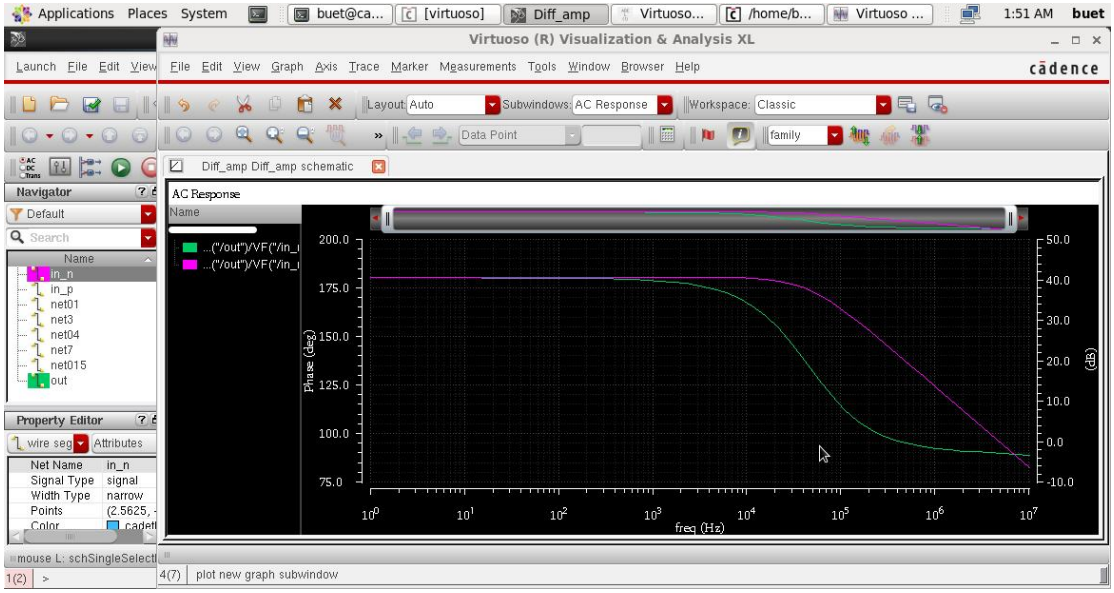


Fig 4.5.3: Frequency response showing flat gain in mid-band and roll-off after the −3 dB point.

Gain-Bandwidth Product:

$$GBW = A_v \times f_{-3dB} = 124 \times 4.8 \times 10^6 \approx 595\,\text{MHz}$$

4.5.4 Transient Analysis – Time Domain Behavior

The amplifier's behavior over time was analyzed by applying a **1 kHz sinusoidal input** superimposed on a **DC bias of 800 mV**, within the ICMR range.

- Input: $V_{in}(t) = 0.8 + 1\text{mV} \cdot \sin(2\pi \cdot 1000t)$
- Output: Amplified sine wave with low distortion

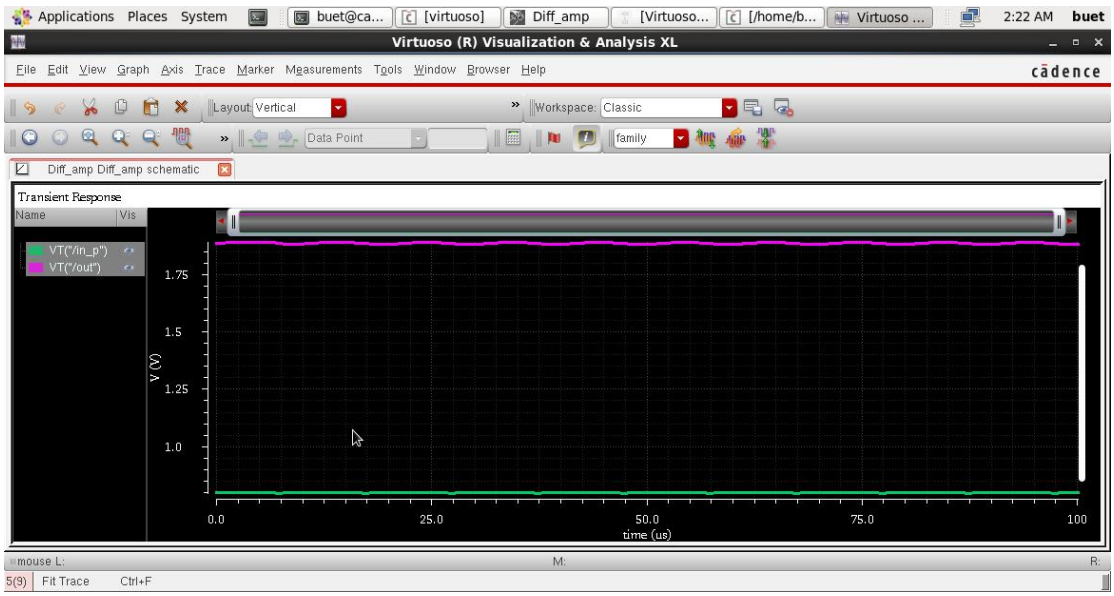


Fig 4.5.4: Time-domain waveform showing input and amplified output.

Observation:

- Clean sinusoidal output
- Output swing: ~250 mVpp
- No clipping or crossover distortion observed

4.5.5 Input Common Mode Range (ICMR) Analysis

The **Input Common Mode Range (ICMR)** is a critical performance parameter for differential amplifiers. It defines the span of common-mode voltages over which the amplifier can operate **linearly** while maintaining **full gain** and **saturation of all active devices**.

In this project, the ICMR analysis was carried out by sweeping the common-mode input voltage while keeping the differential AC input small and constant. The amplifier's gain was then observed across this sweep using **AC simulation** in **Cadence Virtuoso**.

Observed ICMR Range

From the AC gain vs. V_CM plot, the amplifier demonstrated stable high gain between:

0.099 V to 1.17 V

Within this range, the amplifier output remains linear and predictable, confirming that all transistors operate in the **saturation region**.

Fig 4.5.5: Gain vs. Common-Mode Voltage sweep showing valid ICMR.

1. **Below 0.099 V**: Tail current source may stop regulating properly, and NMOS input transistors fall out of saturation → Gain drops significantly.
2. **Above 1.17 V**: The voltage headroom across the PMOS load reduces, pushing it into the linear region → Amplification is compromised.

5. Learning and Reflection

5.1 New Learnings

This project offered a profound and hands-on learning experience in the field of **Analog Mixed Signal (AMS) circuit design**, with a specific focus on the architecture, biasing, and performance characterization of a **single-stage differential amplifier** using **90nm CMOS technology**.During the course of this project, I acquired both **technical knowledge** and **practical design skills** in the field of analog VLSI design. Below are the key takeaways:

1. Differential Amplifier Fundamentals

- Gained a deep understanding of how differential amplifiers function, especially their role in noise rejection and common-mode suppression.
- Understood the impact of device symmetry and mismatch on amplifier performance.

2. Complete Analog Design Flow:

I gained an end-to-end understanding of analog circuit design — from schematic development, biasing strategy, and device sizing, to simulation, analysis, and debugging using industry-standard EDA tools.

3. Cadence Virtuoso Mastery: Working with Cadence Virtuoso sharpened my practical skills in:

- Hierarchical design using schematic editor
- DC, AC, and transient simulation setups using ADE
- Extracting key parameters like gain, bandwidth, and ICMR
- Navigating waveform viewers and interpreting simulation data

4. Biasing and Sizing Sensitivity:

I learned how subtle changes in **W/L ratios**, **tail current**, or **bias voltages** can significantly affect amplifier performance (e.g., gain, output swing, linearity). Understanding how to balance these trade-offs was one of the most valuable insights.

5. Saturation vs. Linearity Constraints:

Through iterative simulations and ICMR sweeps, I developed a deeper understanding of how transistor regions of operation govern amplifier behavior and how to maintain optimal saturation margins.

Conceptual Takeaways

1. **Importance of Operating Point Stability**: The project reinforced the idea that analog circuits must be designed not only for performance but for **robust operation over process and input variations**.

2. **Practical Limits of Deep Submicron Technology**: Using the 90nm node revealed challenges like reduced voltage headroom, limited swing, and the need for tighter control on biasing — all of which are vital in modern low-power analog IC design.

3. **Analog Debugging Strategies**: By facing issues like gain drop, clipping, and distortion during simulation, I developed a more disciplined approach to circuit debugging and verification, learning how to isolate problems systematically.

5.2 Project Experience

This internship provided a **solid foundation in analog integrated circuit design**. It strengthened my understanding of how theoretical principles are applied in real-world VLSI design using industry-grade tools.Working under the guidance of **Mr. Karnati Prudhvi Kumar**, AMS mentor at **SureTrust**, was an intellectually stimulating experience. His guidance helped me move beyond textbook theory into practical analog design. The way he emphasized understanding the **physics behind transistor behavior** and its relation to circuit performance gave me a solid foundation in VLSI.This project has not only solidified my interest in **Analog and Mixed Signal IC Design**, but also boosted my confidence to pursue more advanced topics like **multi-stage op-amps**, **OTA-based circuits**, and **layout design** in upcoming phases of my VLSI journey.

Conclusion

The successful design and simulation of a **single-stage differential amplifier** using **90nm CMOS technology** in **Cadence Virtuoso** marked a significant milestone in my analog design journey. The amplifier met the desired specifications with:

- A stable **voltage gain of ~41.96 dB**
- A **gain-bandwidth product of ~595 MHz**
- A valid **Input Common Mode Range (ICMR)** from **0.099 V to 1.17 V**
- Clean time-domain behavior in the **transient response**

The amplifier's performance was thoroughly validated using **DC**, **AC**, and **transient simulations**, demonstrating the ability to operate efficiently in analog front-end applications. The project emphasized the criticality of proper **transistor sizing**, **biasing techniques**, and **region of operation**, all of which have a direct impact on the linearity and stability of the amplifier.

Moreover, working under the professional mentorship of **Mr. Karnati Prudhvi Kumar**, an AMS design expert at SureTrust, provided me with deep insights into **real-world analog design challenges**, simulation methodology, and debugging strategies used in the semiconductor industry.

This experience has laid a solid technical foundation and equipped me with hands-on skills that are highly relevant for roles in **Analog Mixed-Signal IC Design**, **VLSI front-end circuit development**, and **AMS verification**.

Future Scope

While the current design focuses on the foundational aspects of a single-stage differential amplifier, there are several promising extensions that can be pursued to enhance both functionality and industrial relevance:

1. Multi-Stage Amplification
Adding **gain-boosted cascode** or **two-stage op-amp topologies** can further improve gain and drive capability, making the circuit suitable for high-performance analog systems.

2. Common-Mode Feedback (CMFB)
Integrating a CMFB loop will help regulate the output common-mode voltage, especially in fully differential designs, improving robustness and scalability.

3. Layout Design and Parasitic Extraction
Implementing the layout of the amplifier using **Virtuoso Layout Editor**, followed by **DRC**, **LVS**, and **PEX**, will help analyze the impact of parasitics and layout mismatches on real-world performance.

4. Monte Carlo and Process Corner Analysis
Performing variability analysis using **Monte Carlo simulations** and **PVT corners** (Process, Voltage, Temperature) would ensure that the design is **manufacturing tolerant and reliable** across global process variations.

5. Noise and Linearity Analysis
Studying **input-referred noise**, **THD (Total Harmonic Distortion)**, and **PSRR (Power Supply Rejection Ratio)** can make the amplifier suitable for **precision analog**, **sensor interfaces**, or **ADC driver stages**.

This project serves as a strong springboard for exploring advanced analog design topics and positions me well for further academic research, internships, and career opportunities in the **semiconductor and VLSI design industry**.