GNANAPRABHU A

SI/PI ANALYSIS ENGINEER

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Permanent Address:
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Personal Data:

Date of Birth	: 20/11/1993
Sex	: Male
Nationality	: Indian
Marital Status	: Un Married
Religion	: Hindu

Languages Known:

Speak: English, Tamil

Write : English, Tamil

Career Objective:

Aim to be associated with a progressive organization that gives me scopes and update my knowledge and skills in accordance with the latest trends and to be part of a team that dynamically works towards growth of the organization effectively and efficiently and gain satisfaction thereof.

Educational Qualifications:

- **BE in Electrical & Electronics Engineering (73%), 2015**, from Park College of Engineering and Technology, Tamilnadu. Anna University Affiliated.
- **Higher Secondary Education (86.3%) , 2011**
  PSG Sarvajana Higher Secondary school, Tamilnadu.
- **Secondary Education (94%), 2009**
  Corporation High school, Tamilnadu.

Area of Expertise:

- Package-Die & System level Power Integrity Analysis
- Board level Power Integrity & Thermal Analysis
- Board/package layout review & Ondie cap suggestion/FIVR compensation to meet the best system performance

Work Experience:

- Design/Analysis engineer
  ATE board Design & Power Integrity analysis
  Duration: Feb 2016 – Feb 2018 (2 years)
  Company: Cube Circuits pvt ltd, Coimbatore.

- Design/Analysis engineer
  Power Integrity & Thermal Analysis
  Duration: Mar 2018 – Oct 2020 (2.7 years)
  Company: Sienna Ecad Technologies pvt ltd, Bangalore.

- Graphics Hardware engineer
  Power Integrity analysis
  Duration: Nov 2020 – present
  Company: Intel Technology India pvt ltd, Bangalore.

Job Profile:

- Modified RF, mixed signal load boards & probe card designs for analysis purpose.
- Conversant in PDN topology study, decoupling capacitors study, PDN DC/AC and Transient Analysis.
- Reviewing layout in terms of SI/PI Products development and better quality of deliverables.

- Highly skilled in power supply noise reduction techniques.
- Efficient in providing assistance for package & board layout copper plane, via connectivity, stack up, decoupling capacitor placement optimizations.
- Meticulous knowledge on suggesting decoupling capacitors based on the project requirements.
- Conversant with the various methods/ways of reducing board and component temperatures.
- Worked on PI-Thermal co-simulations.
- Experienced in hybrid and 3D solvers.
- Good knowledge on pre and post layout simulations.
- Worked on S-parameter and Spice models.

Tools Expertise:

- Hyperlynx, Sigrity, ADS, Ansys, HSpice, Cadence Vituoso.

Major Projects:

- **PROJECT-1**

Project : Ponte Vecchio (PVC) -Intel

Description and Responsibility :

Providing proper compensation scheme for Ondie voltage regulators(FIVR) to ensure optimum system performance in AC and transient analysis on different domains - VccBASE(150A), VccEU(102A), VccHBM, MDFI

- **PROJECT-2**

Project : eFPGA package

Client : Achronix semiconductor

Layers : 18

Description and Responsibility :

This package has SERDES 112G, DDR4, GDDR6 interfaces with COREVDD(150A), SERDES(40A), VCC(40A), GDDR6_VDDIO(36A) high current power supplies. Power supply noise is maintained within the specifications for all power supplies including GPIO, CLKIO, FCU vddio powers by doing layout reviews, suggesting low ESR, ESL caps, On-Die capacitance & resistance additions, Optimizing decoupling capacitor placements on package, Ball map reviews & optimizations.

- **PROJECT-3**

Project : CB,MEP boards (System level PDN Analysis)

Client : Achronix semiconductor

Layers : 20

Description and Responsibility :

The characteristics of developed FPGA package are evaluated in these test boards. Board level Impedance and Transient noise analysis are done for GDDR6, SERDES, DDR4, VCC, COREVDD, GPIO, CLKIO, FCUIO power supplies. The power supply specifications are met by decoupling capacitor optimizations and layout reviews. Then the board models are probed with the package & die models to meet the requirements at die side. PDN optimizations done with realistic and step current profiles for each power rail.

- **PROJECT-4**

Project : 5G_RRH_card

Client : Indian Institute of Technology (Madras,Kanpur)

Layers : 18

Description and Responsibility :

This card has 100G lines with high current of 36A.Decoupling capacitors are added to maintain the target impedance with 1% of ripple for 0.85V power rail. Copper shapes of 36A current and other low current power net shapes are modified and added to achieve the voltage drop within 1%. Worked on signal S-parameters extractions.

- **PROJECT-5**

Project : Gen7_COMex_card

Client : Bharat Electronics Ltd

Layers : 26

Description and Responsibility :

In this card, the Intel FPGA is powered by 68A of current with low voltage of 1V.The ripple percentage required is 1%.We maintained a low target impedance upto 125 Mhz.The existing decoupling capacitor networks are optimized to keep the PDN impedance low. The copper shapes, blind and buried vias, source to load distances are optimized to maintain the voltage drop within 1%. Worked on signal S-parameter extractions.

Personal Qualities:

- Positive Approach
- Good Inter-personal Relations
- Ability and willingness to learn new technology and constantly update my knowledge
- Flexibility and adaptability

Declaration:

I consider myself familiar with Engineering aspects and I am confident in my abilities to work in a team and as an individual. I hereby declare that the information provided is true to the best of my knowledge.

Yours faithfully
Gnanaprabhu A