Naveen Kumar
Associate III Validation Engineer

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CAREER OBJECTIVE:

Seeking a position in an organization which offers an opportunity to learn further, achieve, grow my knowledge and experience in order to achieve organization's goal, and to grow with the organization.

WORK EXPERIENCE:

Organization-II: Lancesoft India PVT LTD.
Client : Dell Technologies
Designation : Software Test Engineer-2
Duration : JAN-17 2022 to Till Date

PROJECT – I

Project: OpenManage Enterprise
Duration: MAY-2022 To Till Date
Datacenter Servers: Power Edge 11G, 12G, 13G, 14G, 15G, 16G, MX7000 Chassis, MX5000s & M1000E Chassis
Ethernet Board Type: NIC and SVB Board.
Storage Protocol: Ethernet, iSCSi, FCoE & Fiber Chanel
Non-Dell Server Platform's: HP, Supermicro & Lenovo
API Testing: Swagger & TRALEND API.
Tools: QTEST, Putty, JIRA, MIB Browser, CCProxy, Nmap, SYSLog Watcher , FSD, Redfish, WSMAN & HP ilo.
Network Protocols: VLAN,IGMP,SNMP,TCP,UDP, RIP, OSPF & MPLS
Languages: C++ & Python
OS: Windows-12,16,19 & 22, Linux, Fedora, ESXI.
Role: Software Test Engineer-2 IT
Team Size: 24

OpenManage Enterprise systems management console facilitates business growth, improves IT productivity and enhances customer service. OpenManage Enterprise is a simple-to-use, one-to-many systems management console. It cost-effectively facilitates comprehensive lifecycle management for PowerEdge servers in one console. Deploy as a secure virtual appliance Intuitive dashboard and elastic search engine One to many intelligent automations with user defined policy, template, and baseline Comprehensive RESTful API enables customizable automation and solution integration Scope Based Access Control (SBAC) allows administrators to limit users to specific device groups.

PROFESSIONAL HEIGHLIGHTS:

- Professional 4+ Years of Experience in Dell & Intel SOC Validation, firmware validation, BIOS Validation,Platform Validation, Regression, IEEE Testing, Software Validation and Automation Execution.
- Hands on Experience in storage Functional Testing, and Familiar with NVME, SSD, HDD, RAID, PCIE SSD, M.2 SSD's and 3D NAND SSD's, USB 3.0, USB2.0, PCIE GEN3, PCIE GEN4, JBOF HBA.
- Involving test case content develop and review test case flow understanding.
- Familiar with Pre and Post silicon Validation/Verification, Platform Validation BKC Release's.
- Hands on Experience in Intel server boards, Jumper settings, Knobs, Hardware I/0 peripheral

connection's, BIOS boot flows.

- Performed Regression Testing on latest builds and verification of fixed issues against stable builds.
- Responsible for Execution of Test cases for assigned modules and defect verification.
- Tested compliance policies that include OS level, Device level security checklists.
- Testing effects on the modules at different installation, Uninstalls and Upgrades.
- Participated in Feature Team Meetings for better understanding of the functionality; involved in Tech-talks and Brown bag sessions within the team to share the knowledge.
- Hands on experience network protocols in Linux & Windows 7, 8 & 10 OS.
- Familiar with Intel SV & server platform's (manual testing and debugging).
- Hands on Experience diff Ethernet speeds 10G, 25, 50, and 100G feature test cases for VLAN, interface managers. Responsible for Functionality Testing and Identifying Defects.
- Designing test topology and test strategy, participating in internal reviews for other features
- Recreating the customer faced defects.
- Hands on Experience in regression, smoke sanity testing, debug the issues, Test Case analyze and Encounter the issues.
- Knowledge sharing with across the Team Members
- Performance driven Engineer with experience in Firmware Validation, Bios Validation, and Automation Execution.
- Knowledge on Firmware, BIOS Boot steps & Board bring-up.
- Testing assigned modules functionality under different operating systems ESXI VM WARE OS, Linux & Windows 7, 8 & 10 Features.
- Familiar with Intel Sever platform's H/W Testing and debugging tools
- Regular update regarding my assigned tasks to respective Team Manager through Daily Status report.

PROJECT -I: OPEN MANAGE ENTERPRISE

Organization-I : UST Global
Client : Intel Technologies India PVT LTD.
Designation : Associate III Semiconductor Product Validation Engineer
Time period : May-07 2018 to JAN-06-2021

PROJECT -I: CARLSVILLE & COLUMBIAVILLE

Project: Carlsville 40G & Columbiaville 100GEthernet Card's.
Duration: MAY-2018 To JULY-2019
Silicon: Small Die & Big Die
Ethernet Board Type: NIC and SVB Board.
Multi Speed: 10G, 25G, 40G, 50G, 80G, And 100G.
GEN IV Server Platform's: DELL, HP, TYAN, Supermicro, Sawtooth
IEE Testing Platform's: LECROY GEN4, KEYSIGHT GEN4 & Jammer.
Interoperability Testing: PCI SIG 3.0
Framework: Denver
Tools: Dediprog, NVM, LANCONF, BOBCAT, MAGLAN, PythonSV.
OS: Windows OS(WIN Server 7, 8)64b & 32b, Linux Fedora 64b.
Role: Associate Validation Engineer
Team Size: 8

Carlsville and Colubiaville Gen IV Card's which supports multi speeds on external server platforms, this stage is conducted to search for showstoppers and fatal failures (BSOD/Kernel panic with basic functionality, no PCIe Link, Link parameters are not correlating to expected, etc.) across various platform configurations. During this stage all slots of all available platforms are populated, aiming to fully populate a whole platform at a timed Basic testing, as the name suggests, targeted to test the basic functionality of the PCIe cluster. Basic testing is the core testing of PCIe post-si validation. Basic tests will be marked as Basic in their description. Advanced testing targeted to test advanced features and complicated scenarios. Many tests in this section are taken from the basic section, but coupled to advanced setup (Jammer), or implementing advanced techniques (data integrity).

ROLES & RESPONSIBILITIES :

- Test Bed preparation as per configuration for Test Case Execution.
- Upgrade the Denver framework and Tools to perform the Interoperability Testing on all severs platforms.
- Hands on Experience in BIOS fetching using Dediprog tool (ROM file flash IFWI/NVM Firmware).
- Feature Testing 10G, 25G and 100G Speed's.
- Hands on Experience Basic functionality Sanity and BAT, Manual, Regression and Automation regression on MNG Team, NVM Team, FRC Team, PCIe Team.
- Validating the Tests in Different device states (D0, D3hot).
- Bring-Up the setup for DR State and run the tests in Dr State (Disaster recovery).
- Validating Manually by using NCSI_WS tool for LAN 2 BMC Traffic, Reading CSR Value, Aen's Link status change, Driver status change etc.
- Test Case Execution, Bug filing, tracking, debugging and Issue's Reporting to client on daily basis. Finding the root cause of the defects from clients.

PROJECT- II: DATA CENTER GROUP SD SV INTEL SERVERS SNOWRIDGE-COLUBIAPARK, ICXD-HCC, ICXD-LCC (SAN/LAN)

Client : Intel
Protocols : VLAN, L3 DPDK, L2DPDK, QAT, CPK, ICE, RDMA, Hyper-V, DCG LAN, ROCe.
Storage : SATA, HDD/SSD, NVME, PCIE, OPTANE NVME, 3D NAND, M.2 PCIE SSD & RAID
Network : Link Speeds of 10G, 25G, 50G, 80G and 100G, NVMeoF, KVM Packet Transefer, Hyper-V, TCP, UDP, VF and PF.
PCIE : Enumeration, Hot plug/Un-plug, Bifurcation x8, x16, x4x4x8, Link Training, Resets
Processor : Stress, DC Cycles, Multi/Hyper Threading, Thermal state's and power states.
Memory : DDR4, DDR5, RDIMM, UDIMM,
USB : Front/Rear Panel, Hub, Performance Data, XHCI Enumeration, Benchmarking, TX Reliability, Backward comp Bulk Transfer Reliability.
Virtualization : Hyper-V, NIC Teaming, UEFI Boot, TPM, TXT, BMC for Shutdown/Reset/Power ON/OFF, Pass Through Network, PCIe Storage, USB Pass Through
Tools : Iperf3, Bit Runner, Lanconf, Dediprog, Maglan, ILVSS/IWVSS, SocWatch, Prime95, Intel MLC(Memory Latency Checker), Memtest, BMC.
OS : Linux, Windows, ESXI 6.7(VM WARE OS).
Role : Associate III Semiconductor Product Validation Engineer.
Team Size 12
Duration : August-2019 to Till Date.

Intel® Ethernet 800 Network Adapters (up to 100GbE)

100Gb Intel Ethernet 800 Series Network Adapters help reduce complexity for port-constrained network environments. The Ethernet Port Configuration Tool (EPCT) enables physical port configurations to be changed quickly, and as often as needed. Dive into this infographic of the Ethernet Port Configuration Tool (EPCT), available on 100Gb Intel® Ethernet 800 Series Network Adapters. Learn key features and benefits of this versatile solution.

As data growth acclerates and demanding new workloads become mission critical, our customers need their networks to work harder. With Intel® Programmable Ethernet Switch Products, you can create ultrafast networks that are fully customized to your needs. This portfolio eliminates bottlenecks and can transform even the largest data center into a focused, balanced, and optimized high-performance computer unto itself.

ROLES & RESPONSIBILITY'S:

- Intel Ethernet NIC Validating Stress, Compatibility, Regression and Basic Acceptance Test.
- IFWI image flash/update by Dediprog, Maglan and Bobcat tool
- Hands on Experience Nic card validation using NVM, IFWI and Qualified Denver.
- Validating Stress test, Compatibility test, Regression test and BAT (Smoke test).
- Flashing firmware by using DediProg or Bobcat tool.
- Provide hands-on assistance to Integration & automation team, consultation, reviews and technical guidance to the team as required. Client interaction and issue resolution.
- Revamping test cases to reduce the test execution time.
- Replicating the Customer Issues (Hardware & software) on all Intel platforms and signal integrity.
- Sharing daily and weekly status reports to the project stake holders.
- Familiar with Raising and Tracking Bugs using HSD (High Speed Database) Intel Platform.
- Validating D0-State (Fully powered on), D3hot-State (Powered on but the data will flow on only PCI bus lanes) and Dr-State (Dut in in shutdown mode, It will work on only some Aux Power supply).
- Involved in Platform Validation, triaging and providing isolation data.
- Hands on Experience various low power states S5 or Dr (Shutdown) functional Test.
- Validating user level features, functions and applications in Linux operating system.
- Preparation of Test cases, Test execution, Bug filing, tracking, debugging and Reports.
- Involved in rising/closing defects, executing test cases and creating various dashboard for status purpose.
- Develops pre-Silicon functional validation tests to verify system will meet design requirements.

TOOLS:

NCSI-Work-Shop, PythonSV, PCIe Lane Margin, Iperf3, Bit Runner, Lanconf, Dediprog, Maglan, ILVSS/IWVSS, SocWatch, Prime95, Intel MLC(Memory Latency Checker), Memtest, BMC Tools which all are Intel Proprietery.

EDUCATION QUALIFICATION

- ✓ B.Tech (Bachelor of Technology)in Computer Science And Engineering from JNTU Hyderabad 2015.
- ✓ Intermediate from AKVR JR college affiliated to Board of Intermediate in 2011.
- ✓ SSC from Board of Secondary Education Andhra Pradesh Hyderabad in 2009.

PERSONAL DETAILS

Languages known: English, Kannada & Telugu.
Address: # Ashwath Nagara,Marathalli,Bangalore 560032

DECLARATION

I hereby confirm that the information stated above is true and complete to the best of my knowledge.

Place: BENGALORE **Naveen Kumar**
Date: **(Signature)**