RESUME

SIVA RAMA KRISHNA

Bengaluru - 560048.

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+91-96200 52688.

Professional Summary:

- **5.2 years** of relevant experience in **post silicon** functional validation at IP level for SOC.
- Presently working with ANVHAYA Technical Solutions India Pvt Ltd, Bengaluru as a Validation Engineer, detail as follows.

Work Experience Highlights:

- Work Experience on **Post Silicon Validation** of various subsystems **IP'S** of **SOCs**.
- Experience in developing and automation of test plan and test cases for validation of IP's.
- Involved in **C** based content development for during post silicon validation and Embedded Development.
- Experience in usage of IDE like **Keil vision** till v5.O, **Notepad++.**
- Experience in usage of Debugging tools like JTAG, Trace 32, GDB debugger.
- Experience in usage of Bug tracking and reporting tool like JIRA.
- Experience on **32-bit** Microcontrollers and microprocessors ARM based SOCs.
- Extensively used version controller tools: **GIT**.
- Hands on Experience with tools like **Oscilloscope** and **Logic Analyser**.
- Worked on validation of USB 3.0, USB 2.0, I2C, SPI and UART.
- Worked on Windows and Linux Operating systems.
- Good understanding of Board level Hardware Schematics.
- Good at Human Machine Interface (HMI) programming.
- Actively interacted with Lab technician to rework according to my IP's.
- Raising the tickets to issues bugs and tracking them till they get resolved.
- Analyzing the test log for the test case failure and also verifying and modifying register dump, memory dump, ip dump, and scan dump.
- Actively interacted with cross functional teams to resolve issues thoroughly.
- Experience in Make tool and compilation process.
- Experience in Agile Methodology and Scrum

Technical Skills:

Programming : C and Embedded C

Languages

Low speed protocols : I2C, SPI and UART

High speed protocols : USB

Operating Systems : Windows, Linux

IDE : Cross Compiler IDE - Keil μVision till v5.0, Eclipse IDE

Tools : JTAG, TRACE32, DSO, Logical Analyzer, Notepad ++, Lauterbach,

DMM, and Beyond Compare

Version Control Tool : GIT

Hardware interfacing : EEPROM, 2*16-character LCD, LEDs, 7-Segment LED Display, Push

Button, 4*4 Matrix keypad, RS-232

Career Path:

Project #4 : Validation of USB 2.0Designation : Validation Engineer

Roles and Responsibilities:

• Going through IP specifications.

- Identifying the features to be validated.
- Giving presentations to the team members about IP.
- Understanding and identifying the work point, VF relationship of IP.
- Extensively used the interfaces on SUT using JTAG.
- Debugging the failure test cases and finding the root cause independently.
- Worked on test plan development, test case script development.

Features Validated:

- Validated different data transform modes like LS/FS/HS with Isochronous, Bulk, Interrupt and Control transfers.
- Validated Enumeration process
- Validated Endpoints

❖ Project #3 : Post Silicon validation of SPI IP

❖ Designation : Validation Engineer

Roles and Responsibilities:

- Understanding the SPI specifications documents.
- Reviewing and altering the features that are to be validated.
- Develop test case, Algorithm and reviewed them.
- Created test plan for validating various features of SPI that are to be validated.
- Executed test cases and created log sheet.

Features Validated:

- Transferring data at different speeds for both master and slave.
- Clock Polarity and clock Phase
- Interrupt Handling.
- Mode selection.

Project #2 : Post Silicon validation of I2C

❖ Designation : Validation Engineer

Roles and Responsibilities:

Understanding I2C specifications documents.

- Reviewing and altering the features that are to be validated.
- Develop test case, Algorithm and reviewed them.
- Created test plan for validating various features of I2C.
- Executed test cases and created log sheet.

Features Validated:

- START, STOP, ACK, NACK condition generation.
- WRITE and READ operations in different speed modes.
- Clock Synchronization and Clock Stretching.

❖ Project #1 : Post Silicon validation of UART IP

❖ Designation : Validation Engineer

Roles & Responsibilities:

- Understanding the UART specifications documents.
- Listed the features to be validated as per the requirement
- Develop test case, Algorithm and reviewed them.
- Created test plan for validating various features of UART that are to be validated.
- Executed test cases and created log sheet.

Features Validated:

- UART various baud rate supports.
- Transition FIFO and Reception FIFO test.
- Tx and Rx interrupt tests.
- Hardware flow control test with the help of RTS and CTS.

Educational Details:

 M.Sc Computer Science from Mahatma Gandhi College (Acharya Nagarjuna University).