SiVista

Layer Map

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Layer Map

Layer Name	Layer Number	Description
Cell boundary	1/0	Cell boundary
ndiff	100/0	n-type nanosheet
ndiff -duplicate	100/1	Duplication of ndiff
pdiff	101/0	p-type nanosheet
pdiff - duplicate	101/1	Duplication of pdiff label
npoly	102/0	gate(poly) for nmos
npoly - Extended	102/1	Extended npoly layer
npoly- Pattern Cut	102/2	Pattern cut of npoly layer
ppoly	103/0	gate(poly) for pmos
ppoly - Extended	103/1	Extended ppoly layer
ppoly - Pattern Cut	103/2	Pattern cut of ppoly layer
ndiffcon	104/0	ndiffusion interconnect
ndiffcon - Dummy layer	104/3	In CFET only, Dummy Island
pdiffcon	105/0	pdiffusion interconnect
pviag	106/0	ppoly to Metal0
nviag	107/0	npoly to Metal0
pviat	108/0	pdiffusion to Metal0
nviat	109/0	ndiffusion to Metal0
bspdn_pmos_via	110/0	In CFET only,pdiffusion to power rail
ndiff dvb	111/0	Deep via boundary connects ndiffusion to power rail

pdiff dvb	111/0	Deep via boundary connects pdiffusion to power rail
nwell	120/0	In FinFET only, N type well
Dummy gate	121/0	Ends the cell in X direction
Gate isolation	122/0	In CFET only, gate isolation for split gates
Diff interconnect	123/0	In CFET only, pdiffusion and ndiffusion interconnect via
M0	200/0	Metal0 (horizontal routing)
M0 label	200/1	Metal0 label (horizontal routing)
M0 pin	200/2	Metal0 pin
M0 pin label	200/3	Metal0 pin label
via0	201/0	Metal0 and Metal1 interconnect via
M1	202/0	Metal1 (vertical routing)
M1 label	202/1	Metal1 label (vertical routing)
M1 pin	202/2	Metal1 pin
M1 pin label	202/3	Metal1 pin label
M0 track guide	220/0	Horizontal Metal0 track guide
M1 track guide	221/0	Vertical Metal1 track guide
BM0	300/0	Back side power rail
BM0 label	300/1	Back side power rail label
BM0 pin	300/2	Back side power rail pin
BM0 pin label	300/3	Back side power rail pin label