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A 1GS/s 11bit SAR-assisted Pipeline ADC with 59dB SNDR in 65nm CMOS

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***Abstract*— We present an 11bit 1GS/s time-interleaved (×2) successive approximation register (SAR)-assisted pipeline analog-to-digital converter (ADC) for wideband direct sampling radio-frequency receivers. The proposed ADC architecture combines the speed advantage of the pipeline algorithm and the structural simplicity of the SAR structure. Consequently, both the structure and the operation of the pipeline stages are simplified, thereby enhancing the conversion rate and accuracy. In particular, the proposed ADC eliminates thfe multiplying digital-to-analog converter in the conventional pipeline ADC, hence compatible with process portability. The prototype ADC fabricated in 65nm CMOS process achieves SNDR ≥ 56dB across 500MHz Nyquist bandwidth at 1GS/s conversion rate with 230mW power dissipation. When benchmarked against state-of-the-art pipeline ADCs, it features a competitive Figure-of-merit, i.e., 449.2 fJ/conv.-step.**

***Index Terms*—pipeline, analog-to-digital converter (ADC), offset calibration, nonlinearity minimization.**

I. Introduction

EMERGING wideband direct sampling radio-frequency (RF) receivers are increasingly replacing their conventional narrowband sampling counterparts in communication systems [1-6]. This is in part due to their wider bandwidth and higher data rate, yet advantageously featuring lower system complexity and lower cost. The front-end RF-band analog-to-digital converter (ADC) therein is critical because it is close to the antenna of RF receivers and needs to feature high conversion rate (e.g., GHz) and high accuracy attributes.

Amongst the various ADC architectures, the pipeline architecture has been one of the most prevalent architectures for GS/s ADCs because of the concurrent operation of its pipeline stages [6-11]. As the CMOS technology scales to finer nodes, the conversion rate of the pipeline ADC is continuously enhanced, but the accuracy is generally compromised [6]. Specifically, it is increasingly difficult to achieve high linearity for the multiplying digital-to-analog converter (MDAC) in pipeline stages [7, 12], and this is largely attributed to the decreased transistor linearity and reduced transistor intrinsic gain. In the case of a GS/s 11bit ADC, the amplifier in the MDAC needs to achieve open-loop gain of > 72dB across the entire signal swing, and unity gain bandwidth of > several GHz [6, 7]. It is often observed that the reported pipeline ADCs [6-8] typically exhibit < 9 ENOB (effective number of bits).

On the other hand, the successive approximation register (SAR) ADC in general improves with technology scaling, and is increasingly prevalent. Attributed to its digital-like structure and operation (i.e., no stringent closed-loop amplifiers for MDAC are involved), its conversion rate and accuracy are enhanced.

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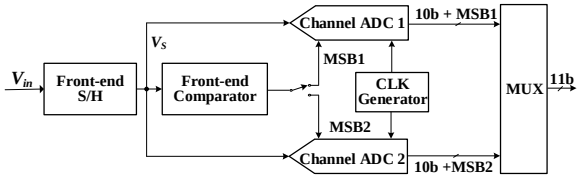

Fig. 1 System architecture of the overall ADC

In view of the aforesaid, there are increasing efforts to exploit the combined benefits of the hybrid ADCs, i.e., SAR-assisted pipeline ADCs. Specifically, several designs [12, 13] employed SAR ADCs as pipeline stages, and replaced the analog residue amplifiers with dynamic/digital amplifiers to accommodate technology scaling. However, the design effort to mitigate accuracy issues arising from the PVT variations of the dynamic amplifiers is very considerable. Another design [14] eliminated the MDAC by means of pipelined sample-and-holds (S/Hs) with cascaded SAR ADCs. However, the requirement of a large number of series-connected S/Hs (i.e., one S/H per bit) operating at the ADC full speed compromises the conversion accuracy and leads to undesirable power and hardware overheads.

In this paper, we propose an 11bit 1GS/s SAR-assisted pipeline ADC embodying time-interleaved S/Hs with cascading SAR ADCs as a new pipeline architecture without the need to use intra-stage MDACs. This architecture offers combined advantages of higher accuracy and higher conversion rate when the process technology scales to finer nodes. Specifically, the adoption of the SAR ADCs without the need for MDACs mitigates the aforesaid accuracy limitation of the conventional pipeline ADC due to technology scaling. Further, the operation of the pipeline stages is simplified to a single-iteration successive approximation (SA), thereby enhancing the conversion rate. In addition, 2bit/step conversion scheme is employed to reduce the number of the S/Hs, and the speed requirement of these S/Hs is substantially alleviated by the time-interleaved technique. The required hardware of the channel ADC is reduced by means of the extraction of the quantization for the MSB (Most Significant Bit) at the front of the channel ADCs. A prototype ADC is fabricated in 65nm CMOS technology and achieves Signal-to-Noise-and-Distortion-Ratio (SNDR) ≥56dB and Spurious-Free-Dynamic-Range (SFDR) ≥60dB across 500MHz Nyquist bandwidth at 1GS/s conversion rate with 230mW power dissipation, leading to a competitive Figure-of-merit of 449.2 fJ/conv.-step.

This paper is organized as follows. Section II describes the proposed ADC. Section III explains the critical building blocks. Following this, Measurement results are presented in Section IV and conclusions are drawn in Section V.

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II. Proposed SAR-assisted 11bit 1GS/s Pipeline ADC

Fig. 1 depicts the system architecture of the proposed ADC. The front-end S/H is employed to mitigate the timing mismatch between two channel ADCs. Subsequent to the front-end S/H, a high-precision front-end comparator is employed to predetermine the MSB. In this manner, the ensuing channel ADCs only need to resolve the subsequent 10 bits instead of the full 11 bits, hence reducing the hardware and power overheads.

II.A. Proposed SAR-assisted 10bit 500MS/s Channel ADC

Fig. 2 depicts the block diagram of the proposed channel ADC wherein the pipeline stages are realized on the basis of the 2bit/step SAR ADCs [15] with resolutions of 2, 4, 6, 8 and 10 bits for Stage_1 to Stage_5 respectively. Each pipeline stage resolves 2 bits, and collectively 10 bits (2nd MSB to LSB) from all pipeline stages. On the basis of the 2bit/step scheme [15], each pipeline stage comprises three comparators, whose outputs are the 3bit raw D_{out}, and the pertinent 2bit digital output is obtained by decoding the 3bit raw D_{out} using full adders; see Fig. 2(a). In addition, the 3bit D_{out} controls the CDAC switches in the ensuing stage by means of digital logic gates and flip flops, akin to the SA control logic in the reported design [15]. The S/Hs are employed herein to sample and hold the input signal, and the sampled signals are multiplexed to the pipeline stages by the switch matrix.

The timing diagram of the proposed ADC architecture is illustrated in Fig. 2(c). The front-end S/H is level triggered while the front-end comparator is rising-edge triggered, and both are clocked at 1GHz. The clock of the front-end comparator is slightly delayed so that the comparator compares the sampled input V_S after the front-end S/H completes its sampling. The 5 S/Hs are time-interleaved and sample V_S from the front-end S/H at 100MS/s with different phases (φ in Fig. 2(b)). The 5 associated pipeline stages operate concurrently and convert at 500MS/s.

Using Figs. 1 and 2, the detailed operation of the proposed ADC is now described. The front-end S/H samples the input signal V_{in}, and the MSB (i.e., MSB1) is predetermined by the front-end comparator. In the channel ADC, one of the S/Hs, taking S/H1 as the case in point, samples V_S and passes it to Stage_1. With the predetermined MSB, Stage_1 converts the sampled input ($V_{S\_sampled}$) and resolves the 2nd and 3rd MSB on the basis of the 2bit/step SAR scheme [15]. Subsequently, Stage_1 passes its digital output D_{out1} to Stage_2; D_{out1} is 3bit raw output [15]. In the meantime, S/H1 buffers $V_{S\_sampled}$ to Stage_2. Similarly, with the predetermined MSB and the received D_{out1}, Stage_2 resolves the 4th and 5th MSB, and passes its digital output D_{out2} to Stage_3. Similar signal processing continues until the last two bits are resolved by Stage_5. Note that digital signals (instead of analog residue signals) are transmitted between the pipeline stages.

II.B. Merits of the Channel ADC

The proposed channel ADC offers three attractive merits. First, as aforementioned, the adoption of the SAR structure as the pipeline stages eliminates the need for the MDAC. This not only simplifies the design and realization of pipeline ADCs, but also largely mitigates the accuracy limitations arising from the MDAC, particularly when the process technology scales to smaller nodes. Second, the operation of the pipeline stages in our channel ADC is simplified to a single-iteration SA, hence leading to higher conversion rate; conversely, in the conventional pipeline stages, a coarse analog-to-digital conversion and a time-consuming MDAC amplification and settling are required. Third, the digital transmission between the pipeline stages features high noise tolerance, potentially improving the transmission accuracy.

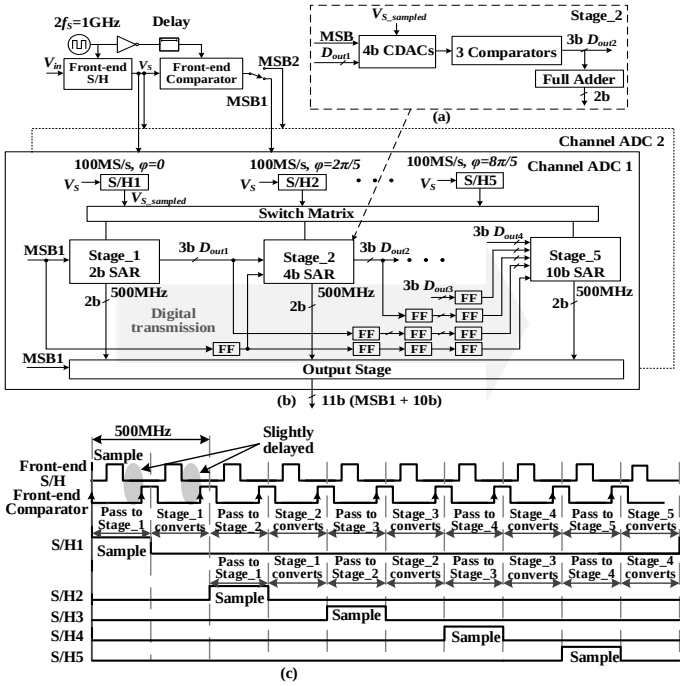

Fig. 2(a) Block diagram of the pipeline stage, (b) block diagram of the proposed MDAC-free channel ADC, and (c) the associated timing diagram

Note that although our channel ADC requires additional S/Hs, the sampling rate of these S/Hs is much lower (e.g., 5 times lower) compared to the conversion rate of the channel ADC. Further, the elimination of the MDAC and the simplified stage operation provide additional time for the S/H settling, hence alleviating the S/H power dissipation. In the context of the overall design, the merits of our channel ADC outweighs the shortcoming, particularly with process technology scaling; these S/Hs can be simply realized using open-loop source followers (see Section III.B later).

II.C. Accuracy Requirement of the Channel ADC

The accuracy of our channel ADC is primarily ascertained by the S/Hs and the SAR stages. Specifically, the *kT/C* switching noise and comparator thermal noise needs to be lower than the quantization noise of the overall ADC (-75.4dB in this case), and the nonlinearity due to S/H gain error and capacitor mismatch need to be < ½LSB. Our design to address these requirements is described in Section III later.

For sake of completeness, note that the S/Hs in the channel ADCs suffer from timing and offset mismatches. In our design, the timing mismatch is mitigated by the front-end S/H, and we mitigate the offset mismatch between the S/Hs and between the two channel ADCs by adopting a reported off-chip calibration

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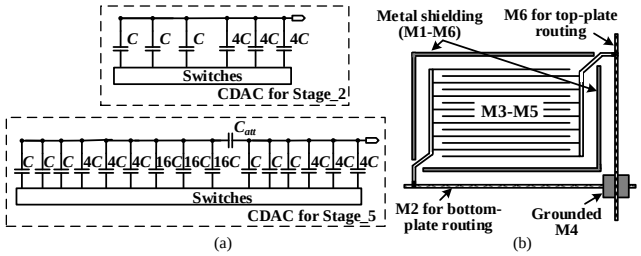

Fig. 3(a) Block diagrams of the CDACs for Stage_2 and Stage_5, and (b) Unit capacitor

[16] with a pilot dc voltage, where the associated power dissipation is approximately 9.46mW.

III. Design and Realization of the Critical Blocks

III.A. Pipeline Stages

The pipeline stages are realized with 2bit/step capacitive-DAC (CDAC) SAR ADCs [15] with increased resolution from the first to the last stages. To mitigate the capacitor overheads, split-CDACs were employed for the last three stages; the first two stages do not employ split-CDACs due to their low resolutions. Fig. 3(a) depicts the block diagrams of the CDACs for Stage_2 and Stage_5. The attenuation capacitor (C_{att}) is slightly enlarged on the basis of the layout extraction to enhance the CDAC linearity. Bottom-plate sampling technique is employed for all the stages to mitigate the inter-stage gain errors caused by the parasitic capacitance at the top plates of the CDACs.

To achieve < -75.4dB *kT/C* noise, the total capacitance of >145fF is required for each CDAC. We design the total capacitance for each CDAC to be the same, i.e., 480fF, primarily for the capacitor matching. Specifically, we use relatively large unit capacitors realized by the Metal-Oxide-Metal fringing structure (M3-M5) enclosed by a grounded shielding ring, as depicted in Fig. 3(b), and employ three layout techniques for all the CDACs. First, M6 and M2 that are vertically far apart from each other are employed for the top- and bottom-plate routings respectively to minimize the parasitic capacitance in between. The M6 and M2 are routed orthogonally to further reduce the parasitic capacitance, and a grounded M4 layer is employed to isolate their cross-area to reduce the coupling. Second, the common-centroid layout technique is employed to address the fabrication process variation. Lastly, we isolate the capacitors from the rest of the circuitry by adopting both guard rings and BFMOAT—a physical layer to block the P-well implant and to create a highly resistive path. On the basis of our layout extraction, the CDACs with a 15fF unit capacitor achieve capacitor mismatch of ~ 0.2%, which is sufficient to ensure the maximum variance of the nonlinearity less than $(\frac{1}{2}\text{LSB})^2$ [17].

III.B. High-linearity S/Hs

The front-end S/H and the five S/Hs in the channel ADC embody similar architecture and modus operandi. For the sake of brevity, only the front-end S/H is described in this section.

Fig. 4 depicts the block diagram of the front-end S/H, mainly comprising bootstrapped switch and high-linearity unity-gain buffers. The sampling capacitor (C_S) is designed to be 450fF to obtain relatively low *kT/C* noise, thereby reducing its accuracy

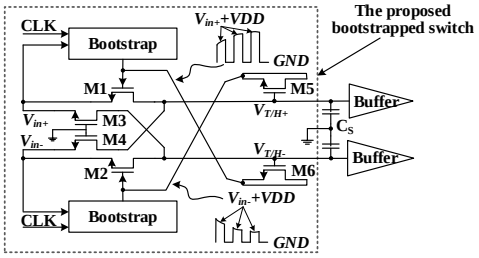

Fig. 4 Block diagram of the front-end S/H

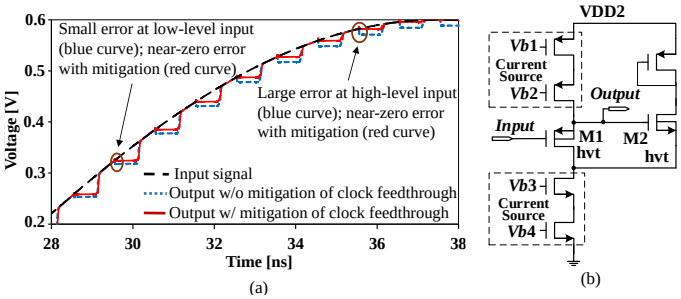

Fig. 5 (a) Simulated output ($V_{T/H+}$ - $V_{T/H-}$) of the bootstrapped switch, and (b) unity-gain buffer in the front-end S/H

degradation to the ensuing building blocks.

B(1). Bootstrapped Switch

The bootstrapped switch is realized by adopting a well-established bootstrap technique [8] to equalize the on-resistance of M1 and M2. The signal feedthrough is mitigated by cancelling it with a 180-degree phase-shifted replica, introduced by the cross-coupled M3 and M4; see Fig. 4. We propose to mitigate the clock feedthrough by equalizing it at both differential signal paths ($V_{T/H+}$, $V_{T/H-}$). In this fashion, the clock feedthrough is mainly a common-mode noise that is largely immune in fully-differential operation. This equalization is realized by employing cross-coupled M5 and M6. Note that the gates (instead of drain or source) of M5 and M6 are connected to the signal paths to avoid the potential charge injection into the signal paths.

Fig. 5 (a) depicts the simulated output ($V_{T/H+} - V_{T/H-}$) of the bootstrapped switch with (solid red) and without (dotted blue) the proposed mitigation of clock feedthrough technique; the dashed black curve is the input signal that serves as the reference for comparison. As expected, the sampling error due to clock feedthrough (see blue curve) increases as the input magnitude increases since the gate of the switch experiences increased voltage drop at high-level inputs. The red curve depicts that the clock feedthrough is heavily mitigated by means of our proposed mitigation technique.

B(2). High-linearity Buffer

The unity-gain buffer is largely an open-loop source follower (M1 and the PMOS Current Source); see Fig. 5(b). The required linearity and gain is achieved by the following three means. First, an additional source follower (M2) is employed to keep the drain-source voltage of M1 constant. Second, the triple well layout technique is adopted for M1 and M2 to eliminate the body effect therein. Third, high threshold-voltage transistors (hvt in Fig. 5(b)) are adopted for M1 and M2, and low threshold-voltage transistors for the other transistors. The low

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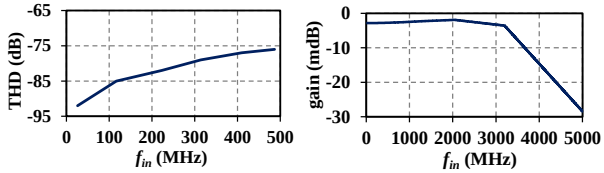

Fig. 6 Simulated THD and voltage gain of the front-end S/H

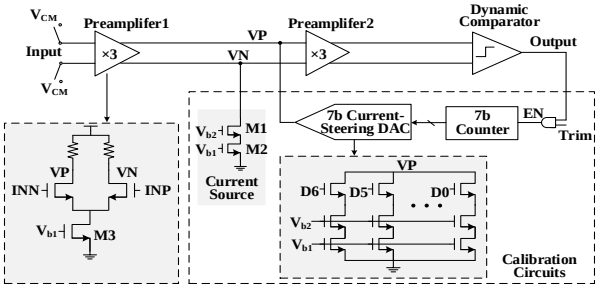

Fig. 7 Block diagram of the proposed comparator

threshold-voltage transistors with smaller parasitic capacitance serve to ensure wide bandwidth, and the hvt transistors serve to minimize the gain error by means of designing the intrinsic gain of M1 and M2 to $(g_{m1}g_{m2})/(g_{ds1}g_{ds2}) > 2^{12}$. On the basis of Spectre simulations, the proposed buffer achieves 3σ gain of > -2.75mdB for input bandwidth up to 3.5 GHz with 1.2 $V_{PP,diff}$ full-scale input signal, which is sufficient for the requirements of 11bit and 1GS/s.

To illustrate the efficacy of the overall front-end S/H, Fig. 6 depicts the simulated total harmonic distortion (THD) and the voltage gain of the front-end S/H as a function of the input frequency (i.e., f_{in}) at a conversion rate of 1GS/s. The THD remains below -75dB for input frequency ≤ 500MHz and the voltage gain is ≥ -2.8mdB for input frequency up to 3.2GHz. Both parameters are sufficient for 11bit and 1GS/s.

III.C. Comparators

Fig. 7 depicts the block diagram of the proposed comparator that serves to predetermine the MSB at the front end and serve as the quantizer in each pipeline stage. The comparator comprises two preamplifiers, one dynamic comparator [15] and circuits for offset calibration.

The noise of the comparator is dominated by preamplifier 1 because the noise contributed by the rest circuitry is largely attenuated either by preamplifier 1, or collectively by preamplifier1 and preamplifier 2. We minimize the noise of preamplifier 1 by increasing the transconductance (G_m) of the input transistors. On the basis of the Spectre noise simulation, the input-referred noise of our comparator with G_m =3.3mS is -56.1dBm, which is 78.6dB below the signal power.

The offset in our comparator is largely eliminated by a proposed calibration embodying a 7b digital counter, a 7b current-steering DAC and a current source realized by two cascoded transistors (M1 and M2). The operation of the calibration is now described. First, the comparator inputs are shorted to V_{CM}. Second, the output of the comparator is pre-set to '1' by means of a deliberate introduction of a positive comparator offset by discharging node VN (by the current source in Fig. 7). Lastly, the current-steering DAC keeps pulling down the voltage at VP until the output of the comparator switches to '0'. In this manner, the comparator offset is largely eliminated.

The calibration range and the calibration resolution (the minimum offset that can be achieved) are both determined by the current-steering DAC. We design the current-steering DAC to be 7 bits so that our calibration is able to eliminate the offset (when referred to the input) up to ±18mV, and achieve the minimum resultant input-referred offset of 0.28mV (< ½LSB after calibration); the 3σ input-referred offset of the comparator without calibration (from simulations) is ±13mV.

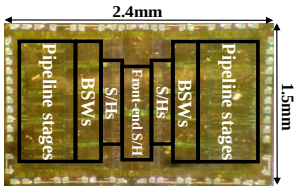

Fig. 8 Microphotograph of the ADC prototype

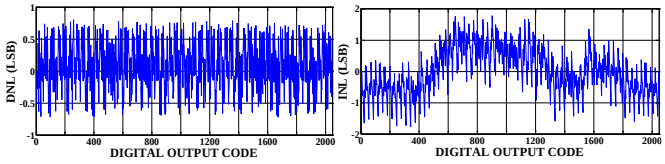

Fig. 9 Measured DNL and INL

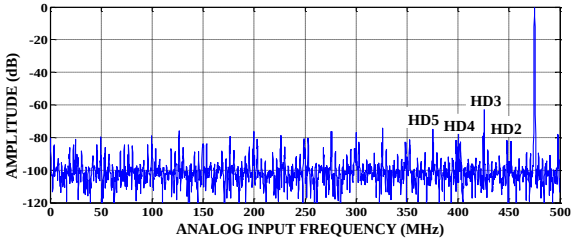

Fig. 10 Measured FFT spectrum (16384 points) at 1GS/s with 475.2MHz input

IV. Experimental Results

Fig. 8 depicts the microphotograph of the proposed ADC prototype realized in 65nm CMOS. The pipeline stages (mostly CDACs) occupy most of the silicon area (approximately 50%), followed by the S/Hs and the bootstrapped switches (BSWs).

The measured total power dissipation at 1GS/s is 230mW, whose breakdown is 150mW for S/Hs, 28.8mW for comparators, 7.2mW for reference generation and the rest for digital logic. The SAR ADCs from the first stage to the last stage in the channel ADC dissipate 3.79mW, 3.85mW, 4.06mW, 4.33mW, and 5.27mW respectively.

Fig. 9 depicts the measured differential nonlinearity (DNL) and integrated nonlinearity (INL) at 1 GS/s. The DNL and INL are within +0.8LSB/-0.7LSB and ±2LSB respectively, which are largely due to capacitor mismatch in the CDACs. Nevertheless, they satisfy the requirement of the proposed ADC for the intended wideband direct sampling receivers.

Fig. 10 depicts the measured spectrum of the ADC prototype output at the conversion rate of 1GS/s with a $1.2V_{P-P}$ full-scale input signal at 475.2MHz. The measured SNDR and SFDR are 55.9dB and 60.05dB respectively. The HD3 (3rd harmonic) is the dominant distortion component, and other than the

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TABLE I Performance Summary and Benchmark

Reference	This work	JSSC'12 [6]	JSSC'13 [7]	ISSCC'06 [8]	ISSCC'11 [9]	JSSC'14 [5]	VLSI'16 [10]	ISSCC'17 [12]	ISSCC'15 [4]
Technology (nm)	**CMOS 65**	CMOS 40	CMOS 40	CMOS 130	BiCMOS 180	CMOS 65	CMOS 28	FinFET 14	CMOS 28
Architecture	**Pipelined/SAR**	Pipeline	Pipeline	Pipeline	Pipeline	SAR	Pipeline	Pipelined/SAR	Pipelined/SAR
Supply voltage (V)	**1.2/2**	2.5	0.9/1.5/1.95	1.2/2.5	1.8/3.3	1	0.9/1.8/2.5	0.95	1
Conversion rate (GS/s)	**1**	3	2.1	1	1	1	5	1.5	5
Resolution (bit)	**11**	12	12	11	12	10	14	10	10
Area (mm^2) excluding pads	**2.5**	0.4	0.5	3.5	2.4	0.78	14.4	0.0016	0.35
Worst SNDR (dB)	**56**	51	50	52	59	50	52	50	46.1
Best SNDR (dB)	**59.1**	57.5	52	55	62	55	63	51	57
Power (mW)	**230**	500	280	250	575	18.9	2300	6.92	150
FoM_{Walden} (fJ/conv.-step)	**449.2**	574.9	516.1	768.6	789.6	73.8	1409.8	17.7	192.5
$FoM_{Schreier}$ (dB)	**149.4**	145.8	145.7	145	148.4	154.2	142.4	160.3	148.1

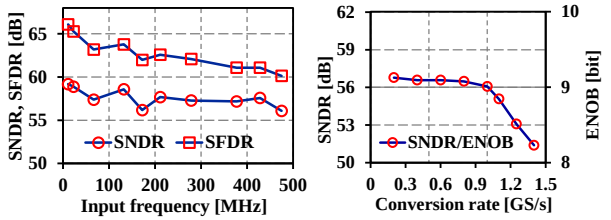

Fig. 11(a) Measured SNDR and SFDR versus input frequency, and (b) Measured SNDR/ENOB versus conversion rate

contribution by the capacitor mismatch in the CDACs, HD3 is also contributed by the sampling/resampling settling error, and the nonlinearity of the unity-gain buffers in the front-end S/H and the S/Hs in the channel ADCs. The other distortions are largely negligible (≤-70dB).

Fig. 11 (a) depicts the measured SNDR and SFDR versus input frequency at 1GS/s. The proposed ADC achieves SNDR ≥ 55.9dB (equivalent to 9 ENOB) up to 475MHz. The peak SNDR is 59.1dB, equivalent to 9.52 ENOB. The SFDR remains above 60.5dB up to 475MHz, and exhibits a peak value of 66dB at low frequency. Fig. 11(b) depicts the measured SNDR/ENOB versus conversion rate. The measurement is performed with normalized input frequency (Input frequency/Conversion rate=0.475). It can be observed that the SNDR remains largely constant (< 1dB degradation) with the conversion rate up to 1GS/s.

Table I tabulates the key parameters of the proposed ADC prototype (realized in 65nm CMOS process), and benchmark against state-of-the-art GS/s ADCs. The primary features of the prototype ADC include SNDR ≥ 55.9dB across 500MHz Nyquist bandwidth at 1 GS/s conversion rate with 230mW power dissipation from a dual power supply of 1.2V/2V. The figure-of-merit (FoM) of our design, either based on Walden FoM_{Walden} or Schreier $FoM_{Schreier}$, is competitive amongst designs employing similar technology nodes; for sake of fair comparison, both FoMs are calculated based on the worst SNDR within the Nyquist bandwidth. As explained in Section II.B, the proposed architecture could potentially achieve better performance with finer technology nodes.

V. Conclusions

A 1GS/s 11bit SAR-assisted pipeline ADC has been reported. The proposed ADC combined the speed advantage of the pipeline algorithm and the structural simplicity of the SAR ADC. Consequently, the MDAC was eliminated, and both the structure and the operation of the pipeline stages were simplified. Measurements on the prototype ADC depicted an SNDR ≥56dB across 500MHz Nyquist input frequency at 1GS/s conversion rate. When benchmarked against state-of-the-art pipeline ADCs, the proposed MDAC-free ADC featured a competitive FoM. Attributed to the elimination of the MDAC and the simplification of the pipeline stages, the performance of the proposed ADC could be substantially enhanced when implemented using finer technology nodes.

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