A CMOS Track-and-Hold Circuit with beyond 30 GHz Input Bandwidth

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***Abstract*— To realize future ultra high-speed data converters, sampling circuits with very large bandwidth are required. This paper studies the design of ultra high-speed Track-and-Hold (T/H) circuits. A bootstrapping circuit for T/H is presented. The proposed T/H is simulated in 32 nm SOI-CMOS technology. It achieves an input bandwidth higher than 30 GHz and provides an SNDR higher than 43.8 dB (ENOB > 7.0 b) when sampling a 34 GHz input signal at 10 GS/s.**

I. INTRODUCTION

Sampling rate of Analog-to-Digital Converters (ADCs) has been continuously increasing in the past decades. Today, ADCs operating up to 65 GS/s are available [1]. The main applications of such ADCs are instrumentation and fiber optic communication systems (e.g. 100 Gb/s long haul links). The architecture of choice for ultra high-speed ADCs seems to be time-interleaving (TI) [1]-[3]. In a TI ADC, multiple sub-ADCs are placed in parallel, and each sub-ADC (channel) processes a different sample of the input signal at a low sampling rate. By increasing the number of the channels in a TI ADC, the aggregate sampling rate of the ADC can be increased. Frontend Track-and-Hold (T/H) circuits are a critical building block in high-speed ADCs. Whether there is a single frontend T/H running at the aggregate sampling rate as in Fig. 1(a), or each channel has a separate T/H running at a low sampling rate as in Fig. 1(b), the T/H should be able to sample very high-frequency input signals. The maximum input frequency can be as high as half the aggregate sampling rate (Nyquist frequency). Table I lists some of the recently reported T/Hs [1]-[7]. Some of these circuits are used in high-speed ADCs and some reported as standalone T/Hs. The highest reported effective resolution bandwidth (ERBW) is about 20 GHz. In Table I, some T/Hs have a low sampling rate and that is because of the time-interleaved topology.

The focus of this paper is on CMOS T/H circuits for TI ADCs as in Fig. 1(b). The challenges in the design of T/H circuits are studied. A circuit is proposed to enhance the linearity and to obtain an ERBW over 30 GHz. The proposed circuit is compared with the conventional topologies and it is shown that it has 15 to 20 dB lower harmonic distortion.

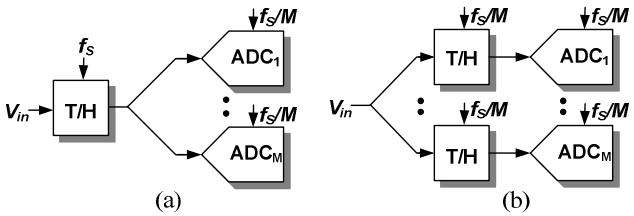


Figure. 1. Time interleaving (by a factor of M) using (a) a single frontend T/H, and (b) separate T/H for each channel.

II. CHALLENGES IN DEISGN OF HIGH-SPEED T/H CIRCUITS

The simplest T/H is built using a transistor as a transmission gate (i.e., as a switch) as shown in Fig. 2(a) [8]. For high-speed applications, switched source-follower (SSF) T/H, shown in Fig. 2(b), is another alternative [5]. We will compare these circuits in section IV, but first we study the tradeoffs in the design of the simple CMOS T/H of Fig. 2(a).

Bandwidth: The bandwidth in tracking mode is given by $(R_{on}C_H)^{-1}$ where R_{on} is the on-resistance of MOS switch and C_H is the hold capacitor. For high-speed applications, a small R_{on} is needed. This translates into a large W/L (width to length ratio) for the MOS switch.

Signal Feedthrough: The leakage of the input signal to the output during the hold mode is not negligible in high-speed applications, because of the large W and large parasitic capacitances of the switch. A method to diminish signal feedthrough is to generate a second feedthrough path with an opposite polarity [3]. In Fig. 3(a), transistor M_f is added to reduce the signal feedthrough.

Charge injection: The product of time constant and charge injection error is proportional to L^2 for a simple CMOS T/H [8]. Thus, a technology with a smaller feature-size enhances the performance of T/Hs. The charge injected into C_H is a function of the gate-source voltage of the switch V_{GS1} [8]. Clock bootstrapping [9] makes V_{GS1} almost constant and is an effective method to reduce the distortion. A conventional bootstrapped T/H is shown in Fig. 3(b). The circuit, however, suffers from a large input capacitance because its complexity

TABLE I. EXAMPLES OF HIGH-SPEED T/H CIRCUITS (SAMPLING RATE IS PER A CHANNEL IN TI ADCS)

Ref.	*Topology*	*f_S (GS/s)*	*min(BW,ERBW) (GHz)*	*Technology*	*Application*
[1]	Charge-mode	N/A	18 GHz	CMOS 40nm	8-b 65 GS/s ADC with ENOB of 5.7b at f_{in}=8GHz
[2]	MOS switch	2.5	7 GHz	CMOS 65nm	6-b 40 GS/s ADC with ENOB of 4.6b at f_{in}=8 GHz
[3]	MOS switch	1.5	6.8 GHz	CMOS 90nm	6-b 24 GS/s ADC with ENOB of 4.8b at f_{in}=8 GHz
[6]	MOS switch	10	3 GHz	CMOS 180nm	5 bit effective resolution (P_D=200mW)
[7]	Switched emitter follower	10	2 GHz	BiCMOS 130nm	THD < -50 dB (P_D=19 mW)
[5]	Switched source follower	30	7 GHz	CMOS 130nm	THD < -29dB (P_D=94 mW)
[4]	Distributed T/H	50	> 20 GHz*	BiCMOS 180nm	5-b 50-GS/s ADC with ENOB of 3.5b at f_{in}=20 GHz

*) 42GHz -3dB bandwidth in track mode

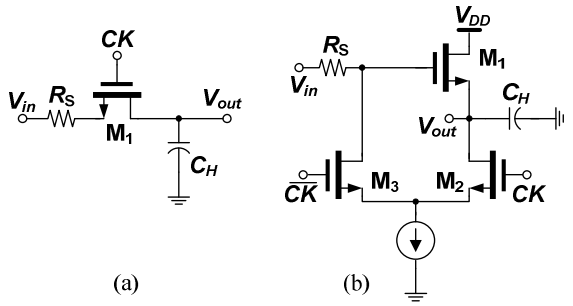


Figure. 2. (a) T/H circuit using MOS switch. (b) Switched source-follower T/H circuit. R_S is the source resistance and its size affects the bandwidth of circuits as well as correct turn off M_1 in (b).

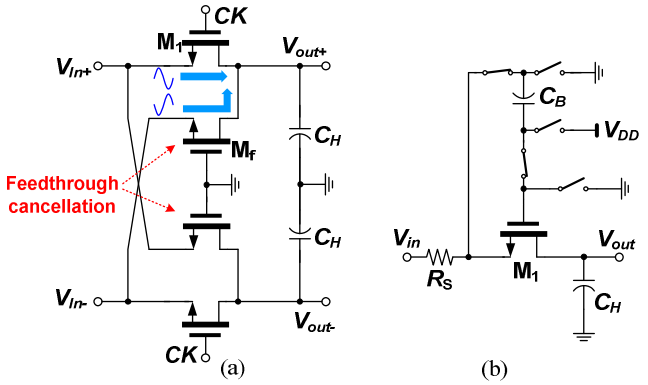


Figure. 3. (a) Differential T/H circuit with signal feedthrough cancellation. W/L of M_f is the same as M_1. (b) A T/H with clock bootstrapping.

and also large C_B [9]. This results in the reduction of the input bandwidth.

Sampling Jitter and Aperture Error: Fig. 4(a) shows the relationship between the rms clock jitter and effective number of bits (ENOB) of the output signal according to [10]. A rms jitter below 100 fs is needed to obtain an ENOB of 6 bits at input frequencies above 30 GHz. Achieving such a low sampling jitter is, to a high extent, independent of the design of the T/H, but more related to the clock generation and distribution circuitry. The limited fall-time of CK results in aperture error. The ENOB, calculated according to [11], is shown in Fig. 4(b). The error stems from the fact that the exact turn off moment of the switch depends on the input voltage. To reduce the error, either the fall time of CK shall be very small or the difference between high level of CK and V_{in} should be constant (as in the clock bootstrapped T/H).

Thermal Noise: Signal-to-noise ratio (SNR) of a T/H is determined by the thermal noise generated by the on-resistance (R_{on}) of the switch, often expressed as kT/C_H (k is Boltzmann constant, and T is temperature) [8]. As shown in Fig. 4(c), for typical input amplitudes, a hold capacitor as small as 100 fF is sufficient for 8-bit precision.

Variable time constant: Dependency of the time constant ($R_{on}C_H$), and consequently, the delay (in tracking mode) on the input voltage amplitude results in distortion [12]. Fig. 4(d) shows the resulting harmonic distortion when modeling R_{on} as $R_{on0}/[1\text{-}a(V_{in}\text{-}V_0)]$, where R_{on} and a are constants, and V_0 is the input DC level. R_{on} of a MOSFET depends on its gate-source voltage [8] and clock bootstrapping can help to reduce the time constant variations by making R_{on} almost constant.

III. PROPOSED CIRCUIT

Considering the discussions in the previous section, clock bootstrapping is an effective method to enhance the performance of T/Hs. We need a bootstrapping circuit that is suitable for ultra high-speed circuits. The proposed circuit is shown in Fig. 5. It uses a PMOS transistor (M_2) to shift the input signal by its gate-source voltage V_{GS2}. When CK is low, M_4 is off and M_3 is on. The voltage at node X is $V_{in}+|V_{GS2}|$. The gate of the main switching transistor (M_1) is also at V_X. The gate-source voltage of M_1 is

$$V_{GS1} = V_Y - V_{in} = |V_{GS2}|. \qquad (1)$$

Since the drain current of M_2 is constant, its gate-source voltage is also constant. The gate-source voltage of M_1 is, to the first approximation, independent of the input voltage. In practice, V_{GS2} weakly depends on V_{in} because of channel-length modulation and body effect. Nevertheless, due to the almost constant V_{GS} of M_1 in Fig. 5, the nonlinearities caused by the charge injection of M_1, the sampling aperture error, and variable R_{on} of M_1 are significantly reduced compared with a conventional T/H.

For a high-frequency input, the delay from input to node Y prevents M_1 to have a completely constant V_{GS}. Using a small-signal model and for in-band frequencies, it can be shown that the delay from input to node Y can be approximated by

$$\tau_{BS} \approx R_{on3}C_Y + (C_{GS2} + C_X + C_Y)/g_{m2}, \qquad (2)$$

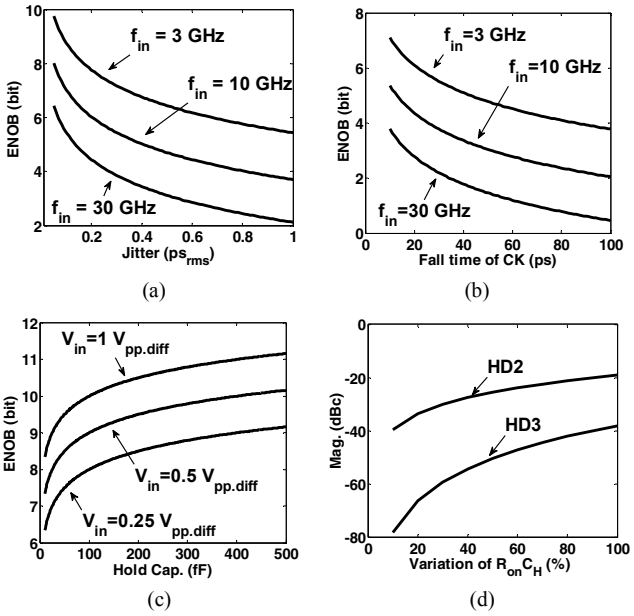


Figure. 4. (a) ENOB versus clock jitter for three different input frequencies. (b) ENOB versus rise/fall time of clock for a single-ended circuit with $0.25V_{pp}$ input (for a differential case, ENOB can be 3-4 bits higher). (c) ENOB versus size of the hold capacitor. (d) Relationship between harmonic distortion and time constant variations (f_{in} is close to f_{-3dB} of T/H).

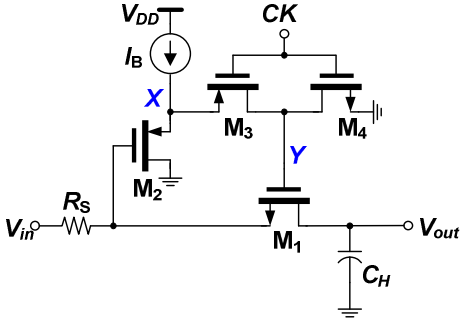


Figure. 5. Proposed T/H circuit (only half circuit is shown; Signal-feedthough cancelation is not shown). I_B is a cascode current source.

TABLE II. COMPARISON CONDITIONS

Model of transistors	BSIMSOI 4.3
Sampling rate	10 GS/s
Input range	$0.5V_{pp,diff}$
Hold capacitor	50 fF
W/L of the main switch(M_1)	8 µm /40 nm

where, C_{GS2} and g_{m2} the gate-source capacitance and transconductance of M_2, respectively. C_X and C_Y model the total capacitance at nodes X and Y, respectively, and R_{on3} is the on-resistance of M_3 in the triode region. The time constant needs to be minimized by proper sizing of the transistor and having a sufficiently large g_{m2}. This sets a lower limit for the bias current of M_2.

IV. SIMULATION RESULTS AND COMPARISON

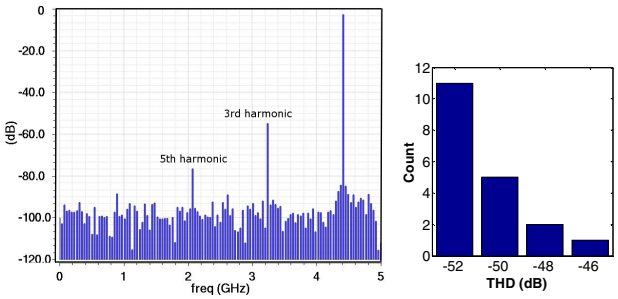
We compare the performance of the two circuits in Fig. 2 with the proposed circuit of Fig. 5. The test conditions are given in Table II. All circuits are differential and have a feedthrough cancellation similar to that in Fig. 3(a). The circuits are designed in a 32 nm SOI-CMOS technology having nominal supply voltage of 0.9 V for thin-oxide transistors and 1.5V for thick-oxide transistors. Circuits are simulated using foundry-supplied model of transistors. All transistors are thin-oxide except for the PMOS transistors used to implement the current source I_B in Fig. 5. In the circuit of Fig. 5, I_B is 1 mA, V_{DD} is 1.5 V, high level of CK is 0.9 V. V_X never goes above 0.95 V, and hence $M_{1\text{-}4}$ can be regular thin-oxide transistors. The W/L of M_1 is selected such that the combination of R_S+R_{on1} and C_H result in a bandwidth higher than 30 GHz.

Fig. 6(a) illustrates the output spectrum of the proposed circuit at an input frequency of 34.41 GHz. The spectrum is obtained using a 256-point FFT. The spurious-free dynamic range (SFDR) of the circuit is larger than 51 dBc, and is limited by 3rd harmonic. Even-order harmonics appear in the output spectrum, only if there is some mismatch and therefore unbalance between positive and negative paths of the differential circuit. The histogram of the total harmonic distortion (THD) after 20 Monte-Carlo simulations, including both mismatch and process variations, is shown in Fig. 6(b). The reduction of THD is mostly caused by 2nd harmonic.

Fig. 7(a) compares the magnitude of the fundamental tone, normalized to its DC value, for the three circuits. The proposed circuit provides the highest bandwidth of 37 GHz, whereas the SSF has the lowest bandwidth. The reason behind the reduced bandwidth of the SSF T/H is that a larger R_S is required for its correct operation; to insure that M_1 in Fig. 2(b) turns off in the hold mode, the product of R_S and I_{SS} should be large enough. With I_{SS} = 2 mA, R_S must be larger than 300 Ω, and this lowers the bandwidth.

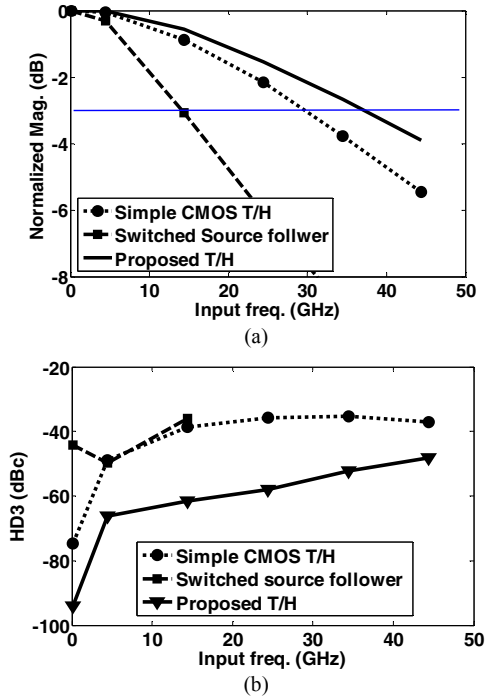
To compare the linearity of the T/Hs, the amplitude of the 3rd harmonic (HD3) is depicted in Fig. 7(b). The simple MOS T/H and the SSF circuit have an almost similar distortion. The harmonic distortion increases to -35 dBc, limiting ENOB to 5.5 bits. Adding thermal noise and jitter to this, the ENOB of the conventional T/Hs is limited to about 5 bits. The results are in agreement with the previous works in Table I. The proposed circuit provides a distortion level below -50 dB up to its -3 dB bandwidth, enabling an ENOB in excess of 7 bits.

To investigate the signal feedthrough and droop, T/H was simulated with a longer hold time as shown in Fig. 8. The signal feedthrough is 0.16 mV_{pp} and the droop rate is 55 µV/ns. The impact of transistor mismatch on the signal feedthrough can be evaluated by Monte-Carlo simulation. For 100 Monte-Carlo simulations, the signal feedthrough remains below $0.58mV_{pp}$. Table III summarizes the results for the proposed circuit. Typical ENOB of 7.3 bit and worst-case ENOB of 7.0 bit are obtained from Monte-Carlo simulations (including the transistor noise). Simulation has shown that ENOB can be increased by increasing the size of the clock buffering inverters, and hence reducing their impact on the clock jitter. But the power consumption of the clock buffers will increase.



(a) (b)

Figure. 6. (a) Spectrum of the output at f_S = 10 GS/s and f_{in} = 34.41GHz. The fundamental tone is downconverted to f_{in} -3f_S = 4.41 GHz and the 3rd harmonic is at 3f_{in} -10f_S . Magnitude is normalized to the input amplitude of 0.5$V_{pp,dif}$. (b) Histogram of total harmonic distortion for 20 runs.



(a)

(b)

Figure. 7. Comparison of the T/Hs in Fig. 2 with the proposed T/H (using bootstrapping) at f_S = 10 GS/s. (a) Magnitude of the fundamental tone is normalized to its DC value. (b) Third-order harmonic distortion versus input frequency.

V. CONCLUSION

In ultra-high-speed applications, a conventional T/H using MOS switch is only suitable for low resolutions (ENOB below 6 bits). We cannot observe any advantage for the switched source-follower T/H over the MOS switch T/H under our test conditions. We have proposed a bootstrapped MOS switch T/H circuit that provides a harmonic distortion about -50 dB. This work shows the feasibility of sampling signals beyond 30 GHz with an ENOB higher than 7 bits.

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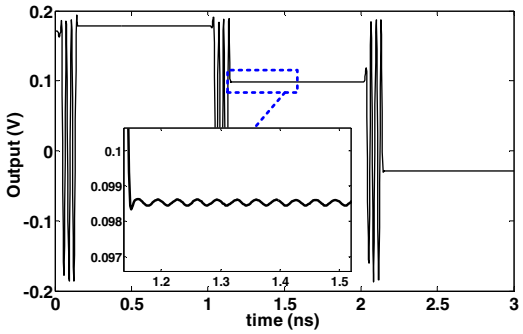

Figure. 8. Differenital output of the T/H. f_S is 1 GHz, track time is 100 ps, and f_{in} is 30.1 GHz. The inset shows the input feedthrough in hold mode.

TABLE III. SUMMARY OF PERFORMANCE (AT 10 GS/S).

Technology	32 nm SOI-CMOS
Supply voltages	0.9 V and 1.5 V
Input ranges	0.5 $V_{pp,diff}$
THD @ f_{in}=34.4 GHz	-46.7 dBc*
SFDR @ f_{in}=34.4 GHz	49.4 dBc*
SNDR @ f_{in}=34.4 GHz	43.8 dB*
ENOB @ f_{in}=34.4 GHz	7.0 bit*
-3dB bandwidth	37 GHz†
Power dissipation	Analog: 3.3 mW clock buffer: 0.6mW

*) Worst-case result after 20 Monte-Carlo simulations.

†) Pre-layout value.

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