14.4-GS/s, 5-bit, 50mW Time-Interleaved ADC with Distributed Track-and-Hold and Sampling Instant Synchronization for ADC-Based SerDes

Tao Jiang[1], and Patrick Y. Chiang[2]

[1]Qualcomm Incorporated, Raleigh, NC, 27617 USA
[2]Fudan University, Shanghai, 201203, China
Email: taoj@qti.qualcomm.com

***Abstract*—A 14.4-GS/s 5-b ADC is designed in 40nm CMOS with eight time-interleaved channels of Flash/Successive-Approximation hybrid sub-ADCs each running at 1.6GS/s. A modified bootstrapped track-and-hold switch incorporates a global clock to synchronize the sampling instant of each individual sub-channel, therefore improving multi-phase alignment. Measurement results show that the ADC can achieve a peak SNDR of 26.5dB, consuming 49.4mW, leading to a FoM of 199fJ/conversion-step, in a core area less than 800µm by 500µm.**

***Index Terms* — ADC, time-interleaving, track and hold, SAR**

I. Introduction

Multi-GS/s ADCs have recently been proposed as promising architectures for next generation wireline applications. As the data rate continues to increase for Serial-Deserializers (SerDes) systems, channel losses continue to worsen for higher data rates, requiring equalization techniques to compensate for the dispersion and reflection. The decision feedback equalization (DFE) is widely used to subtract the inter-symbol interference (ISI) directly from the incoming analog signal via a quantized feedback finite impulse response (FIR) filter. DFE operation has been traditionally processed with analog circuits that unfortunately consume significant power overhead, as well as limited scalability towards high bandwidth and very lossy channels. Recently, architectures that implement the DFE operation in the digital domain have been proposed [1-7], using an ADC to convert the incoming analog signal to digital. Such architectures take the advantages of the increasingly powerful digital signal processing available using CMOS technology scaling, while providing the design flexibility to easily program the DFE coefficient values across a wide range of channel characteristics.

Depending on the data rates of the SerDes system, these ADC-based serial links will operate at sampling rates from 10GS/s and up to 100GS/s. For those ADCs running above 20GS/s [1, 2], a small number (i.e. less than 16) of time-interleaved channels are employed, with each individual channel further time-interleaving multiple successive-approximation (SAR) ADCs to meet the high-speed, low-power requirements. On the other hand, for ADCs operating below 20GS/s [3-6], the number of sub-channels is usually chosen to be 4 or 8, simplifying the multi-phase clock generator design. Furthermore, the flash structure is commonly selected for the sub-channel ADC (sub-ADC) due to its simplistic ability to operate at high sampling rates.

Two issues exist for the time interleaved ADC architecture as mentioned above. First, the sampling instants of the multi-phase clocks for the time-interleaved track-and-hold (T/H) circuits must be evenly spaced, to avoid timing skew mismatch between sub-channels, degrading the ADC's dynamic performance at high input signal frequencies. Hence accurate phase calibration, including the timing error detector and precision phase interpolator (PI), are critical to minimize any harmonic spurs. Second, to achieve a total sampling rate above 10GS/s with only a few channels, each sub-ADC is also required to operate at a high speed. The traditional sub-ADC structure using a Flash suffers from large power consumption, large silicon area, and large capacitive loading to the preceding stage, preventing its practical utility in time-interleaved ADCs.

This work proposes two novel techniques to address the issues described above. First, this ADC introduces a sampling instant synchronization technique to reduce the timing skew problem between multiple distributed T/H, consuming little power/area overhead. Second, it replaces a conventional Flash sub-ADC with a high-speed power-efficient hybrid structure consisting of a 2-bit Flash and a 3-bit asynchronous-SAR with improved feedback loop.

II. Proposed Architecture

The proposed T/H architecture (Figure 1) is inspired by employing a global clock phase to determine the sampling instant for each individual channel, so as to reduce the issue of phase skew matching between multiple sub-ADCs. As shown in Fig. 1, an 8-channel time-interleaved ADC is proposed, with a global sine-wave clock applied to each individual T/H switch to synchronize the sampling instants. Each switch is not only controlled by one of the multi-phase clocks $ck[i]$, but also synchronized by the highest-frequency (f_s) sine-wave clock. Hence, the sampling instant when the input signal is sampled on to the loading capacitors $C_L[i]$ is defined by the global clock *sin*, such that there is minimal static phase error between each individual T/H channel. The sub-channel clocks $ck[i]$ only determine the moments that each T/H channel starts the tracking phase, such that each sub-channel's phase accuracy

This work was funded and supported by LSI Corporation.

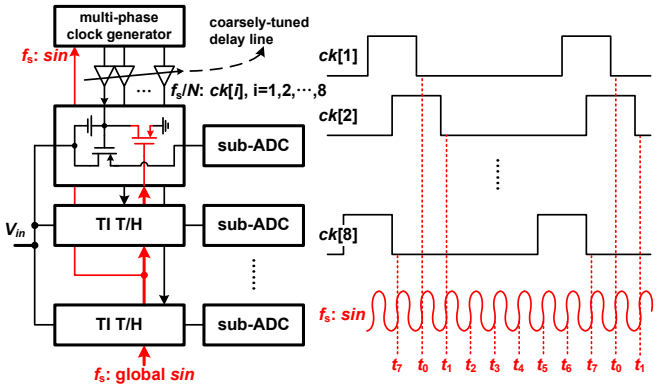

Fig. 1. Proposed distributed time-interleaved T/H with a global sine clock.

requirement is significantly relaxed as long as its tracking duration is sufficient.

In addition, the sine-wave clock is directly generated from a clean sinusoidal source through a single CML, and therefore exhibits smaller dynamic timing uncertainty as supply-induced jitter is reduced. The duty cycle of each individual sub-clock is 1/4 so that at any particular moment only two of the eight channels are connected to the front-end, reducing the capacitive loading seen at the ADC input.

III. Circuit Implementation

A. Track-and-Hold Circuit

To implement the T/H function described in Fig. 1 above, a bootstrapped switch modified from [8] is utilized, where the discharge path connects the gate of the pass transistor M_0 to ground in order to turn it OFF (Fig. 2). During the tracking phase when $ck[i]$ is high, the bootstrapped switch operates normally, with the gate-source voltage of M_0 equal to the constant voltage difference previously stored across the internal capacitor C_0. The NMOS transistor M_1 and its

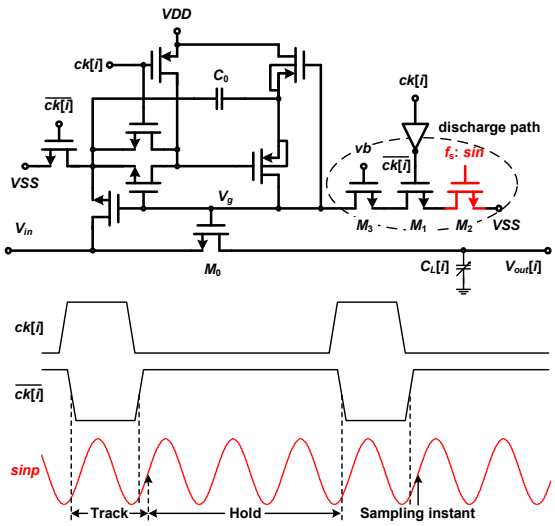

Fig. 2. Modified track-and-hold switch with synchronizing sampling instants.

complementary clock $ck[i]$, is in series with transistor M_2 and its global clock *sin*. The transistor M_0 will be shorted to ground only after both the complementary $ck[i]$ and the global *sin* reach the threshold to turn ON transistors M_1 and M_2, respectively. If the moment when clock *sin* turns ON transistor M_2 occurs after the instant complementary clock $ck[i]$ turns ON transistor M_1, the sampling instant will be defined by the global clock signal *sin* instead of the multi-phase clocks $ck[i]$. The end result is that the sampling instants of all T/H channels are identically synchronized to the global *sin* clock, regardless of any static timing errors between the multi-phase clocks. Therefore, only coarse phase delay is required for the multi-phase clocks, which eases the clock generator design. Furthermore, since the source of M_2 is connected to ground, signal-dependent sampling distortion is also avoided.

To verify that the SNDR of the time-interleaved ADC is not affected by static timing errors in the multi-phase clocks for each individual sub-channel, an experiment is performed. Two sub-channels spaced by 180 degrees apart are selected, with the phases of these two $ck[i]$'s deliberately shifted from the ideal position by a different amount of delay. The measured SNDRs across the entire phase range are shown in Fig. 3, where the phase range is represented by the number of loading capacitors connected into the digitally-controlled delay line, with a unit step size of approximately 1ps. The plane of SNDRs with different static phase delays between sub-channels is relatively flat, showing that such phase misalignments do not greatly affect the SNDR performance of this proposed ADC.

B. Multi-Phase Clock Generation and Distribution

Instead of using a single phase of a sine wave clock with a frequency of f_s (as denoted in Fig. 1), differential phases of a sine wave clock source at a frequency of $f_s/2$ is employed for the odd and the even numbered channels, respectively. The half-frequency clock needed for global synchronization is generated by routing an external off-chip clock with an RMS jitter of around 800fs into an on-chip CML buffer. The CML buffer employs thick-gate transistors and operates under a 1.8V supply, such that its output sine-wave signal is near rail-to-rail for the 1V operation of other blocks in the clock portion. The 8-phase clock generator is designed using a flip-flop loop. A

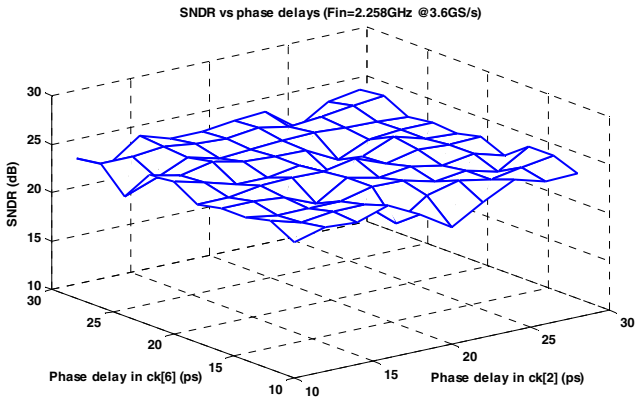

Fig. 3. Combined SNDR vs phase delays in two opposite channels.

true single phase clock structure (TSPC) is used for the flip-flop circuit to ensure high enough speed. The phase of each sub-channel clock can be tuned coarsely using a digitally-programmable delay line.

C. Sub-Channel ADC Design

1) Flash-SAR Hybrid Structure

To expedite the conversion speed of the sub-ADC, a hybrid structure with a 2-bit Flash and 3-bit asynchronous SAR is proposed (Fig. 4). The 2-bit Flash converts the first two bits simultaneously, requiring only one more comparator than a conventional 2-bit SAR. These three comparators compare the differential input signal with the reference levels of $-1/2V_{FS}$, 0 and $1/2V_{FS}$, where V_{FS} is the maximum absolute value of the differential input signal. Their outputs are fed into a capacitive network (C_{array1}) to generate a reference voltage ref_1, whose possible values are $\pm1/4V_{FS}$ and $\pm3/4V_{FS}$, for the subsequent SAR conversion. The 3-bit asynchronous SA, using the same architecture as in [9], is triggered upon the completion of the 2-bit Flash. The 3 comparators in the SAR compare the input signal with the sum of ref_1 and ref_2 successively, where ref_2 is generated by a binary SAR capacitive DAC (C_{array2}) and can have reference values of $\pm1/16V_{FS}$, $\pm1/8V_{FS}$, and $\pm3/16V_{FS}$, depending on the corresponding comparator decisions.

2) Comparator design

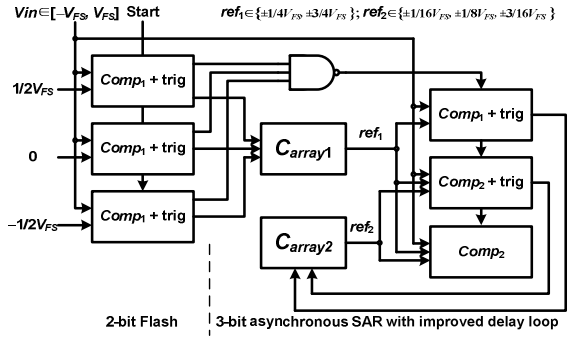

Fig. 4. The Flash-SA hybrid structure of the sub-ADC.

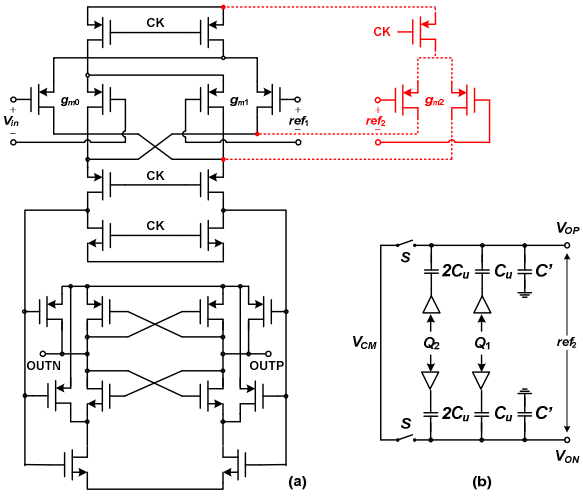

Fig. 5. Schematic of (a) the proposed comparator; (b) the cap-DAC C_{array2}.

A dynamic double-tail latch-type comparator [10] is shown in Fig. 5(a), with only one phase clock used. As illustrated in Fig. 3, two different topologies are used. The one used for the 2-bit Flash and the MSB of the 3-bit SAR ($Comp_1$) has two input pairs, comparing the input differential signal with only one reference voltage. The other comparator used for the remaining bits of the SAR ($Comp_2$) has three input pairs, comparing the signal with the sum of ref_1 and ref_2.

For comparator $Comp_2$, the transconductance (g_m) variation of the input pairs across the entire dynamic range need to be carefully considered. The reason is as follows: in the proposed dynamic comparator, the differential outputs that are both precharged to the supply voltage will start to discharge on the clock's falling edge, at a rate associated with the transconductance current described by the input pairs. Therefore, the relationship between V_{in} and the sum of ref_1 and ref_2 is actually determined by comparing each differential pair's voltage-induced currents, requiring that each differential pair's g_m's is the same.

However, the large-signal G_m of the first-stage differential pair of the comparator can vary greatly with the differential input voltage values [11]. While V_{in} and ref_1 are usually close in value after the first 2-bits of comparison, and the values of g_{m0} and g_{m1} are also close and can vary in a large range, the absolute value of ref_2 is always smaller than $1/4V_{FS}$ and g_{m2} is always large. Therefore, when V_{in} and ref_1 are not in the center of the curve, the induced transconductance currents cannot reflect the real relationship between the voltages. This nonlinearity needs to be compensated for by utilizing a piecewise voltage prescaling for ref_2. As g_{m2} cannot be changed, a smaller ref_2 can be generated by increasing the C' value in C_{array2} (Fig. 5(b)) accordingly.

IV. Measurement Results

The time-interleaved ADC is fabricated in 40nm CMOS process, occupying a total active area of 800µm by 500µm, as is shown in Fig. 6.

The output waveforms of each sub-ADC are separately collected from the oscilloscope, digitized and then combined in a time-interleaved manner in Matlab to reconstruct the overall spectral output. The FFT spectra of the time-interleaved ADC running at 14.4GS/s with input signal frequencies near DC and at around 2.3GHz are shown in Fig. 7. The SNDRs of the time-interleaved ADC running at 8GS/s, 10GS/s, 12GS/s and 14.4GS/s with different input frequencies are plotted in Fig. 8.

One imperfection in this design was discovered during testing, requiring improvements in the future: there is SNDR loss at low input frequencies, which is the result of uncompensated offset in the comparator due to g_m variation. Although as previously discussed, the transconductance nonlinearity can be compensated by using reference voltage prescaling, varying g_m introduces an unpredictable offset voltage that cannot be always cancelled using foreground calibration. To improve linearity, source degeneration can be introduced into the tail node of the first comparator.

V. CONCLUSION

The proposed T/H integrates an additional transistor gated by a global low-jitter sine-wave clock into the time-interleaved track-and-hold, such that the sampling instant of each sub-ADC is synchronized. The proposed technique provides an energy-efficient solution for the problem of phase skews between sub-channels in time-interleaved ADCs. The ADC performance is summarized in Table I, with a comparison with previous measurement results from [5].

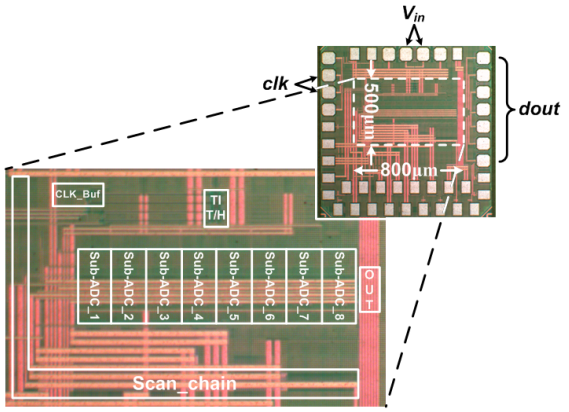

Fig. 6. Chip die photo.

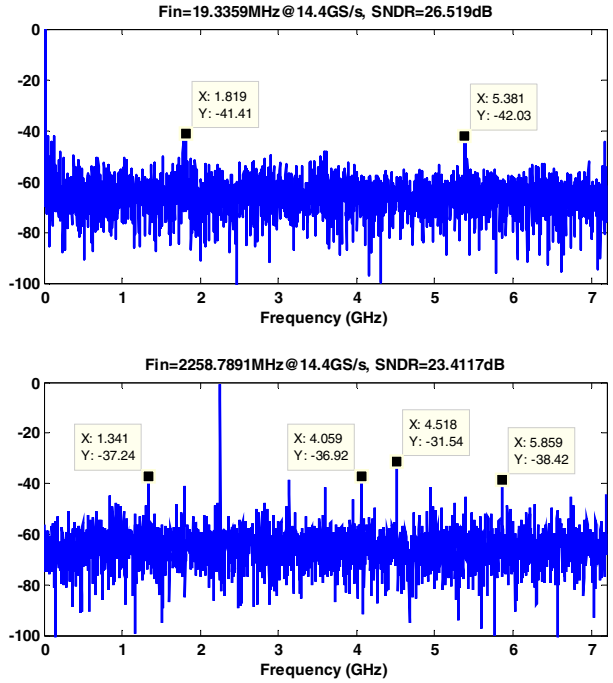

Fig. 7. FFT spectra of ADC at 14.4GS/s with F_{in}=20MHz and F_{in}= 2.26GHz.

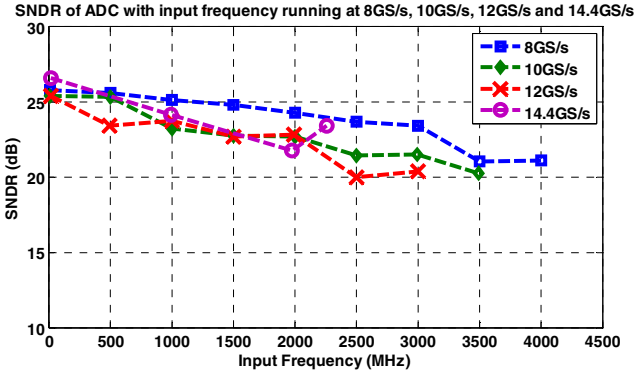

Fig. 8. SNDRs of the time-interleaved ADC versus different F_S and f_{in}.

TABLE I. ADC PERFORMANCE SUMMARY

	This work				[5]	
Technology	TSMC 40nm GP				TSMC 65nm GP	
Active Area	<0.4mm^2				0.44mm^2	
Full Scale	600 mV				590mV	
Resolution	5 bit				5bit	
VDD	1.8V for input clock buffer, 1.2V T/H				1.1V	
	0.9V digital/clock		1.2V for others			
Sample Rate	12GS/s		14.4GS/s		12GS/s	
Total Power	32.1 mW		49.4 mW			
T/H	2.9 mW		2.9 mW		81 mW excluding digital backend, clock buffer etc.	
sub-ADC	20.9 mW		29.6 mW			
Clock (w/o buffer)	8.3 mW		16.9 mW			
F_{in}	19MHz	2GHz	20MHz	2GHz	10MHz	6GHz
SNDR	25.4dB	22.8dB	26.5dB	21.8dB	27.5dB	25.1dB
FoM	176fJ/conv	237fJ/conv	199fJ/conv	341fJ/conv	350fJ/conv	460fJ/conv
T/H	Distributed time-intereleaved T/H with:					
	sampling instants synchronization				background timing skew calibration	
sub-ADC	2-bit Flash and 3-bit asynchronous SAR				5-bit Flash	

REFERENCES

[1] Y. M. Greshishchev, et al., "A 40GS/s 6b ADC in 65nm CMOS," *ISSCC Dig. Tech. Papers*, 2010, pp. 390–391.

[2] I. Dedic, "56Gs/s ADC: Enabling 100GbE," *OFC/NFOEC 2010*, pp. 1-3, Mar. 2010.

[3] M. Harwood, et al., "A 12.5 Gb/s SerDes in 65 nm CMOS using a baud-rate ADC with digital receiver equalization and clock recovery," *ISSCC Dig. Tech. Papers*, 2007, pp. 436–437.

[4] J. Cao, et al., "A 500 mW ADC-Based CMOS AFE With Digital Calibration for 10 Gb/s Serial Links Over KR-Backplane and Multimode Fiber," *IEEE JSSC*, vol. 45, no. 6, pp. 1172-1185, Jun. 2010.

[5] M. El-Chammas and B. Murmann, "A 12-GS/s 81-mW 5-bit time-interleaved flash ADC with background timing skew calibration," *IEEE JSSC*, vol. 46, no. 4, pp. 838-847, Apr. 2011.

[6] B. Zhang, et al., "A 195mW / 55mW Dual-Path Receiver AFE for Multistandard 8.5-to-11.5 Gb/s Serial Links in 40nm CMOS," *ISSCC Dig. Tech. Papers*, 2013, pp. 34-35.

[7] E.-H. Chen, R. Yousry, and C.-K. K. Yang, "Power Optimized ADC-Based Serial Link Receiver," *IEEE JSSC*, vol. 47, no. 4, pp. 938-951, Apr. 2012.

[8] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio ΔΣ modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE JSSC*, vol. 36, no. 3, pp. 349-355, Mar. 2001.

[9] T. Jiang, et al., "A Single-Channel, 1.25-GS/s, 6-bit, 6.08-mW Asynchronous Successive-Approximation ADC With Improved Feedback Delay in 40-nm CMOS," *IEEE JSSC*, vol. 47, no. 10, pp. 2444-2453, Oct. 2012.

[10] M. Miyahara, Y. Asada, D. Paik and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2008, pp. 269–272.

[11] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001, pp. 107–109.