A 1-GSPS 6-bit 2b/step SAR ADC in 130 nm CMOS

By,

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For

EECT 7327 Data converters

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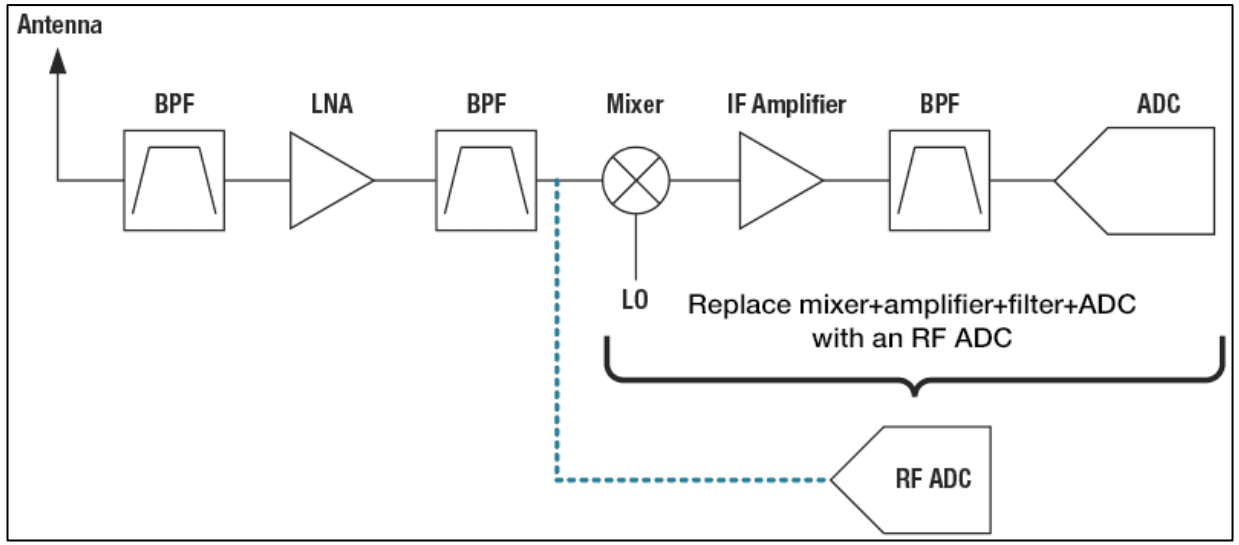
Agenda

- Limitations of conventional SAR and flash ADCs
- Synthesis of a multi-bit conversion SAR ADC
- System level design
- Design of analog blocks
  - Comparator
  - Capacitor network
  - Buffer
  - Track-and-hold amplifier
- Design of SAR logic
- Results

Limitations of conventional ADCs

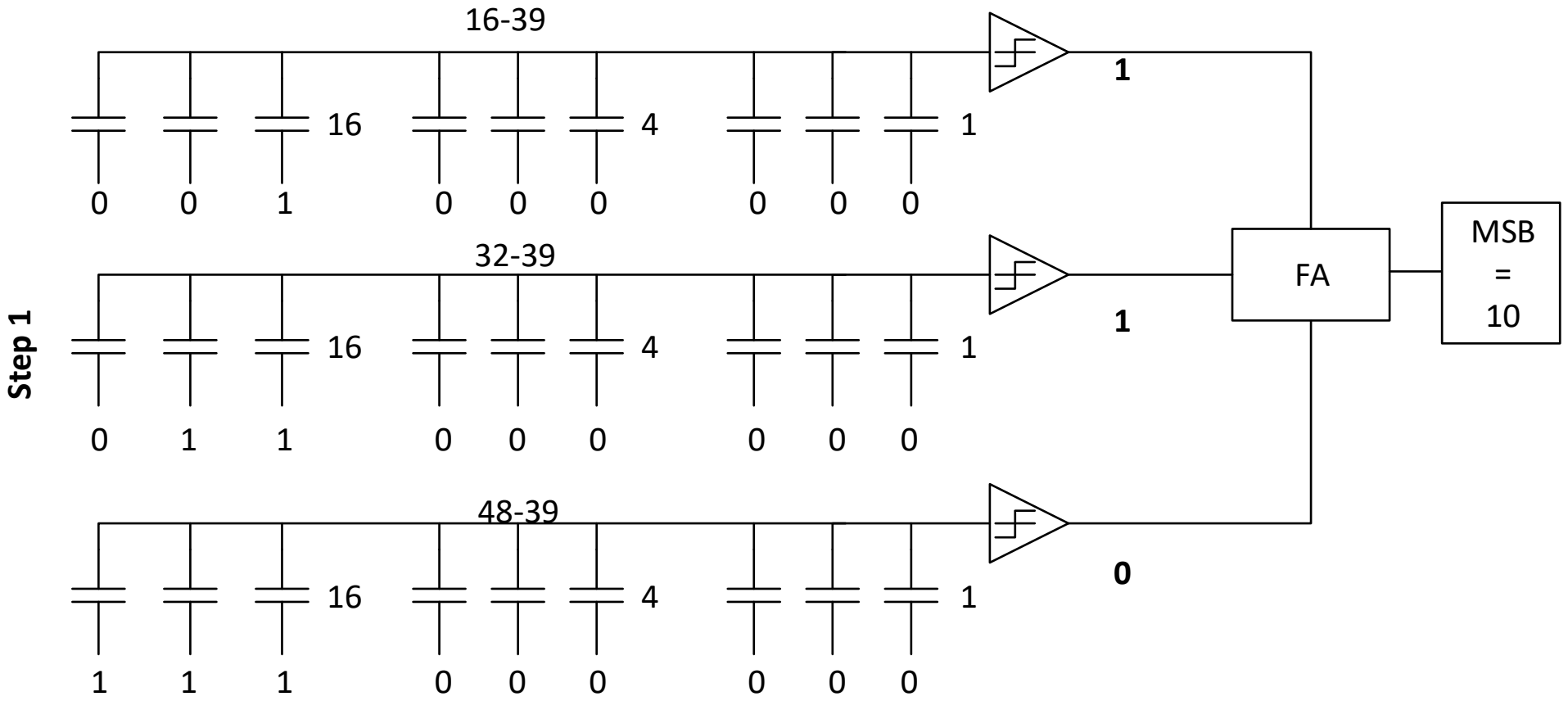


- Modern RF systems require a high speed ADC for miniaturization
- Need low power, small footprint ADCs for portable applications

Limitations of conventional ADCs

Performance metric	Flash ADC	SAR ADC
Static power consumption	High, 2^N (preamplifiers + R string)	Low, 1 digitally assisted comparator
Conversion rate	N bits per conversion	1 bit per conversion
Die area	Large, 2^N (preamplifiers+ R string)	Small, depends on digital circuitry

A new multi-bit conversion scheme



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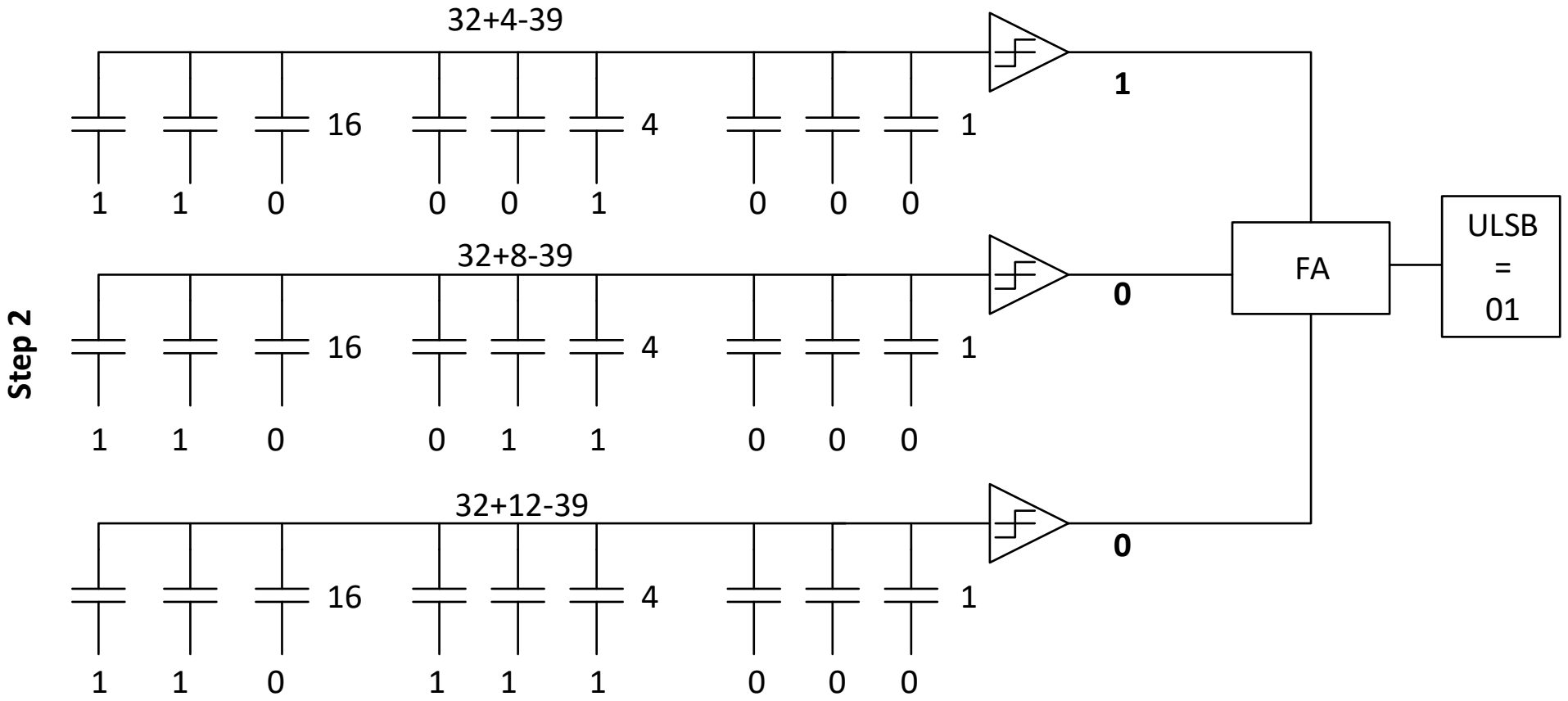

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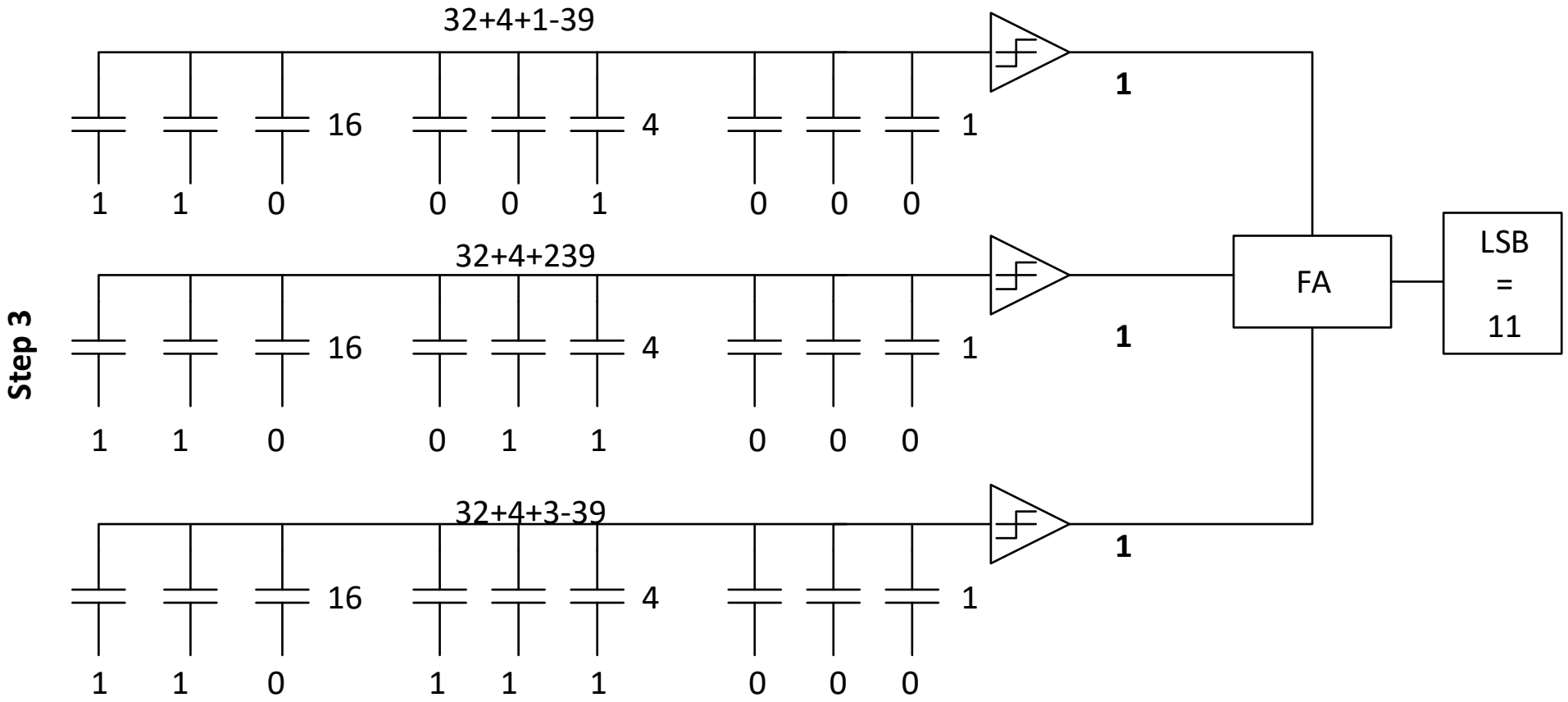
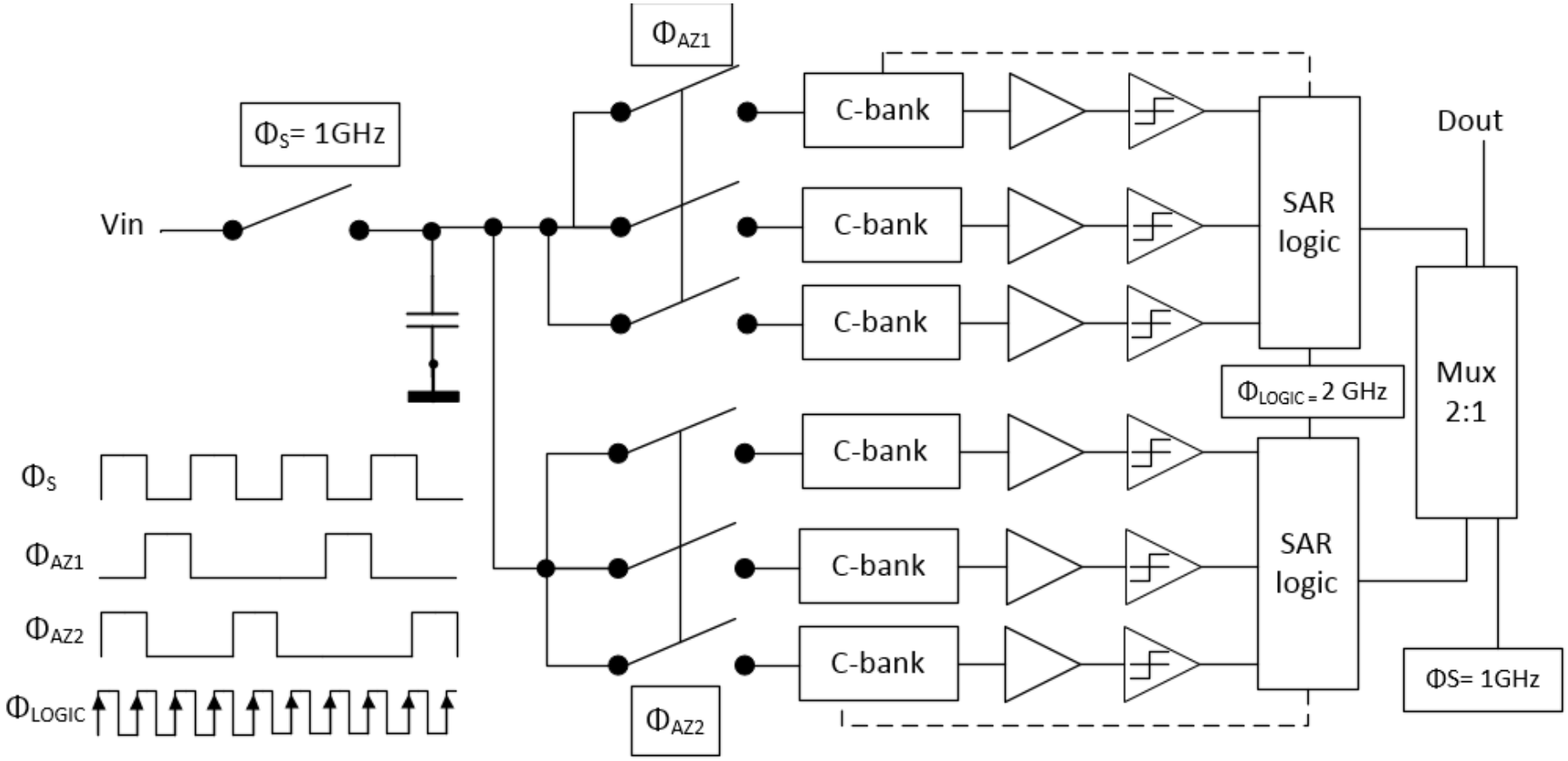
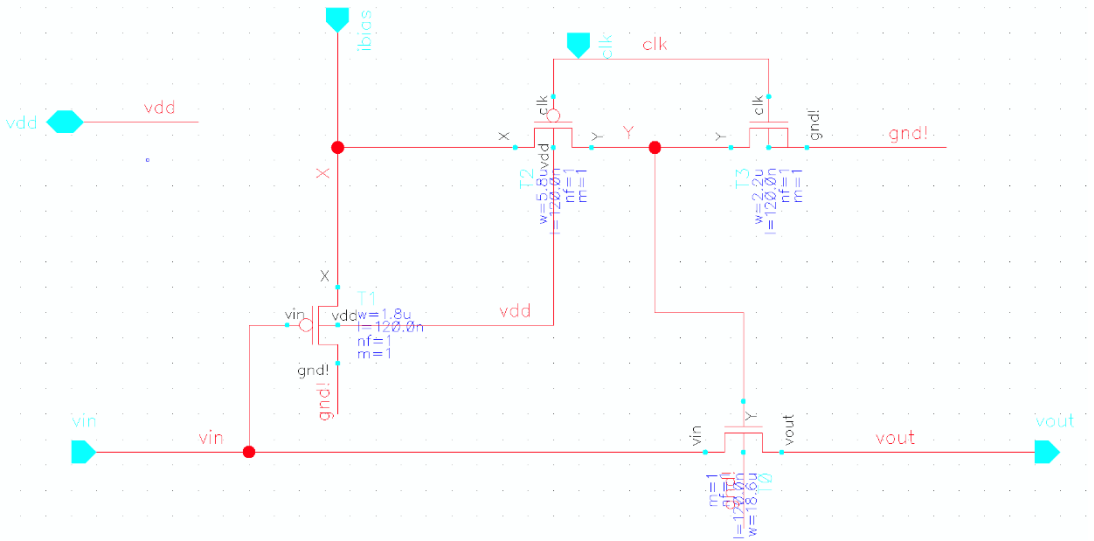
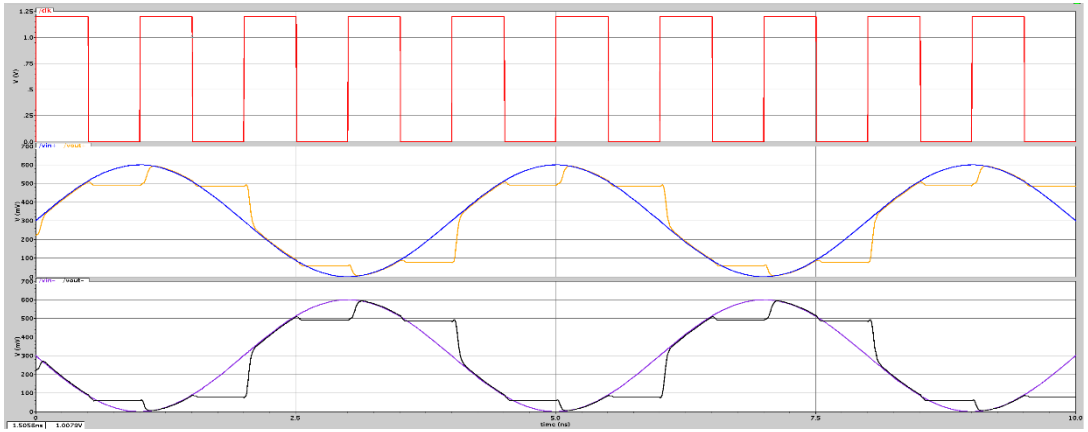


System level block diagram



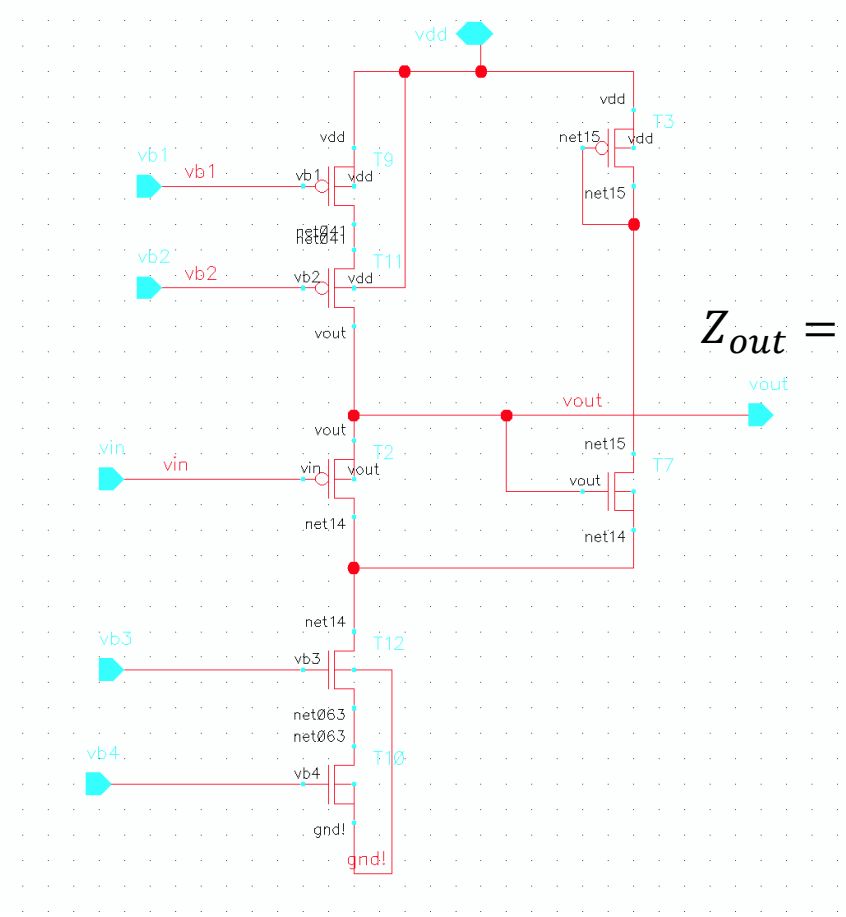
Sample-and-hold Circuit



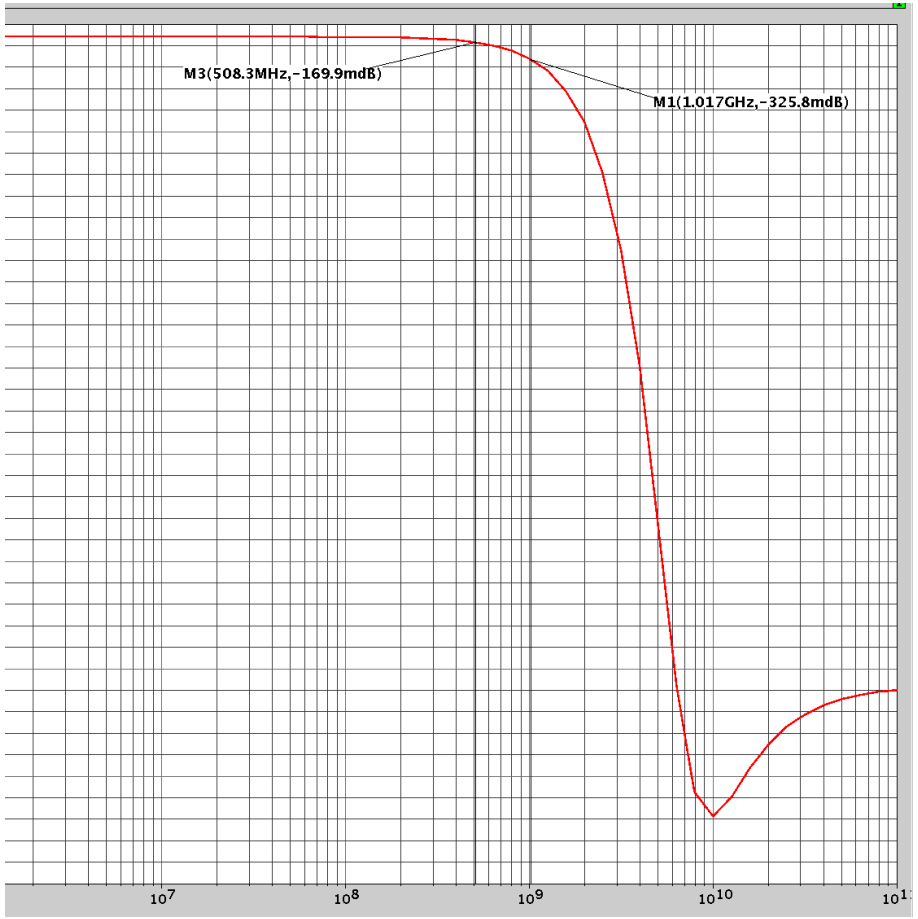


- Differential track-and-hold circuit using bootstrapped switch to avoid signal feedthrough
- Sampling frequency = 1 GHz

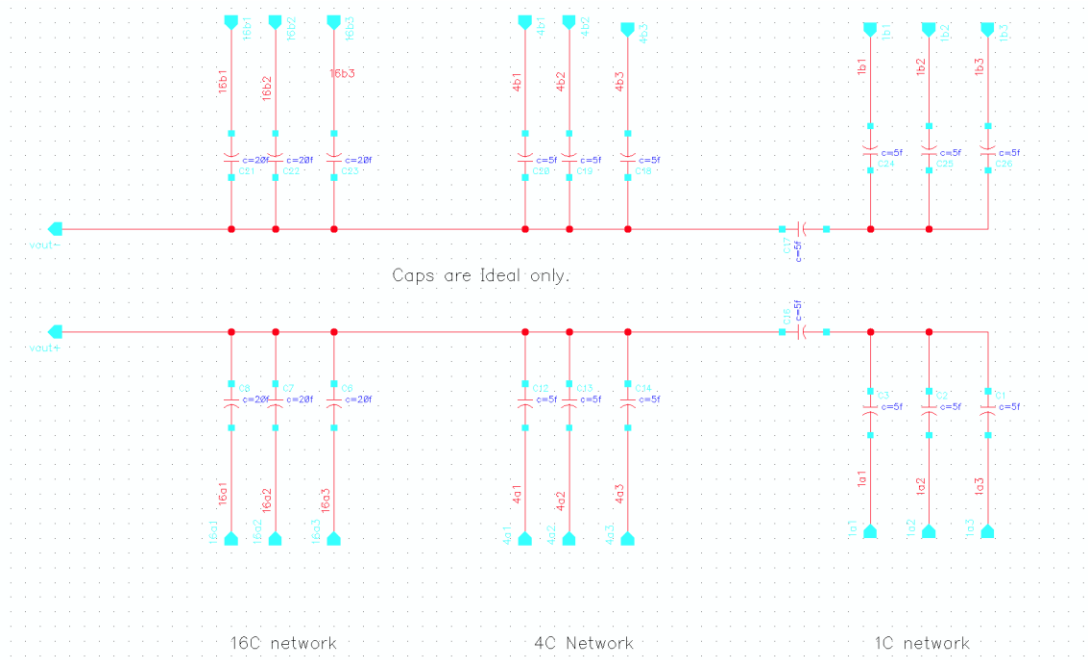
Buffer: super source follower



$$Z_{out} = \frac{1}{g_{m2} r o_2 g m_7}$$

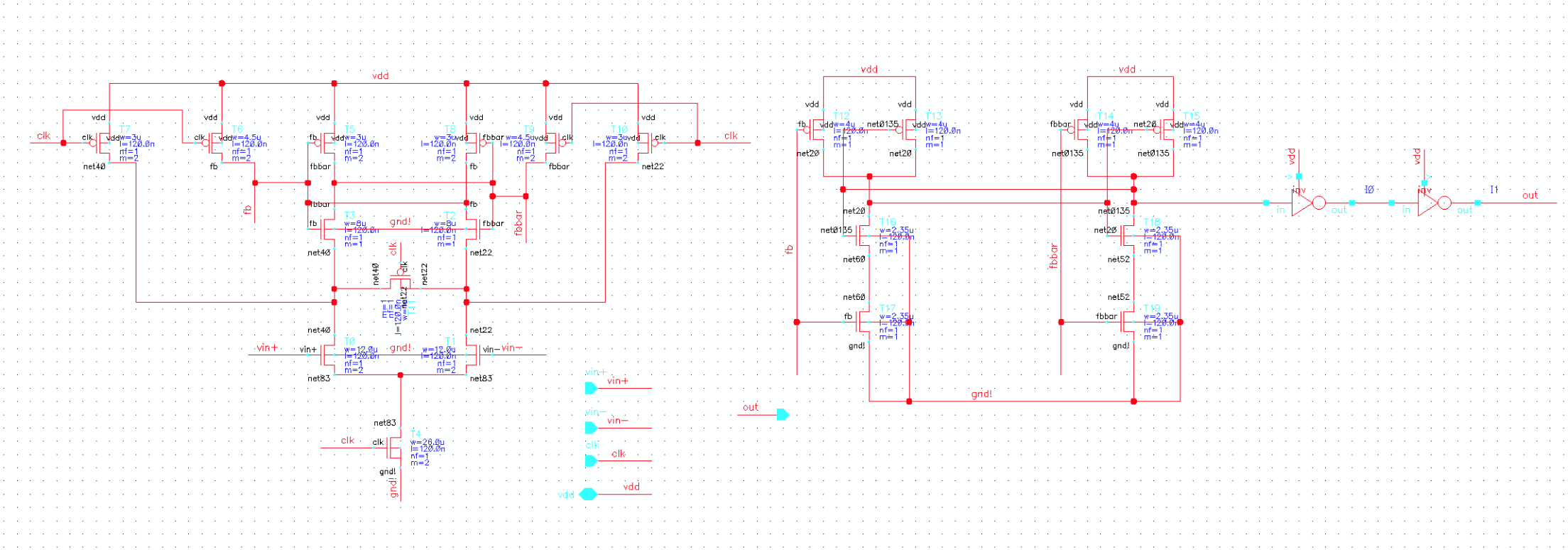


Capacitor bank



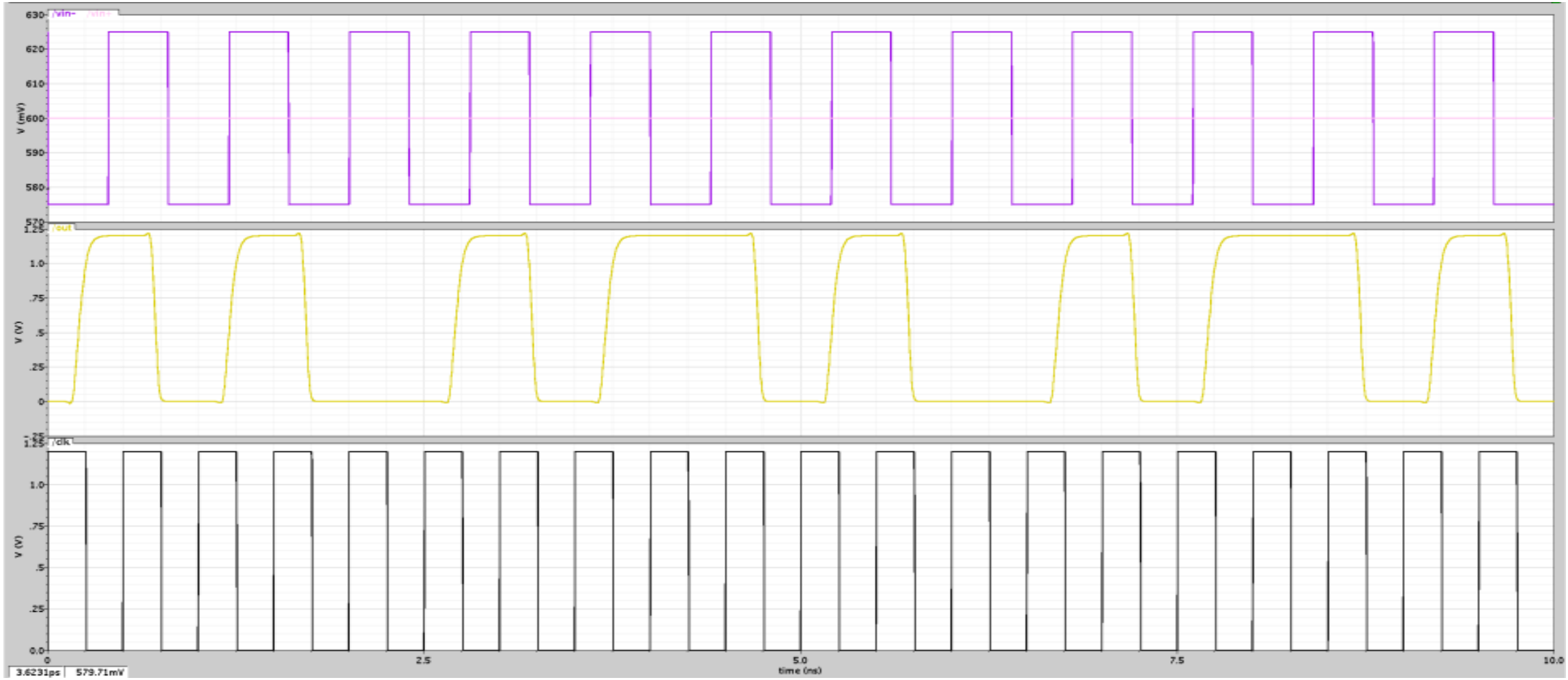
- Unit capacitance = 5fF
- Total capacitance per pin = 240fF
- Can be laid out in metal layers M4-M5-M6 as MIM capacitor
- Allows routing for MOSFETs on lower layers

Comparator

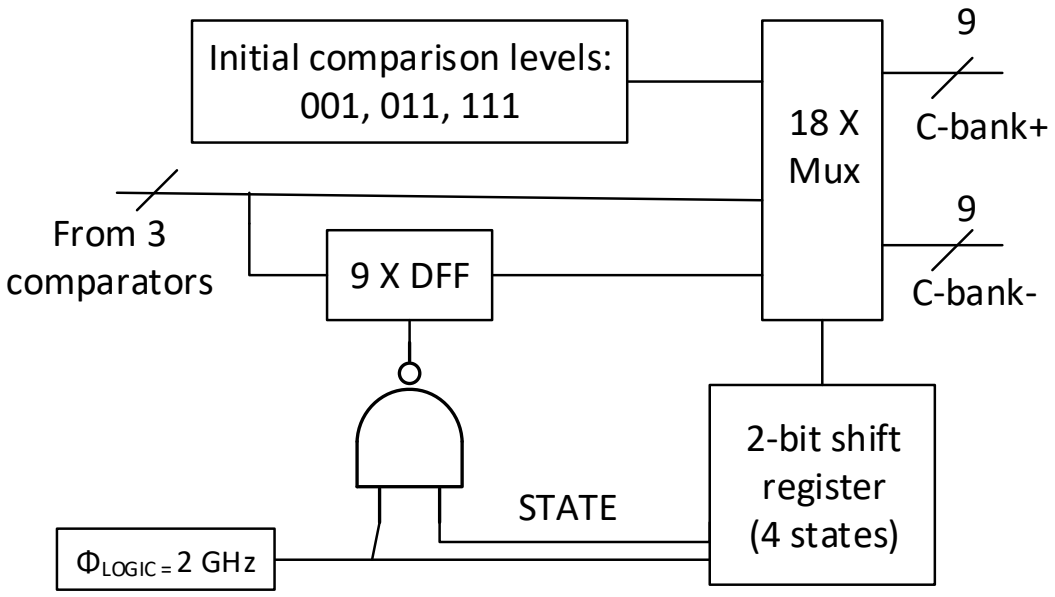


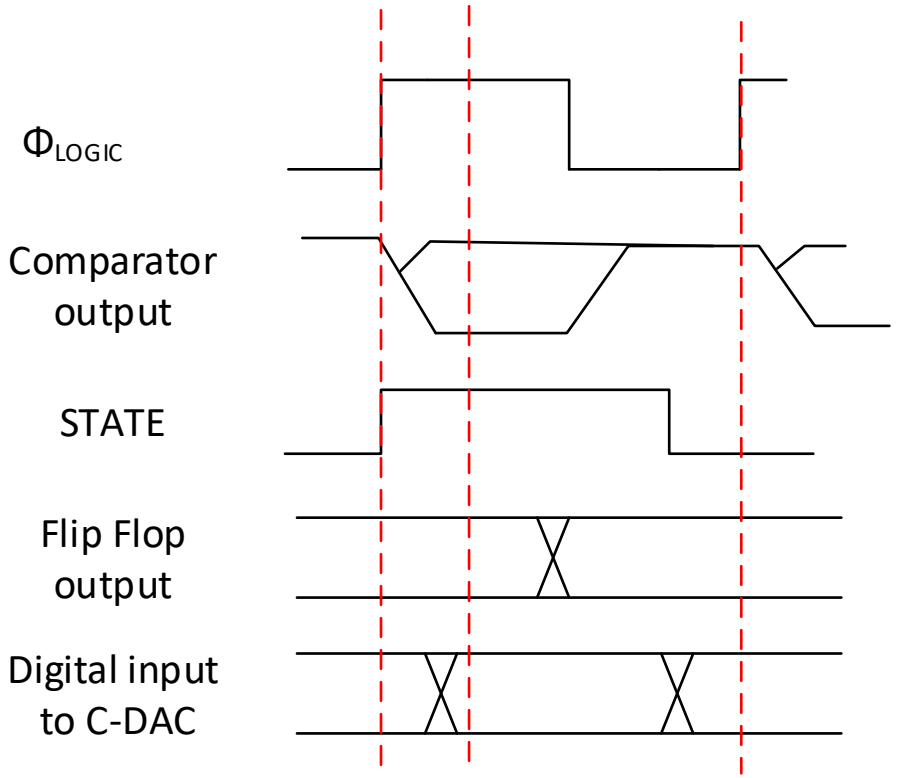
- Positive Edge Triggered Hysteresis Comparator
- NAND Gate output Latch to hold the decision until the next latch edge.
- Dynamic Current consumption of less than **900 µA**.

Comparator Output

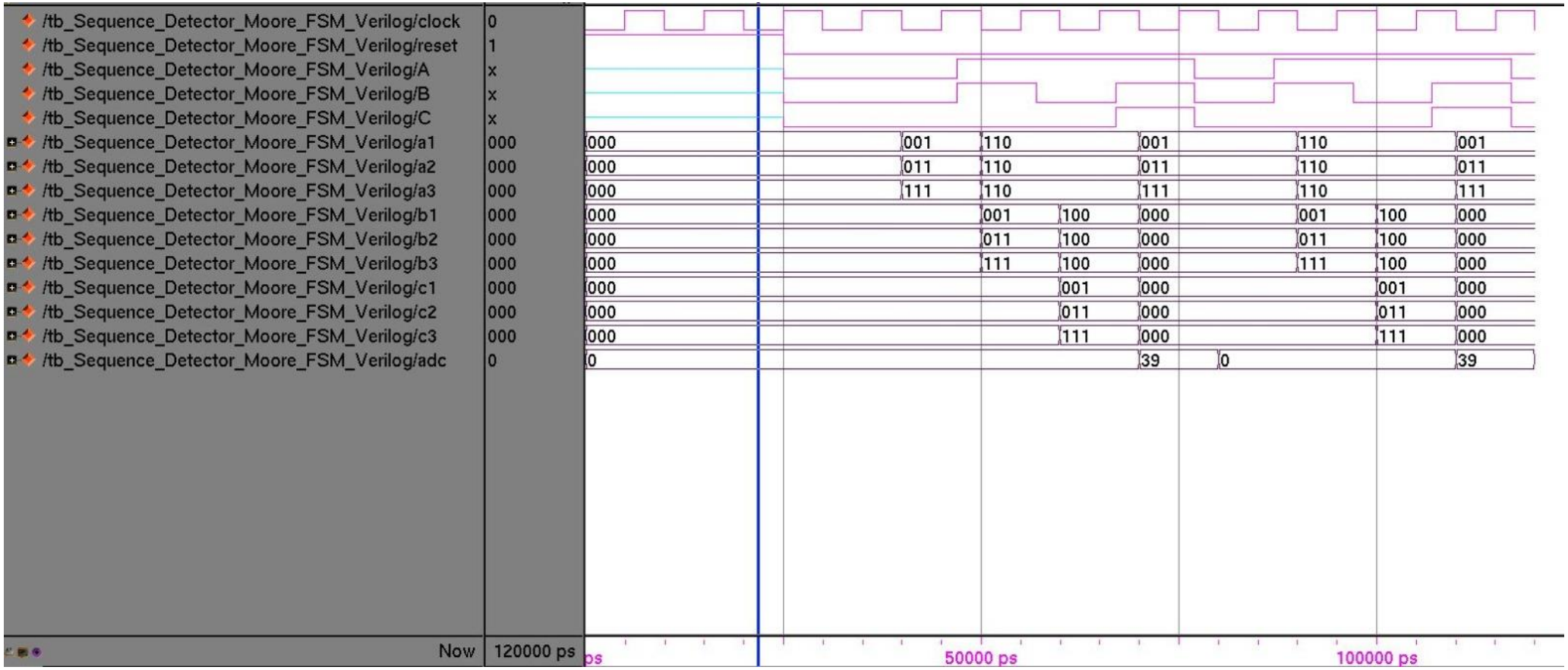


Flip-Flop Bypass SAR Logic

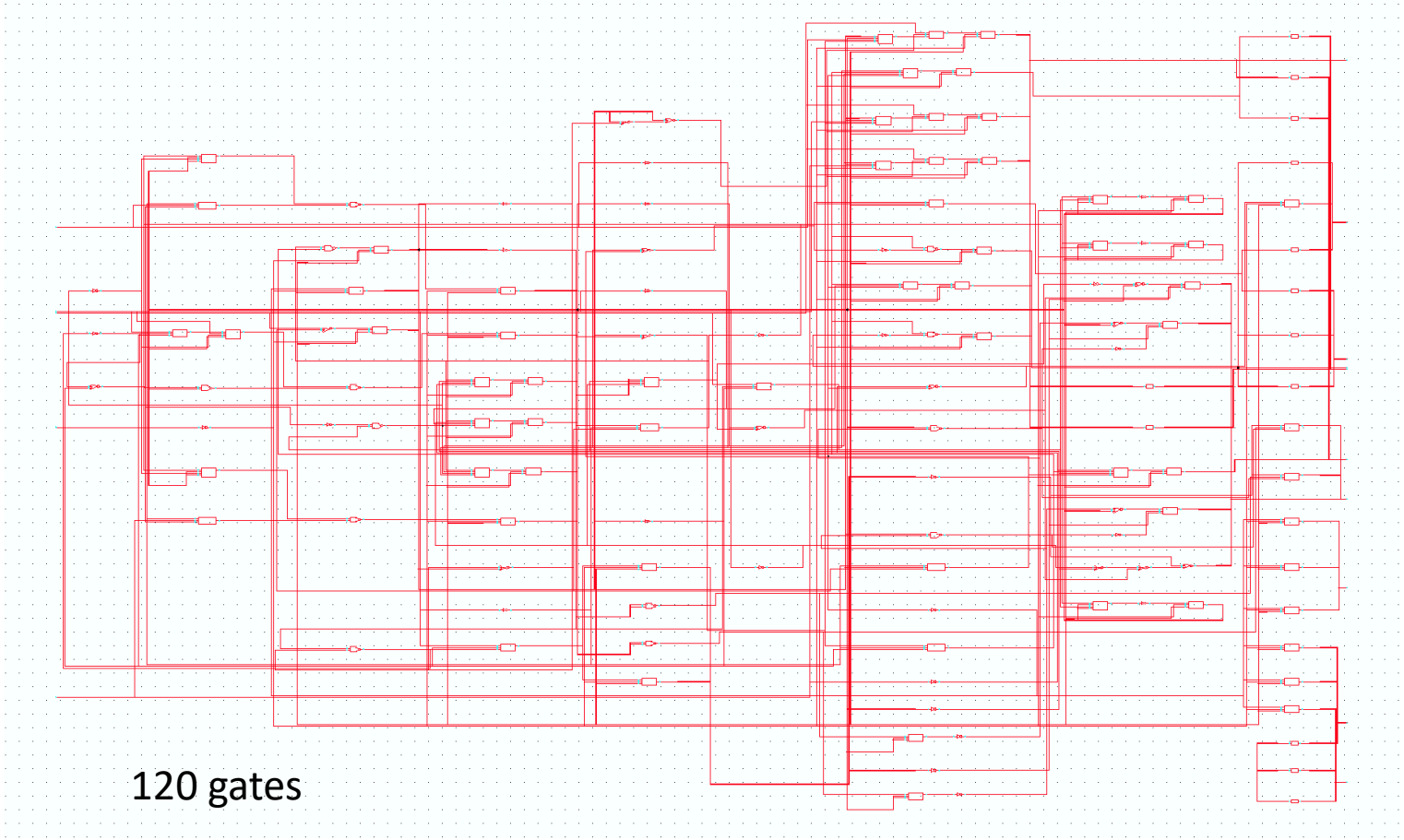




SAR Logic behavioral synthesis



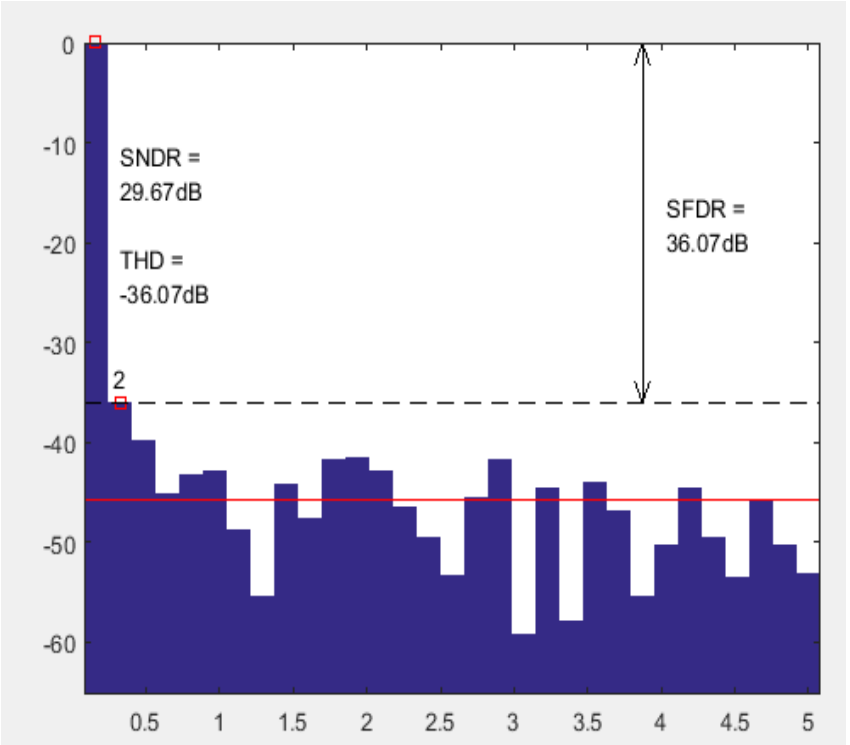
SAR Logic netlist



120 gates

Performance summary

Technology	IBM 130nm
Resolution	6 bits
Input Range	1.2 Vpp Differential
Sampling Frequency	1 GHz
Latency	Approx. 2 clock cycle (2ns)
ENOB	4.6 @ 1 GS/s, f_{in}=265.625MHz 4.3 @ 1 GS/s, f_{in}=500MHz
Power Consumption	<50mW
Input Capacitance	<200fF on each side
Walden FOM	1.29 pJ/conversion @ f_{in}=265.625 MHz 1.827 pJ/conversion @ @ f_{in}=500 MHz



Questions?