An All-Digital PWM-Based ΔΣ ADC with an Inherently Matched Multi-bit Quantizer

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Abstract — An all-digital PWM-based delta-sigma (ΔΣ) ADC is proposed. This system takes advantages of the duration of a pulse, rather than voltage or current, as the analog operand used in its closed-loop operation. Unlike VCO-based ADCs, this ADC as a linear input sampling stage with adequate uncalibrated performance. Furthermore, the architecture allows inherently matched multi-bit quantizer/DAC blocks by taking advantage of delay lines reusable in both quantization and DAC operation. A 3-bit prototype of this ADC in 0.18 µm CMOS process is implemented, tested, and presented. With an OSR of 72 and a bandwidth of 1 MHz, it achieves a dynamic range of 51 dB and SNDR of 49.6 dB while consuming 1.5 mA from a 1.8 V supply. The core occupies an area of 0.0275 mm^2.

Index Terms — Analog-to-digital converter, delta-sigma modulation, time-to-digital converter, VCO-based ADCs, pulse-width modulation, digital-to-time converter.

I. Introduction

Conventional data converter (ADC) architectures face major implementation challenges in advanced (and mostly digital) CMOS technology nodes [1]. One recent trend to alleviate such difficulties is to shift voltage-domain analog processing into the time-domain to take better advantage of the power-efficient and scalable digital circuits: time-based [2] and voltage-controlled oscillator-based ADCs [3]. A time-domain ADC architecture that implements pulse width modulator (PWM) and time-to-digital converter (TDC) in feedback loop is presented [4]. This architecture improves the linearity of PWM. However, major analog blocks (integrator and filter) are required for the noise shaping. The VCO based ADCs provide inherent noise-shaping properties and can operate at low supply voltages and high sampling rates. However, these are suffered from the nonlinear voltage-to-phase transfer characteristics. Background calibration or digital post-correction is necessary to compensate [3][5].

In this paper, we present an all-digital PWM-based ΔΣ ADC. In this system, an input voltage is converted to pulse width and is subsequently processed in an all-digital ΔΣ modulator that processes pulse width. The advantages of this architecture are: 1) its matched multi-bit quantizer and feedback DAC through an identical delay line structure, and 2) adequate uncalibrated performance due to its inherently linear operation.

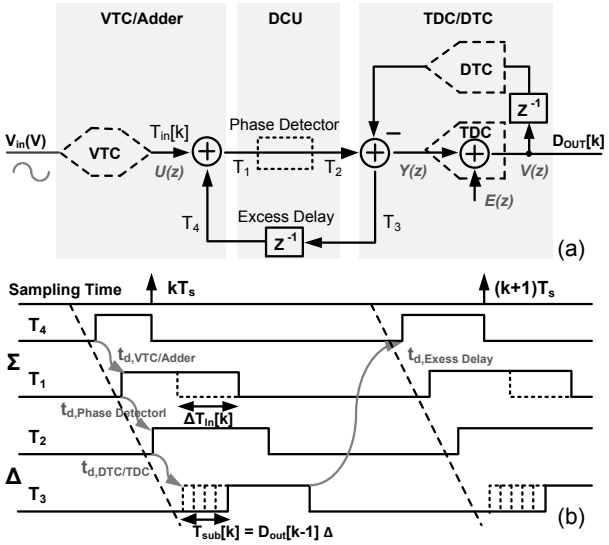

Fig. 1. (a) Architecture and (b) timing diagram of the PWM-based ADC. VTC = voltage-to-time converter, DCU = delay control unit, TDC = time-to-digital converter, DTC = digital-to-time converter

II. PWM-Base Modulator Architecture

The concept of the PWM-based ΔΣ modulator is shown in Fig. 1(a). The analog operand in this architecture is $T_{1:4}[k]$, the "pulse width", an asynchronous pulse that is circulating within a delay loop while addition("Σ" operation) and subtraction ("Δ" operation) are executed based on the average frequency of f_s , the oversampling frequency. The basic operations necessary to implement the ADC are: addition, subtraction, and conversion from voltage to time, from time to digital and digital to time. These operations are described in the following sections.

A. Addition and Subtraction in the Time-Domain

Analog time-domain processing using pulse width as the analog quantity is shown in Fig. 2. To add two pulses, T_{in} and T_{add}, as depicted in Fig. 2(a), we align the start of T_{add} to the end of T_{in}. Then the sum of the pulse widths is the pulse T_{out} that begins with T_{in} and ends with T_{add}.

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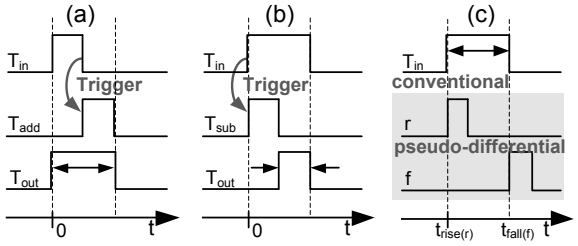

Fig. 2. (a) Addition (b) Subtraction (c) Pseudo-differential pulse in time-domain using pulse widths

Subtraction, depicted in Fig. 2(b), requires aligning the start of T_{sub} with that of Tin. The result of subtraction is the pulse T_{out} which begins when T_{sub} ends, and ends when T_{in} ends. Aligning pulses in the manner described requires a triggering mechanism (and asynchronous digital circuits) which will be explained in detail.

B. Pseudo-Differential Pulses

Normally, a digital pulse consists of a signal that transitions high then low. The "width" of a conventional pulse is the time duration between the rise and fall transitions as shown in Fig. 2(c). For both accuracy and robustness, pseudo-differential pulses are often preferred. A pseudo-differential pair of pulses (r, f) as shown in Fig. 2(c), encodes pulse width in the time duration between the rise transition of r and that of f. The advantages of pseudo-differential pulses for encoding analog quantities are twofold: 1) By encoding information in the rise-to-rise delay rather than rise-to-fall delay, errors due to skewed low to high vs. high-to-low propagation delays are eliminated, and 2) this encoding removes the restriction on minimum pulse widths due to vanishing pulses.

With respect to pseudo-differential pulses, it is clear how pulse widths can be added and subtracted. If two pulses are appropriately aligned, adding a pulse to another is achieved by simply delaying the f pulse of the output. Similarly, to subtract two pulses aligned with their r pulses, only the output r pulse needs to be delayed. Assuming the pulses can be thusly aligned, time-based pulse width addition and subtraction can be implemented using simple digital logic gates.

C. Modulator Topology

The proposed PWM-based ΔΣ ADC architecture is shown in Fig. 1(a). It comprises three major blocks: 1) VTC/Adder, 2) Delay Control Unit (DCU), and 3) Time-to-Digital Converter/Digital-to-Time Converter. The conceptual timing diagram depicted in Fig. 1(b) shows conventional pulses for brevity. however, pseudo-differential pulses are used throughout the rest of this paper. The topology of the modulator is first order error feedback. The system equations are the following:

$$\begin{aligned} \mathrm{V(z)} &= \mathrm{Y(z)} + \mathrm{E(z)} \\ &= U(z) + Z^{-1}Y(z) - Z^{-1}V(z) + E(z) \\ &= U(z) + E(z) - Z^{-1}\big(V(z) - Y(z)\big) \\ &= U(z) + (1 - Z^{-1})E(z) \end{aligned} \quad (1)$$

III. CIRCUIT IMPLEMENT

The circuit topology of the VTC/Adder is shown in Fig. 4(a). The ramp generator consists of a wide-swing current source (I_B = 200μA), an integrating capacitance (C_I = 110fF), and digital switches to create a 0 to 640ps full scale $T_{\mathrm{in}}[k]$ corresponding to a (0.28V-0.68V) linear range of V_{in} with V_{ref} = 0.28V. The continuous-time comparator is a PMOS-input folded-cascode differential amplifier with a buffered output stage. The fixed overall latency is 2.10 ns ($t_{\mathrm{d,VTC/Adder}}$). The complete system showing all the components together is shown in Fig. 4.

A. Voltage-to-Time Converter (VTC)/Adder

The addition as well as the preceding voltage-to-time conversion operation shown in the system model shown in Fig. 1, is performed by the VTC/Adder block. At every cycle, the VTC/Adder conceptually adds its input pulse T_{in} (T_4 in Fig. 1(b)) to the pulse width which is proportional to $V_{in} - V_{\mathrm{ref}}$. The result is T_{out} (or T_1 in Fig. 1(b)). Both the input and output pulses are pseudo-differential pulses (r_{in} , f_{in}) and (r_{out}, f_{out}). To implement the voltage-to-time conversion and addition, two identical half-circuits are used as shown in Fig. 3. The identical circuits have a ramp generator and a continuous time comparator. With the rise of r_{in} , the first ramp generator is triggered. Once its output ramp crosses

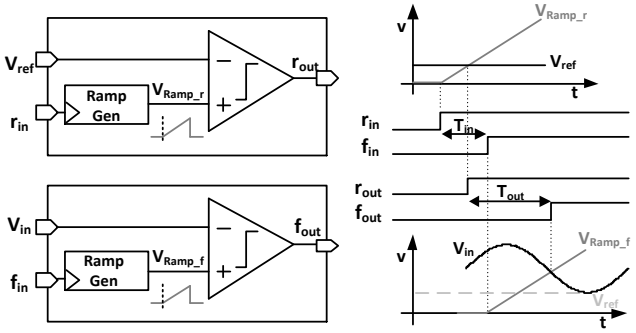

Fig. 3. Block diagram and timing diagram of the VTC/Adder

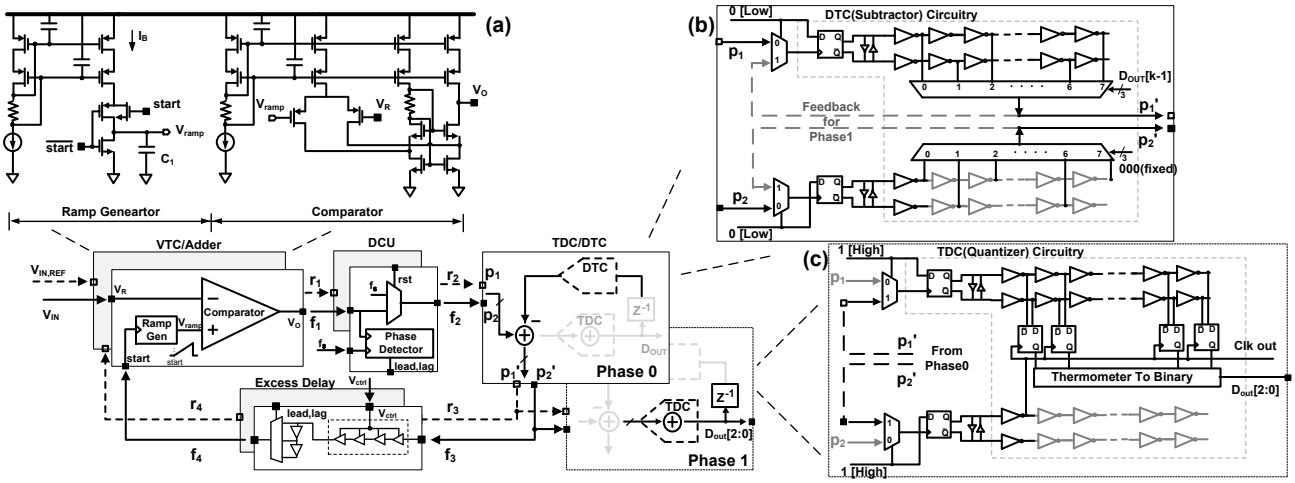

Fig. 4. Complete PWM-based ΔΣ ADC System (a) VTC/Adder circuit showing ramp generator and comparator (b) Digital-to-time converter (DTC) phase (phase 0) of the DTC/TDC (c) Time-to-digital converter (TDC) phase (phase 1) of the DTC/TDC circuit. Note the reuse of the unit delay elements from the previous phase (DTC)

the reference voltage (V_{ref}), the comparator outputs a pulse on r_{out}. Naturally, there is some delay associated with each operation ($t_{\mathrm{d,VTC/Adder}}$). Next, with the rise of f_{in}, the second ramp generator is triggered .The resulting ramp is now compared with the instantaneous value of the input voltage (V_{in}). Larger values of V_{in} result in larger delay from ramp triggering (f_{in}) to comparator output (f_{out}). This delay should be linearly proportional to V_{in} in addition to some fixed delay. Given the pseudo-differential architecture, the common-mode delay ($t_{\mathrm{d,VTC/Adder}}$) is canceled and thus the output pulse width $[t_{\mathrm{rise}}(f_{\mathrm{out}}) - t_{\mathrm{rise}}(r_{\mathrm{out}})]$ is the sum of input pulse width $[t_{\mathrm{rise}}(f_{\mathrm{in}}) - t_{\mathrm{rise}}(r_{\mathrm{in}})]$ and a pulse width proportional to $V_{\mathrm{in}} - V_{\mathrm{ref}}$.

B. Delay Control Unit (DCU)

The main responsibilities of the DCU are to properly startup the loop after global reset and prevent unwanted pulse drifts through dynamically adjusting the excess loop delay. Since sampling in the VTC/Adder is triggered by the f pulse, for a uniform sampling period of T_{s}, the phase detector compares the f pulses at each cycle with the rising edge of a clock with frequency $f_{\mathrm{s}} = 1/T_{\mathrm{s}}$. This activates either a lead or lag signal that is then applied to the excess delay block of the modulator to increase or decrease the loop delay of both r and f pulses through the excess delay block. Referring to Fig. 1, in each cycle, the DCU adjusts the delay of the excess delay to ensure:

$$T_s = t_{d,VTC/Adder} + t_{d,Phase\ Detector} = t_{d,DTC} + t_{d,Excess\ Delay} \quad (2)$$

With just two bits (lead, and lag) the DCU adjusts the excess delay by ±400ps in each cycle. This is in addition to a programmable fixed delay for a wide tuning range of f_{s}. By using this approach, one can ensure that the average oversampling frequency is always locked to an external f_{s} clock which is 144 MHz in the prototype implementation (~7 ns average loop delay). It is important to recognize that the fluctuation in the sampling time of this PWM-based ADC does create errors that are similar in nature to noise artifacts generated by noisy clocks. After releasing the global reset signal, the DCU provides an initial zero-width pseudo-differential pulse to startup the circuit. In normal mode, DCU passes through the input pulse to the output with a constant amount of delay ($t_{\mathrm{d,Phase\ Detector}}$) in Fig. 4.

C. Digital-to-Time/Time-to-Digital Converter

The DTC/TDC block performs the functions of both the ADC and the DAC in the first-order delta-sigma error feedback only structure shown in Fig. 4. Multi-bit delta-sigma is sensitive to mismatch between the ADC and the DAC in regular (voltage-based) ADCs. The unit delay array (with fixed time interval) is the common block both the ADC and the DAC in time-domain. If the operation of these functions can be performed sequentially, then those blocks may be shared. Thus, a reusable structure of multi-bit subtraction and quantization can save area and reduce the effects of mismatch. This novel merged ADC/DAC is possible thanks to time domain processing, not possible in voltage-domain processing.

The DTC/TDC works in two phases. In phase 0(DTC),

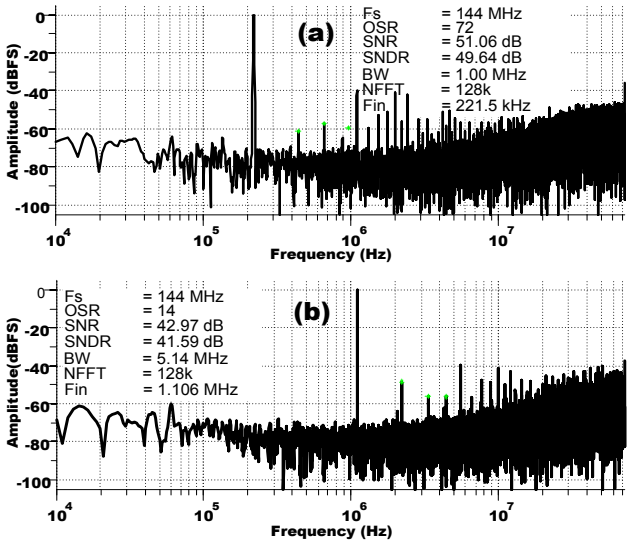

Fig. 5. (a) Magnitude FFT spectrum of a 221.5 kHz sinusoid with OSR = 72. (b) 1.106 MHz with OSR = 14

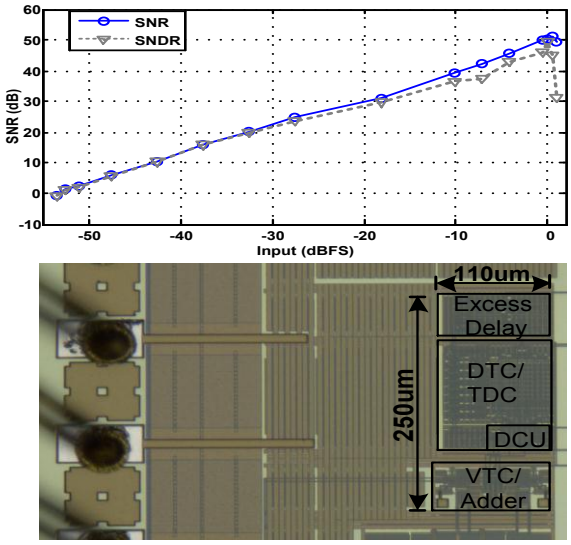

Fig. 6. Dynamic range plot for 221.5 kHz sinusoid, OSR = 72 and Die photo

the block performs time-based subtraction by delaying the *r* pulse by a number of LSB time-units (from the phase 1 output of the previous cycle), which is shown in Fig. 4(b). The resulting pulse is output to the excess delay block and also recirculates through the DTC/TDC for phase 1 (TDC). The same unit delay elements are used in conjunction with flip-flops that implement the time based quantizer shown in Fig. 4(c). Both the DTC and the TDC are 3-bits in this implementation.

IV. Measurement Results

A prototype of the proposed structure was fabricated in a 0.18 µm CMOS process (1.8V, 6M, 1P) in a total area of 110 µm x 250 µm = 0.0275mm^2. The chip micrograph in Fig. 6 outlines the floorplan including the various blocks. The total power consumption is 2.7 mW using a 1.8V supply, where 2.52 mW is consumed by the VTC/Adder and the rest of the digital core consumes merely 180 µW.

Fig. 5(a) shows the measured output spectrum of the ADC for a 400 mV pk-pk (0 dBFS) and 221.5 kHz sinusoidal input converted with an oversampling frequency of fs = 144 MHz FFT length of 128K is used to generate the plot with a 7-term Blackman-Harris window. With OSR = 72, and BW = 1 MHz, SNR and SNDR were measured to be 51.1 dB and 49.6 dB, respectively. 2nd, 3rd and 4th harmonics are all less than -57 dBc without any calibration. Fig. 5(b) shows the measured output spectrum with OSR = 14, BW = 5.14MHz, with a 0 dBFS 1.106 MHz sinusoid with measured SNR = 43dB and SNDR = 41.6 dB.

V. Conclusion

The PWM-based ΔΣ ADC was proposed and a test chip fabricated. The results show a promising architecture that can take advantage of the increasingly higher timing resolution in nanometer scale process nodes. Advantages of this architecture are its simplicity, inherent multi-bit error matching between ADC/DAC, and small area. Compared to other time-based architectures, the proposed architecture is inherently linear and can achieve 8+ bit resolution, without necessarily rely on calibration schemes to remove large systematic nonlinearities. The bottleneck of linearity is the VTC/Adder in this block, which can improve if calibrated.

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