EE 6330 RFIC Design **Spring 2016**
Design Project **Due Date: 04/28/16**

Design and layout a low noise amplifier with the following specification. You should minimize the power consumption while meeting the specification. Be sure to include bonding pads in your layout (80 μm x80 μm, spacing between the pads should be 80 μm. It will be supplied by the TA) as well as including the parasitics associated with the Bond Pads in your design. You should also include parasitic inductance associated with the package. You should integrate as much of the amplifier as possible. However, it may not be possible to integrate everything.

LNA Specifications:

Operating Frequency	**:**	**2.4-2.5 GHz**
G_T	**:**	**> 12 dB**
Γ_{in}	**:**	**Less than -10 dB**
Γ_{out}	**:**	**Less than -10 dB**
V_{DD}	**:**	**1.1 ~ 1.3 V**
IIP_3 (input)	**:**	**> -7 dBm**
Noise Figure (50 Ω)	**:**	**< 2.0 dB**

Model and Process Parameters:

Use the 130-nm MOS transistor model.

For the C_{JS} estimation for MOS capacitors, use the junction capacitance data for the polysilicon-to-n-well capacitors.

C_{JO} (area) = 1.0×10^{-8} F/cm^2

C_{JO} (perimeter) = 2.0×10^{-12}F/cm

ϕ_b= 0.6 V (area, perimeter)

m_J = 0.5 (area, perimeter).

Substrate resistance: 150 Ω for 200 μm x 200 μm n-well area. Assume that the resistance scales inversely with the n-well area.

Package

8-pin package discussed in class.

Off chip components

Capacitors: 10, 20, 30 .... 200 pF. Q at 1 GHz is 50. Parasitic series inductance is 0.6 nH.

Inductors: 2, 4, 6, 8, .. 30 nH. Q at 2.5 GHz is 50.

Variability

On-chip components:

Capacitances associated with transistors: +/- 10%

On-chip inductor: +/- 3%

MOS capacitors: +/- 10%

External components: +/- 10%.

Report Format

The report should include

1. Circuit Description.

2. Layout Description and philosophies behind the layout.

3. Bonding diagram of the IC.

4. Instructions for how the circuit should be used. You may need external components.

5. Initial Hand/Matlab Analysis of Your Circuit

6. Parasitic Extraction/Estimation

7. Circuit Simulation Results

8. Comparison between Hand/Matlab Analyses and Simulation Results

9. Variability analysis

10. Conclusion/Summary.