Design Solutions for Sample-and-Hold Circuits in CMOS Nanometer Technologies

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***Abstract*—Solutions for the design of low-voltage sample-and-hold (S/H) circuits in CMOS nanometer technologies are presented. As a design example, a 0.8-V supply S/H is designed and simulated using a 130-nm CMOS process. It dissipates 0.5 mW at dc and provides almost a rail-to-rail signal swing. When clocked at 40 MS/s and with a 1.4-V_{PP} differential input signal, the simulated spurious-free dynamic range, signal-to-noise ratio, and total harmonic distortion are 57, 67, and −56 dB (9 equivalent bits), respectively, with low sensitivity to supply, temperature, process, and mismatch variations. The proposed solution employs a three-stage low-voltage amplifier without a tail current source in the differential pair and a switch topology, which combines clock voltage doubling and dummy switches.**

***Index Terms*—Bootstrapped switch, nested Miller compensation, sample-and-hold (S/H), very low voltage circuits.**

I. Introduction

TO LIMIT power consumption, the supply voltage of portable systems is scaling down to values that are becoming lower than 1 V. However, to avoid excessive leakage currents, the threshold voltage of CMOS devices does not scale down as quickly as the supply voltage. This reduces the signal headroom of analog circuit sections. In addition, the intrinsic gain of CMOS devices decreases with process scaling [1], and to achieve high open-loop gains, cascading of several gain stages becomes necessary in nanoscale technologies [2]–[4]. In this context, the design of mixed-signal fundamental blocks, such as sample-and-hold (S/H) circuits [5], becomes a challenging task. Indeed, after examining one of the most popular and robust S/H topologies, namely, the *flip-around* architecture shown in Fig. 1, one can realize that both the operational amplifier and the switches require high-performance solutions to operate under reduced voltage swings and with devices providing a low intrinsic gain.

In this brief, we present the design and simulation results of an S/H circuit based on the topology shown in Fig. 1, implemented in a 130-nm CMOS process and operating under a 0.8-V supply. It uses a three-stage fully differential operational amplifier to provide adequate gain and linearity. Each gain stage of the amplifier exploits a novel differential-cell topology that avoids the tail current generator of the conventional differential pair, thus minimizing the supply demand while maximizing the signal swing. In addition, a modification of the clock voltage doubler switch is included to reduce nonideal effects.

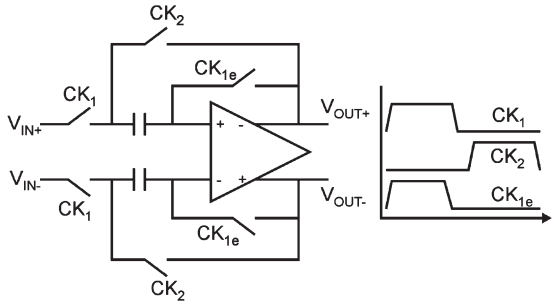

Fig. 1. S/H flip-around architecture.

Section II describes the S/H architecture, along with the adopted operational amplifier and switch topologies. Section III presents the simulation results, showing also the robustness of the solution against process tolerances. Section IV compares the obtained results with those reported in the literature. Section V summarizes the authors' conclusions.

II. S/H Circuit

A. Architecture

Our target is to design an S/H circuit operating under a supply voltage given by two MOS thresholds and achieving a 40-MS/s sampling frequency with an effective number of bits (ENOB) larger than 9 bits in the first Nyquist band.

The proposed implementation is based on the conventional flip-around architecture shown in Fig. 1. Correlated double sampling [5] has been exploited to reduce the offset and flicker noise.

B. Fully Differential Operational Amplifier

Owing to the progressive increase of the MOS small-signal output conductance, the voltage gain of a single-stage amplifier implemented in nanoscale technologies is becoming unsatisfactorily low, whereas nonlinearity and noise increase [1]. To achieve a high gain in a low-voltage design, the adoption of multistage amplifier topologies is the most viable solution; in addition, to maximize the signal swing, simple gain stages should be adopted. For this purpose, many sub-1-V design techniques have been proposed, including body-driven and subthreshold approaches [6]–[8]. However, to ensure applicability

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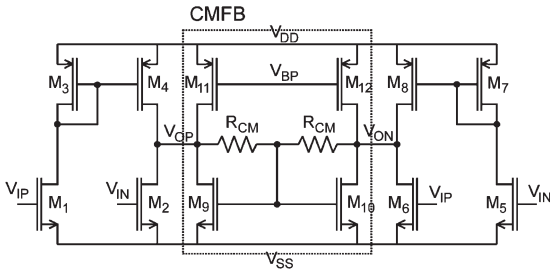

Fig. 2. Schematic diagram of the differential gain cell.

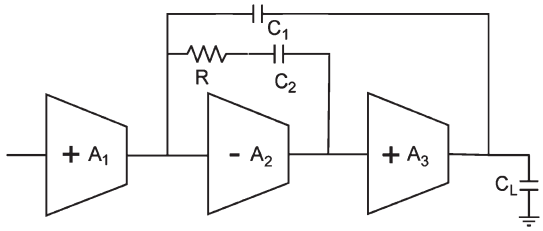

Fig. 3. Amplifier architecture with RNM compensation (single-ended version).

to switched-capacitor circuits (required by the S/H circuit in Fig. 1), body driving should be avoided, as it does not provide a purely capacitive input impedance. Moreover, to guarantee adequate bandwidth, strong inversion biasing should be preferred over weak inversion.

In the proposed implementation, we adopt an approach that allows the design of sub-1-V gain stages (and differential pair cells, in particular) with no tail current source. The basic gain cell is illustrated in Fig. 2 and is similar to that originally adopted by the authors in [9] to implement a two-stage operational transconductance amplifier. The gain cell is made up of two pseudodifferential pairs M_1-M_2 and M_5-M_6 with active loads M_3-M_4 and M_7-M_8. The outputs of these two symmetrical stages are connected to the central structure, made up of M_9-M_{12} and $R_{\rm CM}$, which acts as the common-mode feedback (CMFB) loop. Due to the symmetry of the topology, the voltage at the common node of the two resistors $R_{\rm CM}$ follows the output common-mode voltage signal while remaining at virtual ground for differential input signals. In this manner, the dc output voltage is equal to $V_{\rm GS9,10}$ and is set by current generators $M_{11}-M_{12}$ and the aspect ratio of M_9-M_{10}. High-value resistors have to be used for the common-mode sensing network to avoid limiting the differential gain of the stage and the signal swing. In our design, 100-kΩ resistors ($R_{\rm CM}$) have been implemented as high-resistivity polyresistors, which are usually available in advanced CMOS technologies.

More specifically, if we consider the differential and common-mode input components $v_{i,\rm dm}$ and $v_{i,\rm cm}$, respectively, the single-ended voltage at the noninverting output is given by

$$v_{\rm op} \approx \left(g_{m1}\frac{g_{m4}}{g_{m3}} + g_{m2}\right) r_{\rm op}\frac{v_{i,\rm dm}}{2} + \left(g_{m1}\frac{g_{m4}}{g_{m3}} - g_{m2}\right)\frac{1}{g_{m9}} v_{i,\rm cm}. \quad (1)$$

Therefore, under perfect matching ($g_{m1} = g_{m2},\ g_{m3} = g_{m4}$), the circuit provides an overall differential gain that is equal to $2g_{m1}r_{\rm op}$, which is similar to that of a conventional differential stage. Ideally, the common-mode gain is zero. A finite value is, however, expected because of the process tolerances. A careful layout style should hence be adopted to ensure that the common-mode gain remains substantially lower than 0 dB at all frequencies, thereby avoiding stability problems. As a result of this brief analysis, the cell in Fig. 2 behaves as *truly differential* (and not as pseudodifferential).

Another interesting feature of the proposed circuit is that it allows easy cascading of additional stages with the same topology, providing an inherent input common-mode control (mandatory in a differential cell with no tail current generator). Indeed, when cascading several stages, the CMFB section of the previous stage also sets the bias current of the following, because the input devices of the latter form a current mirror with the NMOS devices in the CMFB of the former. In addition, the CMFB section of the last stage also sets the common-mode input voltage of the first stage through the overall feedback connection.

To achieve a sufficient gain, a three-stage amplifier was adopted. The architecture is shown in Fig. 3. Each gain stage is the one already shown in Fig. 2, and the adopted frequency compensation scheme is the reversed nested Miller (RNM). A single nulling resistor has been used to improve the step response of the amplifier, optimizing the frequency response in a way similar to [4].

Denoting by G_i and A_i the transconductance gain and the voltage gain of the ith stage, respectively, and by C_L the output capacitance, we write the expression of the loop gain, after some straightforward approximations, as

$$F(s) = \frac{v_{\rm OUT}(s)}{v_{\rm IN}(s)} = -A_1A_2A_3\frac{1}{1+s\frac{A_1A_2A_3C_1}{G_1}}\frac{N(s)}{D(s)} \quad (2)$$

where

$$N(s) = 1 + \left(C_2R - \frac{C_2}{G_2}\right)s - \frac{C_1C_2}{G_2G_3}s^2 \quad (3a)$$

$$D(s) = 1 + \left(\frac{C_LC_2}{C_1G_3} + \frac{C_2}{G_3} - \frac{C_2}{G_2} + C_2R\right)s + \frac{C_LC_2}{G_2G_3}s^2. \quad (3b)$$

The nulling resistor can improve the phase margin with respect to the standard RNM topology without increasing power consumption. Setting $G_2R_C = 1$ gives

$$N(s) = 1 - \frac{C_1C_2}{G_2G_3}s^2 \quad (4a)$$

$$D(s) = 1 + \frac{(C_L + C_1)C_2}{C_1G_3}s + \frac{C_LC_2}{G_2G_3}s^2. \quad (4b)$$

The numerator shows a positive and a negative zero at the same frequency; thus, its phase response is flat at all frequencies, whereas the gain response is flat up to $\omega_Z = G_2G_3/C_1C_2$.

The frequency of the two zeros must be set higher than the unity-gain frequency. It is possible to achieve a Butterworth frequency response (i.e., a maximally flat gain) by choosing

$$C_2 = \frac{2C_1^2G_3C_L}{G_2(C_1 + C_L)^2}. \quad (5)$$

As a result of this design procedure, we get a unity-gain frequency $\omega_{\rm GBW} = G_1/C_1$ and complex conjugate poles with

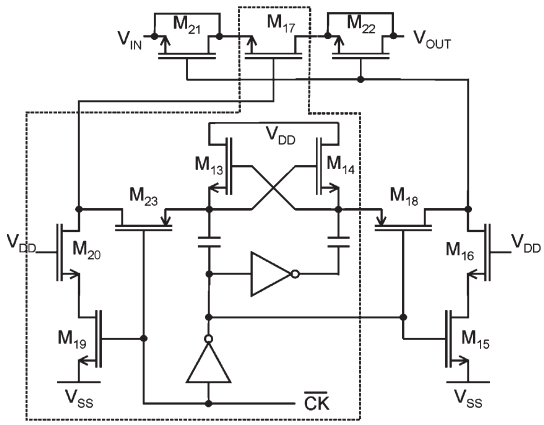

Fig. 4. Modified boosted switch topology.

a natural frequency $\omega_{\mathrm{Pn}} = G_2(C_1 + C_L)/\sqrt{2}C_L C_1$. Because the zeros have no effect on the phase margin, we can express it as a function of the ratio of ω_{Pn} and ω_{GBW}, i.e.,

$$m_\phi = \frac{\pi}{2} - \arctan\left(\frac{\sqrt{2}\omega_{\mathrm{GBW}}/\omega_{\mathrm{Pn}}}{1-(\omega_{\mathrm{GBW}}/\omega_{\mathrm{Pn}})^2}\right). \qquad (6)$$

C. Modified Boosted Switch

Both a limited supply voltage and a large-signal swing require the use of boosted-clock techniques to minimize the errors due to the switches. The adopted 130-nm CMOS technology has device threshold voltages slightly lower than 0.4 V. Thus, a 0.8-V supply voltage (about two threshold voltages) has been chosen to ensure strong inversion operation. The clock voltage has been boosted to about 1.2 V to avoid device stress since the maximum allowed gate-to-source voltage for reliable operation is 1.3 V. The standard boosted switch [5], as shown inside the dashed curve in Fig. 4, has been modified by inserting two dummy switches (M_{21} and M_{22} in Fig. 4) to minimize the principal second-order effects due to charge injection and clock feedthrough. These switches are connected at the input and output of the main switch M_{17}, and their dimensions are half that of M_{17}. In addition, the dummy switches require a boosted clock to replicate the bias point of the main switch, enabling accurate channel-charge cancellation, and this is obtained by exploiting the idle branch of the voltage doubler.

III. Simulations

Simulation results are obtained with Spectre using a 130-nm CMOS technology from STMicroelectronics. The supply voltage is 0.8 V. The main circuit blocks (the operational amplifier and the boosted switch) and the overall S/H circuit are evaluated. Monte Carlo simulations have also been performed to verify the robustness of the design against global and local process variations.

A. Amplifier Performance

The three-stage amplifier is simulated with a load of 400 fF. Often in analog design, minimum-length devices are avoided to improve matching properties and reduce output conductances; however, we have intentionally adopted the minimum length for all devices to demonstrate the viability of the proposed solution, even in nanoscale technologies. The width of the pMOS devices was set three times larger than that of the nMOS devices. The width of the nMOS devices of the first, second, and third stages are 1, 4, and 5 μm, respectively. The Miller capacitors C_1 and C_2 are 200- and 160-fF metal–insulator–metal devices, respectively, and the nulling resistor is implemented with a triode-biased nMOS–pMOS pair whose widths are 5 and 15 μm, respectively.

The amplifier showed an almost rail-to-rail performance with a maximum 0.75-V single-ended output swing.

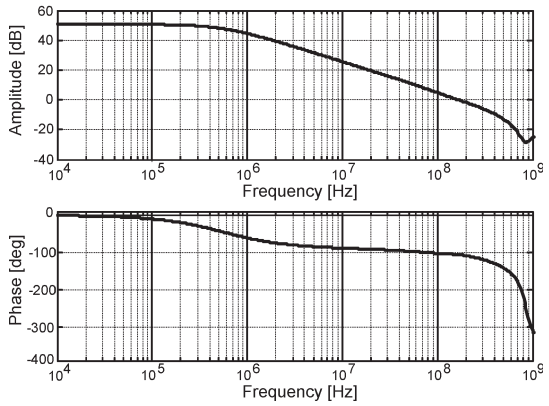

Fig. 5. Amplifier frequency response.

TABLE I
Main Amplifier Performance

	Unit	*Mean*	*Std Dev*
Total current consumption	μA	620	25
DC gain	dB	50	2
Unity-gain frequency	MHz	167	7
Phase margin	deg	74	2
Gain margin	dB	21	3
Common-mode gain	dB	-36	7
CMRR	dB	86	10
PSRR	dB	70	3
Max. output swing	$V_{PP,diff}$	1.5	
Slew rate	V/ns	0.53	-
0.1% settling time	ns	8.2	-
Input-referred noise	mV	0.73	-

Fig. 5 shows the frequency response of the amplifier. The small-signal dc gain is 50 dB with a unity-gain bandwidth of 170 MHz and a phase margin of 74°; the expected value calculated through (6) is 76°. Table I summarizes the main amplifier performance and their standard deviations obtained through 100 Monte Carlo process and mismatch simulations. Noise is integrated from 1 Hz to 10 GHz. The common-mode gain is always lower than -23 dB with an average value of -36 dB. The amplifier has also been simulated at temperatures ranging from 0 °C to 120 °C and supply voltage variations of $\pm 5\%$, showing good robustness in terms of gain, bandwidth, and stability margins.

The behavior of the large-signal gain versus the output magnitude is illustrated in Fig. 6. It is seen that the gain is higher than 40 dB up to a 1.2-$V_{\mathrm{PP,diff}}$ output signal. This relatively high gain ensures an adequate closed-loop linearity performance, as evidenced in Table II, which shows the first two

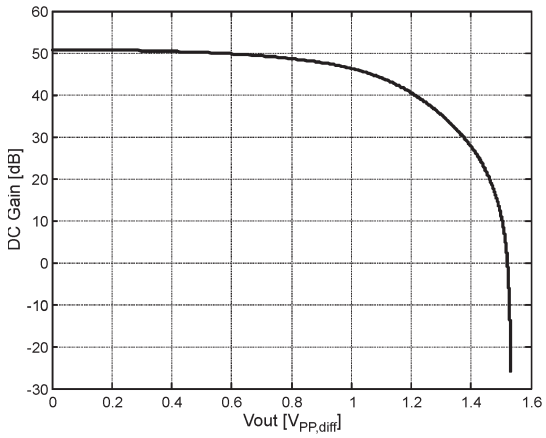

Fig. 6. Amplifier open-loop gain versus differential output swing.

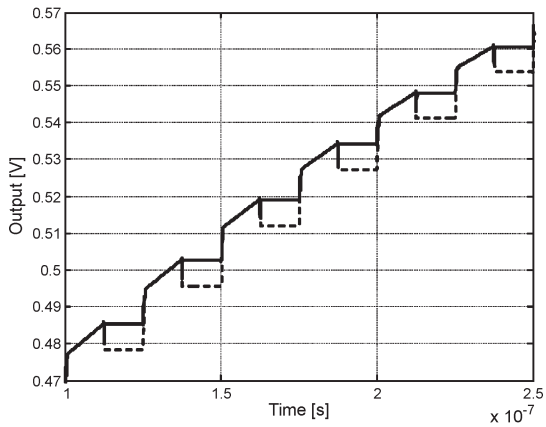

Fig. 7. Switch transient comparison. (Solid) Proposed. (Dashed) Standard.

TABLE II
AMPLIFIER HARMONIC DISTORTION

V_{IN}	$V_{PP,diff}$	0.8	1.2	0.8	1.2
f_{IN}	MHz	1	1	20	20
HD3	dB	-73	-63	-55	-43
HD5	dB	-87	-74	-75	-53

TABLE III
SWITCH PERFORMANCE COMPARISON

		Standard		*Proposed*	
	Unit	*Mean*	*Std Dev*	*Mean*	*Std Dev*
Offset	mV	-7.2	0.2	-0.13	0.05
HD2	dB	-69	1	-67	1
HD3	dB	-87	1	-89	1
Gain	mdB	16	2	-12	1

TABLE IV
S/H MONTE CARLO SIMULATIONS

	Unit	*Mean*	*Std Dev*
Offset	mV	0.0	2.0
Gain	dB	-0.07	0.01
HD2	dB	-84	12
HD3	dB	-74	1
HD5	dB	-103	5
I_{TOT}	μA	640	80

TABLE V
S/H HARMONIC DISTORTION VERSUS INPUT FREQUENCY

f_{IN}	MHz	1.25	21.25	41.25	61.25	81.25
HD3	dB	-75	-67	-62	-58	-54
HD5	dB	-107	-94	-87	-84	-80

odd harmonic distortion components for various input signal swings and frequencies, for a unity gain configuration.

B. Switch Performance

The performance of the proposed switch is compared with that of the standard clock-doubling switch. Simulations have been carried out using a passive S/H circuit as a test bench. The switch transistor size is 2 μm/0.13 μm, and it is loaded by a 200-fF capacitor. The clock is a 0.8-V 40-MHz signal, and the input is a 0.4-V_{PP} 1.25-MHz sinusoid. Table III summarizes the main results. It is apparent that the dummy switches allow cancellation of channel-charge injection and clock feedthrough. As a result, the dc component of the output spectrum is greatly reduced from 7 to 0.13 mV. The second- and third-order harmonic distortion components, as well as the gain error, are the same in the two topologies. The reason why distortion is similar is that the nonlinear ON-resistance is the dominant distortion effects in the simulation. Fig. 7 depicts the output waveform of the proposed and standard switches.

C. Overall S/H Performance

Table IV shows the simulation results for the full S/H circuit. Results are obtained for a 40-MHz clock frequency and a half-swing (0.8 V_{PP}) differential input signal at 1.25 MHz. Sample capacitors of 200 fF and load capacitors of 200 fF have been used. The circuit consumes 640 μA, including 20 μA for the clock signal generator. Noise, which is simulated with typical device models at 60 °C, is 0.23 mV_{RMS}, integrated over the full Nyquist bandwidth, resulting in a signal-to-noise ratio of 62 dB for a 0.8-$V_{PP,diff}$ input signal. Monte Carlo simulations, including both process and mismatch variations, have been performed.

Table V shows the simulation results for different input signal frequencies, at 40 MS/s, and with a differential signal swing of 0.8 V. Total harmonic distortion is higher than 10 equivalent bits (ENOB) throughout the first two Nyquist bands, and linearity is still about 9 ENOB in the fourth Nyquist band. Simulations for different supply voltages and temperatures highlight the good robustness of the proposed solution, with a ±2-dB variation of HD3.

The S/H performance for different input amplitudes up to full swing (1.5 $V_{PP,diff}$) has also been tested, and third- and fifth-order harmonic distortion are reported in Table VI as a function of input peak-to-peak swing. ENOB is 9 bits at 1.4 $V_{PP,diff}$.

Fig. 8 shows the S/H output for a 1.25-MHz 0.8-V_{PP} differential sinusoidal input signal and the detail of the transient response.

IV. COMPARISON WITH THE STATE OF THE ART

Table VII summarizes the performance of several low-voltage S/H circuits available in the literature [10]–[13]. These data show that the proposed S/H circuit is suitable for use in

TABLE VI
S/H SIMULATIONS VERSUS INPUT SWING

V_{IN} ($V_{PP,diff}$)	HD3 (dB)	HD5 (dB)
0.8	-75	-105
0.9	-72	-98
1.0	-70	-95
1.1	-67	-90
1.2	-65	-82
1.3	-62	-75
1.4	-57	-68
1.5	-52	-59

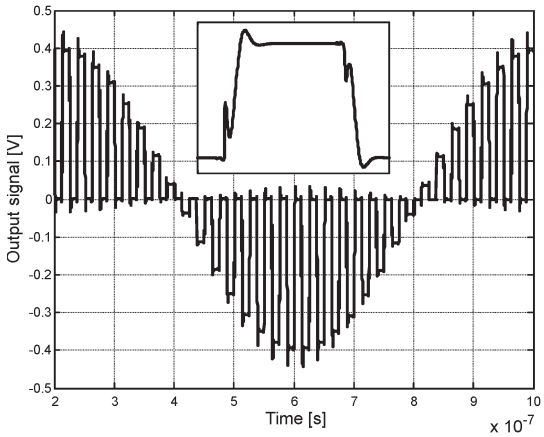

Fig. 8. S/H output for a sinusoidal 1.25-MHz 0.8-V_{PP} differential input waveform.

TABLE VII
PERFORMANCE COMPARISON WITH THE LITERATURE

Param	*Unit*	*This work*	*[10]*	*[11]*	*[12]*	*[13]*
V_{DD}	V	0.8	1	0.5	1.5	1.2
Tech.	nm	130	1200	250	350	500
f_S	MHz	40	1	1	50	40
V_{IN}	$V_{PP,diff}$	0.8 / 1.4	1.4	0.2	0.8	1.2
THD	ENOB	12 / 9	10	10	9	8
SNR	ENOB	10 / 10.8	-	-	-	-
P_D	mW	0.5	0.35	0.3	2.6	1.2
FOM	MHz * bits / mW	960 / 720	28	33	173	267

very low voltage applications for medium-to-high-resolution analog-to-digital converters (ADCs), e.g., for 9–10 bits.

The S/H circuit in [10] adopts a 1.2-μm technology and a supply voltage that is less than $2V_T$. Such a relatively low supply voltage cannot be achieved in our process as it would excessively reduce the signal swing. A lower supply voltage is employed in [11], but at the expense of a reduced signal swing (0.2 $V_{PP,diff}$). In both cases, the sampling frequency is 1 MS/s. A 50-MS/s sampling frequency is obtained in [12], with a 1.5-V supply using a 350-nm technology, whereas a 40-MS/s sampling frequency is obtained under a 1.2-V supply in a 500-nm technology in [13]. Both the last designs employ double sampling to double the sampling rate with respect to the clock frequency, but this makes the circuit sensitive to timing errors, which may affect the S/H linearity.

To compare the relative performance of the designs presented in the literature, implemented in different technologies and supply voltages, the following figure of merit (FOM) that is typically used for ADCs can be considered:

$$\text{FOM} = \frac{f_S \cdot \text{ENOB}}{P_D}. \tag{7}$$

The proposed design exhibits the best FOM, even when operated with the maximum input voltage.

V. CONCLUSION

In this brief, we have presented the design and simulations of a 0.8-V supply, 40-MS/s S/H circuit implemented in a 130-nm CMOS technology. Results show the feasibility of a very low voltage S/H circuit for applications in 9- to 12-bit, 20- to 50-MS/s ADCs. The circuit techniques employed in this brief can also be used to design multiplying DAC blocks, so that a full pipeline ADC is obtained. The proposed S/H circuit is robust against operating conditions and process variations. The largest FOM exhibited by our design is explained by the fact that it achieves the sampling frequency of the fastest design with the power consumption of the slowest design. Better linearity is also achieved.

The adopted approach can be extended to general switched-capacitor circuits. Further research will be published in the near future.

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