SPICEInverse: Synthesis of an Accelerated Multiplexed Impedance Measurement Technique for Wearable Low-Power Electrochemical Systems

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***Abstract*—Wearable devices are easy to use, small, low power devices that can benefit people in their everyday lives . They are made with small form factor, comfortable fit, and unparalled function in mind. The inherent challenge in making a better device is to provide an overview of the user's health for an elongated period of time with minimal recharging or replacement of sensors. Sensors made by semiconductor processes such as accelerometers, thermometers and photoplethysmogram (PPG) have been the pillars of the commercial wearable industry; however, these fail to interact with actual biological samples. A need for analog front-ends tailored for biosensors has risen in recent years. These rely on antigen-antibody interactions. This work demonstrates how a relatively large number of antibody-functionalized biosensors can be interfaced in size-constrained circuit design more efficiently than a row-column decoding scheme.**

***Index Terms*—Impedance measurement, wearable devices, battery-powered devices, handheld devices, Fast Fourier Transform, biosensors, HDAM**

I. Introduction

Impedance measurements techniques have been used for a significantly long time by chemists to study the behavior of electrochemical cells in the frequency domain and unravel surface phenomena occurring at the electrode-electrolyte interface [1]. These discoveries have led to development of low-power, low-form-factor sweat biosensors complemented by highly accurate and repeatable analog front-ends to ensure maximum signal-to-noise ratio in the frequency band exhibiting maximum impedance changes [2], [3]. However, with increase in the sensing resolution, the current consumption of the device increases, leading to shorter battery life. Moreover, if a larger number of sensors are required, this results in an even larger number of switches, which also contributes to the static power consumption as well as parasitic load offered by multiple switches and routing seen by the front-end.

Fig. 1: A multiplexed biosensor system for detection of alcohol and ethyl glucuronide content in sweat using electrochemical impedance spectroscopy (EIS). Source: [3].

II. A primer on impedimetric multiplexed biosensors

Various biosensors have been designed for detecting the presence of a biomarker of interest in human sweat. A large population of these sensors operate on the interaction of the biomarker with a functionalized sensor surface, which is functionalized by immobilizing an antibody using cross-linking chemistry. These antibodies have a specific affinity for biomarkers of interest.

Each sensor will present a change in impedance which can be sensed electrically by an analog front-end. A typical biosensor system will have one biosensor connected to one analog front-end to give a response for a single biomarker; however, it is more efficient to create a multiplexed configuration of biosensors that are stimulated by the same analog front-end to get results from a group of particular biomarkers. Moreover, due to interaction with an ionic fluid, such sensors are prone

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to ionic noise, hence elimination of such noise effects is of prime importance [4]. One such combination of molecules of interest would be detection of alcohol, glucose and lactate in sweat [5]–[11], wherein alcohol consumption leads to high alcohol and glucose levels in contrast to Type II diabetes, where glucose and lactate levels are elevated.

III. Synthesis of Multiplexing by Permutation

Although row-column matrix has been considered one of the most simplistic and acceptable multiplexing standard in the industry, other multiplexing methods do exist that achieve higher load-per-pin count. One such scheme was proposed by Charlie Allen in 1995 which under his name came to be known as 'Charlieplexing'. This scheme allowed for connecting the maximum number of LED loads using minimum number of pins for an LED clock using all permutations possible for connection between bidirectional drivers. However, in case of AC impedance, polarity does not affect the The mathematical proof of using permutations for multiplexing is shown below.

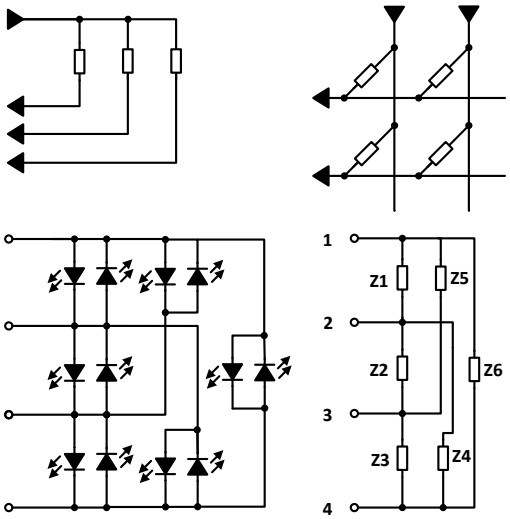

Fig. 2: Circuit implementation for 1:N, row-column decoder, Charlieplex and HDAM networks for $N = 4$.

A. Proof by mathematical induction

The principle of mathematical induction is to prove a mathematical relation is true for every natural number, in this case, the number of available pin N. If $N = 2$, it is evident one can connect a single AC load between these 2 pins, one pin being source and the other being sink. If $N = 3$ is attempted, in the case of 1:N multiplexing, $M = N-1 = 2$ loads can be connected to the system. For a row-column decoder, if $N1 = N2 = N$, then the number of loads that can be connected is $N^2 = 9$ for $2N = 6$ pins. In case of Charlieplexed loads, one can connect $M = N^2 - N = 6$ loads for $N = 3$ pins.

In the case of impedance measurement, the polarity is irrelevant due to oscillating nature of the excitation voltage, hence, complementary connection of loads is not possible in such an application. Thus, if a complementary load is replaced by a single AC load in a Charlieplexed system, a new topology, High Density Analog Multiplexing (HDAM) [12], can be created to connect multiple AC loads by permutation. In this case, the number of supported loads will decrease to $M = N \times (N-1)/2$. If $N = 3$ for this architecture, $M = 3$, which achieves a larger loads-per-pint count or M/N ratio compared to the row-column decoding scheme. A comparison of the above mentioned multiplexing architectures are shown in Fig. 3.

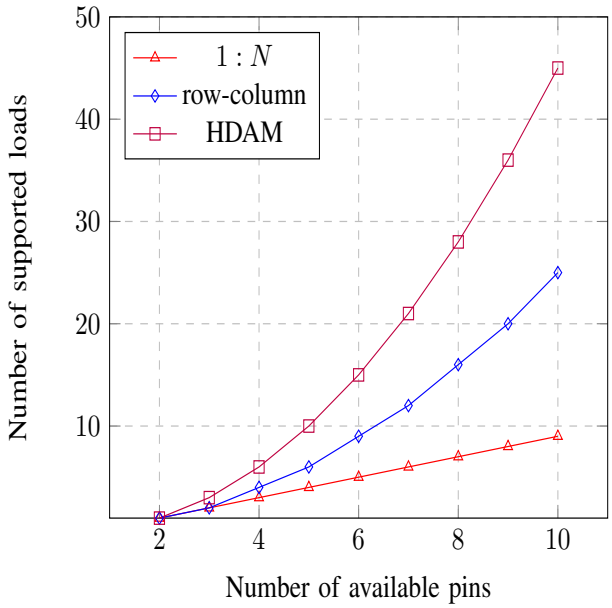

Fig. 3: A plot of number of loads that can be connected to the above mentioned multiplexing techniques against the number of available system pins.

B. Wiring scheme

Algorithm 1 Creation of SPICE netlist for an N-pin HDAM interconnection network

```
for (i=1 ; i<N; i++) do
  for (j=i+1 ; j<N ; j++) do
    append(netlist, Zij, i, j)
  end for
end for
```

The process of interconnection and assignment of designators for a $N > 2$ pin HDAM system is shown in Algorithm 1. It is assumed that each of the N pins in this network will be a network node. The objective is to connect all loads at all possible permutations of pair of nodes such that a single unique load is present between any two nodes. This netlist can be sanity checked to have $M = N \times (N-1)/2$ entries for each of the loads. Each entry will also consist of the source node i and sink node j for each load connected. These

source and sink nodes can also be used to control the switch network between the DAC and ADC and the HDAM network to select each unique load one at a time. It should be noted that since the impedances are symbolic, they are variables and will be computed based on the measured current and excitation voltage applied. The transformation to obtain these values is discussed in the next subsection.

C. Impedance measurement and undesirable effects

The process of measurement of a single load from an interconnected HDAM network is shown in Fig. 4. Let us assume for $N = 4$, the impedance between nodes 1 and 2 need to be measured. Thus, the switching network will be turned on such that node 1 is the source at voltage V_{excite}, whereas node 2 is the sink. It would be desirable to get the impedance as $Z12$ if it were a truly isolated multiplexing scheme. However, the AC loads highlighted in red, viz. $Z13, Z14, Z23, Z24$ and $Z34$ will appear as a different network in parallel to $Z12$. This will cause an undesirable flow of current in the circuit other than $i12$. Let us assume this current flow is $I_{measured}12$ and is measurable via an I-V converter at sink pin 2. The voltage V_{excite} has been set by the user using a DAC at node 1. Thus a circuit can be created as shown in Step 2 of Fig. 4. This network can be simplified as shown in Step 3, where all AC loads except $Z12$ form a series-parallel network. However, for now, one can save the value of $I_{measured}12$ for future computation. Now, based on the netlist, the next load to be switched to would be $Z13$ and $I_{measured}13$ will be measured and stored. This process will be continued till the end of file.

IV. Cancellation of undesirable parallel impedance

A. Solution by impedance terms

The cancellation of impedance terms can be computed using the expression for input impedance as per common circuit analysis methods of reducing the circuit to series-parallel impedance networks. This would require the circuit be converted to a single port network wherein 2 pins selected by the user are used as an excitation port. For example, as shown in Step 3 Fig. 4, the network offers multiple loops for the current to flow. Due to this, it is difficult to estimate whether it is a purely serial or parallel combination of AC loads. Such a network can be solved using star-delta transformation equations at the cost of heavy computational complexity. Thus, to simplify this circuit more, a short loop was implemented on nodes 3 and 4 as shown in Step 4. This results into a fairly simple series parallel combination of AC loads where $Z34$'s contribution is cancelled. Thus, the impedance offered by the undesirable loop is $(Z13||Z14) + (Z23||Z24)$. Thus the resultant impedance between nodes 1 and 2 can be shown as per Eqn. 1. Similarly, one can compute equations for all possible combinations for $Z13$, $Z14$, $Z23$, $Z24$ and $Z34$ as well.

$$Z'_{12} = Z12||\{(Z13||Z14) + (Z23||Z24)\} \tag{1}$$

It should be noted that such a solution is not scalable as it requires a significant effort in computing symbolic input impedance equation. A tool SapWin [13], was used to obtain above mentioned equations, however, the complexity of the polynomial terms increased to the extent of program failure for $N > 4$.

B. Solution by susceptance terms

An effort was directed towards finding a method to create a scalable relationship between true current and the current measured by the sink pin. SPICE uses the relationship $I = GV$ to solve highly complex networks to obtain solutions to current law equations and node voltages. Thus, the input to a SPICE deck is G, which is a conductance matrix and I, which is the matrix of input current sources in the circuit. One may populate node voltages using V if available or compute them using the relationship $I = GV$. In an HDAM network, the current and voltage values are known but the impedance values are not. Thus, the relationship $I = GV$ can be modified to $I = YV$, where $Y = G + jB$ is a complex admittance term. This relationship can used to compute $Y = IV^{-1}$, which is an inverse relationship from what SPICE uses. The $N = 4$ network shown in Step 6 of Fig. 4 can be written as per Eqn. 2. Such an equation can be extended for the other five impedance terms. Here, all $I_{measured}$ and V_{excite} terms are known. All the V_x terms can be obtained by measuring and stored as per the designed system's capability.

$$I_{measured}12 = \begin{bmatrix} Y12 + Y13 + Y14 & Y13 + Y14 \end{bmatrix} . \begin{bmatrix} V_{excite} \\ -V_x12 \end{bmatrix} \tag{2}$$

Algorithm 2 Creation of V matrix for a SPICE-Inverse solver

```
M = N × (N − 1)/2
load netlist
for (i=1 ; i<N; i++) do
  for (j=i+1 ; j<N ; j++) do
    append(Y, Yij)
    append(I, Iij)
    for (k=1 ; k!=i && k<M ; k++) do
      p = netlist[k][2]
      q = netlist[k][3]
      if p == i then
        if q == j then
          V[ij] = V_excite
        else
          V[ij] = V_excite − V_x ij
        end if
      else
        V[ij] = 0
      end if
    end for
  end for
end for
```

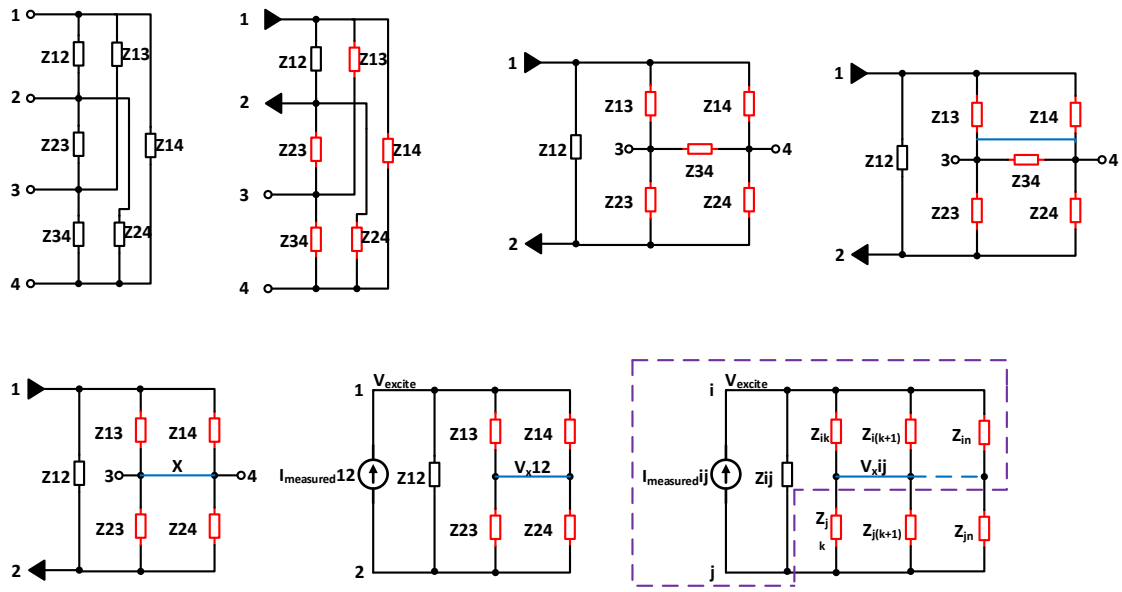

Fig. 4: Simplification of an HDAM circuit to cancel the effect of undesired parallel network. Step 1 is network at rest. Step 2 highlights the the undesirable impedance in parallel with the AC load of interest. Step 3 is redrawing Step 2 to get an idea of the number of series parallel loops. Step 4 shorts the pins not being used as source or sink. Step 5 shows that impedance shorted by the loop are no longer a part of the circuit. Step 6 is a SPICE representation of the Step 5. Step 7 is mathematically deduced from Step 6.

$$\begin{bmatrix} I_{measured}12 \\ I_{measured}13 \\ I_{measured}14 \\ I_{measured}23 \\ I_{measured}24 \\ I_{measured}34 \end{bmatrix} = \begin{bmatrix} V_{excite} & V_{excite}-V_x12 & V_{excite}-V_x12 & 0 & 0 & 0 \\ V_{excite}-V_x13 & V_{excite} & V_{excite}-V_x12 & 0 & 0 & 0 \\ V_{excite}-V_x14 & V_{excite}-V_x14 & V_{excite} & 0 & 0 & 0 \\ V_{excite}-V_x23 & 0 & 0 & V_{excite} & V_{excite}-V_x23 & 0 \\ V_{excite}-V_x24 & 0 & 0 & V_{excite}-V_x24 & V_{excite} & 0 \\ 0 & V_{excite}-V_x34 & 0 & V_{excite}-V_x34 & 0 & V_{excite} \end{bmatrix} \cdot \begin{bmatrix} Y12 \\ Y13 \\ Y14 \\ Y23 \\ Y24 \\ Y34 \end{bmatrix} \quad (3)$$

C. Acceleration of matrix operations

It can be deduced by observation that it is not required to solve the equality between V_{excite} and V_x terms as we are interested in the current split that happens between the desired and undesired impedance at the source node. Thus, the matrix can be reduced as shown in Eqn. 3.

It can be observed from Step 7 that the V matrix is dependent only on loads connected directly to the source node. Thus, this property of the HDAM network can be exploited for the creation of the V matrix can be done using Algorithm 2. Such an algorithm can be easily implemented on a microprocessor or an FPGA.

V. Concluding Remarks

This work successfully demonstrates a novel multiplexing technique modified specifically for low-power bioimpedance measurement front-ends that are contrained by limitations of commercial off the shelf (COTS) electronic parts and small form factor. A technique to connect multiple loads by permutation has been demonstrated to show 100% increase in the number of sensed AC loads. Despite the limitation that is observe due to undesirable parallel impedance, it can be seen that by simple matrix operations, one can isolate true impedance values from an intertwined network of AC loads. Two algorithms have also been presented to create a symbolic network for the HDAM network as well as create a V matrix for cancellation of undesirable impedance.

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