Energy-efficient sub-DAC merging scheme for variable resolution SAR ADC

S.R. Srinivasan and P.T. Balsara

An energy-efficient capacitive digital-to-analogue converter (DAC) switching method for a reconfigurable successive-approximation register (SAR) analogue-to-digital converter (ADC) is proposed. The proposed method can achieve a variable resolution starting from 1 bit with 1 bit resolution increments. The proposed method achieves the energy savings due to the fact that the binary-weighted capacitors are merged with the main-DAC, as and when required. When sized for the same thermal noise as the traditional SAR ADC, the proposed method achieves 96.9% reduction in switching energy and a factor of 2 improvement in static linearity performance. If sized for the same static linearity as the conventional SAR ADC, the DAC area could be reduced by a factor of 4, which further improves the switching energy savings to 99.2%.

Introduction: In recent years, successive-approximation register (SAR) analogue-to-digital converters (ADCs) have emerged as an excellent choice for medium-resolution and low- to medium-speed applications. This is especially true for biomedical sensor applications, where the bandwidth of interest is within a few kilohertz [1]. The popularity of SAR ADCs is because of their energy efficiency [2], and is due to their minimalistic number of active devices (typically a comparator and some digital logic), and their passive capacitive feedback digital-to-analogue converter (DAC). As the capacitive DAC is typically binary weighted, its size increases exponentially with the resolution of the ADC, and therefore a major chunk of the power consumption in the SAR ADC is because of DAC capacitor switching. Recently, many methods have been proposed to improve the efficiency of the DAC switching energy [3–6], making the SAR ADC an ideal choice for portable sensor applications. In this Letter, a new DAC switching scheme is presented, which improves the switching energy by 96.9% and linearity by a factor of 2, when compared with the conventional scheme, and also yields itself favourable to reconfigurable applications.

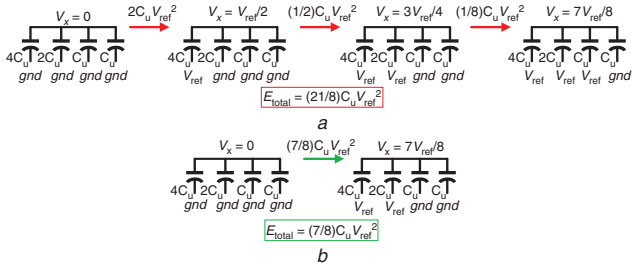

Fig. 1 *Energy savings with a priori information*

a Energy needed with bit-cycling
b Energy needed with simultaneous switching

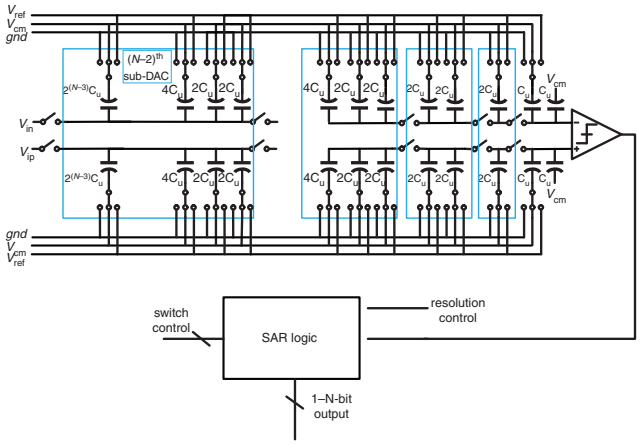

Fig. 2 *N-bit variable resolution SAR ADC with proposed switching scheme*

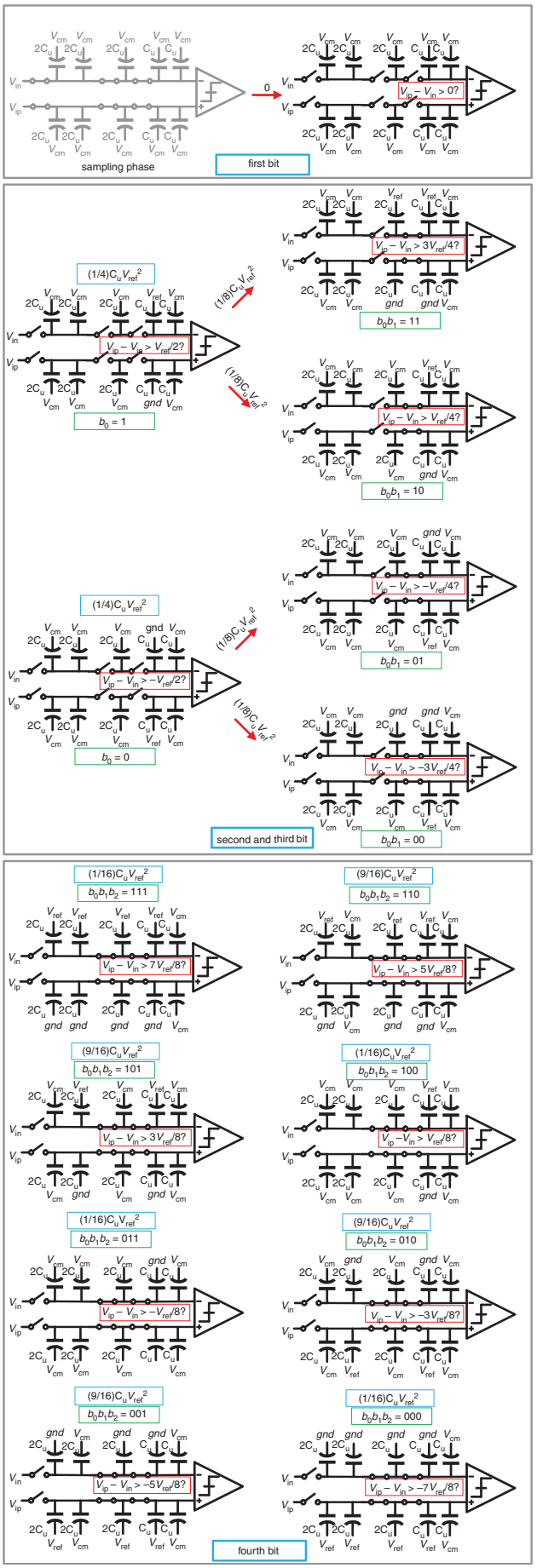

Fig. 3 *Energy consumption of 4 bit DAC with proposed switching scheme*

The main idea of this Letter stems from the fact that using an *a priori* knowledge of the bits to generate a reference voltage on the DAC is a far

more energy-efficient approach than bit cycling. To illustrate this point, an example of a 3 bit DAC is shown in Fig. 1. Here, a conventional capacitive DAC is shown with the bit-sequence '11' (which is the most energy-efficient sequence in a capacitive DAC) and a reference for determining the third bit is generated. The energy needed to arrive at the same DAC voltage with *a priori* bit information is also shown in the Figure, and it can be seen that it requires less switching energy.

This is used in creating an expanding capacitive DAC array. At each step, the sub-DAC (having the same size as the main-DAC) utilises all the previous bits to generate the next reference voltage, and then that merges with the main-DAC and becomes a part of it. This is also equivalent to saying that the sub-DAC, after the merger, acts as the new most significant bit (MSB) capacitor of the main-DAC. As this operation averages the voltages on the sub-DAC and the main-DAC, we have to ensure that the voltage on the sub-DAC is the right value to arrive at the required reference after merging. This can be easily done by building the sub-DAC with binary-weighted capacitors, and switching these capacitors by utilising all the previously generated bits, except the MSB. A tri-level switching scheme has been used in the proposed method that uses three reference voltages: *gnd*, $V_{cm}(V_{ref}/2)$ and V_{ref}. This technique facilitates the proposed idea of a variable resolution SAR ADC. The expandable DAC array can increase in resolution from 1 bit to N-bits in 1 bit increments. The proposed idea of the complete N-bit SAR-ADC is shown in Fig. 2.

At each stage of reference generation, the capacitors in the sub-DAC are switched simultaneously according to the previously determined bits (b_1, b_2, …, b_{M-2}). The MSB (b_0) determines whether a 1 and 0 correspond to (V_{ref} and V_{cm}) or (V_{cm} and *gnd*). The only difference between the sub-DAC and the main-DAC is that the capacitors that form the sub-DAC are scaled up by a factor of 2 to match the size of the main-DAC. For example, the sub-DAC that is merged with the main-DAC to generate the reference voltage for the comparator to determine the Mth bit (b_{M-1}) is identical in size as the main-DAC and has $M-2$ switches that connect to all the binary-weighted capacitors. In Fig. 3, the switching energy of a 4 bit fully differential DAC is shown. Although top-plate sampling is shown in this Figure for simplicity, it can be easily extended to bottom-plate sampling without any change in energy consumption. This minimises the effect of parasitic capacitances of the DAC. It is also worthwhile to note that the common-mode voltage of the comparator is always V_{cm} throughout the process, regardless of the input, which is beneficial to the linearity of the ADC.

Table 1: Average switching energy of different DAC (10 bit ADC) switching schemes

Switching schemes	Average switching energies ($C_u V_{ref}^2$)	Efficiencies
Conventional	1363.3	reference
MCS [3]	169.4	87.6%
EMCS [4]	149.1	89.1%
V_{cm}-based [5]	31.88	97.66%
Hybrid-capacitor [6]	15.88	98.83%
Proposed method	42.67 (noise-matched) 10.67 (linearity-matched)	96.9% 99.21%

For the proposed method, the switching energy required to generate the DAC voltage, which is needed by the comparator for resolving the Mth bit (b_{M-1}) can be written as

$$E_M = \begin{cases} 0, & M = 1 \\ \frac{1}{2^M}.C_u.V_{ref}^2, & M = 2 \\ \frac{1}{2^M}.C_u.V_{ref}^2 + \frac{1}{2}\left(1 - \frac{C_{V_{ref}}}{C_{Total}^{sub-DAC}}\right).C_{V_{ref}}.V_{ref}^2, & M > 2 \end{cases} \quad (1)$$

where $C_{V_{ref}}$ and $C_{Total}^{sub-DAC}$ are given by

$$C_{V_{ref}} = \sum_{i=1}^{M-2} C_i.\overline{(b_i \oplus b_0)}$$

$$C_i = \begin{cases} 2^{M-2-i}C_u, & i \neq M-2 \\ 2C_u, & i = M-2 \end{cases}$$

$$C_{Total}^{sub-DAC} = 2^{M-2}$$

A comparison of average switching energies has been summarised in Table 1 for a 10 bit SAR ADC, and it can be seen that it is competitive with the current state-of-the-art. Intuitively, the energy savings in this technique are because of the fact that during the MSB transition, a much smaller capacitor (for example, C_u instead of $256C_u$ in a traditional fully differential 10 bit DAC) needs to be switched to V_{ref}. As we move towards a higher resolution, all the previous bits are known *a priori* and the required sub-DAC voltage to generate the next reference for the comparator (after merging with the main-DAC) can be achieved in a very efficient manner.

Similar to [4], the worst-case code transition occurs at [10111…] to [11000…] and [00111…] to [01000…]. This translates to bottom-plate capacitor voltages of [V_{ref}, V_{cm}, V_{ref}, V_{ref}, V_{ref}…] to [V_{ref}, V_{ref}, V_{cm}, V_{cm}, V_{cm}…] and [*gnd*, *gnd*, V_{cm}, V_{cm}, V_{cm}…] to [*gnd*, V_{cm}, *gnd*, *gnd*, *gnd*…]. The worst-case integral and differential nonlinearities (INL and DNL) for the proposed scheme can be found by looking at the DAC configurations at the worst-case code transitions and calculating the number of uncorrelated capacitors that contribute to the DAC voltages. Assuming that the unit capacitors (C_u) have a variance of σ^2 from their nominal value, the maximum standard deviation of INL and DNL for the proposed scheme can be calculated as $0.5 \times 2^{(n/2-1)}\sigma$ and $2^{(n/2-1)}\sigma$ LSBs (least significant bits), respectively. This is a factor of 2 improvement in the static linearity performance when compared with the conventional N-bit SAR structure.

Conclusion: An energy-efficient sub-DAC merging scheme for a variable resolution SAR ADC is proposed in this Letter. The switching energy efficiency compares favourably against the previously proposed switching schemes. Fixed common-mode at the comparator during bit-cycling and bottom-plate sampling benefits the overall linearity of the ADC. A factor of 2 improvement in static linearity is also shown, which relaxes the capacitor matching requirements of the DAC array.

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One or more of the Figures in this Letter are available in colour online.

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