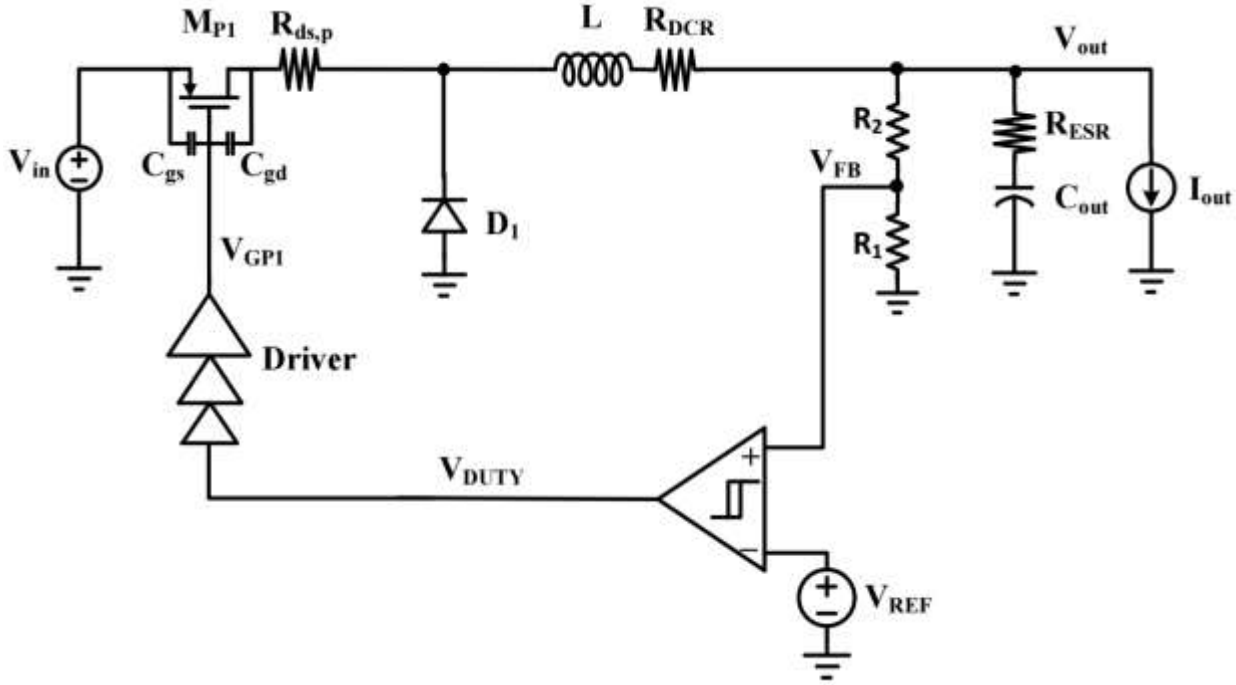
EECT6379 - Energy Harvesting, Storage and Powering for Microsystems

Third Project Assignment | Devang Sankhala (dgs150030) | May 1, 2017



Process files

TSMC 0.35 um process files were used for this assignment. Important characteristic values are given.

Parameter	NMOS	PMOS
μC_{ox}	150 µA/V^2	30 µA/V^2
Threshold voltage	0.6 V	0.7 V
Lambda	0.01	0.001

DCM operation

For this converter, we assume an energy harvesting application. Thus, for DCM operation, the peak current is fixed and the switching frequency is assumed to vary with load.

$$\frac{V_{out}}{V_{in}} = \frac{D_{1x}}{D_{1x} + D_{2x}}$$

Here, D_{1x} is the charging time, whereas D_{2x} is the discharge time for inductor. D_{3x} is the off time beyond the discharge of the inductor. It is assumed to vary inversely with the load current. For the peak current,

$$I_{out} = V_{in} \frac{D_{1x} D_{2x} T_{sx}}{2L} = i_{L,peak} \frac{D_{1x} + D_{2x}}{2}$$

For our application, the input voltage varies drastically, thus for a fixed output current, the switching frequency will change drastically. However, assuming $D_{1x} + D_{2x} \ll D_{3x}$ for minimal switching losses without explicitly calculating them, it is assumed that the factor is approximately 10 for max load. Thus,

for small value of $D_{1x} + D_{2x}$, we take a larger value of inductor. This will also ensure that the peak inductor current is reduced, and will need less frequent charging. Thus, for a given assumptions, **L = 10µH** is selected for a max operating frequency of 300 kHz for maintaining small inductor and capacitor values. As load current decreases by 50 to a minimum value, the frequency will also decrease by 50 times, i.e. 6 kHz. Also, it can be assumed that since $D_{1x} + D_{2x}$= 0.1, the ratio of peak and output current will be 20 as per above equation. **DCR is 0.5 ohm** as per product number given in circuit diagram**.**

Hysteretic comparator

The hysteresis band equation is given by

$$V_{HYS} = 2\sqrt{\frac{I_F}{k\left(\frac{W}{L}\right)_1}}\frac{\sqrt{\beta}-1}{\sqrt{\beta+1}}$$

Now, since an output ripple specification of 50 mV is given and there exists a feedback factor of $\frac{2}{3}$, the hysteresis band should be $33\frac{1}{3}$ V, i.e. $16\frac{2}{3}$ V on each side of 1.2 V reference. Thus, using given process parameters and β = 1.2, the sizing given in the table were selected. It should be noted that the input MOSFETs are highly large for a small hysteresis band. The tail current of 1 µA was selected to dedicate 3 µA to the comparator. The resistive divider is made using 1MΩ and 2MΩ resistors for a feedback factor of $\frac{2}{3}$ and a current of 1 µA. Thus, the static current is set to 4 µA.

One should note that the output ripple will be decided by this hysteresis band, as there is no true closed loop continuous time operation like a PWM control scheme. The output capacitor will be important to suppress the spurs that occur due to energy transfer.

Designator	W (m)	L (m)	Multiplier
M0	1.0E-5	5.0E-7	1.00
M1	1.2E-6	5.0E-7	1.00
M2	1.0E-5	5.0E-7	1.00
M3	1.2E-6	5.0E-7	1.00
M4	1.0E-6	5.0E-7	1.00
M5	1.0E-6	5.0E-7	1.00
M6	1.0E-6	5.0E-7	1.00
M7	1.0E-6	5.0E-7	1.00
M8	1.0E-6	5.0E-7	1.00
M14	1.0E-6	5.0E-7	1.00

Output Capacitor

The maximum spike at the output is expected when the inductor storing a large value of current discharges to the output capacitor in D_{2x} period only. Considering ideal elements, the energy stored by inductor is the energy stored by capacitor.

$$\frac{1}{2}CV^2 = \frac{1}{2}Li^2$$

$$C_{out} = \frac{1}{V^2} L i^2 = \frac{L\left({i_{L,peak}}^2 - {i_{O,min}}^2\right)}{\left({V_{O,max}}^2 - {V_O}^2\right)} = \frac{10\mu(100m^2 - 0.1m^2)}{(1.825^2 - 1.8^2)} = 1\mu F$$

ESR is 0.15 ohm worst case.

Power devices

First, for the PMOS switch transistor, based on the peak load current and drain-source voltage extremes, the sizing is decided.

$$I_D = k \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

Here, a drop of 250 mV and 5 mA average current is assumed across the switch.

For the diode, the current equation for a long-channel diode is

$$I_{diode} = qA \left[\frac{\mu_N V_T \frac{n_i^2}{N_A}}{L} + \frac{\mu_P V_T \frac{n_i^2}{N_D}}{W} \right] \left(e^{\frac{V_D}{V_T}} - 1 \right)$$

This equation shows that by decreasing the dimensions, one can increase the current linearly. However, to keep within fusing limits, multiple diodes are used in parallel.

Designator	W (m)	L (m)	Multiplier
M0	4.0E-6	3.5E-7	256
D0	2.0E-6	7.0E-7	100

Driver

The driver circuitry for the PMOS switch is a tapered inverter chain. Based on the MOSFET gate-source and gate-drain capacitances, an estimated load value is used to design the driver. The input capacitance of the driver is set by the hysteresis converter output. Since we have fixed the maximum frequency to 300kHz, we need that the delay from the hysteresis comparator input to the gate of the switch transistor should be very less than $3\frac{1}{3}$ µs, approximately 10 times less. Also, we need minimum switching loss on the inverter chain. Thus, we need an optimum solution for these two equations. τ is intrinsic to the process and not to sizing. It was found to be 30 ps for this process.

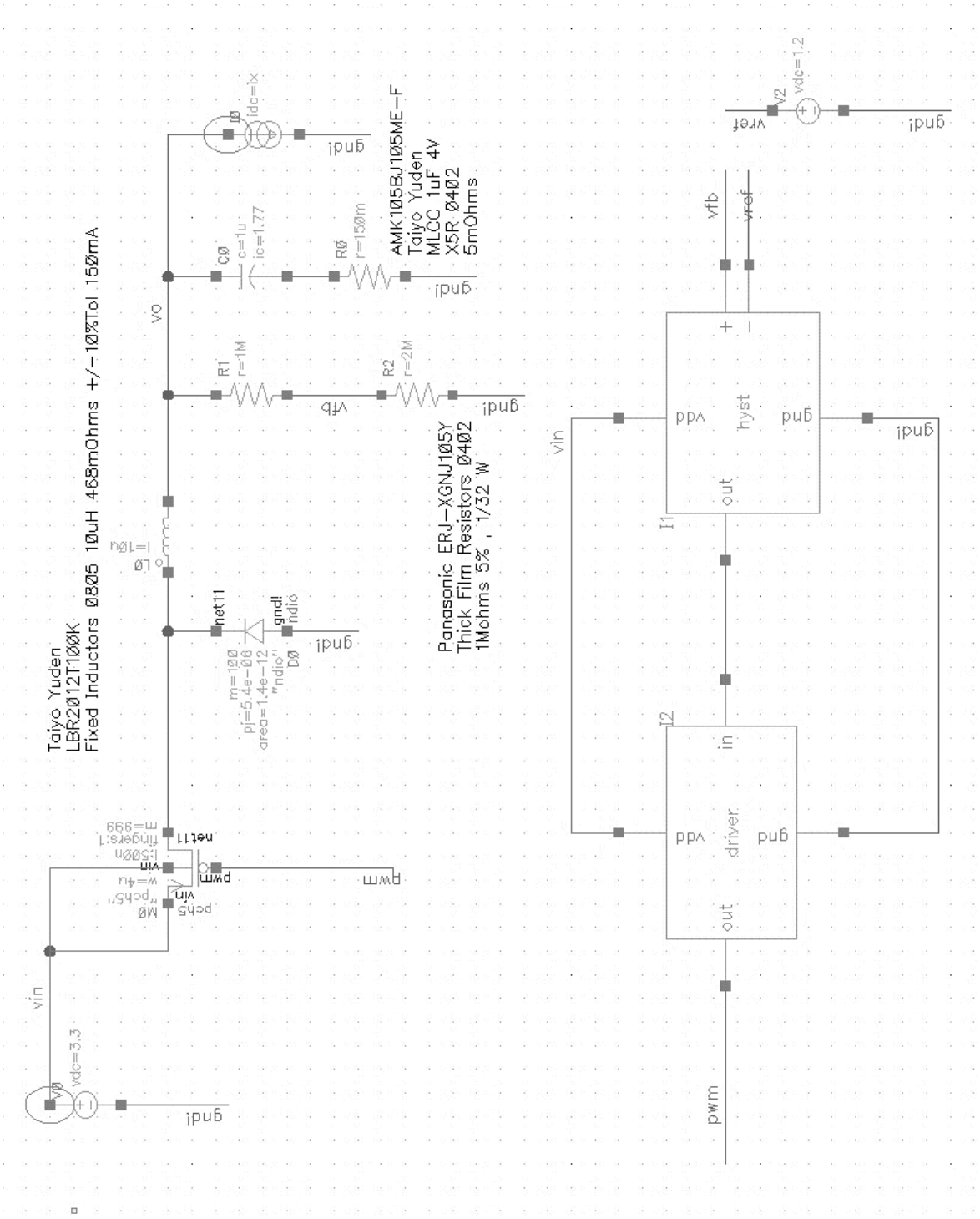
$$D = \sum GBH + \sum P = (N).1.\frac{\left(C_{gs,PT} + C_{gd,PT}\right)}{C_{out,comp}} + N\tau$$

$$P_{loss,chain} = f_s {V_{in}}^2 \sum\nolimits_{N-1} C_{in,i}$$

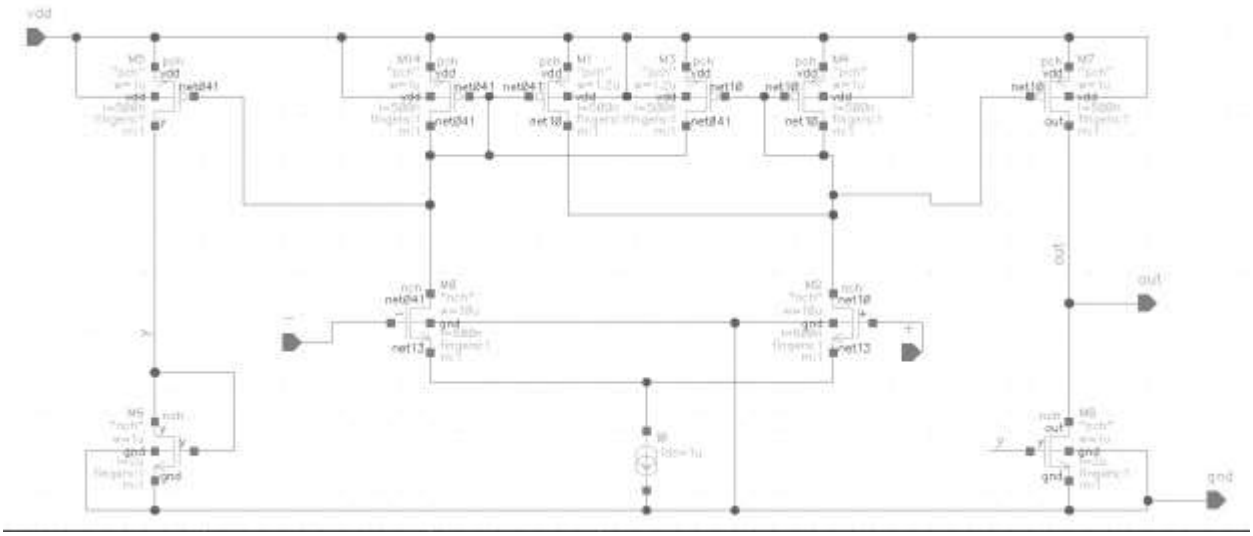
Designator	W (m)	L (m)	Multiplier
M7	1.0E-6	3.5E-7	1
M8	1.0E-6	3.5E-7	1
M1	1.0E-6	3.5E-7	8
M0	1.0E-6	3.5E-7	8

M12	1.0E-6	3.5E-7	64
M13	1.0E-6	3.5E-7	64
M3	1.0E-6	3.5E-7	128
M2	1.0E-6	3.5E-7	128

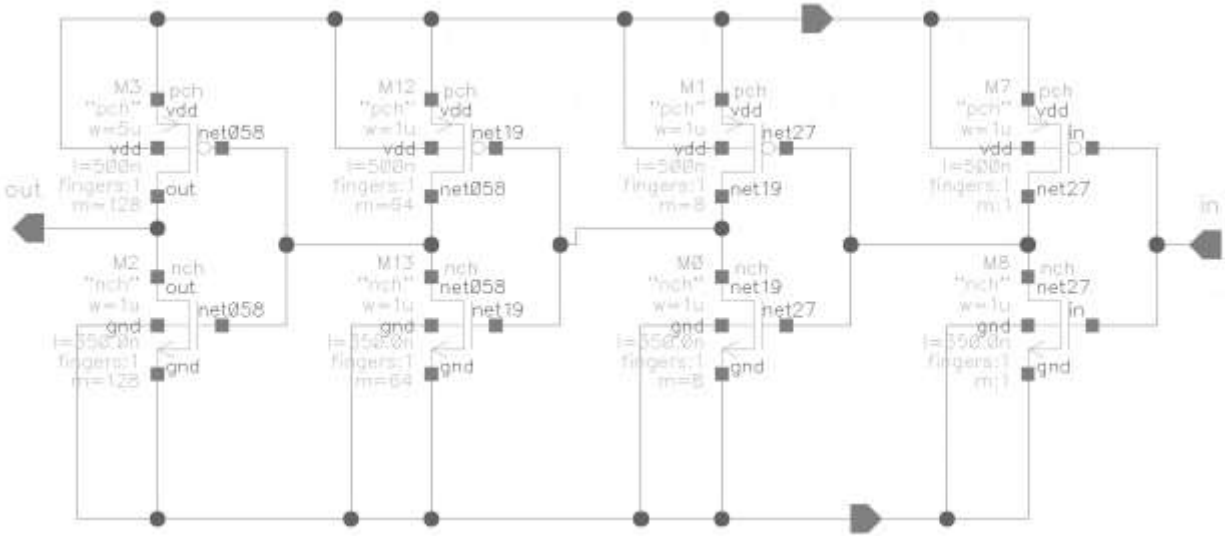
System level circuit



Hysteresis comparator circuit

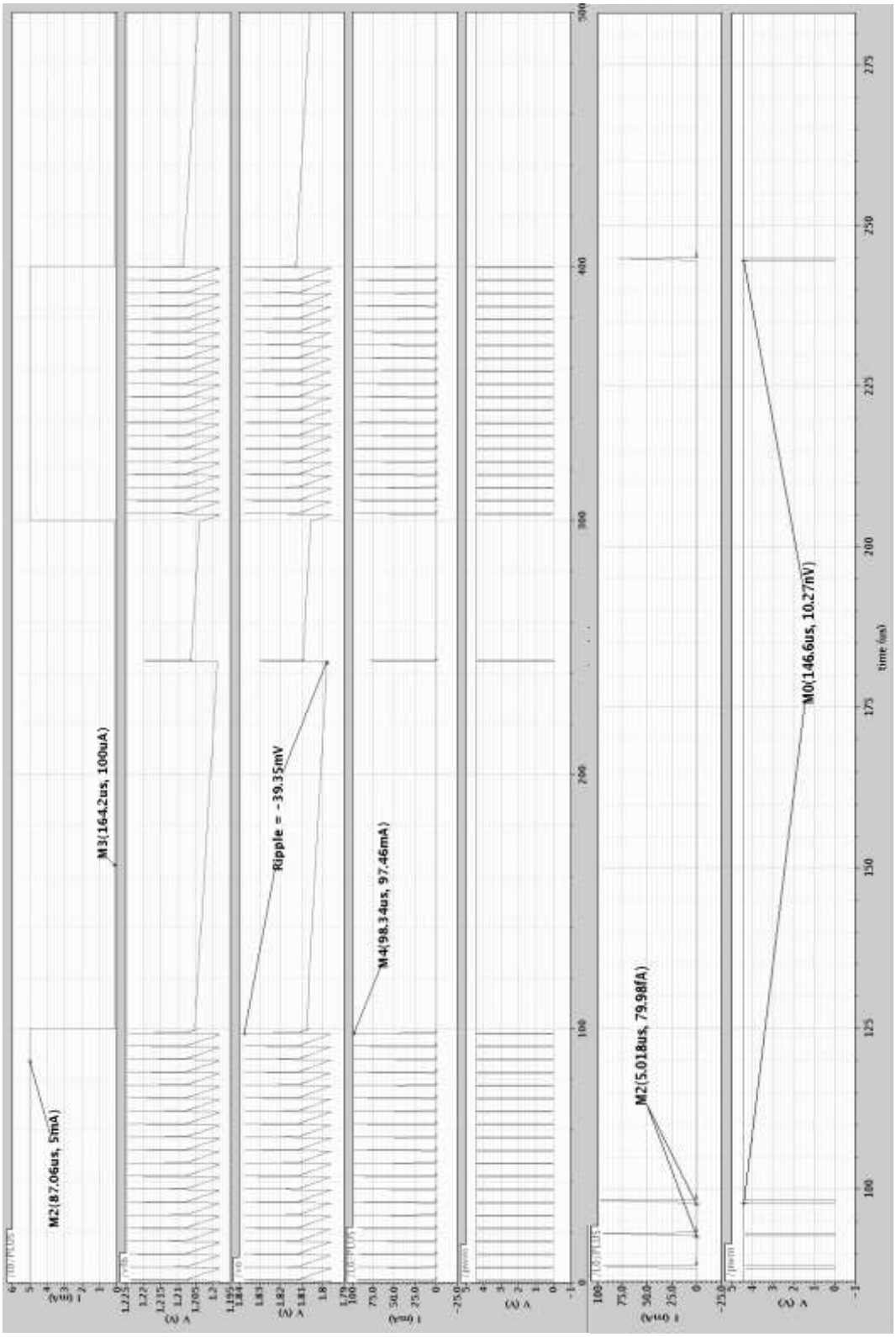


Driver circuit

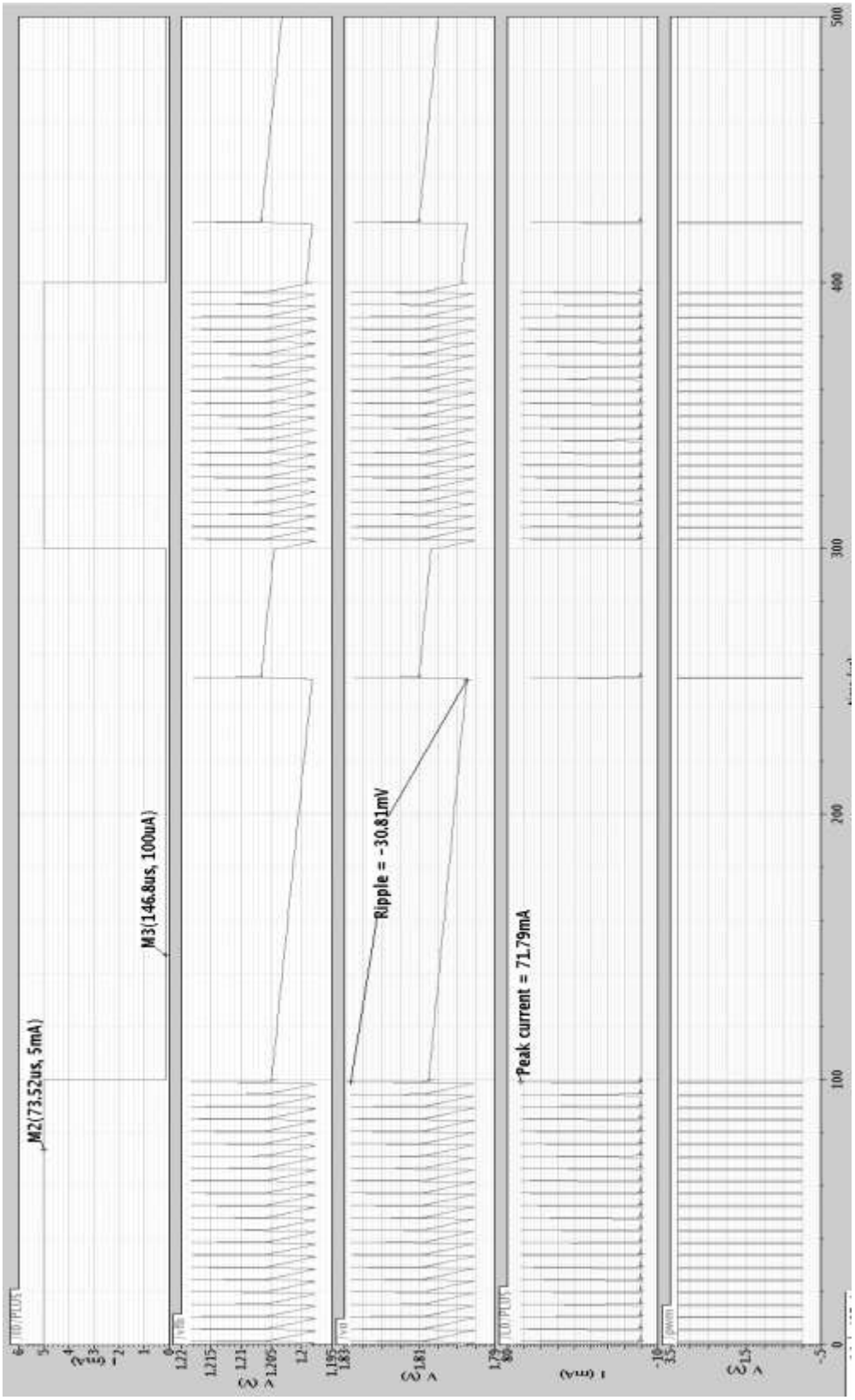


Steady State Transient Waveforms for 500 µs

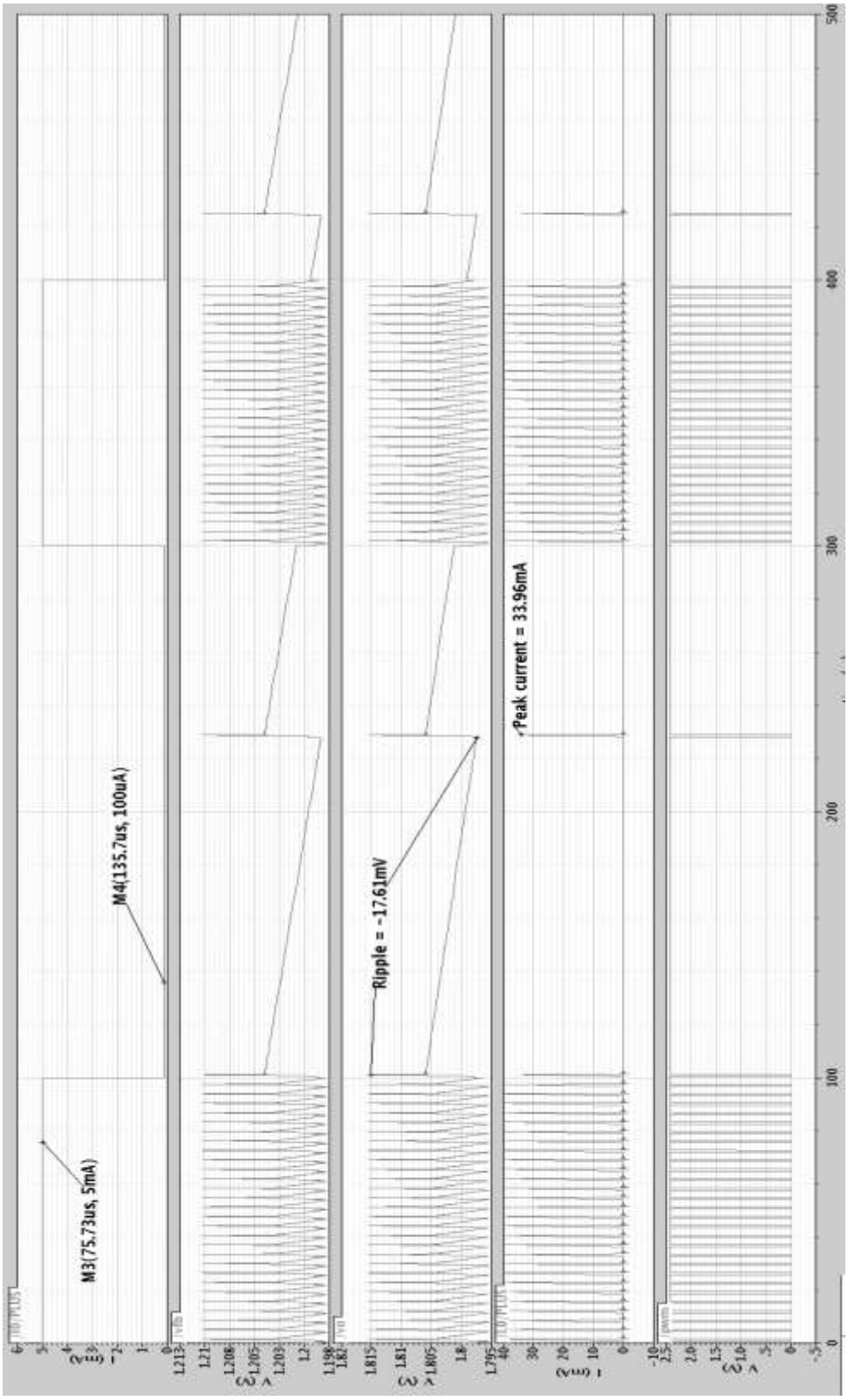
4.4 V input (with period zoomed in)



3.3 V input


M2(73.52us, 5mA)
M3(146.8us, 100uA)
Ripple = -30.81mV
Peak current = 71.79mA

2.4 V input


M3(75.73us, 5mA)
M4(135.7us, 100uA)
Ripple = -17.61mV
Peak current = 33.96mA

Efficiency at 3.3 V input

These values were obtained by averaging the input and output voltage and current values in steady state over a fixed period. It is assumed that the power other than the output power will be dissipated as losses.

Load current (mA)	Efficiency percentage
0.1	93.73
0.2	59.97
0.5	58.44
1	57
2	56
3	56
4	55.53
5	56.46