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A 18.9-nA Standby Current Comparator with Adaptive Bias Current Generator

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***Abstract*— An ultra-low power comparator circuit using adaptive bias current generator (ABCG) is proposed. The circuit consists of an input differential pair, an ABCG, and a latch circuit. The ABCG generates an adaptive bias current, and the latch circuit determines the output logic and controls the operation of the ABCG for ultra-low power dissipation. The ABCG and the latch operate only when the input voltage levels and the logic of the latch do not correspond with each other. Measurements demonstrated that the circuit can achieve high-speed and low-power dissipation due to such operation. The standby current was 18.9 nA with a 10-nA bias current. The power dissipation was 88.5 nW at a 1-kHz input frequency and 3-V supply voltage.**

I. Introduction

Subthreshold LSIs, or LSIs that consist of MOS transistors operating in the subthreshold region, have recently attracted attention as devices for achieving ultra-low power dissipation [1]. However, their design methodology is still in the early stage of development, and ultra-low power circuit design techniques are thus desired. Several studies have been carried out to achieve such LSIs [1]–[4]. We propose an ultra-low power comparator circuit suitable for extremely low power analog LSIs.

A comparator circuit is a fundamental building blocks for performing various analog and digital signal processing in LSIs. One of the most effective and direct ways to reduce the comparator power dissipation is to reduce the bias current to less than one micro-ampere. A conventional two-stage comparator circuit uses nano-ampere current levels, so it takes a long time to evaluate and compare input analog voltages and to output the resultant digital signals. Therefore, a comparator biased with a nano-ampere current cannot be used as is.

An adaptive biasing technique for CMOS amplifier has been presented [5]. This technique is useful for a CMOS operational transconductance amplifier (OTA) design, but it is not practical for application to a comparator design because it increases power dissipation [6]. A comparator circuit design that uses an adaptive bias current generator was recently presented to address the slow transition time of the low-power comparator [7]. However, this circuit could not achieve both the high-speed and low-power requirements. This is because although the adaptive bias technique can increase the speed of the comparator operation, more current than necessary is generated, resulting in high power dissipation. Moreover, because the circuit requires several differential pairs, its configuration becomes large.

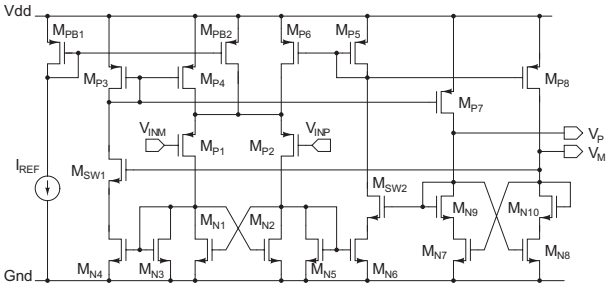

Fig. 1. Proposed comparator consisting of ABCG and latch circuit

In light of this background, we propose a comparator circuit that achieves high-speed and low-power operation by using an adaptive bias current generator (ABCG). The proposed comparator uses two positive feedback loops for the current generation, and it exploits a latch for an output signal decision and current control of the ABCG. Details of the circuits follow.

II. Comparator design

A. Circuit configuration

Our proposed comparator circuit is shown in Fig. 1. It consists of a nano-ampere bias current generator [3], an input differential pair, an adaptive bias current generator (ABCG) with hysteresis control, and a latch [8]. The nano-ampere current generator is used to achieve ultra-low power dissipation [3]. The latch circuit determines output logic V_P and V_M, and it controls the ABCG with MOS transistor switches, $\mathrm{M_{SW1}}$ and $\mathrm{M_{SW2}}$. The ABCG includes two positive feedback loops, L1 and L2: L1 is $\mathrm{M_{P1}}$-$\mathrm{M_{N3}}$-$\mathrm{M_{N4}}$-$\mathrm{M_{SW1}}$-$\mathrm{M_{P3}}$-$\mathrm{M_{P4}}$, and L2 is $\mathrm{M_{P2}}$-$\mathrm{M_{N5}}$-$\mathrm{M_{N6}}$-$\mathrm{M_{SW2}}$-$\mathrm{M_{P5}}$-$\mathrm{M_{P6}}$. In the loops, $\mathrm{M_{N4}}$ and $\mathrm{M_{N6}}$ are designed so that the aspect ratios are K ($>$1) times larger than those of $\mathrm{M_{N3}}$ and $\mathrm{M_{N5}}$. With the current gain factor K being larger than 1, the positive feedback loops will generate a large amount of adaptive bias current I_{ADP}. The ABCG generates I_{ADP} in either loop L1 or L2 depending on the input voltages of V_{INP} and V_{INM}. The latch circuit accepts the current through $\mathrm{M_{P7}}$ or $\mathrm{M_{P8}}$ and changes its internal logic. After determining the logic, the latch shuts off the I_{ADP} through the $\mathrm{M_{SW1}}$ or $\mathrm{M_{SW2}}$ switch transistor because I_{ADP} is now unnecessary for the operation.

The following sub-section describes details of the circuit operation.

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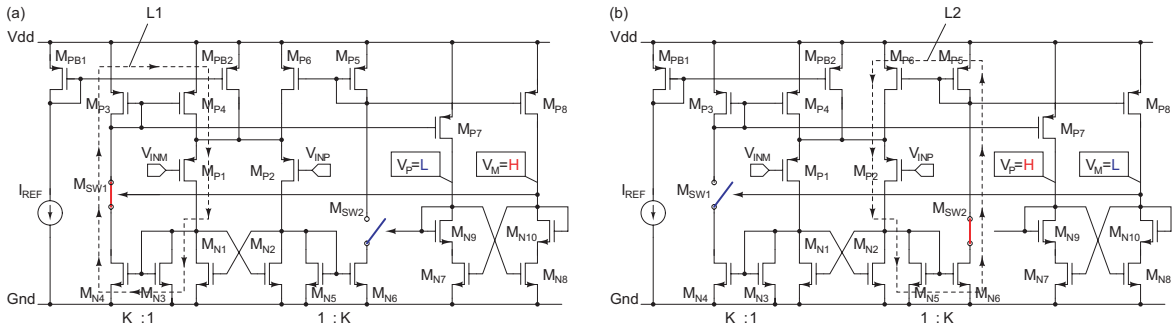

Fig. 2. Comparator operation: (a) initial latch logic is set to V_P=Low and V_M=High, respectively (L1 loop is activated), (b) initial latch logic is set to V_P=High and V_M=Low, respectively (L2 loop is activated).

B. Operation principle

The comparator operation is shown in Fig. 2. The logic of the latch plays an important role for our comparator, so we describe the circuit operation according to the logic of the latch.

1) Logic of latch: V_P=Low, V_M=High.

   When V_{INP} is higher than V_{INM} (V_{INP}>V_{INM}), most of the bias current I_{REF} flows in $\mathrm{M_{P1}}$, and the adaptive bias current I_{ADP} in loop L1 is generated and amplified through the current gain factor of K. The generated I_{ADP} is copied by current mirror $\mathrm{M_{P3}}$-$\mathrm{M_{P7}}$ and changes V_P from Low to High. Therefore, the latch flips its internal logic so that the logic of V_M flips from High to Low. The V_M turns $\mathrm{M_{SW1}}$ off and the I_{ADP} is shut off.

2) Logic of latch: V_P=Low, V_M=High.

   When V_{INP} is lower than V_{INM} (V_{INP}<V_{INM}), most of the bias current I_{REF} flows in $\mathrm{M_{P2}}$. However, because the V_P keeps switch transistor $\mathrm{M_{SW2}}$ off, loop L2 remains inactive and I_{ADP} is not generated. In this case, the internal logic of the latch holds.

3) Logic of latch: V_P=High, V_M=Low.

   When V_{INP} is higher than V_{INM} (V_{INP}>V_{INM}), most of the bias current I_{REF} flows in $\mathrm{M_{P1}}$. However, because V_M keeps switch transistor $\mathrm{M_{SW1}}$ off, loop L1 remains inactive and I_{ADP} is not generated. In this case, the internal logic of the latch holds.

4) Logic of latch: V_P=High, V_M=Low.

   When V_{INP} is lower than V_{INM} (V_{INP}<V_{INM}), most of the bias current I_{REF} flows in $\mathrm{M_{P2}}$, and adaptive bias current I_{ADP} in loop L2 is generated and amplified through the current gain factor K. The generated I_{ADP} is copied by current mirror $\mathrm{M_{P5}}$-$\mathrm{M_{P8}}$ and changes V_M from Low to High. Therefore, the latch flips its internal logic so that the logic of V_P flips from High to Low. The V_P turns $\mathrm{M_{SW2}}$ off, and the I_{ADP} is shut off.

Table I summarizes the operation of the proposed comparator. The I_{ADP} is generated only when the logic of the latch and input voltage levels do not correspond with each other (States 1 and 4).

TABLE I
OPERATION OF PROPOSED COMPARATOR

State	Latch logic		Input voltage levels	Latch action	I_{ADP}	Next state
	V_P	V_M				
1	Low	High	$V_{INP} > V_{INM}$	FLIP	YES	3
2	Low	High	$V_{INP} < V_{INM}$	KEEP	NO	-
3	High	Low	$V_{INP} > V_{INM}$	KEEP	NO	-
4	High	Low	$V_{INP} < V_{INM}$	FLIP	YES	2

The generated I_{ADP} can be modeled as follows. First, we assume that the current flowing in a lower-gate potential transistor is αI_{REF}, where α $(0.5 < \alpha < 1)$ is a ratio depending on the input voltages. The adaptive bias current can be given by

$$I_{ADP} = \alpha I_{REF}\left(1 + K + K^2 + \cdots\right). \quad (1)$$

We designed K to be larger than 1, so an extremely large adaptive current can be obtained. The generated I_{ADP} changes the internal logic of the latch, and then the current is shut off. In this way, high-speed and low-power operation of the comparator can be achieved.

C. Current control for V_{INP}=V_{INM}

As discussed in the previous sub-section, the comparator circuit we propose can achieve high-speed and low-power operation by using the adaptive bias current generation technique and the latch circuit. The adaptive bias current I_{ADP} is generated only when the logic levels in the latch and input voltage levels do not correspond with each other. Therefore, the current dissipation can be minimized.

However, the current dissipation will increase in both loops under the special condition where the input voltages are equal (i.e., V_{INP}=V_{INM}) and when a timing difference in turning the switches on/off occurs. In this condition, because half of the I_{REF} flows in input transistors $\mathrm{M_{P1}}$ and $\mathrm{M_{P2}}$ and both loops are active, adaptive bias currents are generated in both loops. This phenomenon will increase power dissipation.

To solve this problem, we added transistors $\mathrm{M_{P9}}$ and $\mathrm{M_{P10}}$ as shown in Fig. 3. The aspect ratios of $\mathrm{M_{P9}}$ and $\mathrm{M_{P10}}$ are designed to be K' times larger than those of $\mathrm{M_{P5}}$ and $\mathrm{M_{P3}}$. $\mathrm{M_{P9}}$ and $\mathrm{M_{P10}}$ monitor currents flowing in $\mathrm{M_{P5}}$ and $\mathrm{M_{P3}}$, respectively. By using these transistors, we can reduce the current flowing in transistors $\mathrm{M_{P3}}$ and $\mathrm{M_{P5}}$ when adaptive

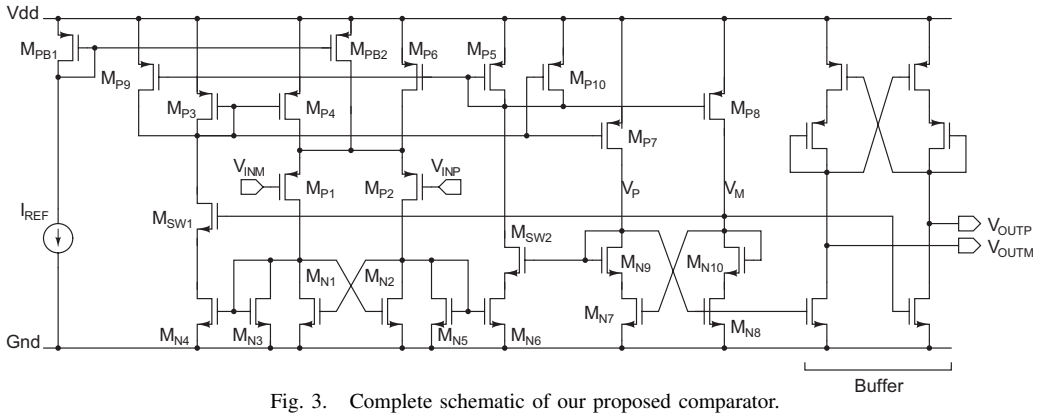

Fig. 3. Complete schematic of our proposed comparator.

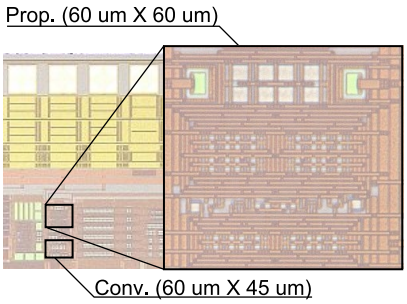

Fig. 4. Chip micrograph

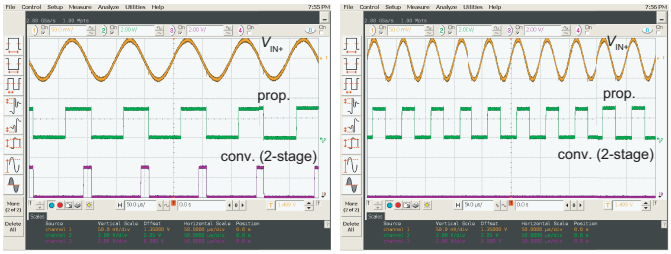

Fig. 5. Measured input and output waveforms at 10-kHz (left) and 20-kHz (right) input frequency. The I_{REF} was set to 30 nA.

bias currents are generated in both loops at the same time. This means that current increase in the positive feedback loops can be reduced which is explained as follows.

First, we assume that the currents flowing in the input transistors $\mathrm{M_{P1}}$ and $\mathrm{M_{P2}}$ and transistors $\mathrm{M_{P3}}$ and $\mathrm{M_{P5}}$ are $I_{REF}/2$ and I_1, respectively. Therefore, the following equation is obtained by Kirchhoff's current law.

$$I_1 = K\frac{I_{REF}}{2} - K'I_1. \quad (2)$$

From Eq. (2), I_1 is given by

$$I_1 = \frac{K}{1+K'}\frac{I_{REF}}{2}. \quad (3)$$

Therefore, the I_{ADP} can be expressed as

$$I_{ADP} = \frac{I_{REF}}{2}\left(1+\frac{K}{1+K'}+\frac{K^2}{(1+K')^2}\cdots\right). \quad (4)$$

When we design $K/(1+K')$ to be smaller than 1, Eq. (4) can be simplified as

$$I_{ADP} = \frac{1+K'}{1+K'-K}\frac{I_{REF}}{2}. \quad (5)$$

From Eq. (5), I_{ADP} can be suppressed even when the same input voltages are applied to the input differential pair and when timing mismatch in turning the switch transistors on/off occurs.

III. Results

We fabricated a prototype chip of our comparator (Fig. 3) using a 0.35-μm, 2-poly, 4-metal standard CMOS process. A micrograph of our prototype chip and a partial enlarged view of the proposed comparator circuit are shown in Fig. 4. A conventional 2-stage comparator was also designed for comparison. Our comparator and 2-stage comparator occupied 3600 μm^2 and 2700 μm^2, respectively. The ratio of $1:K:K'$ was set at $1:2:3$ in this design. For the measurement, the supply voltage, input reference voltage, and input sine wave were set to 3.0, 1.5, and 1.5+0.05$\times\sin 2\pi f_{IN}t$ V, respectively.

Figure 5 shows the measured waveforms of the comparators at a 10-kHz (left) and 20-kHz (right) input frequency. The bias current I_{REF} was set at 30 nA. In the left Fig. 5, both of the comparators could generate an output pulse correctly. The output positive edge of the 2-stage comparator was delayed significantly. This is because the bias current cannot drive the output voltage due to the small bias current of 30 nA in the 2-stage comparator. In constrast, our proposed circuit operated without large delay. In the right figure, the 2-stage comparator could not operate correctly. This is because the delay of the circuit exceeded the input sine wave period. However, our proposed comparator operated correctly.

Maximum frequency $f_{\max}$ as a function of bias current I_{REF} is shown in Fig. 6. The $f_{\max}$ is the highest frequency at which the comparators can generate an output pulse. As the bias current increased, the maximum frequency of the circuits also increased. The $f_{\max}$ of the proposed and conventional comparators at I_{REF}=10 nA was 40 and 5 kHz, respectively, the proposed circuit can operate 8 times faster than the conventional 2-stage comparator. Note that the standby current of our comparator biased with I_{REF}=10 nA was 18.9 nA. Moreover, when the input frequency was fixed, the proposed comparator could operate with lower bias current I_{REF}.

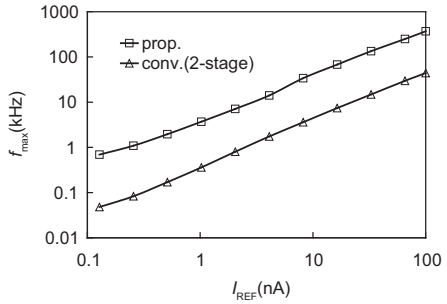

Fig. 6. Measured maximum operating frequency $f_{\max}$ as function of bias current I_{REF}

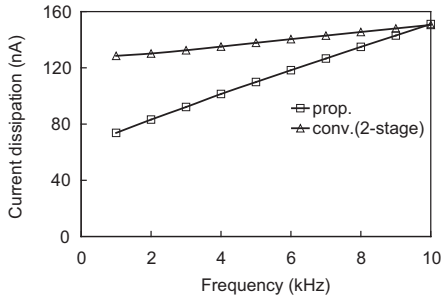

Fig. 7. Measured current dissipation as function of input frequency. Bias currents for proposed comparator and 2-stage comparator were set to 33 and 50 nA, respectively.

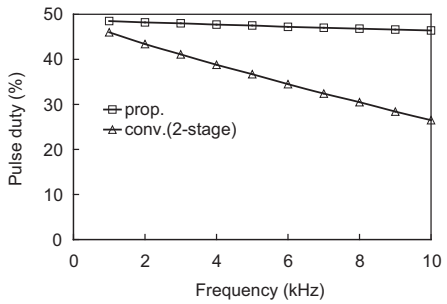

Fig. 8. Measured duty cycle as function of input frequency. Bias currents for proposed comparator and 2-stage comparator were set to 33 and 50 nA, respectively.

The measured current dissipation as a function of input frequency is shown in Fig. 7. The bias currents I_{REF} for the proposed and the 2-stage comparators was set to 33 and 50 nA, respectively. The bias currents were set so that the comparators dissipated the same current at a 10-kHz input frequency. At this condition, both circuits dissipated 151 nA. The current of the proposed comparator was lower than that of the 2-stage comparator as the input frequency decreased. Figure 8 shows the output pulse duty of the comparators with the same input frequency range as in Fig. 7. The duty of the proposed circuit was close to 50%. However, the duty of the 2-stage comparator decreased as input frequency increased. Because the bias current cannot charge the output, the output positive edge was delayed as input frequency increased. These results agreed with the results in Fig. 5.

Table II summarizes the comparator performances. The results show that our proposed comparator can achieve high-speed and low-power operation. As such, the circuit is useful for power-aware LSI applications.

TABLE II

PERFORMANCE SUMMARY OF COMPARATORS

Comparator	Prop.	Conv.(2stage)
Technology	0.35-μm CMOS	
Area	3600 μm^2	2700 μm^2
V_{DD}	3.0 V	
I_{REF}	10 nA	
Current and pulse duty (f_{IN}:1 kHz)	29.5 nA, 50%	28.5 nA, 37%
$f_{\max}$	40 kHz	5 kHz
Standby current	18.9 nA	31.7 nA
I_{REF}	33 nA	50 nA
Current and pulse duty (f_{IN}:10 kHz)	151 nA, 46%	151 nA, 27%
Current and pulse duty (f_{IN}:1 kHz)	73.7 nA, 49%	129 nA, 46%
$f_{\max}$	130 kHz	22 kHz
Standby current	63.5 nA	153 nA

IV. CONCLUSION

We proposed an ultra-low power comparator circuit with an adaptive bias current generator (ABCG). The ABCG generates an operating current, and a latch circuit controls the operation of the ABCG for ultra-low power dissipation. The ABCG and the latch operate only when the input signal levels and the logic of the latch do not correspond with each other. Measurement results demonstrated that the circuit can achieve high-speed and low power dissipation due to such operation. The standby current was 18.9 nA with a 10-nA bias current. The power dissipation was 88.5 nW at a 1-kHz input frequency and 3-V supply voltage.

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REFERENCES

[1] A. P. Chandrakasan, D. C. Daly, J. Kwong and Y. K. Ramadass, "Next generation micro-power systems," *Symp. VLSI Circuits Dig.*, pp. 2-5, June 2008.

[2] K. Ueno, T. Hirose, T. Asai, and Y. Amemiya, "A 300-nW, 15-ppm/℃, 20-ppm/V CMOS voltage reference circuit consisting of subthreshold MOSFETs," IEEE Journal of Solid-State Circuits, vol. 44, no. 7. pp. 2047-2054, 2009.

[3] T. Hirose, Y. Osaki, N. Kuroki, and M. Numa, "A nano-ampere current reference circuit and its temperature dependence control by using temperature characteristics of carrier mobilities," Proceedings of the 36rd European Solid-State Circuits Conference, pp. 114 - 117, September 2010.

[4] T. Hirose, K. Ueno, N. Kuroki, M. Numa, "A CMOS Bandgap and Sub-Bandgap Voltage Reference Circuits for Nanowatt Power LSIs," IEEE Asian Solid-State Circuits Conference, pp. 77-80, November 2010.

[5] M. Degrauwe, J. Rijmenants, E. A. Vittoz, and H. J. De Man, "Adaptive biasing CMOS amplifiers," IEEE Journal of Solid-State Circuits, vol. 17, pp. 522 - 528, June 1982.

[6] R. J. Baker, CMOS Circuit Design, Layout, and Simulation, Second Edition, IEEE Press, 2004.

[7] S. Akita, "Adaptively Controlled circuit," U.S. Patent 6,922,319, July 2005.

[8] H. Shao, C. Tsui, "Low Energy Level Converter Design for Sub-V_{TH} Logics," ASP-DAC 2009, pp. 107-108, 19-22, January 2009.