A 65nm CMOS Comparator with Modified Latch to Achieve 7GHz/1.3mW at 1.2V and 700MHz/47μW at 0.6V

Bernhard Goll and Horst Zimmermann

Vienna University of Technology
Institute of Electrical Measurements and Circuit Design
Gusshausstrasse 25/354, A-1040 Vienna, Austria

Outline

- Introduction
- Schematic of the comparator
- Block diagram of the test chip
- Micrograph of the test chip
- Measurement results
- Key data of the comparator at a glance
- Comparison

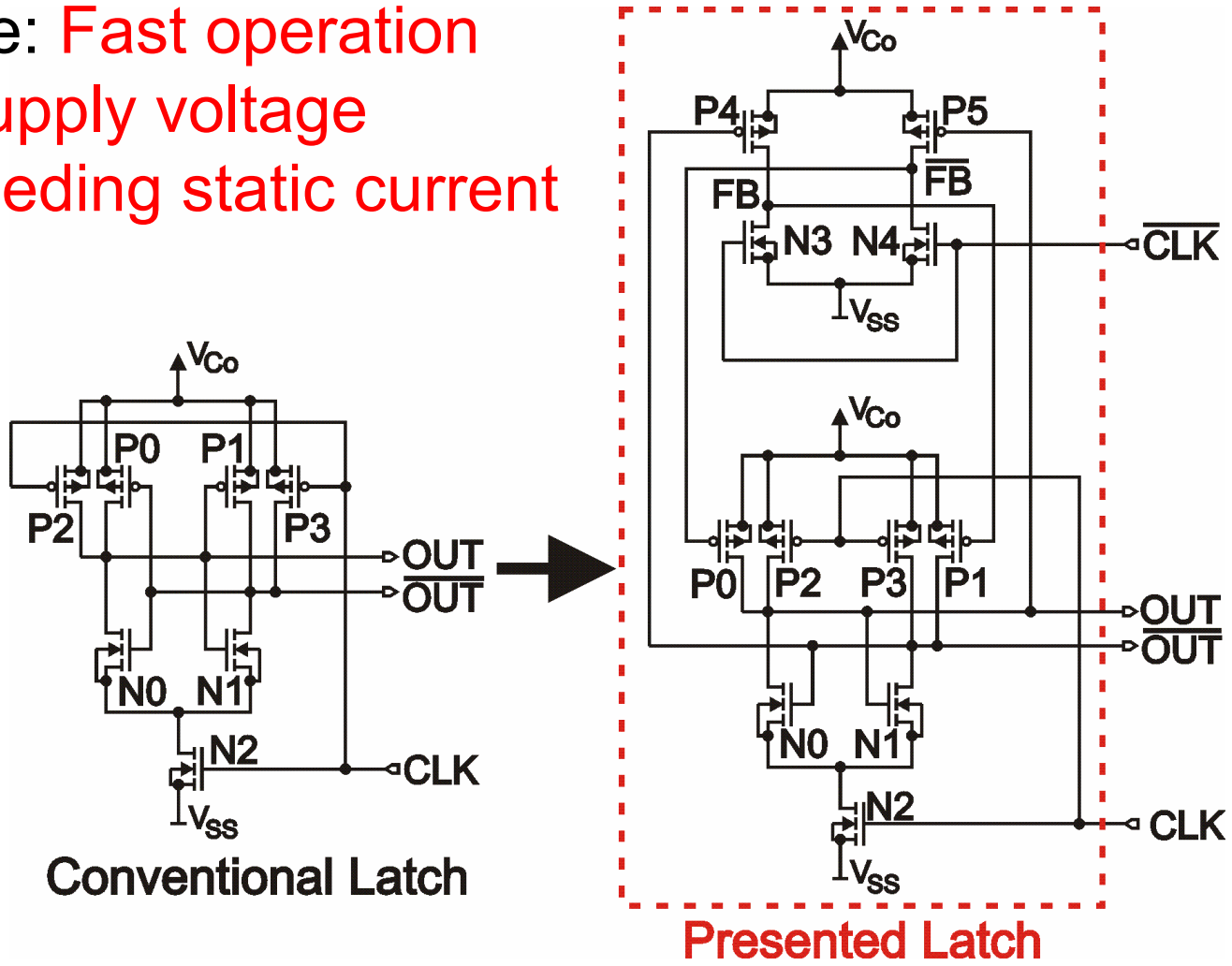
Introduction: motivation for fast, low-power, low voltage comparators

- Low supply voltages in modern CMOS processes
- Low power consumption for mobile devices
- Flash ADCs:
  parallel clocked, mostly regenerative comparators
  - -> low power consumption
  - -> small chip area needed per comparator
  - -> pre-amplifiers are added in front of the comparator to enhance resolution
- Data receivers/repeaters
- Latch-type sense amplifiers in memories

Schematic of the comparator

Splitting up of a conventional latch into two paths between the supply rails:

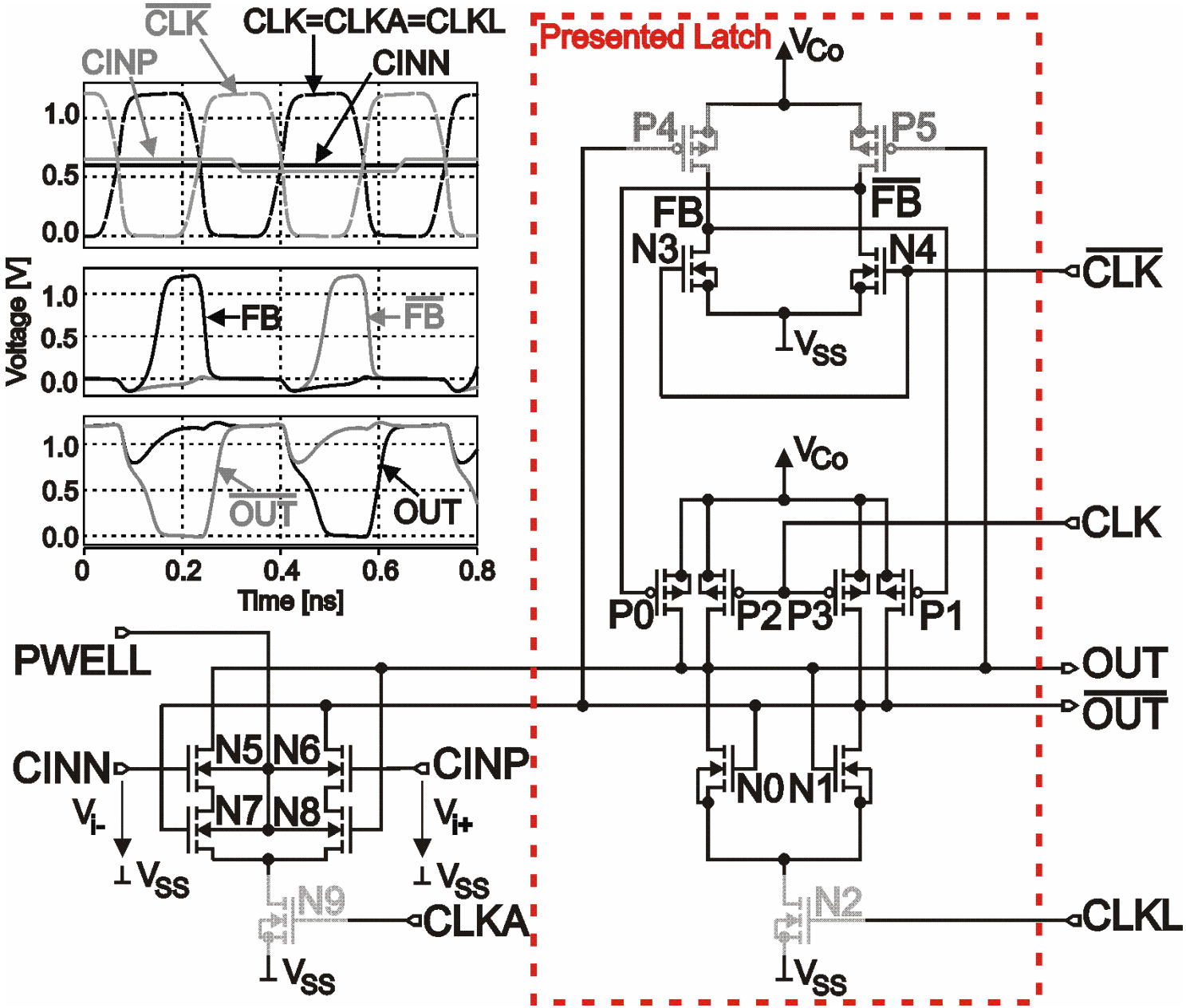
-> Advantage: Fast operation
at a low supply voltage
without needing static current



Schematic of the comparator

Reset phase:

- CLK=CLKA= =CLKL at V_{SS}
- OUT and $\overline{OUT}$ are pulled up to V_{Co}
- FB and $\overline{FB}$ are pulled down to V_{SS}



Schematic of the comparator

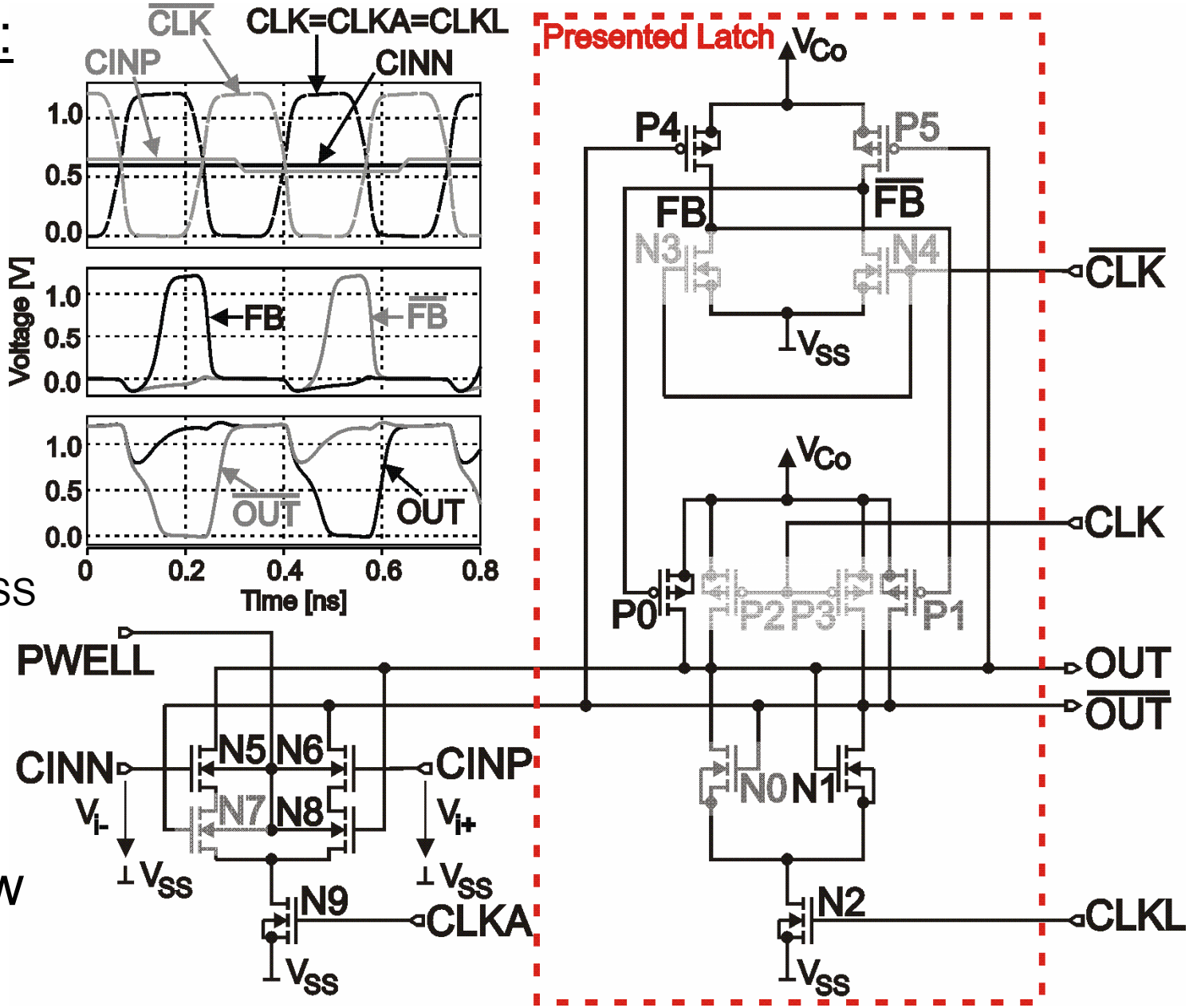
Comparison phase:

- CLK=CLKA= =CLKL at V_{Co}

Case $V_{i+}>V_{i-}$:

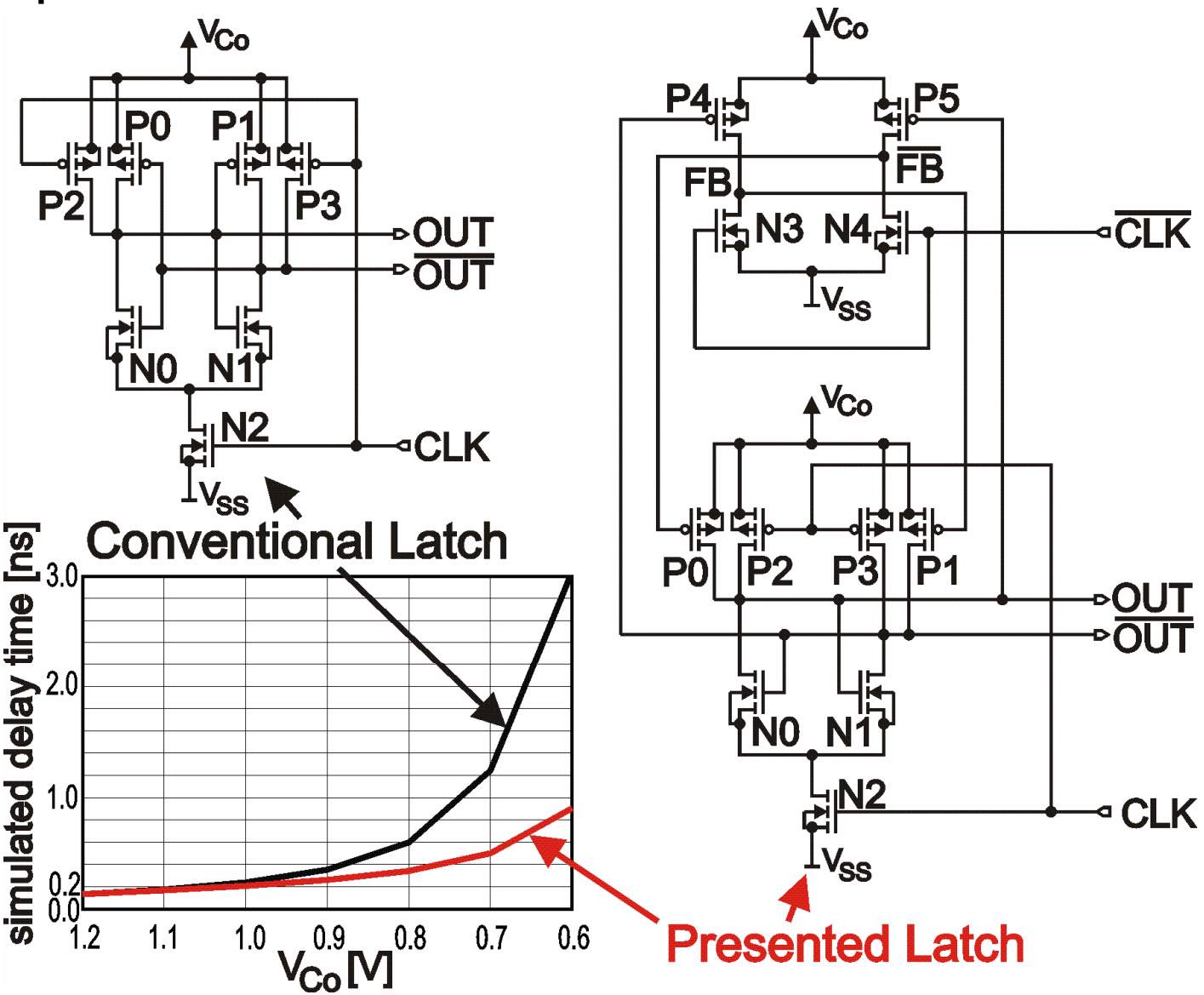
- pos. feedback:
  - FB -> V_{Co}
  - $\overline{FB}$ stays near V_{SS}
  - OUT -> V_{Co}
  - $\overline{OUT}$ -> V_{SS}

- N7, N8 avoids static current flow after decision

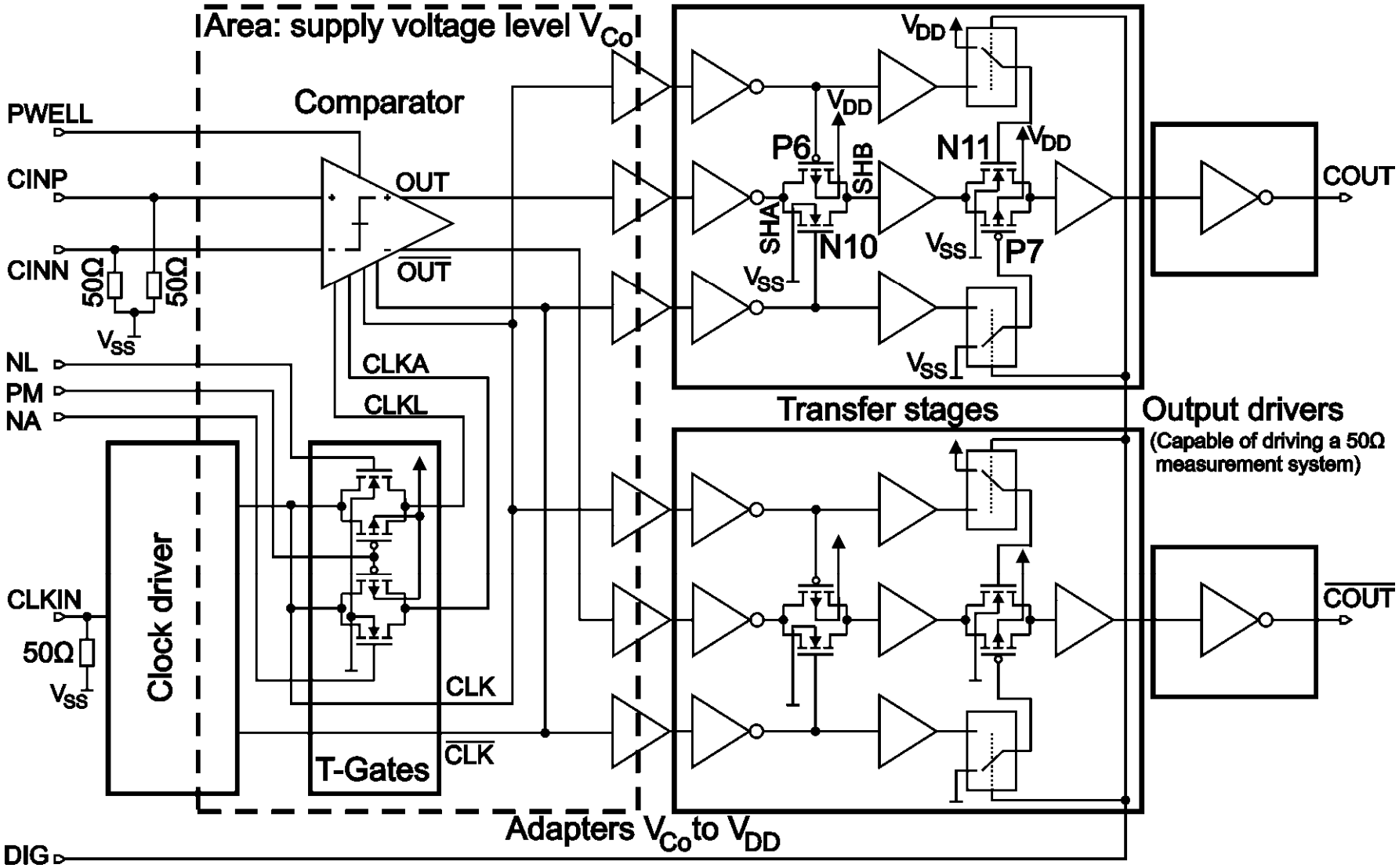


Schematic of the comparator

Comparison of the conventional latch with the presented latch:



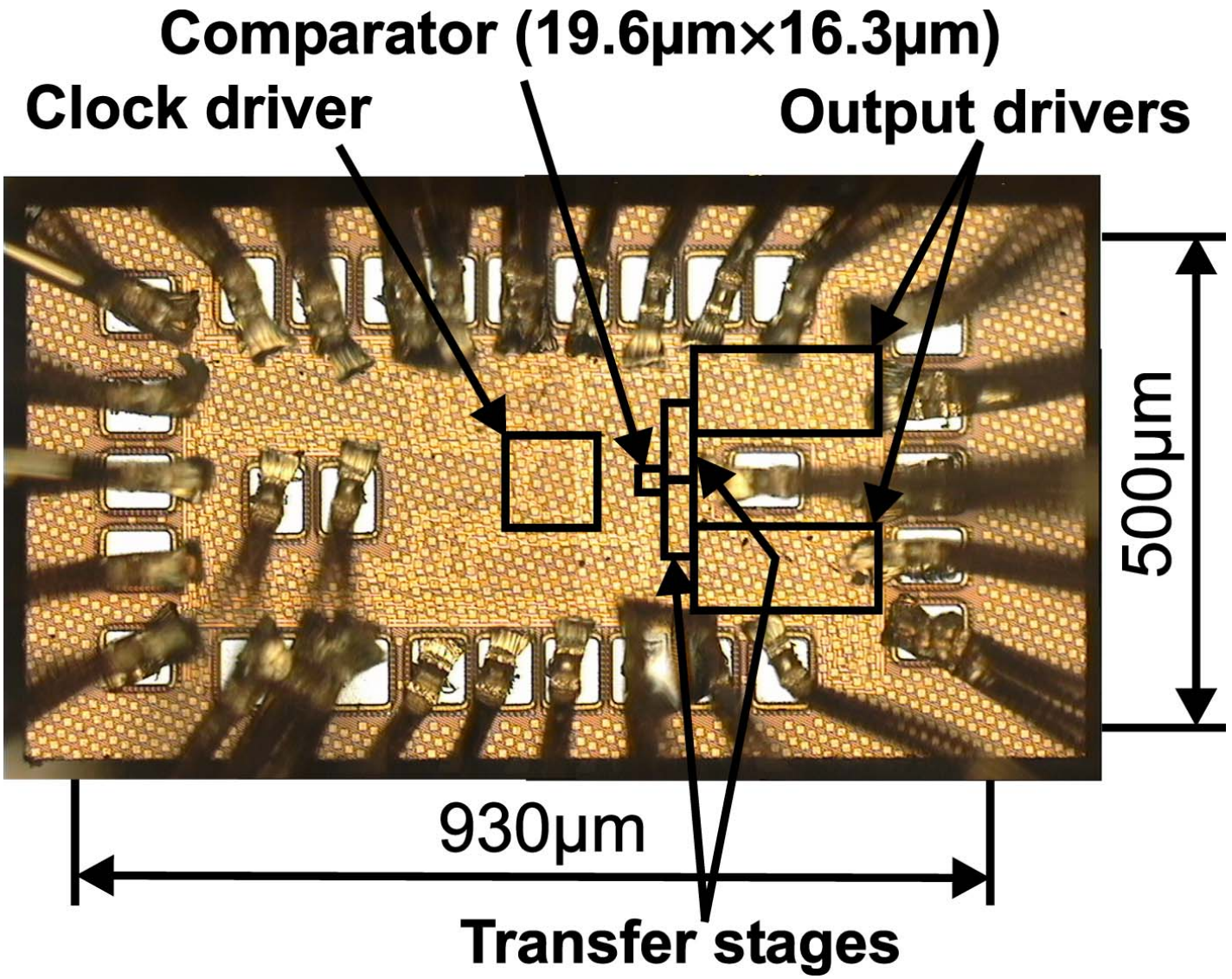
Block diagram of the test chip



T-Gates: For sensitivity tuning at lower clock rates [6]

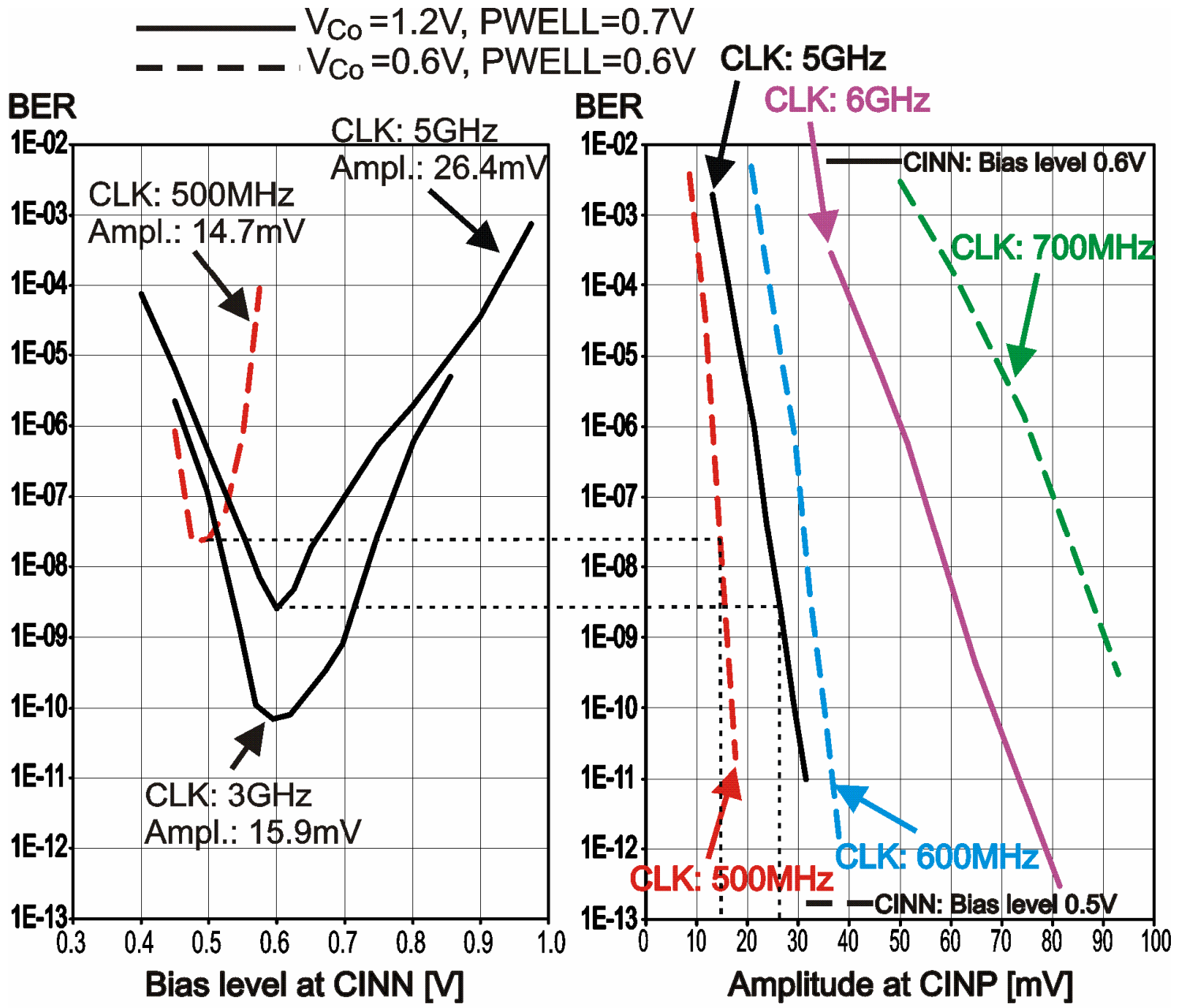
[6] ***IEEE ESSCIRC***, pp. 408-411, 2007

Micrograph of the test chip



Technology: Low-Power 65nm/1.2V CMOS process

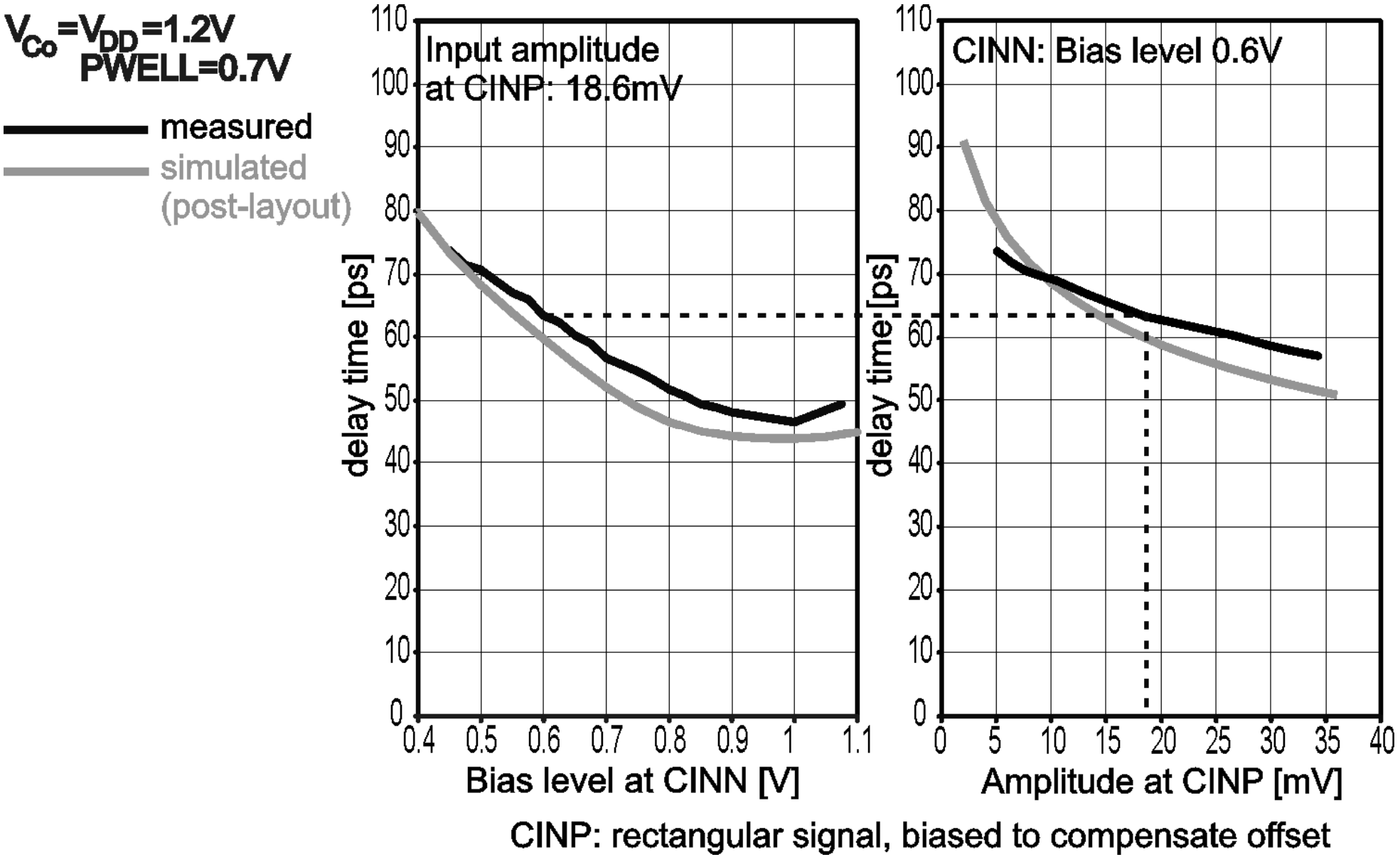
Measurement results: BER



CINP: PRBS 2^{31}-1, biased to compensate offset

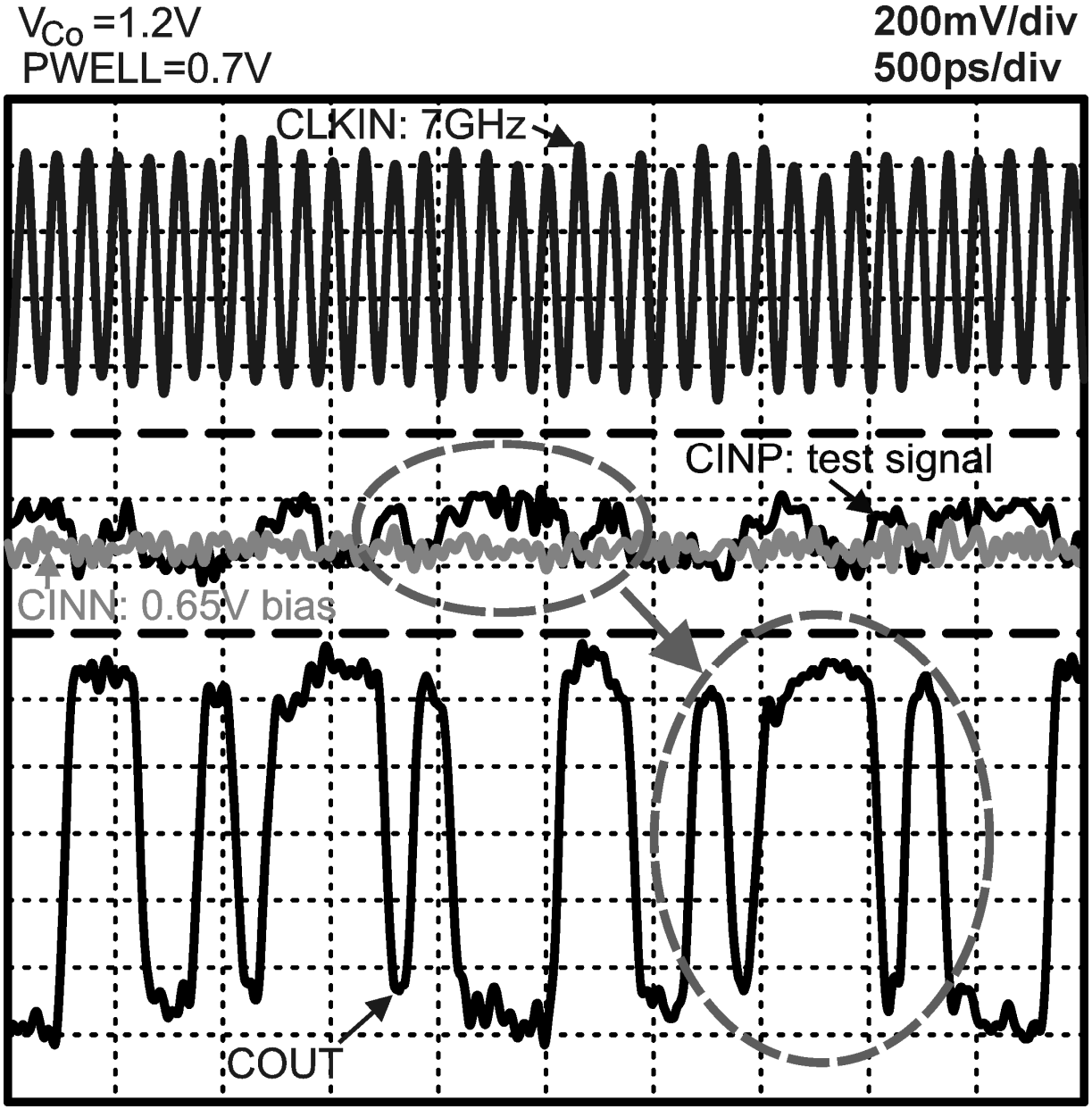
Measurement results

Delay time (time shift between CLK and $\overline{OUT}$) of the comparator



Measurement results

Oscilloscope screenshots at 7GHz clock and V_{Co}=1.2V



Key data of the comparator at a glance

- Technology: 65nm Low-Power CMOS ($V_t \approx 0.4V$)
- Maximum clock frequency: 700MHz @ V_{Co}=0.6V
  7GHz @ V_{Co}=1.2V
- Minimum input voltage difference to achieve a BER<10^{-9}:
  - V_{Co}=0.6V: 16mV @ 500MHz, 90.2mV @700MHz
  - V_{Co}=1.2V: 15mV @ 3GHz, 20mV @ 4GHz
    (sensitivity tuning @ 3GHz and @ 4GHz),
    27.2mV @ 5GHz, 63mV @ 6GHz,
    281mV @ 7GHz
- Power consumption: 47µW @ 0.6V/700MHz
  1.3mW @ 1.2V/7GHz
- Offset: σ=22mV @ 1.2V, σ=47mV @ 0.6V (simulation)
- Size of comparator: 19.6µm×16.3µm

Comparison

Techn.	Supply voltage	Clock	Sensitivity BER=10^{-9}	Power cons.	Offset (σ)	Ref.
0.13µm CMOS	1.5V	n.m.	n.m.	n.m.	8.5mV	[2]
0.18µm CMOS	1.8V	1.4GHz	n.m.	350µW	29.7mV w/o offset comp.	[3]
90nm CMOS	1.2V	2GHz meas. 3GHz sim.	inp. noise σ_n=1.5mV	225µW @2GHz	8mV	[4]
0.12µm CMOS V_t≈0.29V	1.5V	6GHz	29.4mV @5GHz	2.65mW @6GHz	23mV sim.	[5]
	0.5V	0.6GHz	60.5mV @0.6GHz	18µW	57mV sim.	
0.12µm CMOS	1.5V	3GHz	9.2mV @3GHz	584µW @3GHz	16.1mV sim.	[6]
65nm LP-CMOS V_t≈0.4V	1.2V	7GHz	15mV @3GHz 27.2mV @5GHz	1.3mW @7GHz	22mV sim.	This work
	0.6V	0.7GHz	16mV @0.5GHz 90.2mV @0.7GHz	47µW @0.7GHz	47mV sim.	

[2] ***IEEE JSSC***, vol. 39, pp. 1148-1158, 2004.

[3] ***IEEE JSSC***, vol. 39, pp. 837-840, 2004.

[4] ***IEEE ISSCC***, pp. 314-315, 2003.

[5] ***IEEE ISSCC***, pp. 316-317, 2003.

[6] ***IEEE ESSCIRC***, pp. 408-411, 2007.

Thank you for your attention !

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