A 6-bit 1.2-GS/s Low-Power Flash-ADC in 0.13-μm Digital CMOS

Christoph Sandner, *Member, IEEE*, Martin Clara, Andreas Santner, Thomas Hartig, and Franz Kuttner

***Abstract*—We present a 6-bit 1.2-GS/s flash-ADC with wide analog bandwidth and low power, realized in a standard digital 0.13 μm CMOS copper technology. Employing capacitive interpolation gives various advantages when designing for low power: no need for a reference resistor ladder, implicit sample-and-hold operation, no edge effects in the interpolation network (as compared to resistive interpolation), and a very low input capacitance of only 400 fF, which leads to an easily drivable analog converter interface.**

Operating at 1.2 GS/s the ADC achieves an effective resolution bandwidth (ERBW) of 700 MHz, while consuming 160 mW of power. At 600 MS/s we achieve an ERBW of 600 MHz with only 90 mW power consumption, both from a 1.5 V supply. This corresponds to outstanding figure-of-merit numbers (FoM) of 2.2 and 1.5 pJ/convstep, respectively. The module area is 0.12 mm^2.

***Index Terms*—Capacitive interpolation, data converter, flash ADC, sampling.**

I. Introduction

FLASH analog-to-digital converters (ADCs) are still the architecture of choice, where maximum sample rate and low to moderate resolution is required. A typical example is the read-write channel of a disk drive system, where customers often ask for the maximum sample rate that can be achieved by the currently available technology generation.

However, there are additional applications in the wireless area coming up, where only a flash-ADC gives sufficient accuracy at the required large analog bandwidth, for example in ultra-wide-band (UWB) systems. Since a lot of wireless applications are hand-held as well, this poses an important constraint on the specification of the ADC, which is lowest possible power consumption. The reason for this is that in many integrated systems the ADC is the dominant block in terms of power consumption for the whole analog front-end.

In this paper we describe the concept, design, and measurement results of a 6-bit flash-ADC, optimized for low power at sufficiently high data rates and analog bandwidth. With 1.2 GS/s and an effective resolution bandwidth (ERBW) of 700 MHz, the ADC fulfils the requirements currently under discussion for multiband OFDM UWB systems [1]. Due to its large ERBW, different receiver topologies, like low-IF or zero-IF can be supported, both at Nyquist rate, and under sub-sampling operation. However, the presented ADC architecture is not limited to these applications.

Manuscript received November 18, 2004; revised January 31, 2005.

The authors are with Infineon Technologies Austria, Development Center Villach, A-9500 Villach, Austria (e-mail: christoph.sandner@infineon.com).

Digital Object Identifier 10.1109/JSSC.2005.847215

Although almost all recently published high-speed full-flash-ADCs employ resistive interpolation and averaging requiring a dedicated sample-and-hold at the converter input, the capacitive interpolation structure with distributed front-end sample-and-hold has advantages in terms of power, even at GS/s speed. The outstanding figure of merit (FoM) numbers prove the efficiency of the implemented architecture, when compared to state-of-the-art 6-bit flash ADCs.

II. Converter Architecture

Averaging is a well-known technique to improve the linearity of a flash-type ADC beyond the matching limit of the single comparator [2], [4]. Multiple gain-stage architectures allow the use of interpolation to reduce the number of front-end amplifiers and thus the input capacitance of the converter. By scaling the amplifiers in the analog preprocessing chain from front to back also the overall power consumption can be optimized under the given gain/bandwidth constraints. In what follows, two different strategies for implementing a flash ADC employing interpolation and averaging are described.

Resistive interpolation employs averaging resistors between the outputs of adjacent amplifiers [3]. A common problem of such architectures is the need for overrange comparators to maintain linearity at the edges of the conversion range. Special circuit techniques [5] allow reducing the number of overrange comparators, but they rely on matching the termination resistor with the output resistance of the overrange blocks. For the conversion of high-frequency input signals an external sample-and-hold circuit is almost always required, which consumes a significant fraction of the total power budget in wide-band applications.

Capacitive interpolation, on the other hand, uses a purely reactive averaging network between the outputs of adjacent amplifiers [6], [7]. Fig. 1 illustrates the transition from a fully parallel flash-ADC analog front-end to an interpolated structure. In this example every second amplifier in each stage can be omitted by using capacitive interpolation with a factor of two. A big advantage of capacitive interpolation is that it requires neither power consuming overrange comparators nor any static averaging termination. Also, no external sample-and-hold is required, because the interpolation capacitors at each stage are readily used as sampling capacitors implementing a multistage input- and output-offset-sampling architecture with distributed front-end sample-and-hold. In general, a distributed sample-and-hold poses a more severe burden on the driving stage than a dedicated sample-and-hold, because the capacitor to be charged is multiplied by the interpolation factor at the

0018-9200/$20.00 © 2005 IEEE

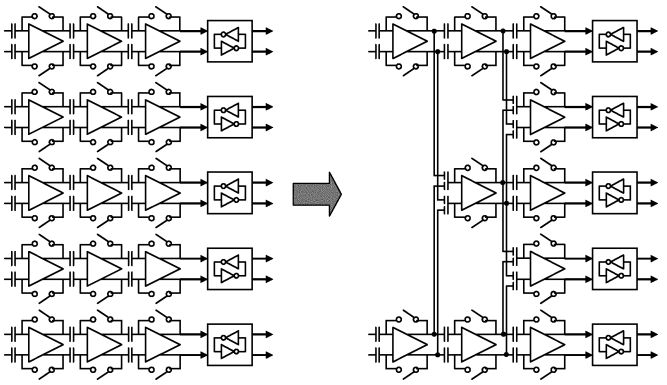

Fig. 1. Transition from parallel flash-ADC front-end to capacitive interpolation.

front-end of the converter. Additionally, the sampling capacitors in this architecture also retain the information of the last sample, because no discharge occurs during the amplification phase. This history might introduce an additional code dependency in the partly nonlinear settling behavior and thus worsen the harmonic distortion [8]. However, the additional power consumption needed in the driver to overcome this problem for a resolution of 6 bits with an optimized converter front-end is still much smaller than for a dedicated sample-and-hold.

The principle of capacitive interpolation combined with the distributed front-end sample-and-hold is explained in Fig. 2, showing a portion of the converter input. The ratio of the interpolation capacitors C_1 and C_2 defines the potential of the virtual reference for the middle amplifier. If both capacitors are identical the virtual reference will ideally be the average of upper and lower reference $(\mathrm{REFP}+\mathrm{REFN})/2$. By choosing different capacitor ratios, different virtual references and thus different interpolation factors can be implemented. Likewise, the interpolation factor at the converter input is given by the total number of front-end amplifiers minus 1. The total input capacitance of the converter in the sampling phase is given by the sum of the front-end capacitors plus wiring parasitics.

The inverting first stage amplifiers then drive the interpolating capacitive network of the second stage, here implementing an interpolation factor of 2 by choosing the interpolation capacitors to be of equal size.

One critical issue of the capacitive interpolation structure is the capacitive divider formed by the sampling capacitor C_S and the parasitic input capacitance of the amplifier C_P during the amplification phase (see Fig. 3). The overall gain of each stage is given by the product of the intrinsic gain of the amplifier and the capacitive divider ratio. In order to minimize the total input capacitance of the converter, the sampling capacitors will be chosen as small as possible, for a resolution of 6 bits ultimately limited by capacitor mismatch and kT/C noise. For minimum gain loss the amplifiers' input devices should therefore be as small as possible. In this case, input offset sampling (IOS) helps to further reduce the input devices' effective mismatch, thus allowing additional downscaling to save power and area.

The principle of input offset sampling is shown in Fig. 3. During Φ_1 the input voltage v_{IN} and the offset voltage v_{OS} of the amplifier with gain A are both sampled on the capacitor

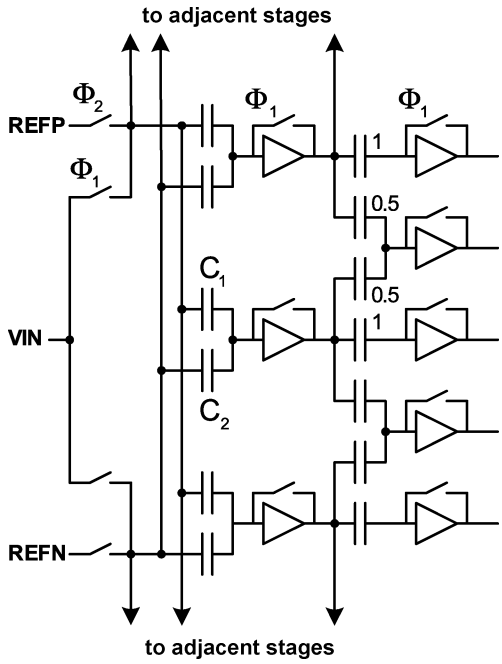

Fig. 2. ADC front-end portion using capacitive interpolation.

C_S. During Φ_2 the difference between the input voltage and the reference voltage v_{REF} is amplified to the output, but the input referred offset $v_{\mathrm{OS,in}}$ is suppressed [13]. If the input capacitance of the amplifier C_P is included, then the residual input referred offset in phase 2 is given by

$$v_{\mathrm{OS,in}} = \frac{v_{\mathrm{OS}}}{1+A} \cdot \frac{C_S + C_P}{C_S}. \tag{1}$$

The capacitive divider at the input of the gain stage thus leads to a gain loss, or equivalently, to an increase in the input referred offset voltage. Since the gain of a single amplifier cannot be chosen arbitrarily large, the total gain must be distributed over a number of cascaded stages. In the multistage architecture of Fig. 4 each stage not only performs input-offset sampling (IOS) of its own offset, but also output offset sampling (OOS) of the previous stage. If the capacitance ratio C_S/C_P and the amplifier gain A are equal for all stages then the residual offset referred to the input of one amplifier/comparator slice with N gain stages is ideally given by

$$v_{OS,in} \approx \frac{1}{A^{N-1}} \frac{1}{1+A} \cdot v_{OS,N} \cdot \left(1 + \frac{C_P}{C_S}\right)^N. \tag{2}$$

Equation (2) assumes that the offset of all stages except the last one $(v_{\mathrm{OS,N}})$, which also includes the comparator, is completely cancelled by the combination of input- and output-offset sampling along the amplifier chain. The offset voltage of the last stage divided by the total gain of the amplifier cascade approximately gives the residual input referred offset. Although this is a rather crude approximation for a practical design, (2) can nevertheless be used to perform a first dimensioning of the principal converter parameters. Averaging then helps to reduce the offset further [9].

With the size of the sampling capacitor at each stage fixed by either noise (kT/C) or mismatch considerations (as in this

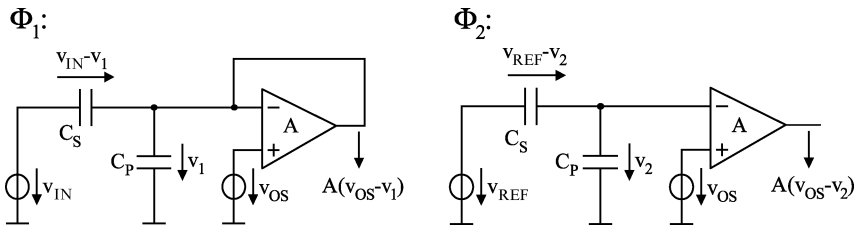

Fig. 3. Input offset sampling for a single stage.

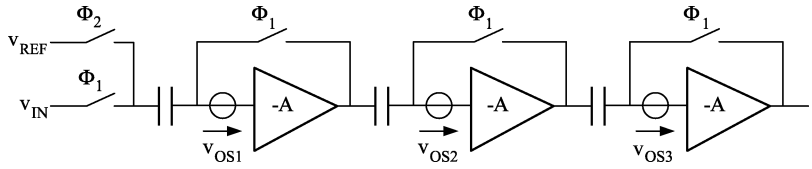

Fig. 4. Multi-stage input and output offset sampling.

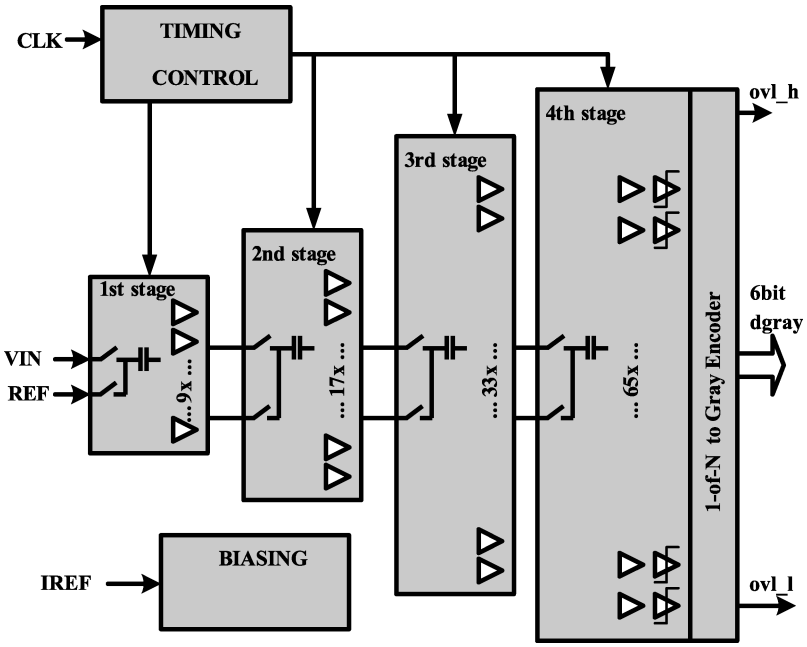

Fig. 5. Implemented ADC block diagram.

design), the total load capacitance $C_{L,n}$ for each amplifier at stage n can be calculated as

$$C_{L,n} \approx I_n \cdot C_{S,n+1} \cdot \frac{1 + \frac{C_S}{C_P}\left(\frac{1}{3} - \frac{1}{3I_n^2}\right)}{1 + \frac{C_S}{C_P}} + C_{\text{wire}}. \qquad (3)$$

I_{n} is the interpolation factor at the output of stage n and C_{wire} is the parasitic wiring capacitance. Since the -3 dB bandwidth for a given power consumption and gain of a differential pair (Fig. 6) is inversely proportional to the load capacitance C_L, the speed is also nearly inversely proportional to the interpolation factor. The optimum interpolation architecture for high speed and low power thus yields $I_{\text{n}} = 2$.

III. Implemented Design

The block diagram of the implemented A/D-converter is shown in Fig. 5. The circuitry is fully differential, although drawn single ended for simplicity. The input signal is sampled in the first clock phase ϕ_1 by the front-end amplifiers forming a distributed sample-and-hold, while the subsequent stages sample the offset voltage. During the second clock phase ϕ_2 the reference voltage is applied to the bottom plates of the front-end sampling capacitors and the difference between input voltage and reference voltage is amplified before it is latched by the comparators at the end of this clock phase.

The capacitive load at each amplifier output and thus the bandwidth of the amplifier is linearly related to the interpolation factor. To optimize the power-bandwidth product of the amplifier, while still profiting from the averaging property, the minimum possible interpolation factor of 2 is chosen at the output of each gain stage. This is also the best choice for distortion reasons. To reach 64 decision levels after three interpolating stages, an interpolation factor of 8 is implemented at the converter input, thus formed by nine parallel input amplifiers. A fourth gain stage directly drives the latching comparator, leading

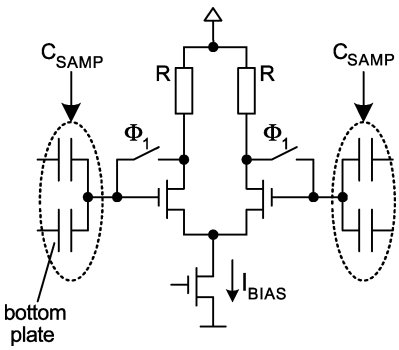

Fig. 6. Amplifier block diagram.

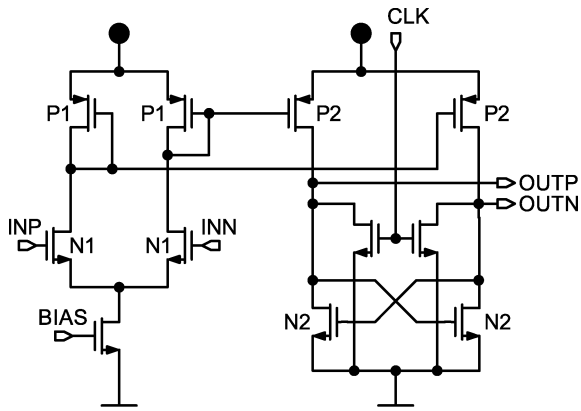

Fig. 7. Final comparator latch.

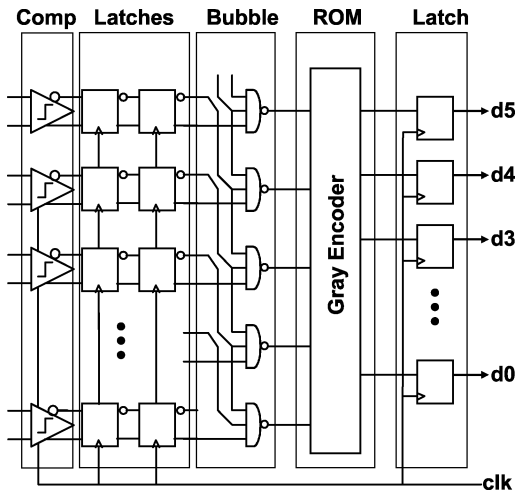

Fig. 8. Digital backend of ADC.

to an 8-2-2-2 interpolation topology. Since the overall interpolation factor is 64, only two reference voltages are needed at the input of the 6-bit ADC, thus avoiding the silicon area and power penalty of a low-resistive reference ladder. Instead, the reference voltages are generated by capacitive voltage division during the amplification phase ϕ_2 (referring to the single-ended representation in Fig. 2)

$$V_{\mathrm{REF\ i}} = V_{\mathrm{REFN}} + \frac{C_1}{C_1 + C_2}(V_{\mathrm{REFP}} - V_{\mathrm{REFN}}). \quad (4)$$

Using the interpolation topology described above, and taking into account matching and noise requirements for the sampling capacitors at the input stage, it was possible to reach a very low input capacitance of only 400 fF. The subsequent gain stages are progressively scaled down by a factor of 2, thus achieving a very compact layout, since all four gain stages end up to have the same height (Fig. 9).

Regarding dc performance, the input referred offset is the most important specification. Since, due to minimum sizing for maximum speed, the offset of the final comparator stage is dominant. Estimations indicate that this offset voltage can be as high as 80 mV one-sigma value, including dynamic effects. This offset must be reduced by achieving sufficient gain in the preceding amplifiers, thus reducing the input referred offset. Each amplifier block (Fig. 6) consists of a differential pair with resistive load. Both MOS and resistor devices must be taken into account for mismatch calculations. pMOS switches connected between inputs and outputs provide the offset sampling. The bandwidth of the amplifier is set to be 3–4 times larger than the sample rate of the converter. The gain of each stage is chosen to be around 2.5 for achieving maximum bandwidth of the whole chain. This yields a total gain of around 39, and thus the 80-mV offset voltage given above are reduced to around 2-mV input referred offset, which compares to 1/16 LSB for 1-V reference voltage.

The final comparator latch is shown in Fig. 7. The input voltage difference is first converted into a current difference and then fed to the cross-coupled latch, formed by transistors N2. During the sampling phase, when the amplifiers sample the analog input signal, the CLK signal is high, thus keeping the comparator outputs OUTP and OUTN at the same level. During the amplification phase CLK goes low, thus releasing the outputs, and the latch can decide whether the input voltage difference was positive or negative. The use of a single nMOS clock switch between both outputs is not possible, due to the low supply voltage of 1.5 V. The time constant formed by the output node parasitic capacitances and the g_m of transistors N2 must be chosen small enough to achieve the desired sample rate. The main advantages of this topology are the almost rail-to-rail output swing, and the reduced kick-back to the pre-amplifiers due to the current mirrors.

For decreasing the BER the 64 outputs of the comparator row are again latched twice by differential latches, before entering a first order bubble correction stage, which also converts the thermometer code to a 1-out-of-N code (see Fig. 8). Finally, this code is converted into a 6-bit Gray code using a ROM-table based on a current steering topology optimized for high frequency operation. For test purposes the digital data is down sampled by a factor of 64, thus standard CMOS pads can be used for the digital outputs.

Fig. 9 shows the layout plot of the implemented test chip. It was fabricated in a 0.13-μm digital CMOS technology with standard-threshold MOS devices (no low-V_T option), single poly, four thin copper metals, and two thick copper metals. The capacitors are of metal-metal sandwich type. Since the converter topology includes a distributed sample and hold, the layout of distributed signal and clock paths must be done as symmetrical as possible to avoid timing mismatches.

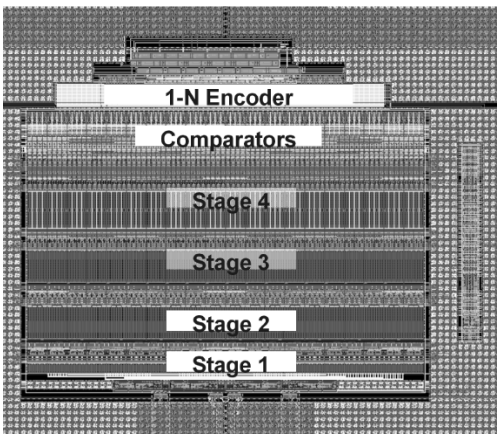

Fig. 9. ADC layout.

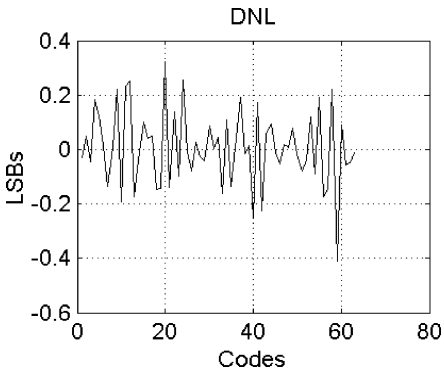

Fig. 10. Measured DNL typ. $<$0.4 LSB (at 600 MS/s).

IV. Measurements

All measurements are done on a standard PCB with ceramic TQFP-44 package and no socket, at room temperature and nominal supply of 1.5 V. Both analog input and sampling clock are applied differentially to the chip by using baluns.

Fig. 10 shows the DNL of the converter, measured at 600 MS/s with a full-scale 50-MHz sine-wave input employing a histogram method. The measured peak DNL of 0.4 LSB thus already includes dynamic effects at that sampling rate. Peak INL is measured $<$0.6 LSB.

In Fig. 11 the maximum sampling rate of the ADC is explored for nominal bias current. The analog signal frequency is kept constant at 121 MHz, while the sampling clock frequency is varied on the x-axis. The ADC shows 5 bit ENOB up to a sample rate of 1.4 GS/s. The clock frequency limit for the digital circuitry is around 1.6 GS/s.

Fig. 12 shows the signal-to-noise ratio (SNR) and signal-to-noise-plus-distortion ratio (SNDR) for a sample rate of 600 MS/s, at reduced bias current to save power. At 51-MHz input frequency, the SNDR yields 35.5 dB, with a spurious free dynamic range (SFDR) of 52 dB and a total harmonic distortion (THD) of 49 dB, thus proving the excellent linearity of the capacitive interpolation topology. The SNDR drops by 3 dB at an ERBW of 600 MHz. The power consumption in this mode is only 90 mW.

In Fig. 13 the same measurement is done for 1.2 GS/s at nominal bias current. SNDR starts at 35.8 dB for low frequencies

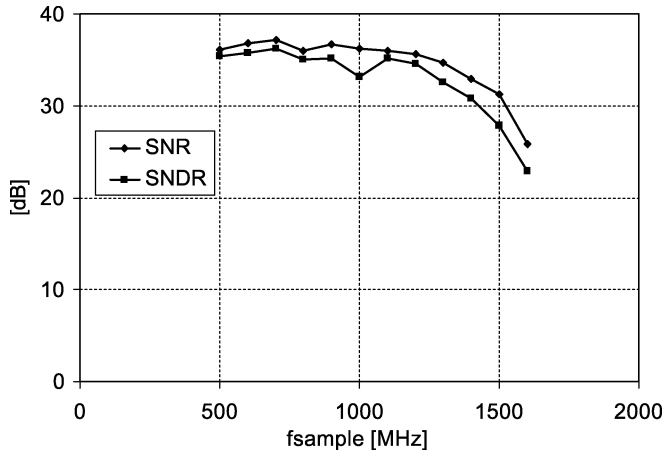

Fig. 11. Measured dynamic performance versus fsample (fsig $=$ 121 MHz).

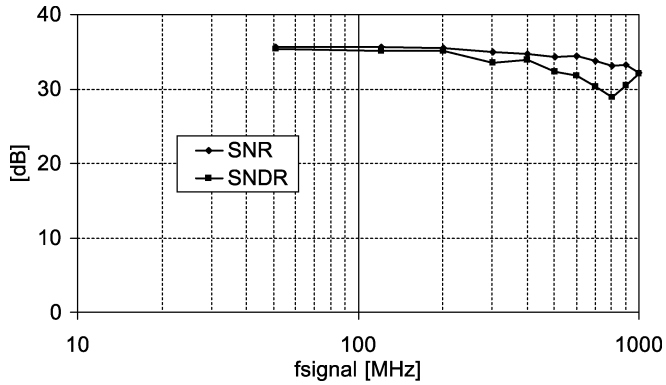

Fig. 12. Measured dynamic performance versus fsignal at 600 MS/s.

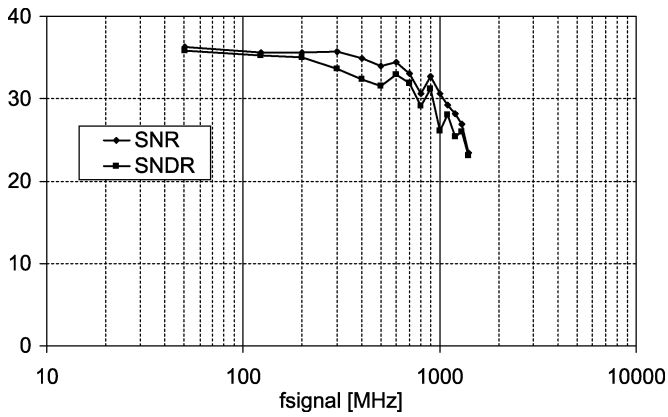

Fig. 13. Measured dynamic performance versus fsignal at 1.2 GS/s.

(THD is 46 dB), dropping by 3 dB at an ERBW of 700 MHz. The power consumption of the converter is 160 mW. These measurements show that this ADC topology is very well suited for applications with wide analog bandwidth requiring a low-power converter. Fig. 14 shows a measured spectrum of the ADC output at 1.2 GS/s and 701-MHz analog input frequency (close to the ERBW). The star markers indicate the location of the harmonics. The SFDR is better than $-$42 dBc, demonstrating excellent linearity even above Nyquist frequency.

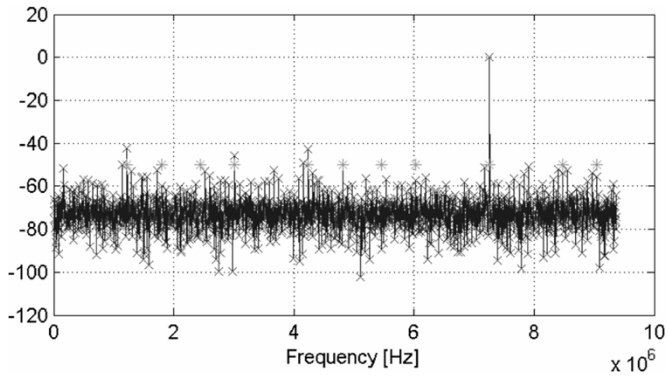

Fig. 14. Measured ADC spectrum at 1.2 GS/s and 701 MHz input frequency.

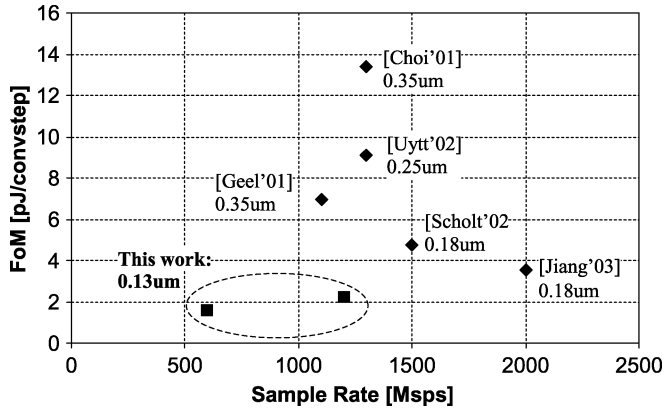

Fig. 15. Comparison to state-of-the-art 6-bit flash ADCs.

TABLE I
ADC PERFORMANCE SUMMARY

	@600MSps	@1.2Gsps
DNL	<0.4LSB	-
INL	<0.6LSB	-
ENOB @ DC	5.6bit	5.7bit
ERBW	600MHz	700MHz
Power	90mW	160mW
FoM	1.5pJ/conv	2.2pJ/conv
Supply Voltage	1.5V	
Reference Voltage	1.0V	
Test chip area	0.12mm²	
Technology	Standard 0.13µm CMOS, Met-Met-Cap, 1Poly, 6 Cu-metals	

To do a comparison with state-of-the-art 6-bit flash-ADCs, a figure of merit (FoM) is calculated [11] as

$$\mathrm{FoM} = \frac{\mathrm{Power}}{2^{\mathrm{ENOB,DC}} \cdot 2 \cdot \mathrm{ERBW}}\ [\mathrm{pJ/convstep}]. \qquad (5)$$

For our ADC we achieve a FoM of 2.2 pJ/conv at 1.2 GS/s, and 1.5 pJ/conv at 600 MS/s. As can be seen in Fig. 15 these are the best FoM numbers for flash ADCs ever published [4], [6]–[9]. Although a smaller feature size technology is used in this work, the achieved performance nevertheless proves the efficiency of the capacitive interpolation architecture with distributed sample-and-hold for flash ADCs in the GHz range. The ADC performance summary is shown in Table I.

ACKNOWLEDGMENT

The authors thank C. Kropf for layout work, P. Schreilechner for board design, and P. Bogner, D. Draxelmayr, and G. Knoblinger for fruitful discussions.

REFERENCES

[1] A. Batra *et al.*. (2003, Sep.) Multi-Band OFDM Physical Layer Proposal, IEEE 802.15 WPAN High Rate Alternative PHY Task Group 3a (TG3a). [Online]. Available: http://www.ieee802.org/15

[2] K. Bult and A. Buchwald, "An embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm²," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1887–1895, Dec. 1997.

[3] R. van de Plassche and P. Baltus, "An 8 b 100 MHz folding ADC," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 1988, pp. 222–223.

[4] K. Kattmann and J. Barrow, "A technique for reducing differential non-linearity errors in flash A/D converters," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 1991, pp. 170–171.

[5] P. Scholtens and M. Vertregt, "A 6-b 1.6-Gsample/s flash ADC in 0.18-um CMOS using averaging termination," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1599–1609, Dec. 2002.

[6] K. Kusumoto, A. Matsuzawa, and K. Murata, "A 10 b 20 MHz 30 mW pipelined interpolating CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1200–1206, Dec. 1993.

[7] J. Mulder *et al.*, "A 21 mW 8 b 125 MS/s ADC occupying 0.09 mm² in 0.13 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2004, pp. 260–261.

[8] M. Clara, A. Wiesbauer, and F. Kuttner, "A 1.8 V fully embedded 10 b 160 MS/s two-stage ADC in 0.18 μm CMOS," in *Proc. CICC*, May 2002, pp. 437–440.

[9] M. Choi and A. A. Abidi, "A 6-b 1.3-Gsample/s A/D converter in 0.35 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1847–1858, Dec. 2001.

[10] G. Geelen, "A 6 b 1.1 GSample/s CMOS A/D converter," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2001, pp. 128–129.

[11] X. Jiang, Z. Wang, and M. F. Chang, "A 2 GS/s 6 b ADC in 0.18 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2003, pp. 322–323.

[12] K. Uyttenhove and M. Steyaert, "A 1.8-V 6-bit 1.3-GHz flash ADC in 0.25 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1115–1122, Jul. 2003.

[13] B. Razavi and B. A. Wooley, "Design techniques for high-speed, high-resolution comparators," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1916–1926, Dec. 1992.

Christoph Sandner (S'93–M'95) was born in Munich, Germany, in 1968. He received the Dipl.-Ing. degree in electrical engineering from the Technical University of Graz, Austria, in 1995.

Since 1995, he has been with the Microelectronics Development Center of Siemens AG, now Infineon Technologies, in Villach, Austria. His main interest is the design of analog and mixed-signal modules, with current focus on high-performance high-speed clock generation circuits, and high-speed analog-to-digital and digital-to-analog converters.

Martin Clara was born in Innsbruck, Austria, in 1970. He received the M.S. degree in electrical engineering from the Vienna University of Technology, Vienna, Austria, in 1996.

In 1997 he joined Infineon Technologies' Design Center in Villach, Austria, where he is currently engaged in analog and mixed-signal design. His interests include high-speed high-resolution A/D- and D/A-converters, linear circuits, and CMOS implementations of analog front-ends for communication systems.

Andreas Santner was born in Villach, Austria, in 1976. He received the Dipl-Ing (FH) degree in microelectronic engineering from the Carinthian Tech Institute (CTI), Villach, Austria, in 2003.

Since 1997, he has been with the Microelectronics Development Center of Siemens AG, now Infineon Technologies, in Villach, Austria. His experience includes the layout and the design from analog and mixed-signal modules, with focus on high-speed ADCs and high-speed clock generation circuits.

Thomas Hartig was born in Chemnitz, Germany, in 1977. He received the Dipl.-Ing. degree in electrical engineering from the Technical University of Chemnitz, Germany, in 2002.

Since 2002, he has been with Infineon Technologies Austria AG, Villach, Austria. Besides the design of analog building blocks, his focus is test development for high-speed mixed-signal modules.

Franz Kuttner was born in Judenburg, Austria, in 1960. He received the Dipl.-Ing. degree in electrical engineering from the Technical University of Graz, Austria, in 1986.

Since 1986, he has been with the Microelectronics Development Center of Siemens AG, now Infineon Technologies, in Villach, Austria. His main interest is the design of analog and mixed-signal modules, especially high-performance analog-to-digital and digital-to-analog converters.