EECT 7327 Project
Report due on Apr. 25th
Presentation on May 7th

Design a 1GS/s 6-bit ADC. You can use any architecture of your choice, as well as time interleaving. Possible architectures are flash, SAR, pipeline, folding/interpolation, etc or hybrid of existing architectures.

Present the system blocks, the individual sub-block circuits, and simulation result of the sub-blocks and system level.

The grade of the project will be determined by the technical merits with a weighting factor of 60% (design innovation, ADC performance in term of FOM @ 500MHz input, simulation results to verify the functionality of each blocks and the overall system), the report quality with a weight factor of 20% (quality of the figures, written English with correct grammar, reasonable logic flow), and the presentation quality with a weight factor of 20% (ppt slides, oral presentation, answering of questions).

We have a time slot for final exam on May 7, 2018, 11:00am - 1:45pm in room SOM 11.202 (our usual classroom). We will use this time slot for project presentation. Each group is given 10 minutes for presentation, with 7 minutes presentation time and 3 minutes Q&A time.

The project report (printed) is due on Apr. 25th, and the presentation ppt file is due on May 6th by email.