

Process files

TSMC 0.35 um process files were used for this assignment. Important characteristic values are given.

Parameter	NMOS	PMOS
μC_{ox}	150 $\mu A/V^2$	30 $\mu A/V^2$
Threshold voltage	0.5 V	0.7 V
Lambda	0.01	0.015

Sizing

Designator	W m	L m	Multiplier	Active area
MN1	4E-06	3.50E-07	100	1.40E-10
MN2	4E-06	3.50E-07	100	1.40E-10
MP1	4E-06	3.50E-07	400	5.60E-10
MP2	4E-06	3.50E-07	400	5.60E-10
			Total	0.0014mm ²

First, for the switch transistor, based on the peak load current and drain-source voltage extremes, the sizing is decided.

$$I_D = k \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

Here, a drop of 25 mV and 2 mA peak current is assumed across all switches. The overdrive is assumed to be 0.7 V. The clock signal peaks are at 1.4 V, but the gate sees 1.4 V plus the voltage on the pumping capacitors. This adds to the advantage of this charge pump design. The sizing is chosen to allow common centroid layout.

Pumping capacitors and conversion gain

The conversion gain of this charge pump is expressed by

$$CG = \frac{2}{1 + \frac{1}{2R_{out}C_p f_s}}$$

For the given problem, the conversion gain is 2, thus the denominator of the above equation should be close to 1. Assume $CG = 1.964$, i.e. output voltage of **2.75 V**. Assume switching frequency of 100 kHz. Also, for worst case output resistance

$$R_{out,min} = \frac{V_{out}}{I_{out,max}} = \frac{2.75V}{1mA} = 2750 \text{ ohm}$$

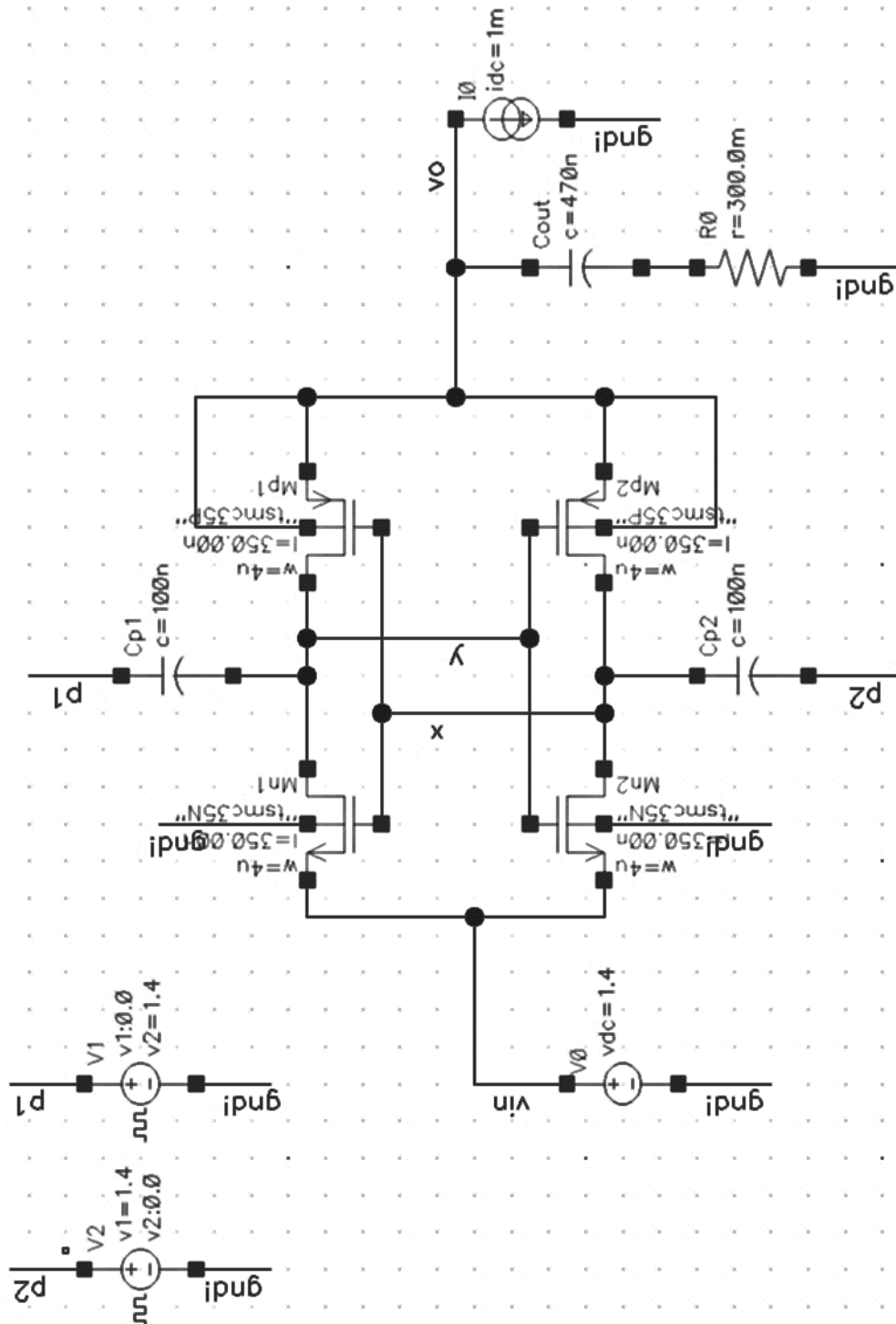
Using above values, we find the pumping capacitor value of 101 nF, which can be rounded off to **100 nF**.

Output Capacitor and output ripple

As per specification, we target a 10-mV ripple. The below equation holds because both phases of the clock allow discharge of the pumping capacitors. This ensures that there are no ESR jumps in the output voltage waveform. Solving below equation for max load of 1 mA and switching frequency of 100 kHz, we get a minimum output capacitor of **470nF**.

$$\Delta V_o = \frac{I_o}{2f_s C_{out}}$$

Circuit



Steady State Waveforms

