High PSR Low Dropout-Regulator for RF SoC applications

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Abstract

Analog RF blocks are integrated on-chip with digital circuits for System on Chip Applications (SoC). The problem with such integration is that Analog and RF blocks is that digital circuits switch violently and can cause ripples further causing distortions in the Analog block as they are susceptible to noise. In this project we aim at designing a High Power Supply Rejection (PSR) Low Drop-Out Regulator (LDO) to provide a constant output voltage to RF/Analog loads. The Drop-Out Voltage is a maximum of 0.2V as more drop across the Power transistor would lead to a lower efficiency. As the power transistor is a PMOS, the Error amplifier used should be such that any ripple caused in the power supply should result in a correlated ripple being fed to the gate of the PMOS because the current in a PMOS depends on the gate-to-source voltage (V_{gs}) and the source in a PMOS is connected to the supply voltage (V_{dd}).

Literature Survey

Various design methods have been proposed to increase the PSR for high frequency operation. Reference [1] discusses the selection of error amplifier based on the pass transistor type. Reference [2] discusses design using cascode devices and multistage design. Reference [3] is an advanced ripple feed forward technique used to cancel the ripple passing through the output resistance of the pass transistor. The results are shown in Table 1. We choose reference [2] to design our system for a simplistic design, while use system blocks from reference [3] for a low headroom performance as we are provided with a larger gate technology node.

Table 1 Summary of results for literature survey

	Reference [2]	Reference [3]
Methodology	Cascode devices	Feed forward ripple cancellation
Quiescent current	NA	50 uA
Load current	150 mA	25 mA
Line regulation	1.5 mV/V	26 mV/V
Load regulation	17.4 mV/mA	48 uV/mA
PSR	40 dB at 1 MHz	56 dB at 10 MHz
Technology node	0.13um	0.13um
Input voltage	> 3 V	> 1.15 V
Output voltage	2.8 V	1 V
Output capacitor	2.7 uF	2 uF

System level design philosophy

Based on the given specifications, it is necessary that a high loop gain and bandwidth be selected for the LDO. This is because the loop gain decides the output voltage accuracy and the bandwidth decides the high frequency PSR specification. Here, a high output voltage accuracy is important as the output voltage is low, and even a small error would result in drastic output change.

As per the specification, the loop gain required is 50dB, thus we design an error amplifier which can meet a high gain specification. However, high gain is limited by limited swing, thus a driver circuit is implemented to drive the gate of the pass transistor. The PSR specification of the system is 35dB at 10 MHz. This can be interpreted as a gain of 1/56 = 0.017. Thus the line regulation should be 17 mV/V.

The system is designed based on the location of poles and zeros. The first pole is located at the output and is formed by the output capacitor and the on resistance of the pass transistor. The second pole is at the output of the error amplifier, the third pole is at the output of the PMOS common source stage and the fourth pole is at the output of the source follower. Thus compensation would require three zeros. However, the second and third pole are located at high frequencies. Thus this becomes a two pole one zero problem. The zero can be introduced using the ESR resistor. The poles and zeros in consideration are tabulated in Table 3.

Table 2 Summary of poles and zeroes

P1	Output pole
P2	Pole of source follower
P3	Pole of the PMOS common source
P4	Pole of the error amplifier
Z1	ESR zero

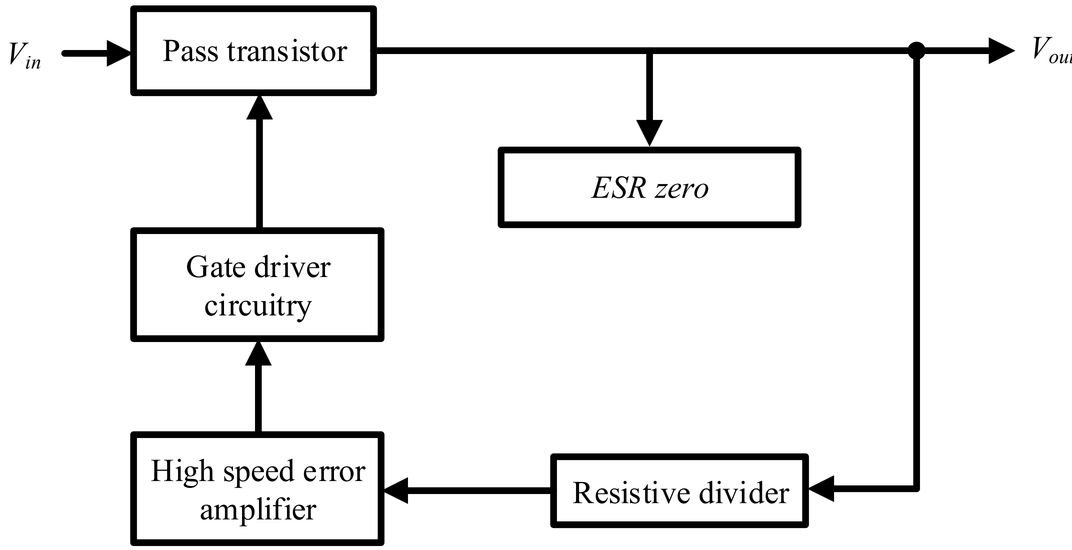
Table 3 Simplified summary of poles and zeros

	Resistance	Capacitance	Frequency
P1	6 ohm	2 µF	12 KHz
P2	900 ohm	6 pF	30 MHz
Z1	0.2 ohm	2 µF	4 MHz

The above table can be used to design the rest of the system. Thus the power transistor is designed for 6 ohm based on the value of P1. Similarly, the Source follower and ESR are designed based on the values of P2 and Z1 respectively.

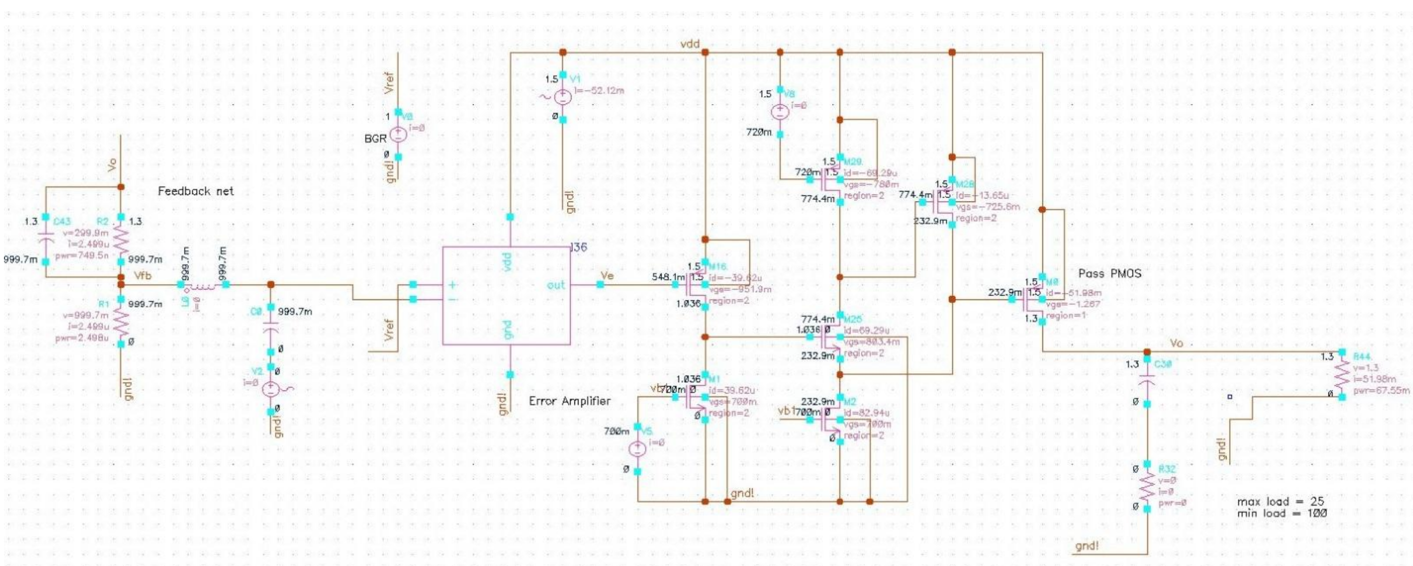
System level block diagram

Fig. 1 System level block diagram



System level circuit diagram

Fig. 2 System level circuit diagram of the LDO



Design Blocks

Power Transistor

This circuit element is used to control the current in the LDO using a negative feedback from an Error Amplifier. If there is a change in the supply voltage then the feedback is given to the error amplifier which amplifies this error and which is fed back to the power FET to restore this change.

For this application, the on resistance of the pass transistor was estimated to be around 6 ohm. Since the output capacitor is rated for 2uF. The first pole of the system is located at 12Khz. The current capacity is estimated to be 10mA/mm based on the process parameters. Thus the size of the power transistor is 5mm.

Table 4 Power transistor specification

Transistor width	4.4 mm
Gate capacitance	6 pF
Drop-out voltage	0.2V
Maximum current	50mA
Minimum current	15mA
Minimum on resistance	6 ohm

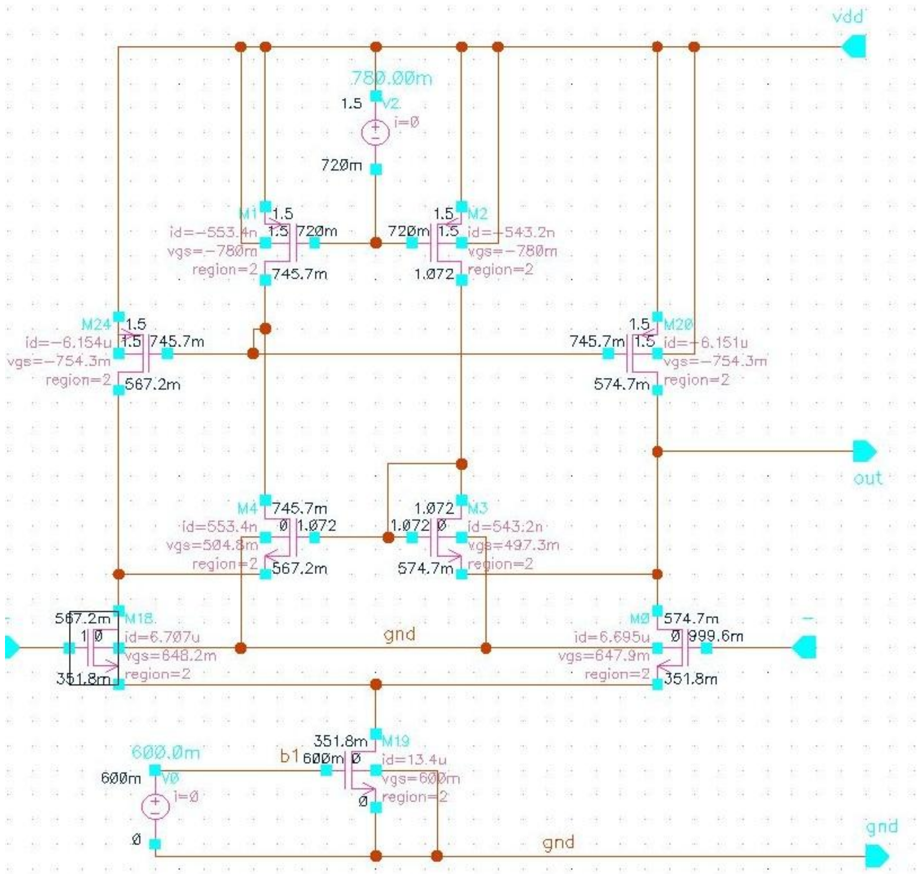
Error Amplifier

The Error amplifier is designed for a high gain high bandwidth operation, so that it can achieve two objectives; (i) To provide an error signal (ii) To provide a high bandwidth path for high frequency transients. The error amplifier is a gain boosted differential pair. The gain boosting is achieved by nesting a differential pair to control the biasing of the PMOS load. This provides a negative feedback to the load bias, effectively increasing the output resistance by the gain of the nested differential pair. This allows for high frequency operation without pole-zero doublets, and eliminates the need of Miller compensation, which limits the bandwidth of the full system. The design is shown in Fig. 3.

Table 5 Error amplifier specification

Gain-Bandwidth	90 MHz
DC-gain	55 dB
Tail current	12 µA
Load capacitance	0.1 pF
Phase margin	65 degrees

Fig. 3 High speed error amplifier



Resistive feedback network

The feedback network is designed for 1.3 V output for a 1.5 V supply. The quiescent current is 2.5 uA, the bandgap voltage used is 1 V.

$$V_o = \left(1 + \frac{R_{f1}}{R_{f2}}\right) V_{ref}$$

Table 6 Feedback network specification

Rf1	120000 ohm
Rf2	400000 ohm
Quiescent current	2.5 µA
Bandgap voltage	1 V
Vout	1.3 V

Fig. 4 Feedback network

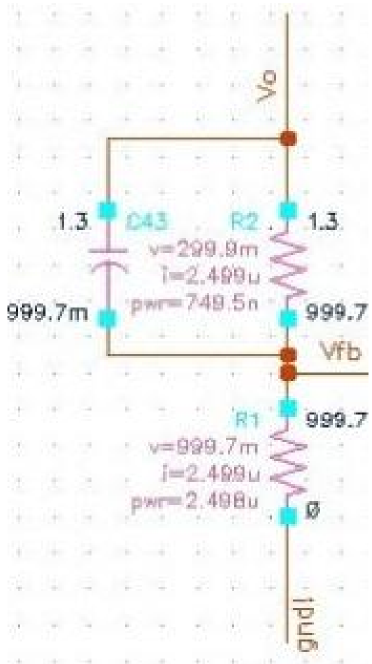
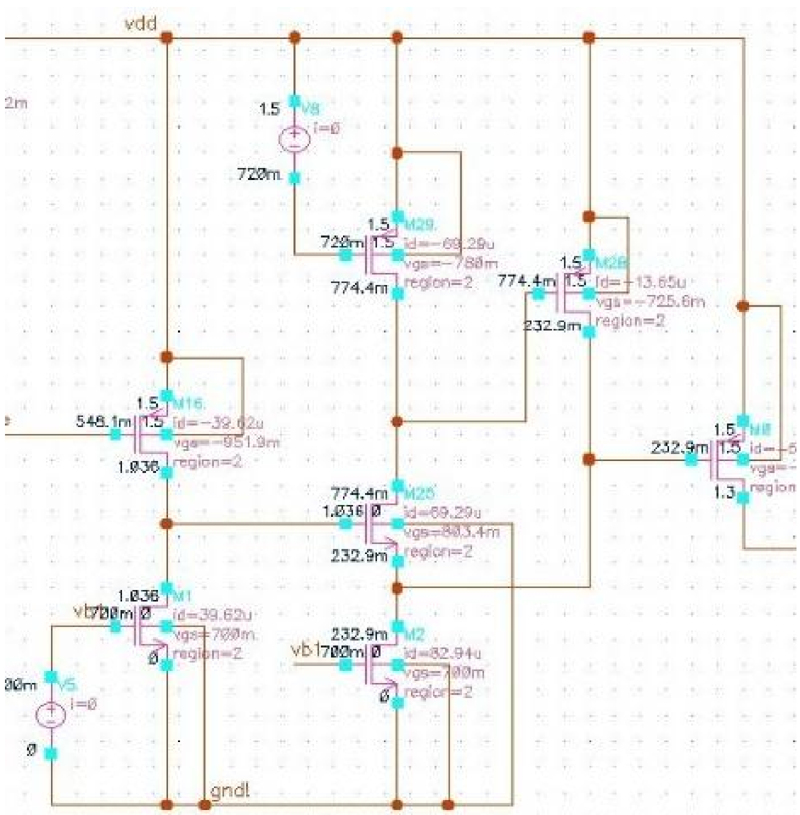


Fig. 5 Gate driver circuitry



Gate driver network

The gate driver comprises of two stages, the first stage is a PMOS common source stage which was designed to increase the output swing of the error signal. The second stage is formed using an NMOS super source follower with a PMOS transistor as an output resistance attenuator. This allows for lower output resistance to drive the large gate capacitance of the power transistor. This creates a pole at 30MHz.

Table 7 Gate driver specification

Quiescent current of common source stage	10 µA
Quiescent current of the super source follower	40 µA
Quiescent current of NMOS branch	20 µA
Quiescent current of PMOS branch	20 µA
On resistance	900 ohm

Load Circuit

The filter capacitor is 2 µF with an ESR of 0.2 ohm. This creates a zero at 400 kHz. The circuit is simulated for steady state using a load resistance of varying from 25-100 ohms to allow a load current from 15-50 mA. For transient response, a pulse current source is used as provided in the required system specifications.

Device Sizes

Table 8 Summary of device sizes

Transistor	W (µm)	L (µm)	W/L
I36M0	0.7	0.35	2
I36M1	4	2	2
I36M2	4	2	2
I36M3	0.4	0.35	1.15
I36M4	0.4	0.35	1.15
I36M18	0.7	0.35	2
I36M19	2	2	1
I36M20	4	2	2
I36M24	4	2	2
M0	4500	0.35	12,857
M1	16	0.35	45.7
M2	48	0.35	137
M16	10	0.35	28.5
M25	20	0.35	57
M28	30	0.35	85.7
M29	80	0.35	228.5

Fig. 6 Loop gain at minimum load current of 15mA

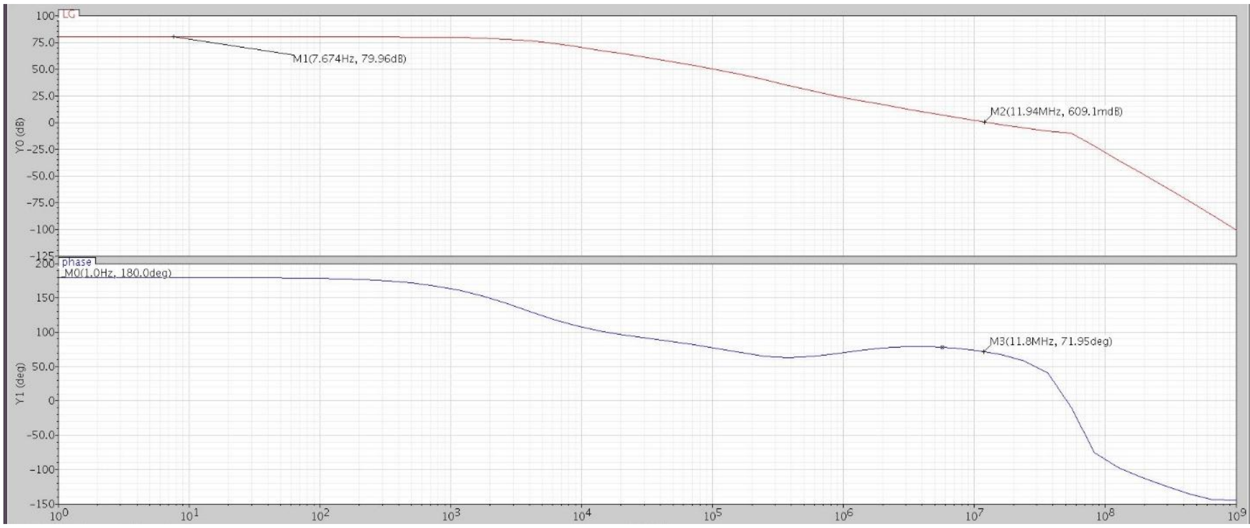
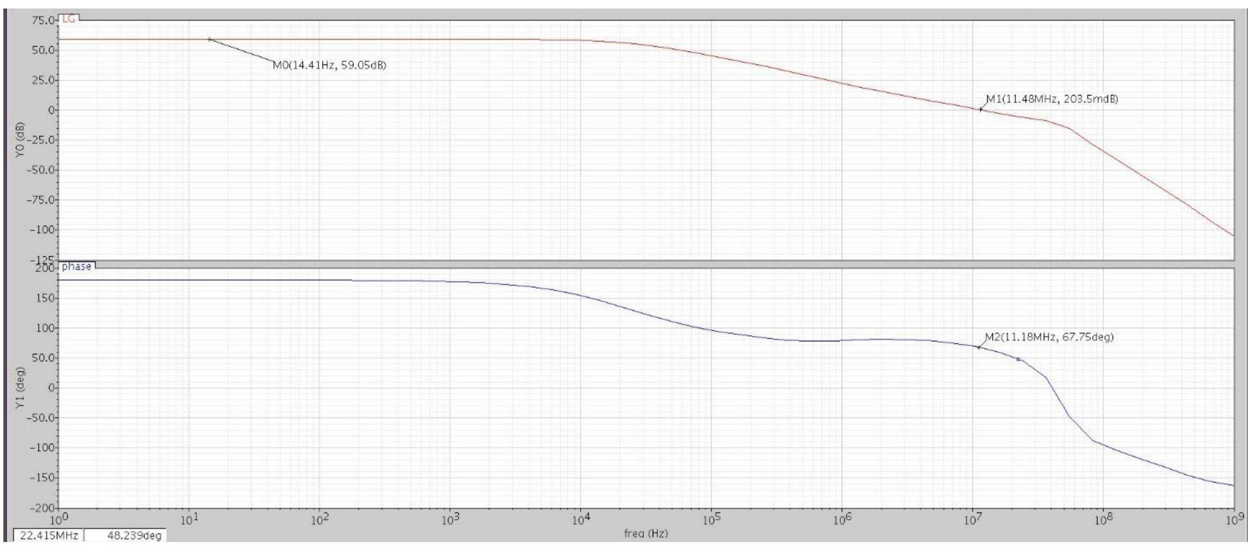


Fig. 7 Loop gain at maximum current of 50mA

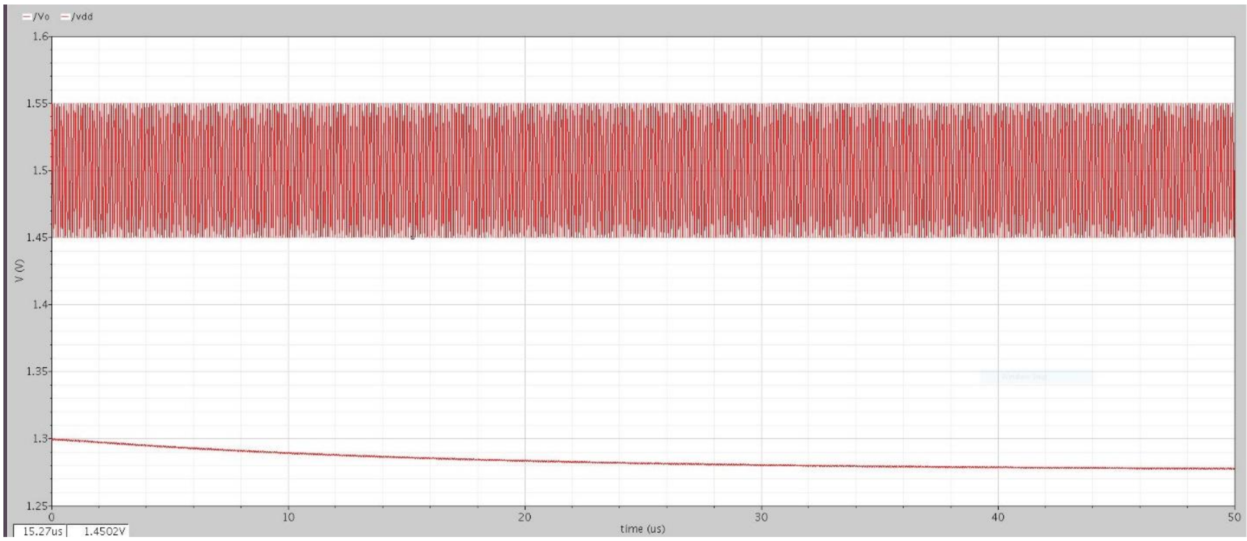


Simulation results

Loop gain

The loop gain of the system depends on the output load current. It can also be observed that poles move closer to each other when the load current increases. Fig. 6 and 7 depict the former statement. The phase margin decreases to 67 degree for a load of 50 mA, while it is 71 degree for a 15 mA load. Here, it should be noted that the minimum allowable current through the pass transistor cannot be zero because to fully turn off the transistor, the upswing of the gate driver should be close to the difference of input voltage and the PMOS threshold voltage. The gate driver cannot swing higher as it is limited by the PMOS resistance attenuator and so the minimum load current value.

Fig. 8 Line regulation simulation for the LDO was performed at 30mA load. A sine wave of 10MHz and 100mV peak to peak is applied to the input.



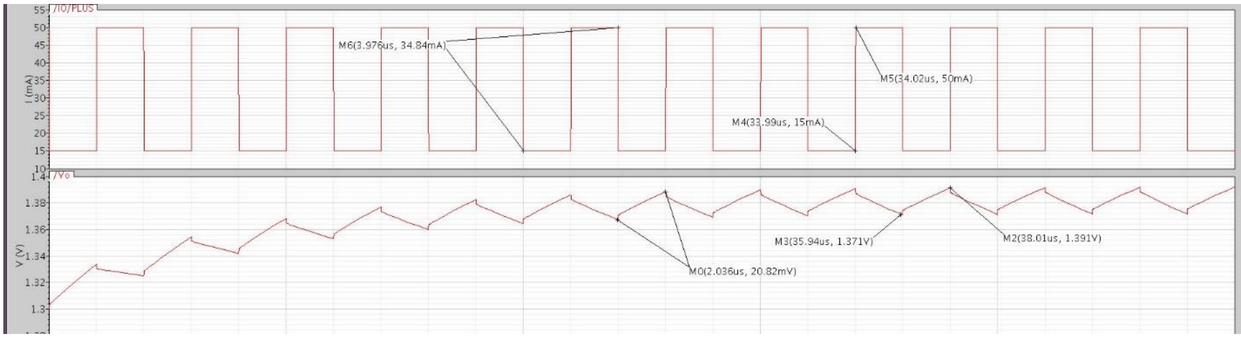
Line regulation

As per the specification, the required PSR specification is 35 dB, i.e. 17 mV/V. For testing the system for line regulation, a sine wave of 10MHz and 100mVpp was applied with the input voltage of 1.5V. The output voltage show a ripple of less than 1mV, thus meeting the specification for line regulation. A DC output error is seen as the loop gain decreases at 10MHz, and the system cannot correct for the error in the given time period. The result is shown in Fig. 8.

Load regulation

As per the specification, the required recovery specification is 2us for a 10ns load step of 30 mA. However, our system cannot go to a full zero load current. So to maintain the load step specification, we perform load step of 15mA to 50mA, which is a 10 ns, 35 mA load step. For testing the system for line regulation, a pulsed current source was applied to the output for nominal input voltage. It can be seen that from Fig. 9. That there is an output error of +80mV which occurs due to low loop gain at 10MHz. However, the output voltage ripple is maintained n steady state at 20mV/35mA which translates to a load regulation of 0.57mV/mA.

Fig. 9 Load regulation simulation test results



Summary of results

Table 9 Summary of achieved system level specifications

Design Parameter	Expected	Achieved
Minimum Supply Voltage	1.5 V	1.5 V
Maximum output current	30 mA	50 mA
Dropout voltage	0.2 V	0.2 V
Quiescent current	60 µA	2.5 + 12 + 10 + 40 = 64.5 µA
Output capacitor	2 µF	2 µF
ESR	1.5 ohm	0.2 ohm
Loop gain magnitude	50 dB	75 dB
Overshoot/undershoot	< 0.15V	0.08V
PSR	35dB at 10MHz	35dB at 10MHz
Transient recovery time	2 us	20 us

Conclusion

A high PSR LDO for RF SoC application is designed with a maximum load current of 50mA and 35dB PSR at 10MHz. The application requires high bandwidth and gain, thus designing in 0.35-micron process is challenging in the sense that necessary loop gain magnitude cannot be achieved at high frequencies without dissipating large current due to large parasitic capacitances. The literature survey states all works in 0.13-micron process and a similar attempt was made in 0.5-micron and a fair comparison was done to meet all specifications.

References

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[5] Razavi, Behzad. 2001. Design of analog CMOS integrated circuits. Boston, MA: McGraw-Hill.