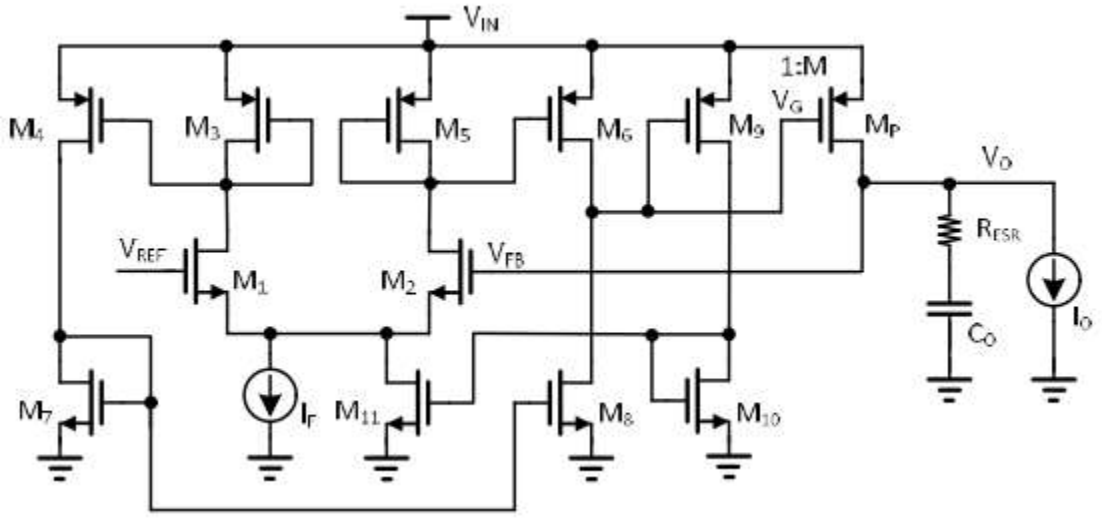
EECT6379 - Energy Harvesting, Storage and Powering for Microsystems

First Project Assignment | Devang Sankhala (dgs150030) | March 21, 2017



Process files

TSMC 0.35 um process files were used for this assignment. Important characteristic values are given.

Parameter	**NMOS**	**PMOS**
μC_{ox}	150 $\mu A/V^2$	30 $\mu A/V^2$
Threshold voltage	0.5 V	0.7 V
Lambda	0.01	0.015

Sizing

Designator	**W m**	**L m**	**Multiplier**	**Active area**
M1	1.20E-05	2.00E-06	4	9.60E-11
M2	1.20E-05	2.00E-06	4	9.60E-11
M3	2.00E-05	2.00E-06	4	1.60E-10
M4	2.00E-05	2.00E-06	4	1.60E-10
M5	2.00E-05	2.00E-06	4	1.60E-10
M6	2.00E-05	2.00E-06	18	7.20E-10
M7	1.60E-05	2.00E-06	4	1.28E-10
M8	1.60E-05	2.00E-06	18	5.76E-10
M9	9.00E-06	2.00E-06	1	1.80E-11
M10	4.80E-06	2.00E-06	1	9.60E-12
M11	4.70E-06	2.00E-06	1	9.40E-12
Mf	5.00E-07	4.00E-06	1	2.00E-12
Mp	2.40E-06	5.00E-07	1444	1.73E-09
			Total	**0.0039mm²**

First, for pass transistor, based on drop out voltage and load extremes, the on resistance is decided for a given voltage swing. This swing is used as a reference to design the OTA output swing. As for the huge gate capacitance, that is used to estimate the pole location at the output of the OTA. Thus, a major current portion is carried by M6 and M8.

$$r_{on} = \frac{1}{k \frac{W}{L} v_{ov}}$$

All sizing done for maximum current allocation assuming all transistors in saturation except the pass transistor which is in triode region at max load. For minimum load, the entire system is assumed to be in subthreshold region. Offset nullification is done at half of max load condition. Thus, at 5.05mA, the output voltage is 1.2 V and quiescent current is 50 microamperes. At other load conditions, the current may vary non-linearly.

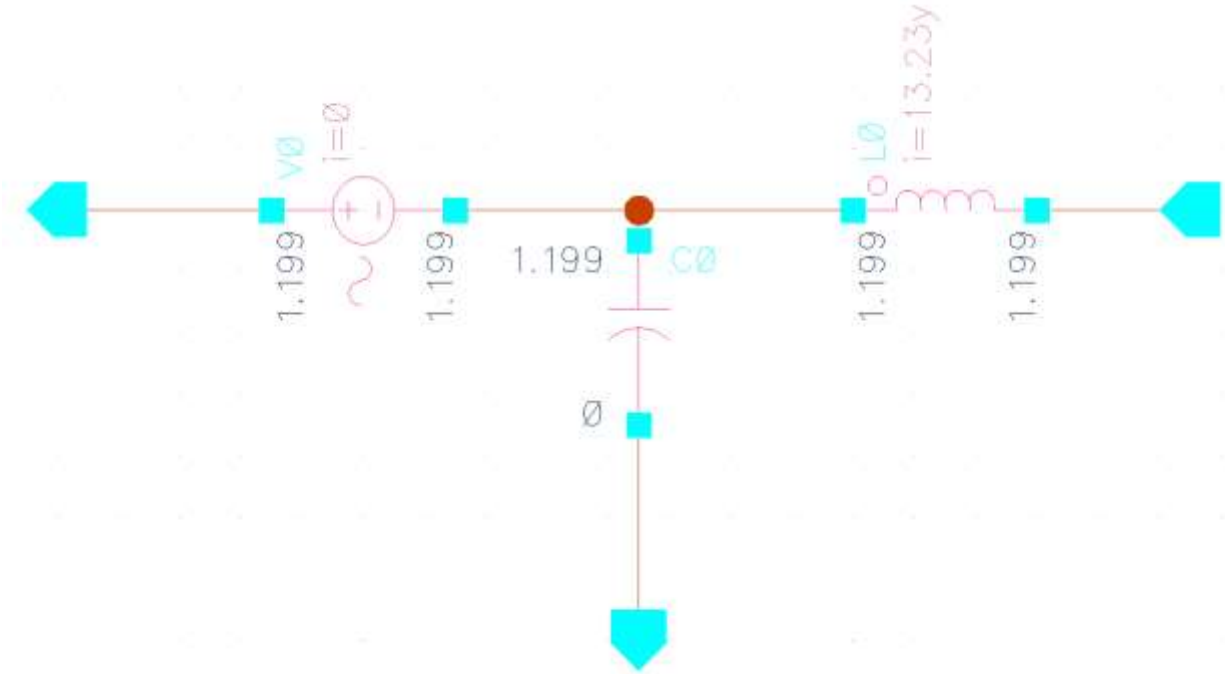
All sizing has been done using g_m/I_D method. By definition, for a given transistor

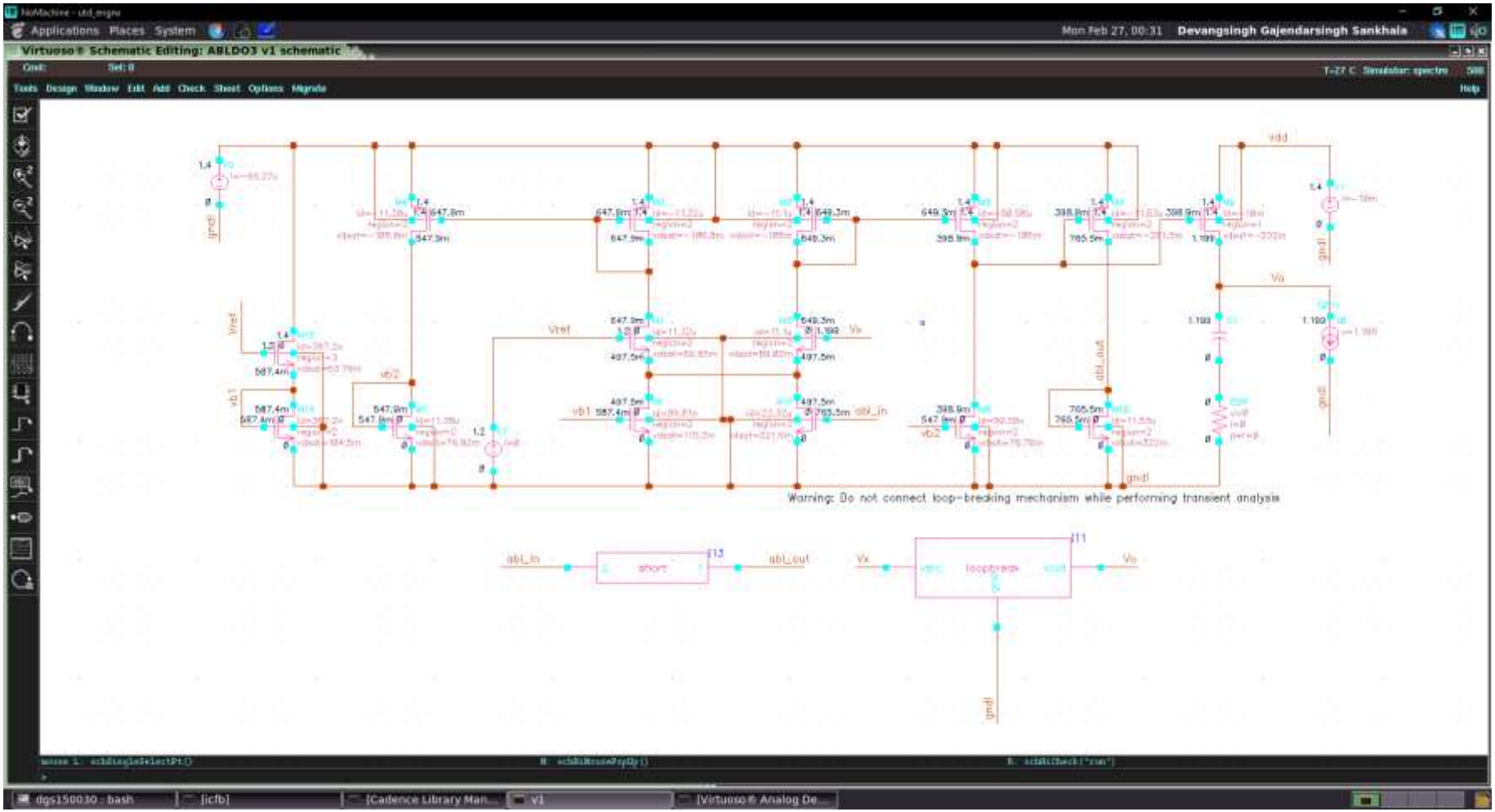
$$g_m = \frac{2I_D}{v_{ov}}$$

Thus, to minimize current and get maximum gain, the lowest overdrive is chosen. Here, 100 mV is chosen considering low headroom with respect to input voltage and threshold voltage values. Thus, for a given transfer function, current and overdrive voltages can be used to estimate system response.

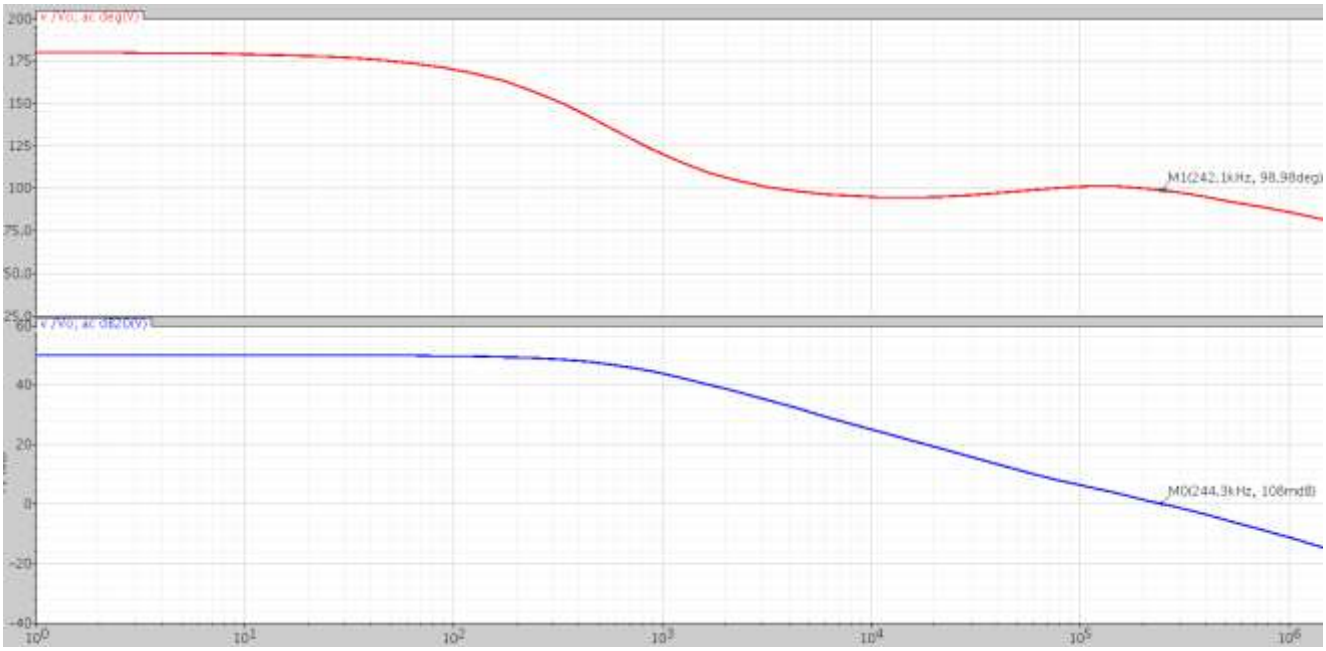
Loop transfer function and frequency response

To test system response, two blocks were designed. The “short” block is a resistor of 0.1ohm to ensure the loop is connected. The “loopbreak” block breaks the AC loop and perturbs the system from “vsrc”.

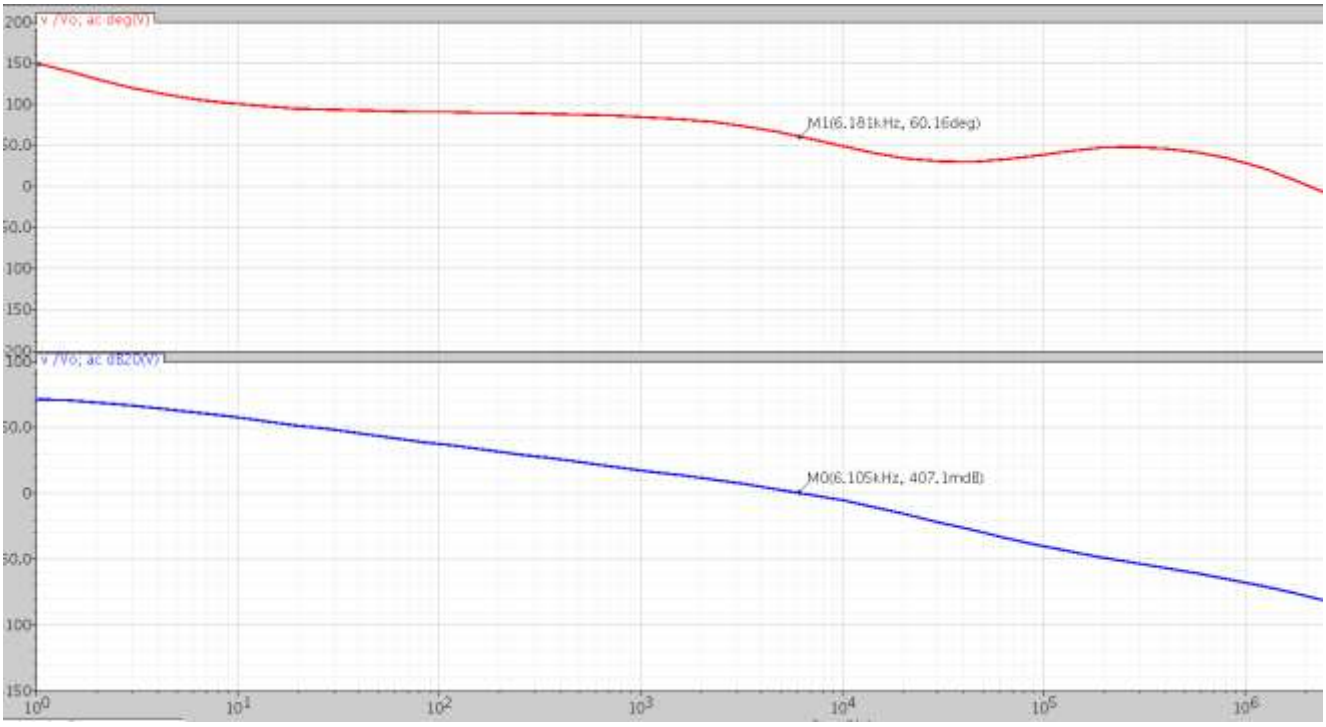



Virtuoso® Schematic Editing: ABLDO3 v1 schematic
Vdd
Vref
Vx
Vo
gndl
abl_out
abl_in
Warning: Do not connect loop-breaking mechanism while performing transient analysis
short
loopbreak

Max load



Min load



Compensation

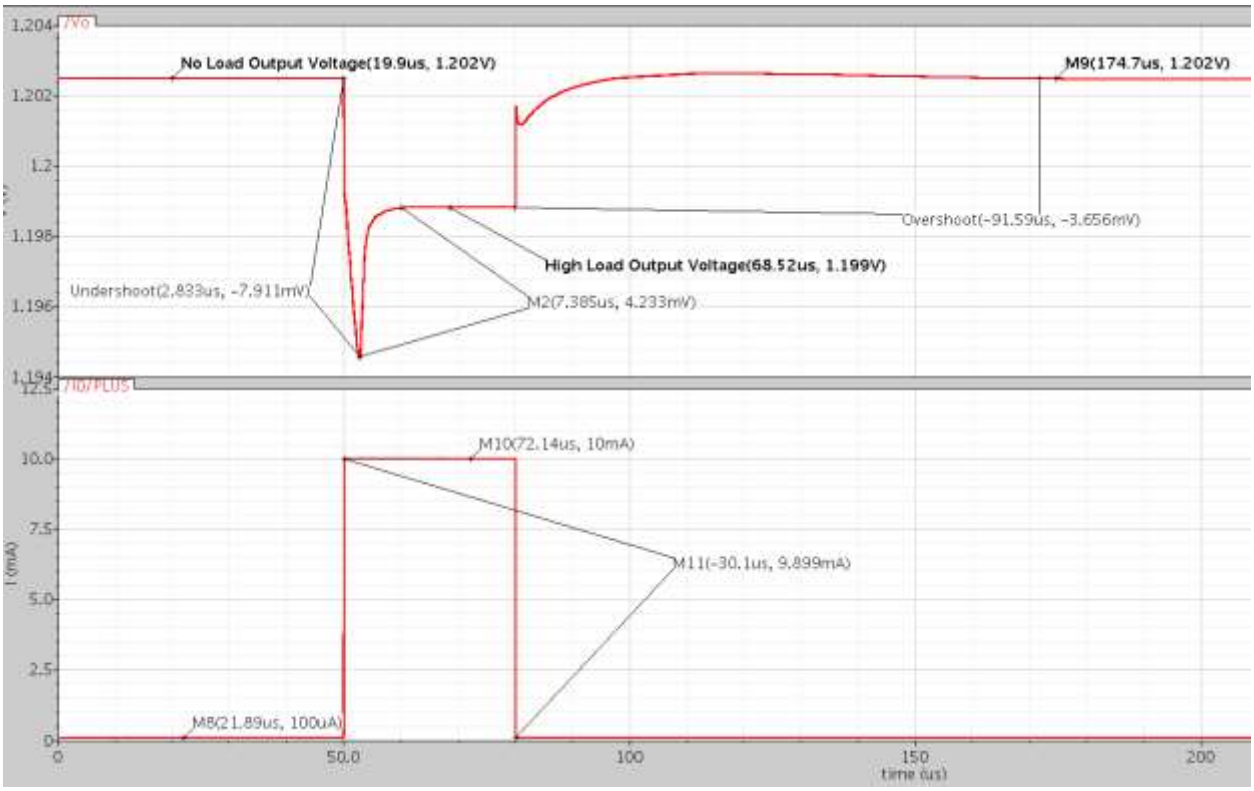
There are two methods of stabilizing the two loops. The first is the use of a large output capacitor with some ESR to create a zero. Considering use of MLCC capacitors made with X7R dielectric, it has an intrinsic worst case resistance of 0.25 ohm for capacitors below 10uF. Considering 50 milliohm PCB trace impedance, the total ESR can be considered as 0.3 ohm.

The second method is to slow down the adaptive bias loop by bringing the dominant pole of the adaptive loop to a lower frequency. This can be done by putting a capacitor across M10, however in this case, there is no need for this compensation as the bandwidth is less. The bandwidth can be lessened by increasing the gate length of M10.

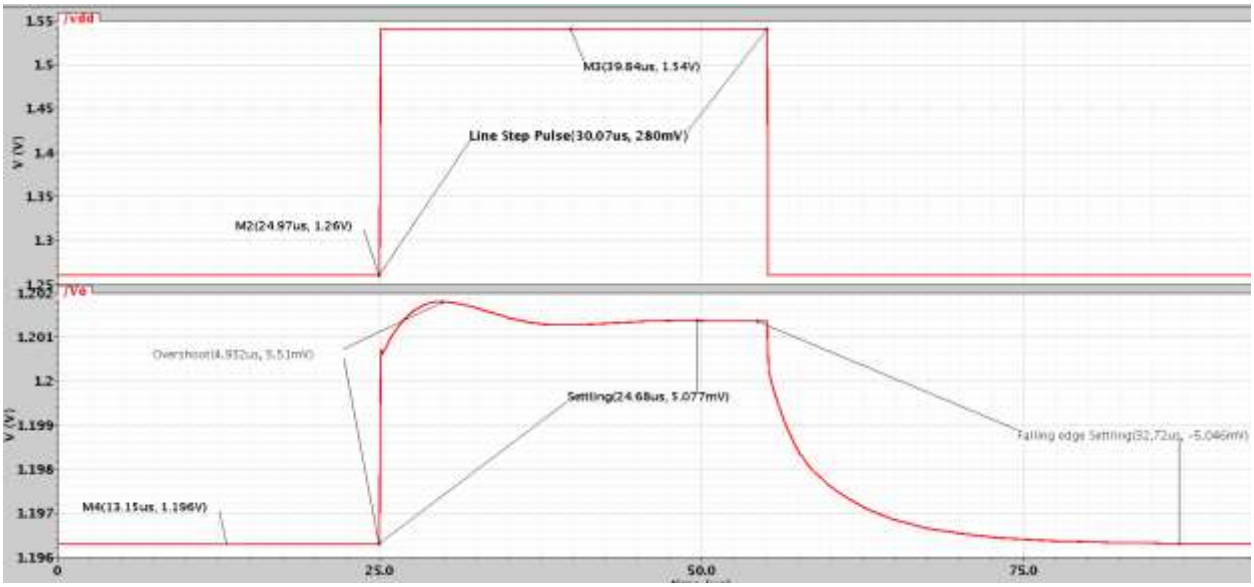
The below results are for a **4.7uF output capacitor and 0.3 ohm ESR**.

Load	Quiescent current	Phase margin degrees	Gain	Settling error	Unity gain frequency	Output voltage
0.1mA	2.97 µA	60	71.63 dB	0.03%	5.8kHz	1.202V
10mA	96.27 µA	98	50 dB	0.3%	242kHz	1.199V

Load Transient



Line Transient



From above transient results,

$$Line\ regulation = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{5}{280} = 17.85\ mV/V$$

$$Load\ regulation = \frac{\Delta V_{out}}{\Delta I_{out}} = \frac{3.6}{9.9} = 36.36\ mV/mA$$