

Very Low-Voltage Digital-Audio $\Delta\Sigma$ Modulator with 88-dB Dynamic Range Using Local Switch Bootstrapping

Mohamed Dessouky, *Student Member, IEEE*, and Andreas Kaiser, *Member, IEEE*

Abstract—A 1-V 1-mW 14-bit $\Delta\Sigma$ modulator in a standard CMOS 0.35- μm technology is presented. Special attention has been given to device reliability and power consumption in a switched-capacitor implementation. A locally bootstrapped symmetrical switch that avoids gate dielectric overstress is used in order to allow rail-to-rail signal switching. The switch constant overdrive also enhances considerably circuit linearity. Modulator coefficients of a single-loop third-order topology have been optimized for low power. Further reduction in the power consumption is obtained through a modified two-stage opamp. Measurement results show that for an oversampling ratio of 100, the modulator achieves a dynamic range of 88 dB, a peak signal-to-noise ratio of 87 dB and a peak signal-to-noise-plus-distortion ratio of 85 dB in a signal bandwidth of 25 kHz.

Index Terms—Analog circuits, bootstrapped switch, delta-sigma modulators, switched-capacitor circuits, very low voltage.

I. INTRODUCTION

FUTURE systems-on-chip will require integration of logic, analog, and memory on the same chip at low power-supply voltages. The need for the development of low-voltage and low-power analog circuit techniques is, thus, twofold. First, the demand on low-voltage low-power mixed-signal circuits is significantly increasing in order to cope with modern advances in portable and battery-operated systems. In these systems, the operating voltage and the total power consumption have a direct impact on the battery weight and lifetime. On the other side, advances in CMOS technology are driven by the digital system need to enhance the circuit speed performance and increase the integration density by continuously reducing the channel length. Lower channel lengths lead to lower supply voltages. The supply voltage is expected to drop down to around 0.6 V for a channel length of 0.05 μm by 2011 [1]. The threshold voltage, however, must remain relatively constant to keep the off transistor leakage within tolerable limits.

Analog-to-digital converters (ADCs) are one of the performance limiting blocks in any mixed-signal circuit. Robust switched-capacitor (SC) circuits are still good candidates even under very low voltage. However, in contrast to digital circuits, the power consumption of analog circuits increases as the supply voltage decreases [2]. In addition, the widely

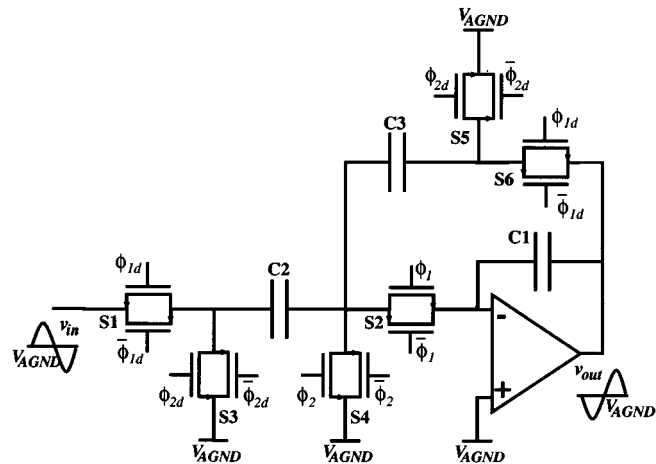


Fig. 1. SC first-order low-pass filter.

used clock voltage multiplication technique [3] cannot be employed anymore for critical switches in the circuit due to the gate dielectric reliability limitation [4]. New circuit techniques are thus needed to allow SC circuit operation under these challenging conditions and maintain, at least, the same signal-to-noise ratio (SNR).

After a brief introduction to low-voltage SC techniques, this paper describes the design of a 1-V 14-bit digital-audio $\Delta\Sigma$ modulator in a standard CMOS technology using a dedicated low-voltage switch. Special attention has been paid to device reliability and power consumption.

II. LOW-VOLTAGE SWITCHED-CAPACITOR OPERATION

Fig. 1 shows a typical first-order low-pass SC section. The analog ground potential V_{AGND} is usually set to $V_{DD}/2$ to maximize signal excursions. The CMOS switch is fully operational for supply voltages higher than the sum of the threshold voltages of both transistors $V_{thn} + V_{thp}$. For lower supply voltages, a conductance gap begins to appear around the middle of the supply range, as will be shown later on. This means that under low-voltage operation, this configuration no longer works.

Some solutions to this problem can be found in the open literature. Special fabrication processes have been modified to have, besides standard transistors, low-threshold transistors. These processes, however, are more expensive since processing steps must be added during circuit fabrication. Since the clock voltage multiplication technique [3] is not compatible with very advanced low-voltage CMOS processes where gate-oxide

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M. Dessouky is with the Laboratoire d'Informatique de Paris 6, University of Paris VI, Paris, France (e-mail: Mohamed.Dessouky@ieee.org).

A. Kaiser is with the Institut d'Electronique et de Microelectronique du Nord (IEMN), F-59046 Lille cedex, France (e-mail: Andreas.Kaiser@isen.fr).

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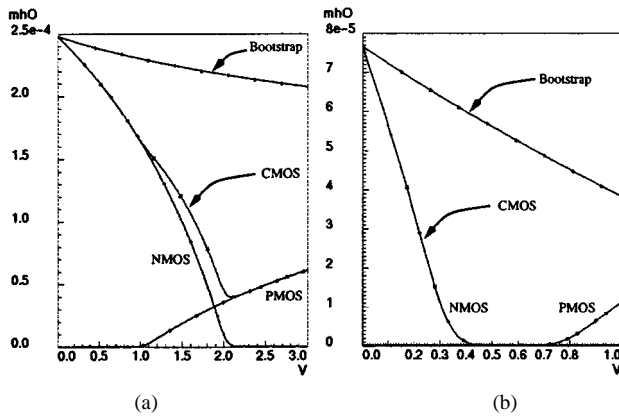


Fig. 8. Comparison of the bootstrapped and the CMOS switch conductance using minimal size transistors $W/L = 0.5\mu/0.35\mu$. (a) $V_{DD} = 3$ V. (b) $V_{DD} = 1$ V.

this limitation, an additional transistor MN2 has been added on the drain side, shown dashed in Fig. 7, such that the switch MNSW becomes completely symmetrical. The gate voltage is thus clamped at a voltage V_{DD} higher than the terminal of the lowest terminal voltage.

This bootstrapping circuit thus allows switch operation (transistor MNSW) from rail-to-rail while limiting all gate-source/drain voltages to V_{DD} avoiding any oxide overstress. Fig. 8 shows the conductance of a minimal size bootstrapped switch versus the source potential for two different supply voltages. Also shown is the conductance of a CMOS switch. For the 3-V case, shown in Fig. 8(a), the bootstrapped switch conductance has less variations than that of the CMOS case. This means that using this switch would reduce significantly harmonic distortion effects, such as charge injection related to switch operation. For the 1-V case, shown in Fig. 8(b), while the CMOS switch fails due to the conductance gap for signal voltages in the mid-supply range, the bootstrapped switch allows rail-to-rail operation. In spite of the fact that the gate-source potential of the bootstrapped switch is held constant, the conductance drops with the source voltage due to the source-bulk potential which increases the threshold voltage. In [15], a solution to this bulk effect is proposed through the use of a separate well p-transistor as the main switch and controlling its bulk potential.

It is to be mentioned that other bootstrapped switch implementations have been proposed. In [16], a MOS-only implementation was presented, however, no attention has been paid to reliability problems. In [4], reliability problems have been addressed, however, the bootstrap implementation [14] used in this work has the merit of being much simpler and addressing the transient reliability problem.

B. Opamp

In very low-voltage SC circuits, stacked transistors cannot be used to achieve the required DC gain. Thus, usually a two-stage amplifier is needed. Fig. 9 shows the used opamp [8]. It is based on a fully differential folded-cascode p-type two-stage Miller-compensated configuration. The second stage is a common-source amplifier with active load which also allows a large output swing.

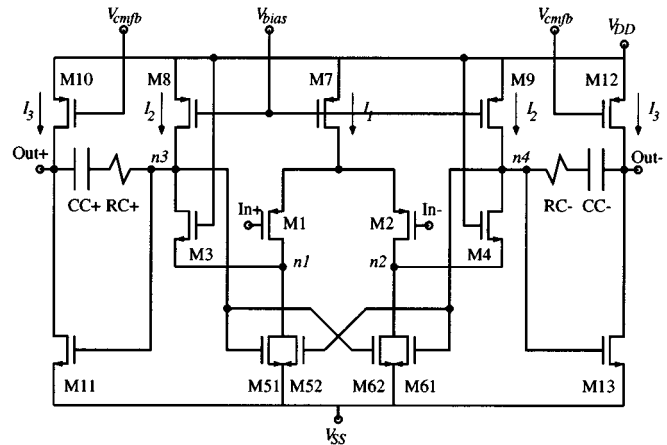


Fig. 9. Two-stage amplifier with inherent first-stage CMFB.

Due to the differential structure, the CM output voltage of *both* stages needs to be regulated using common-mode feedback (CMFB). Biasing of class-A amplifiers is typically accomplished with a CMFB circuit that senses the output CM voltage in order to control the tail current source in the first stage. However, owing to stability considerations, the gain and bandwidth of the CMFB loop are limited to, at most, those of the differential mode signal path. Moreover, since the gain from the first stage to the output is positive, an additional inverting amplifier is needed to achieve a stable CMFB, thus increasing the overall power consumption. This CMFB amplifier also limits the output swing of the original differential amplifier.

In order to avoid this extra CM amplifier, the CMFB circuit for the first stage has been replaced by the cross-coupled connection of transistors M51, M52, M61, and M62, similar to [17]. The differential output conductance seen at the output of the first stage (nodes $n3$ and $n4$) is given by

$$g_{ds_{out1}} = g_{ds8} + (gm_{51} - gm_{52}) \frac{g_{ds3}(g_{ds1} + 2g_{ds51})}{g_{ds3} + g_{ds1} + 2g_{ds51} + gm_3 + gmb_3}. \quad (1)$$

With $gm_{51} = gm_{52}$, the transconductance gm_{51} seen at the gate of transistors M51 and M61 is thus canceled by the opposite action of the parallel transistors M52 and M62, respectively. This negative feedback connection causes the differential signal at the output of the first stage to see a high load impedance limited by $1/g_{ds8}$. On the other hand, for the common mode signal, the output conductance is still given by (1) with the negative sign turned positive. The conductance is thus limited by $gm_{51} + gm_{52}$. This is a low impedance and consequently the first stage does not require an additional CMFB circuit.

For the second stage, a simple passive SC CMFB circuit, shown in Fig. 6, is used. Since the output CM of the amplifier is set to $V_{DD}/2$, bootstrapped switches must be used in the CMFB circuit for those switches connected to the amplifier output. Those bootstrapped switches, however, can be shared with the sampling network connecting the integrator output to the subsequent stage, as shown in Fig. 6.

The amplifier has a minimum supply voltage, determined by the cross-coupled connection, of $V_{GS51} + V_{DSsat8}$ which is around 1 V. This low supply voltage allows biasing the cascode

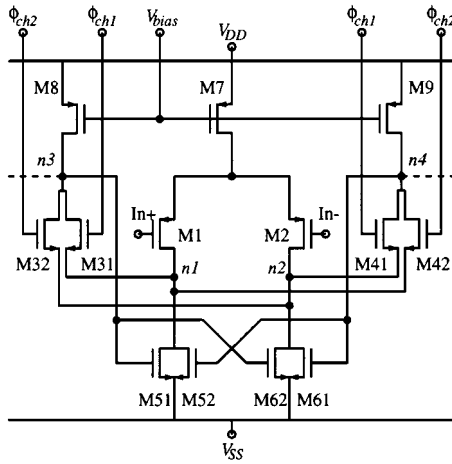


Fig. 10. Output chopping using the cascode transistors.

transistors directly through V_{DD} which eliminates the need of an additional biasing voltage. On the other hand, this connection limits the maximum allowable supply voltage necessary to keep the cascode transistors in saturation. It may also degrade the power supply rejection ratio (PSRR) since the supply noise is directly injected in the signal path. However, this effect is greatly reduced through the fully differential structure where this noise results in a CM signal which is rejected by the fully differential operation. The amount of the cancellation is limited by the mismatch of the two differential signal paths.

While flicker noise can be reduced using larger gate areas for the transistors contributing to the noise (namely M1, M2, M5, M6, M8, and M9), this causes higher parasitic capacitance on the internal nodes increasing the amplifier power consumption. In order to overcome this, chopper stabilization has been used [18]. Input chopping can be easily done using four input switches as shown in Fig. 6. However, since the opamp uses a two-stage structure with a compensation capacitor, the same switching arrangement cannot be used at the output. In fact, the compensation capacitance acts like a memory element that prohibits the opamp output to be chopped instantaneously. Instead, the output of the first stage is chopped as shown in Fig. 10 using only two additional cascode transistors M32 and M42 in parallel with the existing ones but with their sources connected to nodes $n2$ and $n1$, respectively [8]. The gates of both cascodes are then driven by the two *overlapping* chopper clocks ϕ_{ch1} and ϕ_{ch2} at half the sampling frequency. The two chopper clocks must overlap to avoid the simultaneous cutoff of both cascodes in parallel which would increase the settling time of the opamp. This arrangement reduces the $1/f$ noise for all transistors but M8 and M9 where a larger transistor length must still be used. Chopper stabilization is used only for the first integrator stage, since the noise of subsequent stages undergoes noise shaping by the loop filter.

C. Comparator

Since there are no critical design requirements on the comparators used in $\Delta\Sigma$ modulators, a simple low-voltage comparator similar to that presented in [10] is used. The comparator

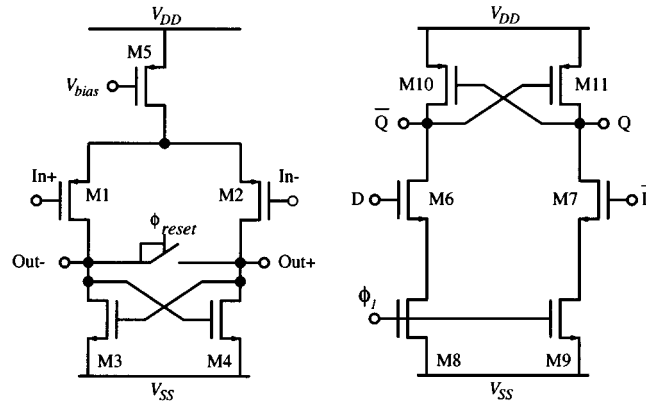


Fig. 11. (a) Low-voltage comparator. (b) Low-voltage latch.

is shown in Fig. 11(a). It is composed of the input p-type differential stage M1/M2 transistors which drives the positive feedback connection of transistors M3 and M4 used for the regeneration action.

In [10], resetting is done by shorting both outputs to V_{SS} . In this design, however, resetting the comparator to the metastable state is achieved using a bootstrapped switch, as shown in Fig. 11(a). This enhances the comparison speed by eliminating the time needed by the outputs to rise from V_{SS} to the metastable state.

The input CM of the comparator is at V_{SS} , a simple SC circuit is used to shift the level of the last integrator output which is around $V_{DD}/2$ to V_{SS} .

The same latch, shown in Fig. 11(b) [10] is also used. The metastable point at the comparator output should be chosen below the threshold level of the latch V_{th6} , such that if the outputs of the comparator have not diverged enough in the available time, the latch should not trigger [10].

V. DESIGN SYNTHESIS

Starting from high-level specification requirements determined using MATLAB [12] simulations, circuit sizing has been done following the layout-oriented design methodology presented in [19]. Sizing plans have been developed for the amplifier, the integrator, and the bootstrapped switch and incorporated in the knowledge-based sizing tool COMDIAC [20]. In the same time, the corresponding layout templates have been prepared using the layout language CAIRO [21]. These templates have been then used concurrently *during* sizing to calculate the associated circuit parasitics including diffusion and routing capacitances and to compensate for them by readjusting transistor sizes. This is done through a special parasitics estimation mode allowed by the layout tool [19] without any layout generation. The final layout has also been generated using the same templates.

The automating sizing procedures also allow to size *separately* each switch based on its charge and the required settling error. This allows to optimize switch sizes, which happens to be large under low-voltage operation as a result of the small switch overdrive, leading to the minimization of the clock feedthrough due to the associated large switch parasitic capacitances.

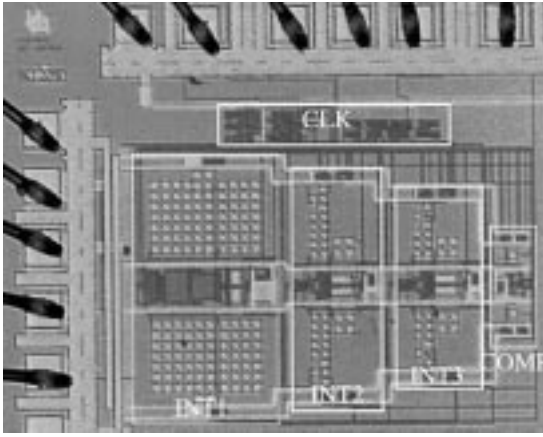


Fig. 12. Chip die photo.

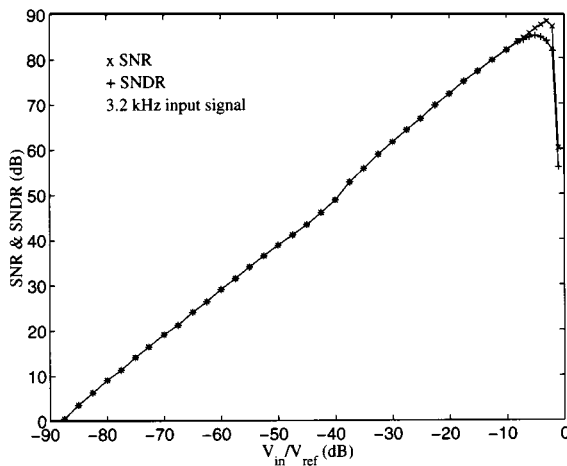


Fig. 13. Measured SNR and SNDR.

VI. EXPERIMENTAL RESULTS

The modulator has been implemented in a 0.35- μm standard CMOS process with double-poly and triple-metal levels. The threshold voltages for the n- and p-transistors are 580 and 600 mV, respectively. Fig. 12 shows the chip photograph. Capacitors have been implemented using the two poly layers. The core area excluding bonding pads is $0.9 \times 0.7 \text{ mm}^2$. A single clock at 5 MHz is used to drive the modulator. The nonoverlapping delayed clock phases as well as the overlapping clock phases at half the clock frequency needed for the chopper stabilization circuit are all generated on chip.

On the test board, the input signal is converted from single-ended to differential using a transformer and shifted to a CM level equal to $V_{DD}/2$. The digital output of the modulator is captured with a data analyzer through optocouplers to isolate ground noise of the digital measurement equipment. The data are then transferred to a PC, which performs fast Fourier transform (FFT), windowing, and graphical representation.

The modulator operates at a V_{DD} of 1 V and dissipates 950 μW including the digital circuitry. 60% of the total power is consumed by the first integrator. The reference voltage is set to 1 V and is brought on chip on a separate pad. With an oversampling ratio of 100, the signal bandwidth is 25 kHz. Fig. 13 shows the measured SNR and signal-to-noise-plus-distortion

TABLE II
CONVERTER PERFORMANCE SUMMARY.

Supply Voltage	1 V
Reference Voltage	1 V
DR	88 dB
Peak SNR / SNDR	87 dB / 85 dB
Oversampling Ratio	100
Sampling Rate	5 MHz
Signal Bandwidth	25 kHz
Power Consumption	950 μW
Figure of Merit $\times 10^6$	275
Die Area	0.9 mm \times 0.7 mm
Technology	0.35 μm CMOS TMDP

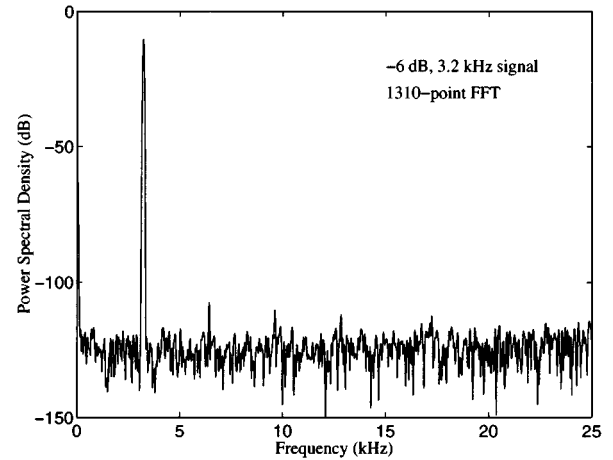


Fig. 14. Measured baseband output spectrum.

ratio (SNDR) versus the relative input amplitude (V_{in}/V_{ref}). An input sinusoidal signal at 3.2 kHz was used to produce these plots. It is apparent that the modulator achieves a dynamic range (DR) of 88 dB, and a peak SNR and peak SNDR of 87 and 85 dB, respectively. The measured performance is summarized in Table II. Fig. 14 shows the output baseband spectrum for a 3.2-kHz input signal at -6 dB relative input level. The frequency independence of the noise floor indicates that the modulator's performance is thermal-noise limited rather than quantization-noise limited.

Various ADC implementations are often compared using the following figure of merit [3]:

$$\text{FM} = \frac{4kT \times \text{DR} \times f_N}{P} \quad (2)$$

where f_N is the Nyquist sampling frequency and P is the total power dissipation. Compared to another very low-voltage $\Delta\Sigma$ implementation presented in [10], the current design achieves practically the same figure of merit, whereas the SNDR is about 25 dB higher. Further improvement in the dynamic range may be obtained by reducing the opamp thermal noise.

VII. CONCLUSION

A 1-V $\Delta\Sigma$ modulator has been implemented using the local switch bootstrapping technique. Rail-to-rail operation of bootstrapped switches allows very low-voltage robust SC implementations in standard CMOS technologies while avoiding tran-

sistor gate oxide overstress. Contrary to clock boosting circuits, the bootstrapping circuit presented in this work is thus fully compatible with future low-voltage technologies. Furthermore, switch charge injection and linearity is improved due to the constant gate-source overdrive. An additional transistor renders the switch completely symmetrical and eliminates transient reliability problems.

Modifications introduced to the two-stage folded cascode opamp allow very low-voltage operation and permit the use of a passive CMFB SC circuit.

Obtained results show the feasibility of very low-voltage high performance circuits using common SC techniques.

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Mohamed Dessouky (S'00) was born in Cairo, Egypt, in 1969. He received the B.S. and M.S. degrees in electrical engineering from the University of Ain Shams, Cairo, in 1992 and 1995, respectively, and the Ph.D. degree in electrical engineering from the University of Paris VI, Paris, France, in 2001.

In 1992 he joined the Electronics and Electrical Communication Engineering Department, University of Ain Shams, where he has been a Research and Teaching Assistant, and will shortly become an Assistant Professor. His research interests include low-

voltage design of switched-capacitor circuits, analog-to-digital conversion, and CAD for analog and mixed-signal integrated circuit design.



Andreas Kaiser (M'87) was born in Freiburg, Germany, in 1958. He received the Engineering Diploma from the Institut Sup  rieur d'Electronique du Nord (ISEN), Lille, France, in 1984, and the Ph.D. degree from the University of Lille in 1990.

From 1984 to 1990 he was a Teaching and Research Assistant at ISEN. In 1990 he joined the Centre National de la Recherche Scientifique (CNRS), where he is responsible for the analog IC design group at the Institut d'Electronique et de Microelectronique du Nord (IEMN), Lille. He is also

an Associate Professor with the Electronics Department of ISEN. His research interests are analog and mixed signal IC Design, CAD and MEMS. He served as Program Chairman of the European Solid-State Circuits Conference in 1995.