Analysis and Design of a Low-Voltage, Low-Power, High-Precision, Class-AB Current-Mode Subthreshold CMOS Sample and Hold Circuit

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Abstract—This paper proposes the design of a current-mode sample and hold circuit using subthreshold MOSFETS. The proposed circuit combines negative feedback and the compressive $I - V$ characteristic of a class-AB weak inversion transconductor to achieve low switching error, high signal-to-noise ratio and high dynamic range from a low supply voltage and very low current consumption. The paper also provides a feedback analysis of current mode sample and hold circuits. Several design issues including circuit stability, mismatch, linearity, noise, and power consumption are discussed and a comparison of class-A and class-AB versions of subthreshold sample and hold circuits is made. The design verification of the proposed class-AB current mode sample and hold circuit is done by circuit simulations using 0.13 μm CMOS model parameters. The results show that, from a 0.6 V supply and with a power consumption of 27.5 nW, the proposed circuit provides 73 dB signal-to-noise ratio, 77 dB dynamic range, and a figure of merit of 1.9 nW/MHz.

Index Terms—Analog sampled data, current mode, low voltage, sample and hold, subthreshold CMOS, switched current, ultra-low.

I. INTRODUCTION

PROCESSING electrical signals in the voltage domain using CMOS circuits is encountering the problem of signal swing reduction. This results from CMOS process scaling that reduces the supply voltage and thereby forces the maximum signal swing to go down [1]. To recover the signal-to-noise ratio (SNR) and the dynamic range (DR), current mode signal processing has become attractive since the nonlinear behavior of the devices, i.e. the square and exponential laws for strong and weak inversion behaviors, respectively, provide a compressive voltage swing. A wide range of current signal swings can thus obtained from a low supply voltage [2].

In the area of biomedical electronics that focuses on the design of implantable devices, minimizing power and area consumption are major requirements. To operate circuits at very low current consumption and limited supply voltage, the CMOS devices will be forced into their weak inversion region, which creates a design difficulty in terms of noise and mismatch [3], [4]. Therefore, a suitable circuit technique that can satisfy the requirements and overcome the problem of noise and mismatch is needed.

In this paper, we aim for the feasibility to perform signal processing functions within a small silicon area and which consume very little electrical power and provide high SNR and DR. As it was introduced with the distinct feature of small area and mismatch insensitive sampled data operation, the analog current-mode technique called 'switched current (SI)' is reexamined in detail focusing on its fundamental circuit operation. In theory, the basic circuit cell of the SI technique (SI memory cell) indeed provides a current sample and hold (CSH) operation within a compact circuit that is insensitive to transistor mismatch. This is because the CSH operation is performed through a single MOSFET device and there is no need for any linear capacitor since the gate-source parasitic capacitance can be employed as a memory element. In practice, the SI memory cell suffers from the nonideality of MOS switches and the memory transistor itself. Therefore, only one transistor performing CSH operation can never give sufficient accuracy [2]. The deep investigation into the feedback mechanism of the SI memory shown in this paper reveals that to enhance its performance, thereby suppressing switching errors induced by the effect of charge injection and clock-feedthrough of the MOS switches, a two-stage closed-loop circuit topology is required. Moreover, using a class-AB subthreshold transconductor to design this closed-loop CSH circuit, the bias current can be kept low, thereby obtaining a low wide-band shot noise, while input signals can go many times higher than the bias current level. As a consequence, high SNR and DR are obtained [5].

The remaining sections of this paper are organized as follows. The feedback analysis of the SI memory cell and a discussion on performance enhancement techniques are presented in Section II. In Section III, the subthreshold circuit topology choices that are possible for the design of the CSH circuit are comparatively discussed in terms of power consumption, signal excursion, noise, and linearity. In Section IV, the class-AB CSH circuit design is described. Simulation results using TSMC 0.13 μm CMOS technology of the class-AB CSH circuit are presented in Section V. Section VI discusses some considerations on the layout generation. The conclusions will finally be drawn in Section VII.

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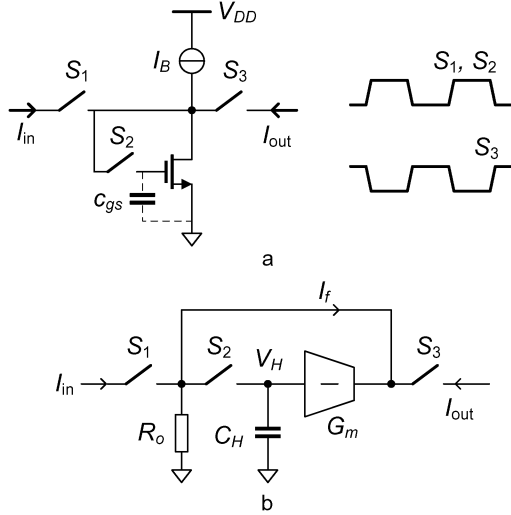
Fig. 1. Second-generation SI memory cell. (a) Circuit schematic and its controlled clock signals. (b) Small signal model.
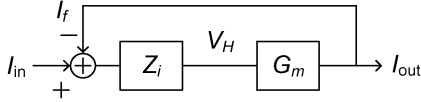

Fig. 2. Feedback block diagram of the second-generation SI memory cell.

II. FEEDBACK ANALYSIS OF A SECOND-GENERATION SI MEMORY CELL: THE NEED FOR A LARGER LOOP GAIN

A. Reexamination of a Second-Generation SI Memory Cell

Fig. 1(a) shows a second-generation SI memory cell [2]. It comprises only one transistor biased by constant current I_B and switches $S_1 - S_3$ controlled by two nonoverlapping clock signals. Considering small signal operation and including channel length modulation, the circuit in Fig. 1(a) can be modeled as shown in Fig. 1(b), where R_o and G_m represent the output resistance (output resistance of I_B in parallel with that of the transistor) and transconductance factor of the transistor.

During the sampling phase (S_1 and S_2 are closed and S_3 is opened), the gate and drain terminals of the transistor are connected creating a feedback loop as shown in the block diagram in Fig. 2. As one can see, the error current resulting from $I_{in} - I_f$, (where I_{in} and I_f represent the input and feedback currents, respectively) will flow into Z_i, thereby creating voltage V_H which is the input voltage of transconductor G_m. Finally, V_H will be converted into I_f by G_m again.

From the block diagram, the loop gain (LG) of the system can be found as

$$\text{LG} = G_m Z_i = \frac{G_m R_o}{1 + s C_H R_o}, \qquad (1)$$

where C_H equals the parasitic gate-source capacitance C_{gs} of the transistor. In this case, LG equals the intrinsic gain of a single transistor which is becoming smaller in deep submicrometer technology [6]. The input impedance of the circuit can be also found to be

$$Z_{in} = \frac{V_H}{I_{in}} = \frac{Z_i}{1 + \text{LG}} \cong \frac{1}{G_m} \frac{1}{\left(1 + \frac{s C_H}{G_m}\right)}. \qquad (2)$$
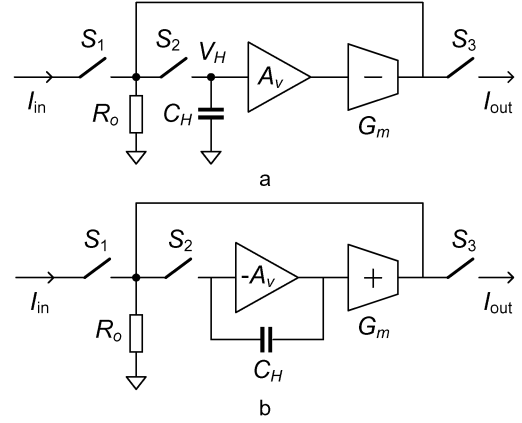

Fig. 3. CSH circuit with LG enhancement with (a) grounded holding capacitor and (b) miller holding capacitor.

It can be seen from (1) and (2) that R_o directly contributes to LG but insignificantly affects Z_{in}. On the other hand, R_o plays a role when the feedback loop is broken during the hold phase (S_1 and S_2 are opened and S_3 is closed). It defines the output resistance of the memory cell since the gate voltage of the transistor is held constant by the charge conserved within memory capacitor C_{gs}.

B. Reconsideration of the Performance Enhancement Techniques

There are two different approaches to enhance the LG thereby improving the CSH closed-loop operation: 1) increasing R_o by exploiting cascoded transistors [7] and 2) increasing G_m by cascading G_m stages [5], [8]–[11]. At first glance, these two solutions seem to provide a satisfying improvement as long as the LG is enhanced sufficiently. This is true only for the case of a continuous-time signal for which the feedback loop is always maintained. For sample and hold operation in which the feedback-loop is being switched and the swiching mechanism is performed by MOS switches, the latter solution is preferable because it gives the possibility to suppress the error from charge injection and clock-feedthrough effects. As we have seen from (2), the former approach does not help fixing the voltage swing at the sampling node. The voltage at the switching node V_H varies according to the amplitude of I_{in} inducing a signal-dependent charge injection error which leads to output signal distortion [12]. On the other hand, for a larger G_m, a smaller voltage swing is what we obtain from (2) and this helps the charge injection error to become less signal-dependent such that it can be possibly canceled out by operating the CSH circuit in a differential fashion.

The G_m enhancement technique can be realized as shown in Fig. 3. In Fig. 3(a), a voltage amplifier A_v is inserted in front of the G_m. This results in a higher effective tranconductance $G_{mt} = A_v G_m$, which can be made very large. By doing so, the error current is forced to be very small by the very large LG resulting in a very small variation of V_H. Therefore the charge injection error can be considered signal-independent. To realize voltage amplifier A_v, another G_m stage is used and unfortunately at least one additional time-constant is introduced by parasitic resistances and capacitances of all the active elements, which may lead to instability. Pole splitting can be applied to stabilize the system by changing the location of the holding
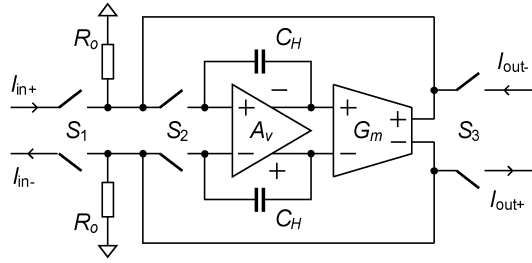
Fig. 4. Fully differential CSH circuit.

capacitor C_H (which is now used as a miller capacitor in the sampling phase) and the polarities of amplifiers A_v and G_m as shown in Fig. 3(b) [9], [10]. For proper frequency compensation (which will be discussed in the next subsection), the bandwidth of the CSH will be limited. This is a fundamental trade-off of a low distortion CSH circuit.

To get rid of the charge injection error, thereby minimizing distortion of the output signal, a fully differential structure, as shown in Fig. 4, is desirable. In the case that the pair of switches S_2 is identical and the pair of holding capacitors C_H is perfectly matched, constant charge injection error voltages will appear at the input terminals of the G_m with the same amplitude and phase. These error voltages will be seen as a common mode signal and suppressed by the common mode rejection capability of the G_m. As a result, a high linearity CSH circuit is obtained [5], [8], [12], [13]. It is worth to note that even in the situation that both G_ms are nonlinear, the complete error cancellation mentioned above can be achieved as long as the C_Hs and S_2s are identical and the former are linear, and the sampling period is sufficiently long for complete settling of V_H. Unfortunately, for the case that C_Hs are weakly nonlinear and/or switches S_2 are not matched perfectly, the charge injection error voltages can only be canceled out partially. Subsequently, output distortion will be generated from the residue input offset of G_{m2}. Effects of this imperfection will be discussed analytically in Section III-D.

C. Stability and Transient Behavior

In practice, the voltage amplifier can be formed by a transconductor with high resistive loads and the dc voltage levels at the internal nodes need to be stabilized by common-mode feedback (CMFB) circuits. Including parasitic capacitances, a more practical CSH circuit can be represented by the macro-model shown in Fig. 5. Assuming all the circuit elements are linear and omitting the CMFB circuits and breaking the loop at the input of G_{m2}, the circuit can be redrawn as in Fig. 6 to find the circuit's LG. It can be seen that the circuit is now in the form of a generic two stage amplifier and the LG can be found to be [14]

$$\frac{V'_t}{V_t} \cong \frac{4G_{m1}G_{m2}R_1R_2\left(1-\frac{sC_H}{G_{m1}}\right)}{s^2R_1R_2(C_1C_2+C_HC_1+C_HC_2)+sG_{m1}R_1R_2C_H+1}. \tag{3}$$

Its open-loop unity gain frequency, poles, and RHP zero can be approximated to be

$$\omega_u \cong G_{m2}/C_H, \tag{3.1}$$

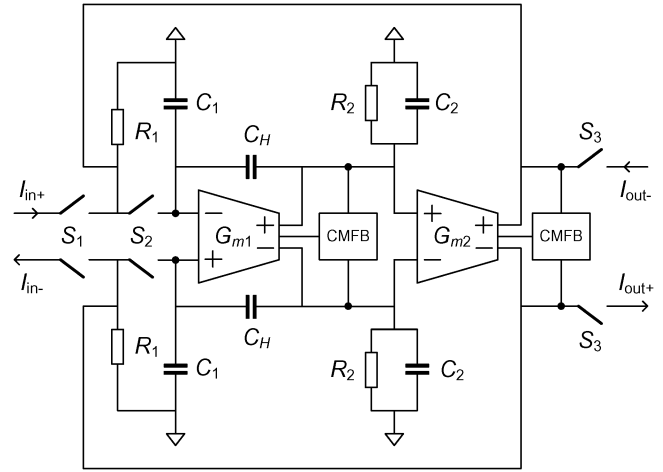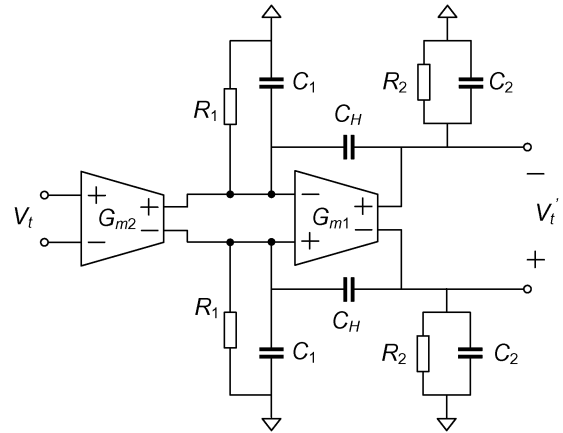

Fig. 5. Macro-model with parasitic included.

Fig. 6. Broken loop circuit for LG testing.

$$\omega_{p1} \cong -(G_{m1}R_1R_2C_H)^{-1},$$
$$\omega_{p2} \cong -G_{m1}/(C_1+C_2), \tag{3.2}$$

and

$$\omega_{z1} \cong G_{m1}/C_H, \tag{3.3}$$

respectively.

Assuming we can set $C_H \ll C_1 + C_2$, a pole-zero doublet can be avoided and setting $\omega_{p2} \geq 2.2\omega_u$, a 60° phase margin, ϕ_M can be achieved.

To estimate how fast a clock signal can be applied to this CSH circuit, the settling time, t_s, of the close-loop response of the system in Fig. 5 needs to be found. Within the range of an acceptable normalized output settling error (ε), from (3) we can find that [15]

$$t_s \cong \frac{2\pi C_H}{G_{m2}\sqrt{4\tan\phi_M(1-\tan\phi_M)}}, \tag{3.4}$$

where ε is approximated as

$$\varepsilon \cong \exp\left(-\pi\sqrt{\tan\phi_M/(4-\tan\phi_M)}\right). \tag{3.5}$$

We thus find the maximum sampling frequency of this sample and hold as $f_{s\max} \leq 0.5t_s^{-1}$. Note that this analysis is based on
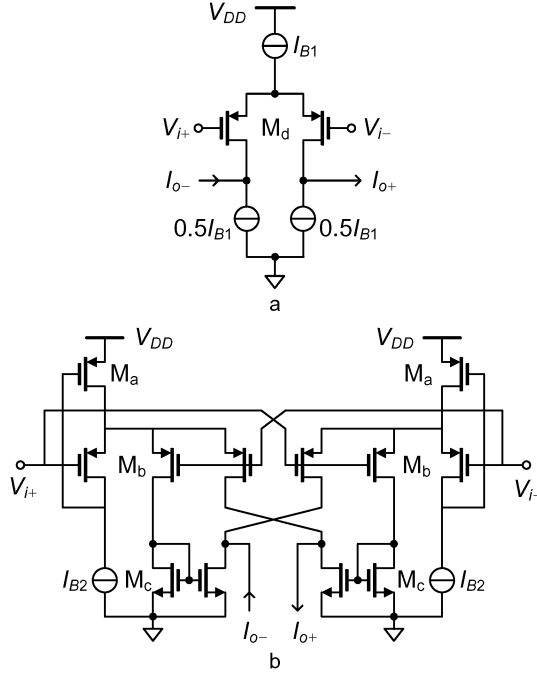
Fig. 7. Subthreshold transconductors. (a) Class-A. (b) Class-AB.

the assumption that the on-resistances of all MOS switches are small enough to create very small time constants compared to C_H/G_{m2} and it is valid for ϕ_M greater than 45°.

III. DESIGN CONSIDERATION: CLASS-A VERSUS CLASS-AB

For low voltage design, defined by $V_{DD} < 2V_{th}$ [16], there are two choices of subthreshold circuit cells to replace G_{m2} in the previous section to form a CSH circuit: class-A and class-AB transconductors, as shown in Fig. 7(a) and 7(b), respectively.

Assuming all the transistors are working in weak inversion saturation ($V_{DS} > 4U_T$), the large signal characteristics of the class-A and class-AB transconductors can be expressed by

$$I_{\text{od}} = \frac{I_{\text{o}+} - I_{\text{o}-}}{2} = \frac{I_{B1}}{2} \tanh\left(\frac{V_{i+} - V_{i-}}{2n_P U_T}\right)$$
$$= \frac{I_{B1}}{2} \tanh\left(\frac{V_{\text{id}}}{2n_P U_T}\right) \tag{4}$$

and

$$I_{\text{od}} = \frac{I_{\text{o}+} - I_{\text{o}-}}{2} = 2I_{B2} \sinh\left(\frac{V_{i+} - V_{i-}}{n_P U_T}\right)$$
$$= 2I_{B2} \sinh\left(\frac{V_{\text{id}}}{n_P U_T}\right), \tag{5}$$

respectively, where n_P is the subthreshold slope factor of the PMOSTs.

To design the CSH to be power efficient and to handle an input signal as large as possible, the large signal characteristics of (4) and (5) should be neither neglected nor even approximated. In this section, we provide comparative discussions on several design issues between class-A and class-AB CSH circuits.

A. Current Consumption

Considering current consumption, we divide the circuit operation into two cases: 1) *static*, which is defined as the situation in which there is no incoming signal and 2) *dynamic*, which is the situation in which the current consumption varies with the input signal.

For the class-A circuit [Fig. 7(a)], the current consumption can be found for both situations to be

$$I_{\text{staticA}} = I_{\text{dynamicA}} = I_{B1}. \tag{6}$$

In contrast, the class-AB circuit [Fig. 7(b)] allows the current to go higher than its bias current level for the dynamic situation. This entails a larger circuit and hence leads to more current consumption as can be seen from (7) and (8), respectively

$$I_{\text{staticAB}} = 6I_{B2} \tag{7}$$
$$I_{\text{dynamicAB}} = 2I_{B2}\left(1 + 2\cosh\left(\frac{V_{\text{id}}}{n_p U_T}\right)\right). \tag{8}$$

In order to come to a reasonable comparison between these classes of circuit operation, we use the condition that provides a static condition with the same ω_u and ϕ_M. This condition can be satisfied by equating the small signal transconductance gains of both circuits, i.e., $g_{mA} = g_{mAB}$.

From (4) and (5) and by using a Taylor's series expansion we can find that

$$g_{mA} = \frac{I_{B1}}{4n_P U_T} \tag{9}$$

and

$$g_{mAB} = \frac{2I_{B2}}{n_P U_T}. \tag{10}$$

For $g_{mA} = g_{mAB}$, we then have $I_{B1} = 8I_{B2}$ and this leads to

$$I_{\text{staticAB}} = 0.75 I_{\text{staticA}}. \tag{11}$$

From now on, we will use this condition to analyze the circuit performance.

B. Signal Excursion and Drivability

After setting $I_{B1} = 8I_{B2}$, let us consider (4) and (5) again. In the case that the circuits in Fig. 7(a) and 7(b) are working as transconductors and that the input terminals are driven by the same differential input voltage, V_{id}, the output currents, I_{od}, for both cases are shown in Fig. 8 ($I_{B1} = 8I_{B2} = 8$ nA). It can be seen, as expected, that for a small V_{id} both circuits behave linearly giving the same tranconductance. For $V_{\text{id}} > 25$ mV, the output current of the class-A circuit starts saturating but for the class-AB circuit it keeps increasing exponentially. This implies that, for the CSH circuit using class-A circuitry, we can not apply an input current larger than its bias current. However, using class-AB circuitry the input current magnitude might be theoretically unlimited.
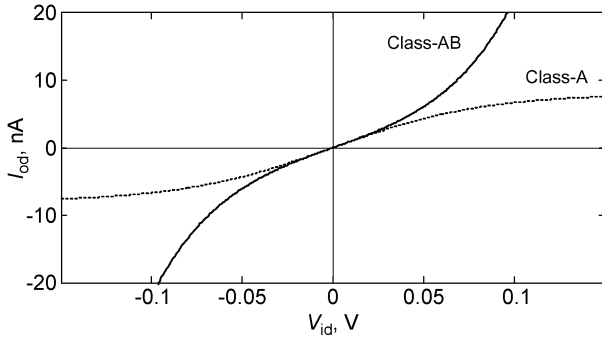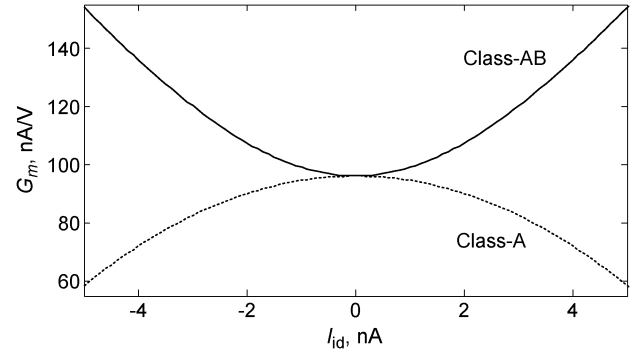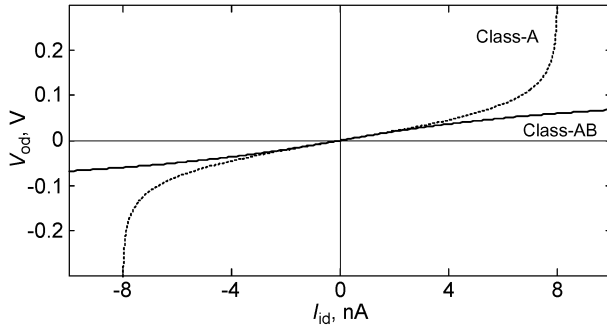
Fig. 8. $V - I$ transfer characteristics of the subthreshold transconductors.

Fig. 10. Transconductance of class-A circuit and class-AB circuit.

Fig. 9. $I - V$ transfer characteristics of the subthreshold transconductors.

This argument becomes clearer when we operate the transconductors in a negative feedback fashion as transimpedance amplifiers by applying input current I_{id}, taking output voltage V_{od} and observing the behavior of V_{od} for the entire range of the varied I_{id}. Hence, the output currents and the input voltages of the transconductors become input and output variables, respectively, and (4) and (5) are rewritten as

$$V_{od} = 2n_p U_T \tanh^{-1}\left(\frac{2I_{id}}{I_{B1}}\right) \qquad (12)$$

and

$$V_{od} = n_p U_T \sinh^{-1}\left(\frac{I_{id}}{2I_{B1}}\right), \qquad (13)$$

for the case of class-A and class-AB, respectively. These transfer characteristics are plotted and shown in Fig. 9. This situation can ideally happen when negative feedback is applied and the LG is large enough to make the voltage at the input nodes constant. Then input current I_{id} can be applied (see Fig. 5). As I_{id} comes close to I_{B1} (8 nA), the voltage goes extremely high for the case of a class-A circuit. This is an undesired feature for low voltage circuits in general since this large voltage excursion will push some circuit elements (transistors in this case) out of their proper operating region and eventually degrades the entire circuit performance. For class-AB, the circuit behaves in an opposite way such that, although the current goes high, the voltage can be kept low.

Another important design parameter that should be paid attention to is the large signal transconductance G_m. This parameter influences the dynamic circuit's LG. Taking the first derivatives with respect to V_{id} of (4), (5) and substituting (12) and (13) into the results, we can find that

$$G_{mA} = \frac{I_{B1}}{4n_p U_T} \operatorname{sech}^2\left(\tanh^{-1}\left(\frac{2I_{id}}{I_{B1}}\right)\right) \qquad (14)$$

and

$$G_{mAB} = \frac{2I_{B2}}{n_p U_T} \cosh\left(\sinh^{-1}\left(\frac{I_{id}}{2I_{B2}}\right)\right), \qquad (15)$$

for class-A and class-AB circuits respectively. To give more insight, (14) and (15) are graphically shown in Fig. 10. As one can see, G_{mA} is reduced when I_{id} goes high while G_{mAB} is enhanced. From these curves, we can predict that the accuracy (charge injection error cancellation) and bandwidth [see (3.1)] of a class-A CSH circuit will be degraded when a large I_{id} is applied since the LG becomes smaller. For a class-AB CSH circuit, the accuracy and bandwidth will be enhanced to some extent and if I_{id} keeps increasing the circuit will require a longer settling time and finally will start oscillating. This is a serious issue so that the maximum magnitude of I_{id} needs to be identified. This will be done in Section IV.

C. Noise

Since both the class-A and AB CSH circuit share the same G_{m1} stage, only the noise contribution from G_{m2} will be considered here. The flicker noise can be neglected for simplicity since it will be nullified by the inherent auto-zeroing mechanism of the CSH circuit [17]. The output current shot noise of G_{m2} will be sampled and stored on C_H. The stored noise will be converted into current noise again at the output during the hold phase. This sampled noise will be added to the noise generated by G_{m2} during the hold phase. Due to aliasing, this type of noise becomes dominant [17].

Considering Fig. 7 and assuming each current source to be formed by a single transistor operating in weak inversion saturation, the respective circuit schematics with their equivalent shot noise sources are shown in Fig. 11(a) and 11(b) for the class-A
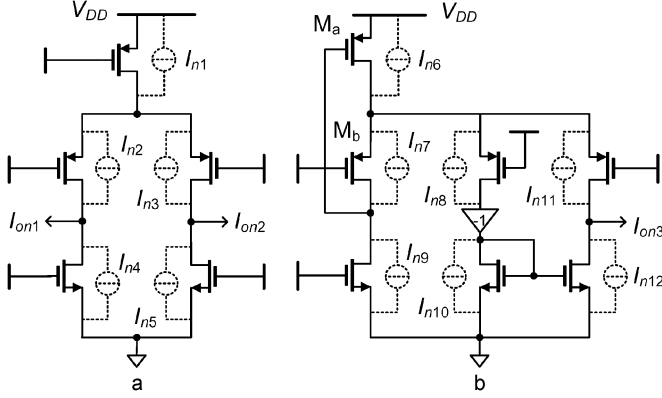
Fig. 11. Transconductors with noise sources: (a) class-A and (b) class-AB half circuit.

transconductor and the half circuit of the class-AB transconductor. For the class-A case, the average output current noise power spectral density can be found to be

$$
\begin{aligned}
S_{ioutA}(f) &= \frac{S_{ion1}(f) + S_{ion1}(f)}{4} \\
&= \frac{S_{in2}(f) + S_{in3}(f) + S_{in4}(f) + S_{in5}(f)}{4}, \\
&= qI_{B1} = 8qI_{B2}
\end{aligned}
\tag{16}
$$

where q represents the electron charge. The output current noise from the upper current source can be neglected at the output since it appears as a common-mode phenomenon only.

Let us now consider Fig. 11(b). For the static condition, due to the negative feedback formed by Ma and Mb and its large LG, noise i_{n6} does not contribute to the output. Noise sources i_{n9} and i_{n7} can be referred to the gate terminal of Mb and relayed to the output via the transistors in the middle and the right branches. This leads to

$$
\begin{aligned}
S_{ioutAB}(f) &= \frac{S_{ion3}(f)}{2} \\
&= 2\left[S_{in7}(f) + S_{in9}(f)\right] \\
&\quad + \frac{1}{2}\left[S_{in8}(f) + S_{in10}(f) \right. \\
&\qquad\qquad \left. + S_{in11}(f) + S_{in12}(f)\right] \\
&= 12qI_{B2}.
\end{aligned}
\tag{17}
$$

It can be seen for the static condition that the class-AB circuit produces 50% more noise power than the class-A circuit.

Note that (17) represents the output current noise power after neglecting noise generated from G_{m1}. In fact, both G_{m1} and G_{m2} contribute noise to the output and G_{m1} acts as an input stage with a high voltage gain and subsequently dominates the output noise power for the static situation. We know from the last section that when an input signal is applied, the drain currents of the transistors in the middle and right branches of Fig. 11(b) (G_{m2}) can be many times larger than I_{B2} (while there is no input current flowing into G_{m1} but only its bias

current) and, as a consequence, more output noise power will be generated. Therefore, for the dynamic situation with high input modulation index, the majority of output noise power will come from G_{m2} instead of G_{m1}. However, when the input current amplitude increases beyond I_{B2}, the signal power increases quadratically while the noise power spectral density increases linearly, and, as a consequence, an enhanced output signal-to-noise ratio is thus obtainable for high input modulation indices.

D. Discussion on Effects of Transistor Mismatch, Input Current Imbalance, and Switching Error Cancellation

1) *Static Offset Voltage*: The transistor mismatch creates an offset voltage that can be modeled at the input of G_{m2}. As in the case of flicker noise, this offset is to a large extent canceled out by the CSH auto-zeroing mechanism.
2) *Input Current Imbalance*: The fully differential structure of the CSH circuit requires a balanced differential input current defined by

$$
I_{in+} = -I_{in-} = I_{id}.
\tag{18}
$$

If (18) cannot be maintained, there will be a common-mode current being forced into the circuit. This common mode current will be nullified by the CMFB circuit, thereby shifting either up or down the voltage at the input node corresponding to the direction of the common mode current. For a small imbalance, this will modify the on-resistances of switches S_1 and S_2 and, as a consequence, leads to a settling time variation of the switches. For a very large imbalance, operation failure can occur.
3) *Switching Error Offset*: At the end of the sampling phase, the nonlinearity of and the mismatch between capacitors C_H, the mismatch between switches S_2 and an insufficient LG lead to incomplete switching error compensation. Also this residue error can be modeled as an input offset voltage V_{offSW} to G_{m2}, which appears during the hold phase only and equals

$$
V_{offSW} = V_{CFT+} - V_{CFT-},
\tag{19}
$$

where V_{CFT+} and V_{CFT-} are error voltages induced by charge injection and clock-feedthrough effects of the MOS switches [18] appearing on the noninverting and inverting terminals of G_{m2}, respectively. Effects of V_{offSW} will be shown for the class-A and class-AB circuits, respectively, in the following paragraph.

During the hold phase V_{offSW} is added to the differential input voltage, V_{id}, leading to

$$
I_{od} = I_{B1} \tanh\left(\frac{V_{id} + V_{offSW}}{2nU_T}\right),
\tag{20}
$$

and

$$
I_{od} = 2I_{B2} \sinh\left(\frac{V_{id} + V_{offSW}}{nU_T}\right).
\tag{21}
$$

Low order harmonic distortion components can be found for the class-A circuit to be equal to

$$HD_{2A} = \frac{\tanh\left(\frac{V_{offSW}}{2nU_T}\right)\left(\tanh^2\left(\frac{V_{offSW}}{2nU_T}\right) - 1\right)}{1 - \tanh^2\left(\frac{V_{offSW}}{2nU_T}\right)}$$

$$\times \left(\frac{\hat{I}_{id}}{I_{B1}}\right), \tag{22}$$

$$HD_{3A} = \tanh\left(\frac{V_{offSW}}{2nU_T}\right)\left(\frac{\hat{I}_{id}}{I_{B1}}\right)^2, \tag{23}$$

and

$$HD_{4A} = \frac{\tanh^4\left(\frac{V_{offSW}}{2nU_T}\right)\left(\tanh\left(\frac{V_{offSW}}{2nU_T}\right) - 1\right)}{1 - \tanh^2\left(\frac{V_{offSW}}{2nU_T}\right)}\left(\frac{\hat{I}_{id}}{I_{B1}}\right)^3, \tag{24}$$

where $\hat{I}_{id}$ represent the amplitude of the sinusoidal input current I_{id}.

For the case of the class-AB CSH circuit, it can be found that

$$HD_{2AB} = \frac{1}{16}\tanh\left(\frac{V_{offSW}}{nU_T}\right)\left(\frac{\hat{I}_{id}}{I_{B2}}\right)^2\left(1 - \frac{1}{16}\left(\frac{\hat{I}_{id}}{I_{B2}}\right)^2\right) \tag{25}$$

and

$$HD_{4AB} = \frac{1}{1024}\tanh\left(\frac{V_{offSW}}{nU_T}\right)\left(\frac{\hat{I}_{id}}{I_{B2}}\right)^3. \tag{26}$$

There is no HD_3 for this case.

Note that the distortion analysis here is obtained by ignoring the nonlinearity of the common-mode feedback circuits which may further degrade the linearity of the CSH circuit. However, for comparison, this result is sufficient to support that the class-AB transducer provides less undesired harmonic components.

IV. DESIGN OF A CLASS-AB SAMPLE AND HOLD CIRCUIT

From the previous section, we can see that the class-AB circuit provides less distortion, consumes less power, and allows very high current signal swing while the internal voltage swing can be kept low. For this reason, even though in the static situation the class-AB circuit contributes 50% more noise than the class-A circuit, a larger signal-to-noise ratio can be obtained. In this section, several issues of the class-AB CSH circuit design are discussed.

Replacing C_H by PMOS capacitors ($M_{cap}s$), as shown in Fig. 12, to save silicon area, the $M_{cap}s$ need to be biased in strong inversion to maximize their capacitances. To do so, the input and output nodes of active element A need to be biased to accommodate the threshold voltage of M_{cap}. Since we would like to keep the noise power low and we do not need a high current drivability for this stage but high voltage gain, the class-A folded cascode transconductor shown in Fig. 13(a) is chosen to realize element A. Its common-mode output voltage can be controlled by the CMFB1 circuit shown in Fig. 13b
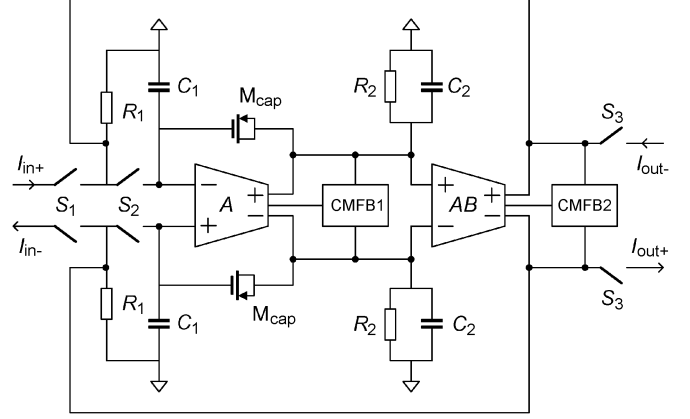

Fig. 12. Macro-model with MOS capacitors and parasitic included.
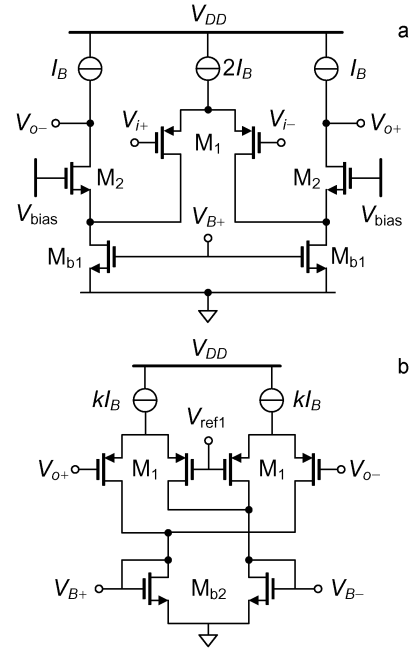

Fig. 13. (a) Folded cascode amplifier and (b) its common-mode feedback circuit.

where $k = 0.05$ is a scaling factor to save current consumption. The class-AB circuit in Fig. 14(a) is used for active element AB and its CMFB2 circuit is shown Fig. 14(b). The bias current in this case is not scaled down since, to minimize noise and satisfy the stability condition, I_{B2} is set low already ($I_{B2} = 0.4$ nA) and scaling down further it may become difficult to make it precise.

A. Bias Conditions

To keep all transistors working in weak inversion saturation the following bias conditions are set:

$$V_{ref2} \cong 4U_T \text{ and } V_{ref1} \cong V_{ref2} + |V_{tp}|, \tag{27a}$$

and

$$V_{DD} \cong V_{ref1} + V_{SG3} + 4U_T + V_{swing}, \tag{27b}$$

where V_{swing} is room for the internal voltage swing that follows from the relationship of (13).
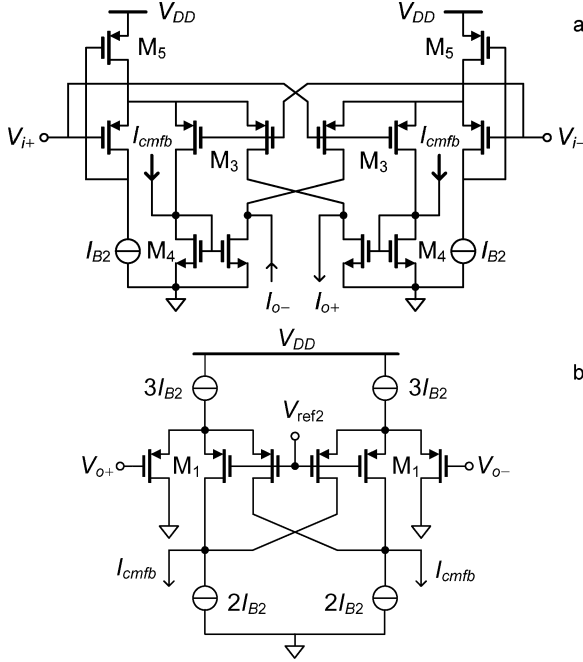
Fig. 14.   (a) Subthreshold class-AB transconductor and (b) its common-mode feedback circuit.
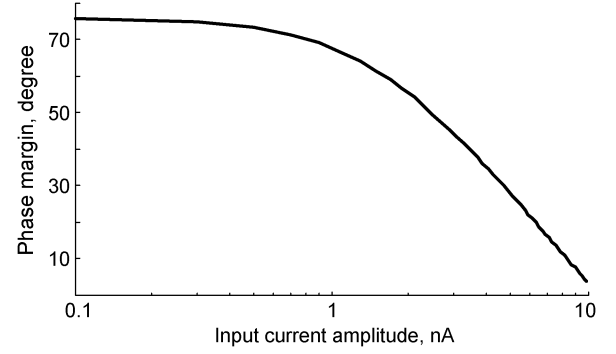

Fig. 15.   Phase margin versus input current amplitude.
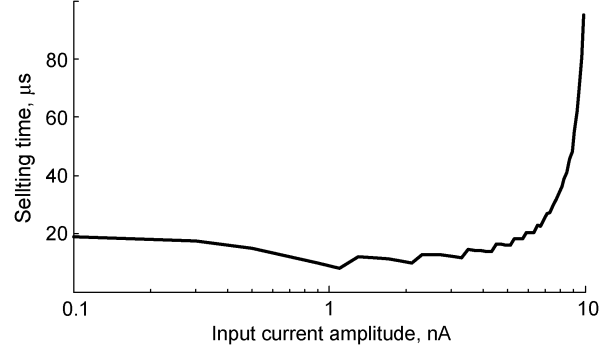
Fig. 16.   Settling time versus input current amplitude.

TABLE I
TRANSISTOR DIMENSIONS

MOSFET	W [μm]	L [μm]
M_1	2	0.5
M_2	1.5	0.5
M_3	0.25	1.5
M_5	0.5	1
M_{b1}	20	1
M_{b2}, M_4	1	1
M_{cap} (0.25pF)	10	10

To satisfy the condition of $\phi_M \geq 60°$, $\omega_{p2} \geq 2.2\omega_u$. In order to fulfill this condition, the bias currents are set to

$$I_B = 25I_{B2}. \tag{28}$$

This leads to a total current consumption (excluding that of the bias circuit) of

$$I_{B\text{total}} = 4.1I_B + 12I_{B2} = 114.5I_{B2}. \tag{29}$$

B. Input Current Limitation and Settling Behavior

As mentioned in Sections II-C and III-B, a 60° phase margin cannot be maintained for the entire range of I_{id}. It is indicated by (15) that G_{mAB} changes according to I_{id} and this leads to circuit instability for large amplitudes of I_{id}. We set the safety limit at a $\phi_M \cong 45°$, for which $\omega_u = \omega_{p2}$. Hence, the maximum I_{id} that we can apply within this safety limit can be found as

$$I_{\text{idmax}} \cong 2I_{B2}\sinh\left(\cosh^{-1}\left(3.125\frac{C_H}{C_1 + C_2}\right)\right). \tag{30}$$

For I_{id} larger than I_{idmax}, the phase margin will become smaller than 45°.

Fig. 15 shows the theoretical plot of ϕ_M versus input current amplitude, $\hat{I}_{id}$, for the following realistic parameters, $I_B = 10$ nA, $I_{B2} = 0.4$ nA, $n = 1.6$, $U_T = 26$ mV, $R_1 = 400$ MΩ, $R_2 = 120$ MΩ, $C_1 = 0.2$ pF, $C_2 = 0.32$ pF, and $C_H = 0.25$ pF. It can be seen that for input amplitudes greater than 0.5 nA, ϕ_M decreases rapidly.

The settling time, t_s, of this closed-loop system behaves consistently with ϕ_M. Fig. 16 shows a plot of t_s versus $\hat{I}_{id}$ with $\varepsilon = 0.02$. As $\hat{I}_{id}$ increases, the system response goes from over damped to critically damped and t_s decreases when $\hat{I}_{id}$ increases. For $\hat{I}_{id}$ slightly greater than 1 nA, the system response moves to the underdamped case and a ripple of t_s occurs

[22]. Finally, t_s goes up rapidly as $\hat{I}_{id}$ approaches 10 nA since the system enters the undamped situation. This implies that the maximum sampling frequency of this CSH circuit depends on $\hat{I}_{id}$ and, in this particular example, to cover $\hat{I}_{id}$ from 0.1 nA up to 5 nA, the sampling interval should be longer than 20 μs. Also for higher amplitudes (5 nA < $\hat{I}_{id}$ < 10 nA), the required sampling period rapidly rises and reaches 0.1 ms at $\hat{I}_{id} = 10$ nA.

V. CIRCUIT SIMULATIONS

The class-AB CSH circuit has been designed and simulated in Cadence/RF Spectre using TSMC 0.13 μm CMOS process parameters. Transistor sizes are shown in Table I. $V_{DD} = 0.6$ V, $V_{ref1} = 0.42$ V, $V_{ref2} = 0.1$ V and $C_H = 0.25$ pF. Biasing currents $I_B = 10$ nA and $I_{B2} = 0.4$ nA are set for G_{m1} and G_{m2}, respectively. All switches are realized by NMOSTs with a threshold voltage of $V_{tn} \cong 0.3$ V and driven by clock signals switching between V_{DD} and ground. The dimensions of the switches are all identical and chosen to be as small as the process allows to minimize charge-injection and clock-feedthrough effects ($W = 0.15$ μm and $L = 0.13$ μm). The quiescent power of the entire circuit equals 27.5 nW.
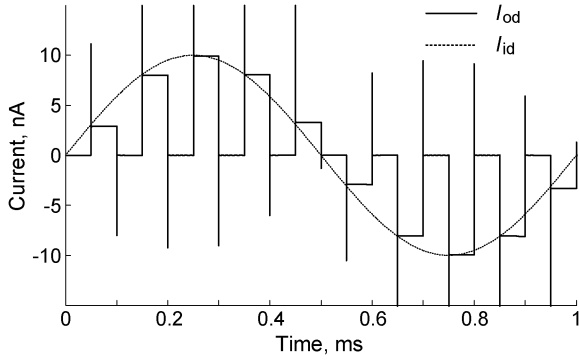
Fig. 17. Transient input and output current: $I_{id} = 10$ nA$\sin(2000\pi t)$ and $f_s = 10$ kS/s.

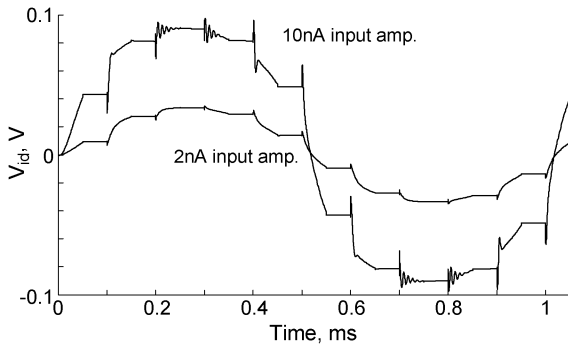Fig. 18. Internal node voltage swings at different input amplitudes.
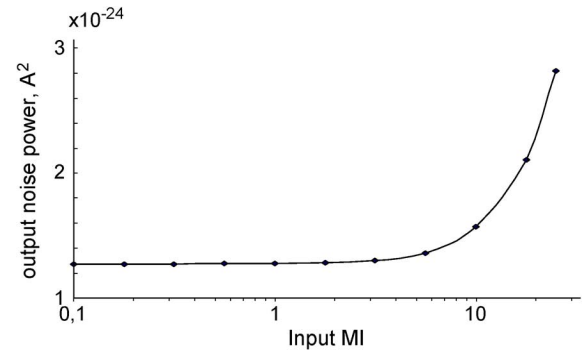

Fig. 19. Integrated noise power from 1 Hz–10 kHz as a function of the modulation index.

Fig. 20. Spectral performance metrics as function of the modulation index.

Fig. 21. Monte-Carlo simulation of the THD for an input MI of 25.

Fig. 17 shows the transient input and output currents with an amplitude and frequency of 10 nA and 1 kHz when the CSH is sampled by a 10 kS/s clock signal with a rise and fall time of 50 ns. The large glitches appearing at the beginning of the hold phase are induced by a sudden change of the CSH circuit's output resistance as a consequence of the discontinuity of the LG. The nonoverlapping clock transition (from switching off S_2 to switching on S_3) allows large voltages (products of the held currents and the large output resistances) being produced at the output terminals of G_{m2}. It leads to large voltage differences across switches S_3 (assuming they are loaded by a similar CSH circuit having a fixed input voltage). Switching on S_3 will bring down the high voltages to this voltage. This process happens across the drain-source parasitic capacitances of S_3 for a very short period of time, when the large currents flowing through the output in addition to the desired output current are generated. This mechanism not only produces the glitches but also deteriorates the circuit's linearity. At the moment that the output voltages suddenly go high before completely closing S_3, small charges (fed through the parasitic gate—drain capacitances of M3) will be added to C_H giving a memorized voltage error [23]. However, there are two ways to reduce these glitches thereby enhancing the circuit's linearity: 1) trying to eliminate the nonoverlapping moment by employing a special clock scheme [24] and 2) creating low impedance output nodes by introducing current followers at the output terminals of G_{m2}. This can be done at circuit level by cascoding output transistor M3 [7]. However, since the introduced voltage error is already small, we have not adopted any of these solutions for our design.
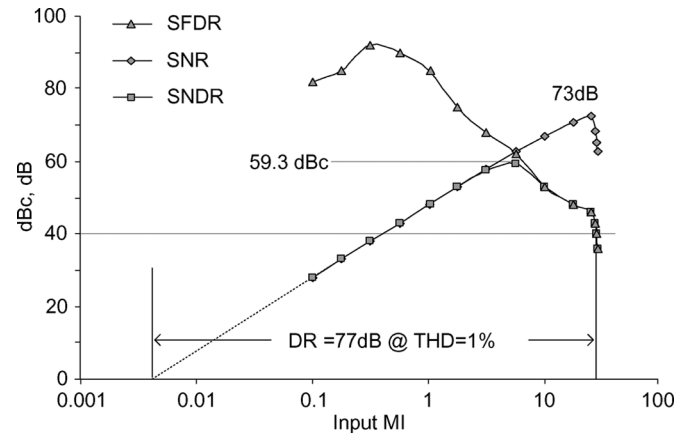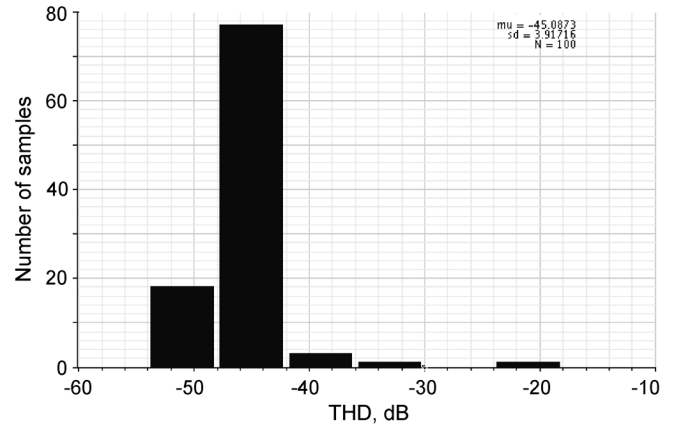
The internal differential voltage swings at the input of G_{m2} are shown in Fig. 18. For a 1 kHz sinusoidal input current with an amplitude of 2 nA, the CSH circuit responds slowly since G_{m2} and ω_u are low and there is no ringing during the entire cycle. For the case of a higher input current amplitude (10 nA), the ringing appears when V_{id} reaches 0.09 V. This is because G_{m2} is enhanced according to (15) and ω_u moves closer to ω_{p2}; the phase margin and settling time of the CSH circuit are degraded.

Noise and linearity performances were verified using periodic steady state (PSS) and periodic noise (PNOISE) analyses for

Fig. 22. SFDR versus input modulation index PVT simulations: (a) typical at 40 °C; (b) slow at 80 °C; and (c) fast at 0 °C cases.

TABLE II
PERFORMANCE COMPARISON

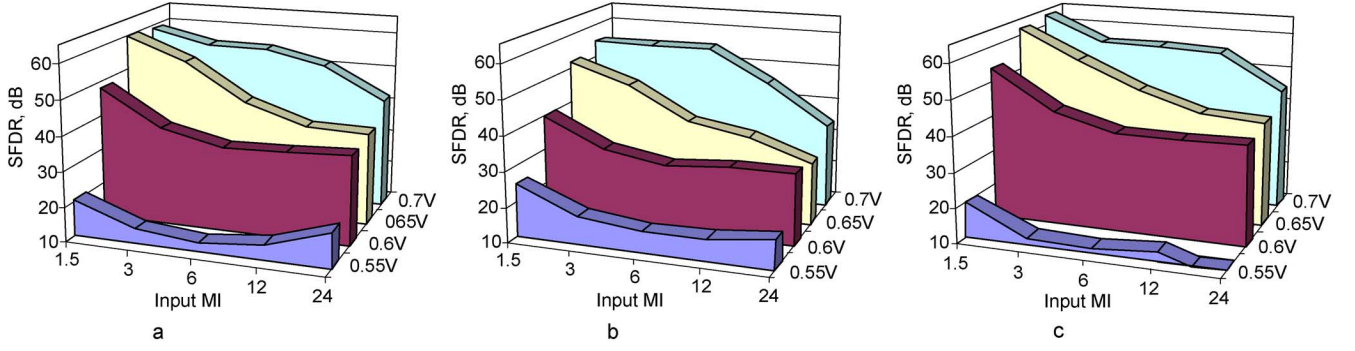| Parameter	[4][*]		[19][*]	[20][**]	[21][**]	This work[*]	
Tech. [μm]	0.35[†]	0.18[††]	0.35	0.35	0.35	0.13	0.13
V_{DD} [V]	1	0.35	3.3	1	2	0.6	0.8
Static P [W]	5.8μ	2.6μ	6m	3m	6m	28n	1.84μ
f_s [MS/s]	1	1	13	35	100	0.02	1
SNR_{max} [dB]			60	56	62	73	72
ENOB [bit]	-	-	-	-	13	9.6	8.7
DR [dB]	73	68.2	60	56	-	77	76
THD [dB]@	−41	−38.6	−66	−55	−77	−40	−40
f_{in} [Hz],	-	-	1.3M	1.32M	1M	1k	50k
MI	1	1	0.98	0.9	0.9	27	22

[*]simulation, [**]measurement, [†]cascoded SI cell, [††]S²I cell

12 harmonics. A 1 kHz input signal with its amplitude varying from 40 pA to 11.5 nA was applied with a 20 kS/s sampling rate. Fig. 19 shows the output noise power integrated from 1 Hz to 10 kHz as a function of the modulation index (the modulation index is defined by $MI = \hat{I}_{id}/I_{B2}$). It can be seen that the noise power remains constant in the range of $0.1 < MI < 1$. For MI higher than 1, the noise increases. This is in line with what we predicted in Section III-C, namely, that the input current modulates the drain currents of the transistors in the class-AB transconductor, thereby creating more shot noise.

The spurious-free dynamic range (SFDR), SNR, and signal-to-noise plus distortion ratio (SNDR) are plotted and shown in Fig. 20. From this plot, a DR (measured up to a 40 dB SFDR corresponding to a total harmonic distortion, THD, of 1%) of 77 dB is obtained and an SNDR of 59.3 dB can be achieved at a 2.25 nA input amplitude. This leads to an effective number of bits of

$$ ENOB = \frac{SNDR - 1.76}{6.02} = 9.6 \text{ bits.} \quad (31) $$

Therefore, a figure of merit that embraces the effects of distortion, sampling speed, and power consumption, of

$$ FoM = \frac{P}{f_s \cdot 2^{ENOB}} = 1.9 \text{ nW/MHz} \quad (32) $$

is obtained where P represents the average power consumption and f_s is the sampling rate. This number is more than an order of magnitude lower than that of the measured results obtained from a recently proposed CSH circuit (of which FoM = 30 nW/MHz) [21].

To see the effect of transistor mismatch on the circuit linearity, a Monte-Carlo transient simulation using a 976.6 Hz 10 nA amplitude sinusoidal I_{id} (corresponding to MI = 25, which is the maximum amplitude that can be applied before oscillation; see Fig. 18) and $f_s = 20$ kS/s has been done. The results are shown in Fig. 21. For 100 runs, a mean value of the THD of −45 dB is obtained with a standard deviation of 3.92 dB.

Fig. 22 shows the CSH circuit's simulated SFDR versus MI for extreme processes, temperature, and supply voltage conditions with the same setup as used for the above Monte-Carlo simulation. It can be seen that the minimum operating supply voltage that the circuit can handle is 0.6 V. From this supply voltage, running slow transistors at high temperature (80 °C) gives us the worst results. For MI greater than 1.5, the SFDR falls from 40 dB to around 30 dB. For higher supply voltages, better linearity is obtained for all process and temperature corners.

A performance comparison with previously reported CSH circuits is presented in Table II. In addition to the simulations mentioned above, we also tested the CSH circuit for higher input and sampling frequencies (50 kHz and 1 MS/s, respectively). To do so, the bias current levels were changed to $I_{B1} = 25I_{B2} = 500$ nA. To handle the larger gate-source voltages of all transistors, we increased the supply voltage to $V_{DD} = 0.8$ V. The results are summarized in the last right column. At this bias point, transistors that form G_{m1} enter moderate inversion for both static and dynamic situations. For the dynamic situation with high input modulation index, some transistors that form G_{m2} will be forced into moderate inversion as well. As a consequence, parasitic capacitances C_1s become bigger and C_2s

change dynamically according to the input amplitude. This affects the dynamic stability condition and results in a reduced allowable signal swing. The obtained DR becomes 2 dB less than the low-power, low-frequency operation purely based on weak inversion operation. In terms of linearity, THD better than -40 dB is obtained at MIs lower than 22 while the same level of THD can be achieved for MIs up to 27 in the lower power low-frequency case. In comparison with other designs, as can be deduced from the SNR$_{max}$ of [19]–[21], class-A operation provides us less than 62 dB of dynamic range. As we can see from [4] (weak inversion class-AB SI memory cells) and this work, to reach higher than 70 dB DR, class-AB operation is required.

VI. LAYOUT CONSIDERATIONS

Apart from separating digital and analog supply lines in order to avoid coupling, parasitic immittances at every circuit node may also lead to performance degradation and should be carefully analyzed as well before completing the layout.

A first-order estimation can be made by considering that in low-power circuits operating at relatively low frequencies, only parasitic capacitances in parallel with the signal path may play a significant role. As our design contains transistors in weak inversion that suffer from threshold voltage mismatch, these transistors must be of large size with identical width and length. Local surrounding (dummy) and common centroid layout arrangements should also be applied. This gives us extra parasitic capacitances at every node in the circuit. Fortunately, by circuit inspection, we can see that the internal high impedance nodes already have capacitances associated, C_1 and C_2, and all other nodes have a relatively small impedance (dominated by g_m^{-1}). Hence, all parasitic immitances due to the layout can thus be accounted for by C_1 and C_2.

The analysis results provided in Section II-C already include these capacitance values. After layout extraction, these values can guide us in adjusting the Mcaps to maintain circuit stability and a proper transient response. The actual output noise power obtained may deviate a little from the noise power obtained from circuit schematic simulation due to the modified transfer function which may result from the compensation for parasitic capacitances. However, this is not expected to severely degrade the overall circuit performance.

VII. CONCLUSION

Theory and design of a subthreshold class-AB CSH circuit have been presented. Benefitting from negative feedback and the exponential behavior of the transistors in weak inversion, the proposed CSH circuit can be operated from a very low supply voltage and consumes very little quiescent power. In addition to that, high SNR, DR, and a very good FoM are obtained. Monte-Carlo and corner simulations also confirm that a good linearity of the circuit can be maintained when realistic mismatch, process, voltage, and temperature variations are taken into account.

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