# 20MSPS 4-bit Charge Redistribution Digital-to-Analog Converter with Deglitching Sample-and Hold Filter

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**Abstract**

Digital-to-analog converters (DAC) are used to recreate analog signals stored in digital form. Such a circuit takes digital input and converts it to equivalent analog voltage which can be used to drive a transducer. There are two major categories of DACs: Nyquist rate and Oversampling rate converters. The most simplistic DAC topology is the Nyquist rate converters. The most common Nyquist rate converters used historically are R-2R network DAC and Current steering DAC. However, they consume a lot of current and would not be an optimum choice for portable applications. Thus, charge redistribution DAC pose a greater advantage for the same application in low chip area and low power.

## I. INTRODUCTION

DAC (Digital to Analog Converter) is a device in electronics, which converts a digital signal into and analog signal. Several DAC architectures exist in literature and the suitability of DAC for an application is dependent on certain parameters as resolution, accuracy, sampling frequency. To achieve precision DAC's are mostly implemented as integrated circuits.

DACs are used in music players, televisions, mobile phones to convert digital data (audio/video) to analog signals. *The audio DAC is a low speed high resolution type while the video DAC is a high speed low to medium resolution type*.

A DAC converts a finite binary number into a physical quantity i.e. voltage, pressure. An ideal DAC converts the digital data into continuous data by processing it through a reconstruction filter to prevent the loss of data during conversion. A DAC might convert a data into a sequence of rectangular functions that can be modeled with zero-order hold or it can produce a pulse modulated output that can be similarly filtered to produce a smoothly varying signal.

The reconstruction of data is contingent to its bandwidth meeting certain requirements, e.g. a baseband signal with bandwidth less than Nyquist frequency. The data is written to DAC with a clock signal, that latches each data in a sequence, simultaneously the DAC output voltage changes from previous value to the value represented by the currently latched data. In simple words, the DAC output voltage is held at the current value till the next input is latched, which results in a piecewise constant or staircase shaped output.

*The fact that DACs output a sequence of piecewise constant values (known as zero-order hold in sample data textbooks) or rectangular pulses causes multiple harmonics above the Nyquist frequency. Usually, these are removed with a low pass filter acting as a reconstruction filter in applications that require it.*

### Types of DAC

1. The pulse width modulator is a basic DAC type.

2. Oversampling DACs or interpolating DACs use a pulse density conversion technique. A low resolution DAC is possible to be use with oversampling technique. This technique is preferred in high resolution DACs (i.e. greater than 16 bits) due to its high linearity and low cost.
3. Binary weighted DAC utilizes a summing op-amp circuit. The MSB to LSBs are distinguished by weighted resistors. This is one of the simplest and fastest conversion methods but suffers from poor accuracy because of high precision required for each individual voltage or current.
4. The R-2R ladder DAC which is a binary-weighted DAC that uses a repeating cascaded structure of resistor values R and 2R. This improves the precision due to the relative ease of producing equal valued-matched resistors (or current sources). They offer lower conversion speed then binary weighted DAC.
5. A charge redistribution DAC offers better performance over other types of DACs.

**Specifications of DAC:**

1. *Resolution*: It is defined as the smallest analog increment corresponding to 1 LSB change. Resolution = $V_{LSB} - \frac{V_{ref}}{2^N}$, N = number of bits.
2. *Speed*: This is the rate of conversion of single digital input to its analog equivalent. This conversion rate is dependent on clock speed of input signal and settling time of converter.
3. *Linearity*: This is the difference between the desired analog outputs to the actual output over the full range of expected values.
4. *Settling time*: The time taken by the output signal to settle within +/- ½ LSB of its final value after a given change in input scale. This is limited by the slew rate of the amplifier.

**Differential non-linearity (DNL)** and **Integral Non-linearity (INL)** determine the static performance of DAC. DNL shows how two adjacent analog values deviate from ideal 1 LSB step and INL shows how much the DAC transfer characteristics deviates from the ideal one.

**II. PROPOSED TOPOLOGY**

**The Charge Redistribution Topology**

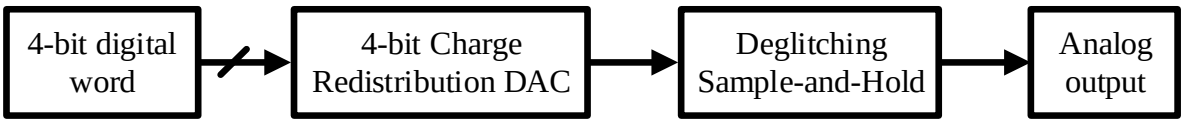


*Fig. 1 Top level block diagram*

Fig. 1. is used to depict the topology to be designed. The 4 bit digital word shall be provided at the beginning of every conversion cycle. The DAC core will convert the 4-bit digital value to the equivalent analog value. However, the capacitor network being binary weighted, ringing may be observed at the change of MSB. To prevent the ringing, a deglitching sample-and-hold circuit is introduced at the output stage.

**Charge Redistribution DAC core**

The 4 bit-charge Redistribution DAC is one of the sub-category of switch-capacitor amplifier circuits. The switch capacitor amplifier is shown in Fig. 2. Here, clock phase 1 is the sampling phase where the input is sampled. Thus, the voltage is stored as charge in capacitor C1. The clock phase 2 is the amplification phase, and here the switches are set so as to create an inverting amplifier configuration,

where C2 is the feedback impedance. Thus, the gain of the system is -C1/C2. This property can be exploited to create a data converter such that the output voltage changes based on the value of C1. The proposed DAC circuit is shown in Fig. 3.

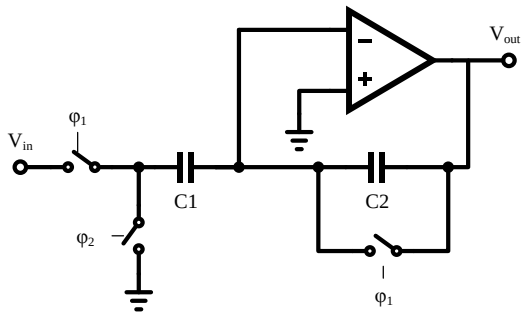


*Fig. 2 A basic switch capacitor amplifier*

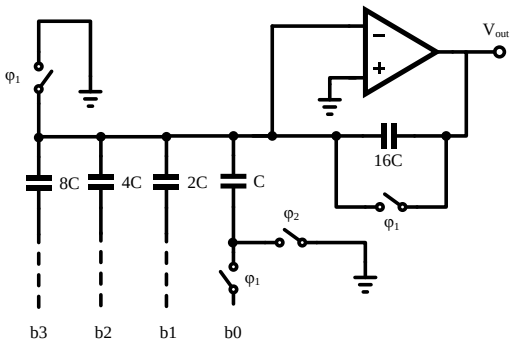


*Fig. 3 A 4-bit switch capacitor DAC*

As shown, the bit values are stored on binary weighted capacitor network as charge when clock phase 1 is active. It should be noted that the bit value '0' is ground voltage, whereas bit value '1' is some reference voltage selected based on the input common-mode of the operational amplifier. For phase 2, the network acts as an inverting amplifier of gain -CN/16C, where CN is the equivalent capacitance activated as a result of the logic '1' bits.

**Deglitching of Binary weighted DAC output**

Glitching is a major problem for binary weighted DAC, as when there is a major digital word change, e.g. from 1000 to 0111, the output changes drastically due to the MSB input network impedance being smaller. This causes the output to ring based on the phase margin of the operational amplifier. This introduces distortion in the output signal, as observed in Fig. 4. Thus, a deglitching circuit can be implemented using a sample-and-hold circuit as shown in Fig. 5.

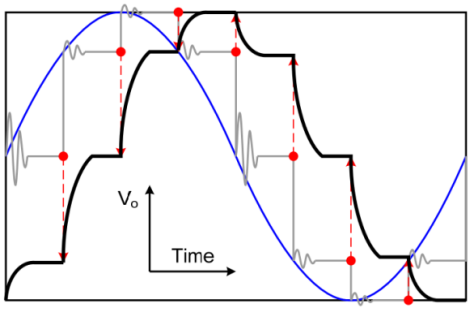


*Fig. 4 Signal through a DAC Topology. Blue: expected output. Gray: output of DAC core. Black: Output after Deglitching*

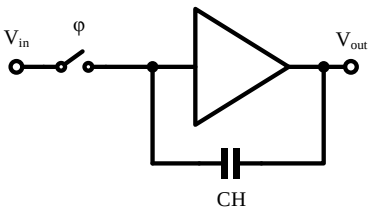


*Fig. 5 Sample-and-hold circuit*

When the clock phase is active, the output of the DAC core is sampled and stored as charge in capacitor CH. When the clock is inactive, the charge is held by the operational amplifier and CH. Thus, it should be noted that for deglitching function, the sampling phase should be active only when the output of the DAC core has settled [1].

**III. SPECIFICATIONS**

Considering system-on-chip (SoC) solutions becoming more popular for an integrated solution in portable electronics, it is assumed that the DAC works at the same voltage as the digital counterpart of the SoC. This enables for simpler integration without need of higher supply voltage or special need of voltage translators. The below specifications are based on typical DAC operating conditions.

| | |
|---|---|
| Supple voltage | +/- 1.5 V |
| Load capacitance | 1 pF |
| Sampling rate | 20 MSPS |
| Differential nonlinearity (DNL) | +/- 0.5*LSB |
| Integral nonlinearity (INL) | +/- 1*LSB |

Based on the above requirements, we define the specifications for the DAC operational amplifier as given below. Since we assume that we sample at 100 MSPS, by Nyquist's sampling theorem, we design the DAC amplifier for 2.5 X operation. The output swing is limited to 1.3 considering 0.25 V of headroom on both power rails.

| | |
|---|---|
| GBW | 170 MHz |
| Closed loop gain | 2x |
| Settling time | 15 ns |
| Settling error | -60 dB |
| Load capacitance | 1pF |
| Output swing (peak to peak) | 1.3 V |
| Slew rate | >250 V/µs |

For the deglitching sample-and-hold, we assume that since the sampling rate is 100 MSPS, the gain bandwidth product is set to 100 MHz since it should not allow passing of ringing as well as higher frequency output transitions. Thus, it rejects any signal perturbations beyond the input sampling rate. Also, since the gain bandwidth product depends on the current consumed, the sample-and-hold can work at a lower current, reducing power consumption.

| | |
|---|---|
| GBW | 100 MHz |
| Closed loop gain | 1x |
| Settling time | 15 ns |
| Settling error | -60 dB |
| Load capacitance | 1 pF |
| Output swing (peak to peak) | 1.3 V |

## IV. LITERATURE REVIEW

There is a lot of existing literature concerning the DAC architectures and their implementation. Charge redistribution DAC has been discussed in [2] which has served as an important reference for the design of DAC architecture. The authors in this paper have proposed an 8-bit charge redistribution and due to the usage of double bit processing in a single capacitor, the capacitor area was considerably reduced in comparison to conventional binary-weighted DAC.

Folded cascode topology is the most popular approach for achieveing high speed op-amps. The author in [3] has discussed the design of single stage folded cascode gain boost amplifier, which has a high gain and unity gain frequency. This paper has served as an motivation for the design of folded cascode topology for the DAC architecture.

The frequency response of an Op-amp helps in analysing its behavior and therefore the performance of the circuit. The analysis of poles-zeros and the settling time thus forms an important part of the design analysis. The authors in [4] have studied the effects of poles-zeros on the frequency response and settling time of operational amplifiers. They have shown how the presence of these in transfer function of op-amps degrades its settling time but causes only minor changes in the frequency response.

Sample and Hold circuit discussed in [5] describes the design of an all-npn open loop sample and hold amplifier intended for use at the front end of analog-to-digital converters. Its series-capacitor sampling technique is useful in low voltage applications.

## V. ARCHITECTURE DESCRIPTION

As explained in Section II, 1. **Charge redistribution DAC topology** is being used and the proposed circuit design is shown in Fig 3. The folded cascade op-amp is being used for the proposed topology because of the numerous advantages it has to offer. It offers high voltage swing, input-output can be shorted and the choice of input common mode is easier. The bias voltage is critical for the circuit.

### *2.* Folded cascode

For a ***folded cascode*** op-amp, in an NMOS/PMOS cascode amplifier the input device is replaced by opposite type while still converting the input voltage to current. Folded structure provides the choice of voltage levels because it does not stack the cascode transistors on top of the input device.

Folded topology can also be applied to differential op-amps. Fig 13. shows the folded cascode topology used for the designed DAC circuit. $M_1$ and $M_2$ are the input NMOS pair with $M_3$ as the tail current source. $M_{11}$ – $M_{14}$ are the PMOS cascode loads while $M_{10}$, $M_{15}$-$M_{17}$ is the wide swing current mirror. The tail current source $M_3$ must be wide enough to carry the drain currents of $M_1$ and $M_3$.

Here, NMOS input pair is being used as for comparable device dimensions and $I_{bias}$, the PMOS differential pair exhibits a lower gm than the NMOS pair. But this lowers the pole at the folding point (node X) i.e. $M_{13}$-$M_{14}$.

Node X = $\frac{1}{gm_{14} + gmb_{14}} . C_{tot}$, magnitude of both these components is relatively high and hence the pole is away from the origin.

The **frequency response** of the folded cascade op-amp is determined by the output pole which is given by:

$$p_{out} = \frac{1}{C_{out}\, R'_{out}} \text{ , where } R'_{out} = (\frac{2+k}{2+2k})R_{out} \text{ and k is given in Table 1.}$$

$C_{out}$ is all the capacitance connected from the output of p-amp to ground. All other poles must be greater than GB= $\frac{gm_1}{C_{out}}$ . To achieve more gain, the folded cascade op-amp can be enhanced to boost the output impedance (Fig. 6)

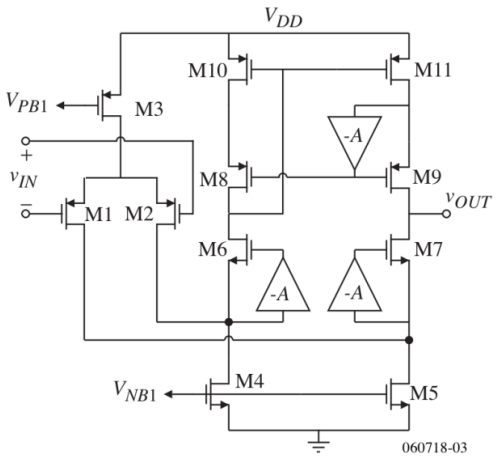


*Fig.6 Enhanced gain folded cascade [5]*

Voltage gain = $g_{m1}R_{out}$, where $R_{out} = [Ar_{ds7}g_{m7}(r_{ds1}||r_{ds5})]||(Ar_{ds9}g_{m9}r_{ds11})$

$M_5$ and $M_{11}$ are biased with $V_{DS} = V_{DS}(sat)$ to achieve maximum output swing. Similar concept was applied to the final simulated folded cascade circuit.

***3.*** **Sample & Hold Circuit for deglitching**:

Sample and hold circuit is used to track an analog signal. The circuit holds the signal when the "hold" command is given, thereby acting as an analog signal storage device. An ideal sample and hold circuit can track any analog signal and hold the same without any delay. The hold signal can then be used for digital data conversion, because of which this circuit finds wide use in data converters. Fig. 7 shows a basic sample and hold circuit and the following fig shows a simple S/H Amplifier consisting of a switch, hold capacitor, and input and output buffers.

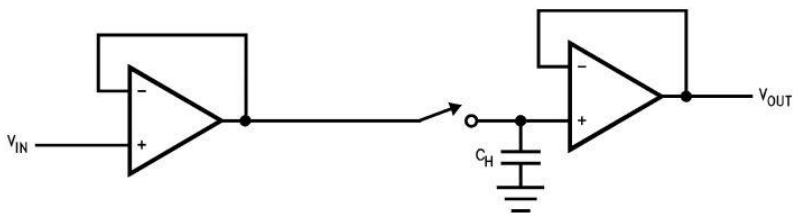


*Fig 7. A Simple S/H Amplifier Consists of a Switch, Hold Capacitor, and Input and Output Buffers*

There are two working modes for the S/H circuit: sample to hold mode and hold to sample mode. Fig. 8 shows the transition between the two modes.

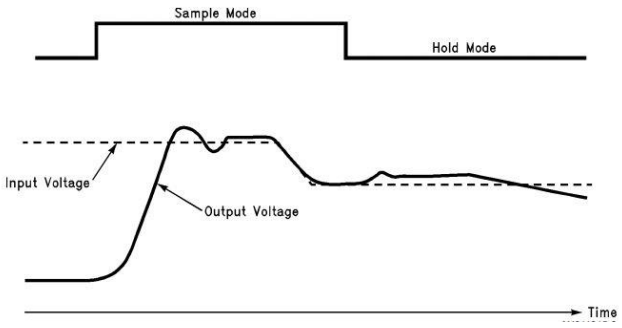


*Fig.8 Two modes of S/H and the transitions between the two modes [7]*

It is important to understand the specifications of the circuit for each mode while designing the same.

**Important performance parameters for sample and hold circuit:**

1. *Sampling pedestal or hold step*: This step occurs every time there is a transition from sample (tracking the signal) mode to hold mode. Due to delay or less precision there is an error in the voltage being held to the value of input voltage at the time of sampling. It is always required to minimize this error to prevent any distortion in the signal. The hold step can be determined by

$$V_{HS} = \frac{Q}{C_H}$$

Where Q = charge transferred to the hold capacitor, hence hold step can be reduced by increasing the value of the hold capacitor.

2. *Droop rate*: It is the rate at which the output voltage is changing due to leakage from the hold capacitor. The droop rate depends on the value of the hold capacitor

$\frac{dV_{CH}}{dt} = \frac{I_L}{C_H}$, $I_L$ is the hold capacitor leakage current.

3. *Aperture jitter or uncertainty*: This occurs due to the effective sampling time changing from cycle to cycle. It mainly occurs when high speed signals are sampled which causes an error in the held voltage to the input voltage.

4. *Speed*: It is always desired to use the circuit at high speed to frequently sample and then hold the signal. But while using with Op-amps there is always a tradeoff between its 3-dB bandwidth and slew rate to power consumption

***4.*** **CMOS Transmission gate**:

For implementing logic functions, series and parallel combinations of switches can be utilized. These switches are controlled by input logic variables to connect the input and output nodes.The switches can be implemented either by single NMOS transistor (Fig. 9) or by a pair of complementary MOS

transistors connected together to form CMOS transmission gate configuration (Fig. 10). Pass transistors reduce the number of transistors required to implement the logic.

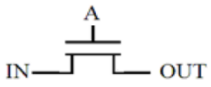


*Fig.9 Pass Transistor [8]*

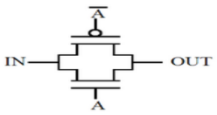


*Fig.10 Transmission gate [8]*

**High CMOS Transmission Gate:**

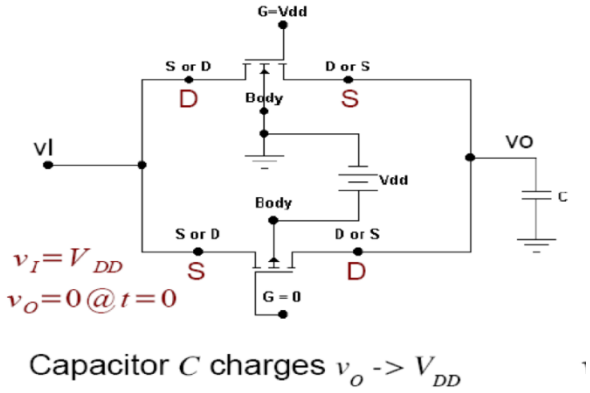


*Fig.11. High CMOS transmission gate [8]*

- PMOS device has source (S) on left and: $V_S = V_{DD} = V_B$ , $|V_{tp}| = |V_{t0p}|$, $V_{SB} = 0$; hence there is no PMOS body effect.
- NMOS is ON, $0\,V \leq v_o < V_{DD} - V_{TN}$, $v_{SG} = V_{DD} - 0 > |V_{tP}|$ for $0\,V \leq v_o \leq V_{DD}$, PMOS is ON $0\,V \leq v_o < V_{DD}$

**Low CMOS Transmission Gate:**

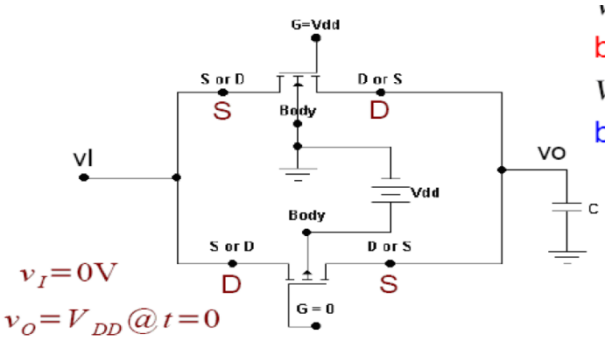


*Fig.12. Low CMOS transmission gate [8]*

- $V_{SB} = v_o - V_{DD}$, there is a PMOS body effect and $|V_{tp}| \neq |V_{t0p}|$.
- $V_{SB} = v_I = 0V$, there is no NMOS effect and $V_{tn} = V_{t0n}$.
- NMOS: $v_o = 0$ @ $t = 0$

- NMOS is on $0V \leq \ \mathrm{v_o} \leq \mathrm{V_{DD}}$
- PMOS: $V_{SG} = \ \mathrm{v_o} - 0 > \left| V_{tp} \right|$ for $\left| V_{tp} \right| < \ \mathrm{v_o} \leq \ \mathrm{V_{DD}}$
- PMOS is ON $\left| V_{tp} \right| < \mathrm{v_o} > \mathrm{V_{DD}}$

**Resistance of Transmission Gate:**

- $R_n = \frac{2V_{DD}}{K_n(V_{DD}-V_{tn})^2}$
- $R_p = \frac{2}{K_p(-V_{DD}-V_{tp})}$

**ON- Resistance of Transmission Gate:**

*PMOS and NMOS : Saturation*

- $r_{DSN} = \frac{2(V_{DD}-\mathrm{V_O})}{K_n(V_{DD}-\mathrm{V_O}-V_{tn})^2}$
- $r_{DSP} = \frac{2(V_{DD}-\mathrm{V_O})}{K_p(V_{DD}-\left|\mathrm{V_{tp}}\right|)^2}$

*PMOS Linear and NMOS Saturation*

- $r_{DSN} = \frac{2(V_{DD}-\mathrm{V_O})}{K_n(V_{DD}-\mathrm{V_O}-V_{tn})^2}$
- $r_{DSP} = \frac{2}{K_p[2(V_{DD}-\left|\mathrm{V_{tp}}\right|)-(V_{DD}-\mathrm{V_O})]}$

*PMOS Linear and NMOS OFF*

- $r_{DSN} = \infty$
- $r_{DSP} = \frac{2}{K_p[2(V_{DD}-\left|\mathrm{V_{tp}}\right|)-(V_{DD}-\mathrm{V_O})]}$

**VI. CALCULATIONS**

Folded cascode amplifier:

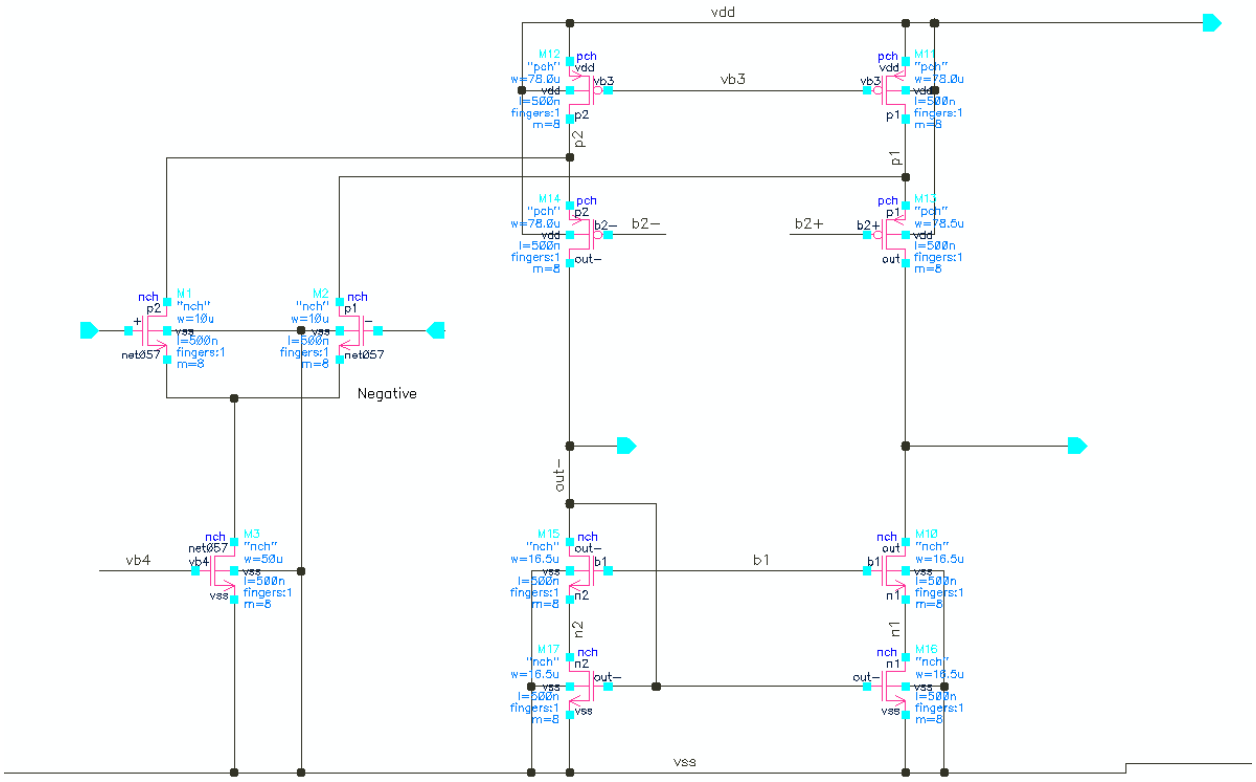


*Fig.13. Folded cascode*

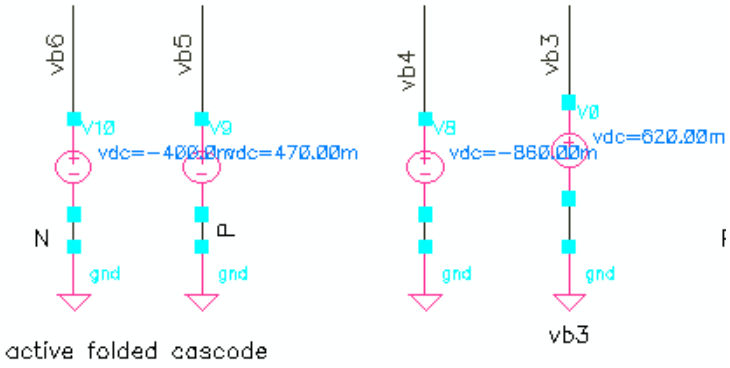


*Fig.14. Folded cascode bias*

Table 1: Calculation of folded cascode op-amp

| Step | Relationship | Design Equation/Constraint | Comments |
|---|---|---|---|
| 1 | Slew Rate | $I_3 = SR.C_L$ | |
| 2 | Bias currents in output cascodes | $I_{12} = I_{11} = 1.2 - 1.5I_3$ | Avoid zero current in cascodes |
| 3 | Maximum output voltage, $v_{out}$(max) | $S_{11}=\frac{2I_{11}}{K_pV_{SD11}^2}$ $S_{13}=\frac{2I_{13}}{K_pV_{SD13}^2}$ $S_{11} = S_{12}$ $S_{13} = S_{14}$ | $V_{SD11}(sat) = V_{SD13}(sat) = 0.5[V_{DD} - v_{out}(max)]$ |
| 4 | Minimum output voltage, $v_{out}$(min) | $S_{16}=\frac{2I_{16}}{K_nV_{SD16}^2}$ $S_{10}=\frac{2I_{10}}{K_nV_{SD10}^2}$ $S_{16} = S_{17}$ $S_{10} = S_{15}$ | $V_{SD10}(sat) = V_{SD16}(sat) = 0.5[v_{out}(min) - \lvert V_{SS}\rvert]$ |
| 5 | GB=$\frac{gm_1}{C_L}$ | $S_1 = S_2 = \frac{gm_1^2}{K_nI_3} = \frac{GB^2C_L^2}{K_nI_3}$ | |
| 6 | Minimum input CM | $S_3 = \frac{2I_3}{K_n(V_{in}(\min) - V_{SS} - \sqrt{\frac{I_3}{K_nS_1}} - V_{T1})^2}$ | |
| 7 | Maximum input CM | $S_{11} = S_{12} = \frac{2I_{12}}{K_p(V_{DD} - V_{in}(\max) + V_{T1})^2}$ | $S_{11}$ and $S_{12}$must meet or exceed value in step 3. |
| 8 | Differential Voltage Gain | $\frac{v_{out}}{v_{in}} = (\frac{gm_1}{2} + \frac{gm_2}{2(1+k)})R_{out}$ $= (\frac{2+k}{2+2k})gm_{1,2}R_{out}$ | k = $\frac{R_{II}\,(g_{ds2} + g_{ds12})}{gm_{13}\,r_{ds13}}$ |
| 9 | Power dissipation | $P_{diss} = (V_{DD} - V_{SS})(I_3 + I_{17} + I_{16})$ | |

- $R_{II} = gm_{10}\, r_{ds10}\, r_{ds16}$
- $R_{out} = R_{II} \,||\, gm_{13}r_{ds13}\,(r_{ds11} + r_{ds1})$
- $V_{DD} = 1.5\,V, V_{SS} = -1.5\,V$

- Parameters for 0.35 µm model:
  $K_p = 30\mu A/V^2, V_{Thp} = 0.766\,V, \Lambda_p = 0.01\,V^{-1}$
  $K_n = 150\mu A/V^2, V_{Thn} = 0.546\,V, \Lambda_n = 0.01\,V^{-1}$

- Overdrive voltage $V_{GS} - V_{Th} = V_{DS}(sat) = V_{OV}$
  let $V_{DS1,2}(sat) = 0.15$ V
  $V_{DS3}(sat) = 0.104$ V
  $V_{DS11,12}(sat) = 0.184$ V
  $V_{DS13,14}(sat) = 0.144$ V
  $V_{DS10,15}(sat) = 0.146\,V$
  $V_{DS16,17}(sat) = 0.146$ V
- $v_{out}(max) = V_{DD} - |V_{DS11}(sat)| - |V_{DS13}(sat)|$ = 1.5 – 0.184 – 0.144 = 1.172 V
- $v_{out}(min) = V_{SS} - V_{DS10}(sat) - V_{DS16}(sat)$ = -1.5 + 0.146 + 0.146 = -1.208 V
- $V_{SD11}(sat) = V_{SD13}(sat) = 0.5[V_{DD} - v_{out}(max)]$

- Input Common Mode range,
  $v_{in}(max) = V_{DD} - |V_{DS11}(sat)| + V_{Tn}$ = 1.5 – 0.184 + 0.546 = 1.862 V
  $v_{in}(min) = V_{SS} + V_{DS3}(sat) + V_{DS1}(sat) + V_{Tn}$ = -1.5 + 0.104 + 0.15 = -1.245 V

**Step 1:**

Slew rate, SR > 250 V/µs, let SR = 700 V/µs , Load capacitance $C_L$= 1pF

$I_3 = SR.C_L = 700 \times 10^6.10^{-12} = 700\mu A$

**Step 2:**

$I_{12} = I_{11} = 1.5I_3 = 1.2 \times\ 700\mu A = 840\mu A$

**Step 3:**

$V_{SD11}(sat) = V_{SD13}(sat) = 0.5[V_{DD} - v_{out}(max)] = 0.5[1.5 - v_{out}(max)] = 0.5[1.5 - 1.172] = 0.164$ V

$S_{11} = S_{12} = \frac{2I_{11}}{K_p V_{SD11}^2} = \frac{2 \times 840 \times 10^{-6}}{30 \times 10^{-6} \times 0.164^2} = 1285$

Currents in $M_{14} = M_{13} = I_{12} - I_2 = 840 - 350 = 490\mu A$

$S_{14} = S_{13} = \frac{2I_{13}}{K_p V_{SD13}^2} = \frac{2 \times 490 \times 10^{-6}}{30 \times 10^{-6} \times 0.164^2} = 1133$

Assuming worst case currents in $M_{14} = M_{13} = 840\mu A$

$S_{14} = S_{13} = \frac{2I_{13}}{K_p V_{SD13}^2} = \frac{2 \times 840 \times 10^{-6}}{30 \times 10^{-6} \times 0.164^2} = 1285$

**Step 4:**

$V_{SD10}(sat) = V_{SD16}(sat) = 0.5[v_{out}(min) - V_{SS}] = 0.5[v_{out}(min) - 1.5] = 0.5[-1.208 + 1.5] = 0.146$ V

$S_{10} = S_{15} = S_{16} = S_{17} = \frac{2I_{16}}{K_n V_{SD16}^2} = \frac{2 \times 840 \times 10^{-6}}{150 \times 10^{-6} \times 0.146^2} = 325$

**Step 5:**

$S_1 = S_2 = \frac{gm_1^2}{K_n I_3} = \frac{GB^2 C_L^2}{K_n I_3} = \frac{(2 \times \pi \times 170 \times 10^6 \times 10^{-12})^2}{150 \times 10^{-6} \times 700 \times 10^{-6}} = 180$

**Step 6:**

$S_3 = \frac{2I_3}{K_n(V_{in}(\min) - V_{SS} - \sqrt{\frac{I_3}{K_n S_1}} - V_{T1})^2} = \frac{2 \times 700 \times 10^{-6}}{150 \times 10^{-6}(-1.245 + 1.5 - \sqrt{\frac{700 \times 10^{-6}}{150 \times 10^{-6} \times 11}} - 0.546)^2} = 820$

**Step 7:**

Checking the values of $S_{11}, S_{12}$ are large enough to satisfy the maximum input common mode voltage.

$S_{11} = S_{12} \geq \frac{2I_{12}}{K_p(V_{DD} - V_{in}(\max) + V_{T1})^2} = \frac{2 \times 840 \times 10^{-6}}{30 \times 10^{-6}(1.5 - 1.862 + 0.546)^2} = 1168$

Which is less than 1285.

**Step 8:**

- $gm_{11,12} = \sqrt{2I_{11,12}K_pS_{11,12}} = \sqrt{2 \times 840 \times 10^{-6} \times 30 \times 10^{-6} \times 1285}$= 8047.6 µS
  $g_{ds11,12} = \frac{1}{r_{ds11,12}} = \Lambda_p \times I_{11,12} = 0.01 \times 840 \times 10^{-6}$= 8.4 × $10^{-6}$ S
- $gm_{13,14} = \sqrt{2I_{13,14}K_pS_{13,14}} = \sqrt{2 \times 490 \times 10^{-6} \times 30 \times 10^{-6} \times 1285} = 6146.46$ µS
  $g_{ds13,14} = \frac{1}{r_{ds13,14}} = \Lambda_p \times I_{13,14} = 0.01 \times 490 \times 10^{-6}$= 4.9 × $10^{-6}$ S
- $gm_{10,15,16,17} = \sqrt{2I_{10,15,16,17}K_pS_{10,15,16,17}} =$
  $\sqrt{2 \times 490 \times 10^{-6} \times 150 \times 10^{-6} \times 325}$=6911.946 µS
  $g_{ds10,15,16,17} = \frac{1}{r_{ds10,15,16,17}} = \Lambda_n \times I_{10,15,16,17} = 0.01 \times 490 \times 10^{-6} = 4.9 \times 10^{-6}$ S
- $gm_{1,2} = \sqrt{2I_{1,2}K_pS_{1,2}} = \sqrt{2 \times 350 \times 10^{-6} \times 150 \times 10^{-6} \times 180} = 434.41$µS
  $g_{ds1,2} = \frac{1}{r_{ds1,2}} = \Lambda_n \times I_{1,2} = 0.01 \times 350 \times 10^{-6}$=3.50 × $10^{-6}$S
- $R_{II} = gm_{10}\, r_{ds10}\, r_{ds16}$ = (6911.9 µS) $\frac{1}{4.9 \times 10^{-6}\ \text{S}} \frac{1}{4.9 \times 10^{-6}\ \text{S}}$ = 28.87 MΩ
- $R_{out} = R_{II} \,||\, gm_{13} r_{ds13}\, (r_{ds11} + r_{ds1})$ =
  (28.87 MΩ) ||(6146.46 µS) $\frac{1}{4.9 \times 10^{-6}\ \text{S}} \left(\frac{1}{8.4 \times 10^{-6}\ \text{S}} + \frac{1}{3.5 \times 10^{-6}\ \text{S}}\right) = 18.70$ MΩ
- k = $\frac{R_{II}\,(g_{ds2} + g_{ds12})}{gm_{13}\, r_{ds13}}$ = 0.73
- $\frac{v_{out}}{v_{in}} = \left(\frac{2+k}{2+2k}\right) gm_{1,2} R_{out}$
  **=2138=66.6dB**

**Step 9:**

$P_{diss} = (V_{DD} - V_{SS})(I_3 + I_{17} + I_{16})$

= (3)(700µ +490µ+490µ)=**5.04 mW**

**VII. SIMULATION CIRCUIT & RESULTS**

*To achieve the device sizes as per the calculations, a multiplier of 8(m=8) has been used in the simulation circuit.*

**Folded cascode error amplifier:**

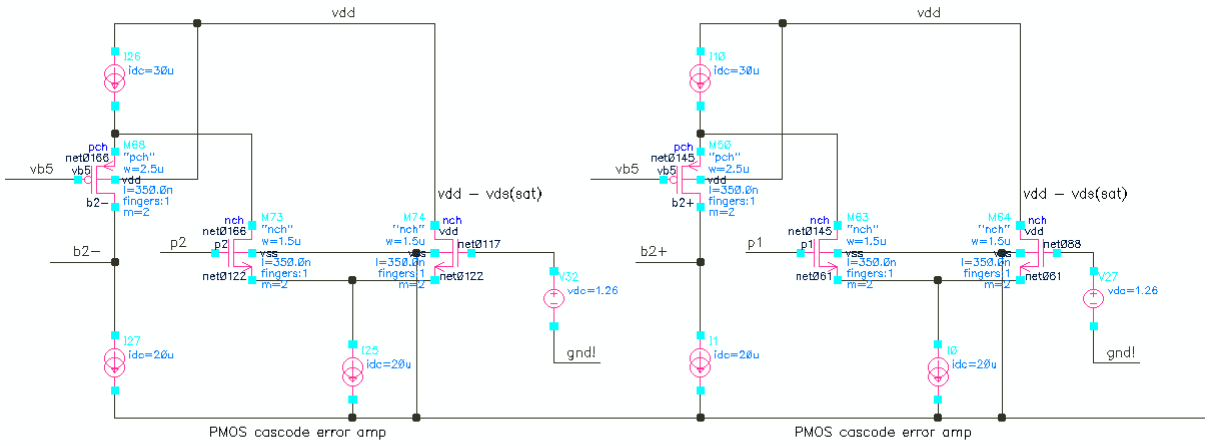


*Fig.15. PMOS cascode error amplifier*

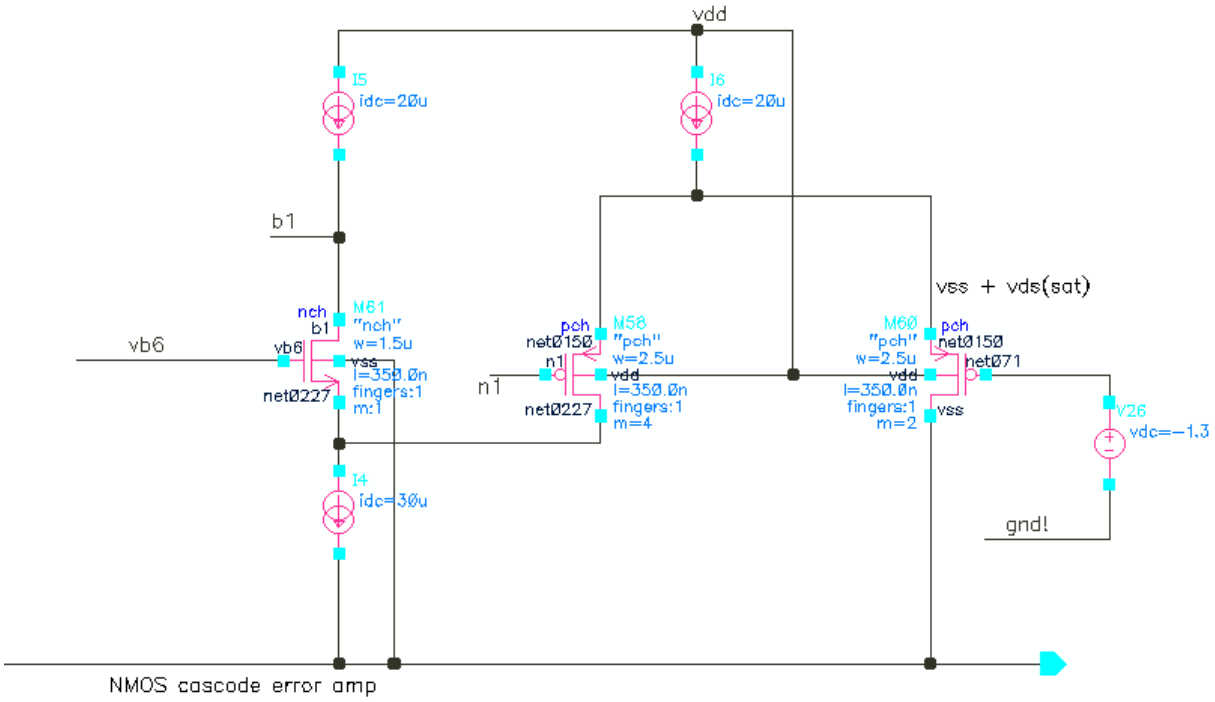


*Fig.16. NMOS cascode error amplifier*

## Folded cascode AC Analysis:

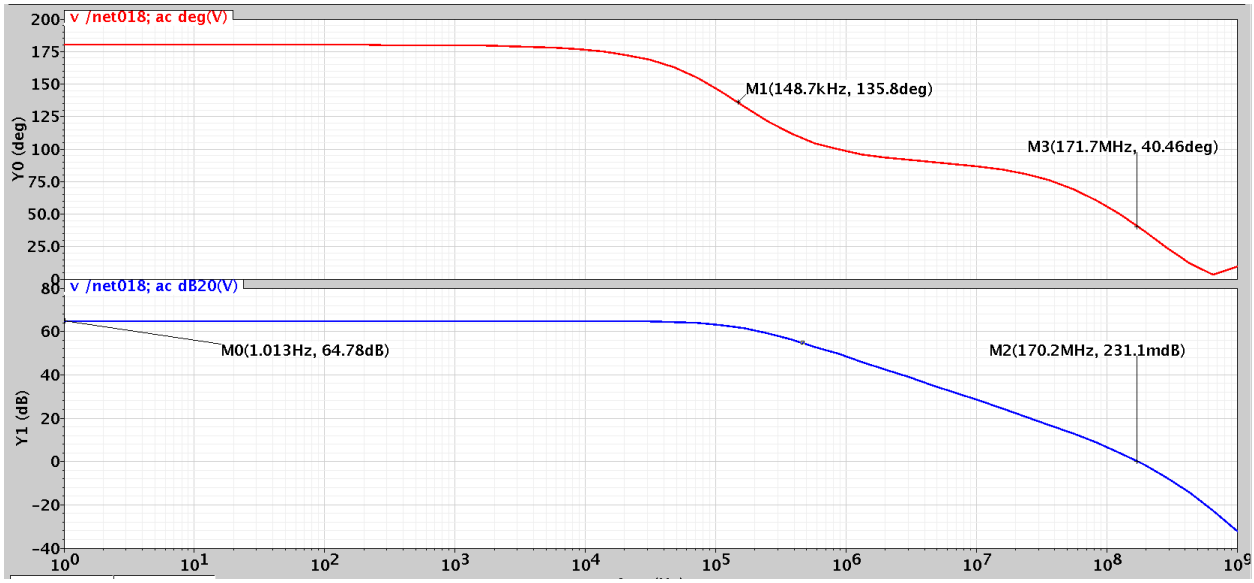


*Fig.17. Folded cascode AC analysis*

## Folded cascode Transient Analysis:

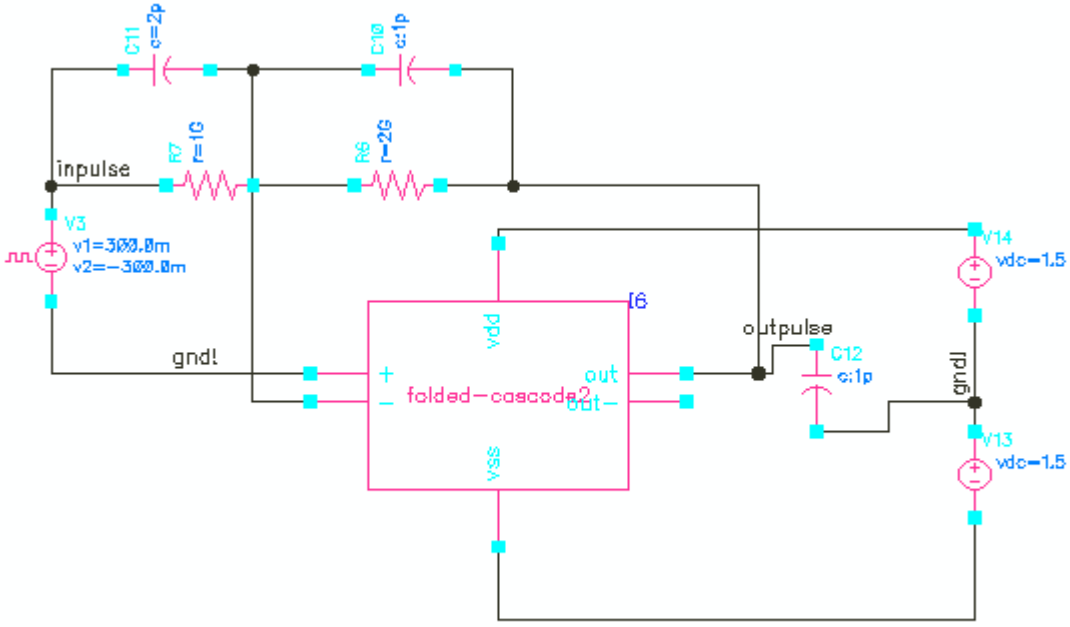


*Fig.18. Folded cascode transient test block*

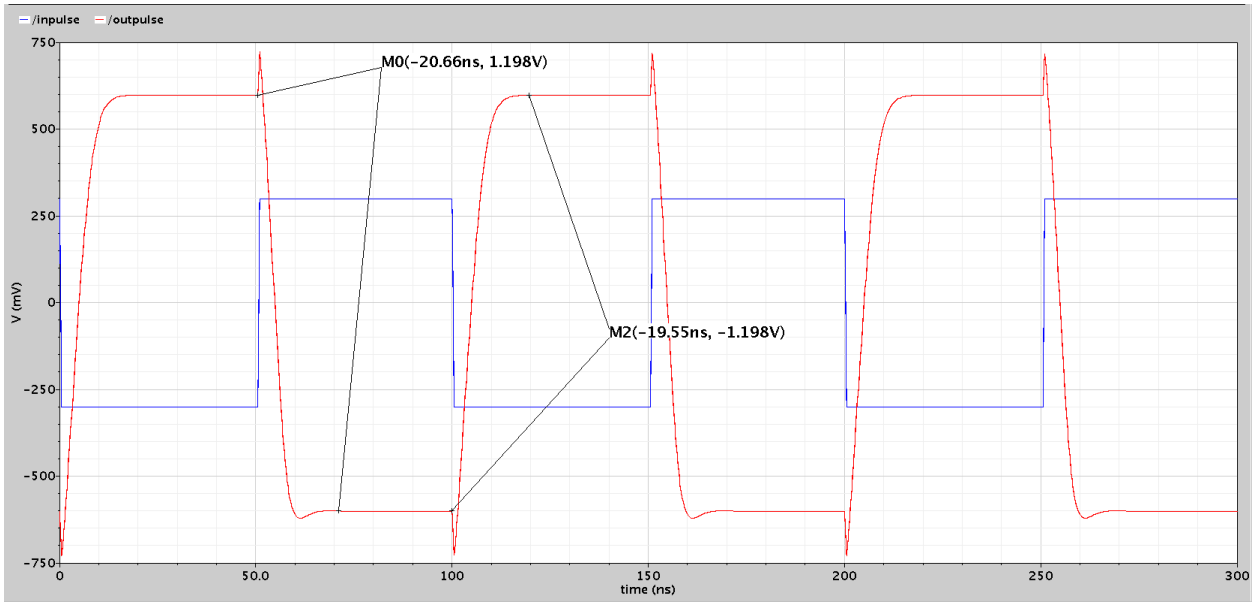


*Fig.19. Folded cascode: transient analysis*

## Transmission Gate:

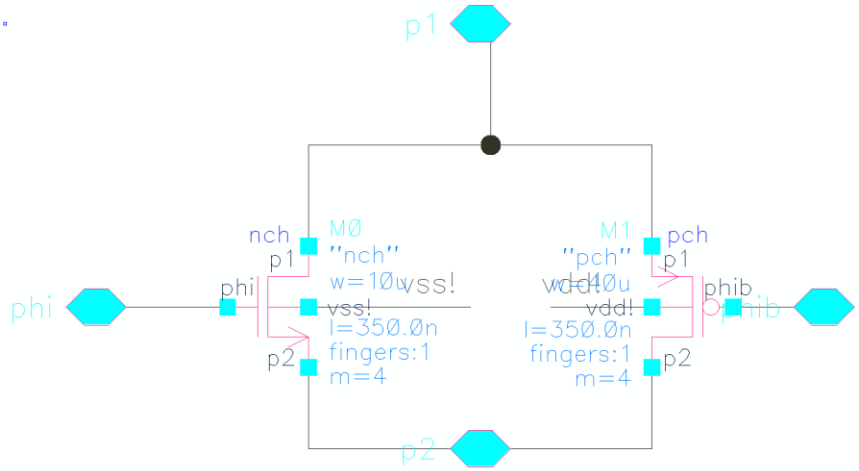


*Fig.20. Transmission gate block*

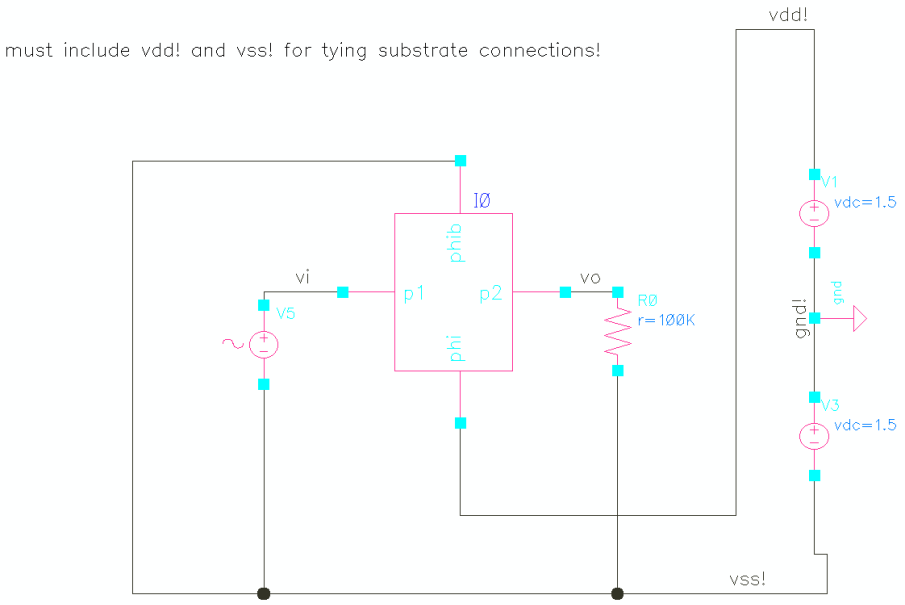


*Fig.21. Transmission gate test block*

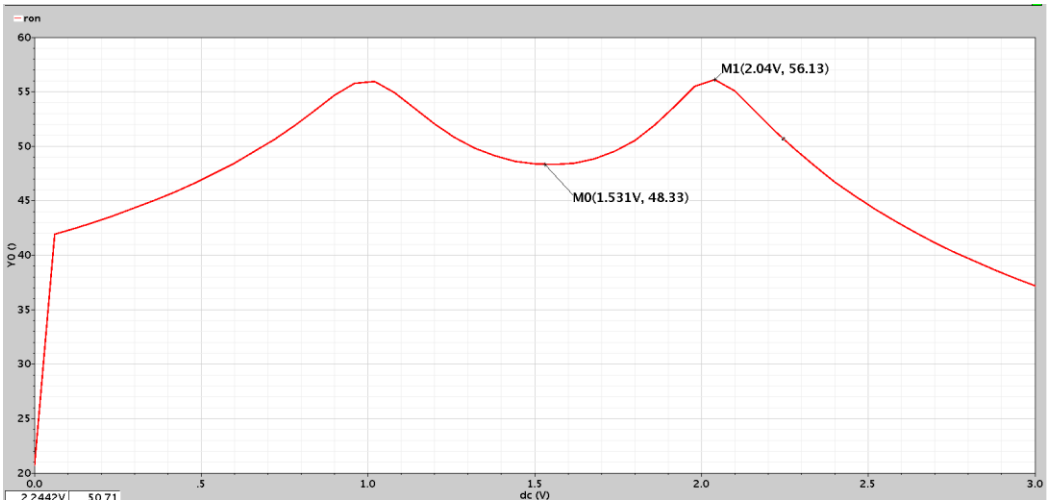


*Fig.22. On Resistance, $R_{on}$*

$$R_{on} = \frac{v_o - v_i}{i_{p1}} = 0.03\ \Omega$$

**Overall circuit:**

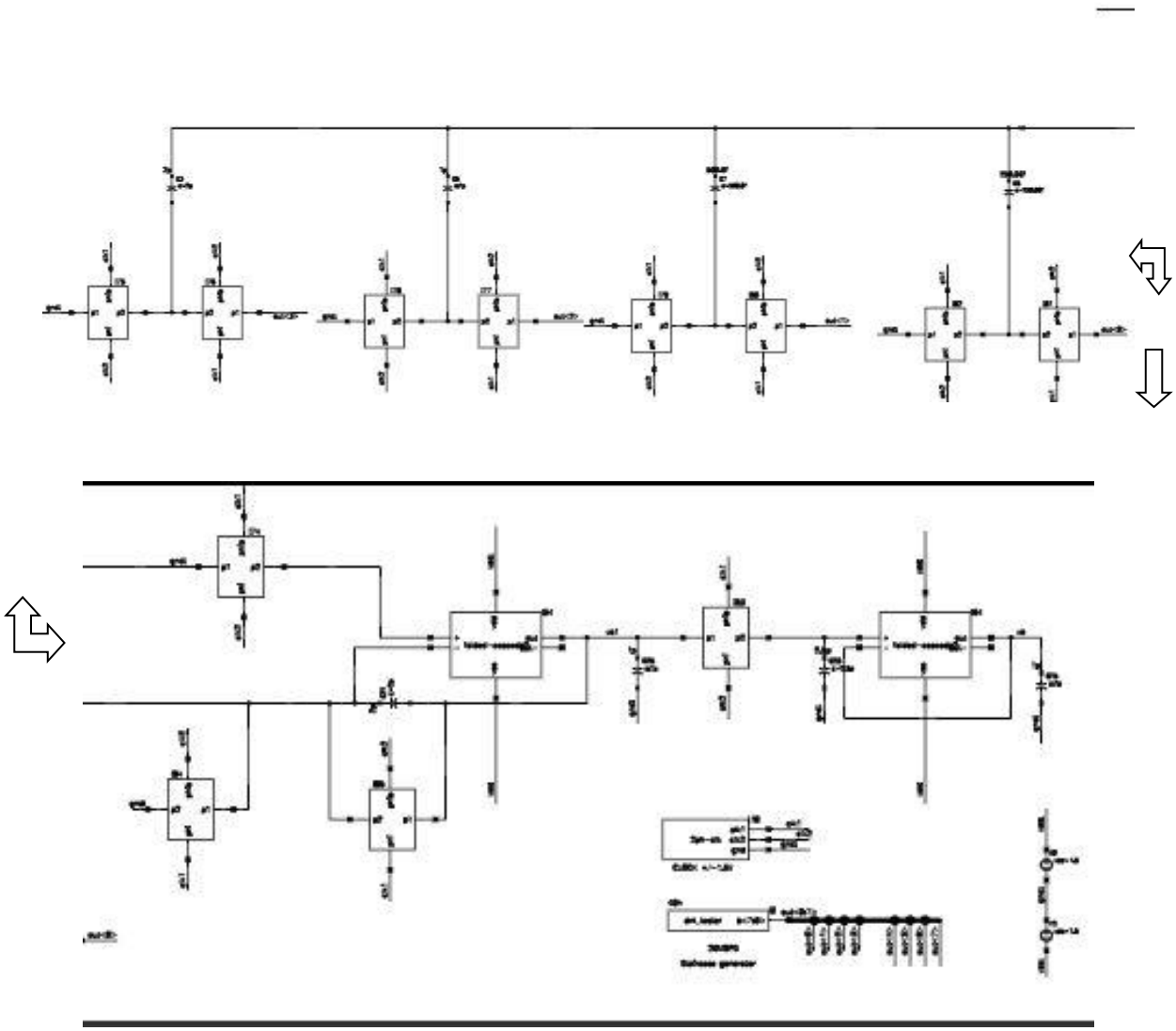

*Fig.23. Overall circuit*

## Test of Overall Circuit:

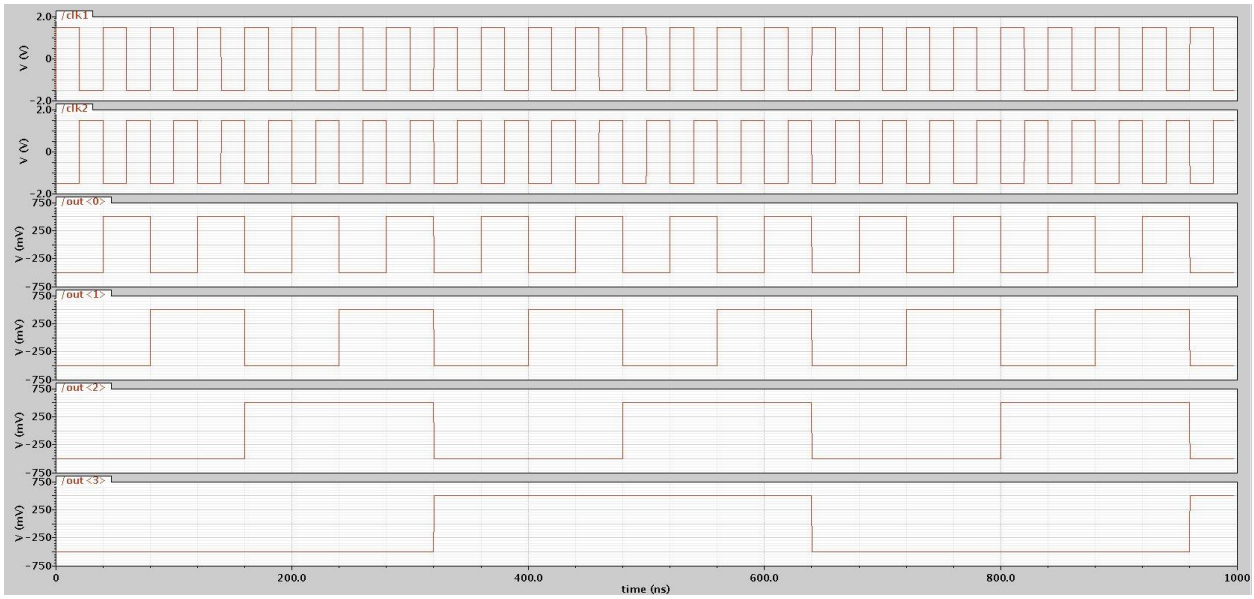


*Fig.24. Input: Data lines*

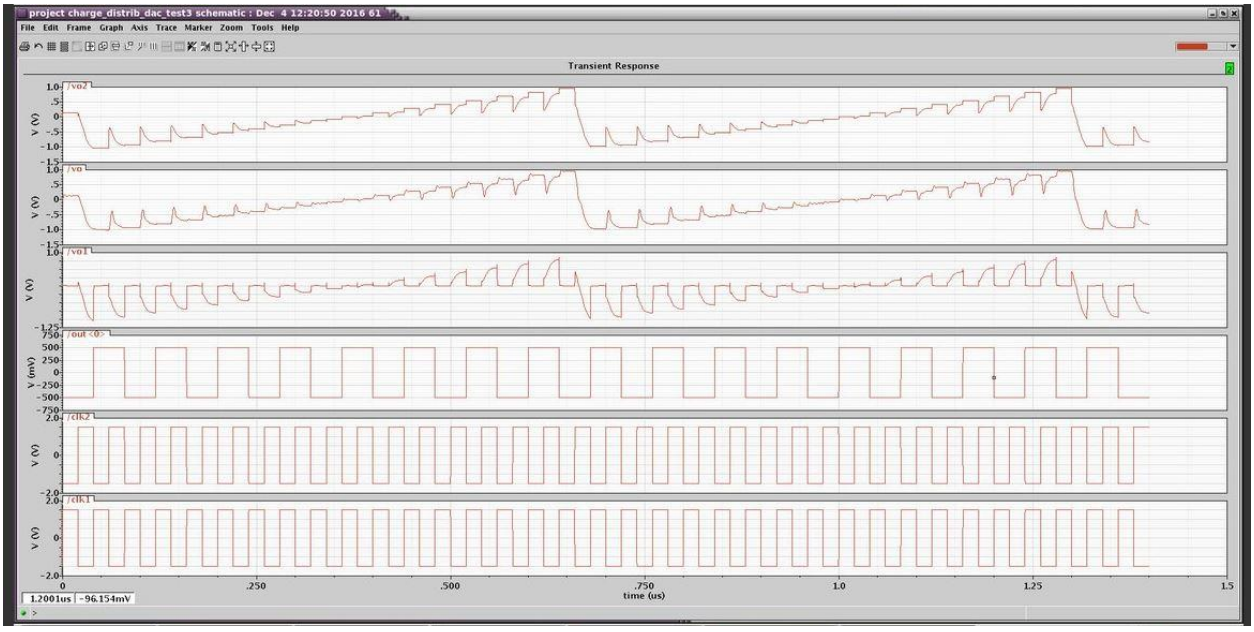


*Fig.25. Output*

## DNL and INL Testing:

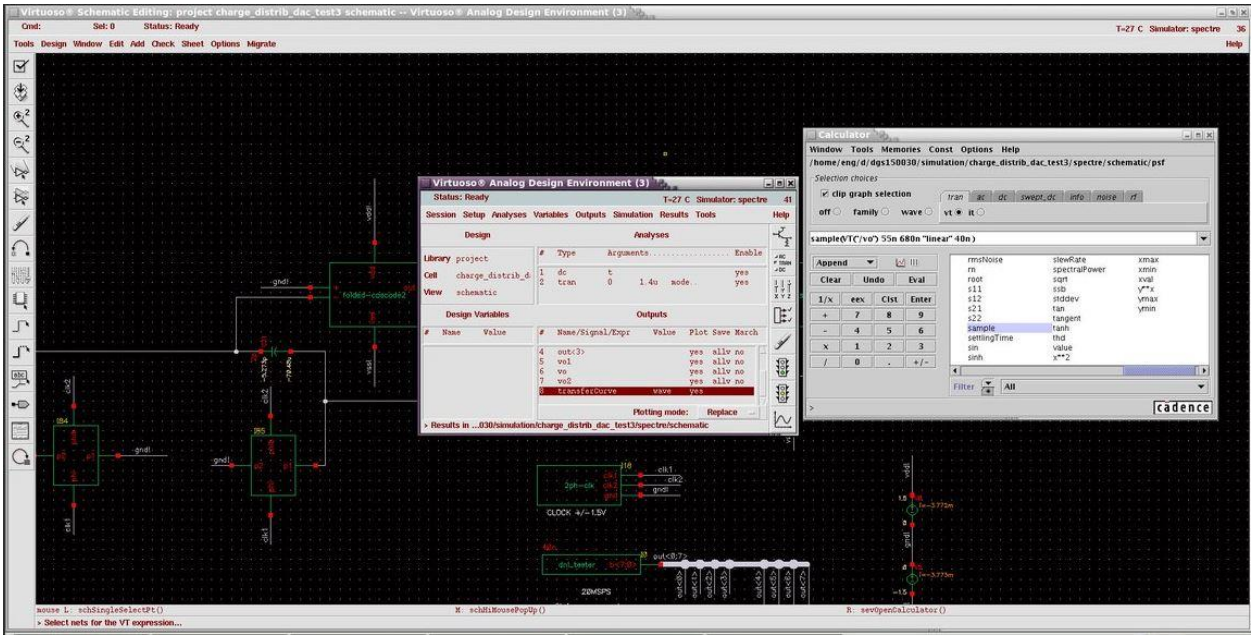


*Fig.26. INL curve sample function*

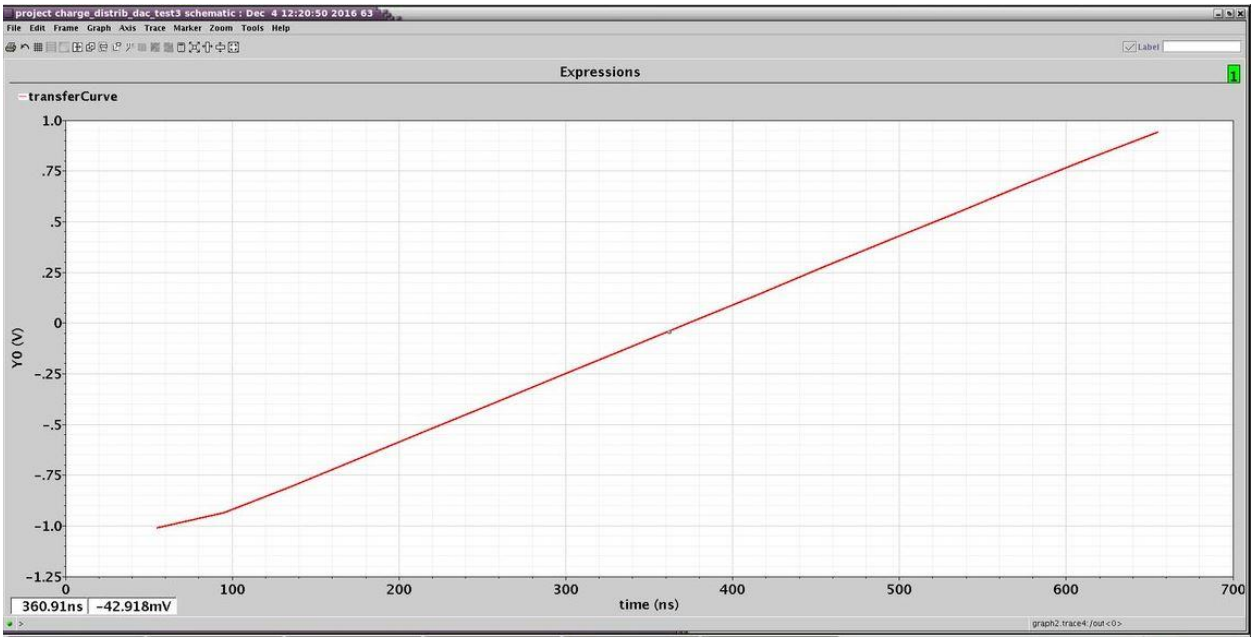


*Fig.27. INL curve*

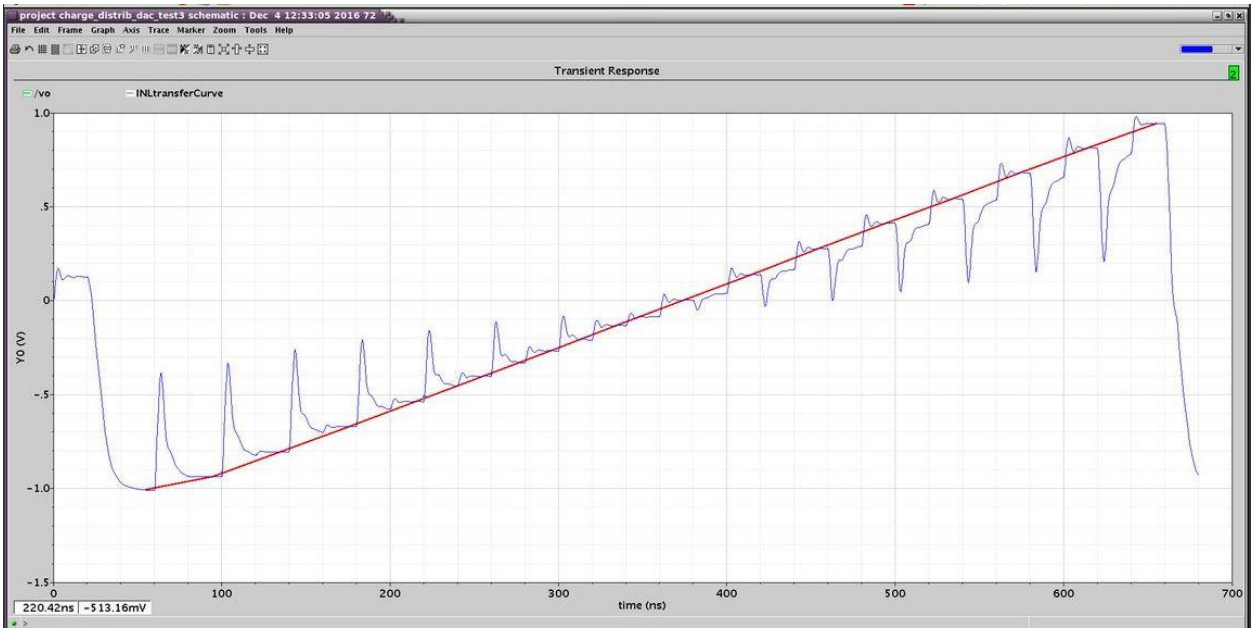


*Fig.28. INL transient response transfer curve*

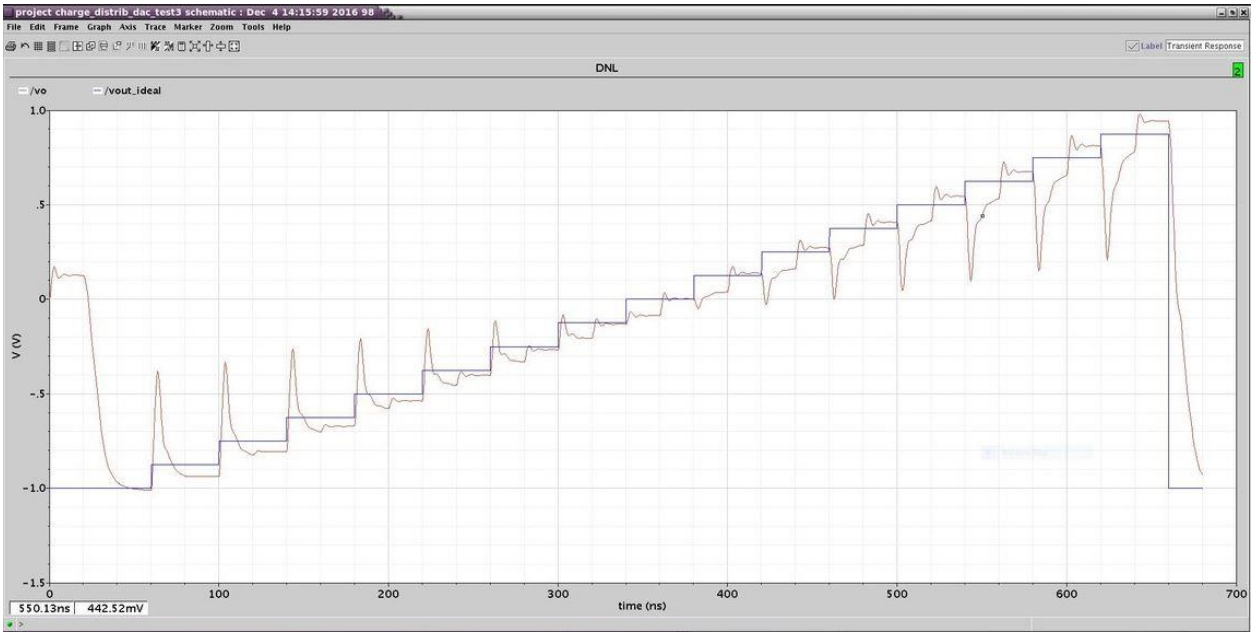


*Fig.29.DNL curve*

**VIII. RESULTS COMPARSION**

| S.NO. | Specifications | Expected | Achieved |
|---|---|---|---|
| 1. | Supple voltage | +/- 1.5 V | +/- 1.5 V |
| 2. | Load capacitance | 1 pF | 1 pF |
| 3. | Sampling rate | 20 MSPS | 20 MSPS |
| 4. | Differential nonlinearity (DNL) | +/- 0.5*LSB | 1 LSB |
| 5. | Integral nonlinearity (INL) | +/- 1*LSB | 1LSB |
| 6. | GBW | 170 MHz | 171.7 MHz |
| 7. | Closed loop gain | 2x | 2x |
| 8. | Settling time | 15 ns | 20 ns |
| 9. | Settling error | -60 dB | -55.38 dB |
| 10. | Load capacitance | 1pF | 1pF |
| 11. | Output swing (peak to peak) | 1.3 V | 2.3 V |
| 12. | Slew rate | >250 V/µs | 700 V/µs |

**IX. FINAL RESULTS**

Hence, the circuit is designed and tested for 20 MSPS 4-bit Charge Redistribution with following specifications:

| | |
|---|---|
| Supple voltage | +/- 1.5 V |
| Load capacitance | 1 pF |
| Sampling rate | 20 MSPS |
| Differential nonlinearity (DNL) | 1 LSB |
| Integral nonlinearity (INL) | 1LSB |
| GBW | 170 MHz |
| Closed loop gain | 2x |
| Settling time | 20 ns |
| Settling error | -55.38 dB |
| Load capacitance | 1pF |
| Output swing (peak to peak) | 2.3 V |
| Slew rate | 700 V/µs |

**X. CONCLUSION**

The DAC was implemented and tested for above mentioned conditions.

1. The specification were limited by the technology, i.e. with 0.35 µm CMOS technology working with supply of +-0.9 V and achieving GBW>200MHz and $A_v$ >50 dB is difficult.
2. Parasitic were generated due to large size of transistors, which affected the high frequency operation.
3. A careful design is required to achieve high speed and high gain for a data converter.
4. Capacitor DAC is more power efficient compared to R-2R DAC which consumes twice the current for the same number of nits due to resistor network.

## XI. REFERENCES


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