

29.1 A 5mW CT $\Delta\Sigma$ ADC with Embedded 2nd-Order Active Filter and VGA Achieving 82dB DR in 2MHz BW

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Conventional continuous-time delta-sigma modulator (CTDSM) architectures do not allow independent control of the shape and bandwidth of the signal transfer function (STF), since the STF is simply a by-product of NTF synthesis. This is particularly troublesome when the input to the CTDSM consists of large out-of-band interferers; handling them without saturating the quantizer needs larger in-band DR, leading to increased power dissipation. A solution to this problem is to use a filter upfront to attenuate interferers. Alternatively [1], the filter can be moved into the CTDSM loop. In [1], a 1st-order RC filter was used to “tame” the STF peak of a cascade of integrators with feedforward summation (CIFF) DSM. Apart from the limited selectivity offered by a 1st-order filter, an active feedback path was necessary to stabilize the loop. The CTDSM in our work obtains an STF with a sharper transition band and a lower cutoff frequency (normalized to the desired signal bandwidth) compared to [1], with the aim of more effectively attenuating close-in interferers. This is realized by embedding a 2nd-order active filter into the CTDSM. We show that this has the same functionality as the filter upfront, but achieves better linearity (for the same noise and power dissipation) when compared to the filter-CTDSM cascade. Further, no extra active circuitry is necessary to stabilize the loop. Measurements of a CTDSM (signal BW=2MHz), with a built-in VGA (0 to 18dB) and a 2nd-order Butterworth filter (4MHz cutoff), show that the out-of-band IIP3 improves by about 10dB when compared to the CTDSM with the filter placed upfront. The filtering CTDSM+VGA, which uses a single-bit quantizer and a 4-tap FIR DAC, achieves a DR of 92dB in a 2MHz BW while consuming 5mW in a 0.13μm CMOS process. The peak instantaneous DR/SNR/SNDR are 82/80.5/74.5dB. With the VGA, the DR is 92dB.

A 1-bit quantizer necessitates a 4th-order NTF and OSR=64 ($f_s=256\text{MHz}$) to achieve the desired signal-to-quantization-noise ratio (SQNR). The CIFF-B architecture (Fig. 29.1.1(a)) is chosen as a prototype, as it combines the best features of the CIFF and cascade of integrators with feedback (CIFB) loops [2]. The STF rolls off as $1/s^3$ at high frequencies but peaks outside the signal band, which is problematic when there are interferers, due to the following. The maximum stable amplitude of the single-bit CTDSM at frequency f_{in} is $\approx 0.7V_{FS}/\text{STF}(f_{in})$, where V_{FS} is the full scale. A 6dB STF peak restricts the CTDSM input to $(1/2)0.7V_{FS}$, necessitating a 6dB smaller in-band noise, thereby increasing power dissipation.

A way of addressing the STF peak in the 4th-order CIFF-B CTDSM is illustrated with the help of the normalized modulator (1Hz sampling rate) of Fig. 29.1.1(a). The upfront 2nd-order low-pass filter, H_1 , attenuates interferers and, as seen in Fig. 29.1.1(c), the effective STF of the H_1 -CTDSM cascade is flat and has 5th-order roll off at high frequencies. Since the BW of H_1 is low, close-in interferers can be effectively attenuated, relaxing in-band SNR requirements. However, cascading H_1 with the CTDSM is not power efficient as *both* the filter and the CTDSM contribute to noise and distortion of the system. The technique proposed in this work moves the filter beyond the first integrator of the CTDSM as shown in Fig. 29.1.1(b). Comparing Fig. 29.1.1(a) and (b), we see that the transfer function from u to y is the same. Embedding H_1 into the CTDSM alters the NTF, necessitating a compensation path with gain $a_4(1-H_1)/s$ to restore it. Assuming the DC gain of $H_1=1$, this path has a zero at DC, which cancels the integrator pole. Fortunately, this can be realized without extra hardware by injecting v into the second integrator of the filter. This way, the gain from v to y is the same in Fig. 29.1.1(a) and (b), rendering the systems equivalent. However, the filter's noise and distortion are reduced by the gain of the first integrator when referred to the CTDSM input, thus the filter can be impedance-scaled, saving power. When compared to the H_1 -CTDSM cascade, the linearity of the filtering-CTDSM of Fig. 29.1.1(b) is enhanced thanks to overall feedback. While this compensation technique is illustrated with a 2nd-order filter, the idea can be extended to LPFs of arbitrary order (which can be realized as a cascade of biquads).

Figure 29.1.2 shows the single-ended diagram of the CIFF-B CTDSM with the 2nd-order embedded filter drawn in blue. Active-RC integrators are used for better linearity and wide-swing. The high-speed path around the quantizer is through

I₁. The RZ DAC₁ compensates for excess loop delay (~600ps). DAC₄ and DAC₃ are resistive 4-tap FIR DACs, implemented using semi-digital techniques. R₃₁ implements the feedforward path across I₃. Optimized tap-weights for DAC₄ reduce jitter noise by 15dB when compared to a 1-bit CTDSM without an FIR DAC. Integrator I₄ is cascaded with a 2nd-order Butterworth filter H₁ ($f_{3db}=4\text{MHz}$). The FIR DAC₃ feeding into the 2nd integrator (I₂) of H₁ compensates the loop for the effect of H₁, restoring the NTF. The delay introduced by F(z) in DAC₄ is compensated by FIR DAC₂ with filter F_c(z). The OTAs are 2-stage designs with ac-coupled feedforward compensation [4]. Capacitors are implemented as digitally programmable banks to tune out time constant variations. Varying R_{in} implements the VGA; when R_{in} is reduced to increase gain, the bias current in the 2nd stage of I₄ is increased to maintain loop gain.

Intuition for power reduction resulting from embedding the filter into the CTDSM is given using Fig. 29.1.3. Part (a) shows the filter-CTDSM cascade. Assuming only resistor noise, the inband thermal noise density is $\approx 6R4\text{kT}$. When the filter is embedded (Fig. 29.1.3(b)), the CTDSM input and DAC impedances are doubled, and the filter impedance is increased by $\approx 3\times$. In spite of this, the input noise density is smaller at $\approx 5R4\text{kT}$. Thus, the power in OTAs \hat{A}_1 , \hat{A}_2 and \hat{A}_3 can be reduced while achieving similar linearity, since 3rd-order distortion depends on G_{OTA}R (G_{OTA} is the OTA transconductance). In this work, \hat{A}_1 , \hat{A}_2 and \hat{A}_3 are scaled so that they consume 0.65, 0.33 and 0.75 times the currents of A₁, A₂ and A₃, respectively. This way, the G_{OTA}R products for \hat{A}_1 , \hat{A}_2 and \hat{A}_3 are about 2, 1 and 1.5 times the corresponding products for A₁, A₂ and A₃, respectively. Thus, not only is power dissipation lower when the filter is embedded into the CTDSM, linearity is also enhanced with respect to a filter-CTDSM cascade, while achieving similar noise.

Two CTDSMs, one with an embedded filter (called $\Delta\text{-}H_1\text{-}\Sigma$) and another with a filter upfront (called $H_1\text{-}\Delta\Sigma$) are fabricated in a 0.13μm CMOS technology. Figure 29.1.3(c) shows the measured STF and maximum stable amplitude (MSA), which remain almost the same for both designs. The MSA was measured with the VGA gain set to 8. The area and power dissipation of $\Delta\text{-}H_1\text{-}\Sigma$ are 0.33mm² and 5mW (including references and for the highest VGA gain setting), respectively. Thanks to impedance scaling, these are about 25% smaller compared to those of $H_1\text{-}\Delta\Sigma$. Figure 29.1.4 shows the SN(D)R plots of $\Delta\text{-}H_1\text{-}\Sigma$. The peak instantaneous DR is 82dB, which increases to 92dB with the VGA. Figure 29.1.5(a) shows the PSDs at the outputs of $\Delta\text{-}H_1\text{-}\Sigma$ and $H_1\text{-}\Delta\Sigma$ (gain set to 1) when the input consists of two -11dBFS tones at 4.75 and 10.5MHz, and a small desired signal at 2MHz. The filtering effect of the CTDSM is apparent. Further, the IM₃ product at 1MHz is 20dB smaller with the embedded filter, representing an IIP3 improvement of $\approx 10\text{dB}$. Figure 29.1.5(b) shows the PSDs when the interferers are 30 and 61 MHz tones (gain set to 4). IM3 is better in the embedded case by about 13dB (IIP3 better by $\approx 6.5\text{dB}$). Inband IIP3/IIP2 improve by about 3dB/10dB. Figure 29.1.6 compares the performance of this design with other filtering CTDSMs [1]-[3]. Higher power efficiency, linearity and DR are achieved with better close-in filtering. References [5] and [6] are stand-alone CTDSMs (which do not have a desirable STF) implemented in more advanced technologies. The design presented in this work achieves a comparable FoM, especially considering that it is a filter+CTDSM.

Acknowledgments:

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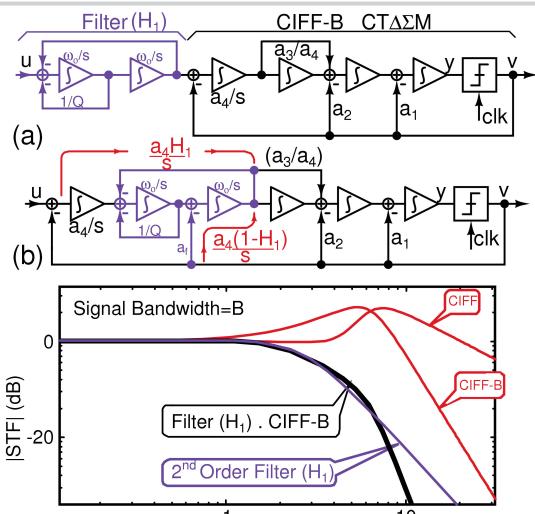


Figure 29.1.1: CIFF-B CTDSMs with (a) upfront filter (b) embedded filter (c) Resulting STF.

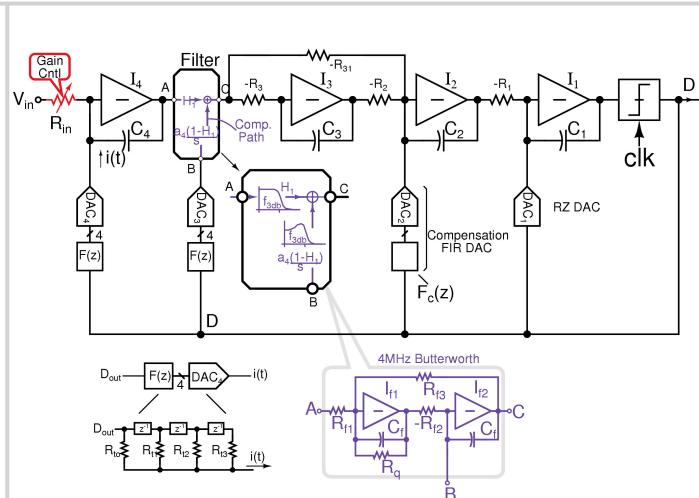


Figure 29.1.2: CTDSM with VGA and embedded second order Butterworth filter.

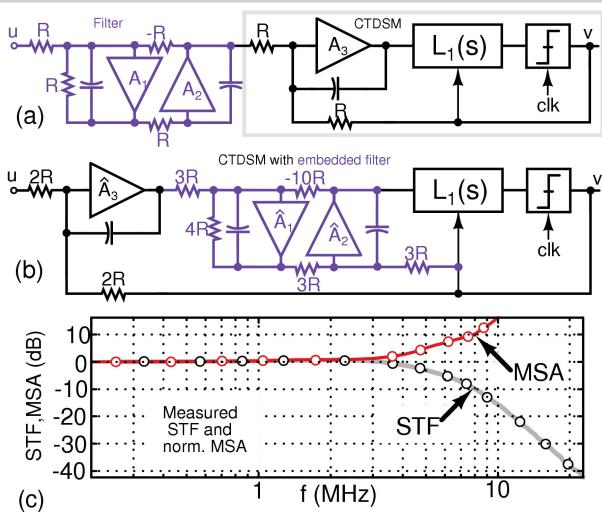


Figure 29.1.3: Impedance levels in a CIFF-B CTDSM with (a) upfront filter (b) embedded filter. (c) Measured STF and maximum stable amplitude (MSA) (normalized to the MSA @ DC).

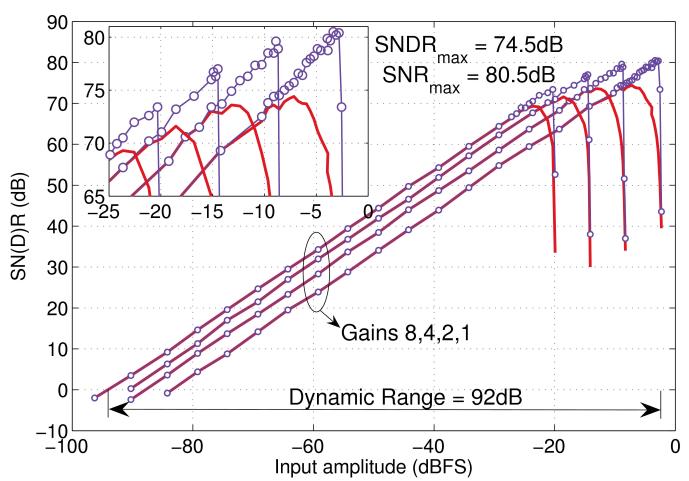


Figure 29.1.4: Measured SN(D)R for various gain settings, for the CTDSM with embedded filter.

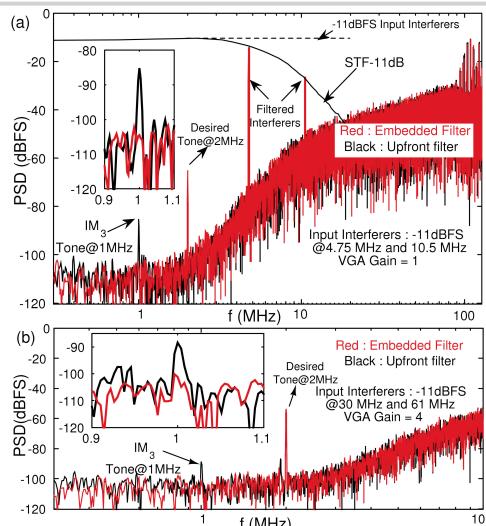


Figure 29.1.5: Response to out-of-band interferers at (a) 4.75 and 10.5 MHz (b) 30 and 61 MHz.

	This work Embedded Filter $\Delta H_1 - \Sigma$	This work Upfront Filter $H_1 - \Delta$	[1]	[2]	[3]	[5]	[6]
BW (MHz)	2	2	1	1	6	1.92	2
fs (MHz)	256	256	64	64	405	245.76	128
DR with VGA (dB)	92	90.8	89	89.5	-	-	-
DR (dB)	82	81	65	71	75.6	83	80
SNRmax (dB)	80.5	79.5	59	68.5	74.6	78	79.1
SNDRmax (dB)	74.4	73.7	59	68.5	74.6	78	79.1
Pd (mW)	5	6.8	2	2.35	54	2.8	4.5
FoM _{SNDR} (fJ/lV)	291	430	1373	540	1025	112	153
DR + 10log ₁₀ (BW/Pd)	168.0	165.7	152.0	157.3	156.1	171.4	166.5
Inband IIP3 / IIP2 (dBFS) 2 MHz input tones	25.5 / 83	22.3 / 73.5	-	-	-	-	-
Out-of-band IIP3 (dBFS) 4.75 & 10.5 MHz tones	35.7	26.2	5.7	-	-	-	-
Out-of-band IIP3 (dBFS) 30 & 61 MHz tones	40.8	33.7	-	-	-	-	-
(Filter 3dB BW)/Signal BW	2	2	3	-	1.43	-	-
Hi freq. roll off (dB/dec)	100	100	40	60	80	40	20
Active area (mm ²)	0.33	0.42	0.14	0.10	0.21	0.09	0.08
Technology (nm)	130	130	180	180	90	40	65
Supply (V)	1.4	1.4	1.8	1.8	2.4/1.4	1.2	-

Figure 29.1.6: Summary and Comparison: [1-3] are filtering ADCs, [5-6] are stand alone CTDSMs.

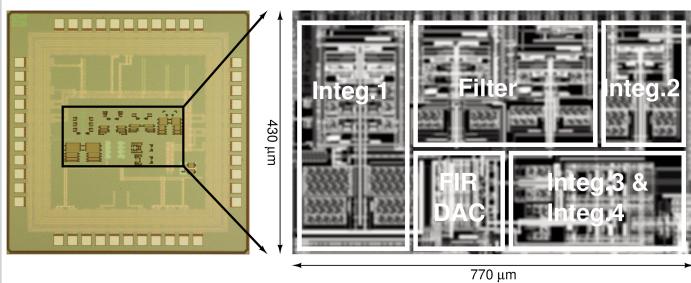


Figure 29.1.7: Die photo of the CTDSM with embedded filter (0.13 μ m CMOS). The active area is 27% smaller than the CTDSM with the filter placed upfront.