

THE UNIVERSITY OF TEXAS AT DALLAS

ERIK JONSSON SCHOOL OF ENGINEERING &

COMPUTER SCIENCE

DATA CONVETRERS

(EECT 7327 - SPRING 2018)

HOMEWORK-3

REPORT SUBMITTED BY:

**DEVANG SANKHALA
BHARGAV PATEL**

**Net-id: dgs150030
Net-id: bbp160230**

Comparator Circuits:

1. Comparator-1 [Ref :[1]]:

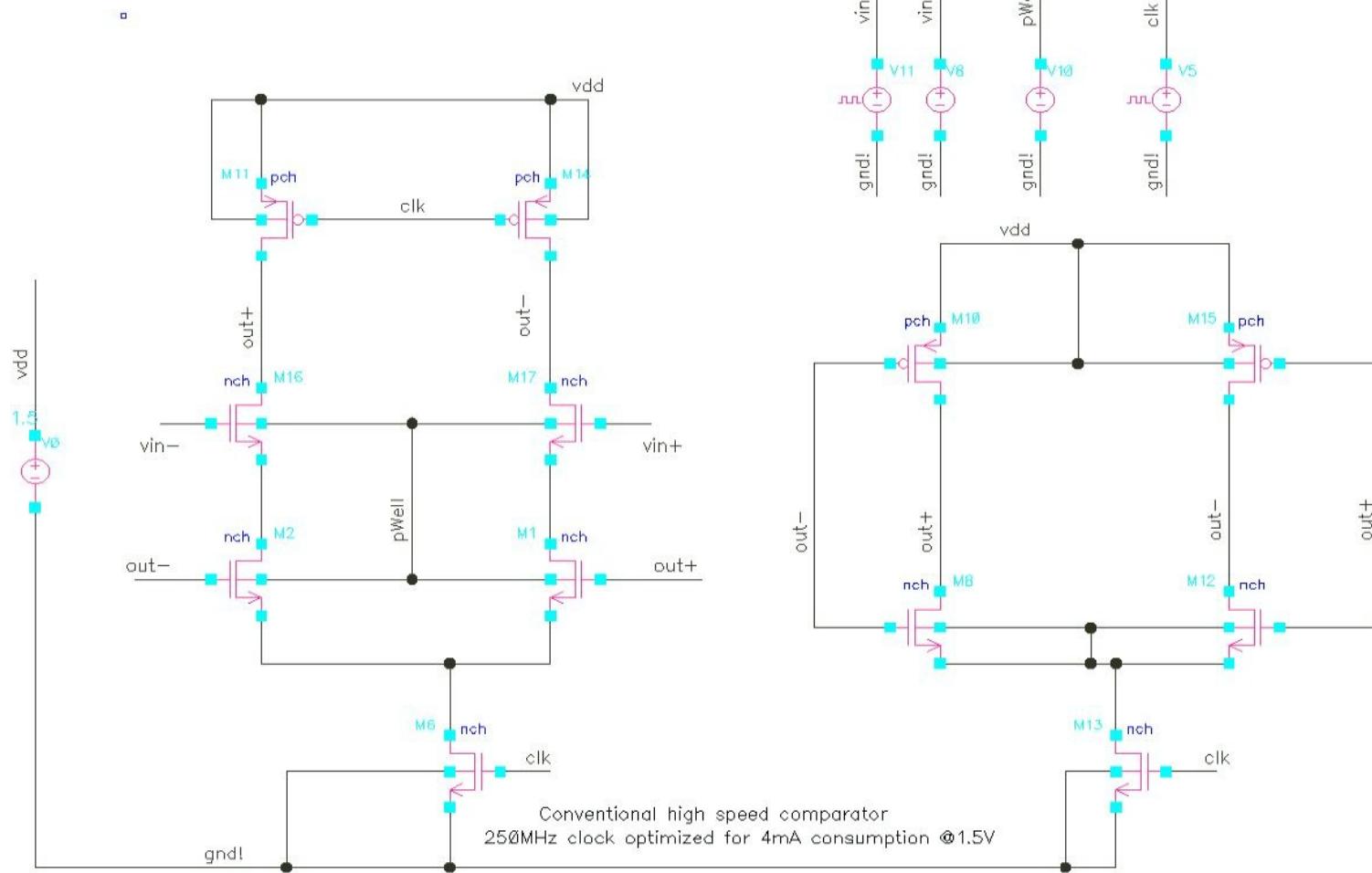


Fig.1 High Speed Comparator (250MHz) with Conventional cross-coupled Latch (Comparator-1)

- The dynamic latch comparator shown in figure 1 is most widely used because it has many advantages such as high-speed, zero static-power consumption, high input-impedance and full-swing output.
- During the pre-charge phase (Clock is low) both the output nodes out+ and out- are charged to power supply voltage (1.5 V) and during the evaluation phase(Clock is High) the output of the comparator depends on the differential input (Vin+ and Vin-). Comparator consists of a latch followed by a pre-amplifier.

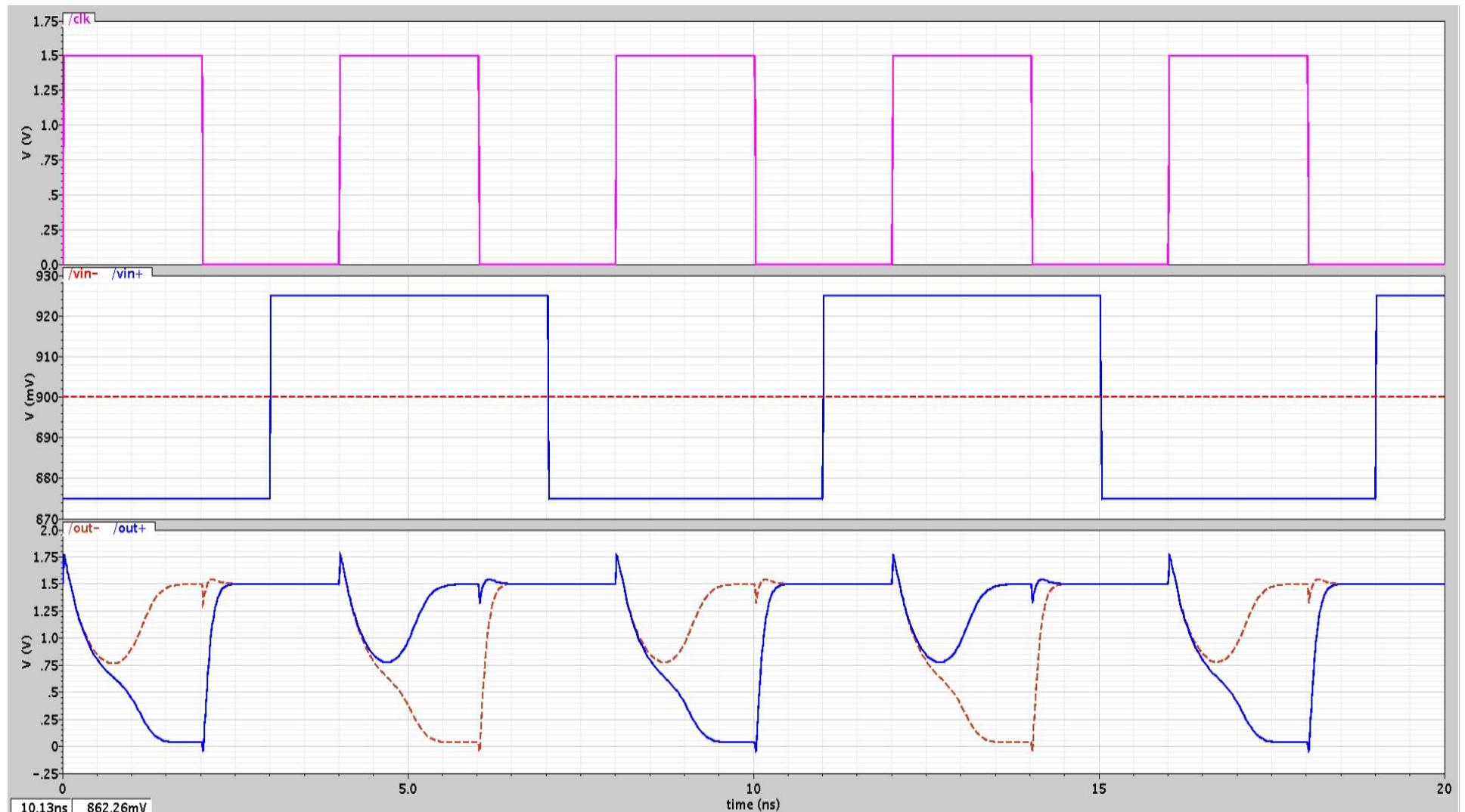


Fig.2 Comparator1 Simulation Waveforms

- Fig.2 shows Simulation waveforms for Comparator circuit 1. Vin- and Vin+ are differential inputs with 50mV difference. Comparator operates with clock of **250MHz**.
- Worst case delay for both the nodes are 552.9ps (out+) and 533.5ps (out-) respectively. Noise Margin high for digital output is Approx. 1V.

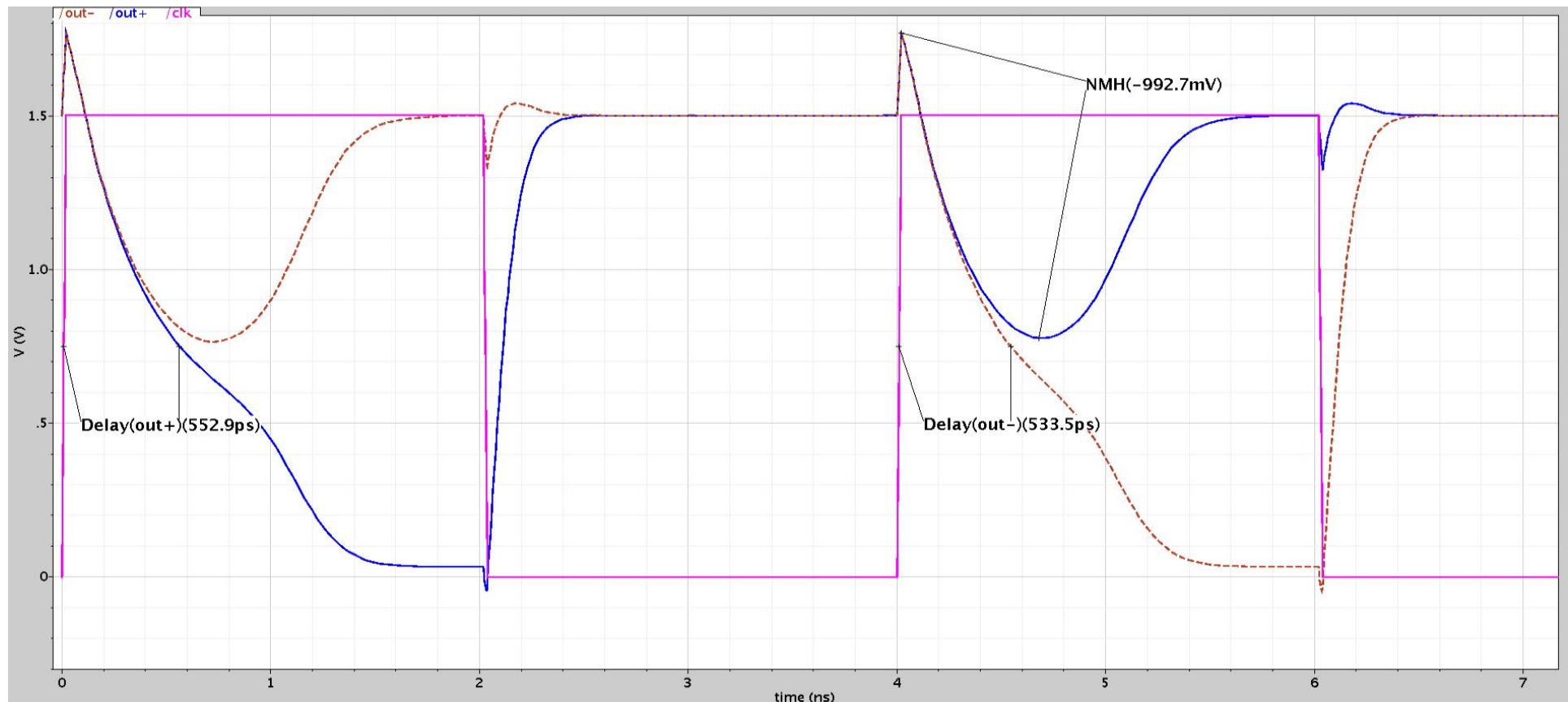


Fig.3 Delay and Noise Margin for Comparator-1 Outputs

2. Comparator-2 [Ref :[1]]:

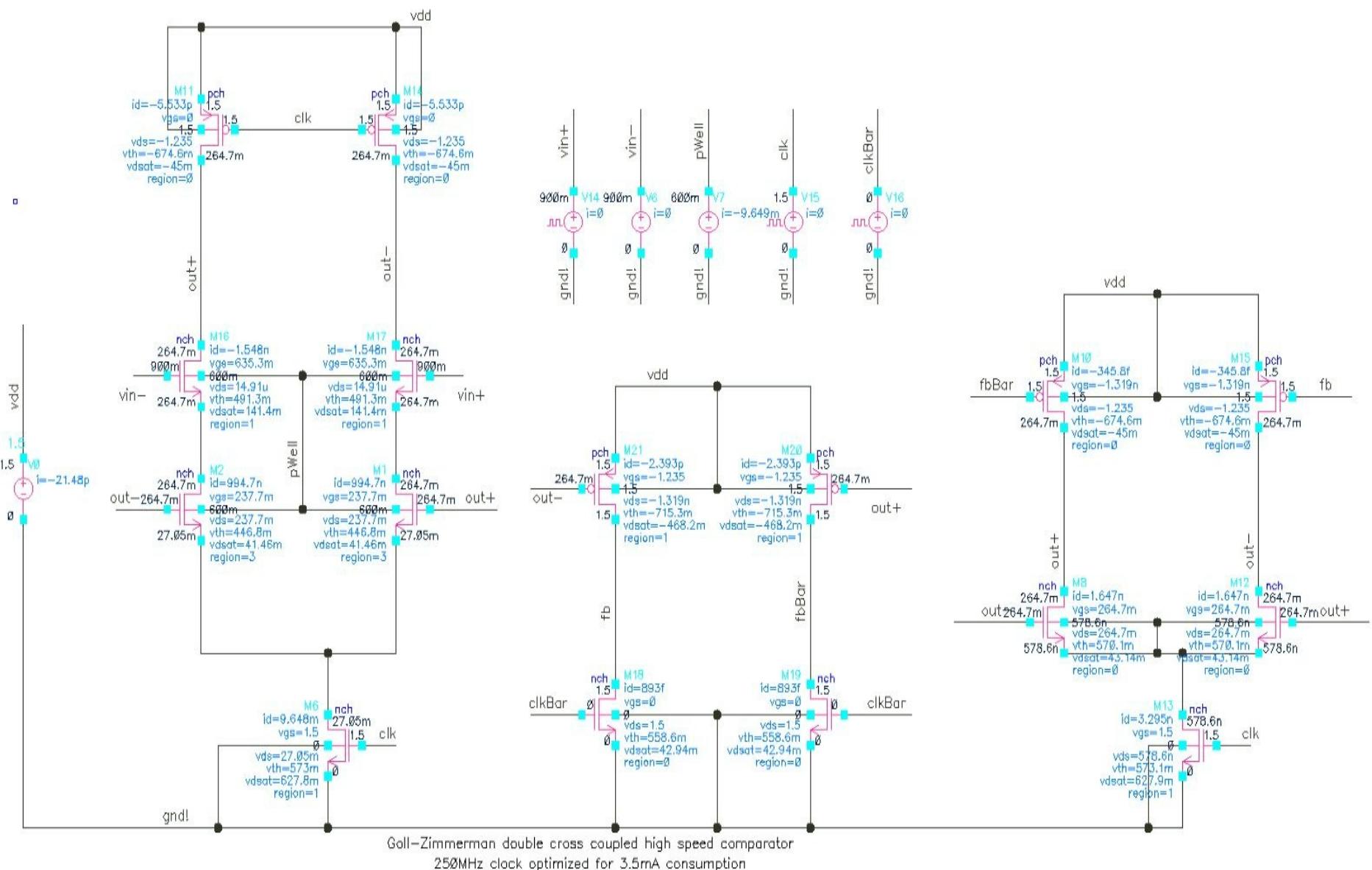


Fig.4. Double Cross Coupled High Speed Comparator (Comparator-2)

- In contrast to a conventional latch (Fig.5), which consists of two cross-coupled inverters (M8,M12,M10,M15) the double cross coupled latch is expanded into two paths between the supply rails so that only the threshold voltage of one transistor (instead of two) has to overcome in each path.
- Clock period consists of a reset phase ($\text{clk}=\text{Low}$), which builds up a start condition ($\text{Out+}=\text{Vdd}$ and $\text{fb}=0$) to compare voltage vin+ with vin- in the following comparison phase ($\text{clk}=\text{Vdd}$). During reset, transistors M13 and M6 are switched off and reset
- transistors M10 and M15 pull both output nodes Out- and Out+ to Vdd, which in succession turn M20 and M21 off and nodes fB and fBbar are discharged to gnd by M18 and N4, which are switched on.
- The gates of transistors M2 and M1 are also at voltage level Vdd, so that M2 and M1 are initially switched on, when comparison phase starts. For comparison, M6 and M13 are turned on ($\text{clk}=\text{Vdd}$) and P2, P3, N3 and N4 are switched off. If $\text{vin+}>\text{vin-}$, then out+ is discharged with transistor M17 more than out- with M16 and positive feedback is started.
- out is pulled towards gnd by M17 and M12 more than out by M16 and M8 thus M21 is turned on before M20 and fb is pulled towards vdd while fbar remains near gnd for sufficient $|\text{vin+}-\text{vin-}|$. Hence, M15 and M8 are switched off, M11 and M12 are on, out is pulled to vdd, out to gnd, and fb is at vdd. Due to the separated p-well (triple-well process) of NMOS transistors, the body effect can be used to reduce the threshold voltages of transistors N5 to N8 by setting PWELL to maximum 0.7V.
- Fig.2 shows Simulation waveforms for Comparator circuit 2. Vin- and Vin+ are differential inputs with 50mV difference. Comparator operates with clock of **250MHz**.
- Worst case delay for both the nodes are 378ps (out+) and 354.2ps (out-) respectively. Noise Margin high for digital output is Approx. 1V.

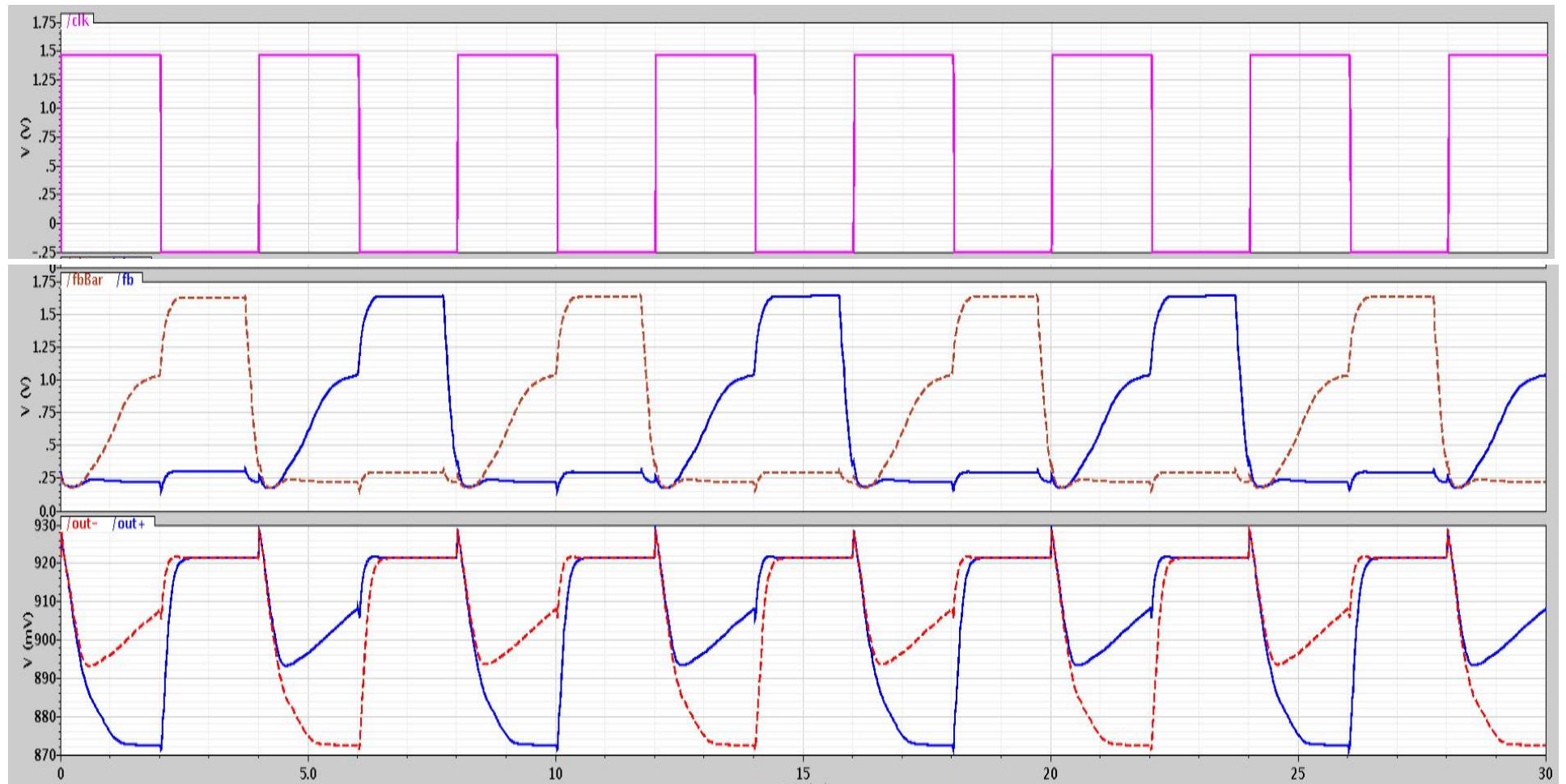


Fig.5 Comparator-2 Simulation Waveforms

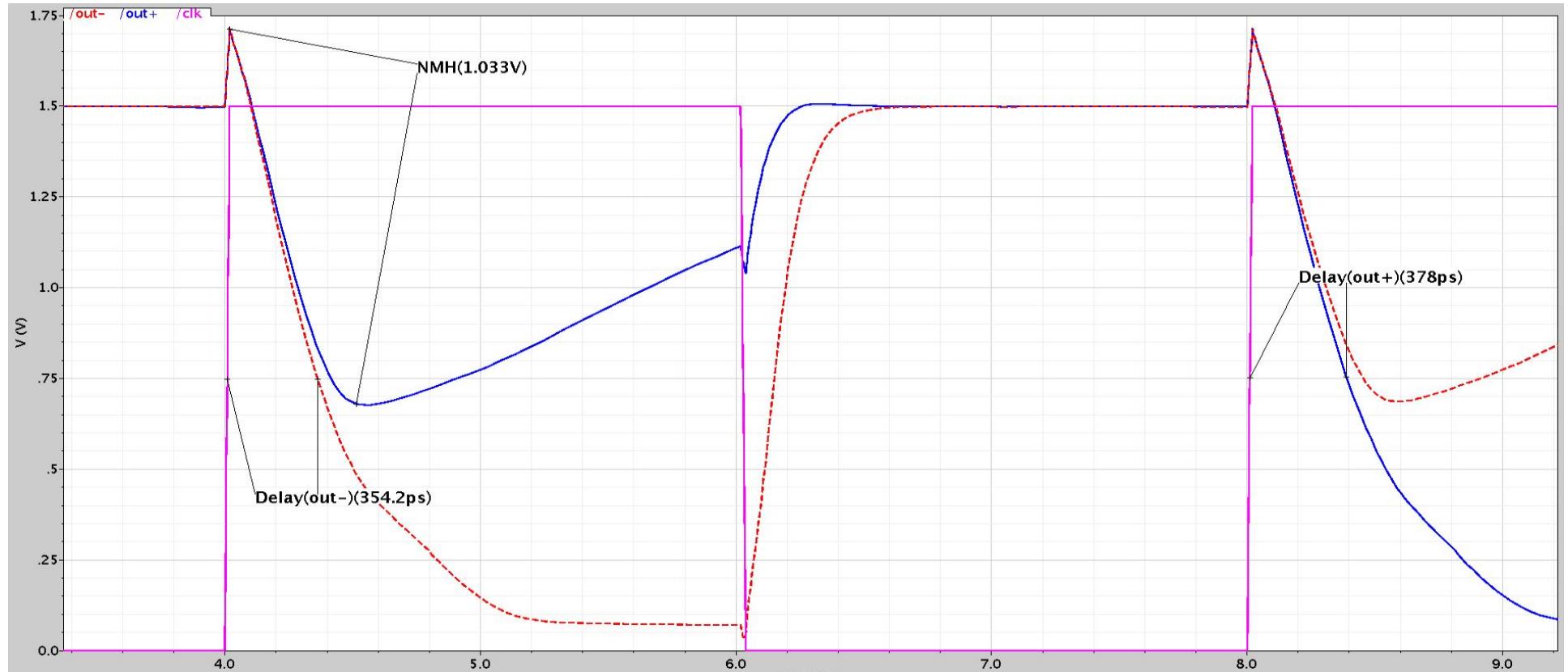


Fig.6 Delay and Noise Margin for Comparator-2 Outputs

3. Comparator-3 [Ref :[2]]:

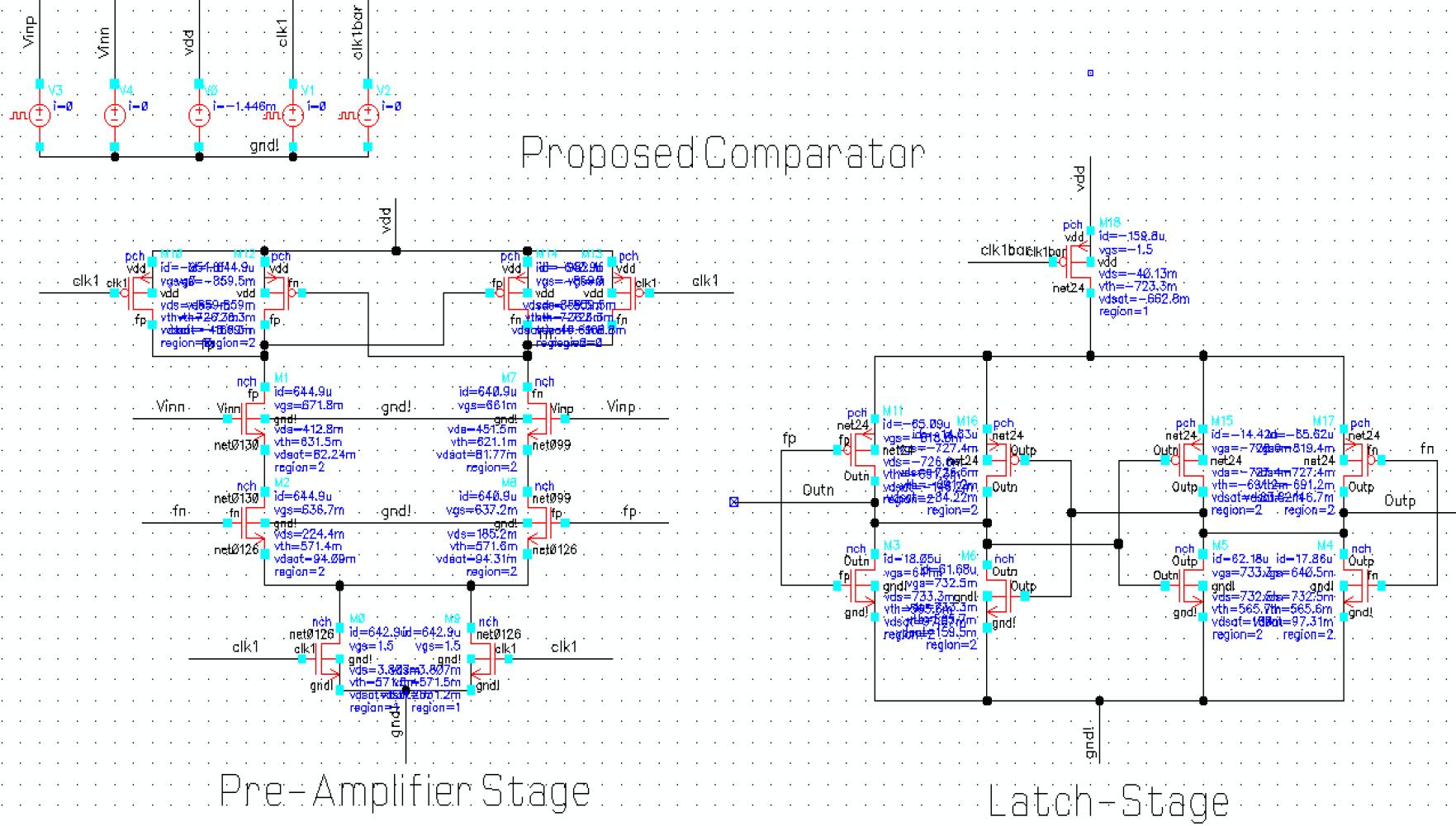


Fig.7 Proposed Comparator for Clock frequency of 250MHz

- Single tail comparator is unable to draw much power required for a high-speed comparator. Dual rail however provides sufficient power to the comparator circuit: one rail to latch and one rail to differential pair.
- When the clock clk1 is LOW, the transistors M10 and M13 are turned ON and the transistors in Mtail1 is turned OFF. The comparator is in reset mode and the outputs are ‘0’.
- The transistors M11 and M17 pulls up the drain potential to VDD. If the input Vinp > Vinn, then the transistor M7 tries to discharge the potential to ground with M8 and Mtail1 Transistors. But the outputs remain at their zero potential since the transistors M3 and M4 are ON.
- After some time when the clock clk1 is HIGH, the transistors M10 and M13 are OFF and the transistors in Mtail1 are ON. This is the evaluation phase of the comparator. The drain potential of M1 is already at higher potential and it will discharge through M2 and Mtail1 transistors to zero. Hence, fn node goes to zero. And output outp becomes High. Latch helps in holding the outputs in a particular level.
- M12 and M14 provides pre-charges the nodes fn and fp. M10 and M13 act as PMOS loads. M1 and M7 provides low gain amplification. M2 and M8 acts as switches to lower the power dissipation. M5, M6, M15 and M16 forms the latch. Two tail transistors are used Mtail1(M0 and M8) and Mtail2 (M18). When fn is ‘High’ M4 is ON and Outp becomes zero.
- Similarly, when fp is ‘High’ M3 is ON and Outn becomes Zero. When One node becomes zero the other node is charged to Vdd. By adding a PMOS Transistor to the overall circuit the output swing is increased. A PMOS and NMOS Transistor at the output of the differential pair gives a better amplification and swing.
- Mtail1 Transistors provide faster pull down which can be achieved by increasing width of M0 and M8 Transistors. Width of Mtail1 is kept large and width of Mtail2 is kept small for faster operation.
- Proposed Comparator is shown in Fig.7. A Conventional dynamic comparator is not able to drive large transistors due to only one supply rail. Here it can drive large loads since power consumption would be more in case of dual supply rail.
- Fig.8 shows Simulation waveforms for Comparator circuit 2. Vinp and Vinn are differential inputs with 50mV difference. Comparator operates with clock of **250MHz**.
- Worst case delay for both the nodes are **658ps (outp)** and **729ps (outn)** respectively. Noise Margin Low for digital output is Approx. **400mV**

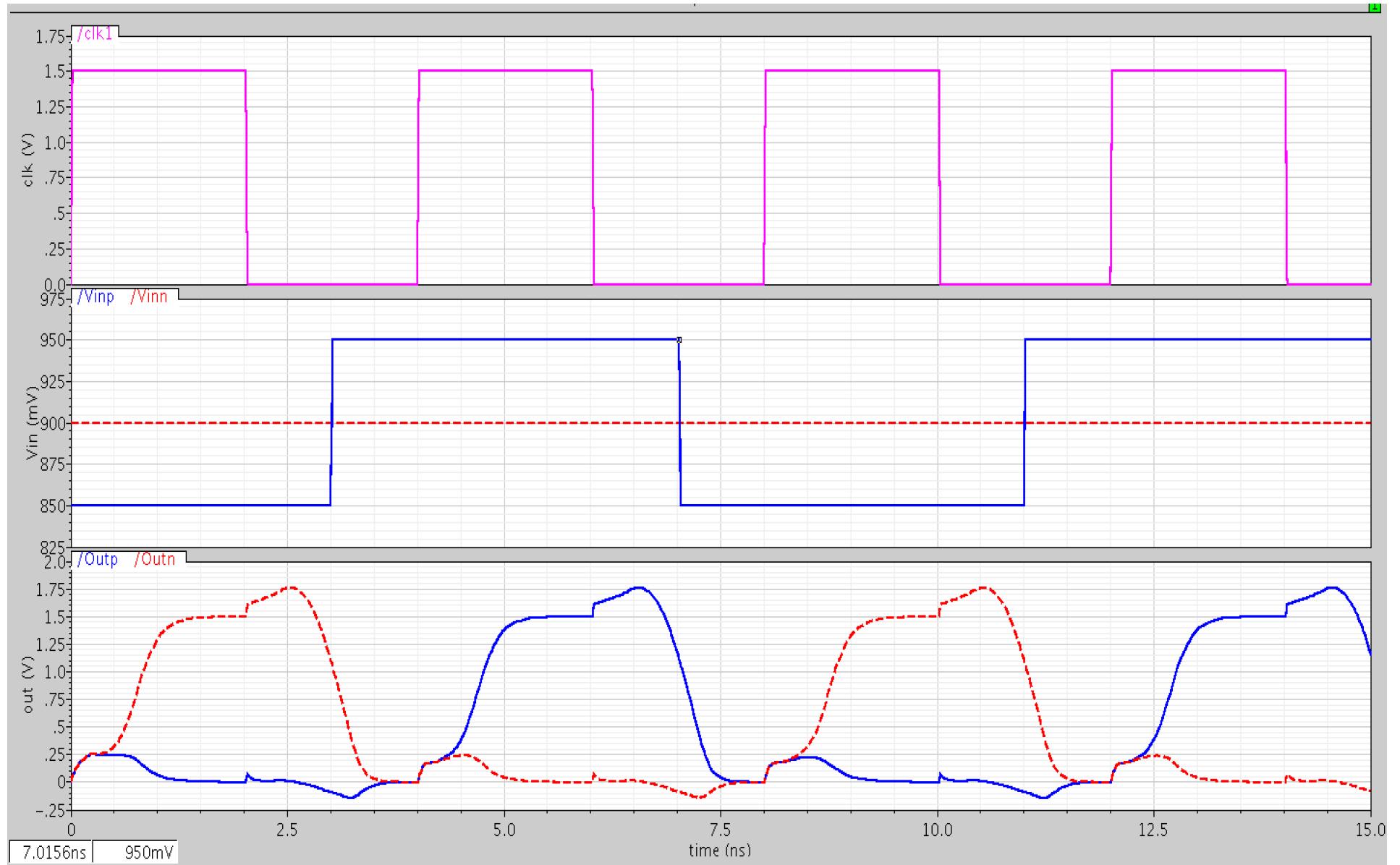


Fig.8 Comparator-3 Simulation Waveforms

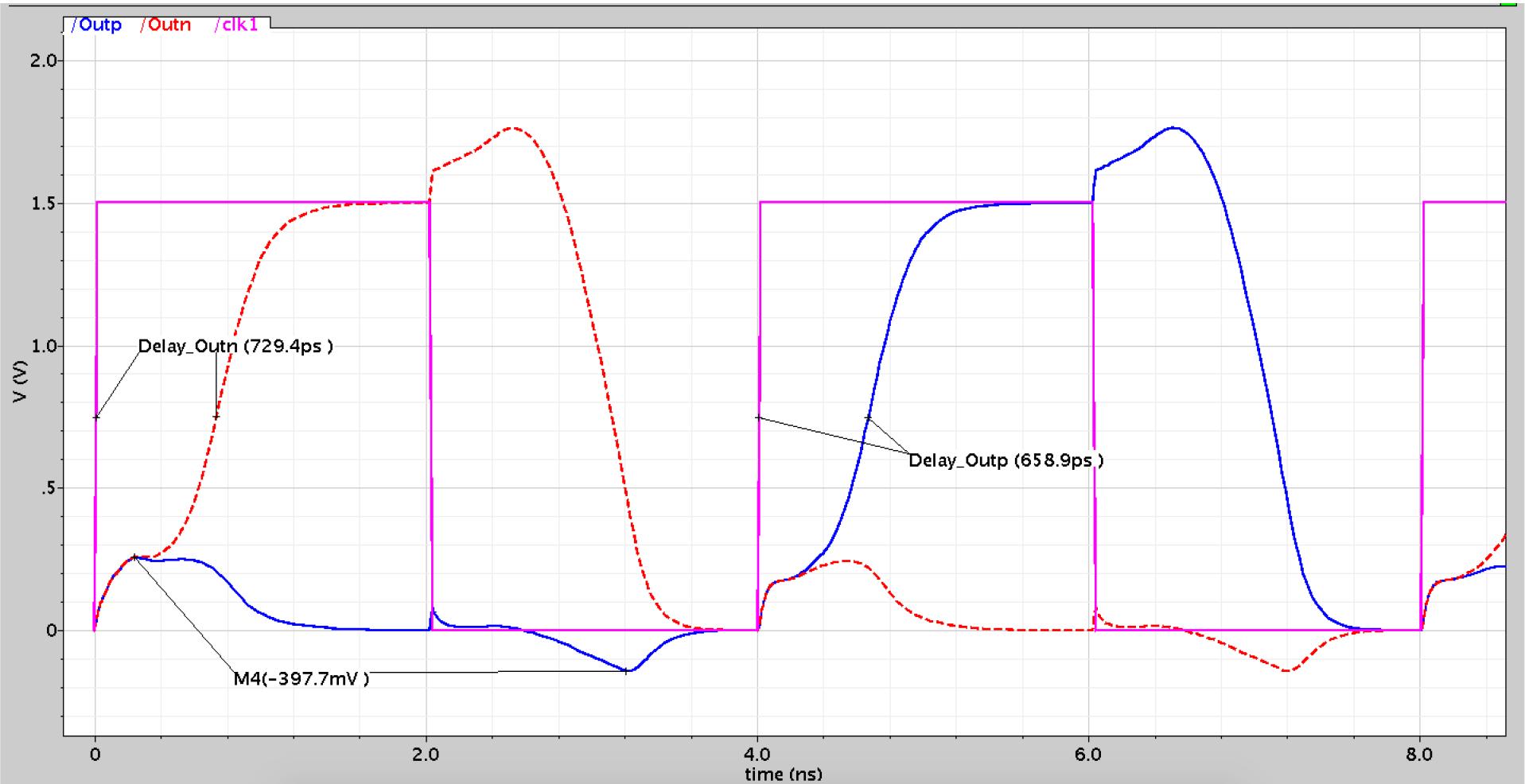


Fig.9 Delay and Noise Margin for Comparator-3 Outputs

Comparator Comparison Table

Parameter	Comparator Ckt-1	Comparator Ckt-2	Comparator Ckt-3
Supply Voltage (Vdd)	1.5 V	1.5 V	1.5 V
ΔV_{in}	$\pm 25\text{mV}$	$\pm 25\text{mV}$	$\pm 50\text{mV}$
f_s	250MHz	250MHz	250MHz
V_{cm}	0.75 V	0.75 V	0.75 V
Worst case Delay	$t_p = 552.9\text{ps} \& 533.5\text{ps}$	$t_p = 378\text{ps} \& 374.2\text{ps}$	$t_p = 658\text{ps} \& 729\text{ps}$
Current Consumption	4mA	3.5mA	3.7mA
Noise Margin	$\approx 1\text{V}$	$\approx 1\text{V}$	$\approx 400\text{ mV}$

Track & Hold Circuits:

1. T&H Circuit-1 [Ref :[3]]:

- Architecture of Bootstrap Switch is shown in Fig 10. Instead of applying VDD to the Gate, by applying ($VDD + V_{IN}$) to the Gate terminal, V_{GS} can be made constant.
- This can be implemented by connecting a capacitor from Gate to Source terminals. When switch is ON sampling capacitor charges to VDD. Then $V_{GS} = VG - VS = (VDD + VIN) - VIN = VDD$ i.e. a constant.
- Therefore ON Resistance of Bootstrap Switch becomes linear and there is no harmonic distortion. Implementation of given Bootstrap Switch is shown in Fig 2.

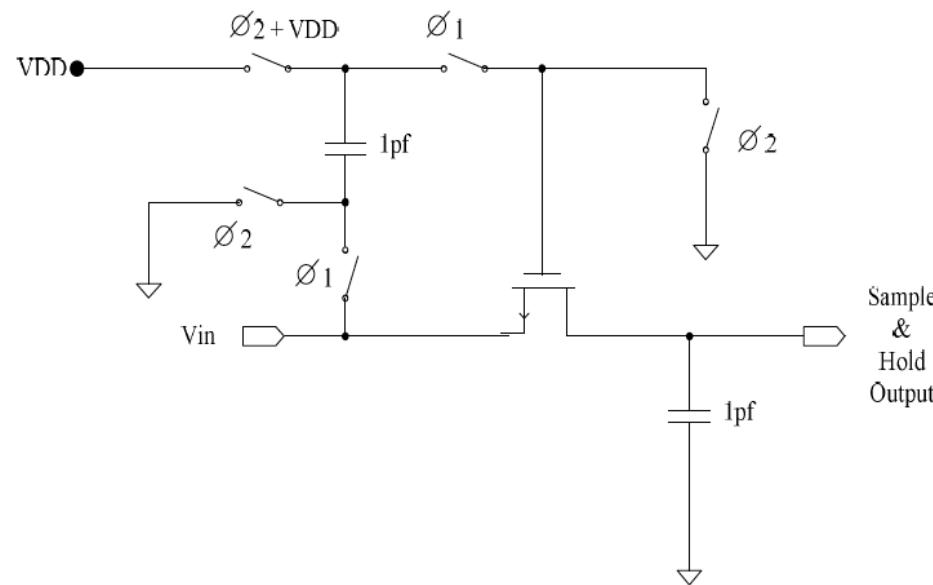
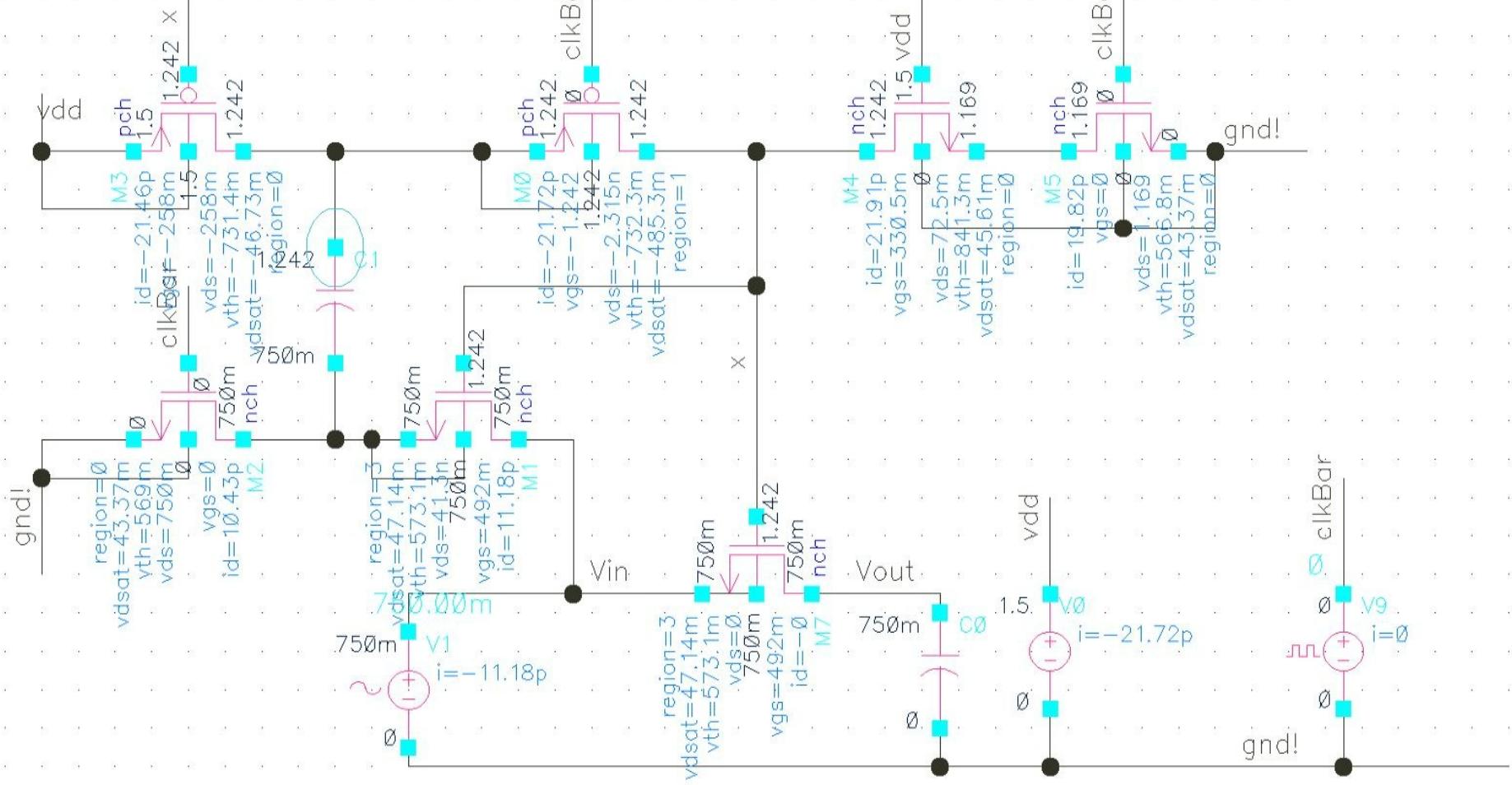


Fig.10 Proposed T/H Circuit (Ref: [3])



- Simulation Waveforms of proposed T/H circuit are shown in Fig.12. f_s is **50 MHz** and Input Frequency f_{in} is **5MHz**.
- Fig.12 shows how Gate voltage of Pass Transistor is boosted along with V_{in} .

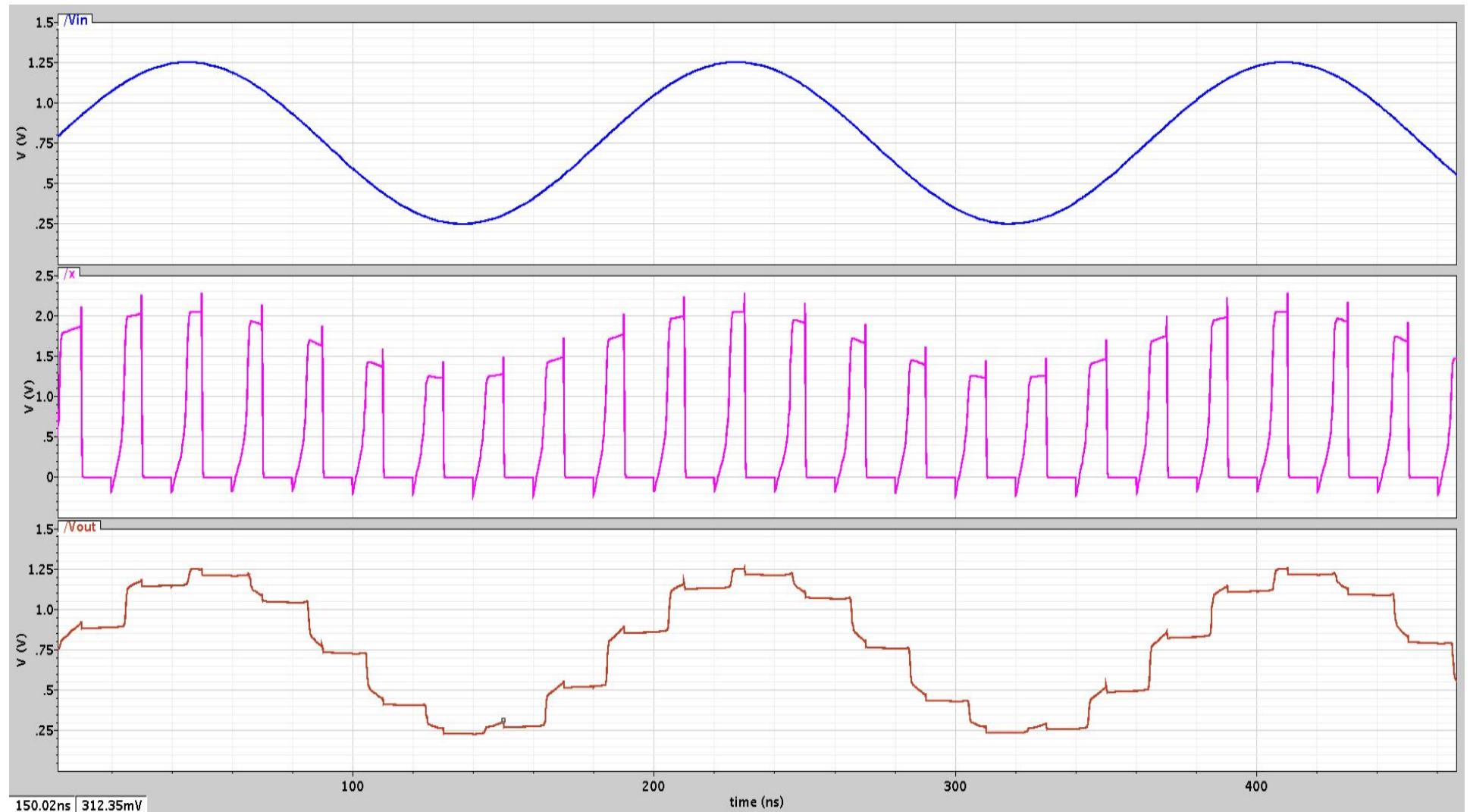


Fig.12 T/H Circuit-1 Simulation Waveforms

2. T&H Circuit-2 [Ref :[4]]:

- In a Time-Interleaved ADC, multiple sub- ADCs are placed in parallel, and each sub-ADC (channel) processes a different sample of the input signal at a low sampling rate. By increasing the number of the channels in a TI ADC, the aggregate sampling rate of the ADC can be increased.
- Frontend Track-and-Hold (T/H) circuits are a critical building block in high-speed ADCs. Whether there is a single frontend T/H running at the aggregate sampling rate or each channel has a separate T/H running at a low sampling rate as in Fig. 13, the T/H should be able to sample very high-frequency input signals. The maximum input frequency can be as high as half the aggregate sampling rate (Nyquist frequency).

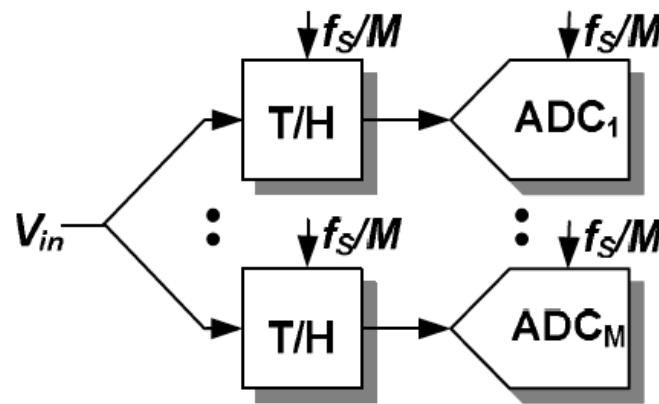


Fig.13 Separate T/H for each channel in TI ADC.

- Proposed T&H circuit can be used extensively for TI ADC where separate T/H is used for each channel. Proposed Bootstrapping T&H Circuit is shown in fig.14. It uses a PMOS transistor (M1) to shift the input signal by its gate-source voltage V_{GS2} . When CLK is low, M1 is off and M3 is on. The voltage at node X is $V_{in} + |V_{GS2}|$. The gate of the main switching transistor (M1) is also at V_X .
- The gate-source voltage of M0 is $V_{GS1} = V_Y - V_{in} = |V_{GS2}|$.
- Since the drain current of M2 is constant, its gate-source voltage is also constant. The gate-source voltage of M0 is, to

the first approximation, independent of the input voltage. In practice, V_{GS2} weakly depends on V_{in} because of channel-length modulation and body effect.

- Nevertheless, due to the almost constant V_{GS} (Boot-Strapping charge is stored in V_{GS} of M2) of M2 in Fig. 14, the nonlinearities caused by the charge injection of M0, the sampling aperture error, and variable R_{on} of M1 are significantly reduced compared with a conventional T/H.
- For a high-frequency input, the delay from input to node Y prevents M0 to have a completely constant V_{GS} . Using a small-signal model and for in-band frequencies, it can be shown that the delay from input to node Y can be approximated by

$$\tau_{BS} \approx R_{on3}C_Y + (C_{GS2} + C_X + C_Y) / g_{m2}$$

- Where, C_{GS2} and g_{m2} the gate-source capacitance and trans-conductance of M2, respectively. C_X and C_Y model the total capacitance at nodes X and Y, respectively, and R_{on3} is the on-resistance of M3 in the triode region. The time constant needs to be minimized by proper sizing of the transistor and having a sufficiently large g_{m2} . This sets a lower limit for the bias current of M2.

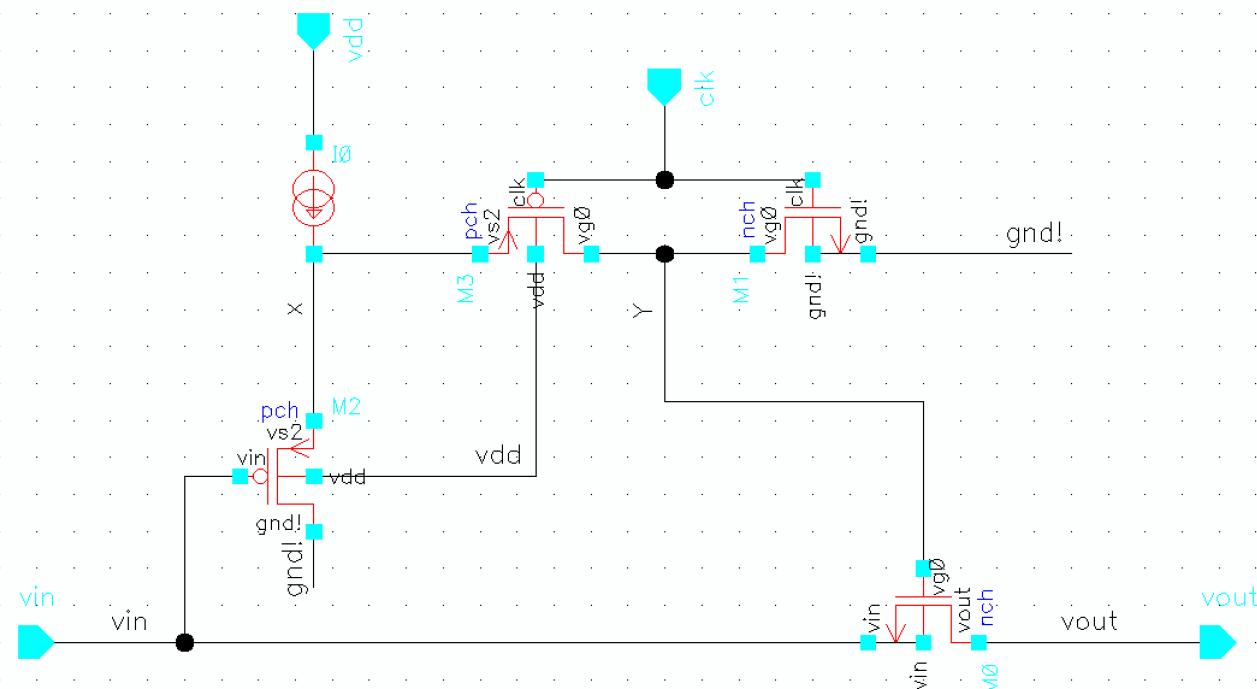


Fig.14 Proposed T&H Circuit

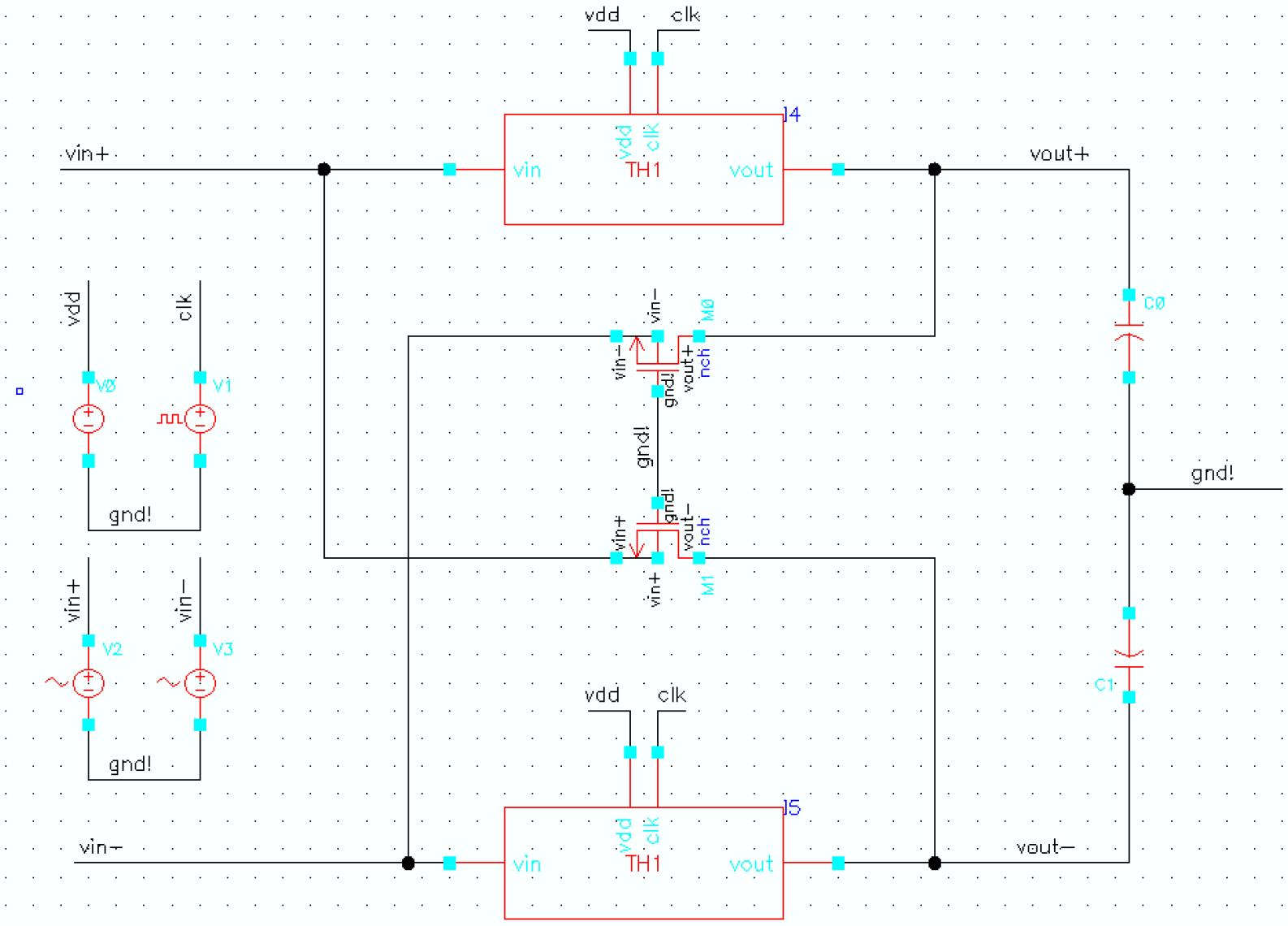


Fig.15 Differential T/H Circuit for Feed-Through Cancellation

- As shown in Fig.15 M0 and M3 are connected to have feedthrough cancellation and they are of same size as Pass Transistor shown in Fig.14

- Simulation Waveforms of proposed T/H circuit are shown in Fig.16. f_s is **250 MHz** and Input Frequency f_{in} is **2.5GHz**.
- Fig.17 shows Input Feed-Through in Hold mode. Fig.18 Shows delay in Track mode.

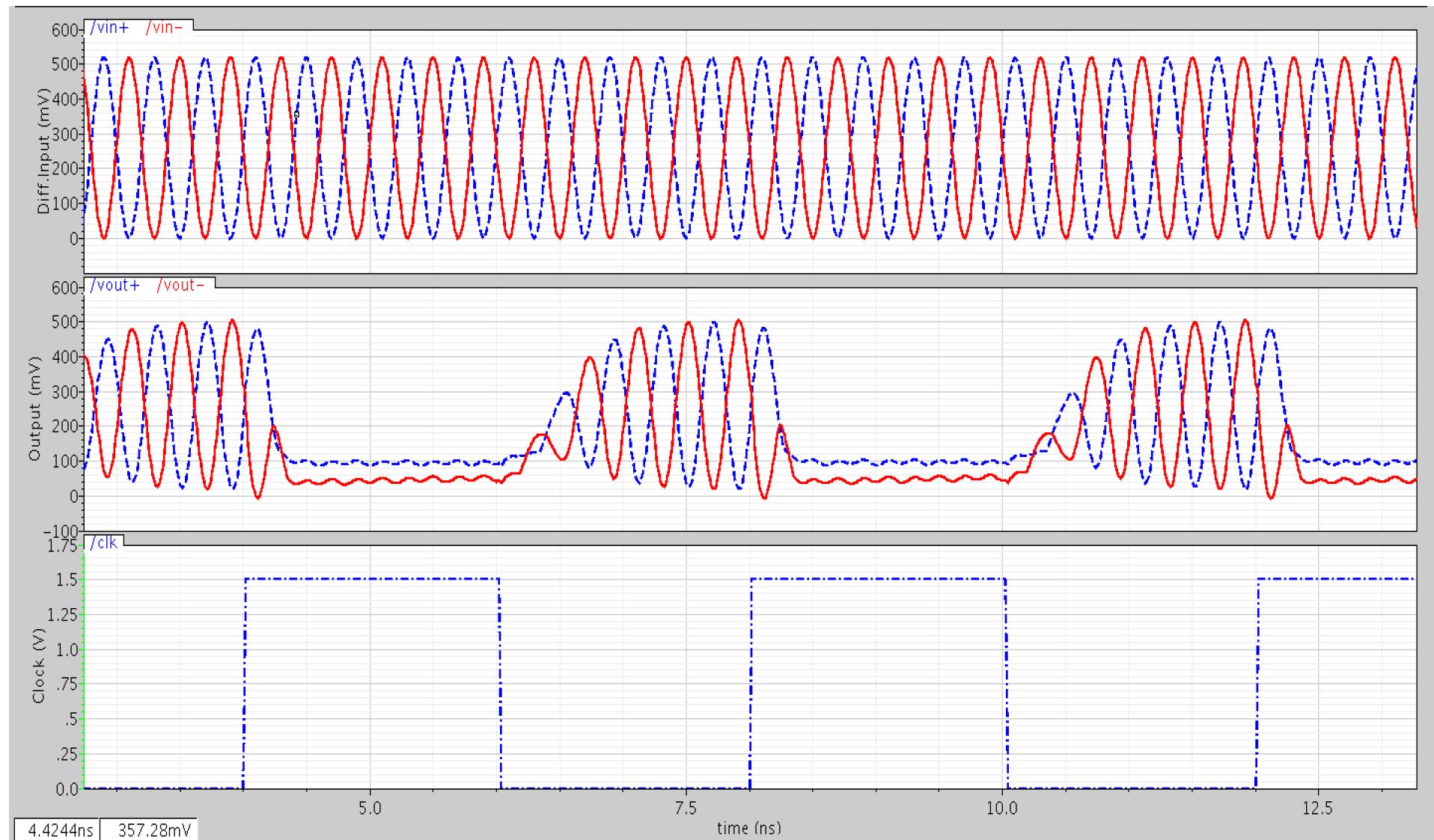


Fig.16 T/H Circuit-2 Simulation Waveforms

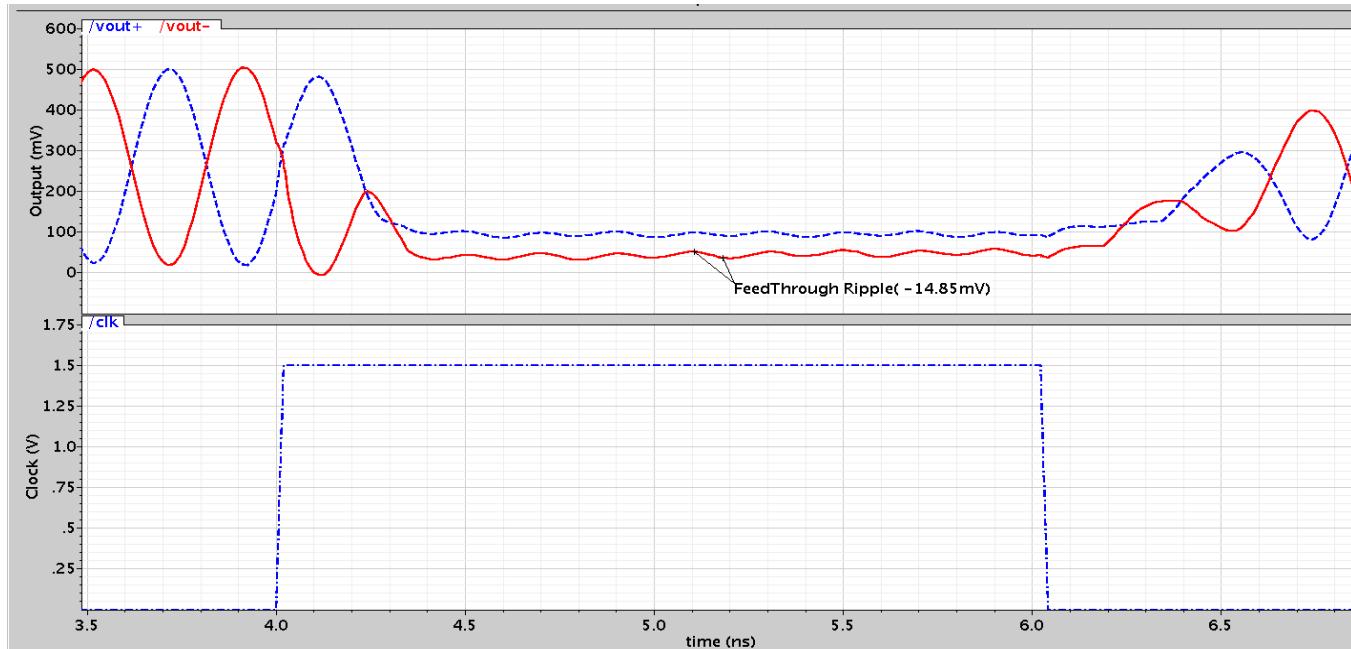


Fig.17 Feed-Through in Hold Mode

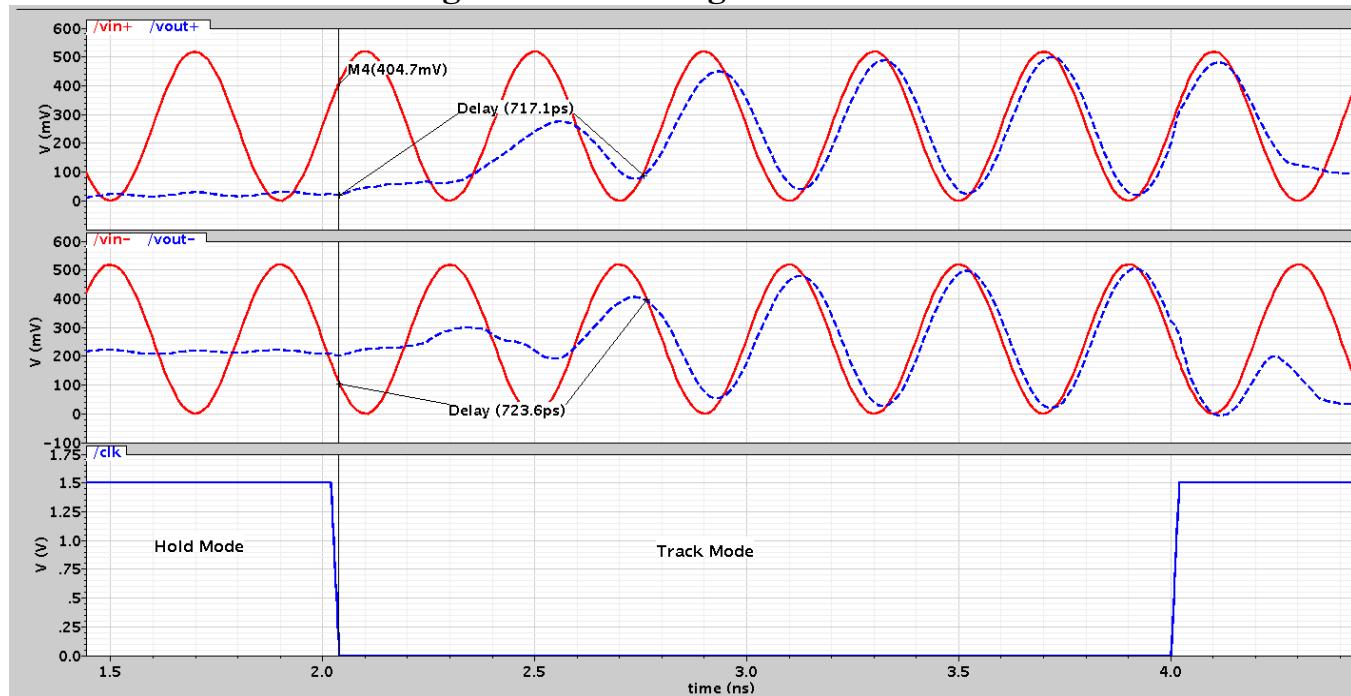


Fig.18 Delay in Track Mode

3. T&H Circuit-3 [Ref :[5]]:

- The proposed T/H architecture (Figure 19) is inspired by employing a global clock phase to determine the sampling instant for each individual channel, to reduce the issue of phase skew matching between multiple sub-ADCs.
- As shown in Fig. 19, an 8-channel time-interleaved ADC is proposed, with a global sine-wave clock applied to each individual T/H switch to synchronize the sampling instants.
- Each switch is not only controlled by one of the multi-phase clocks $ck[i]$, but also synchronized by the highest-frequency (f_s) sine-wave clock. The sampling instant when the input signal is sampled on to the loading capacitors $C_L[i]$ is defined by the global clock Sin .

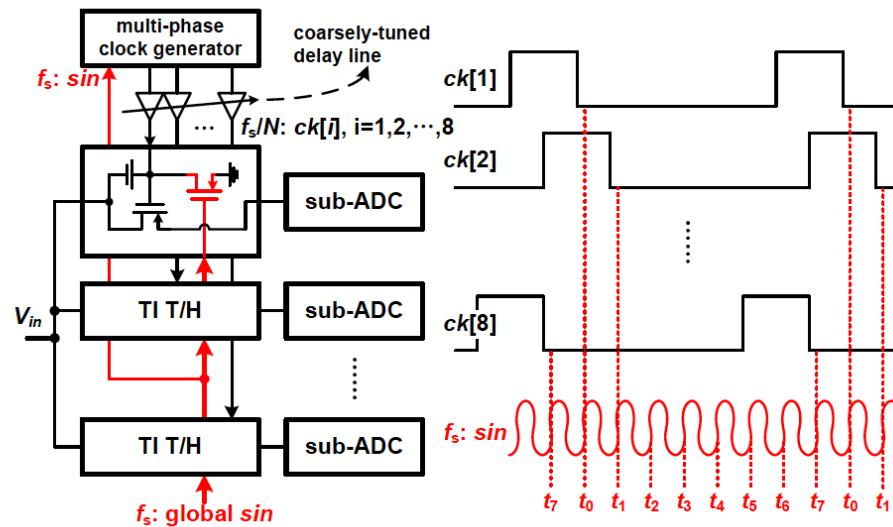


Fig.19 Distributed Time-Interleaved with global sine clock.

- To implement the T/H function described in Fig. 19 above, a modified bootstrapped T&H circuit shown in Fig.20 is utilized, where the discharge path connects the gate of the pass transistor M6 to ground in order to turn it OFF.
- During the tracking phase when clk is high, the bootstrapped switch operates normally, with the gate-source voltage of M6 equal to the constant voltage difference previously stored across the internal capacitor C_0 .
- The gate of transistor M6 will be shorted to ground only after both the complementary clk and the global sin reach the threshold to turn ON transistors M4 and M5.

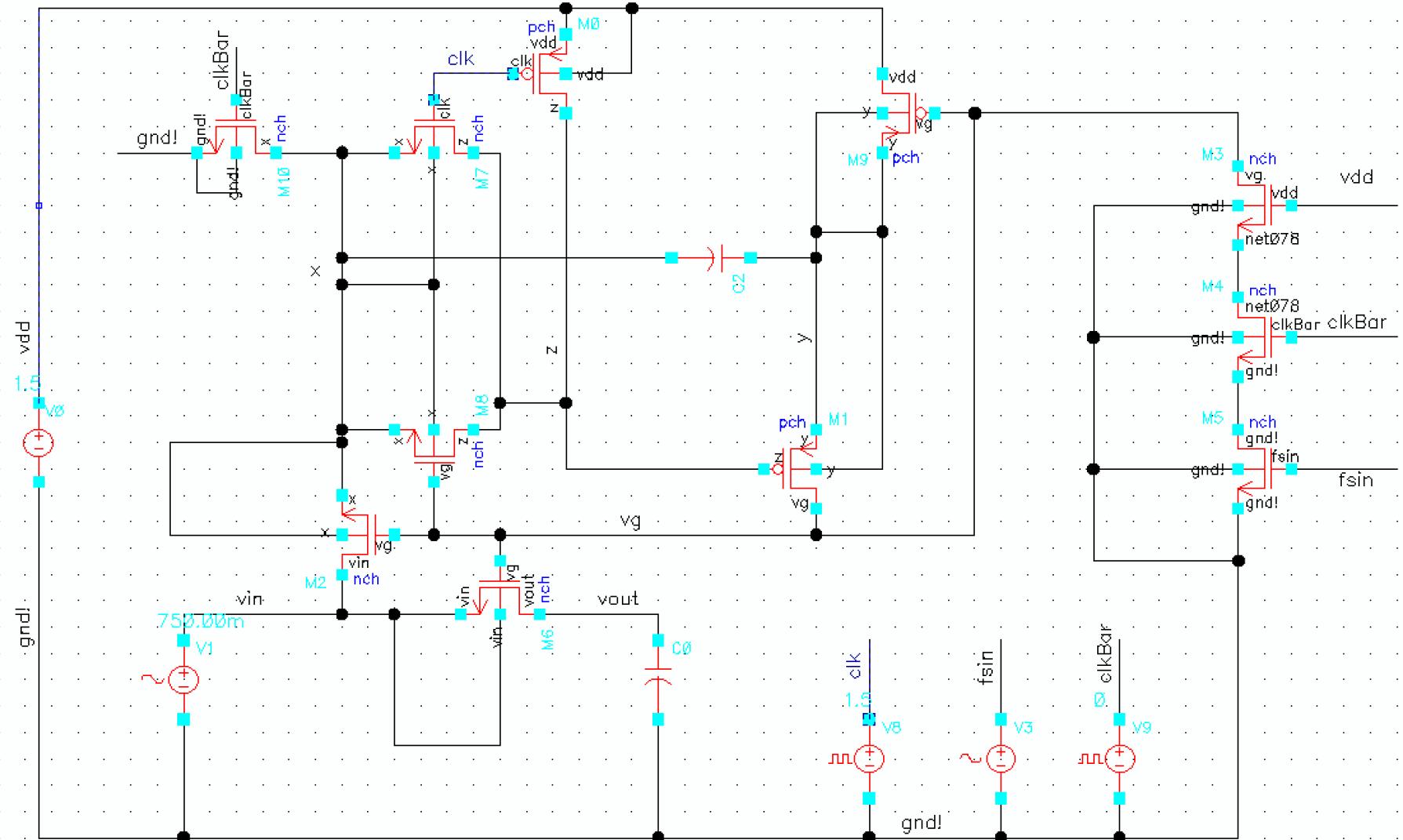


Fig.20 Proposed T&H circuit for each phase

- When Clk is low and Clkbar is high, Capacitor is charged to Vdd through M10 and in High Clk phase, X node reaches to Vin and Vin+Vcap will appear across M6 (Pass Transistor) through M1 Transistor.
- Simulation Waveforms of proposed T/H circuit are shown in Fig.21. f_s is **100 MHz** and Input Frequency f_{in} is **1GHz**.
- Fig.22 shows Input Feed-Through in Hold mode. Fig.23 Shows delay in Track mode.
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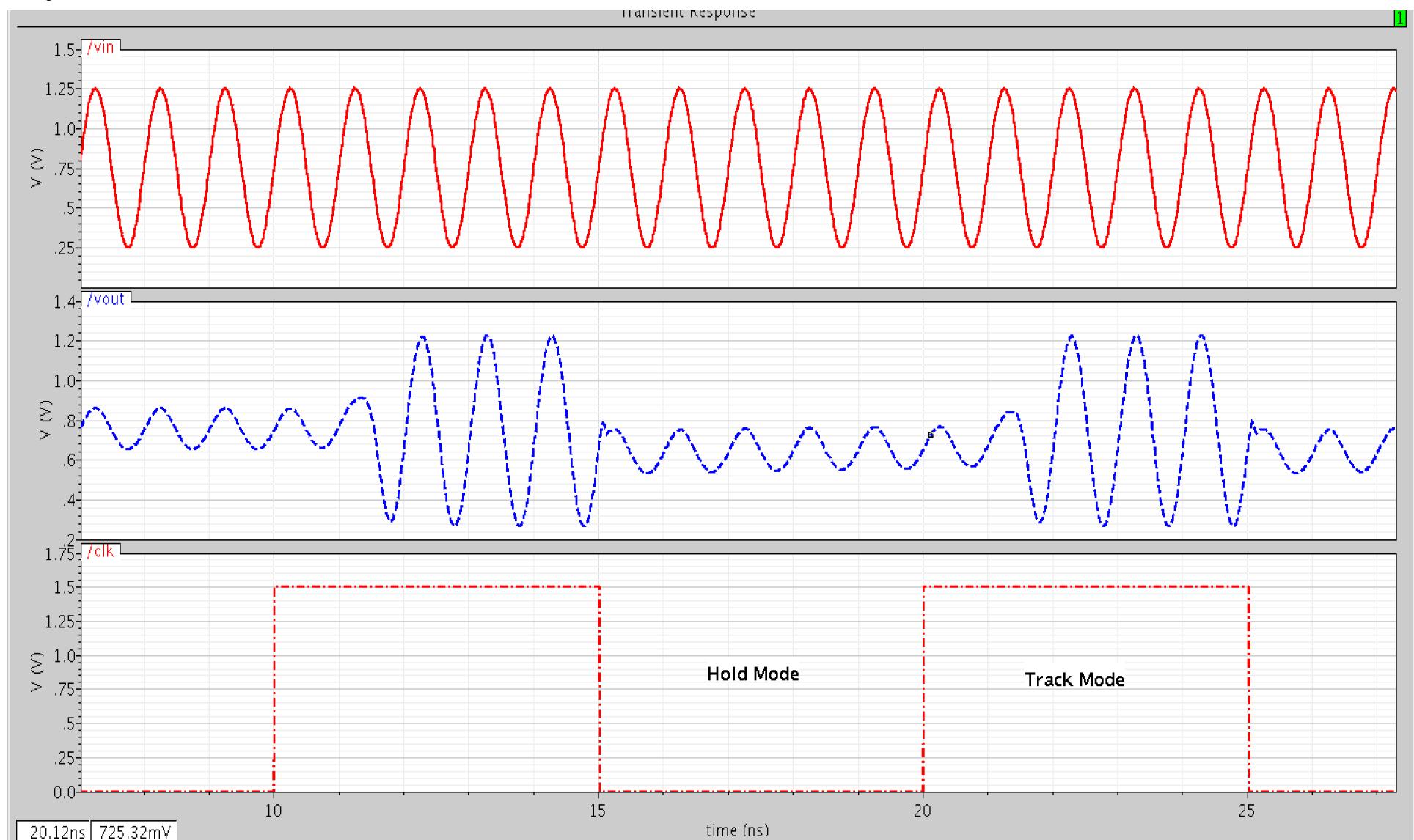


Fig.21 T/H Circuit-3 Simulation Waveforms ($f_{in}=1\text{GHz}$)

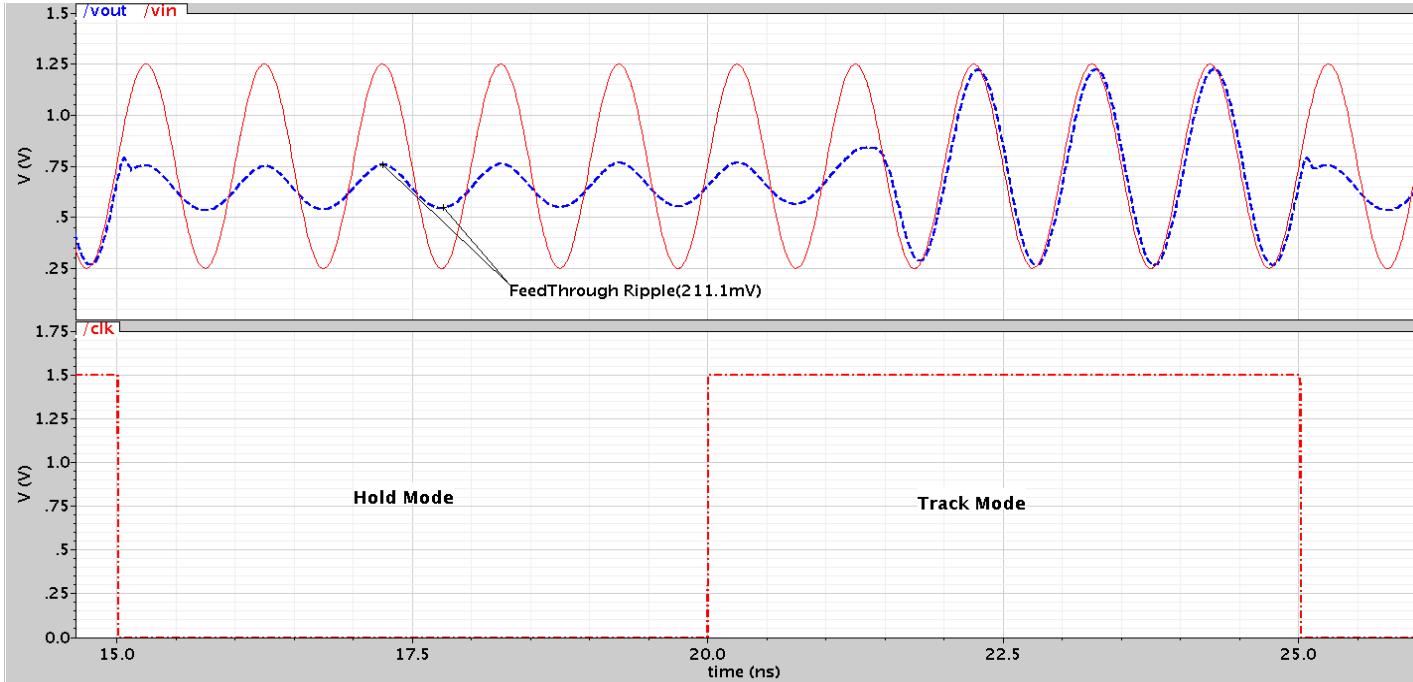


Fig.22 Feed-Through in Hold Mode

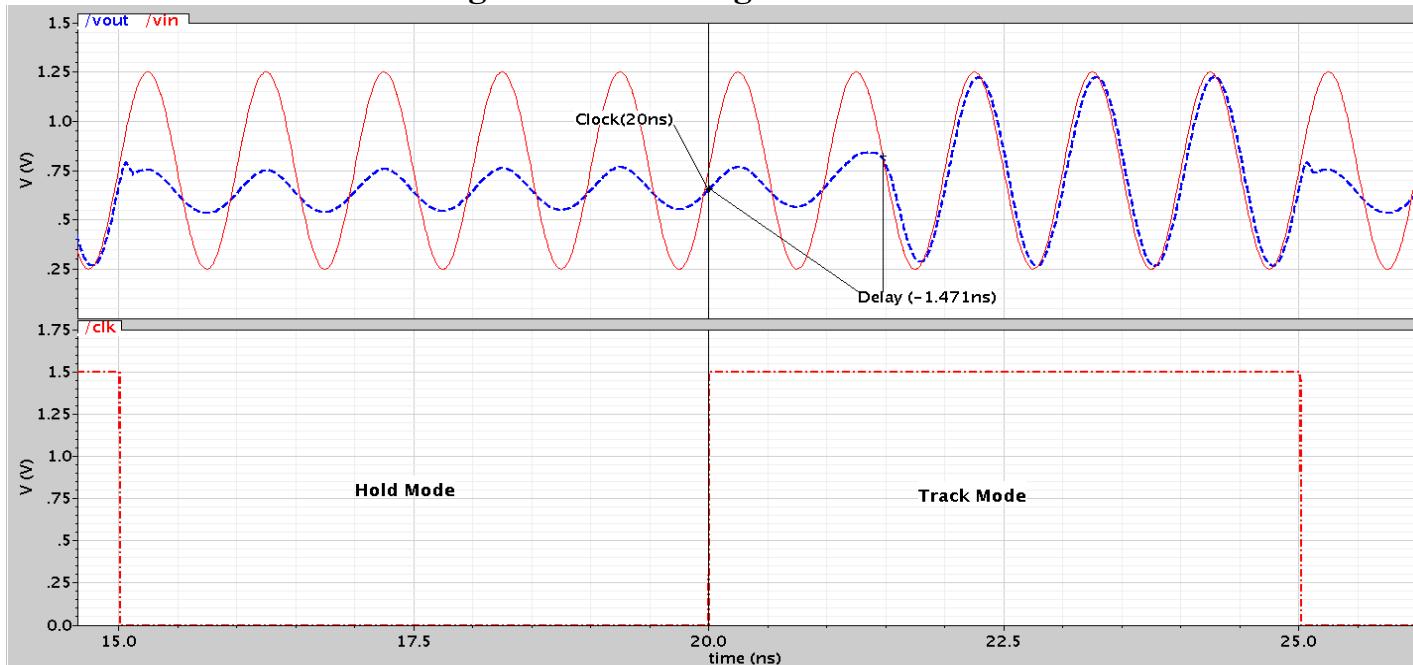


Fig.23 Delay in Track Mode

- Fig.24 Shows waveforms for circuit operates with $f_{in}=5\text{MHz}$.

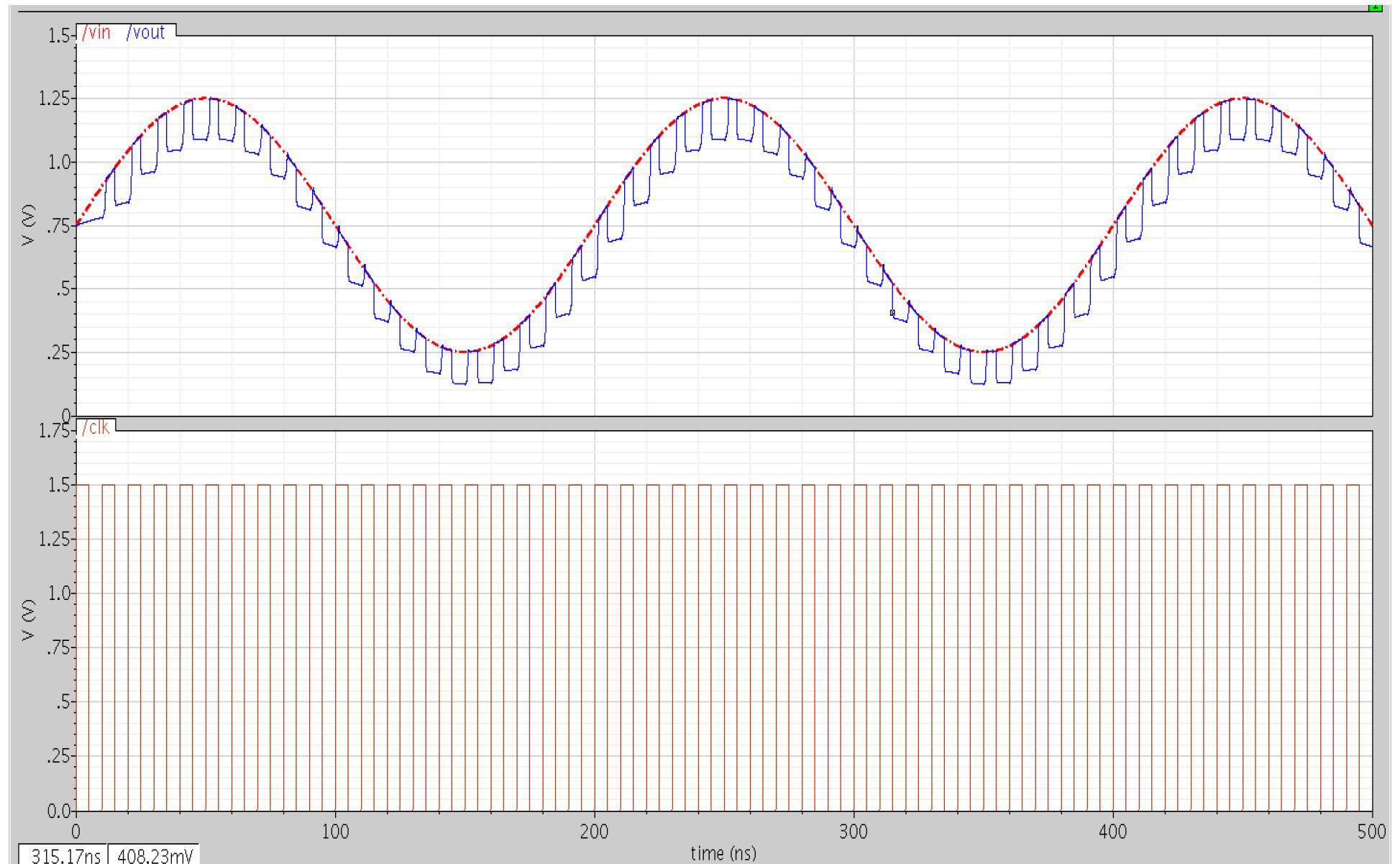


Fig.24 T/H Circuit-3 Simulation Waveforms ($f_{in}=5\text{MHz}$)

- Fig.25 Shows waveform of boosted Gate Voltage across Pass Transistor (M6)

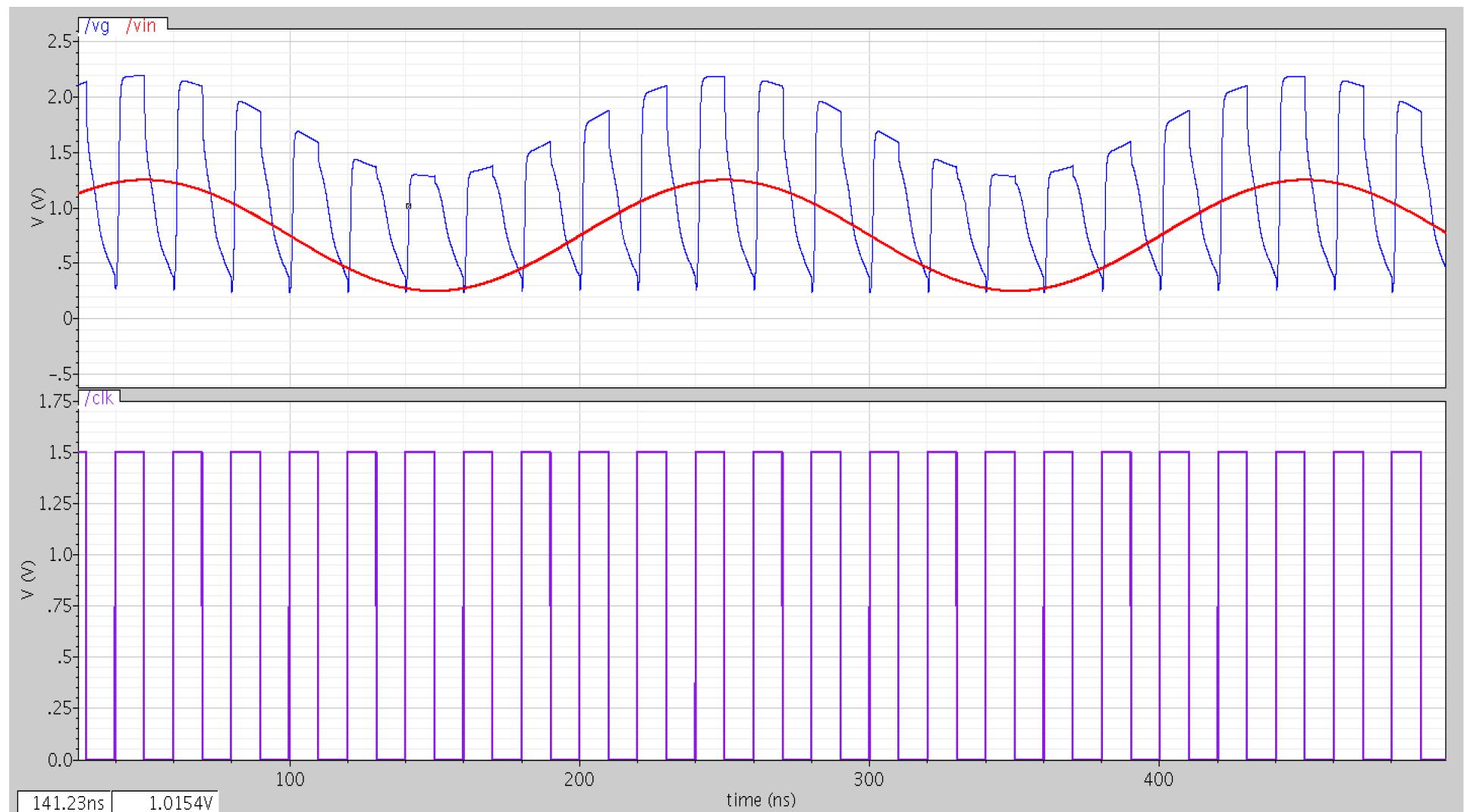


Fig.25 Waveform of V_g of Pass Transistor

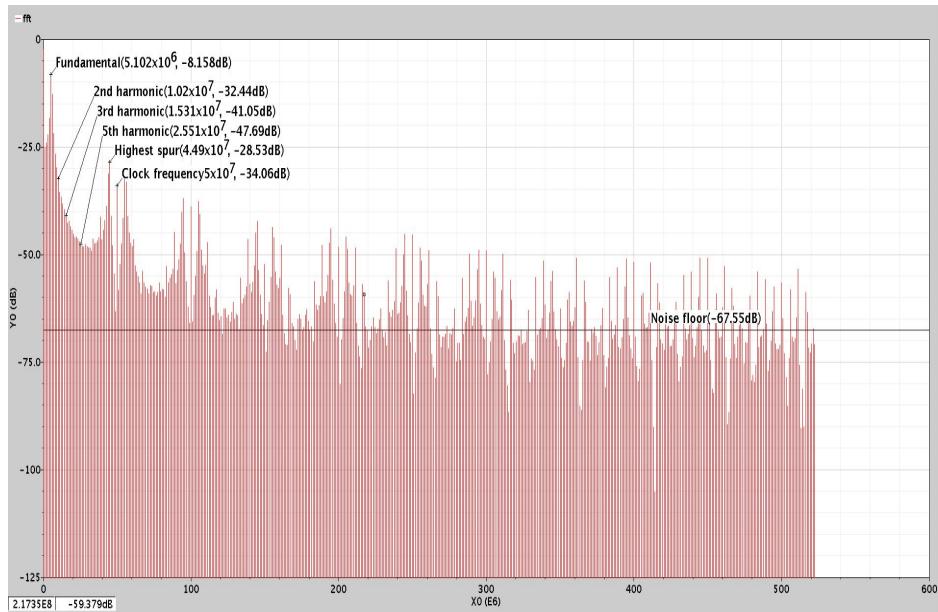


Fig.26 FFT Analysis for T&H Circuit-1

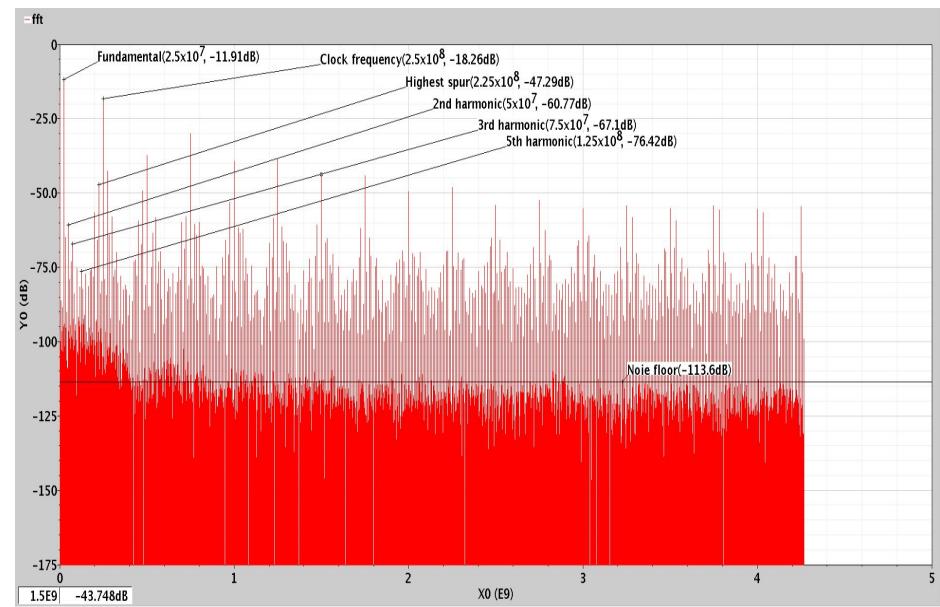


Fig.27 FFT Analysis for T&H Circuit-2

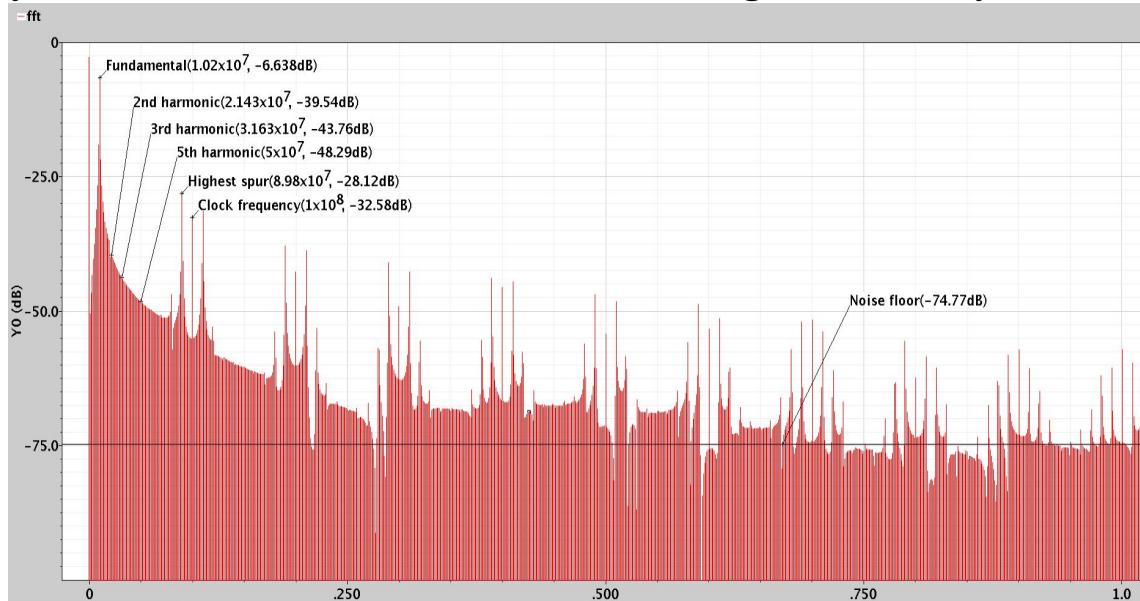


Fig.28 FFT Analysis for T&H Circuit-3

Track & Hold Circuit Comparison Table

Parameter	T&H Ckt-1	T&H Ckt-2	T&H Ckt-3
Supply Voltage (Vdd)	1.5 V	1.5 V	1.5 V
C_L	1pF	1pF	1pF
f_s	50MHz	250 MHz	100MHz
THD	-23.61	-47.86	-31.15
SFDR	20.37	35.38	21.52
SNDR	20.21	64.17	32.37
Input Signal Bandwidth	20MHz	100MHz	40MHz
Current Consumption	0.18mA	9.5mA	0.44mA

References :

- [1] Goll, Bernhard, and Horst Zimmermann. "A 65nm CMOS comparator with modified latch to achieve 7GHz/1.3 mW at 1.2 V and 700MHz/47 μ W at 0.6 V." *Solid-State Circuits Conference-Digest of Technical Papers, 2009. ISSCC 2009. IEEE International*. IEEE, 2009.
- [2] Hussain, Sarfraz, Rajesh Kumar, and Gaurav Trivedi. "Comparison and design of dynamic comparator in 180nm SCL technology for low power and high speed Flash ADC." *Nanoelectronic and Information Systems (iNIS), 2017 IEEE International Symposium on*. IEEE, 2017.
- [3] TP, Jeniba Baswam, B. Harshavardhan, and E. Venkata Ramesh. "A distortion compensating flash analog-to-digital conversion using bootstrap switch." *Advances in Electrical Engineering (ICAEE), 2014 International Conference on*. IEEE, 2014.
- [4] Sedighi, Behnam, Anh T. Huynh, and Efstratios Skafidas. "A CMOS track-and-hold circuit with beyond 30 GHz input bandwidth." *Electronics, Circuits and Systems (ICECS), 2012 19th IEEE International Conference on*. IEEE, 2012.
- [5] Jiang, Tao, and Patrick Y. Chiang. "14.4-GS/s, 5-bit, 50mW time-interleaved ADC with distributed track-and-hold and sampling instant synchronization for ADC-based SerDes." *Wireless Symposium (IWS), 2015 IEEE International*. IEEE, 2015.

APPENDIX II

REFERENCE PAPERS FOR COMPARATORS

APPENDIX I

REFERENCE PAPERS FOR T&H CIRCUITS