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19.4 A 65nm CMOS Comparator with Modified Latch to Achieve 7GHz/1.3mW at 1.2V and 700MHz/47 μ W at 0.6V

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Clocked regenerative comparators, which use positive feedback of a latch to force a fast decision, are used for many applications. In [1] a 10GHz 3-stage comparator in 1.2V 0.11 μ m CMOS is presented and is designed to extract every 4th bit of a 40Gb/s data stream. A BER<10⁻¹² for V_{pp} at the input is achieved. Depending of the intended application, the constant tail current and the low-voltage swing of the CML blocks may or may not be beneficial. In [2] a latch-type sense amplifier (in 1.5V 0.13 μ m CMOS) for use in SRAMs is investigated. The delay time is 119ps for an input voltage difference of 100mV. A disadvantage is that for proper operation a sufficiently large supply voltage is needed due to the stack of transistors and therefore the comparison time is longer than 11ns at 0.7V. In [3] a comparator with similar circuit structure in 1.8V 0.18 μ m CMOS is described, consuming 350 μ W at 1.4GHz. The standard deviation of the offset without compensation is $\sigma=31.6$ mV. The sense-amplifier presented in [4] (1.2V 90nm CMOS, 225 μ W @ 2GHz) also consists of a typical latch with two cross-coupled CMOS inverters. The comparator in [5] (1.5V 0.12 μ m CMOS, low-threshold transistors) reaches a sensitivity (BER=10⁻⁹) of 16.5mV @ 4GHz/1.5V and 25.8mV @ 500MHz/0.5V. The design of the latch still needs static current and so 2.65mW is needed at 6GHz/1.5V.

The schematic of the comparator described in this paper is shown in Fig. 19.4.1. The comparator is fabricated in a 1.2V 65nm low-power CMOS process with V_r=0.4V. In contrast to a conventional latch (see Fig. 19.4.2), which consists of two cross-coupled inverters (N0, P0 and N1, P1), the presented latch is expanded into two paths between the supply rails so that only the threshold voltage of one transistor (instead of two) has to be overcome in each path. A clock period consists of a reset phase (CLK=CLKA=CLKL=V_{SS}), which builds up a start condition (OUT=OUT'=V_{CO} and FB=FB'=V_{SS}) to compare voltage V_{i+} at CINP with V_{i-} at CINN in the following comparison phase (CLK=V_{CO}). During reset, transistors N2 and N9 are switched off and reset transistors P2 and P3 pull both output nodes OUT and OUT' to V_{CO}, which in succession turn P4 and P5 off and nodes FB and FB' are discharged to V_{SS} by N3 and N4, which are switched on. The gates of transistors N7 and N8 are also at voltage level V_{CO}, so that N7 and N8 are initially switched on, when comparison phase starts. For comparison, N2 and N9 are turned on (CLK=CLKA=CLKL=V_{CO}) and P2, P3, N3 and N4 are switched off. If V_{i+>V_i-}, then OUT is discharged with transistor N6 more than OUT' with N5 and positive feedback is started. OUT' is pulled towards V_{SS} by N6 and N1 more than OUT by N5 and N0 thus P4 is turned on before P5 and FB is pulled towards V_{CO} while FB remains near V_{SS} for sufficient IV_{i+-V_i-}. Hence, P1 and N0 are switched off, P0 and N1 are on, OUT is pulled to V_{CO}, OUT' to V_{SS}, and FB is at V_{CO}. The decision is done and no static current flows. Transistors N7 and N8 avoid static current flow through the input part via N9 [5], because N7 is turned off due to OUT=V_{SS}. For the case when V_{i+<V_i-}, OUT is pulled to V_{SS} and OUT' to V_{CO}. Due to the separated p-well (triple-well process) of NMOS transistors, the body effect can be used to reduce the threshold voltages of transistors N5 to N8 by setting PWELL to maximum 0.7V. According to Monte-Carlo simulations on 50 samples, the standard deviation of the comparator offset is $\sigma=22$ mV at V_{CO}=1.2V and $\sigma=47$ mV at V_{CO}=0.6V.

The comparison of the presented latch with a conventional latch, which is used in typical comparators, is shown in Fig. 19.4.2. In this simulation, the input stage of Fig. 19.4.1 (transistors N5 to N9) has been connected to each latch. The diagram shows the simulated delay time (50% rising edge of CLK to the time point when IOUT-OUT' has reached 50% of V_{CO}) of both latches versus the supply voltage V_{CO}. Both latches are designed to have the same delay time at V_{CO}=1.2V. If the supply voltage is reduced, then the increase in the delay time of the conventional latch is much more than that of the presented latch (3ns as compared to 0.9ns at V_{CO}=0.6V).

The block diagram of the test chip with the comparator is shown in Fig. 19.4.3. The chip is divided into 2 parts, one with a supply voltage of V_{DD}=1.2V for optimal functionality of CMOS logic (included for measurement purposes), and a second with the supply voltage of V_{CO} where the comparator is placed. The clock is applied to CLKIN and is processed by the clock driver to 2 complementary square-wave clock signals (CLK, \bar{CLK} , duty cycle $\sim 50\%$) with the logic levels V_{SS} and V_{CO}. Each adapter consists of two separately supplied inverters to convert the logical levels V_{CO} and V_{SS} to levels V_{DD}=1.2V and V_{SS}. During reset phase of the comparator the transmission gate P6/N10 is closed and the decision is held in the transfer stage dynamically at node SHB. With digital pin DIG, it can be chosen whether transmission gate N11/P7 is always open or only open when the transmission gate P6/N10 is closed for achieving a constant delay time at the chip outputs to simplify delay adjustments for BER measurements. With the addition of block T-Gates the possibility of sensitivity tuning [6] for lower clock rates is added, where the currents through transistors N2 and N9 in Fig. 19.4.1 can be controlled with bias voltages at NA and NL, when PM=V_{DD}. When the transmission gates are completely open (NA=NL=V_{DD}, PM=V_{SS}), then CLK=CLKA=CLKL and sensitivity tuning is off.

BER measurements are done by applying a bias voltage at CINP, which is superimposed with a 2³¹-1 PRBS and a reference bias voltage at CINN. For measurements CINN and CINP are biased separately for offset compensation. Here the amplitude is defined by IV_{i+-V_i-+offset}. The left side of Fig. 19.4.4 shows the measured BER versus the bias level at CINN. The optimal operating point (lowest BER) is for V_{CO}=1.2V at 0.6V and for V_{CO}=0.6V at 0.5V. For these optimal points, the dependence of the BER to the amplitude is measured (right side of Fig. 19.4.4). To achieve BER=10⁻⁹ at V_{CO}=1.2V, an amplitude of 15mV @3GHz, 20mV @4GHz (sensitivity tuning @3GHz and 4GHz), 27.2mV @5GHz, 63mV @6GHz and 281mV @7GHz has to be applied. If V_{CO} is lowered to 0.6V (T-Gates completely open), 16mV @500MHz and 90.2mV @700MHz are measured. The measured power consumption is 1.3mW @1.2V/7GHz, 1.19mW @1.2V/6GHz, 41 μ W @500MHz/0.6V and 47 μ W @700MHz/0.6V. Compared to [5] an improvement of more than 50% in power consumption has been achieved at 6GHz.

The delay time (see Fig. 19.4.5) of the comparator (64ps @CINN=0.6V, 18.6mV amplitude) is measured with an additional on-chip circuit (measurement circuit and comparator delay time variation have $\sigma=11$ ps) for detecting the time shift between CLK and OUT'. It can be seen, that the measured result is similar to the simulated one. At lower input amplitudes, the measurements are influenced by more random switching of the comparator.

Figure 19.4.6 shows oscilloscope screenshots at 7GHz clock frequency. A micrograph of the test chip is shown in Fig. 19.4.7. The comparator occupies 19.6×16.3 μ m².

Acknowledgement:

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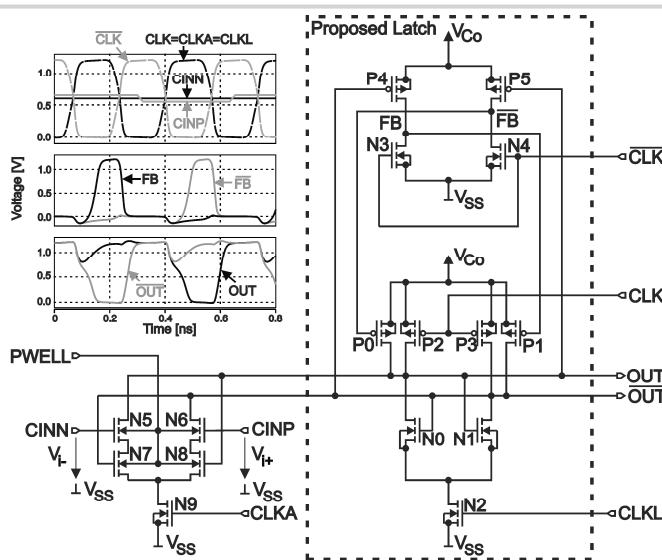


Figure 19.4.1: Schematic of the comparator.

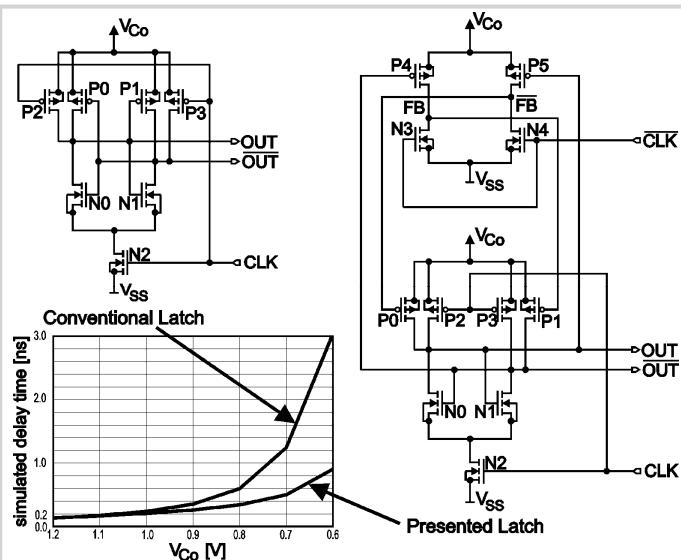


Figure 19.4.2: Comparison of the conventional latch with the presented latch.

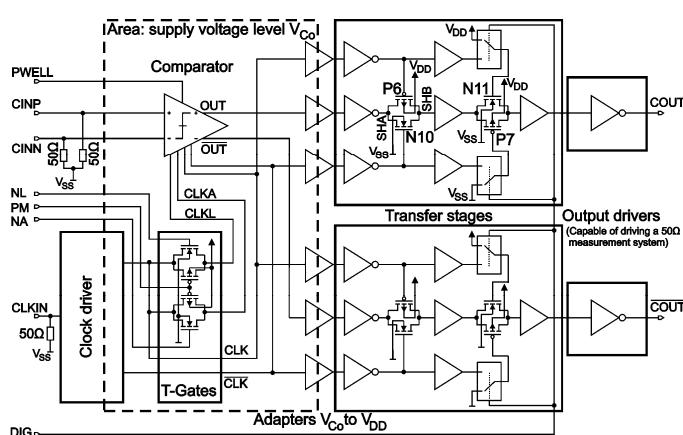


Figure 19.4.3: Block diagram of the test chip with the comparator.

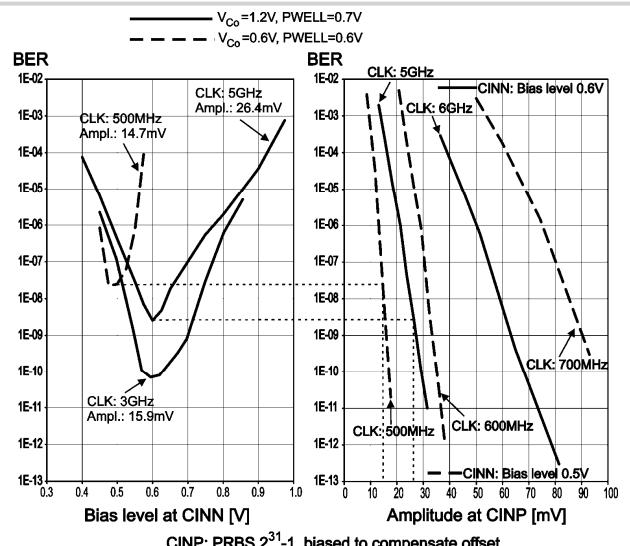


Figure 19.4.4: BER measurements with PRBS $2^{31}-1$.

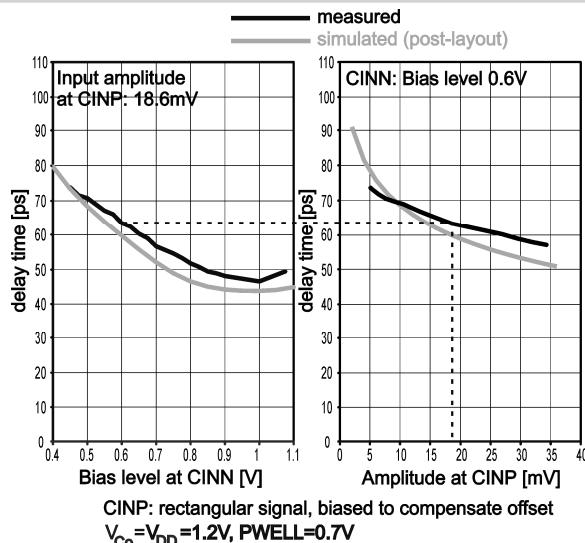


Figure 19.4.5: Measured delay time of the comparator.

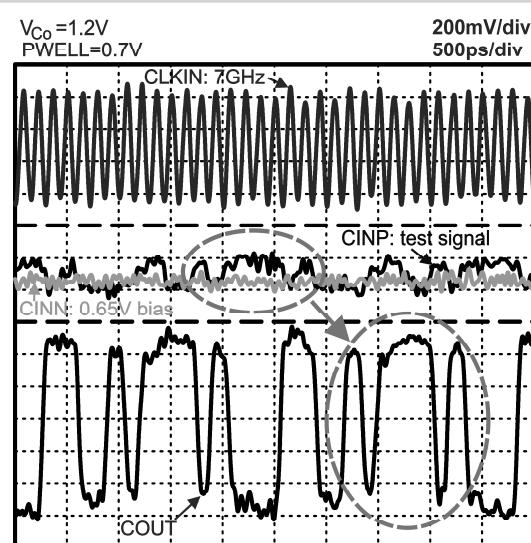


Figure 19.4.6: Oscilloscope screenshots (7GHz clock frequency).

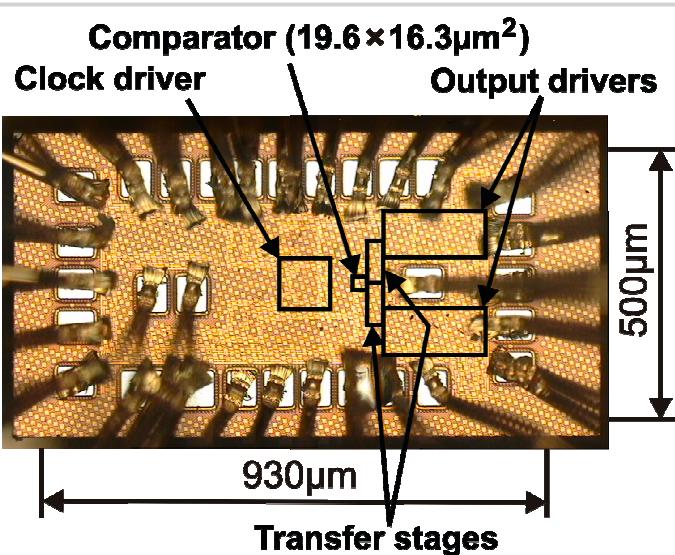


Figure 19.4.7: Micrograph of the test chip.