

# Synthesizing and Simulating Verilog code

Using Xilinx Software

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# Xilinx ISE 14.6

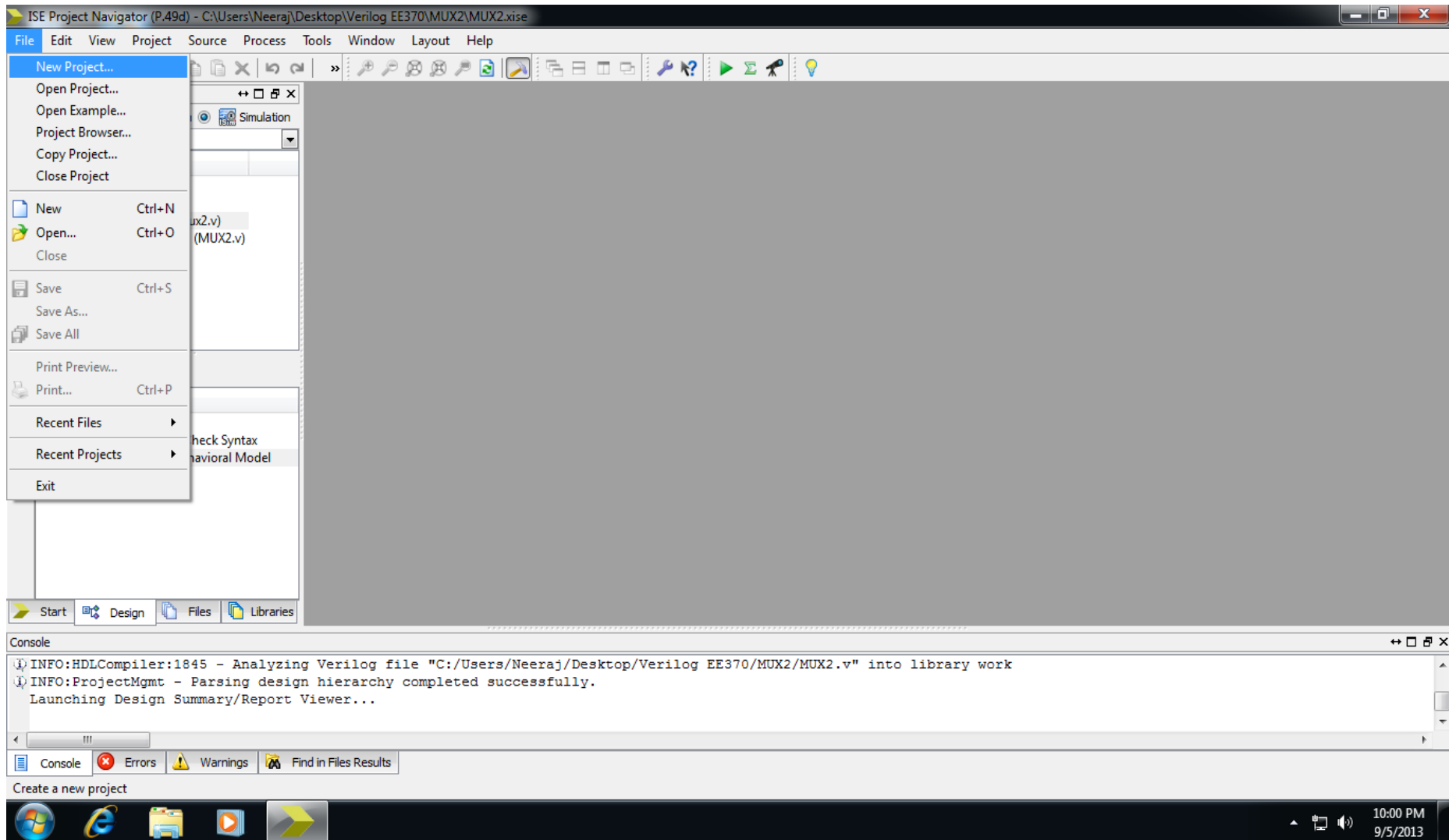
- Download link-

<http://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/design-tools.html>

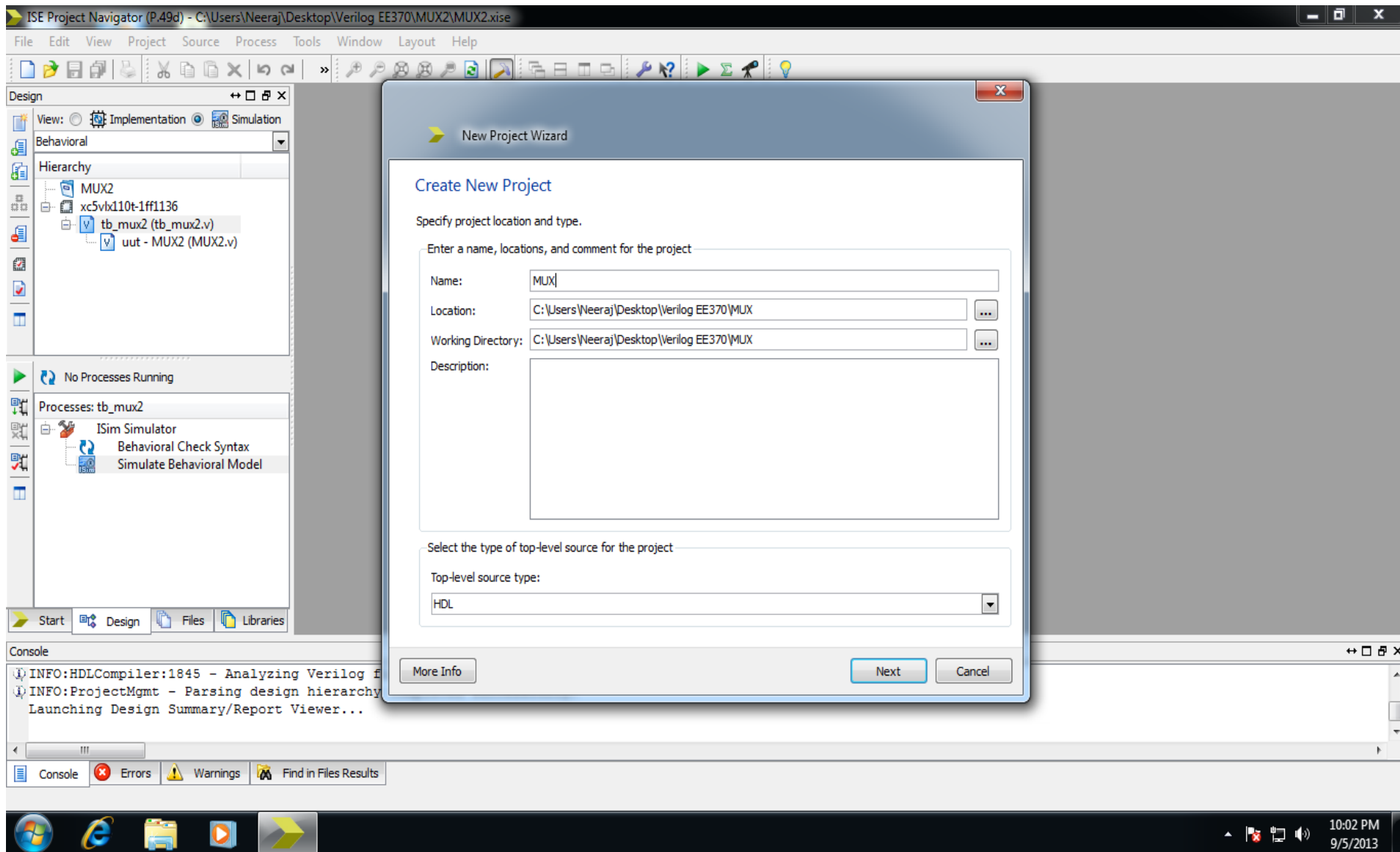
- Choose the Full Installer for Windows
- You need to register on their website.
- Install the software. When it prompts for licence choose WebPack Licence which is available for free.
- Note: Preferable install it in Windows 7 environment. Xilinx 14.4 has some annoying bugs when run with Windows 8. I think they still do not support windows 8.

# Open the Xilinx ISE Software

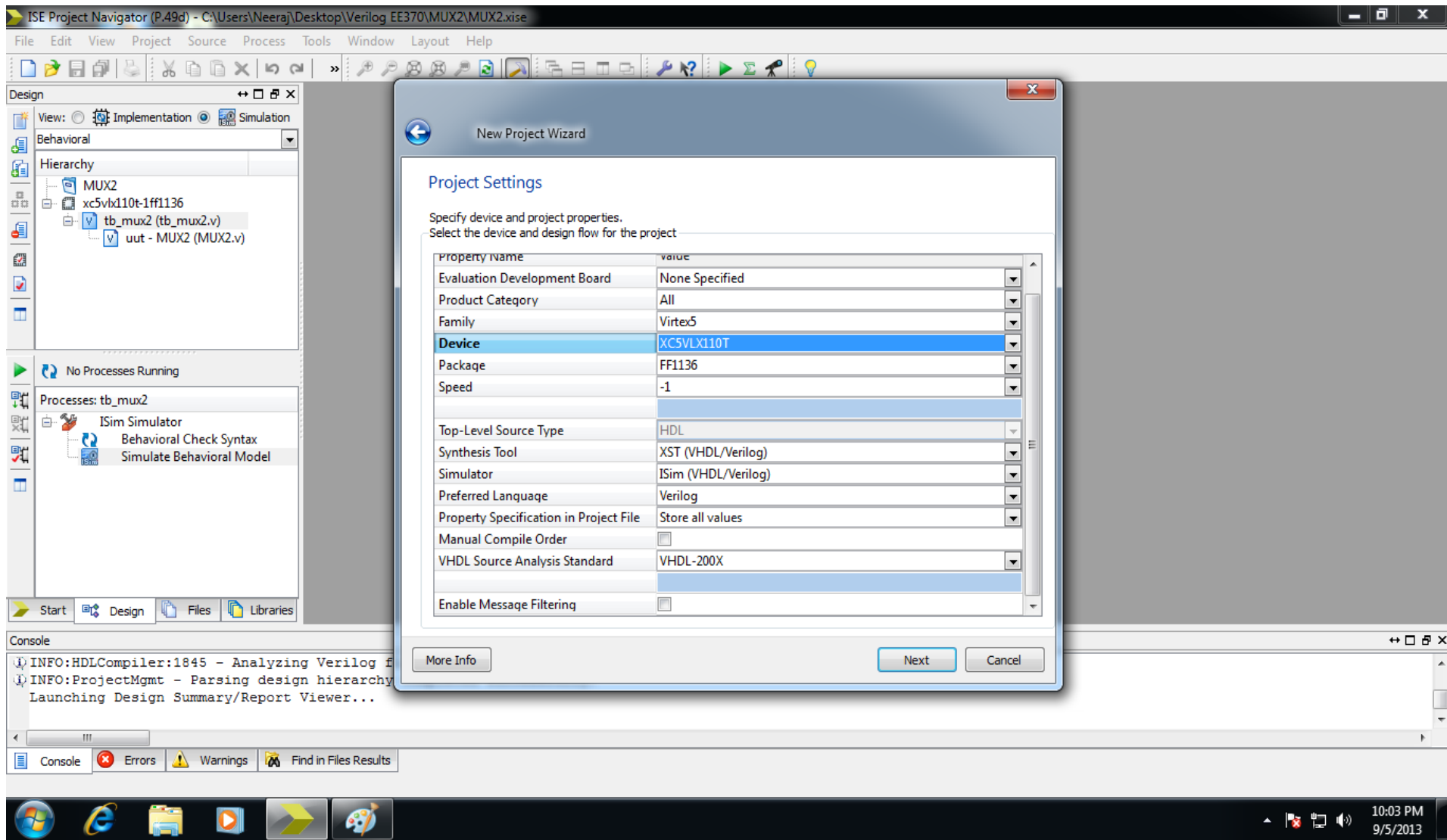
## Open New Project



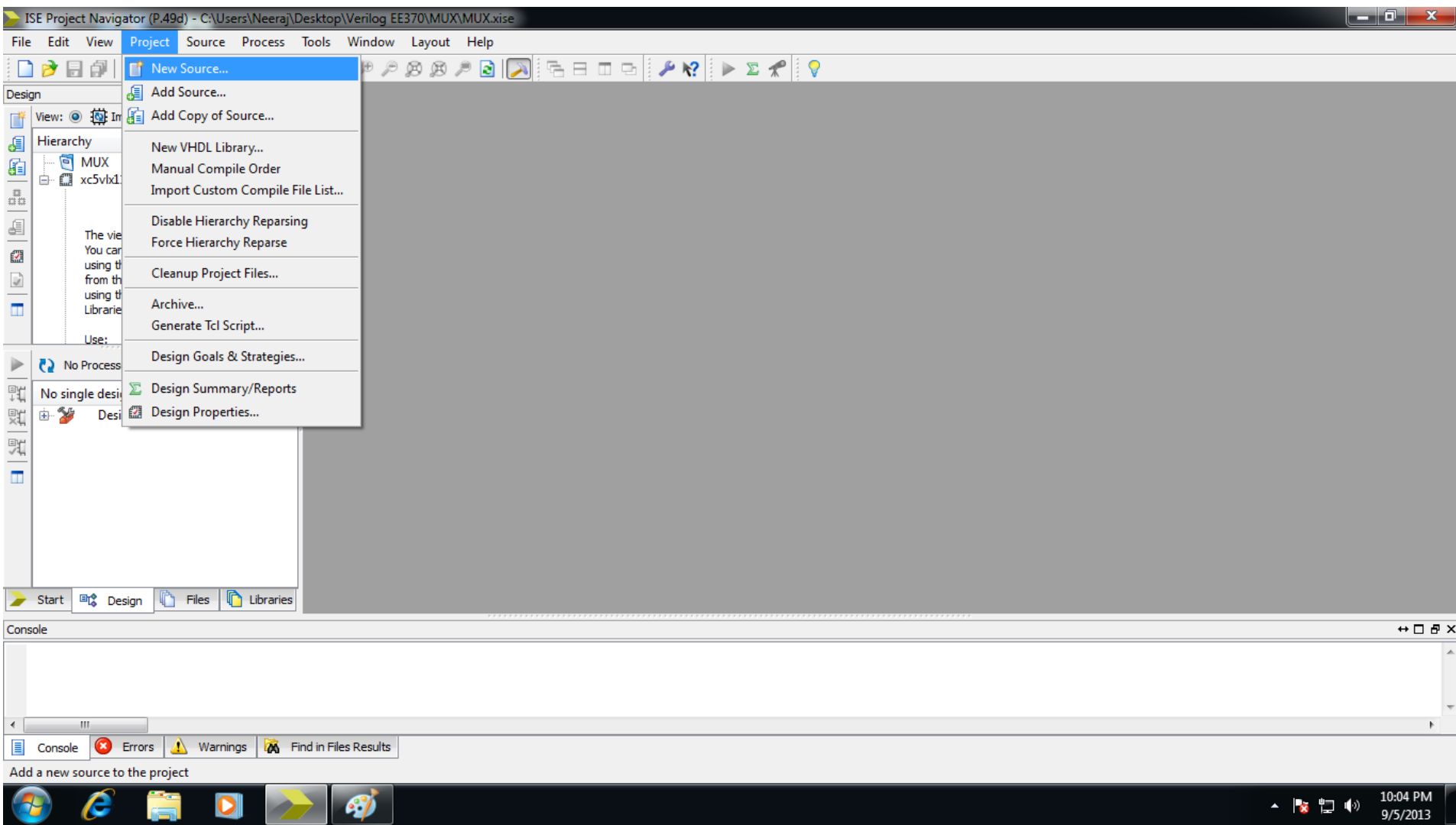
# Choose the location to create New Project



Choose settings as shown as FPGA chosen is available .  
Click Next and then click Finish.

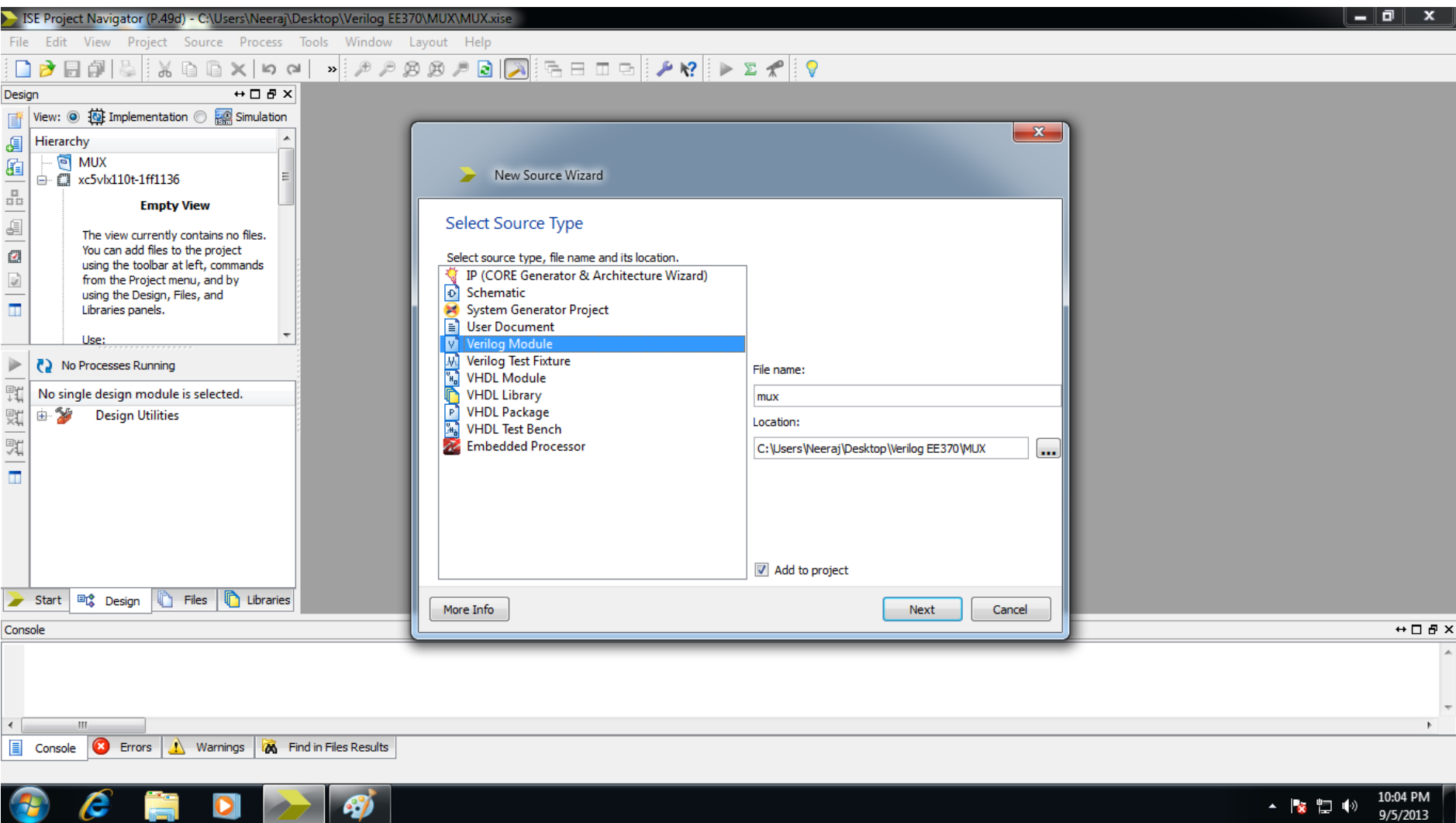


# Create New Source as shown

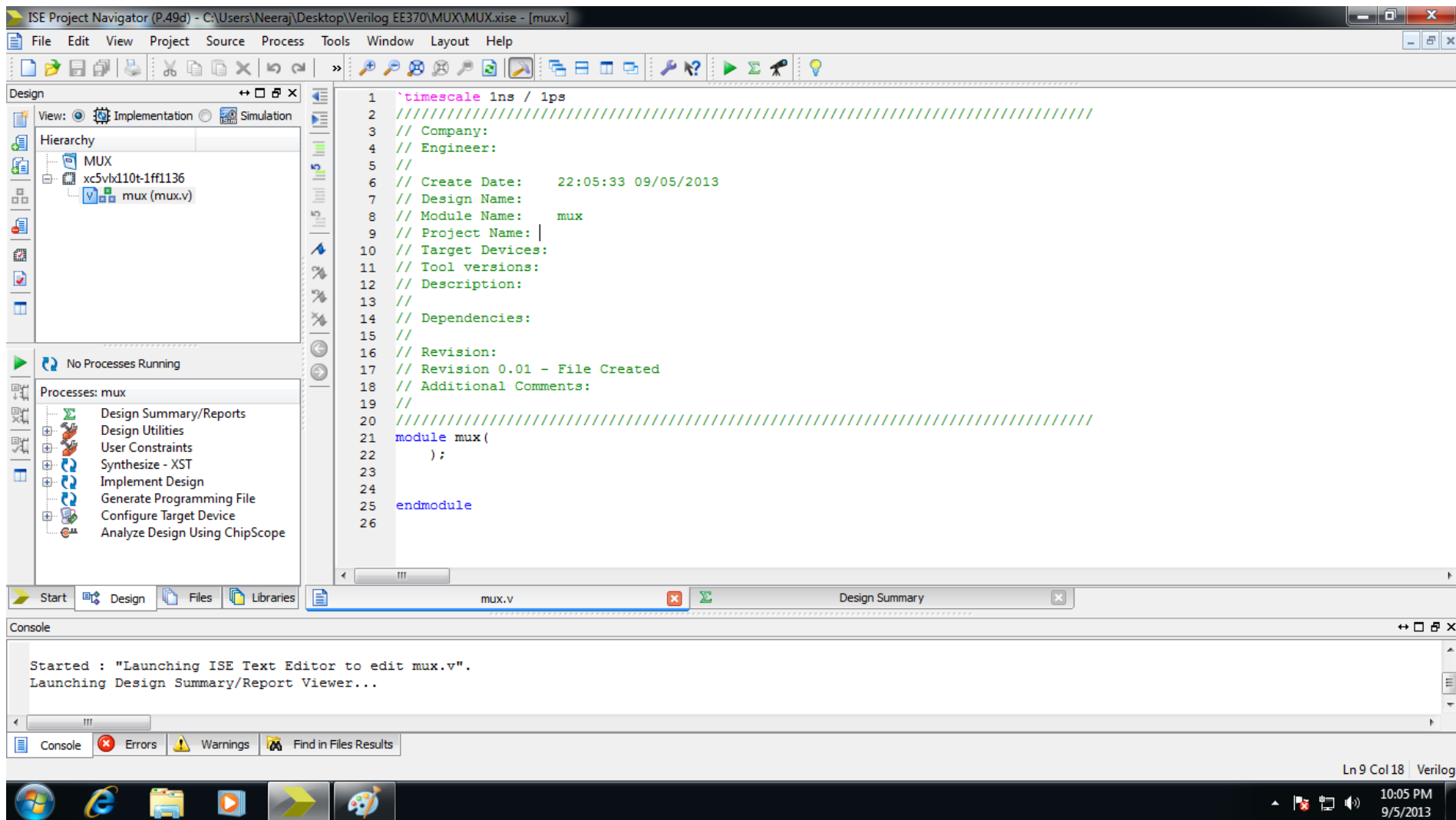


# Select Verilog module.

## Click Next twice and then Finish.



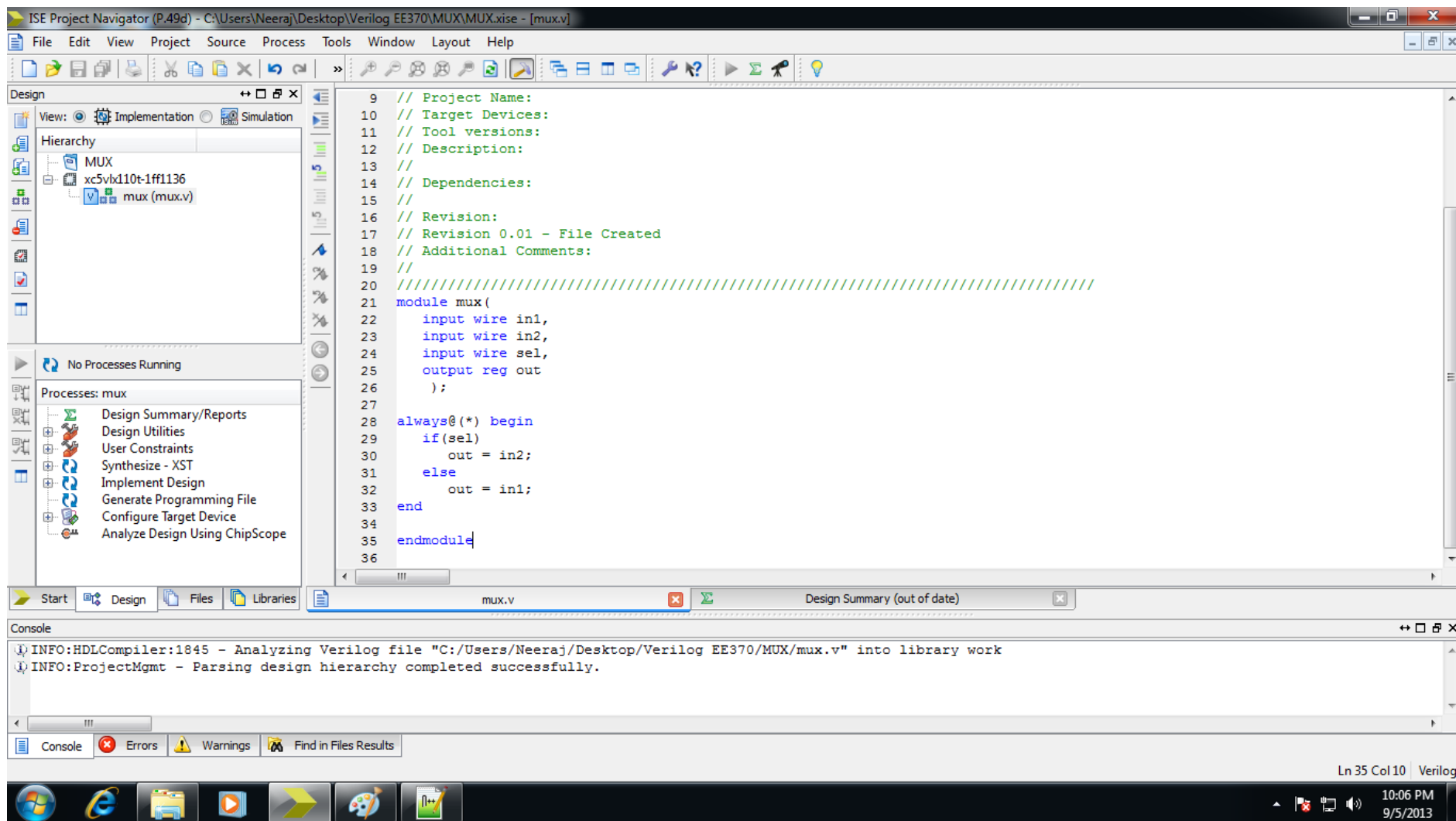
# You can now write your module.



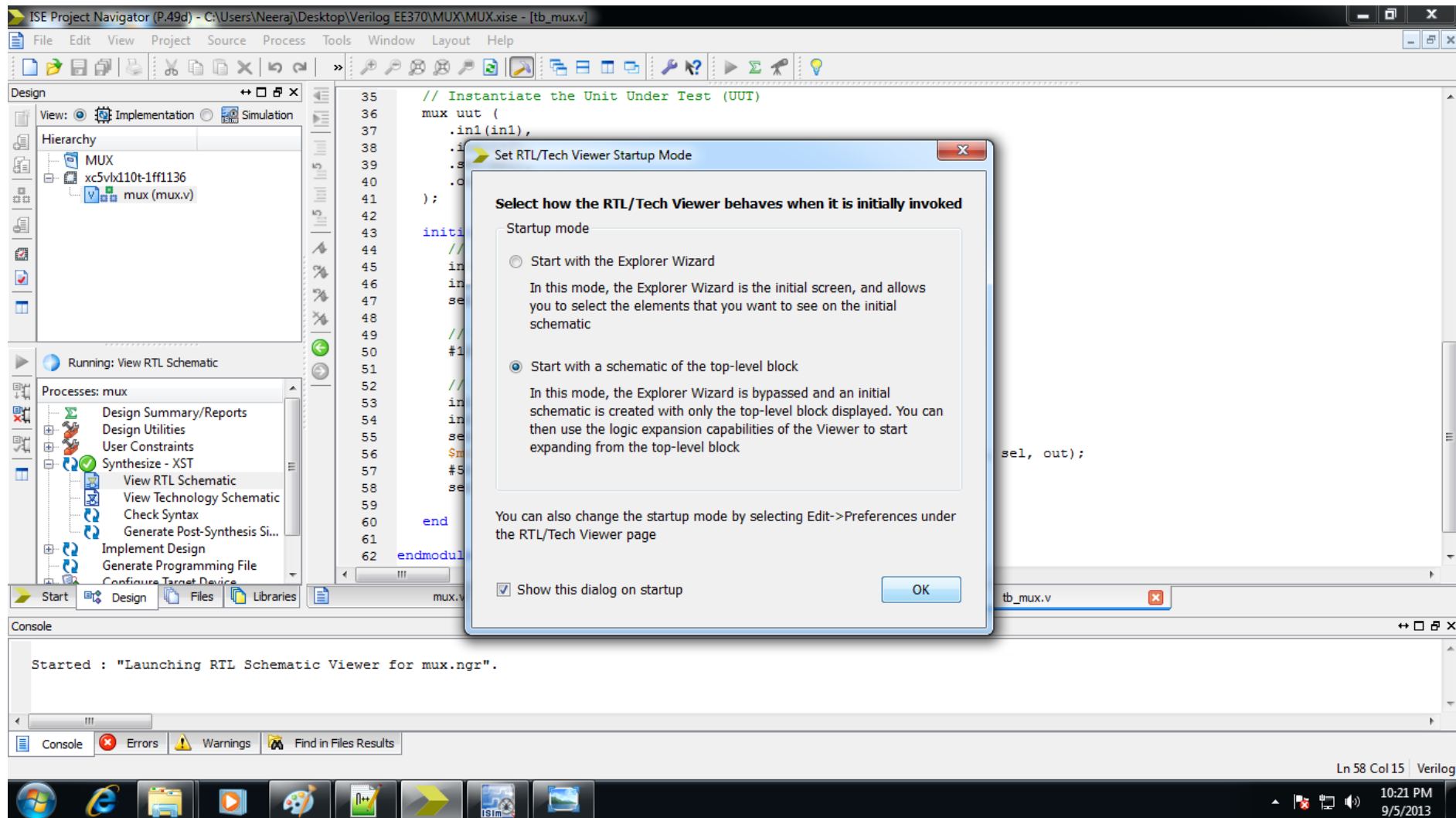


# Code for mux written.

## Double click on synthesize, on the left hand side.



# To see the circuit click on view RTL schematic option and then press ok.



Go on clicking in the black area to zoom in the circuit elements.

The screenshot displays the Xilinx ISE Project Navigator interface. The main window shows the RTL schematic of a multiplexer (mux). The schematic is enclosed in a green box labeled 'mux:1'. Inside, there is a sub-block 'out\_imp:1' which contains three logic gates: 'and2b1', 'and2', and 'or2'. The inputs are 'in1', 'in2', and 'sel'. The outputs are 'out11', 'out21', and 'out3'. The final output is 'out'. A tooltip 'Zoom to Full View' is visible over the schematic area.

The Design Navigator on the left shows the project hierarchy: 'mux' (RTL1) is selected. The 'Processes' panel shows 'Synthesize - XST' as the current process. The 'Design Objects of Top Level Block' panel at the bottom shows the instances 'mux' and 'out\_imp'.

Instances:

- mux
- out\_imp

Pins:

- out
- out\_imp

Signals:

- out
- out\_imp

Properties: (No Selection)

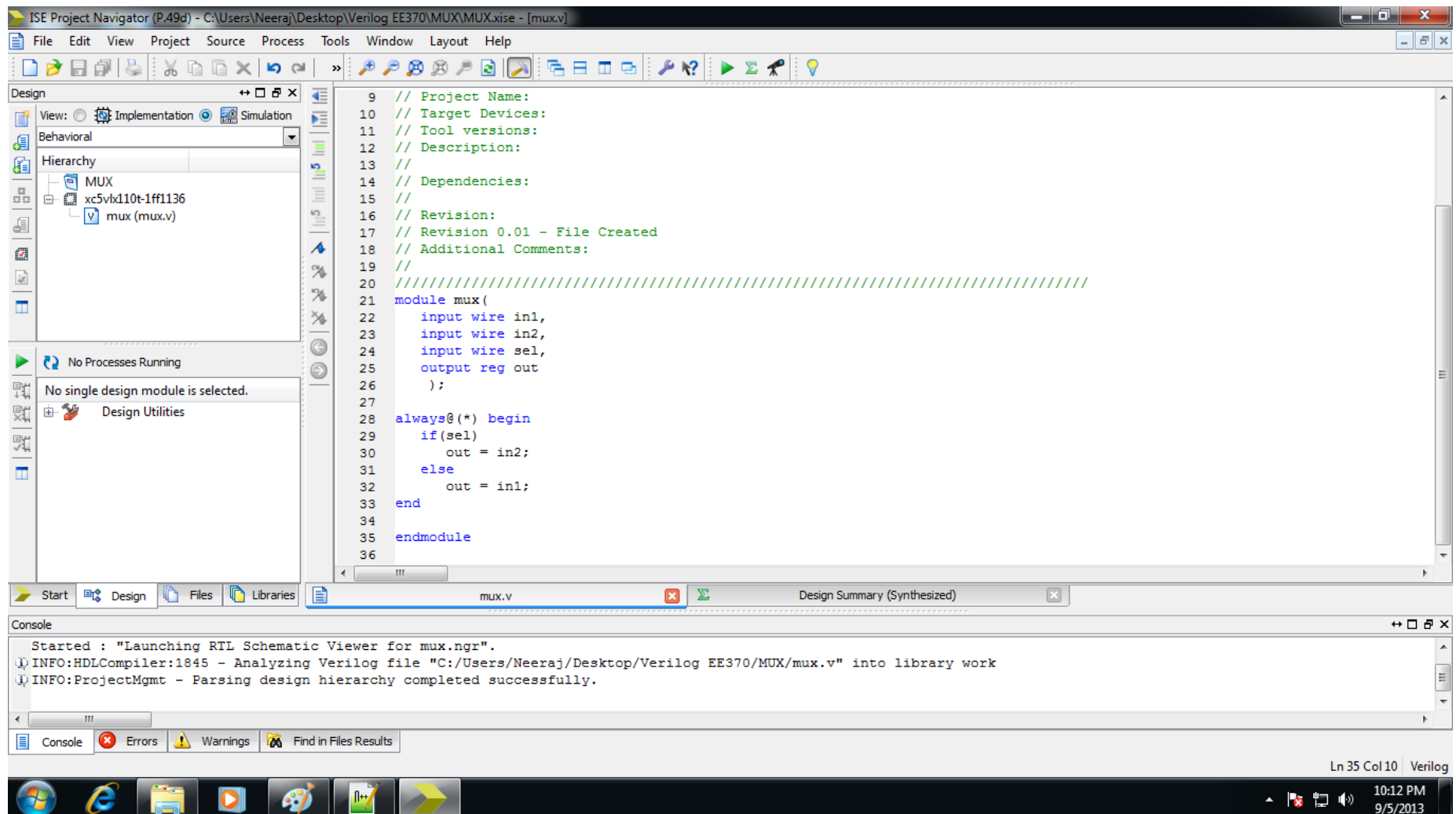
Console, Errors, Warnings, Find in Files Results, View by Category

Set view such that the entire contents is visible

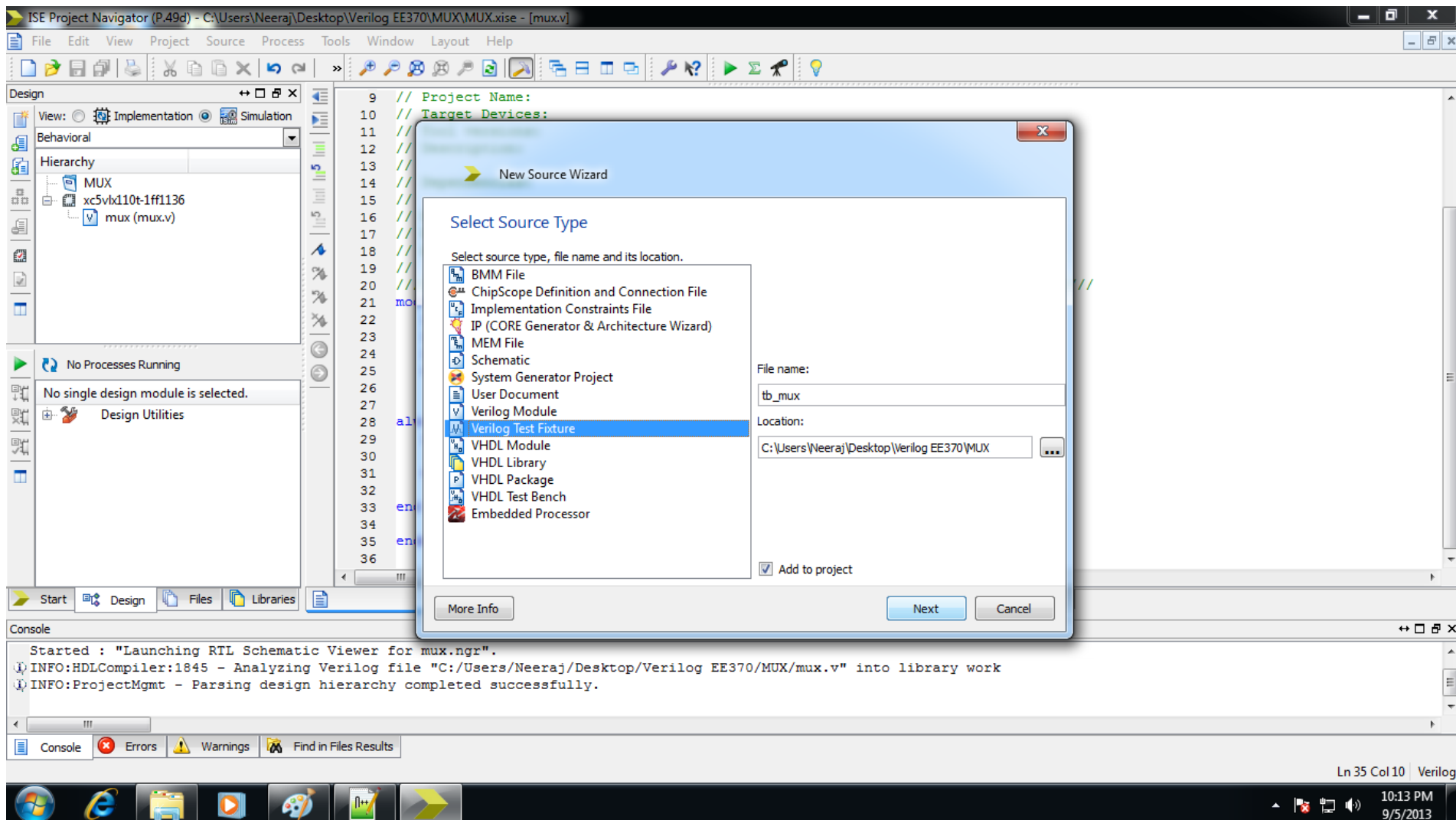
[ -376, -28 ]

10:10 PM  
9/5/2013

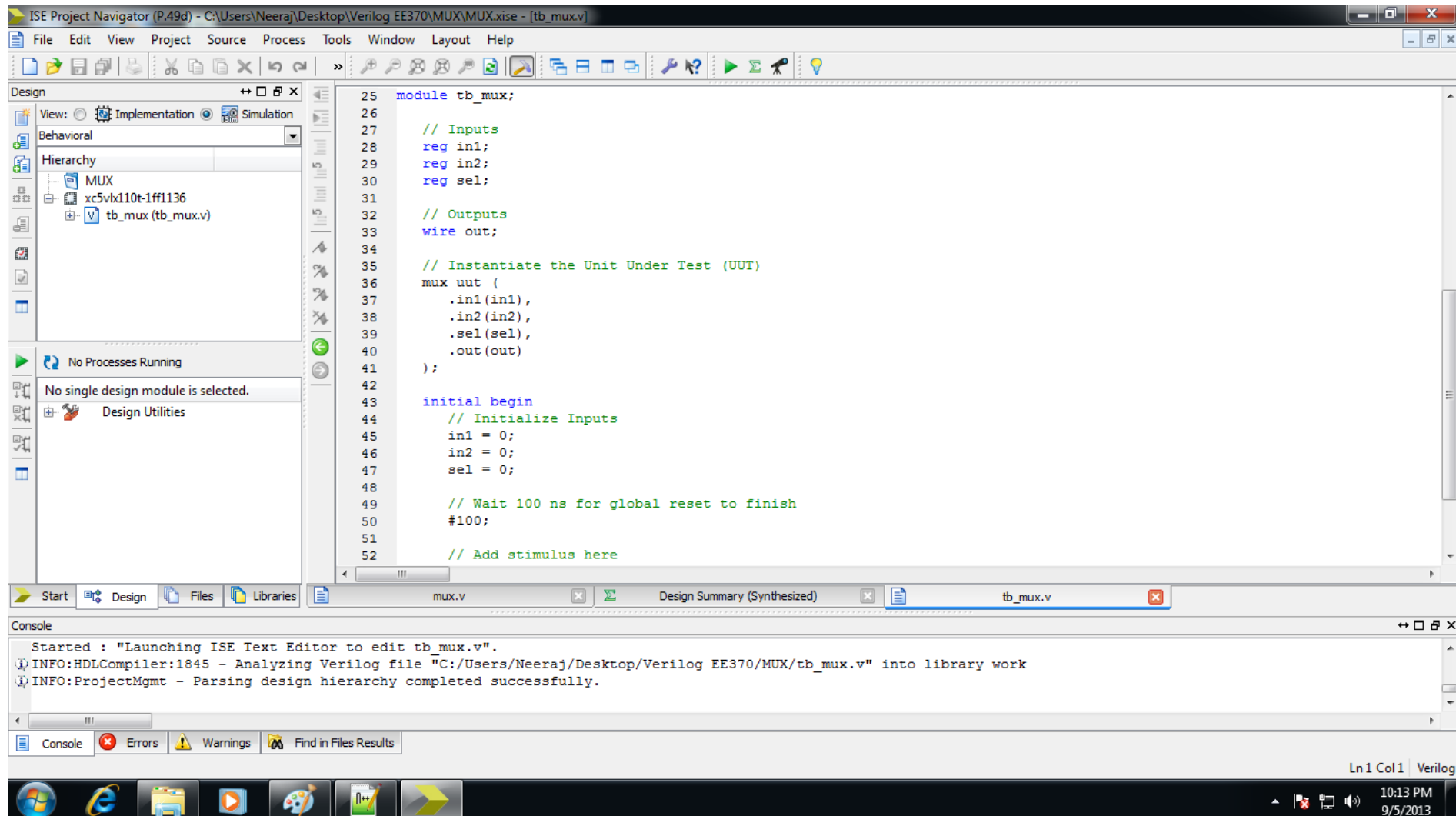
# To run simulation click on Simulation option at the top of left column



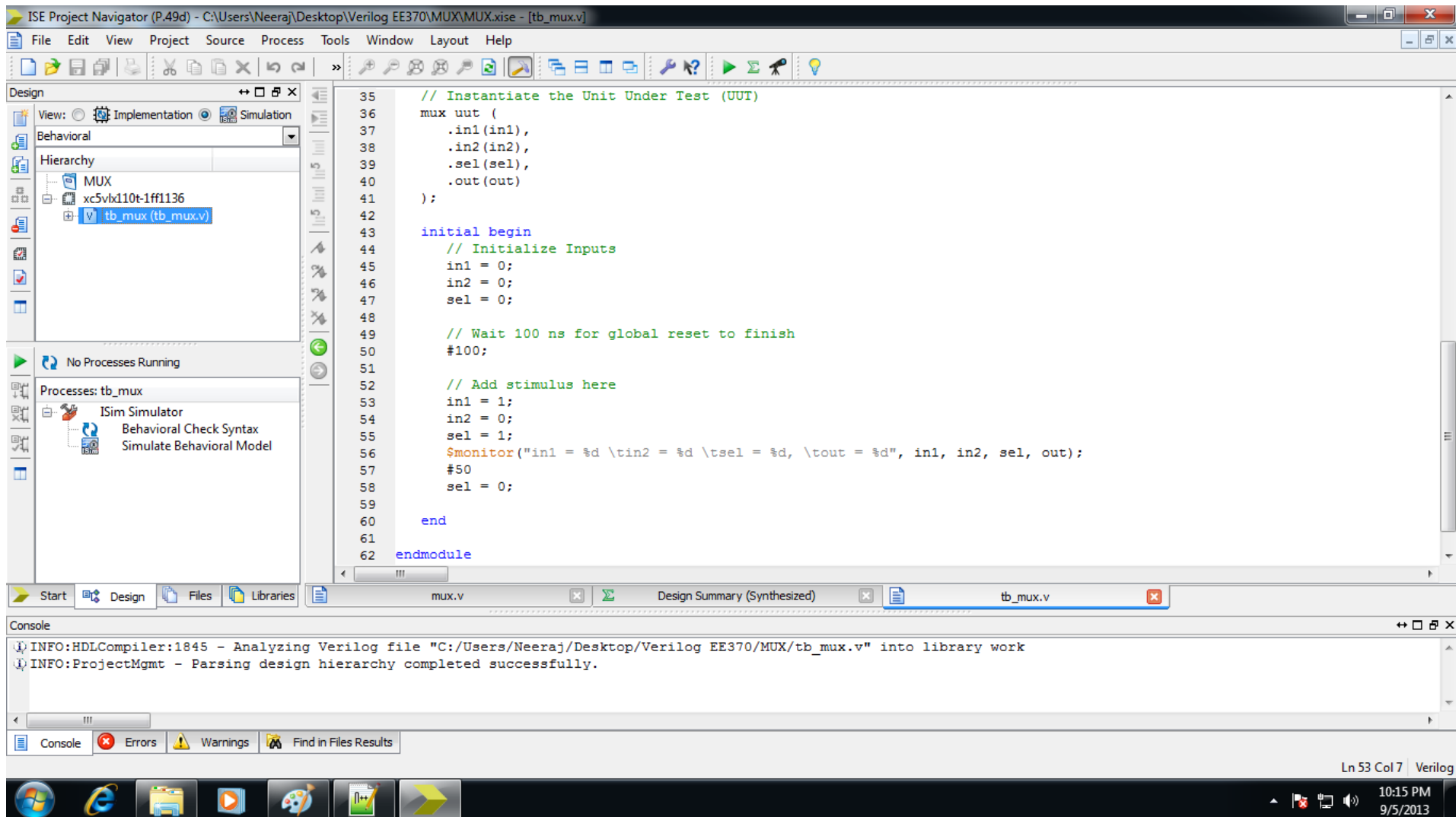
# To create a Test bench, create New Source. Select Verilog Test Fixture



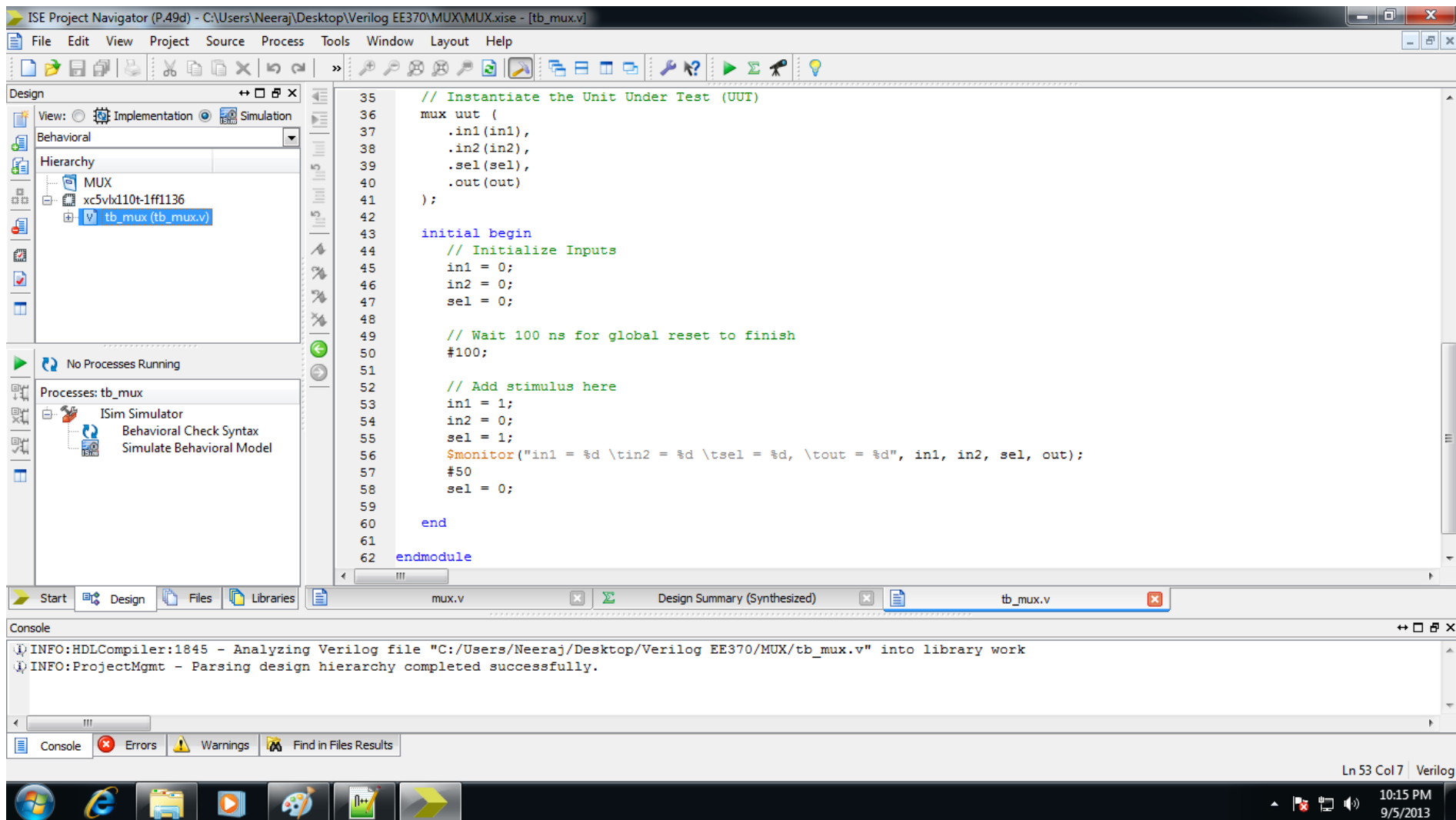
# Template of Test bench will be created instantiating the mux module.



Add the testing code in the initial block below  
Add Stimulus here comment.



# Double click on Simulate Behavioral Model option.





This is the simulation window. You can verify the working using waveforms or using printed statements at the bottom.

The screenshot shows the ISim (P.49d) simulation window. The main area displays a waveform plot for the simulation of a multiplexer (tb\_mux). The plot shows four signals: out, in1, in2, and sel. The time scale is 1.00us, and the total simulation time is 1,000.000 ns. The waveform shows that the output (out) is 1 when in1 is 1 and in2 is 0, and 0 when in1 is 0 and in2 is 1. The select signal (sel) is 0 for the first half of the simulation and 1 for the second half.

The console at the bottom shows the simulation results and status:

```
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
in1 = 1      in2 = 0      sel = 1      out = 0
in1 = 1      in2 = 0      sel = 0      out = 1
ISim>
```

The status bar at the bottom right indicates the simulation time: Sim Time: 1,000,000 ps.