Synthesizing and Simulating Verilog code

Using Xilinx Software

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Xilinx ISE 14.6

- Download link-

http://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/design-tools.html

- Choose the Full Installer for Windows

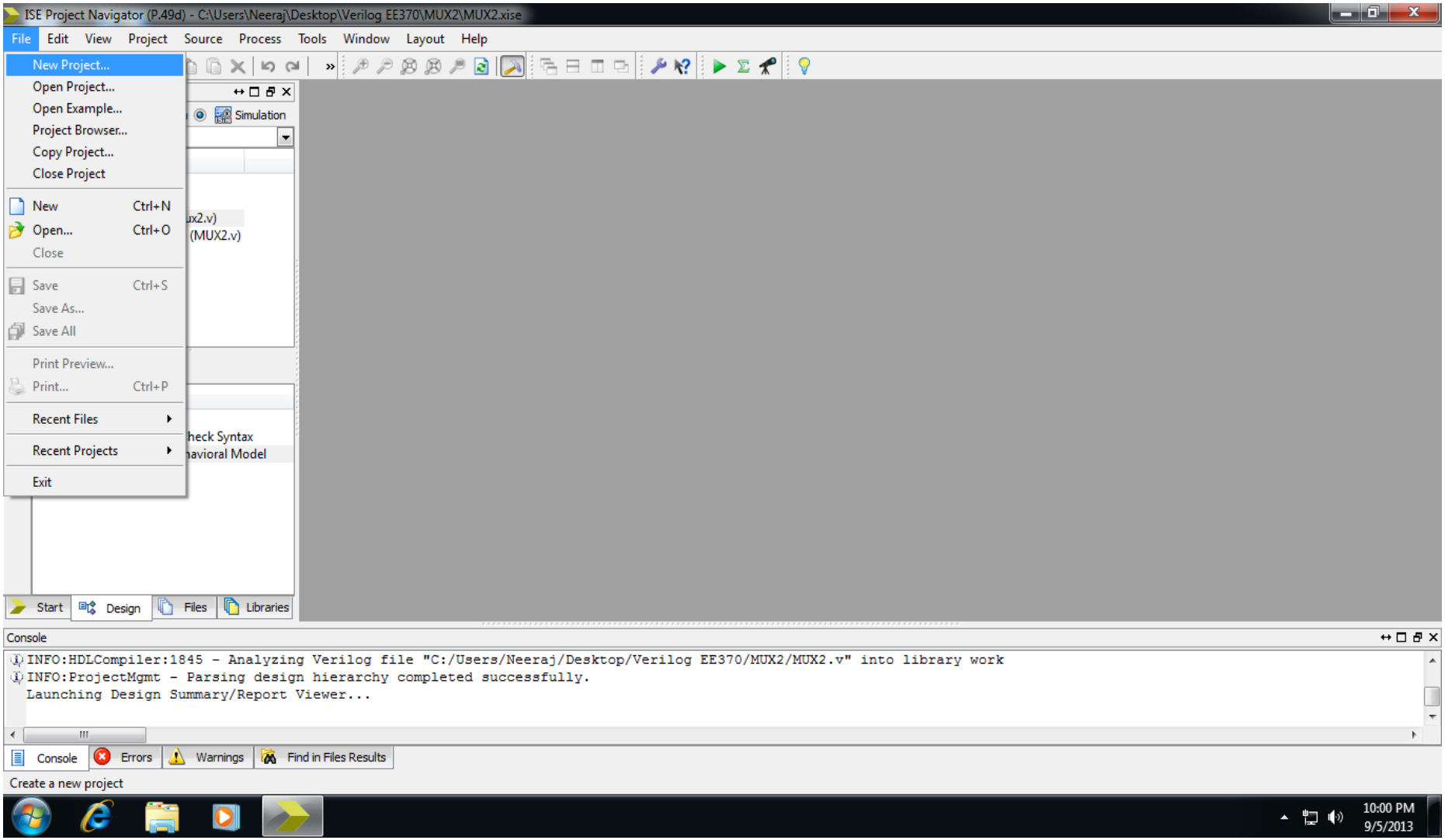
- You need to register on their website.

- Install the software. When it prompts for licence choose WebPack Licence which is available for free.

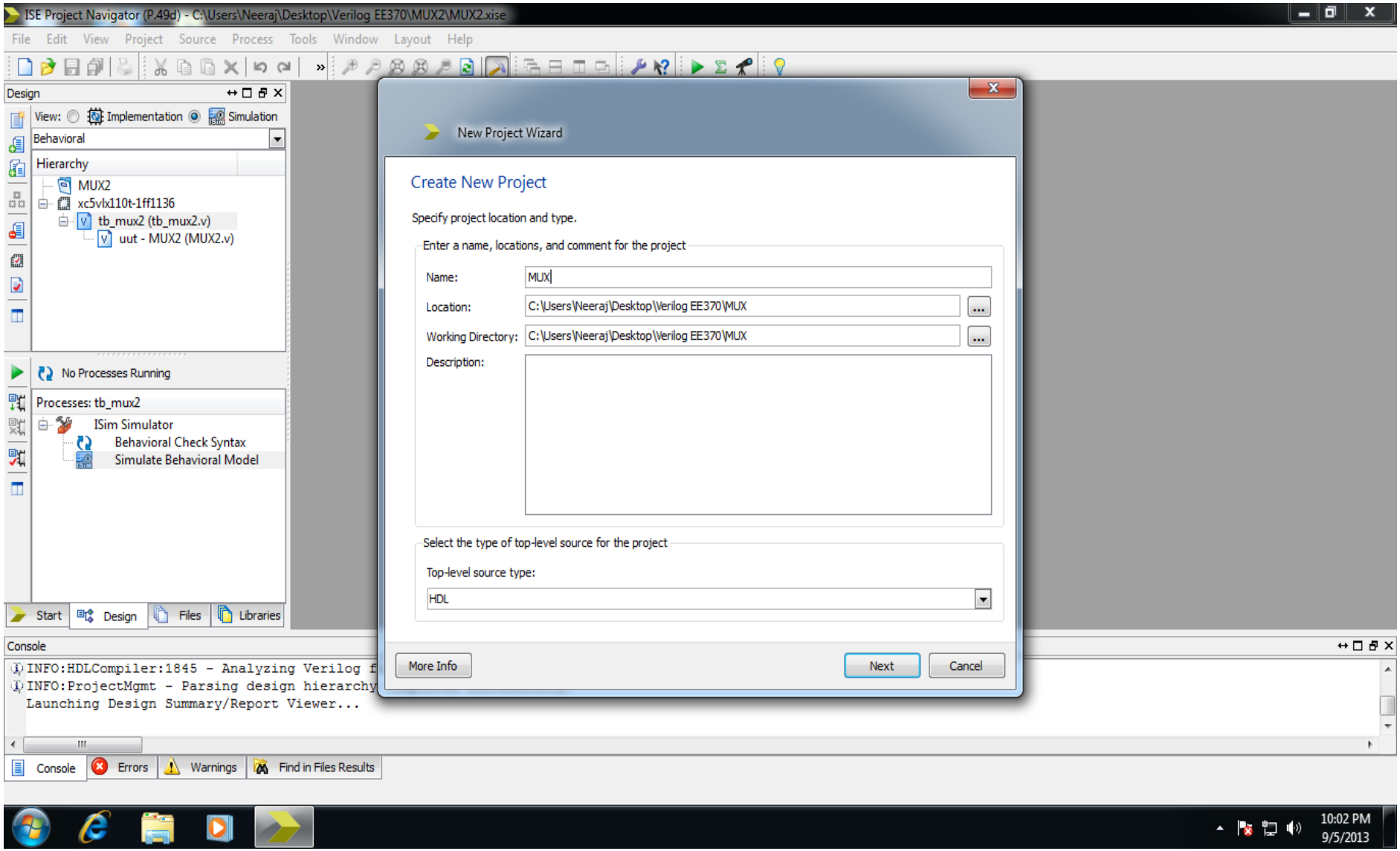
- Note: Preferable install it in Windows 7 environment. Xilinx 14.4 has some annoying bugs when run with Windows 8. I think they still do not support windows 8.

Open the Xilinx ISE Software

Open New Project

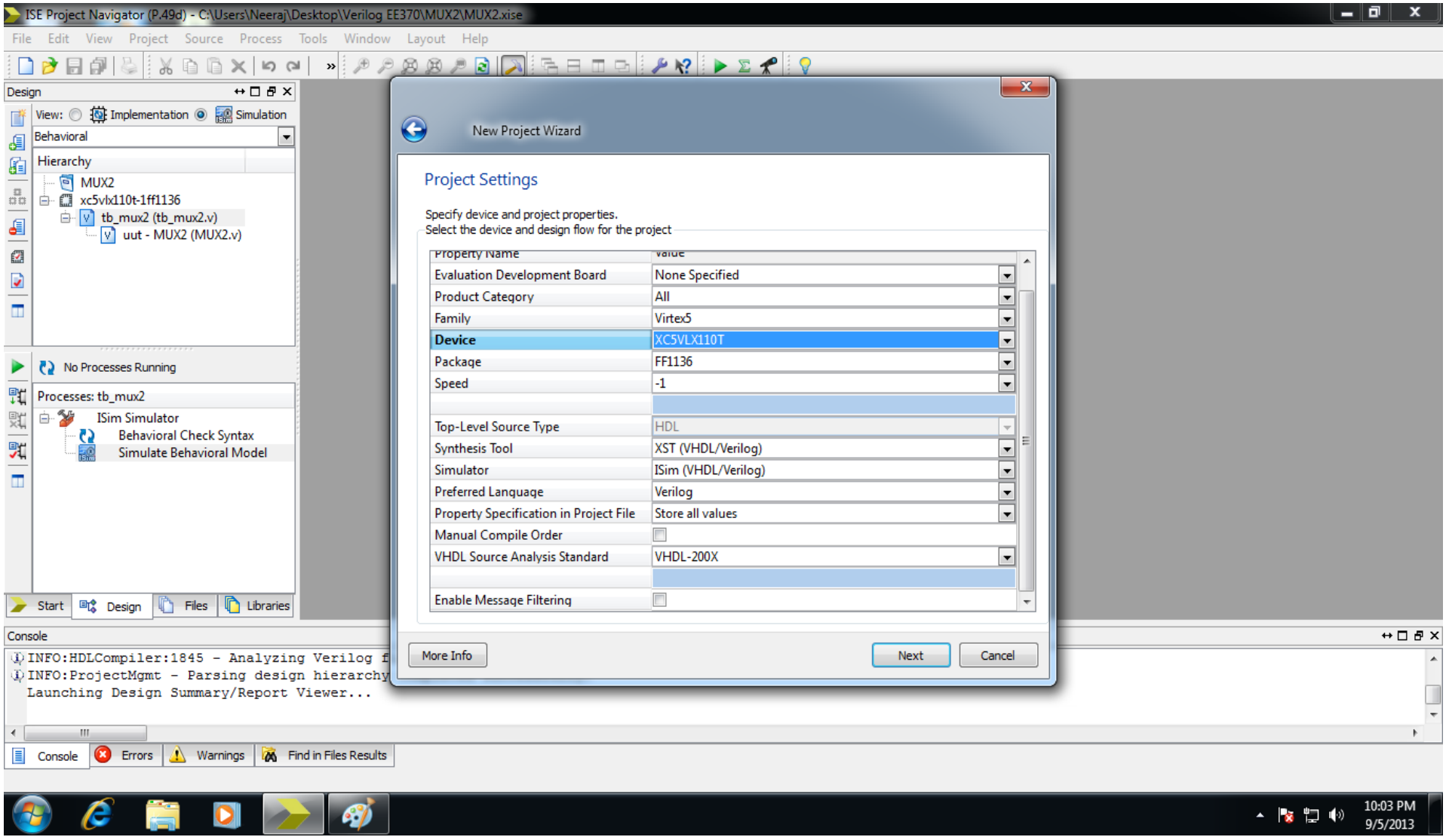


Choose the location to create New Project

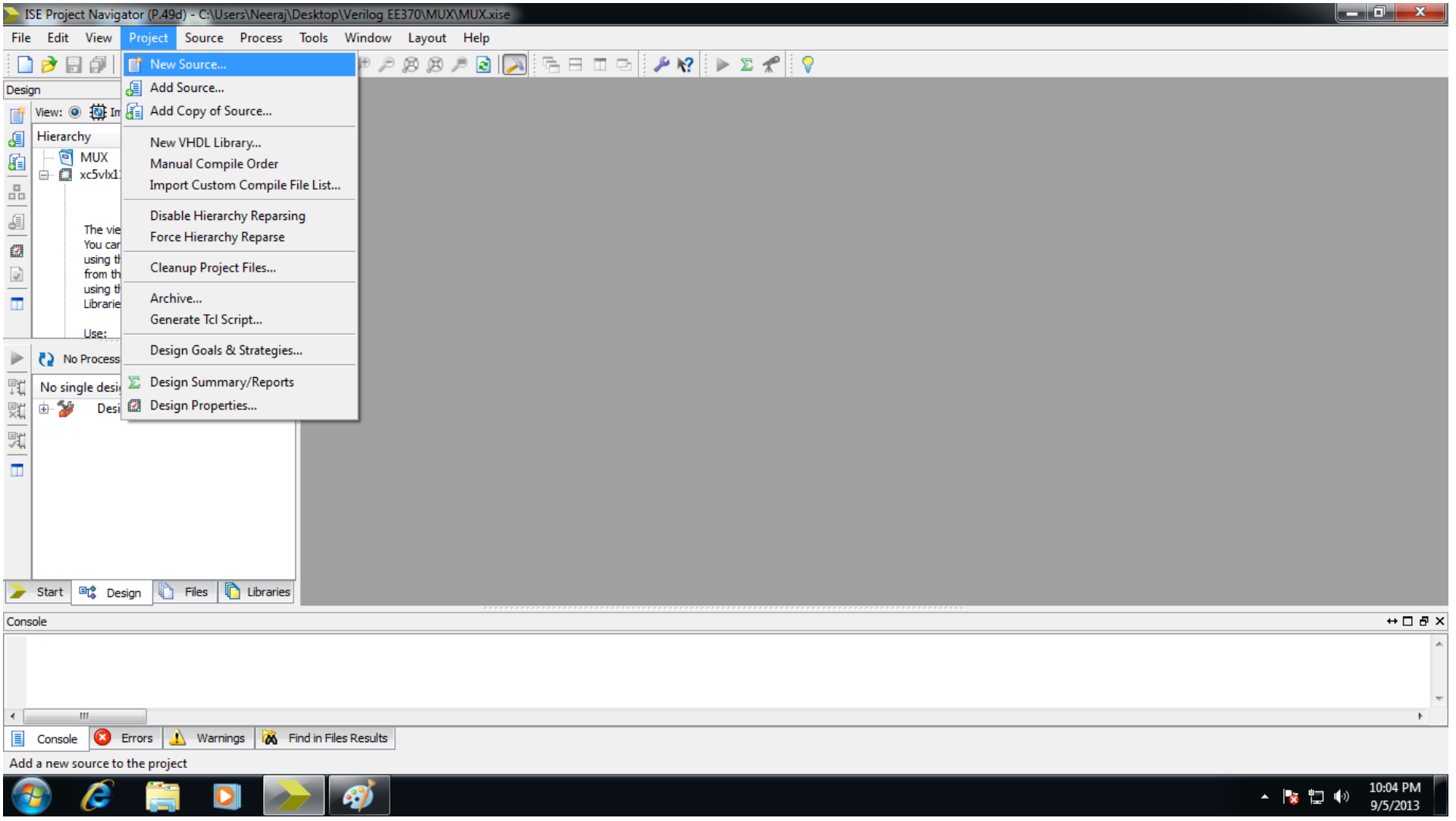


Choose settings as shown as FPGA chosen is available .

Click Next and then click Finish.

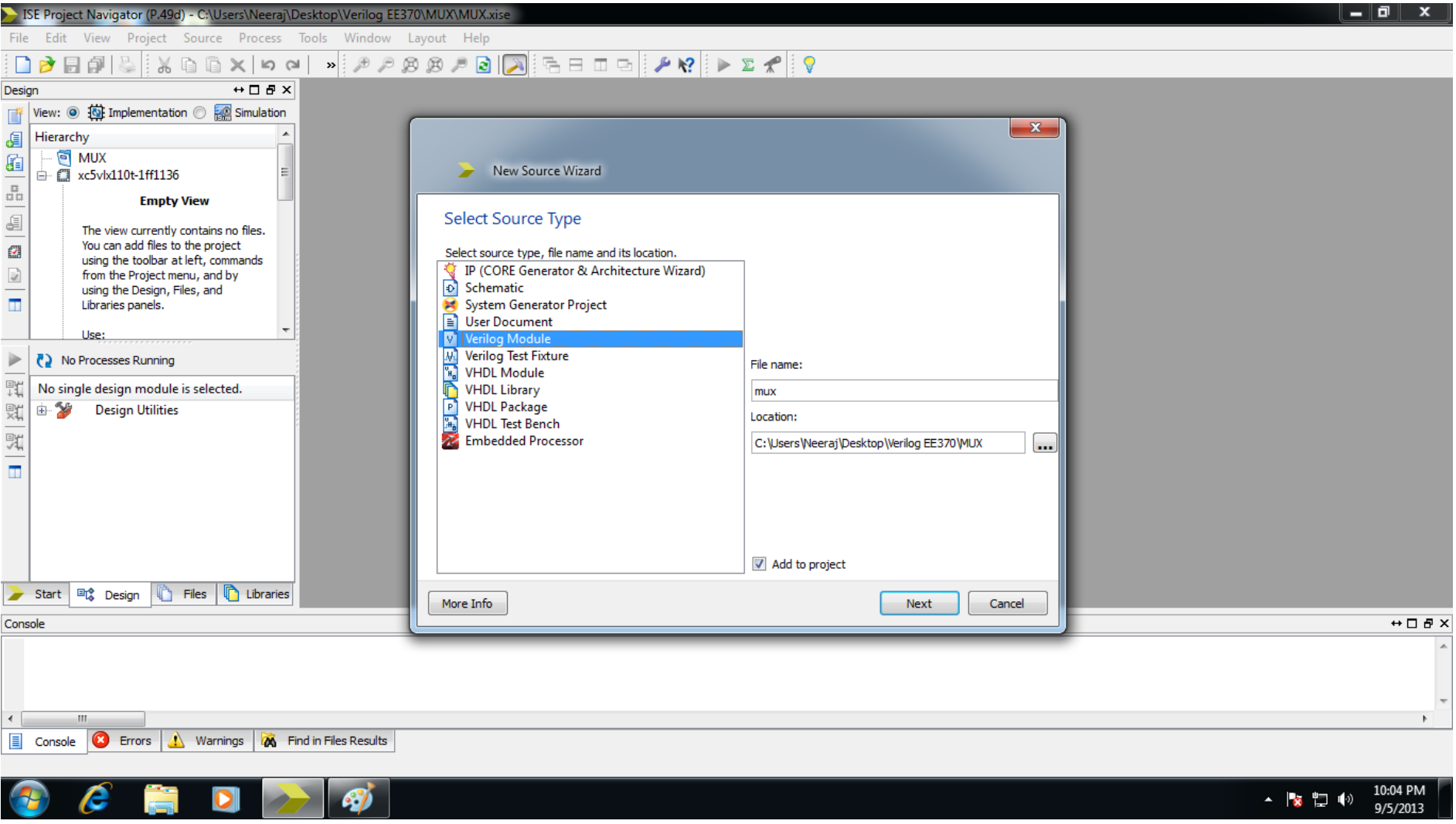


Create New Source as shown

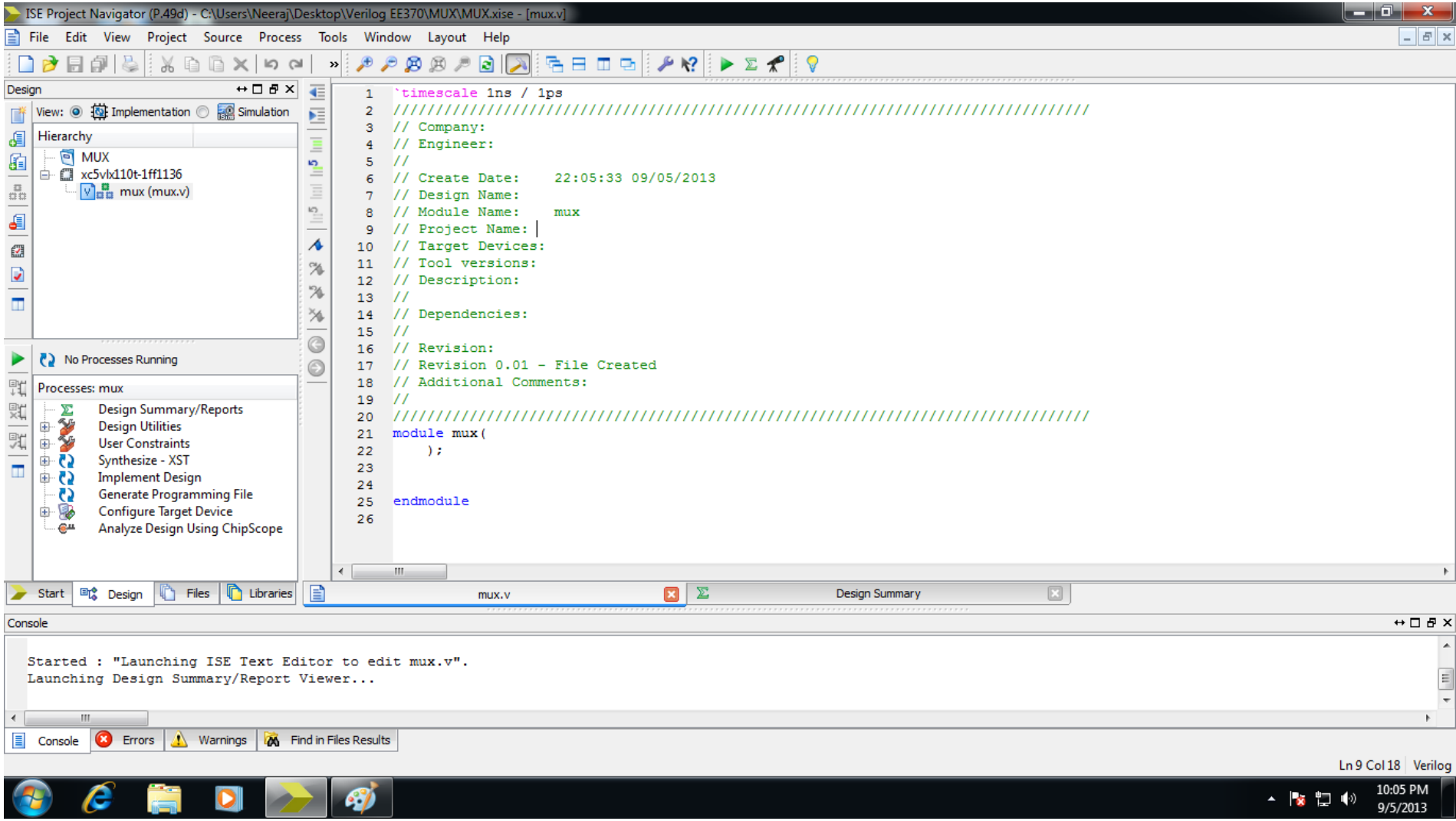


Select Verilog module.

Click Next twice and then Finish.

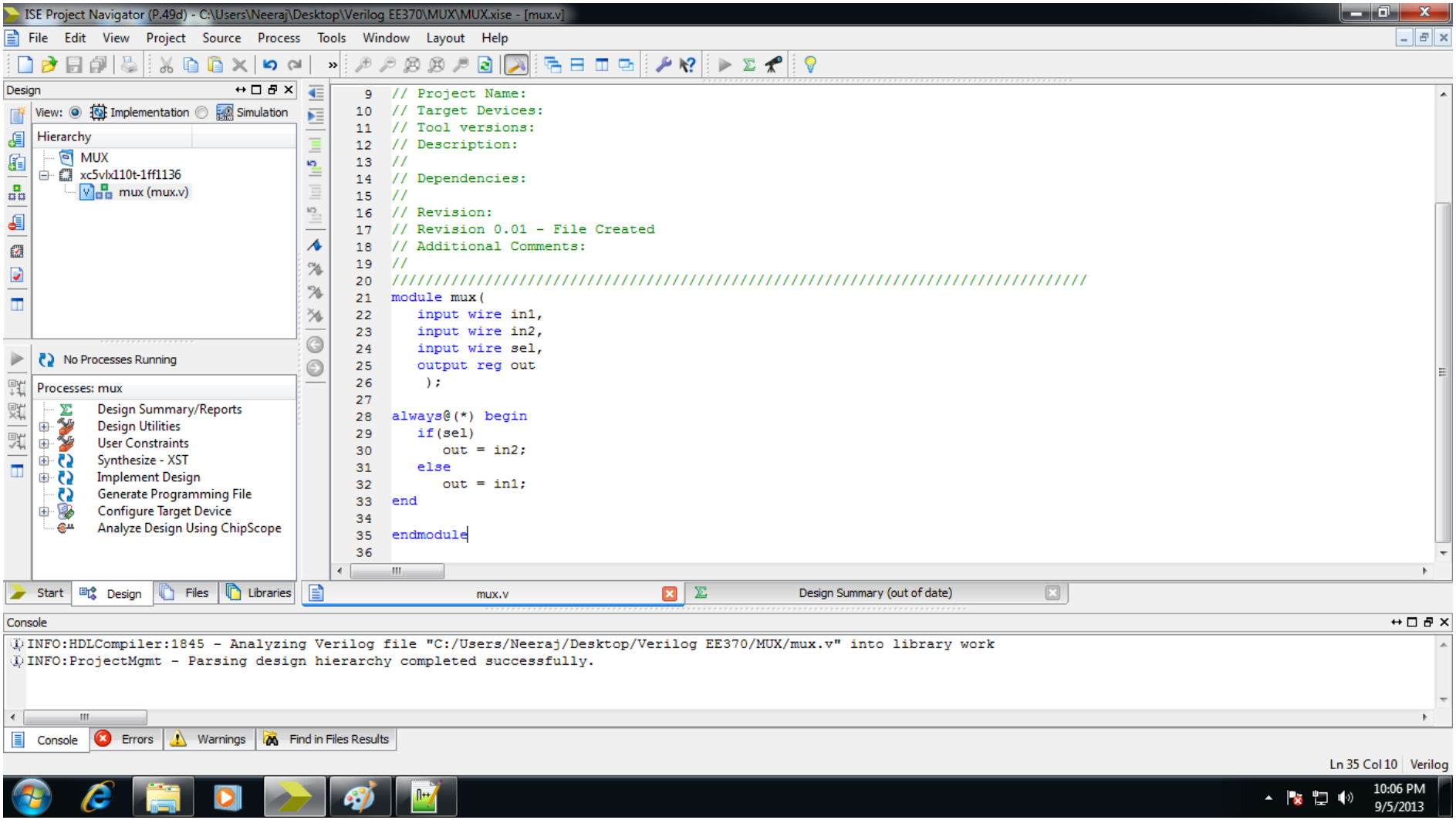


You can now write your module.

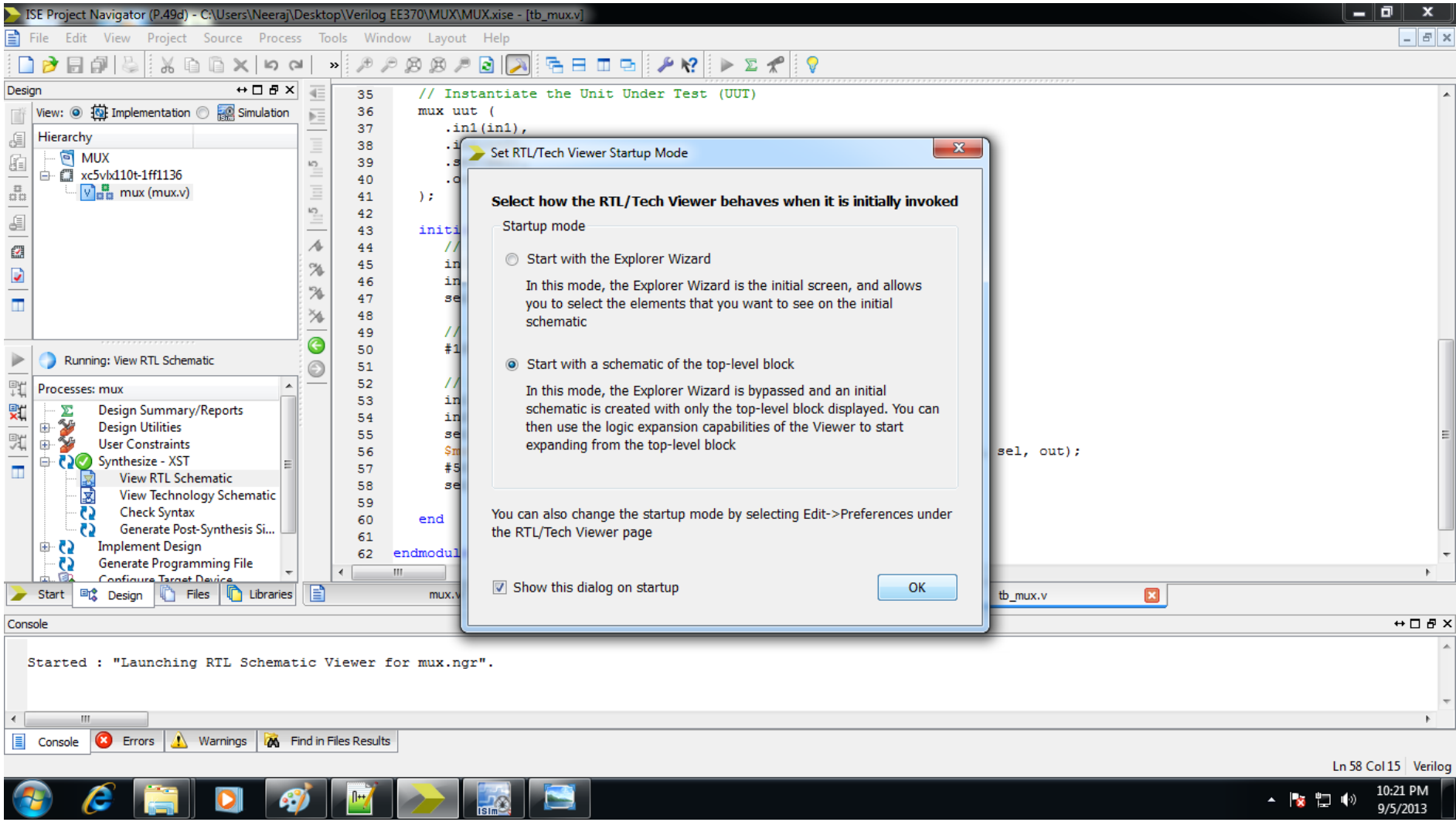


Code for mux written.

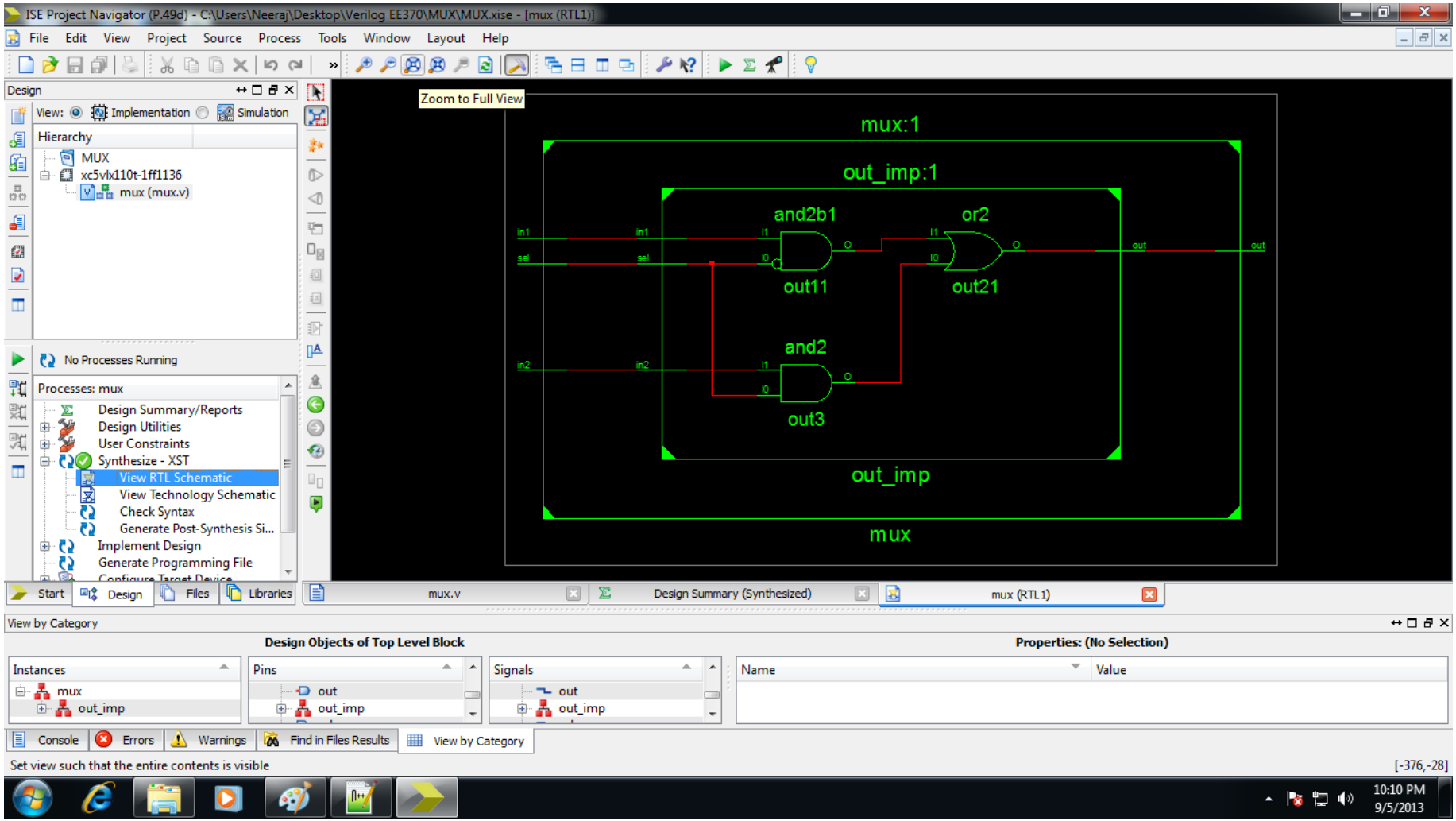
Double click on synthesize, on the left hand side.



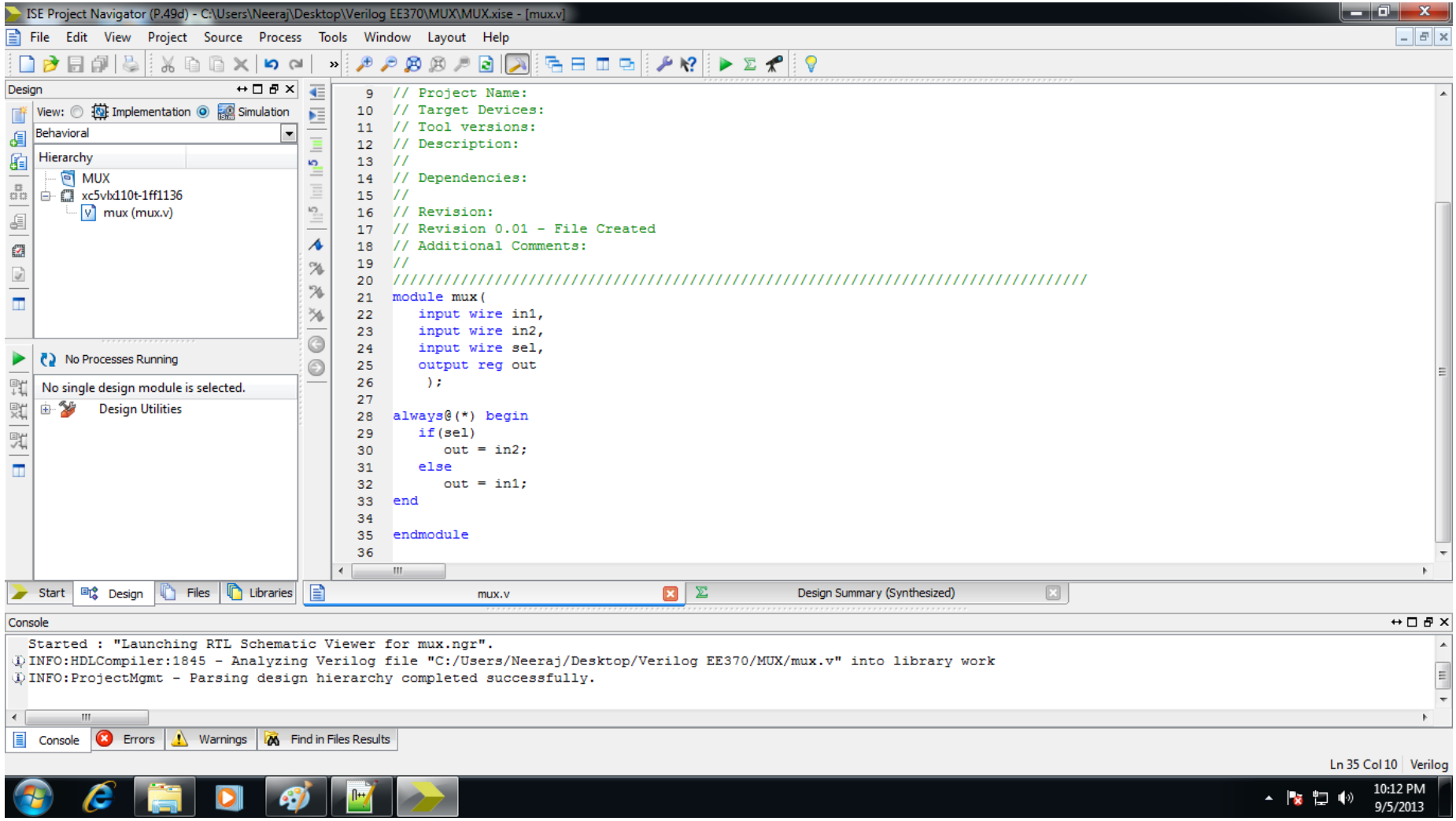
To see the circuit click on view RTL schematic option and then press ok.



Go on clicking in the black area to zoom in the circuit elements.

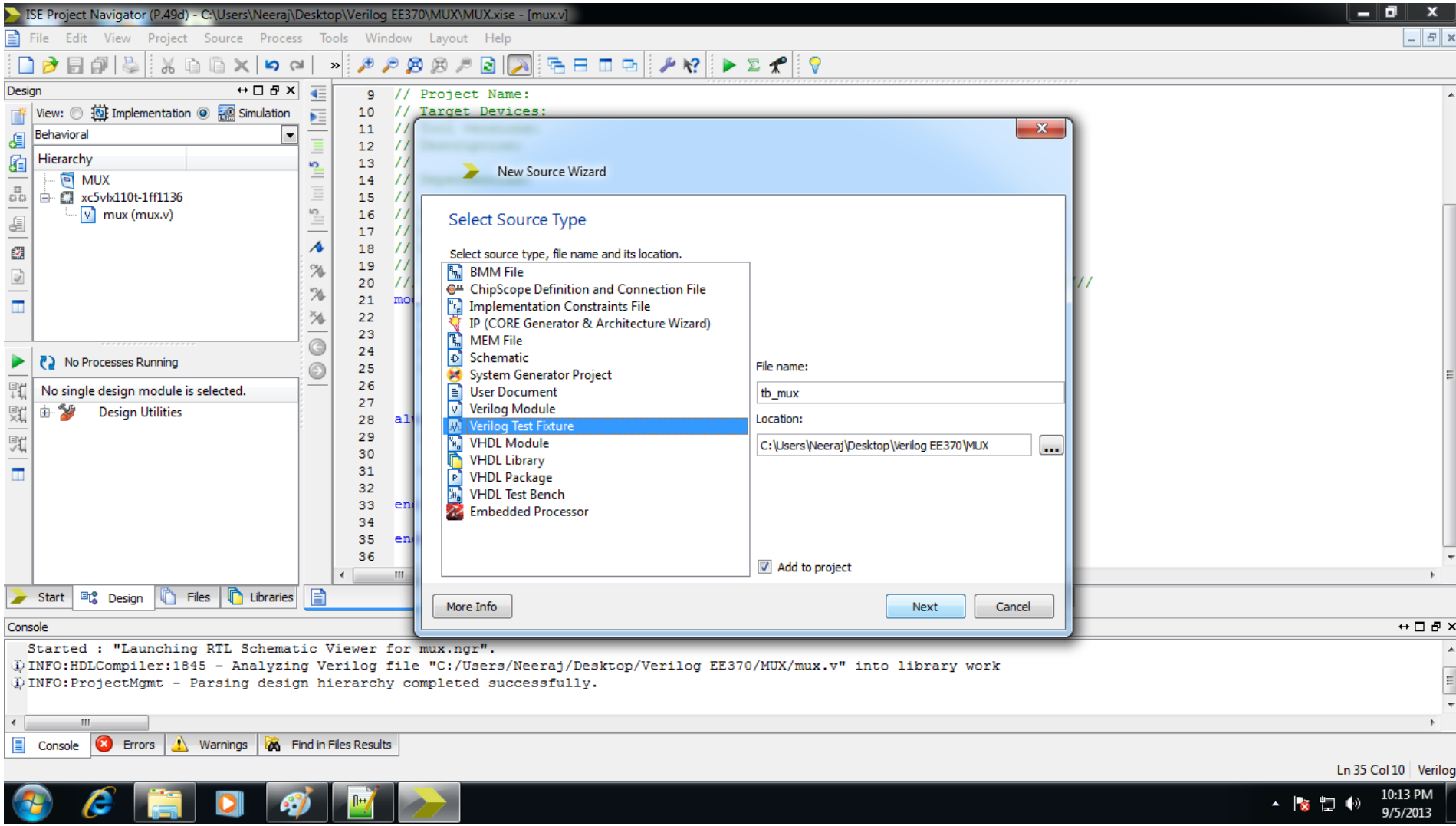


To run simulation click on Simulation option at the top of left column

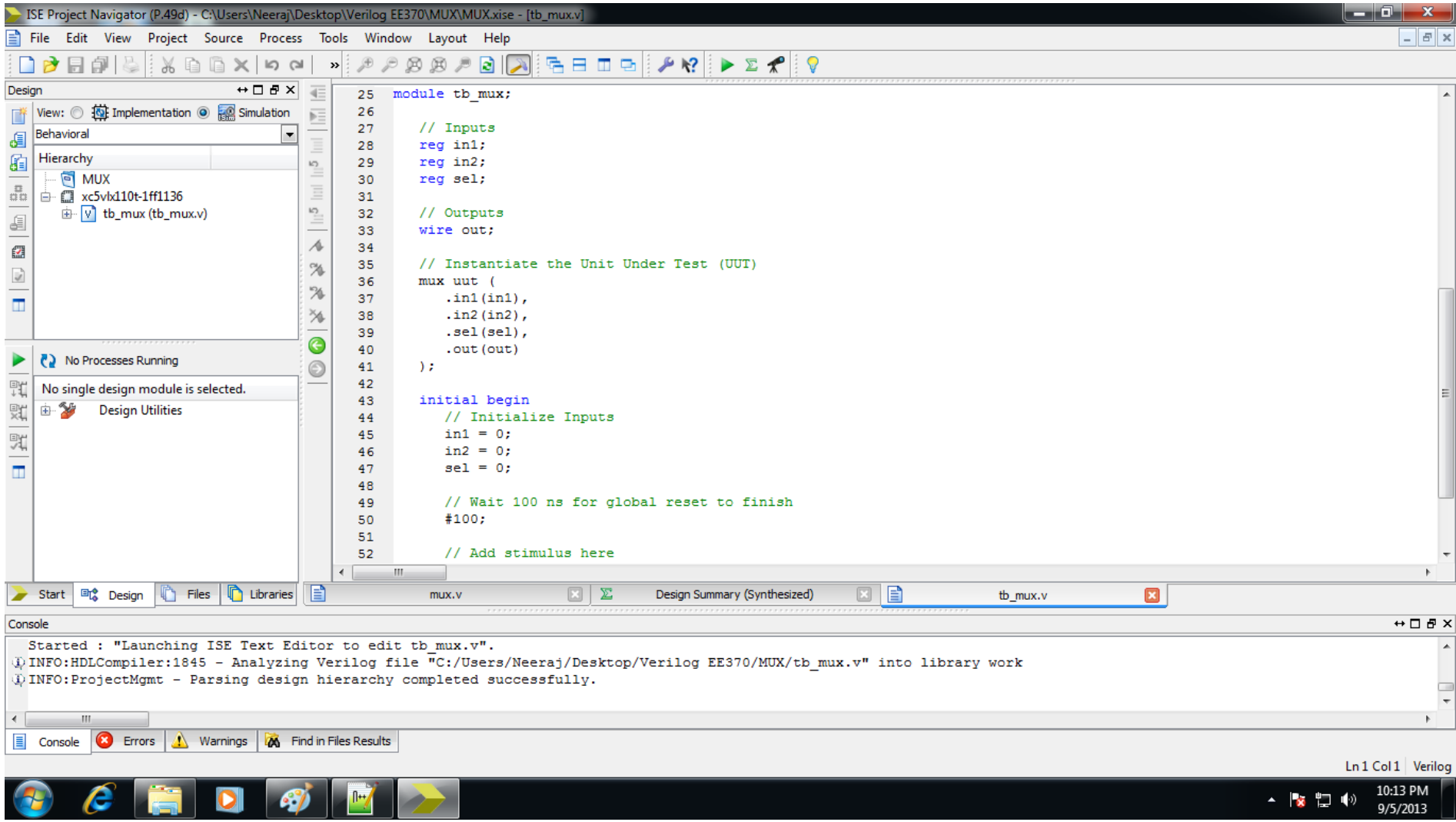


To create a Test bench, create New Source.

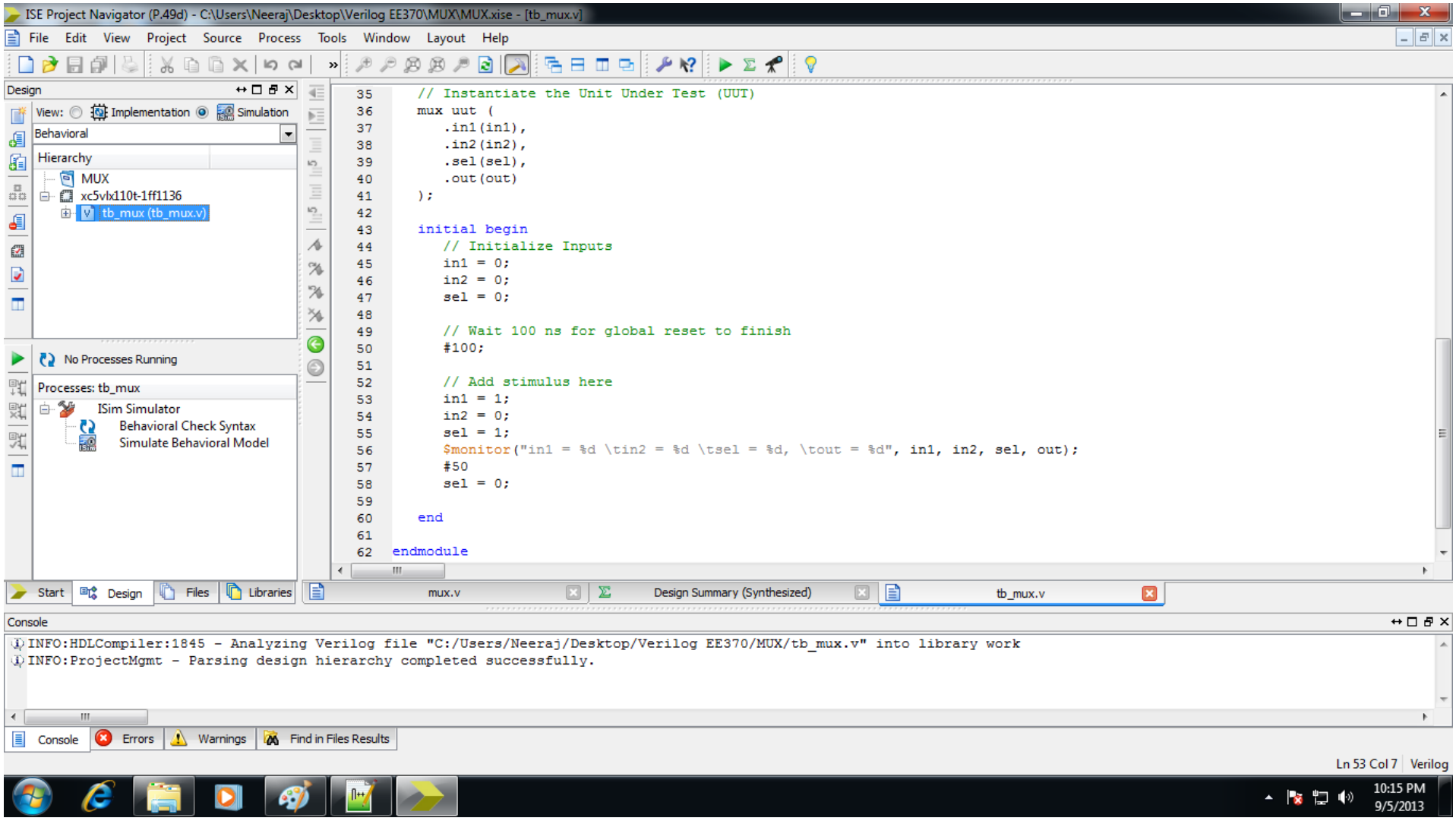
Select Verilog Test Fixture



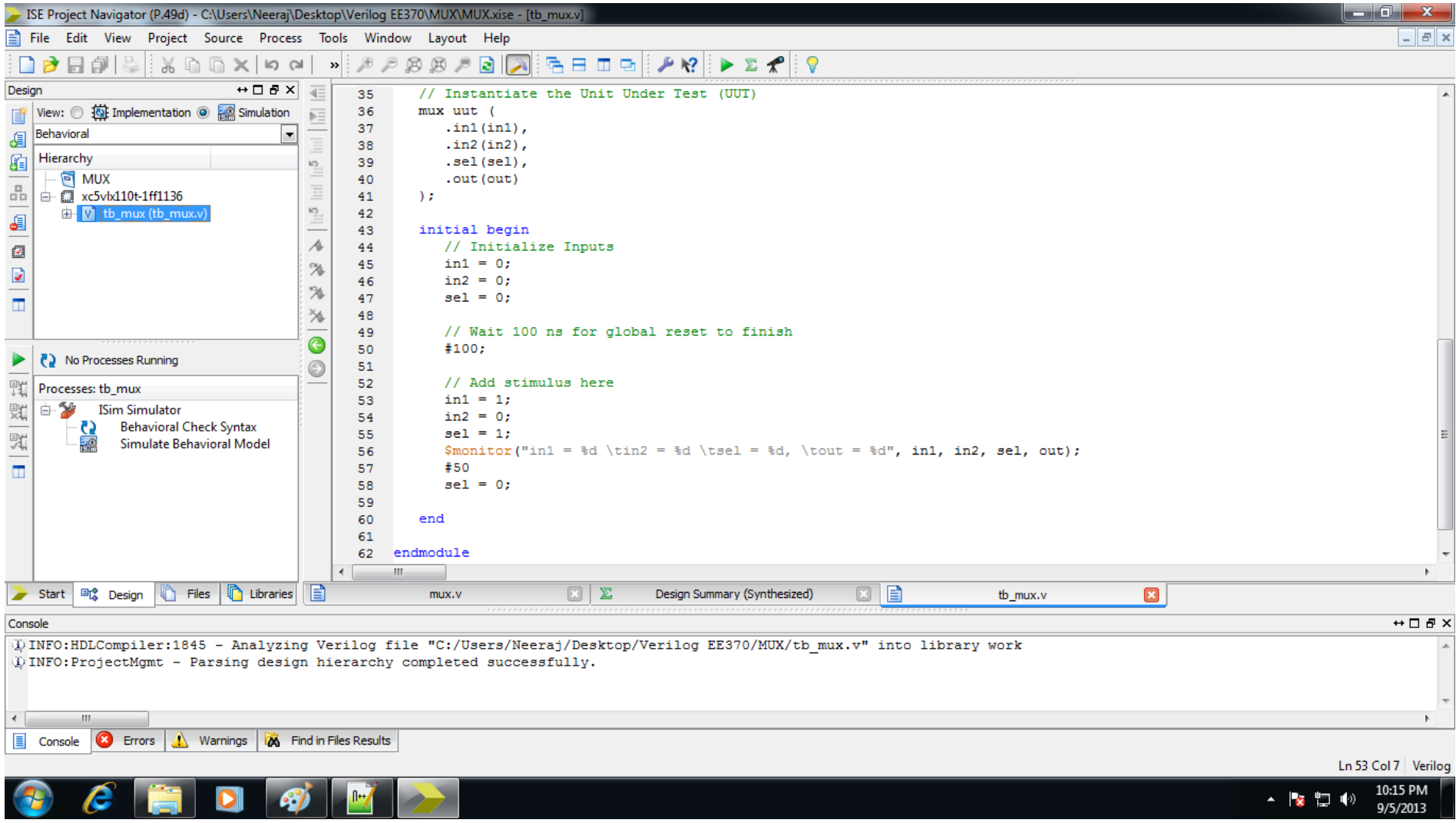
Template of Test bench will be created instantiating the mux module.



Add the testing code in the initial block below Add Stimulus here comment.



Double click on Simulate Behavioral Model option.



This is the simulation window. You can verify the working using waveforms or using printed statements at the bottom.