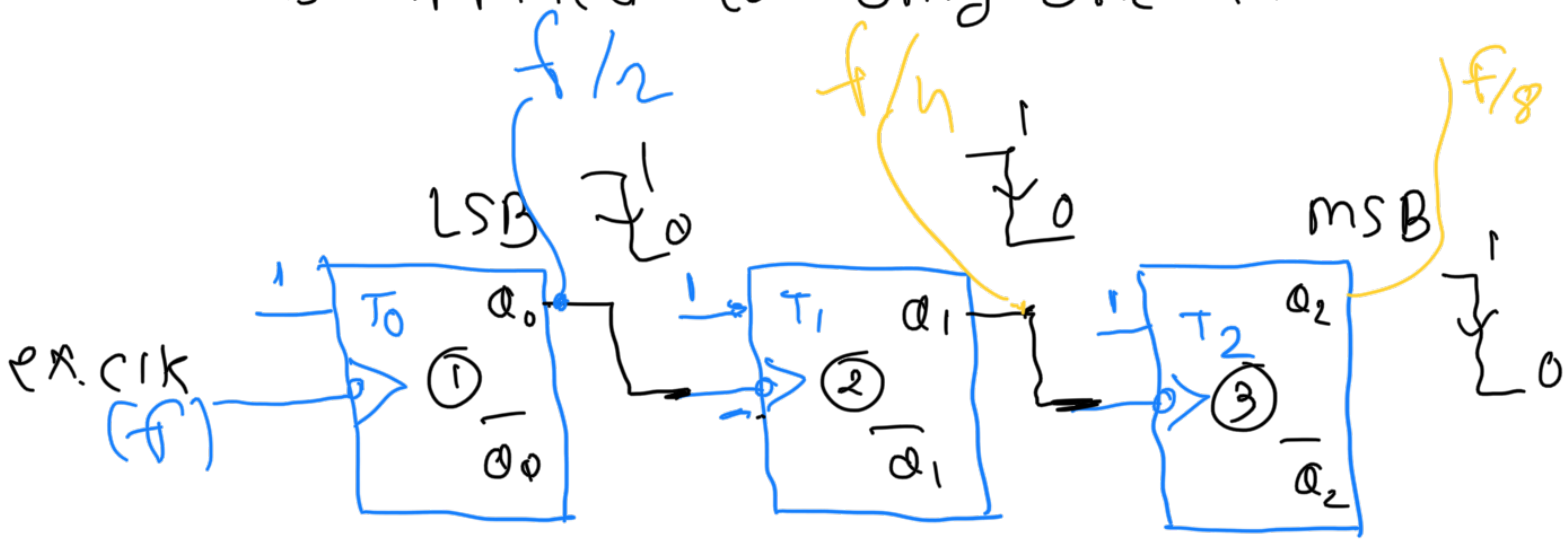
Asynchronous Counter: ripple counter.

→ FlipFlops are always in toggle mode.
(JK, J=1, K=1, T FF → T=1)

→ Clk is applied to only one FF.



Q_0 will toggle at every clk pulse.

Q_1 will change when Q_0 transits from "1" to "0". "High to low"

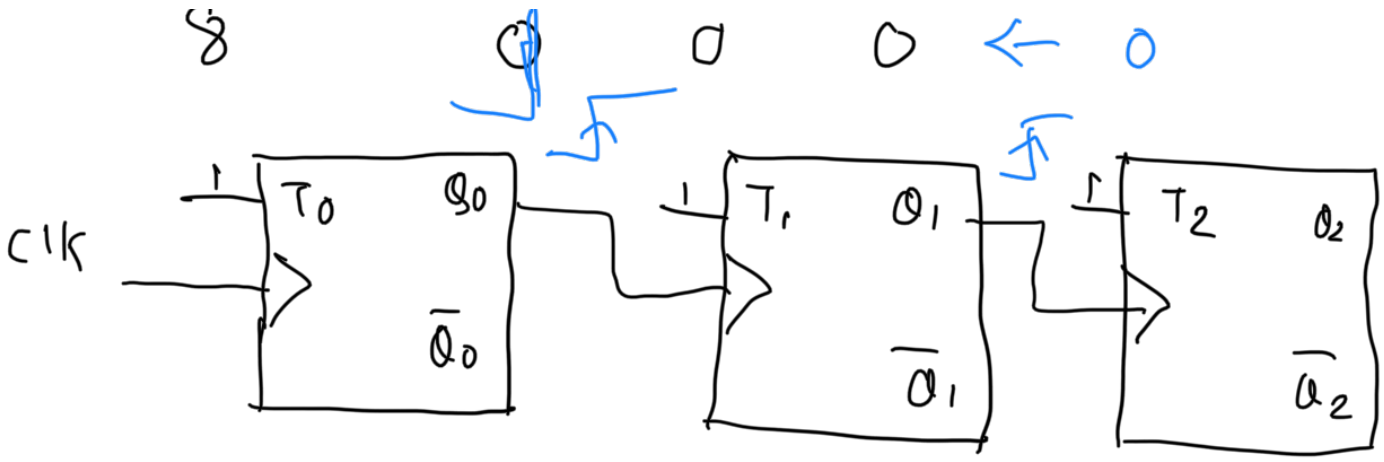
Q_2 will change when Q_1 transits from "1" to "0".

clk	Q_0 (LSB)	Q_1	Q_2 (MSB)	
-	0	0	0	← 0
1	1	0	0	← 1
2.	0	1	0	← 2
3.	1	1	0	← 3
4.	0	0	1	← 4
5.	1	0	1	← 5
6.	0	1	1	← 6
7.	1	1	1	← 7

MOD - 8 Counter.

0-1-2-3-4-5-6-7-0.

UP Counter.



→ Q_0 will toggle at every clk pulse.

→ Q_1 will change when Q_0 transits from "0" to "1".

→ Q_2 will change when Q_1 transits from "0" to "1".

clk	Q_0	Q_1	Q_2	
—	0	0	0	0
1.	1	1	1	7
2.	0	1	1	6
3.	1	0	1	5
4.	0	0	1	4
5.	1	1	0	3
6.	0	1	0	2
7.	1	0	0	1
8.	0	0	0	0

} MOD-8 Down Counter.

Type of Counter	edge triggering.	connection of clk. ($\downarrow \rightarrow (+)$, $\bar{Q} \rightarrow (-)$)
UP	-ve	+
down	+ve	+

Down	-ve	-
Up	+ve	-

Output freq at first FF → F/2

(∵ because it can count- 2)

Output freq at third FF → f/8

(∵ because it can count- 8)

---

max. Input clk frequency

minimum time required to perform proper operation is

$= N \times t_{pd}$

N = no. of flip flop

t_{pd} = pro. delay of FF.

$$T \geq N \times t_{pd}$$

$$\frac{1}{T} \leq \frac{1}{N \times t_{pd}}$$

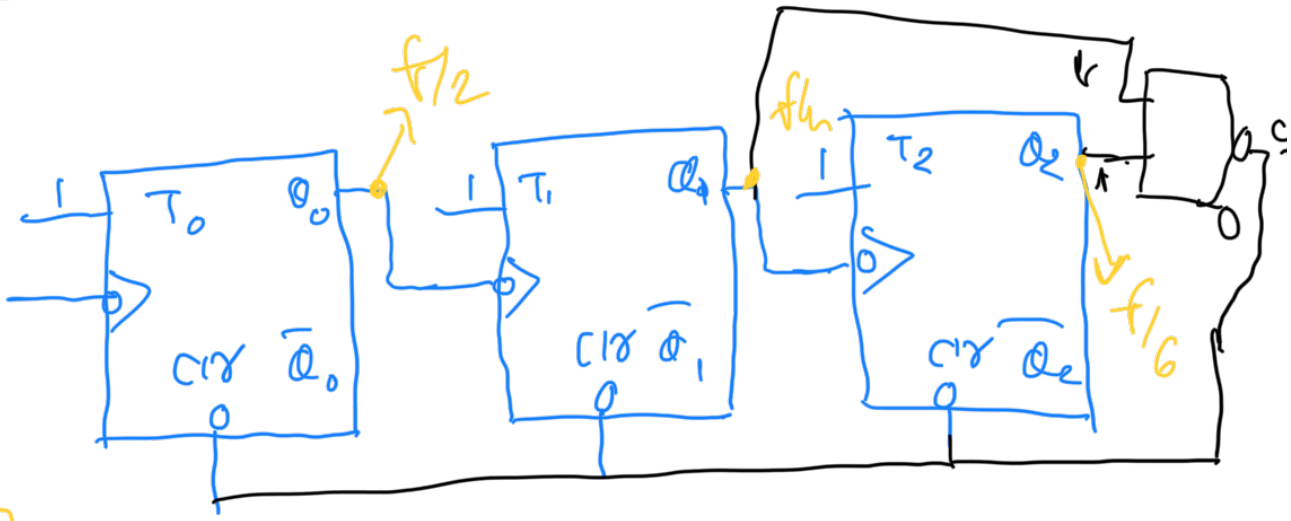
$$f \leq \frac{1}{N \times t_{pd}}$$

$$f_{max} = \frac{1}{N \times t_{pd}}$$

* Construction of Asynchronous Flip Flop:

→ mod- 6 up Counter:

mod- 5

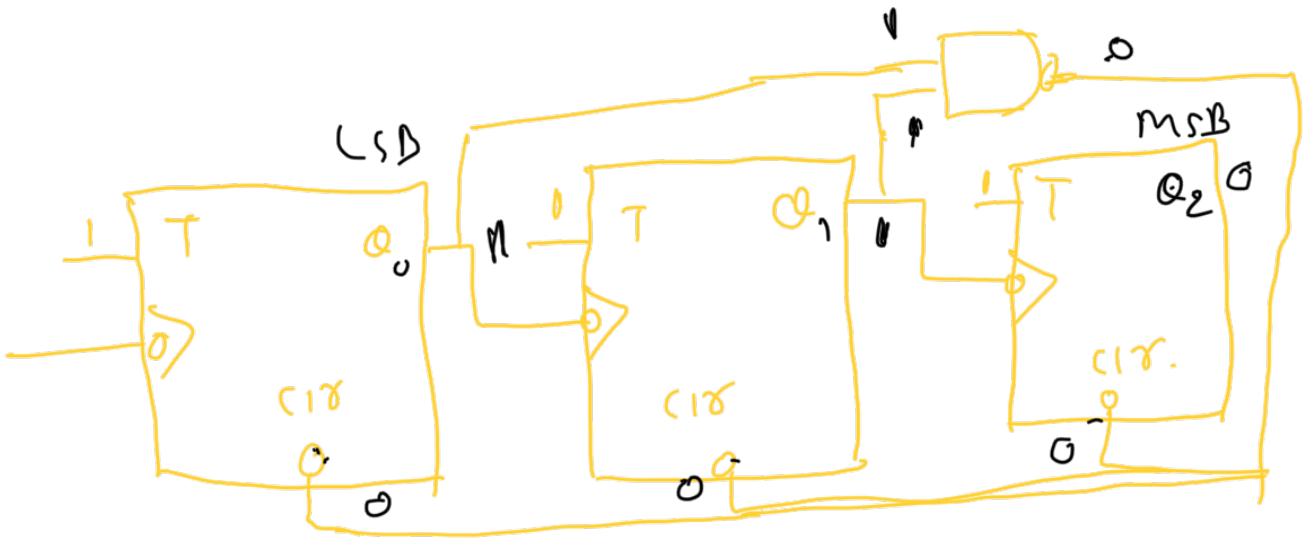


clr
→ active low
→ NAND

active high
→ AND

clk	Q_0	Q_1	Q_2
—	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1 → 0 0 0

Q.1



Asynchronous → OP.

→ (-ve) (+)

→ up counter.

110

mod-3 up counter

0 0 0

1 0 0

0 1 0

0 0 0

1 0 0

0 1 0

0 0 0

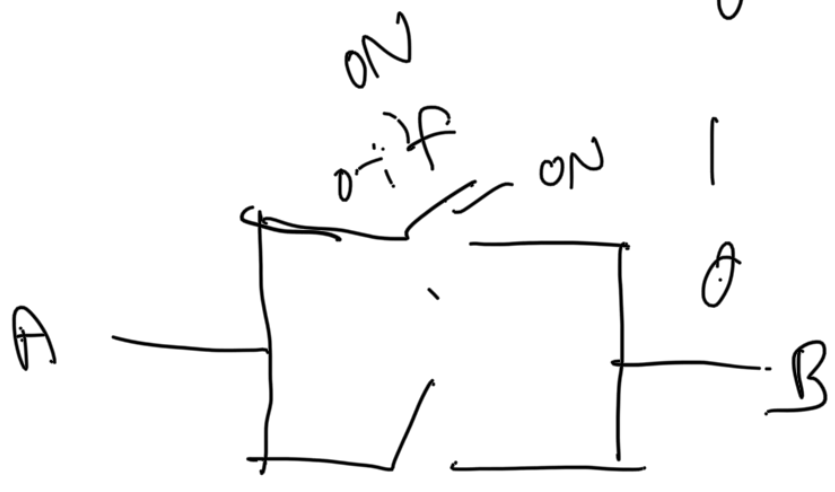
1 0 0

1 0 1

0 1 1

1 1 1

0



ON ON off