

A Project Report on

IMPLEMENTATION OF 4-BIT RCA USING QUANTUM DOT CELLULAR AUTOMATA AND MENTOR GRAPHICS

Submitted in partial fulfillment of the requirement for the award of degree of

BACHELOR OF TECHNOLOGY

in

ELECTRONICS AND COMMUNICATION ENGINEERING

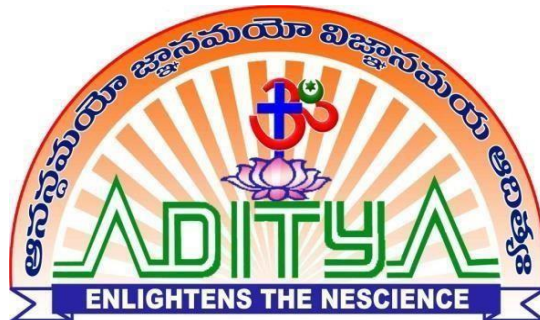
Submitted by

D. HARSHA (20P31A04J4)

Under the Esteemed Guidance of

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Associate Professor



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Aditya Nagar, ADB Road, Surampalem-533 437

(2023-2024)

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CERTIFICATE

This is to certify that the project report entitled “**Implementation of 4-Bit RCA using Quantum Dot Cellular Automata and Mentor Graphics**” is being submitted by **D. Harsha (20P31A04J4)**, has been carried out in the partial fulfillment of the requirement for the award of the degree of **Bachelor of Technology** in **Electronics and Communication Engineering, Aditya College of Engineering & Technology**, Surampalem, affiliated to **JNTUK, Kakinada** is a record of bonafide work carried out by them under my guidance and supervision during the academic period 2023-2024.

Project Guide

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EXTERNAL EXAMINER

DECLARATION

We are here by declaring that the entire project work embodied in this dissertation entitled “**Implementation of 4-Bit RCA using Quantum Dot Cellular Automata and Mentor Graphics**” has been independently carried out by us. A superior knowledge, no part of this work has submitted for any degree in any institution, university and organization previously.

Yours sincerely,

D. HARSHA (20P31A04J4)

ACKNOWLEDGEMENT

It gives us immense pleasure to express a deep sense of gratitude to my guide **Mr. Anjaiah Talamala, M. Tech, (Ph.D)**, Associate Professor, Department of ECE for whole hearted and invaluable guidance throughout the project. Without his sustained and sincere effort, this project work would not have taken this shape. He encouraged and helped us to overcome various difficulties that we have faced at various stages of our project work.

We would like to sincerely thank our Head of the department **Dr. R V V Krishna, M. Tech, Ph.D**, for providing all the necessary facilities that led to the successful completion of our project work.

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We would like to thank **all the faculty members** and the **non-teaching staff** of the Department of Electronics and Communication Engineering for the indirect support for helping us in completion of this project work.

Finally, we would like to thank all our **friends** and **family members** for their continuous help and encouragement.

With sincere regards,

D. HARSHA (20P31A04J4)

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Upon completion of the course, students will be able to:

CO#	Course Outcomes	Blooms Taxonomy level
CO1	Identify the problem by applying acquired knowledge.	Remember
CO2	Use literature to identify the objective, scope and the concept of the work.	Apply
CO3	Analyze and categorize executable project modules after considering risks.	Analyse
CO4	Choose efficient tools for designing project modules.	Evaluate
CO5	Integrate all the modules through effective team work after efficient testing.	Create
CO6	Explain the completed task and compile the project report.	Understand

CO-PO/PSO MATRIX:

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O 1	PS O 2
CO1	2	2	2		2								2	2
CO2	2	2	2	2				2	2				2	2
CO3	2		2	2				2	2				2	2
CO4	2				2						2			2
CO5				2	2				2	2			2	2
CO6									2	2	2			2
Course														

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CO-PO Justification

CO No.	PO/PSO	CL	Justification
CO1	PO1	2	Understanding the principles of VLSI design and the fundamentals of RCA design using Mentor Graphics.
	PO2	2	Recognizing the drawbacks and limitations of the existing RCA design based on Quantum Dot Cellular Automata.
	PO3	2	Recalling the steps involved in designing and implementing an RCA using QCA.
	PO5	2	Remembering the utilization of contemporary VLSI design tools for simulation and verification purposes in the project.
	PSO1	2	Our project trains students in ECE and VLSI fields by implementing the RCA using QCA tool, crucial for modern electronics applications.
	PSO2	2	Our project utilizes well-equipped laboratory infrastructure to mentor students in developing innovative electronics projects, exemplified by the implementation of an RCA using Quantum Dot Cellular Automata.
CO2	PO1	2	Applying the knowledge of VLSI design principles to implement the RCA using Quantum Dot Cellular Automata.
	PO2	2	Applying problem-solving skills to address the drawbacks identified in the existing RCA design.
	PO3	2	Applying the design methodologies to develop an optimized RCA solution using QCA.
	PO4	2	Applying investigative skills to analyze the performance improvements achieved through the QCA technique.
	PO8	2	Applying ethical principles in adhering to professional conduct and intellectual property rights during the project.
	PO9	2	Applying teamwork skills to collaborate effectively within the project team.
	PSO1	2	Moderately mapped as we conducted tests in basic operations in QCA.
	PSO2	2	Our project utilizes well-equipped laboratory infrastructure to mentor students in developing innovative electronics projects, exemplified by the implementation of an RCA using Quantum Dot Cellular Automata.
CO3	PO1	2	Analyzing the effectiveness of the QCA technique in enhancing RCA performance.
	PO3	2	Moderately mapped as we need to design basic gates by using QCA technology.
	PO4	2	Analyzing the results of simulations and experiments to evaluate the performance of the QCA based RCA.
	PO8	2	Analyzing ethical considerations related to research integrity and professional conduct.

	PO9	2	Analyzing team dynamics and individual contributions towards project goals.
	PSO1	2	Our project trains students in ECE and IoT fields by implementing the RCA using Quantum Dot Cellular Automata, crucial for modern electronics applications.
	PSO2	2	Our project utilizes well-equipped laboratory infrastructure to mentor students in developing innovative electronics projects, exemplified by the implementation of an RCA using Quantum Dot Cellular Automata.
CO4	PO1	2	Evaluating the impact of the QCA technique on RCA performance compared to traditional methods and existing RCA's.
	PO5	3	Evaluating the effectiveness of VLSI design tools in optimizing the RCA design.
	PO11	3	Evaluating the project's progress and resource management throughout its lifecycle.
	PSO2	2	Our project utilizes well-equipped laboratory infrastructure to mentor students in developing innovative electronics projects, exemplified by the implementation of an RCA using Quantum Dot Cellular Automata.
CO5	PO4	2	Creating experimental setups to test and validate the performance of the RCA using QCA.
	PO5	2	Creating design implementations using modern VLSI design tools.
	PO9	2	Creating a collaborative environment within the team to faster innovation and productivity.
	PO10	2	Creating comprehensive reports and presentations to communicate project findings effectively.
	PSO1	2	Our project trains students in ECE and IoT fields by implementing an RCA using Quantum Dot Cellular Automata, crucial for modern electronics applications.
	PSO2	2	Our project utilizes well-equipped laboratory infrastructure to mentor students in developing innovative electronics projects, exemplified by the implementation of an RCA using Quantum Dot Cellular Automata.
CO6	PO9	2	Understanding the importance of teamwork and collaboration in achieving project objectives.
	PO10	2	Understanding the significance of clear communication in conveying ideas and progress updates.
	PO11	3	Understanding the principles of project management and financial considerations in executing the project successfully.
	PSO2	2	Our project utilizes well-equipped laboratory infrastructure to mentor students in developing innovative electronics projects, exemplified by the implementation of an RCA Quantum Dot Cellular Automata.

Signature of the Guide

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ABSTRACT

QCA technology is a new platform, which is a transistor less and wire-less technology, hence it is one of the best alternatives to CMOS technology for developing low power and high-speed digital circuits at nano-scale level. The limitations of CMOS technology such as large number of transistors and wire connections in a small area was overcome by QCA technology. Therefore, we have chosen the QCA technology. Adder is a basic architecture in constructing all digital circuits. First, a full adder is designed in both QCA as well as Mentor Graphics which has improved performance in propagation delay and cell count. Then with the help of 4 full adders a 4-Bit Ripple Carry Adder is implemented in QCA and compared the results with the existing RCA in QCA. From the comparison, it is found that the proposed ripple carry adder has better performance than the existing adder circuits.

CHAPTER – 1: INTRODUCTION

1.1 VLSI (Very Large-Scale Integration):

Very large-scale integration (VLSI) is a technology that combines millions or billions of transistors onto a single integrated circuit (IC) chip. The term originated in the 1970s, along with other terms like "SSI" (small-scale integration) and "LSI" (large-scale), which are defined by the number of transistors or gates per IC. VLSI technology enables the creation of compact and complex ICs that can be used in a variety of applications, including: consumer electronics, computers, communication systems, medical devices, handheld devices, and supercomputers. In order to power new age technologies like AI/ML, IoT, AR/VR, cloud, etc., which are gradually replacing legacy technologies, it is necessary to design and produce extremely efficient and specialized chips.

A single chip can hold an ever-increasing number of transistors thanks to VLSI technology. The creation of transistors with smaller dimensions and better performance characteristics has been made possible by the development of semiconductor materials and manufacturing techniques. These advancements in VLSI design has caused an ongoing rise in integration density, allowing for the creation of extremely sophisticated and complex electronic systems. As the number of transistors integrated on a chip increases, the processing power of electronic systems also improves significantly. With more transistors available, complex computations can be executed at a faster rate, enabling high-performance computing. As a result, disciplines like artificial intelligence and machine learning, data analytics, and scientific simulations have advanced significantly

1.2 CMOS TECHNOLOGY:

Complementary Metal-Oxide-Semiconductor (CMOS) is a technology that uses a combination of metal, oxide, and semiconductor materials to create electronic circuits that are reliable and low-power. CMOS technology is used to manufacture computer processors, memory chips, and other digital devices. It helps regulate the flow of electricity through these components, which is important for their proper functioning.

CMOS technology is used in a wide range of digital circuits, including microprocessors, memory chips, and other digital logic circuits. It is also used in various applications, such as sensors, image processing, and wireless communications. CMOS

technology allows the on-chip integration of digital and analog functionalities. It uses complementary and symmetrical pairs of p-type and n-type metal-oxide semiconductor field-effect transistors (MOSFETs) for logic functions. MOSFETs act as amplifiers or switches that control the amount of electricity flowing between source and drain terminals, based on the amount of applied voltage. There are different logic families like RTL, DTL, TTL and MOS, ECL logic family. Some of them are already obsolete, and are not used in the design these days. While some of the logic families like TTL, ECL, MOS and CMOS logic families are quite popular and widely used in the digital circuits. In both NMOS and PMOS transistor, the voltage applied between the gate and source acts as a control voltage.

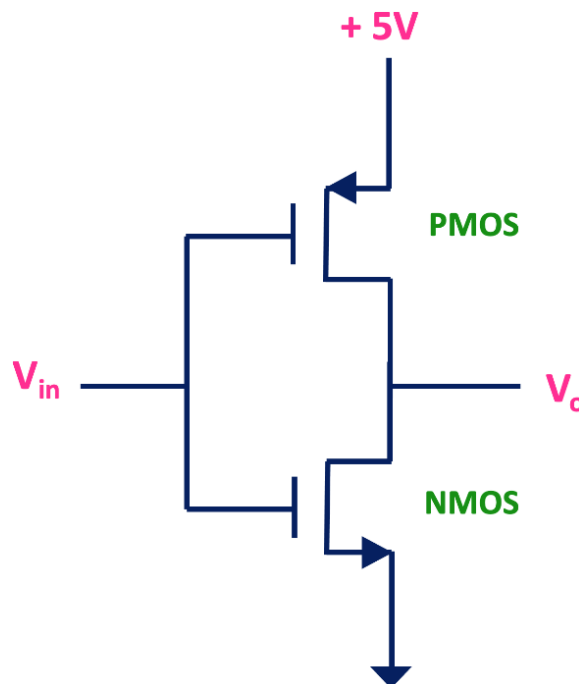


Fig 1.2.1: CMOS Inverter

CMOS based logic gates use complementary pair of NMOS and PMOS transistors. When MOS transistors are used as logic gate then they are used as a switch. By controlling the gate to source voltage, PMOS and NMOS transistor can be used as a switch. And they can be used to design a logic gate. CMOS logic uses both NMOS and PMOS transistors. The PMOS transistors are used as pull-up network and NMOS transistors are used as pull-down network because of that, the static power consumption of the CMOS based logic gates and logic circuit is very low compared to the logic gates which are designed using only either NMOS or PMOS transistors.

By connecting the inverter at the output of the NAND gate, we can implement AND gate. The CMOS AND gate are shown below.

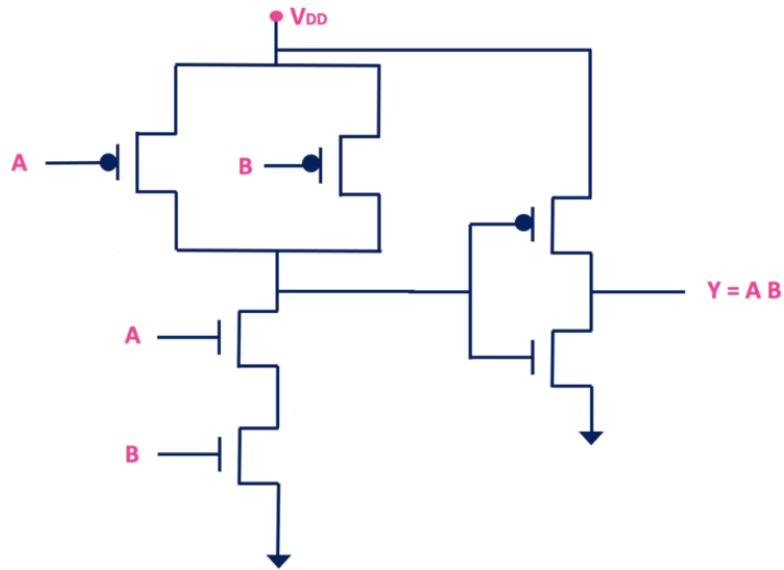


Fig 1.2.2: AND gate

Similarly, to implement the OR gate, just add the inverter at the output of the NOR gate. The CMOS OR gate is shown below.

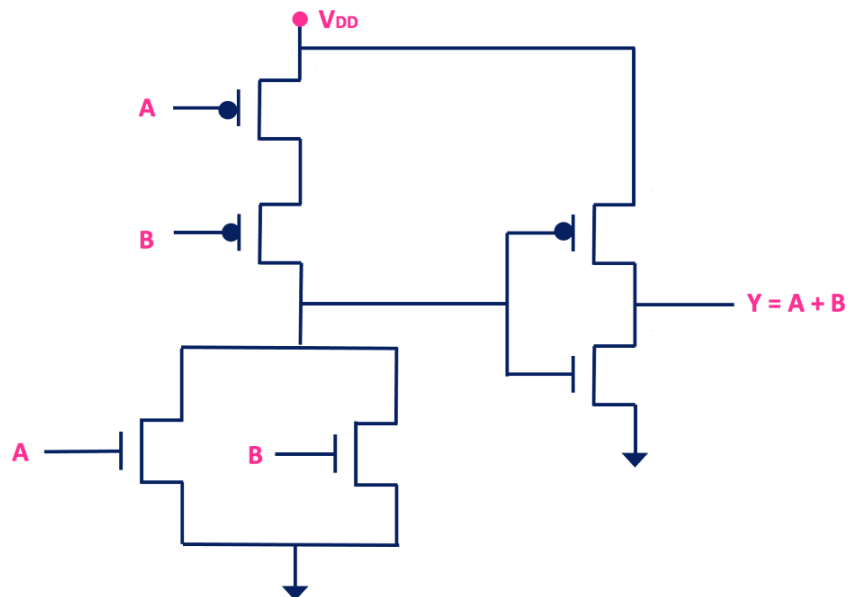


Fig 1.2.3: OR gate

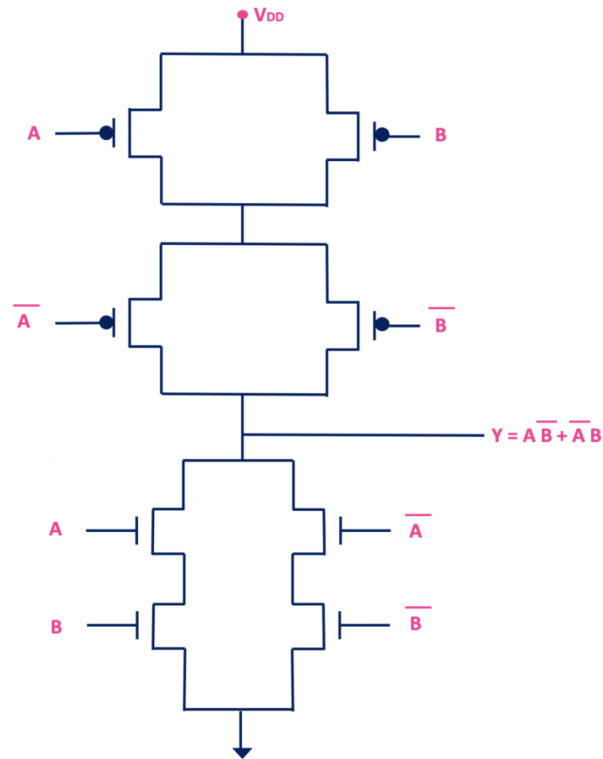


Fig 1.2.4: XOR gate

1.3 MENTOR GRAPHICS:

Mentor Graphics is one of the vendors of VLSI design tools and a supplier of Electronic Design Automation (EDA) tools, providing software and hardware design solutions that enable companies to develop better electronic products faster and more cost- effectively.

Mentor Graphics was a US-based electronic design automation (EDA) which is used to design complex VLSI architectures

- This includes schematic entry tools for traditional designs and HDL (Hardware Description Language) entry tools for digital designs using languages like Verilog, VHDL, and System Verilog.
- Mentor Graphics offers synthesis tools that convert RTL (Register Transfer Level) descriptions of digital circuits into gate-level representations. This step optimizes the design for area, power, and timing constraints while preserving its functionality.

1.3.1 MENTOR GRAPHICS PROCEDURE:

Mentor Graphics is a tool to run VLSI.

(130 size of transistor, channel length dist. between source to drain)

1) Open the tool, Right click open terminal CSH

```
#csh
```

```
#source /home/Mentor_Graphics/cshrc/ams_2009.cshrc
```

```
#dmgr_ic
```

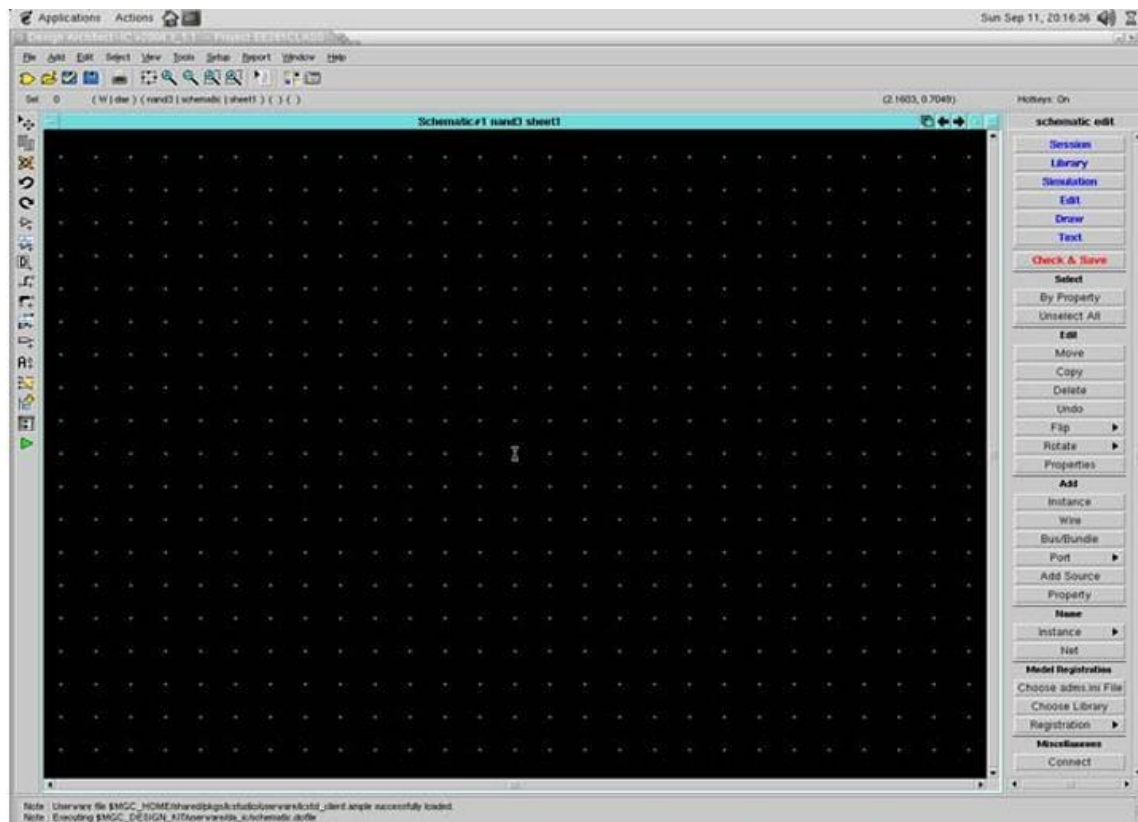


Fig 1.3.1.1: Interface of Mentor Graphics

2) Create a project:

Click on File, click on New and then click Project. Click on Browse, Up directory, click on /home and then go to work folder, give a file name of your choice. Then choose Library, next Browse, again up directory, /, home and then Mentor_Graphics, go to FOUNDARY, GDK, Pyxis_SPT_HEP, ic_reflibs and then tech_libs, generic13 and finally OK.

3) Add standard libraries:

Select project and then right click to get the options, click new, library, name and ok. Select the library you have added in your new project and right click to click new, cell, experiment and ok. Now select a cell, right click to select new and then schematic and the experiment name and ok for the cell to be created.

4) Add an instance:

- In order to add instance, click on add instance, then generic13, click symbols, go to nmos/pmos and then ok.
- In order to add a wire, click add wire, which is in yellow colour.
- In order to add sources and ground, click on library, then generic library and then pmos for Vdd and nmos for GND.
- In order to add input and output ports, select port in, right click to select edit object, click NET, click 'A' and output to 'Y'. Click view all for center alignment.

5) Check and Save:

Click check and save, then schematic shows 0 errors and 0 warnings if there are no errors in the schematic. Check report and close.

6) Generating a symbol:

To generate a symbol, click add and generate symbol, choose the required shape as per the experiment and ok. Customize pin list, bubble at output, then experiment name and ok. Repeat the step 5 to check and save the symbol.

7) Test bench:

Test bench is used to simulate schematic and used for verifying results

Click Project Navigator, your library, new, cell, file name, ok. Click file name, right click for new schematic. Click Add instance, choose symbol, your library, cell, symbol, ok. Paste symbol, click ESC and double tap symbol and close it. Click library, source library, DC source and Schematic window, paste and ESC. Click library, generic library and add sources Vdd and Ground.

8) Edit the sources as per the requirements, for example:

Mag 1V, then click edit object and 5V, ok.

Click Pattern, edit object and 8-bit pattern and enter 11010110, ok.

Check & save as per step 5.

9) For Simulation mode:

Click on the green-colored triangle symbol, enter Simulation mode, ok. After entering into the simulation mode, it will not allow any new modifications in the test bench. Apply the required parameters for AC, DC, Transient outputs and the output waveforms can be obtained in EZ Waves, which is used for plotting latest waveforms.

CHAPTER – 2: LITERATURE SURVEY

Alkaldy, Bagherzadeh, and Navi introduced a novel and robust single-layer wire crossing approach for exclusive XOR and sum of products logic design utilizing quantum-dot cellular automata (QCA) with 494 cells count and 0.68 area. This research addresses the challenge of implementing efficient wire crossing techniques in QCA-based logic circuits and contributes to the development of reliable and scalable QCA architectures for digital logic design. Also, this study highlights the ongoing efforts to optimize QCA-based systems for low-power and high-performance applications, laying the foundation for future advancements in nanotechnology.

Hashemi and Navi presented a novel and robust quantum-dot cellular automata (QCA) full-adder design with 442 cells count and 1 area. This research contributes to advancing the field of QCA-based arithmetic circuitry by introducing innovative approaches to full-adder implementation. By addressing the challenges of robustness and reliability in QCA circuits, their work paves the way for more practical and their study underscores the importance of developing reliable building blocks for QCA-based systems, highlighting the ongoing efforts to overcome technological limitations in nanoscale computing.

Hashemi, Tehrani, and Navi proposed an efficient full-adder design using quantum-dot cellular automata (QCA) with 308 cells and 0.29 area. This research contributes to the optimization of QCA-based arithmetic circuits, aiming to enhance their efficiency and reliability. By introducing novel techniques for full-adder implementation they address the growing demand for high-performance computing systems in the field of quantum computing. Their work underscores the significance of efficient circuit design methodologies in overcoming the inherent challenges of QCA technology.

La brado and Thapliyal investigated the design of adder and subtractor circuits within the framework of majority logic-based field-coupled QC Anano computing with 295 cells count and 0.3 area. Their work, contributes to advancing the field of quantum-dot cellular automata (QCA) by exploring novel computing paradigms. Their study underscores the ongoing exploration of alternative computing architectures beyond traditional CMOS technologies, highlighting the potential of QCA nano

computing for future computing applications.

Abedi, Jaberipur, and Sangsefidi proposed a coplanar full adder design in quantum-dot cellular automata (QCA) using clock zone-based crossover with 262 cells count and 0.34 area. This research contributes to advancing the field of QCA-based arithmetic circuitry by introducing innovative techniques for full adder implementation. By leveraging clock zone-based crossover, Abedi et al. aim to enhance the performance and scalability of QCA adders, addressing the growing demand for efficient computing architectures in nanotechnology-driven systems.

CHAPTER – 3: QCA AND IT'S WORKING

QCA is a new platform which is wireless and transistor less technology, so it is also called as one of the alternatives to CMOS technology. QCA is used for implementing complex VLSI architecture and developing low-power, high speed digital circuits at nano- scale level compared to CMOS. The limitations of CMOS technology such as high integration density within small area due to large number of transistors and wire connections between them was overcome by QCA technology.

3.1 QCA CELLS AND IT'S POLARIZATION:

In this technology, the binary information could be transmitted through Coulombic repulsion between the neighboring QCA cells. Here, the binary value 0 or 1 is encoded through the reconfigurations of electrons in the quantum dots of QCA cells.

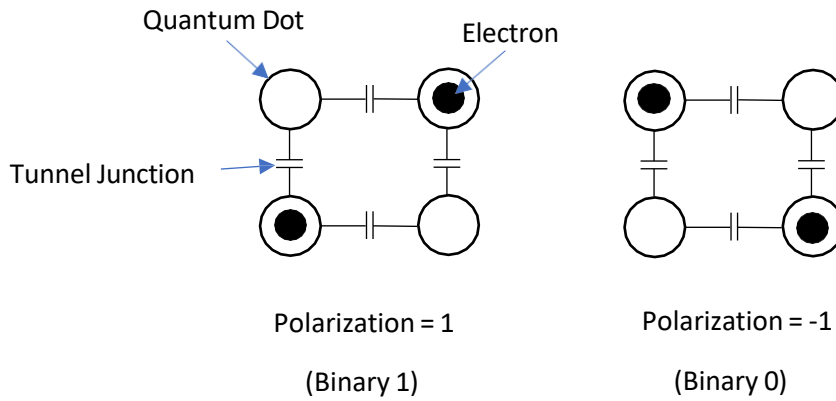


Fig 3.1.1: QCA cells

- If electron is in Clock-wise then it is Logic 1
- If electron is in Anti clock-wise then it is Logic 0

Depending upon the location of electron pair charge in the QCA cell, polarizations are represented by two ground state polarizations namely -1 for binary 0 and +1 for binary 1. These -1 and +1 state polarizations are formulated as:

$$p = \frac{[(p1 + p3) - (p2 + p4)]}{p1 + p2 + p3 + p4}$$

QCA based circuits are constructed using QCA cells. The basic device consists of four quantum dots arranged in a square with two excess electrons that tend to repel each

other, resulting in two stable configurations. The square shape QCA cells comprises of four quantum dots with two dots occupied by electrons. These electrons reside over in the diagonal corner of the cell due to Coulombic repulsion of force between them. Tunnelling of electrons between the quantum dots results in two polarized states. These states namely $PL = -1$ and $PL = +1$ represents logic value '0' and '1'. Wires in QCA, are constructed either using normal cell or rotated cell. Due to less complexity, normal cell as shown in are preferred over compared to rotated cell. The polarization state of cells gets changed when input is applied at one end of the wire.

Based on the polarization either logic '0' or logic '1' will be a transmitted horizontally or vertically. Quantum Dot Cellular Automata (QCA) is a classical digital device that represents data as charge configuration rather than charge flow. Data is passed in QCA by arranging electrons along diagonals with cells tending to assume the same configuration as their neighbors. The basic native gate in QCA is the majority gate, which has three inputs and one output.

Advantages of QCA over CMOS:

- Transistor-less, operates at nano-scale, high integration density, low power consumption.
- Switching frequency not limited like in CMOS.

3.2 QCA DESIGNER TOOL:

QCA Designer is the product of an ongoing effort to create a rapid and accurate simulation and layout tool for quantum-dot cellular automata (QCA). QCA Designer is capable of simulating complex QCA circuits on most standard platforms. It is a software application used in the field of Qualitative Comparative Analysis (QCA). It helps researchers to analyze complex datasets and identify patterns and relationships among variables. Also, it is an advanced software application tailored specifically for Qualitative Comparative Analysis (QCA), a method widely used in social science research to analyze qualitative data. This tool provides researchers with a comprehensive platform to input their data, define conditions, and conduct analyses to uncover intricate patterns, configurations, and relationships among variables.

At its core, the QCA Designer tool allows researchers to systematically analyze how various combinations of conditions contribute to specific outcomes or phenomena of

interest. It enables users to specify the presence or absence of conditions across cases and systematically compare different configurations to identify which are associated with the outcome under study. One of the key advantages of the QCA Designer tool is its user-friendly interface, which simplifies the often-complex process of conducting QCA.

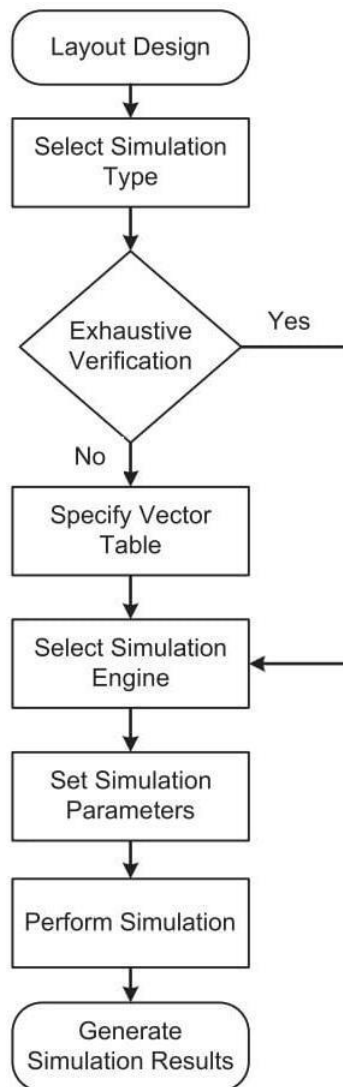


Fig 3.2.1: Design flow of QCA Designer

Researchers can easily input their data, define conditions using Boolean logic (such as AND, OR, and NOT), and visualize the results through intuitive graphs and diagrams. Moreover, the QCA Designer tool typically includes a range of analytical features to enhance the rigor and validity of the analysis. These may include checks for consistency and coverage of cases, sensitivity tests to assess the robustness of findings, and options for conducting subgroup analyses to explore variations across different contexts or groups.

uncover causal mechanisms, identify critical factors, and gain deeper insights into the complex relationships within their qualitative data. By providing a structured and systematic approach to analysis, it enables researchers to generate nuanced and evidence-based explanations of social phenomena.

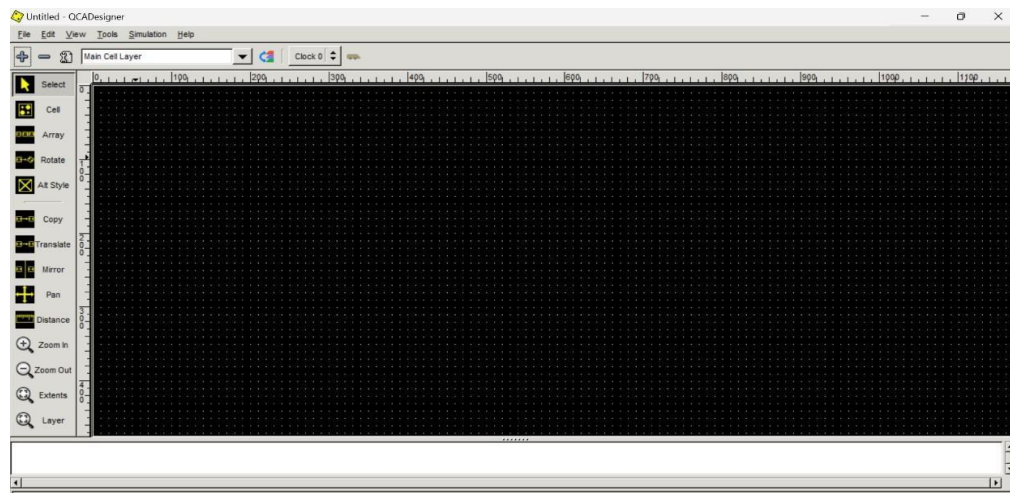


Fig 3.2.2: Interface of QCA Designer Tool

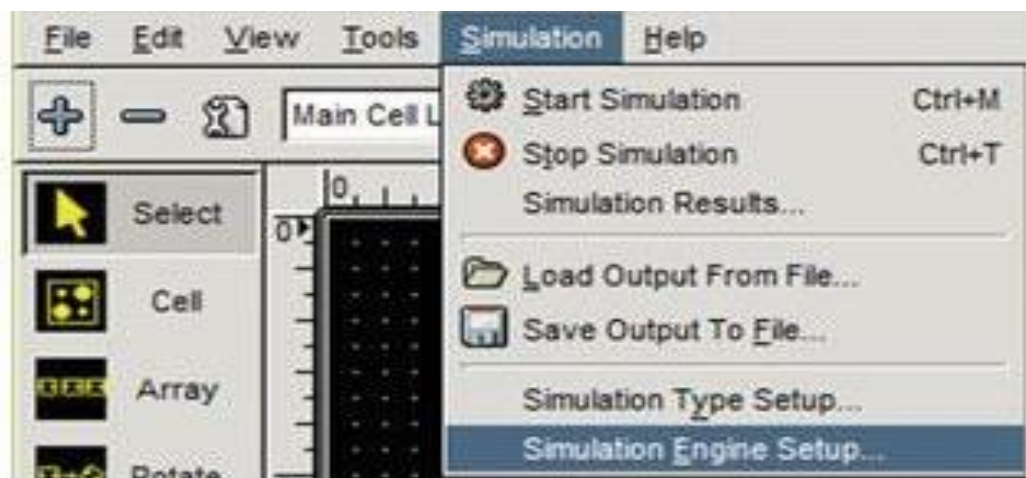


Fig 3.2.3: Simulation Design in QCA Tool

3.3 QCA WIRE:

The QCA wire is the one of the most important parts of the design.

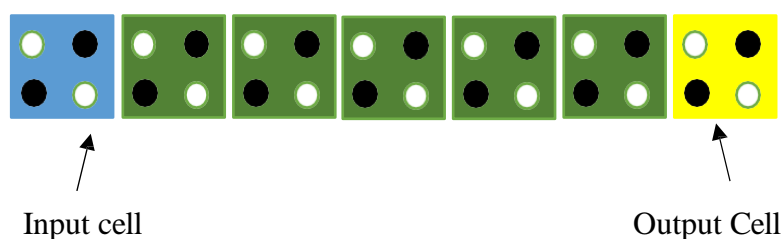


Fig 3.3.1: QCA Wire

The wire is used for communication purpose, Same in QCA the wire is used for passing the input or output. The wire in QCA will be used for the passing of data. The data passing will play a major role because the input must be passed from one cell to another so that the circuit will work. The wire will pass the data from one cell to another cell. The cell will work by arranging the cells by each other in a line. The input is shown as an electron form the electron will decide the data whether it is 0 or 1 when the electron is clockwise then it is logic 0 and if the electron is anticlockwise then it is logic 1.



Fig 3.3.2: Logic 0 and Logic 1

3.4 CLOCKING IN QCA:

Clocking in QCA is used to control the polarization state of cells and passing the data. Two ways of Clocking is performed: zone clocking and continuous clocking. There are four types of clock zones in QCA named as clock zone 0, clock zone 1, clock zone 2, and clock zone 3 whose phase differs by 90° . The cells with identical color are assigned the same clocking zone. QCA will protect the design from delay so we use a clock. The clock will pass data from the small clock to the high clock condition.

- Clock 0 - Green
- Clock 1 - Violet
- Clock 2 - Blue (Lite)
- Clock 3 – White

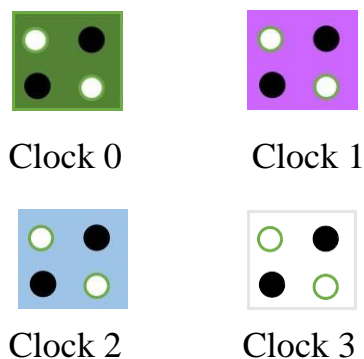


Fig 3.4.1: Clock cells in QCA

As shown in the figure there are four phases in QCA circuits namely switch, hold, and release and relax phase respectively. Four clocks are,

- Clock 0 is for “Switch”
- Clock 1 is for “Hold”
- Clock 2 is for “Release”
- Clock 3 is for “Relax”

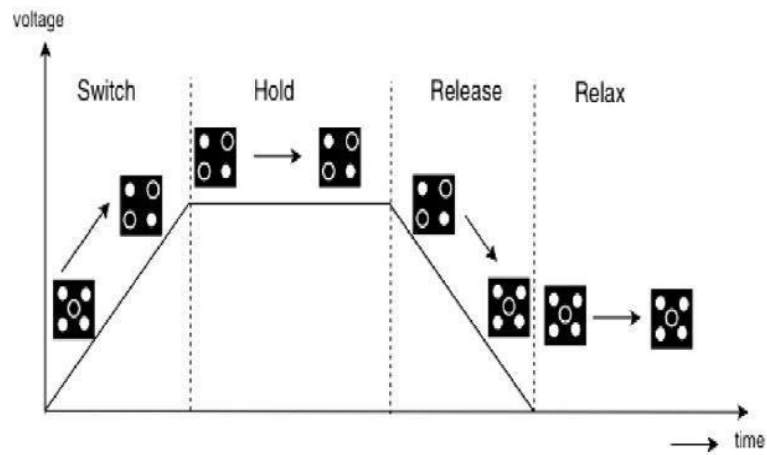


Fig 3.4.2: Clocking in QCA

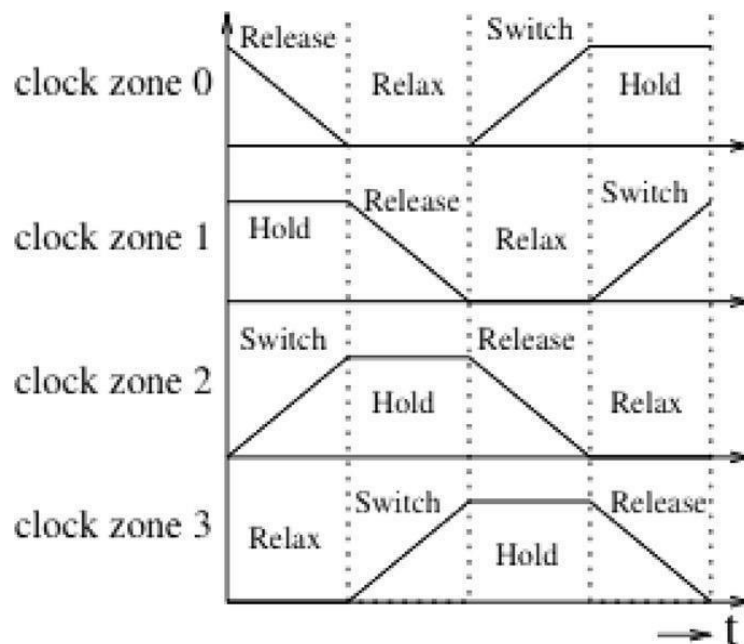


Fig 3.4.3: Clock zones of QCA cells

3.5 BASIC QCA GATES:

3.5.1 MAJORITY VOTER GATES:

The majority voter (MV) gate is a basic logic element in QCA. It's a universal block in QCA technology that can form AND and OR gates. Designing the QCA circuit generally requires an Inverter, QCA wire and a three-input Majority Voter gate. The signal propagates in QCA wire as a result of the electricity inter linkage between cells. A Majority Voter gate has five cells. Among five, three cells work as input cells and one cell works as output cell as given in. The middle cell is called as device cell and its logic operation depend on logic of input cells.

- QCA works based on majority gate
- A majority gate consists of 5 cells
- A cell consists of 4 Quantum dots
- Where Orange color represents **Fixed polarization**
- Blue color represents **Input**
- Yellow color represents **Output**
- If electron is in Clock-wise then it is Logic 1
- If electron is in Anti clock-wise then it is Logic 0

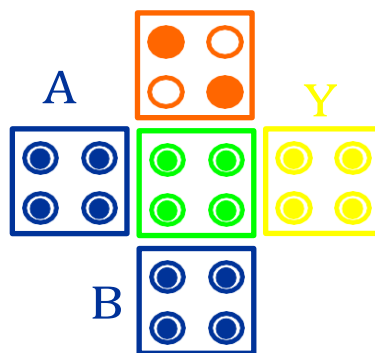


Fig 3.5.1.1: Majority voter gate

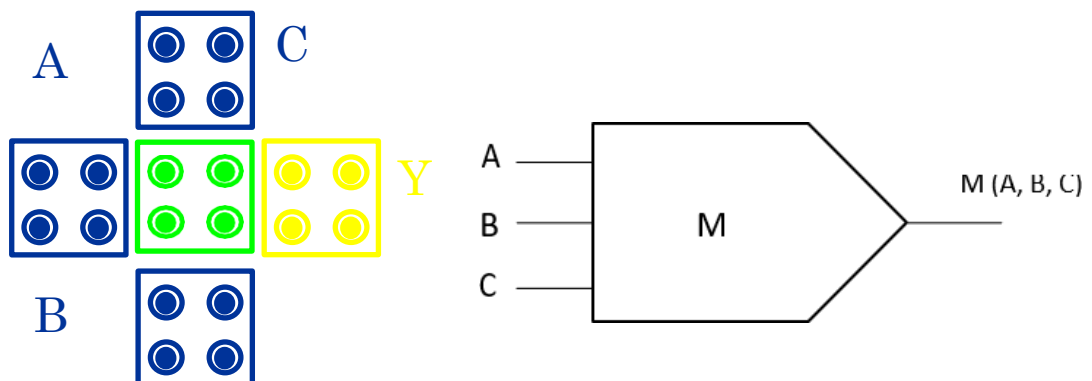


Fig 3.5.1.2: 3-input Majority voter gate

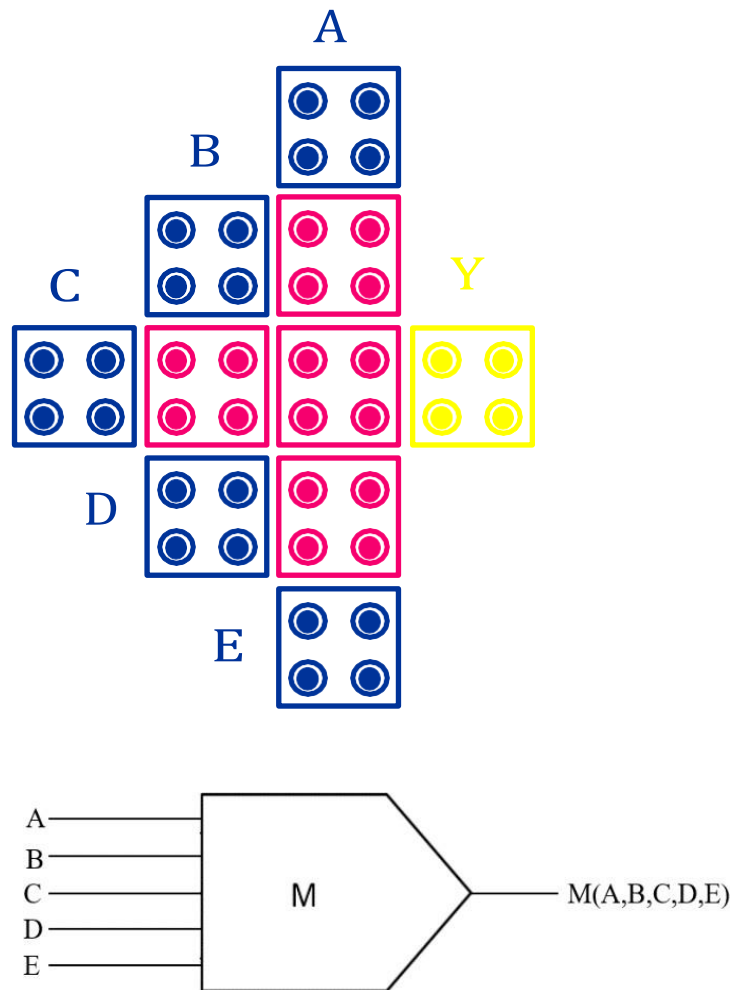


Fig 3.5.1.3: 5-input Majority Gate

3.5.2 INVERTER:

Inverter is a circuit with one input whose output is high if the input is low and vice versa. The not operation outputs an inverted version of the input. Hence, a not gate is also known as an inverter.

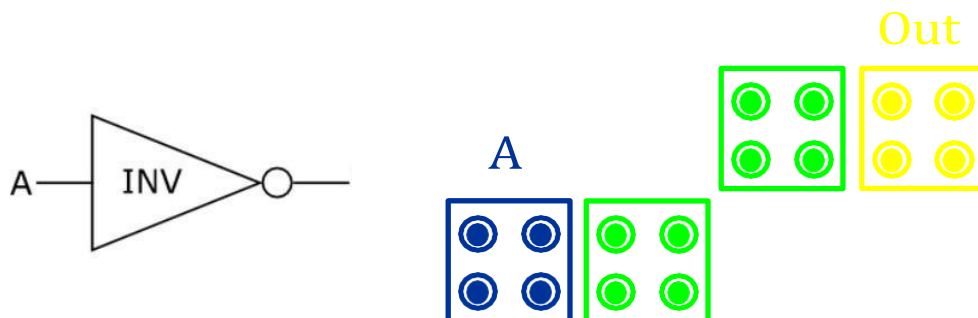


Fig 3.5.2.1: Inverter

CHAPTER – 4: EXISTING METHOD

4.1 EXISTING TECHNIQUE:

Actually, full adders and RCA circuits are fundamental units in logic circuits and digital arithmetic. RCA's layout is designed and implemented simply, but it is quite slow since each full adder has to wait for the calculated carry bit from the previous one. To overcome this problem, we can reduce the delay in RCAs by decreasing the delay of full adders.

The Existing method, Full adder using Quantum Dot Cellular Automata (QCA) which consists of three-input XOR gate and a three-input majority gates. Using this Full adder, higher adders like 4-bit RCA (Ripple Carry Adder) has been designed with the area of 0.208, cell count-262, Delay that has 1.75. An increase in the QCA cell count ends up in an increase of the area and delay of the design.

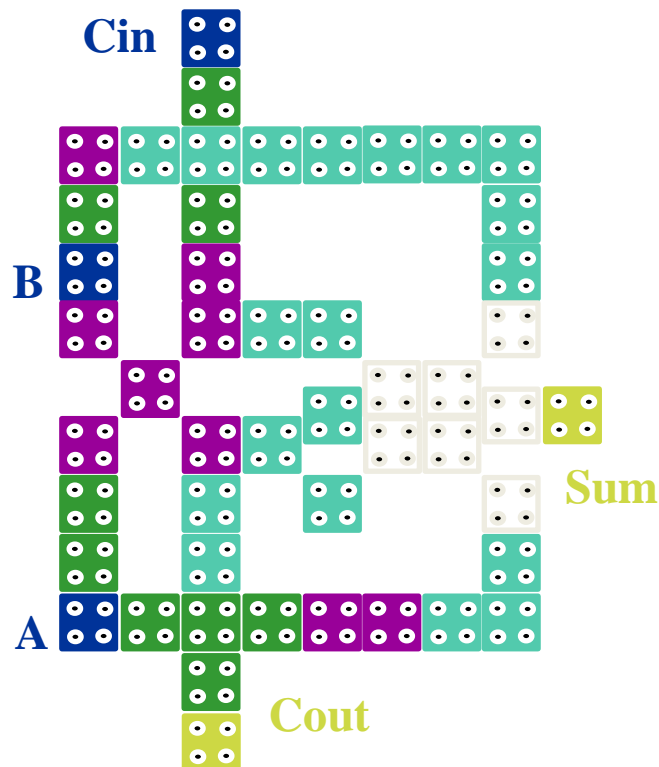


Fig 4.1.1: Existing Full Adder Circuit in QCA

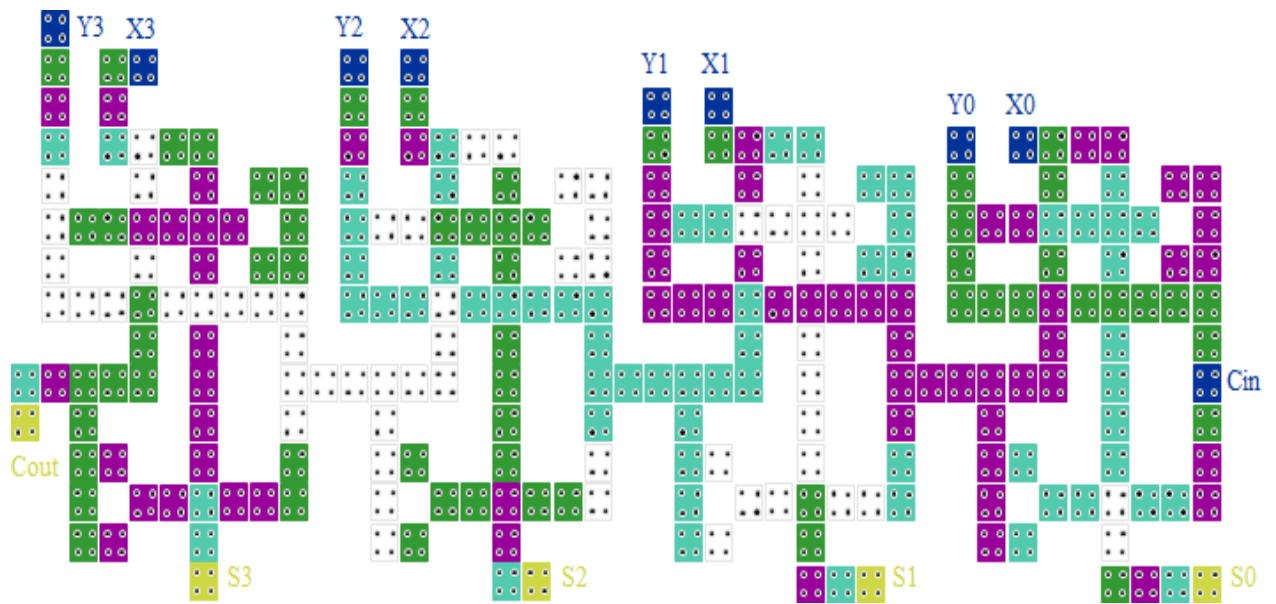


Fig 4.1.2: Existing Ripple Carry Adder Circuit in QCA

Disadvantages:

- Decreasing the amount of consumed space in RCA designed by QCA technology
- Reducing the complexity and latency in RCA designed by QCA technology
- Decreasing the number cells in RCA designed by QCA technology.

CHAPTER – 5: PROJECT IMPLEMENTATION

5.1 AND GATE:

The AND gate is a basic digital logic gate that implements from mathematical logic - AND gate behaves according to the truth table. A HIGH output (1) results only if all the inputs to the AND gate are HIGH (1). If not all inputs to the AND gate are HIGH, LOW output results.

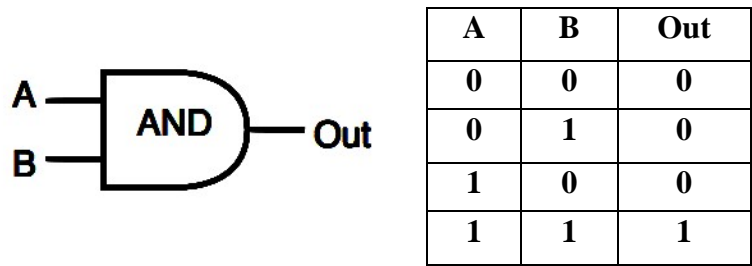


Fig 5.1.1: Symbol and Truth Table of AND Gate

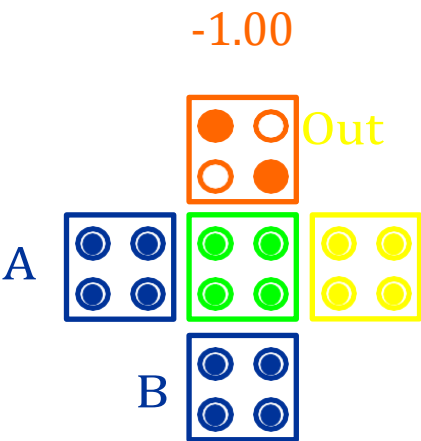


Fig 5.1.2: Implementation of AND Gate using QCA

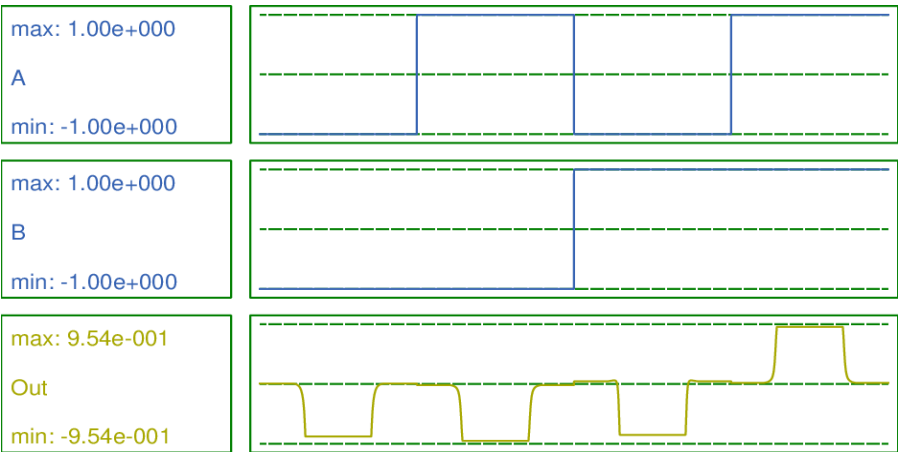


Fig 5.1.3: Simulation results of AND Gate

5.2 OR GATE:

The OR gate is a digital logic gate that implements logical disjunction. The OR gate outputs "true" if any of its inputs are "true" otherwise, it outputs "false". The input and output states are normally represented by different voltage levels.

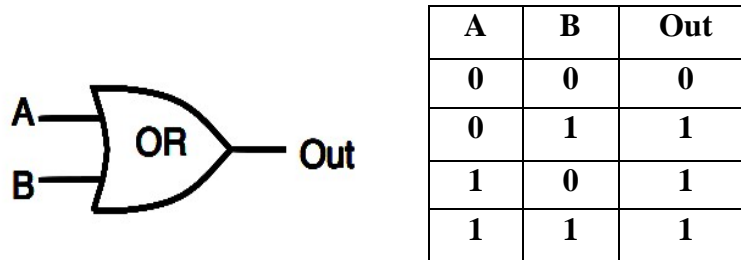


Fig 5.2.1: Symbol and Truth Table of OR Gate

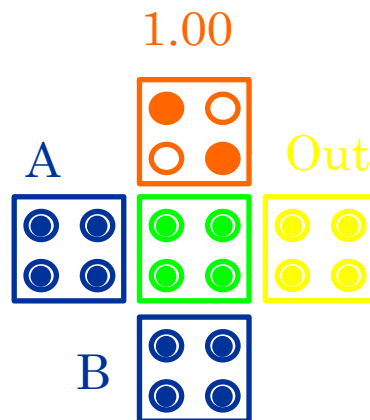


Fig 5.2.2: Implementation of OR Gate using QCA

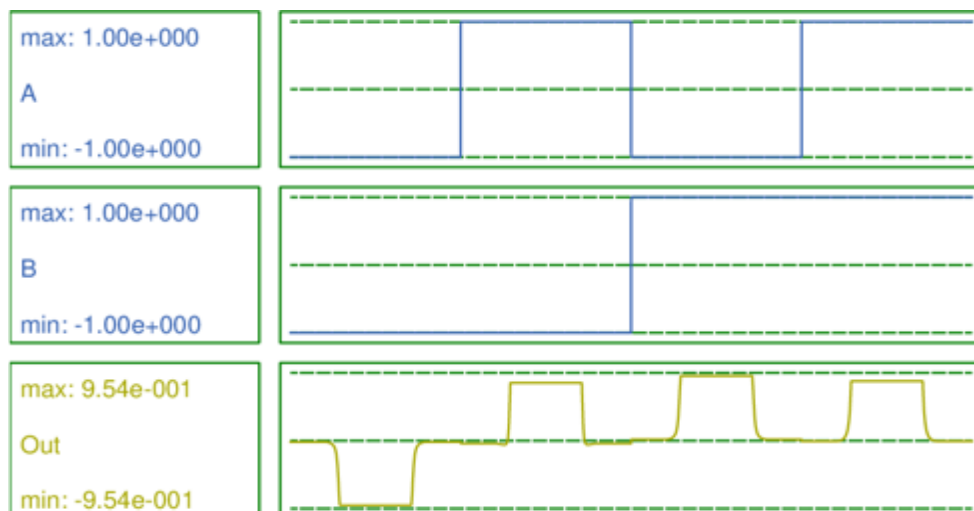


Fig 5.2.3: Simulation results of OR Gate

5.3 NOT GATE:

A NOT gate, also known as an inverter, is a digital logic gate that outputs the opposite of its input signal. A NOT gate has one input and one output, and the output is the opposite of the input. For example, if the input is 1 (true), the output will be 0 (false), and vice versa.

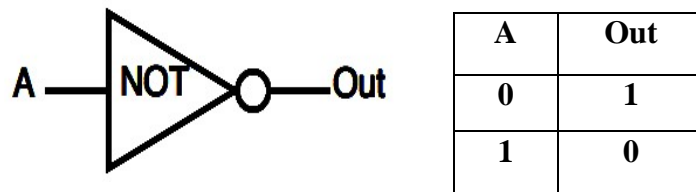


Fig 5.3.1: Symbol and Truth Table of NOT Gate

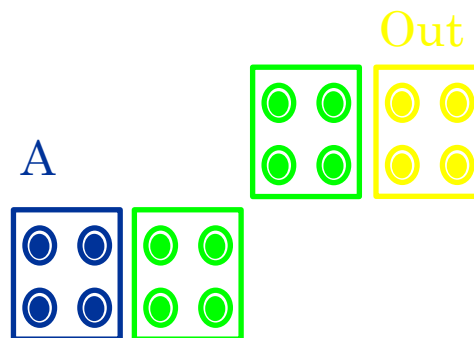


Fig 5.3.2: Implementation of NOT Gate using QCA

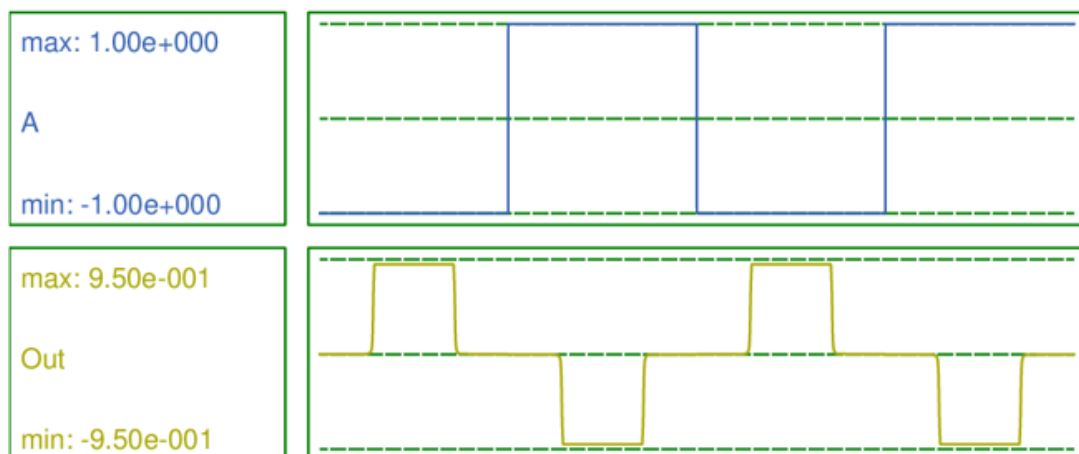


Fig 5.3.3: Simulation results of NOT Gate using QCA

5.4 NAND GATE:

NAND gate is another type of universal logic gate used to perform logical operations. The NAND gate performs the inverted operation of the AND gate. NAND gate produces a low or logic 0 output only when it's all inputs are high or logic 1.

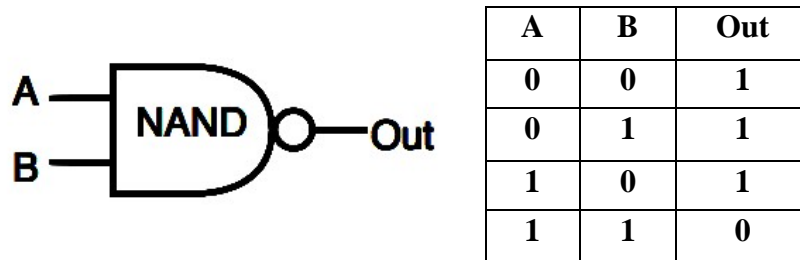


Fig 5.4.1: Symbol and Truth Table of NAND Gate

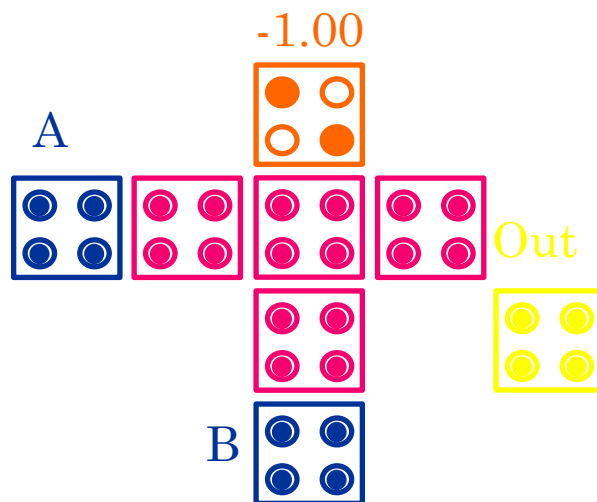


Fig 5.4.2: Implementation of NAND Gate using QCA

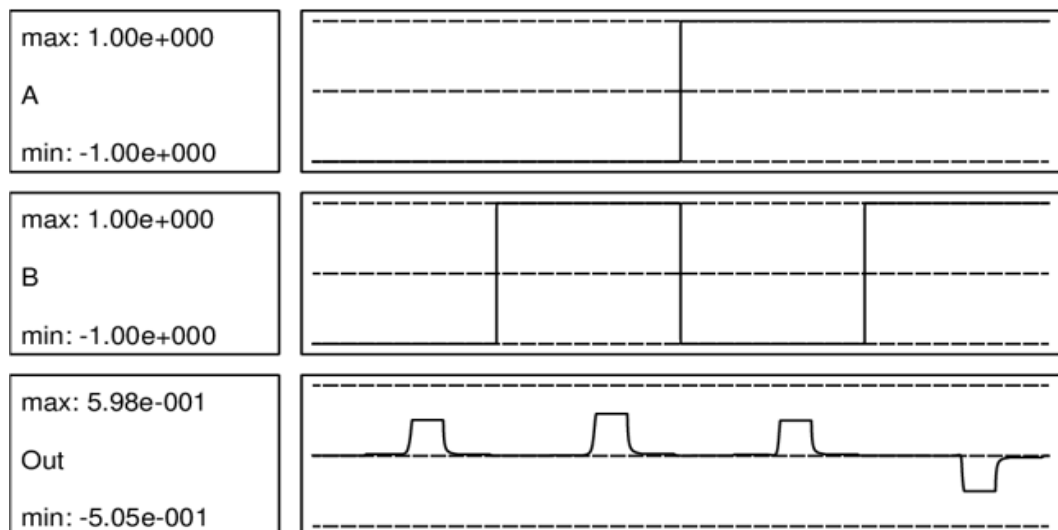


Fig 5.4.3: Simulation results of NAND Gate using QCA

5.5 NOR GATE:

The NOR gate is a type of universal logic gate that can take two or more inputs but one output. It is basically a combination of two basic logic gates i.e., OR gate and NOT gate. A NOR gate gives a high or logic 1 output only when its all inputs are low or logic 0.

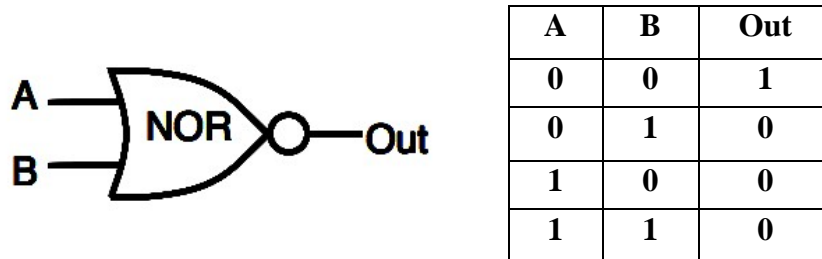


Fig 5.5.1: Symbol and Truth Table of NOR Gate

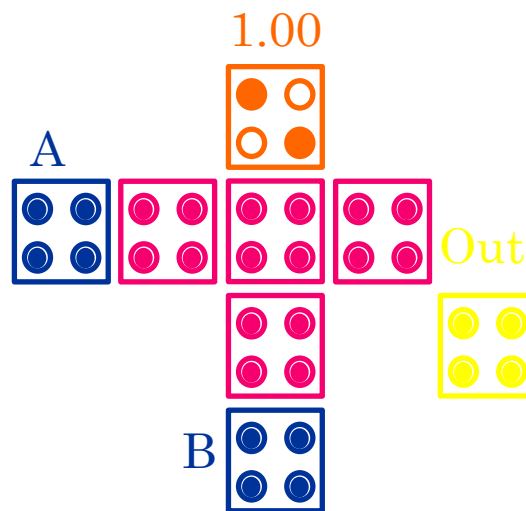


Fig 5.5.2: Implementation of NOR Gate using QCA

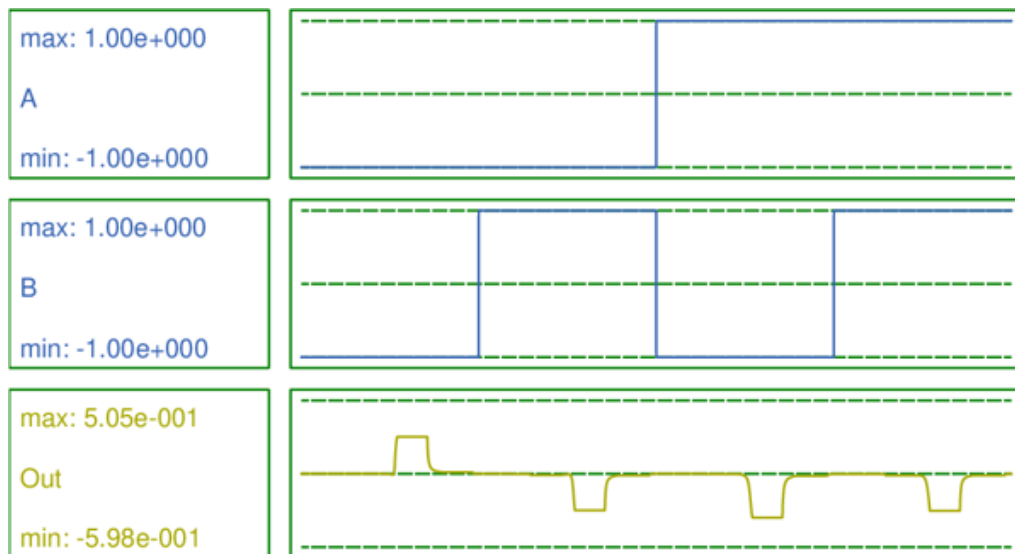


Fig 5.5.3: Simulation results of NOR Gate using QCA

5.6 XOR GATE:

XOR gate is a digital logic gate that gives a true output when the number of true inputs is odd. An XOR gate implements an exclusive or () from mathematical logic; that is, a true output results if one, and only one, of the inputs to the gate is true.

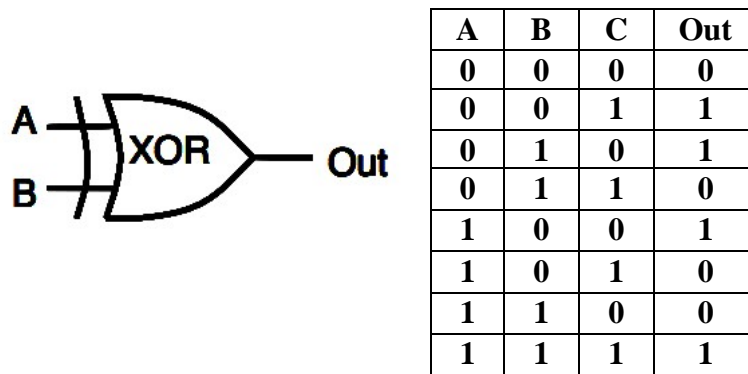


Fig 5.6.1: Symbol and Truth Table of XOR Gate

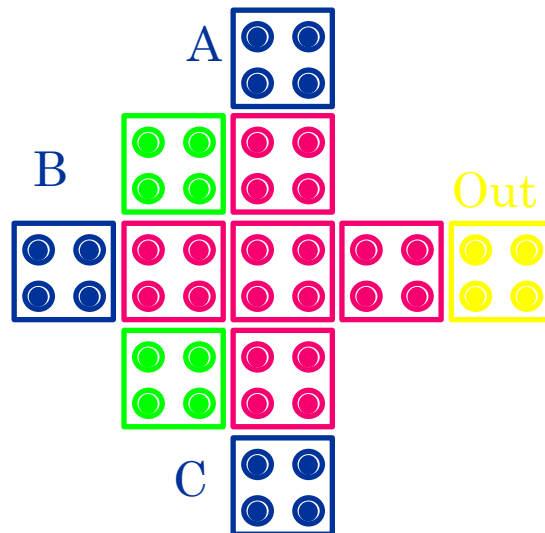


Fig 5.6.2: Implementation of XOR Gate using QCA

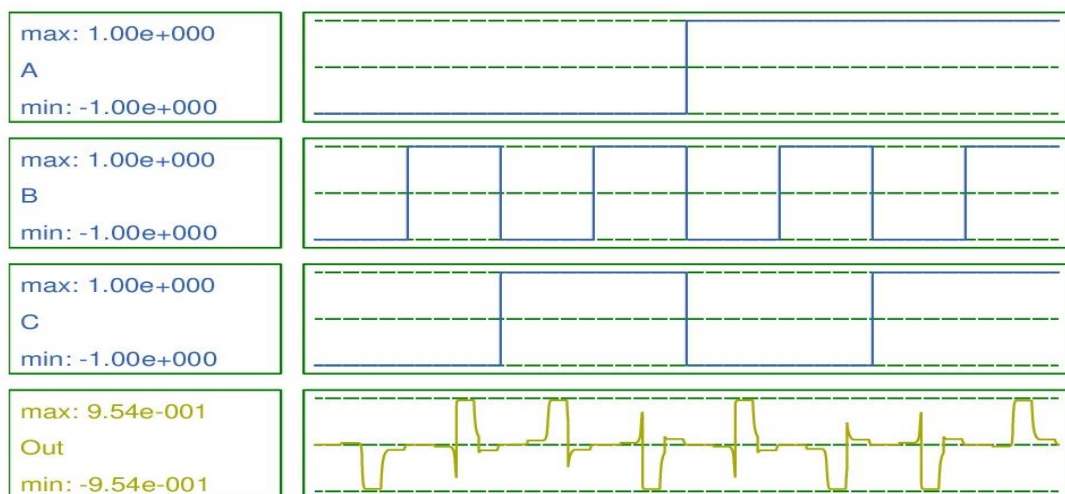


Fig 5.6.3: Simulation results of XOR Gate using QCA

5.7 XNOR GATE:

The XNOR gate is another type of special purpose logic gate used to implement exclusive operation in digital circuits. It is used to implement the Exclusive NOR operation in digital circuits. It is also called the Ex-NOR or Exclusive NOR gate.

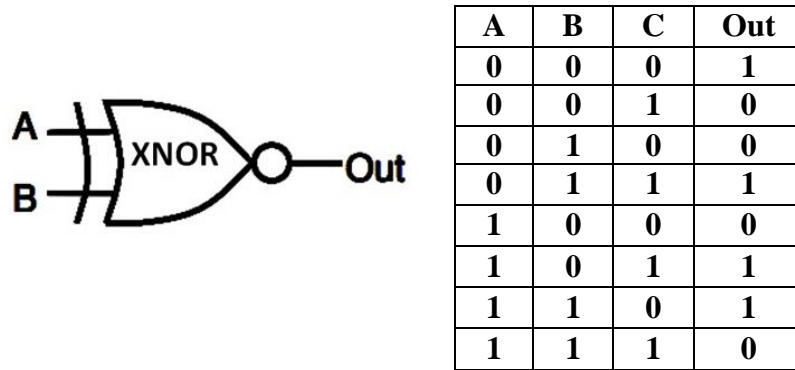


Fig 5.7.1: Symbol and Truth Table of XNOR Gate

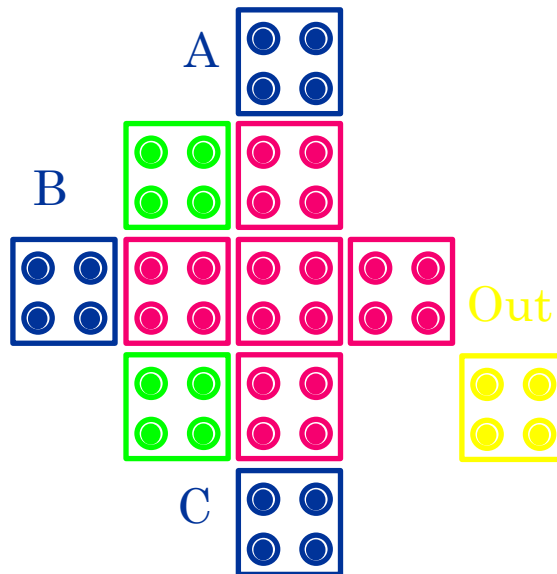


Fig 5.7.2: Implementation of XNOR Gate using QCA

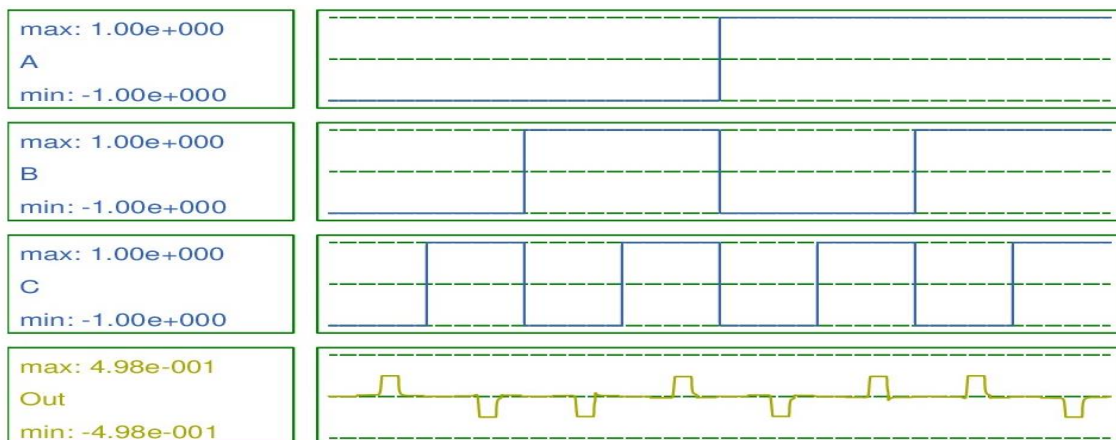


Fig 5.7.3: Simulation results of XNOR Gate using QCA

5.8 PROPOSED TECHNIQUE:

We have proposed the 4-bit Ripple Carry Adder (RCA) with four full adders using Quantum Dot Cellular Automata (QCA) with less cell count and delay compared to the Existing Technique as shown below.

As we know that QCA is called as one of the alternatives of CMOS Technology for developing low-power, high speed digital circuits. To prove that QCA is one of the best tools compared to CMOS technology we have also implemented the 4bit Ripple carry Adder in Mentor graphics tool as well.

5.8.1 FULL ADDER IMPLEMENTATION IN QCA:

Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM. It is a combinational logic circuit. Full adder is the basic element in performing all arithmetic and logical operations in ALU of a processor. Adder architecture is a basic architecture in constructing all digital circuits. Many computational blocks such as multipliers, arithmetic logic unit's (ALU), shift registers are constructed using these adders in QCA technology.

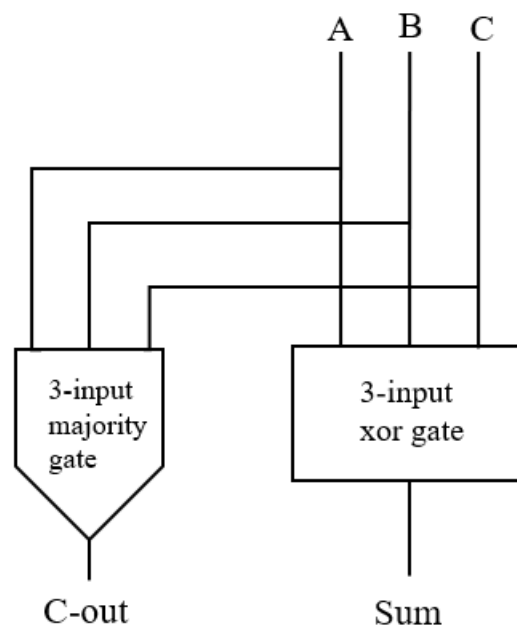


Fig 5.8.1.1: Block Diagram of Proposed Full Adder Circuit

Adders are essential not only for addition, but also for subtraction, multiplication, and division. Addition is one of the fundamental arithmetic operations. A combinational circuit that performs addition of two bits is called a Half Adder.

One that performs addition of three bits is called a Full Adder. A new Full adder is proposed which is designed with minimum QCA cells compared to the existing designs. Also, a Ripple Carry Adder (RCA) is designed using a proposed Full adder which has improved performance in propagation delay and cell count. This adder architecture finds applications in designing all secured Nano-communication network.

Inputs			Outputs	
A	B	C _{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 5.1: Truth Table of Full Adder

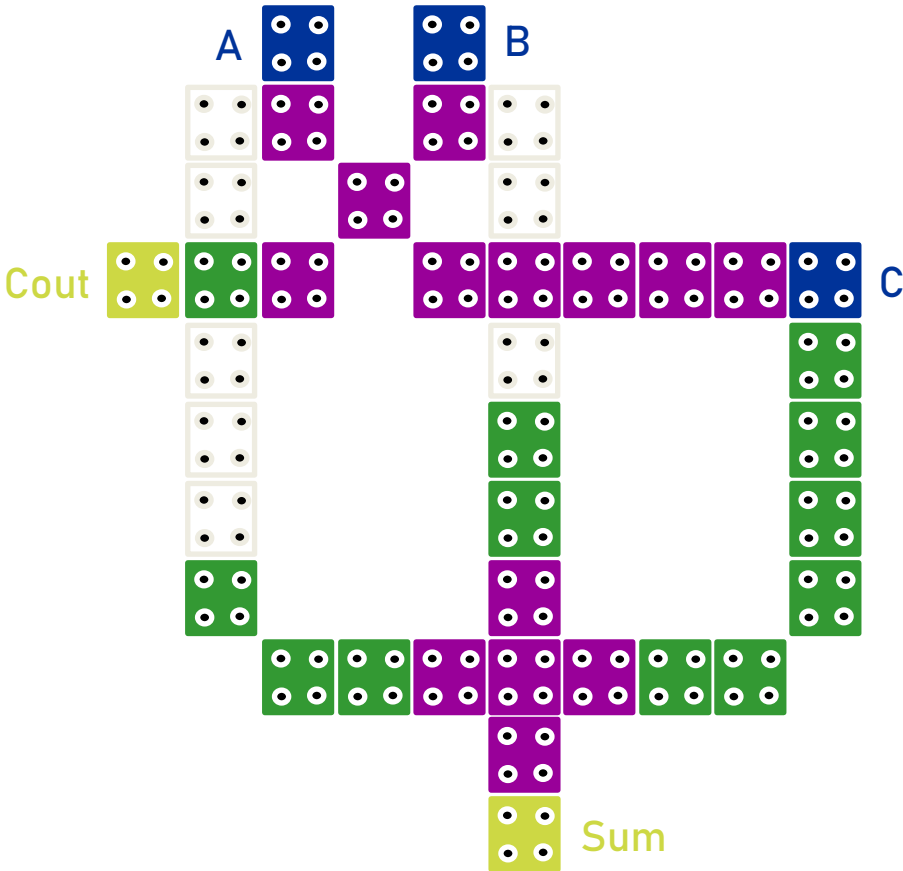


Fig 5.8.1.2: Full Adder Circuit in QCA

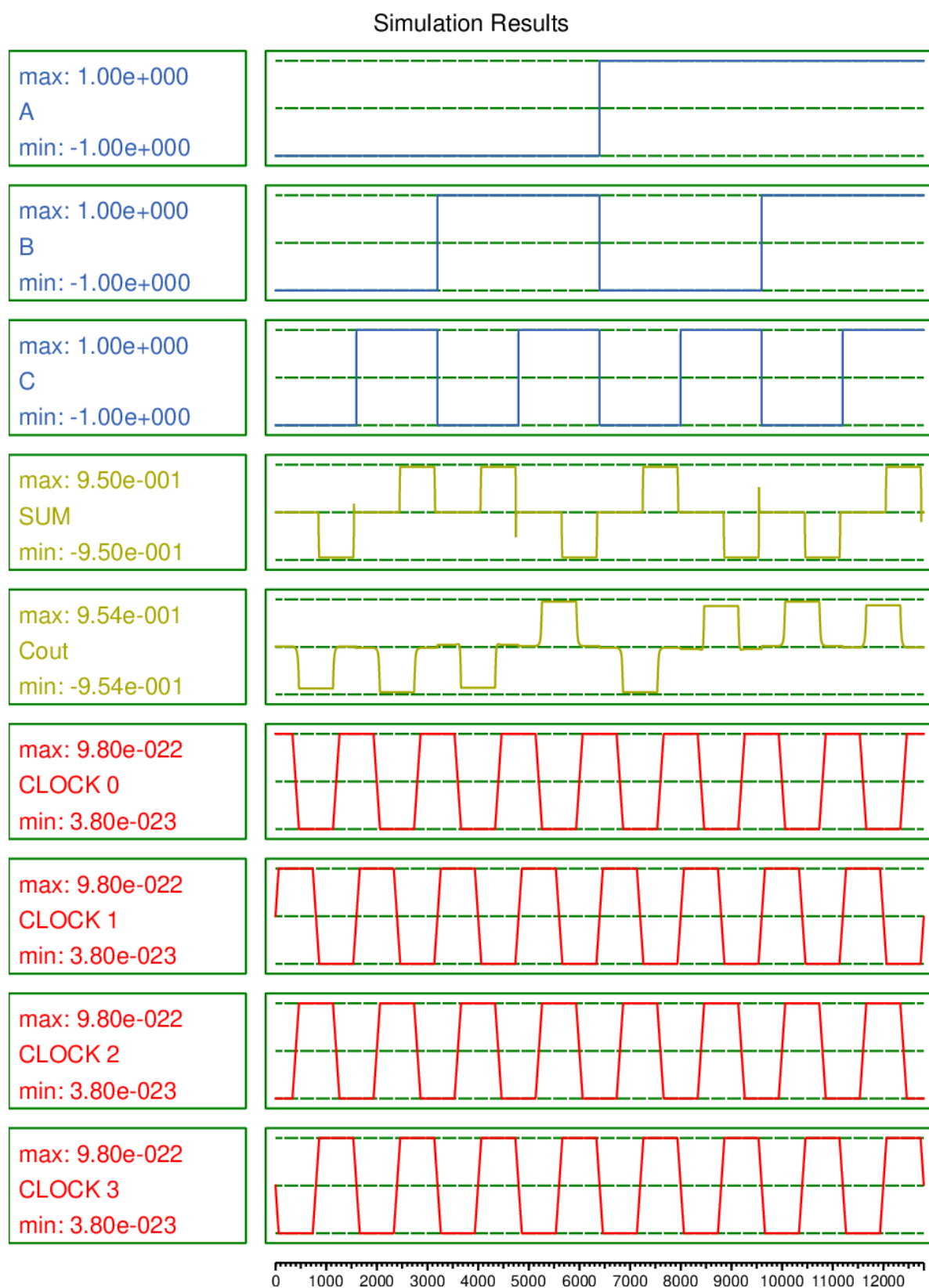


Fig 5.8.1.3: Output waveforms of Full Adder using QCA

5.8.2 RIPPLE CARRY IMPLEMENTATION IN QCA:

A structure of multiple full adders is cascaded in a manner to give the results of the addition of an n bit binary sequence. This adder includes cascaded full adders in its structure so, the carry will be generated at every full adder stage in a ripple-carry adder circuit.

These carry output at each full adder stage is forwarded to its next full adder and there applied as a carry input to it. This process continues up to its last full adder stage. So, each carry output bit is rippled to the next stage of a full adder. By this reason, it is named as “RIPPLE CARRY ADDER”.

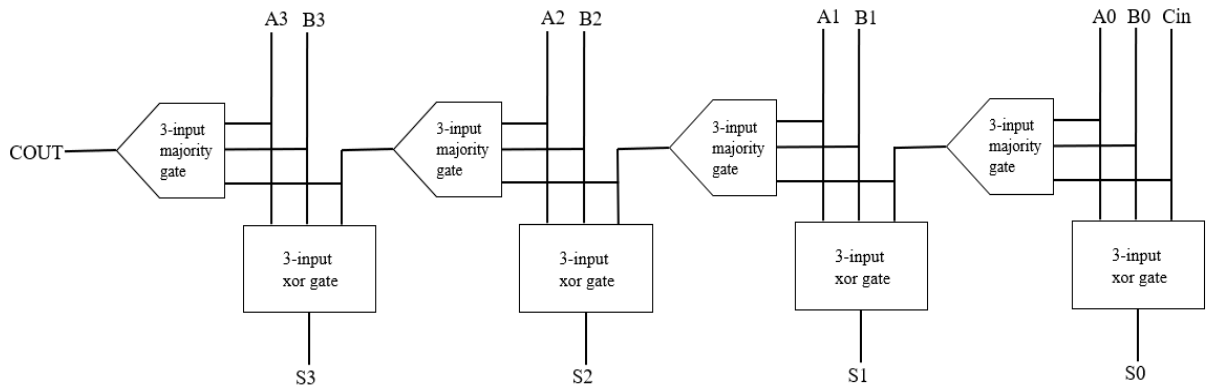


Fig 5.8.2.1: Block Diagram of Proposed 4-Bit RCA in QCA

In QCA, only few Ripple Carry Adders (RCA) are proposed. Also, a Ripple Carry Adder (RCA) is designed using a proposed Full adder which has improved performance in propagation delay and cell count. This adder architecture finds applications in designing all secured Nano-communication network. It describes the existing designed full adders and their limitations. Adder circuits are broadly employed in all digital computation systems.

An efficient 4-bit Ripple Carry Adder (RCA) is designed based on the proposed full adder connected in a way that allows addition of multiple-bit numbers that performs higher end addition in an effective way. A full adder can add one-bit numbers along with a carry bit and provides a sum bit and a carry bit as output. To add two four-bit numbers, you need four full adders, with each full adder adding two bits and the carry from the previous adder.

	A				B				Sum				Carry
Cin	A3	A2	A1	A0	B3	B2	B1	B0	S3	S2	S1	S0	Cout
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	1	0	0	1	0	0
0	0	0	1	0	0	0	1	0	0	1	0	0	0
0	0	0	1	1	0	0	1	1	0	1	1	0	0
0	0	1	0	0	0	1	0	0	1	0	0	0	0
0	0	1	0	1	0	1	0	1	1	0	1	0	0
0	0	1	1	0	0	1	1	0	1	1	0	0	0
0	0	1	1	1	0	1	1	1	1	1	1	0	0
0	1	0	0	0	1	0	0	0	0	0	0	0	1
0	1	0	0	1	1	0	0	1	0	0	1	0	1
0	1	0	1	0	1	0	1	0	0	1	0	0	1
0	1	0	1	1	1	0	1	1	0	1	1	0	1
0	1	1	0	0	1	1	0	0	1	0	0	0	1
0	1	1	0	1	1	1	0	1	1	0	1	0	1
0	1	1	1	0	1	1	1	0	1	1	0	0	1
0	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 5.2: Truth Table of 4-bit Ripple Carry Adder

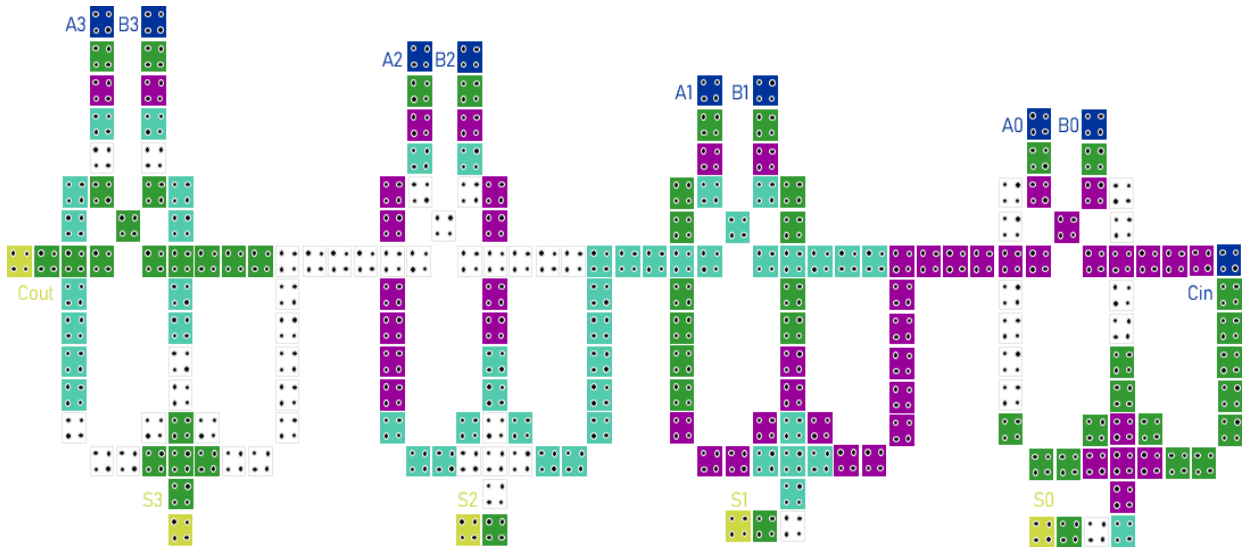
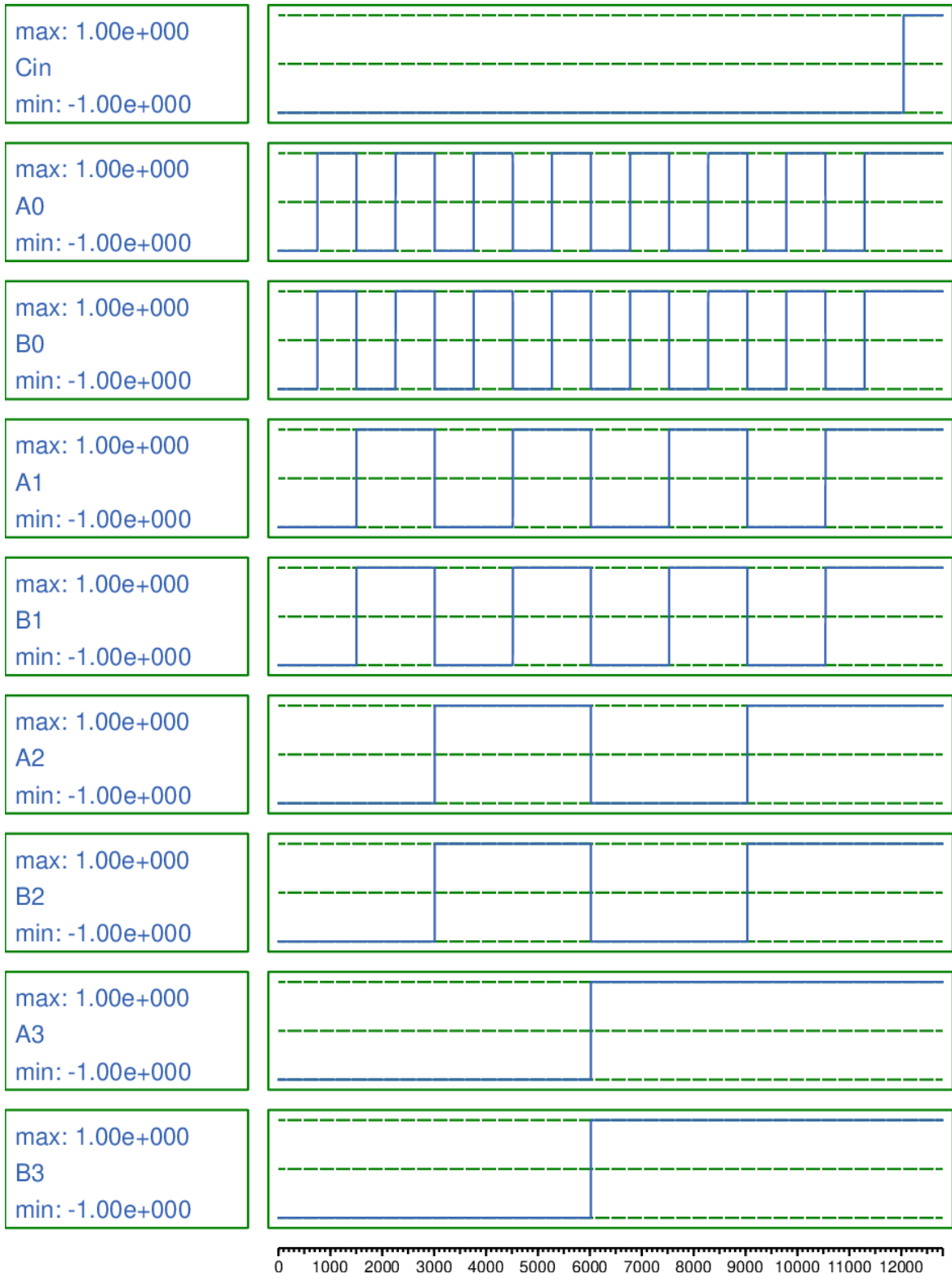


Fig 5.8.2.2: 4-Bit RCA Circuit in QCA

Simulation Results



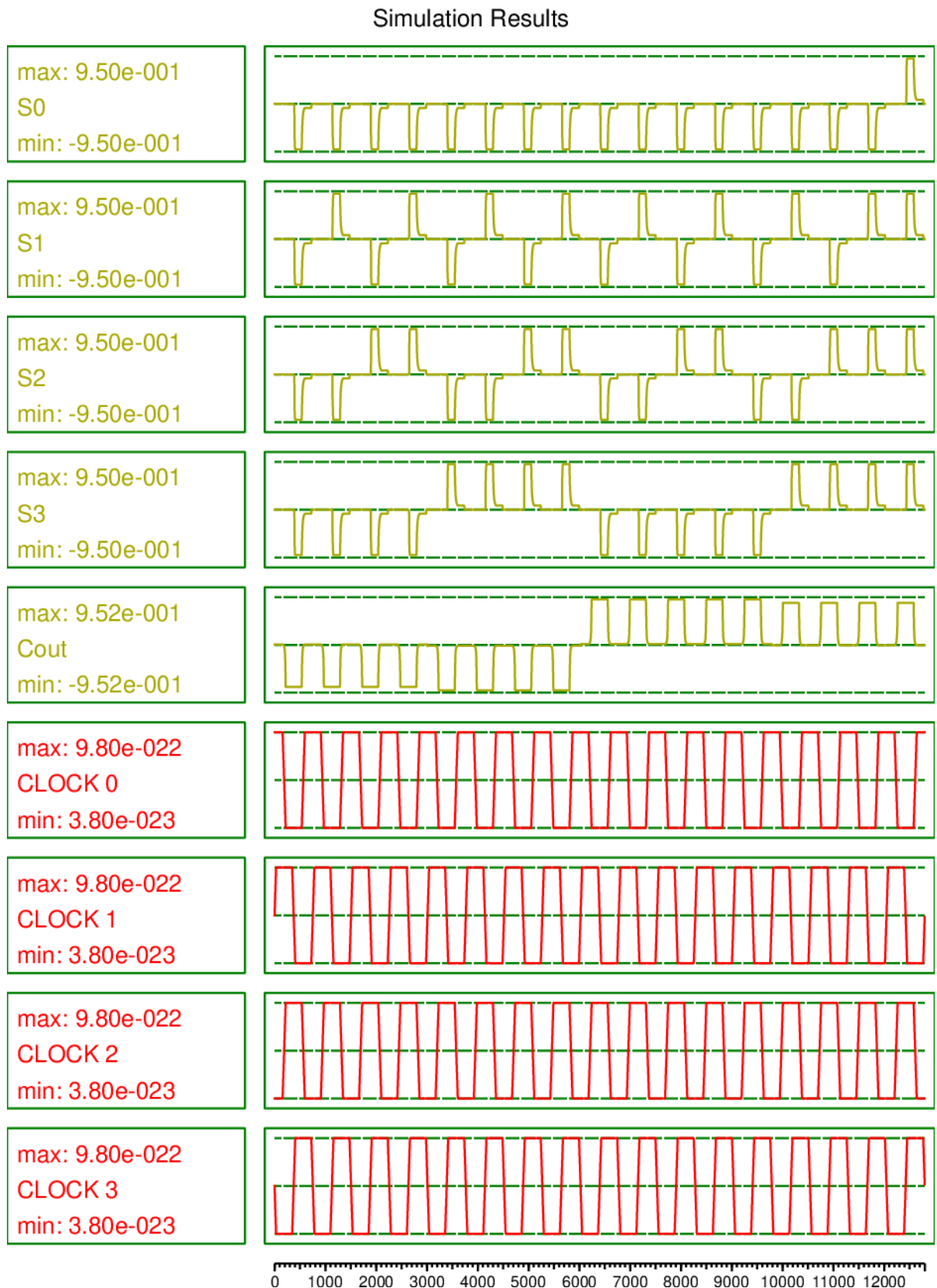


Fig 5.8.2.3: Output waveforms of 4- bit RCA using QCA

5.8.3 FULL ADDER IMPLEMENTATION IN MENTOR GRAPHICS:

The symbols, test benches for the full adder and 4-bit ripple carry adder are as shown in the below figures:

- The full adder has 3 inputs, namely A, B and C and their outputs are SUM and CARRY. The mathematical equation used for the operation of full adder is:

$$\text{SUM} = A \text{ xor } B \text{ xor } C$$

$$\text{CARRY} = AB + BC + AC$$

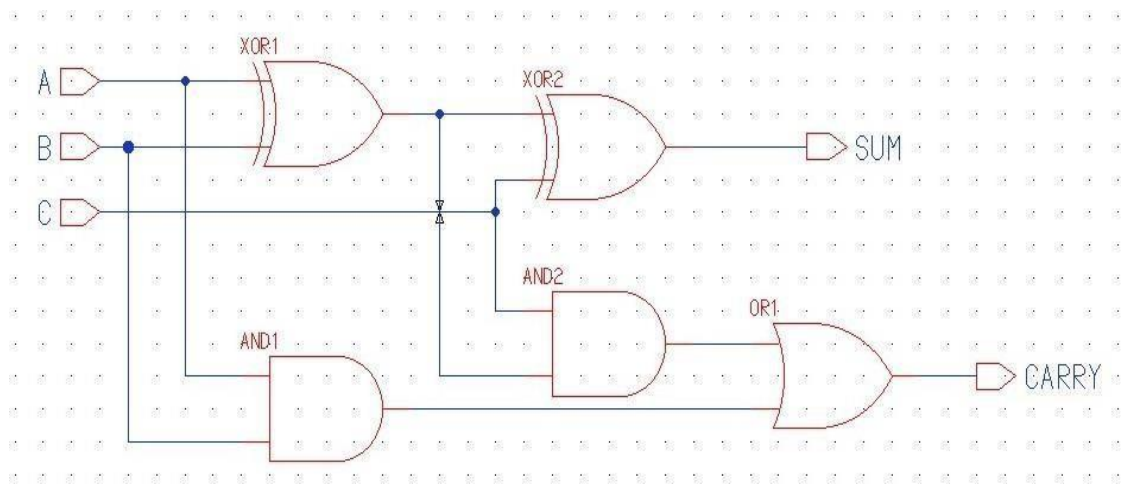


Fig 5.8.3.1: Full Adder Schematic in Mentor Graphics

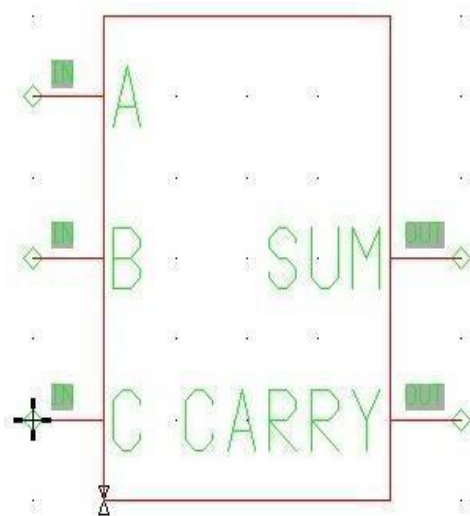


Fig 5.8.3.2: Full Adder Symbol in Mentor Graphics

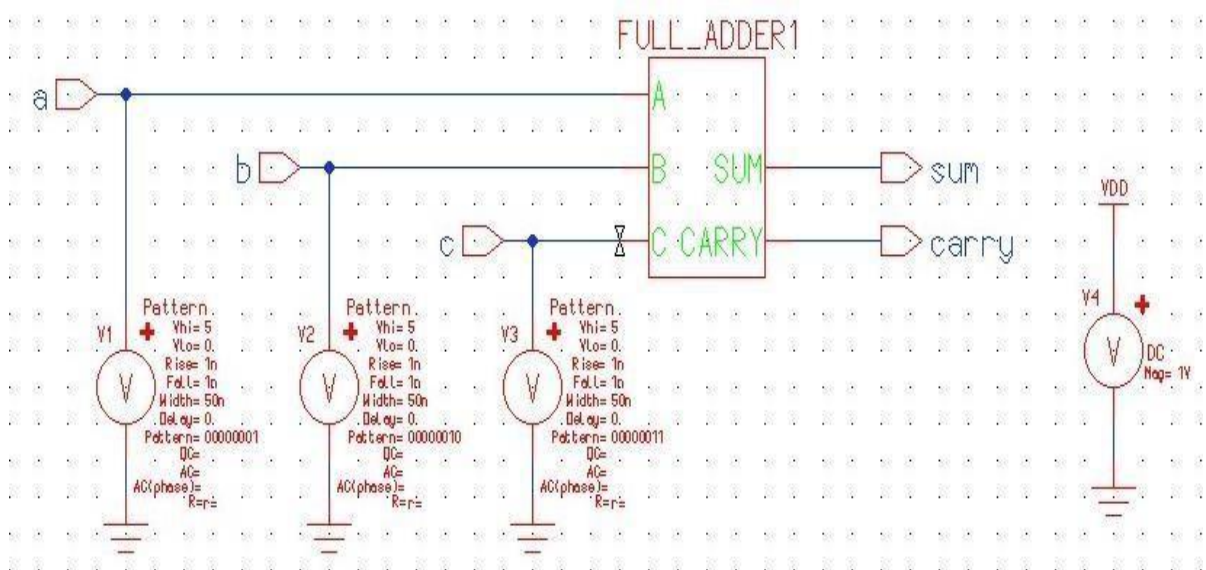


Fig 5.8.3.3: Full Adder Test Bench in Mentor Graphics

5.8.4 RIPPLE CARRY ADDER IMPLEMENTATION IN MENTOR GRAPHICS:

- The 4 – bit ripple carry adder has:
 - It has 8 inputs, namely A1, A2, A3, A4 and B1, B2, B3, B4 and a carry input Cin.
 - It gives 4 outputs namely, S1, S2, S3, S4 and Cout
 - The 1st stage of the ripple carry adder takes A1, B1, Cin as inputs and produces output of S1 and intermediate carry.

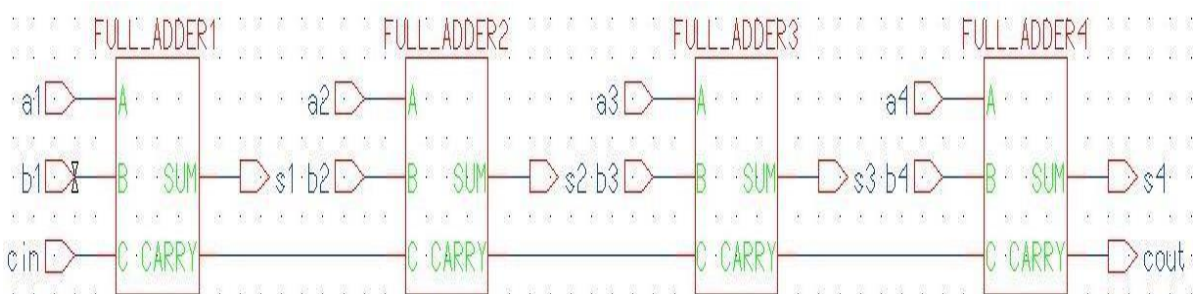


Fig 5.8.4.1: RCA Schematic in Mentor Graphics

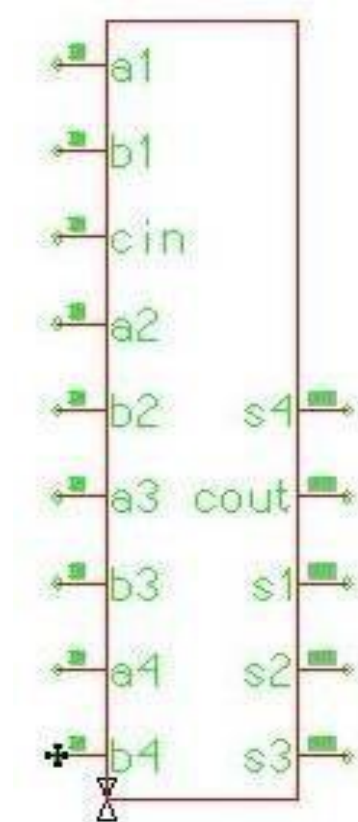


Fig 5.8.4.2: Ripple Carry Adder Symbol in Mentor Graphics

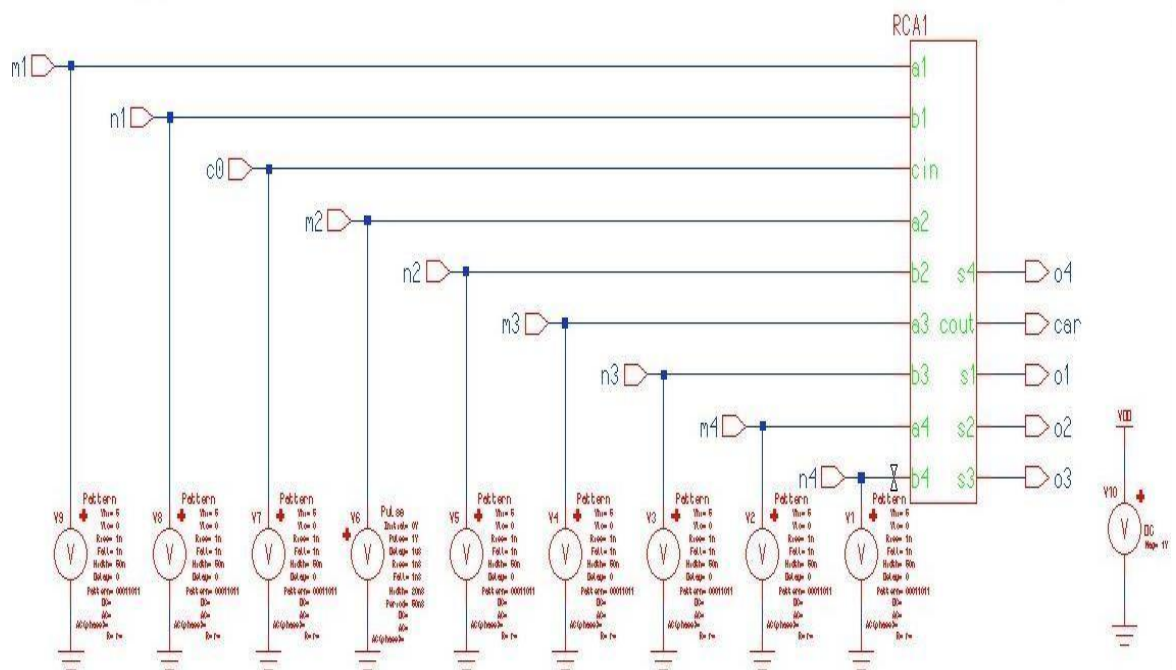
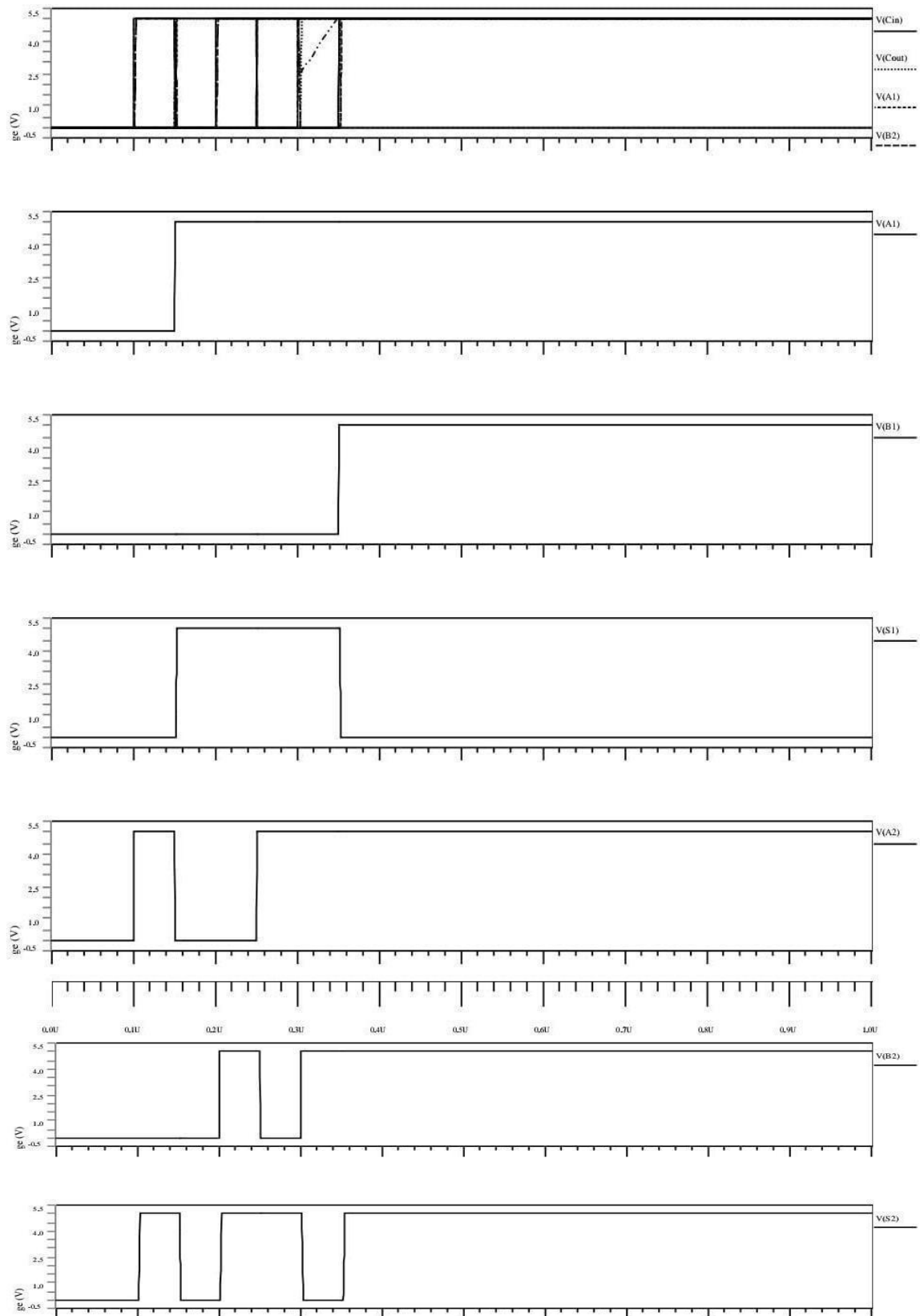


Fig 5.8.4.3: Ripple Carry Adder Test Bench in Mentor Graphics



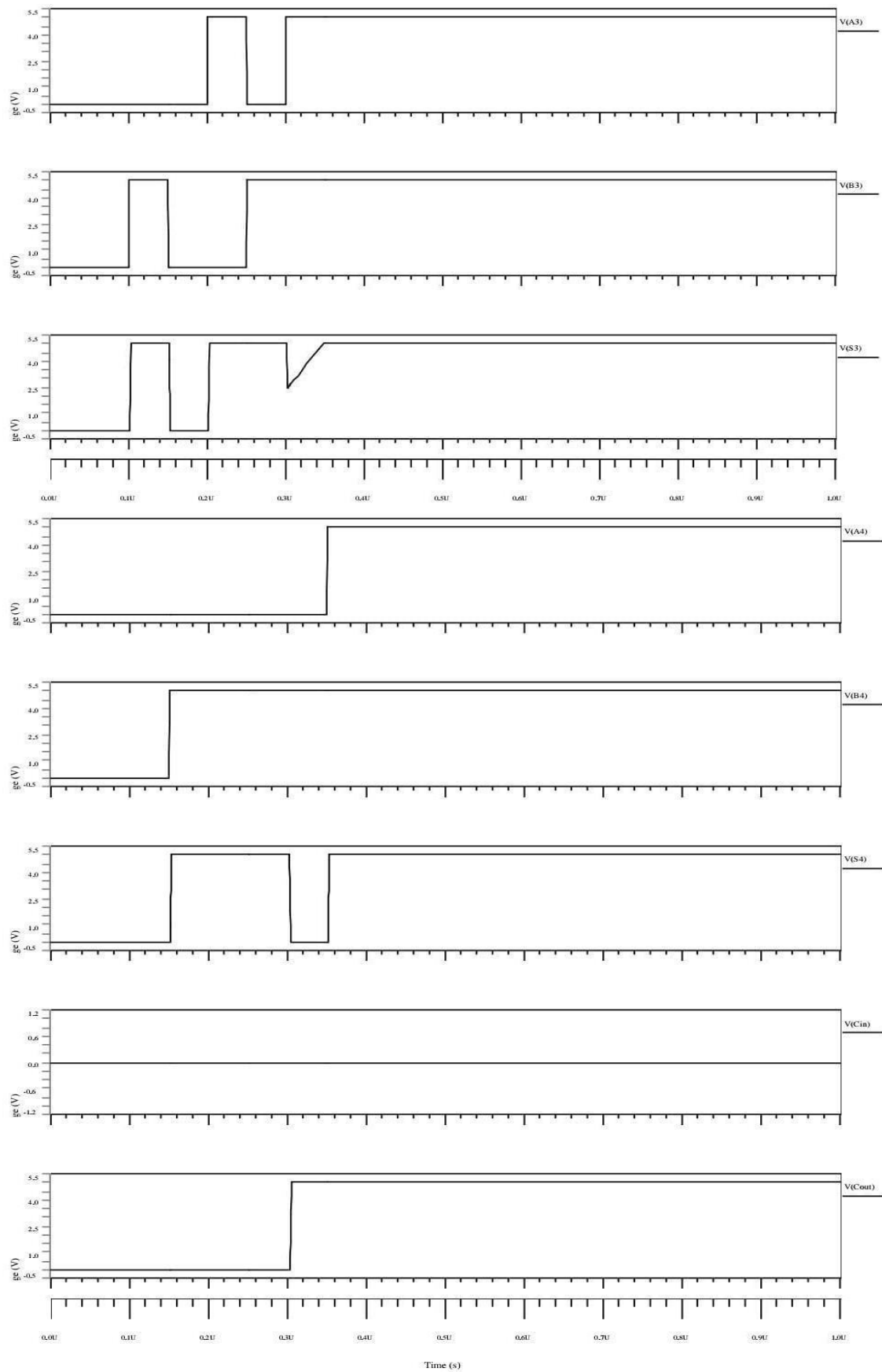


Fig 5.8.4.4: Output waveforms of 4- bit RCA using Mentor Graphic

CHAPTER – 6: RESULTS

The comparison between the adders in Mentor Graphics and Quantum Dot Cellular Automata (QCA) are tabulated below:

The table shows that the area of the full adder circuit in Mentor Graphics is $9 \mu m^2$ and the area in QCA Designer is $0.06 \mu m^2$. The transistor count of full adder in Mentor Graphics is 28 whereas the cell count in QCA Designer is 39.

Parameters	Full Adder in Mentor Graphics	Full Adder in QCA
Area	$9 \mu m^2$	$0.06 \mu m^2$
Transistor Count/ Cell Count	28	39

Table 6.1: Comparison between parameters for Full Adder in Mentor graphics & QCA

The table shows that the area of the 4-bit ripple carry adder circuit in Mentor Graphics is $34 \mu m^2$ and the area in QCA Designer is $0.34 \mu m^2$. The transistor count of 4-bit ripple carry adder in Mentor Graphics is 112 whereas the cell count in QCA Designer is 208.

Parameters	RCA in Mentor Graphics	RCA in QCA
Area	$34 \mu m^2$	$0.30 \mu m^2$
Transistor Count/ Cell Count	112	208

Table 6.2: Comparison between parameters for RCA in Mentor graphics & QCA

Reference	Cell count	Area(μm^2)	Delay
[1]	494	0.68	4.25
[2]	442	1	2
[3]	308	0.29	2
[4]	295	0.3	1.5
[5]	262	0.34	1.75
Proposed	208	0.3	1.25

Table 6.3: Parameter comparison between existing and proposed methods

The table 6.3 shows the area covered, cell count and the delay of the existing circuits and the proposed circuits, they are listed to show that the proposed method is more efficient and faster than the existing circuits.

The comparison between the existing and proposed 4-bit ripple carry adder is tabulated below:

	Existing Circuit	Proposed Circuit
Area	$0.34 \mu m^2$	$0.30 \mu m^2$
Cell Count	262	208
Delay	1.75	1.25

Table 6.4: Comparison between Existing and Proposed Circuits

This table shows the comparison between the existing and proposed circuits, which includes parameters such as area, cell count and delay. The existing circuit has an area of $0.34 \mu m^2$, 262 cell count and delay of 1.75 clock cycles, while the proposed circuit has area of $0.30 \mu m^2$, 208 cells and delay of 1.25 clock cycles. Therefore, the proposed circuit has lesser area, cell count and delay when compared to the existing circuit.

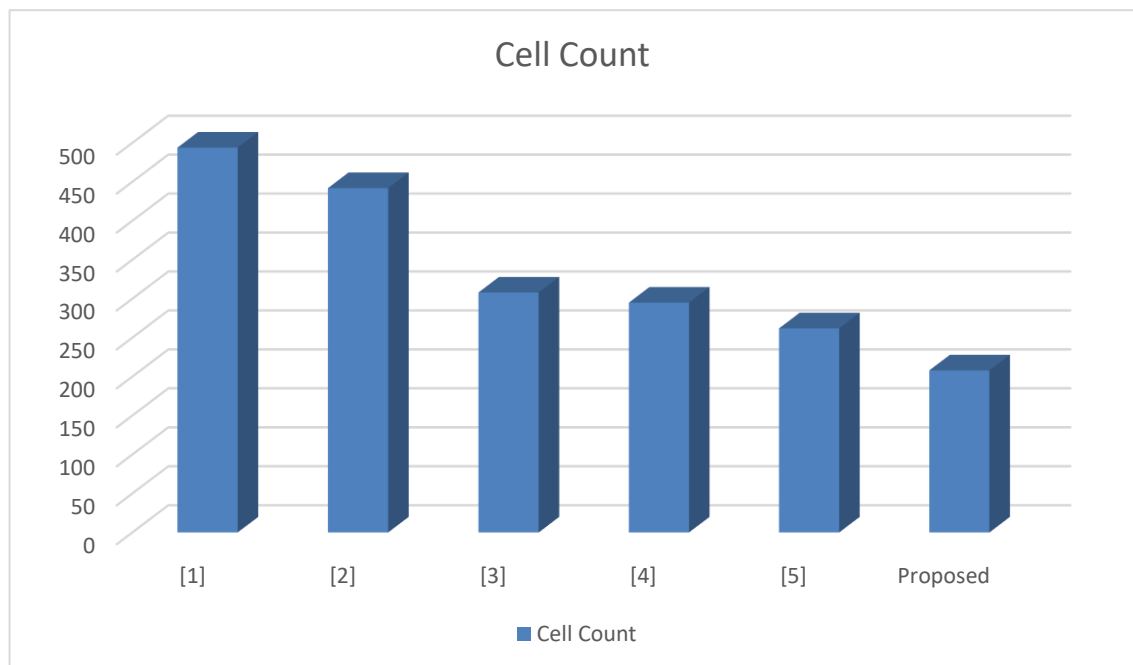


Fig 6.1: Cell count comparison between existing and proposed methods

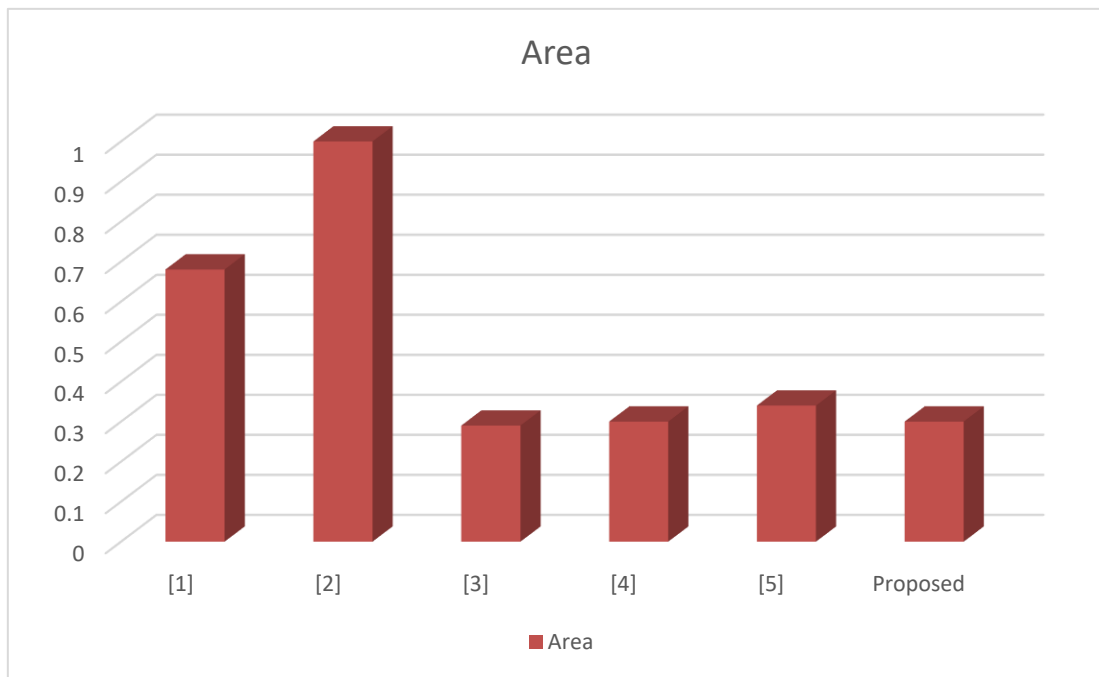


Fig 6.2: Area comparison between existing and proposed methods

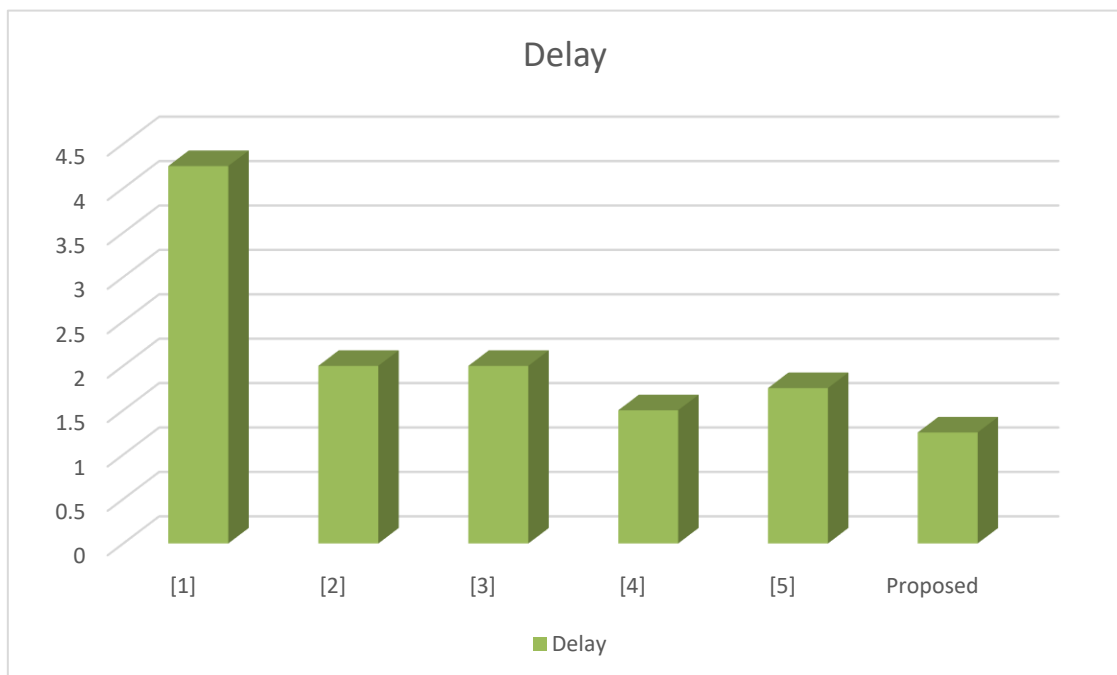


Fig 6.3: Delay comparison between existing and proposed methods

CHAPTER – 7: CONCLUSION AND FUTURE SCOPE

The QCA architecture for 4-Bit Ripple Carry Adder is implemented over here with the help of proposed full adder architecture. The proposed adders have less delay, cell count and lesser area when compared to the existing adders. QCA full adder circuit is proposed which is designed with minimum number of QCA cells. The proposed full adder requires only 39 QCA cells, an area of $0.06 \mu\text{m}^2$ to implement its function. Then an efficient 4-bit Ripple Carry Adder (RCA) is designed based on the proposed full adder that performs higher end addition in an effective way. Also, the simulation results shows that the proposed 4-bit Ripple Carry Adder (RC A) requires only 208 QCA cells, an area of $0.3 \mu\text{m}^2$ and delay of about 1.25 clock cycles to implement its function with enhanced performance in terms of delay, area and cell count.

Future Scope:

In future, high-speed adders which play an important role in multiplier designs could be designed and its computational performance could be improved further. The 4-bit ripple carry adder using QCA are used in Arithmetic Logic Units (ALUs) in processors, Digital Signal Processing (DSP) for faster audio and image processing, strengthening encryption and data security, error detection and correction in communication and storage systems, accelerating data compression techniques for faster transmission and reduced storage requirements, improving performance and energy efficiency in embedded systems, enhancing throughput and scalability in parallel computing architectures and in prototyping and exploration of QCA technology in FPGA-based systems.

CHAPTER - 8: REFERENCES

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