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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

RELEVANCE TO PO's & PSO's :

Project Title : Implementation of 4-Bit RCA using Quantum Dot Cellular Automata and Mentor Graphics.

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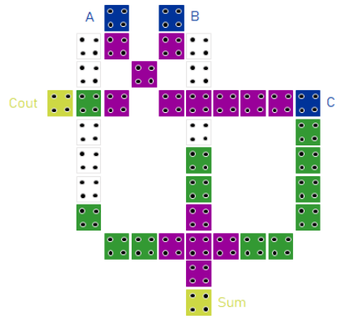
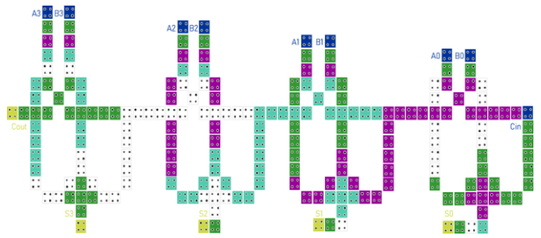
ABSTRACT	PO's Mapping	PSO's Mapping
QCA technology is a new platform, which is a transistor less and wire-less technology, hence it is one of the best alternatives to CMOS technology for developing low power and high-speed digital circuits at nano-scale level. The limitations of CMOS technology such as large number of transistors and wire connections in a small area was overcome by QCA technology. Therefore, we have chosen the QCA technology. Adder is a basic architecture in constructing all digital circuits. First, a full adder is designed in both QCA as well as Mentor Graphics which has improved performance in propagation delay and cell count. Then with the help of 4 full adders a 4-Bit Ripple Carry Adder is implemented in QCA and compared the results with the existing RCA in QCA. From the comparison, it is found that the proposed ripple carry adder has better performance than the existing adder circuits.	**PO1** **PO3** **PO5** **PO8** **PO9** **PO10** **PO12**	**PSO1** **PSO2**

PO1	To implement the knowledge of VLSI to implement RCA.
PO3	Designed the QCA of 4-Bit RCA by using gates.
PO5	We used modern tool named QCA to design the RCA.
PO8	The basic rules have been followed while developing this project.
PO9	Able to work effectively as an individual ,and as a leader/member of team.
PO10	Good communication among members for better output.
PO12	The modifications can be done to this model for the other purpose.

PO1 Engineering Knowledge	PO2 Problem Analysis	PO3 Design &Development of Solution
PO4 Investigations	PO5 Modern toolusage	PO6 The Engineer& Society
PO7 Environment & Sustainability	PO8 Ethics	PO9 Individual &team work
PO10 Communication	PO11 ProjectManagement &Finance	PO12 Life-longLearning

PSO1 Industry-ready in the area of electronics & communications, VLSI.	PSO2 To provide well equipped laboratory infrastructure where anindividual is mentored to develop innovative electronics project





CONCLUSION: QCA full adder circuit is proposed which is designed with minimum number of QCA cells. The proposed full adder requires only 39 QCA cells, an area of 0.06 μm2 to implement its function. Then an efficient 4-bit Ripple Carry Adder (RCA) is designed based on the proposed full adder that performs higher end addition in an effective way. Also, the simulation results shows that the proposed 4-bit Ripple Carry Adder (RC A) requires only 208 QCA cells, an area of 0.3 μm2 and delay of about 1.25 clock cycles to implement its function with enhanced performance in terms of delay, area and cell count. In future, high-speed adders which play an important role in multiplier designs could be designed and its computational performance could be improved further.