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Effective RCA design using quantum dot cellular automata

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ABSTRACT

Quantum dot Cellular Automata (QCA) is a transistor less technology alternative to CMOS for developing low-power, high speed digital circuits. Adder circuits are broadly employed in all digital computation systems. In this paper, a novel coplanar QCA full adder circuit is proposed which is designed with minimum number of QCA cells. The proposed full adder requires only 13 QCA cells, an area of 0.008 μm^2 and delay of about 2 clock cycles to implement its function. Then an efficient 4-bit Ripple Carry Adder (RCA) is designed based on the proposed full adder that performs higher end addition in an effective way. Simulations results are obtained precisely using QCA designer tool version 2.0.3. Also the simulation results shows that the proposed 4-bit Ripple Carry Adder (RCA) requires only 70 QCA cells, an area of 0.18 μm^2 and delay of about 5 clock cycles to implement its function with enhanced performance in terms of latency, area and QCA Cost. From the comparisons, it is found that our work achieves over 55% improvement in QCA cell count.

1. Introduction

QCA technology is a new platform which implements complex VLSI architectures with very less power consumption and achieves high speed at nano-scale level compared to CMOS technology [1]. Also, in CMOS technology, the voltage and current represents the binary values and the circuit switching frequency couldn't be increased beyond certain values.

The limitations of CMOS technology such as high integration density within small area due to large number of transistors and wire connections between them was overcome by QCA technology. In this technology, the binary information could be transmitted through Coulombic repulsion [2] between the neighboring QCA cells. It is a transistor less technology. Here, the binary value 0 or 1 is encoded through the reconfigurations of electrons in the quantum dots of QCA cells.

Adder architecture is a basic architecture in constructing all digital circuits [3]. Many computational blocks such as multipliers, arithmetic logic unit's (ALU), shift registers are constructed using these adders in QCA technology. Many high speed DSP processors architecture designs and parallel computations also depends on adder design. Many adders were constructed and implemented previously in QCA [2–9]. In this paper, a new Full adder is proposed which is designed with minimum QCA cells compared to the existing designs. In QCA, only few Ripple Carry Adders (RCA) [3,15,20] are proposed. Also a Ripple Carry Adder (RCA) is designed using a proposed Full adder which has improved performance in propagation delay and cell count. This adder architecture finds applications in designing all secured Nano-communication network.

The rest of the paper is organized as follows: Section 2 describes the fundamental information in QCA. Section 3 describes the existing designed full adders and their limitations. Sections 4 and 5 presents the proposed 1-bit full adder and 4-bit Carry propagation adder design and their implementations. Section 6 presents the performance evaluation of the proposed adders and previous adder design. Results and comparison are discussed in Sections 7 and 8 gives the conclusion of the proposed work.

2. QCA basics

2.1. Quantum dot cellular automata cell and QCA wire

QCA based circuits are constructed using QCA cells. The square shape QCA cells [1] comprises of four quantum dots with two dots occupied by electrons. These electrons resides over in the diagonal corner of the cell due to Coulombic repulsion [3] of force between them. Tunneling of electrons between the quantum dots results in two polarized states. These states namely PL = −1 and PL = +1 [1,3] represents logic value '0' and '1' respectively as shown in Fig. 1(a).

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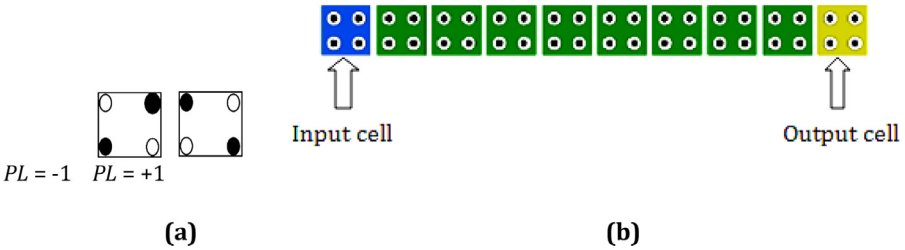


Fig. 1. (a) Polarization state of a cell (b) QCA wire.

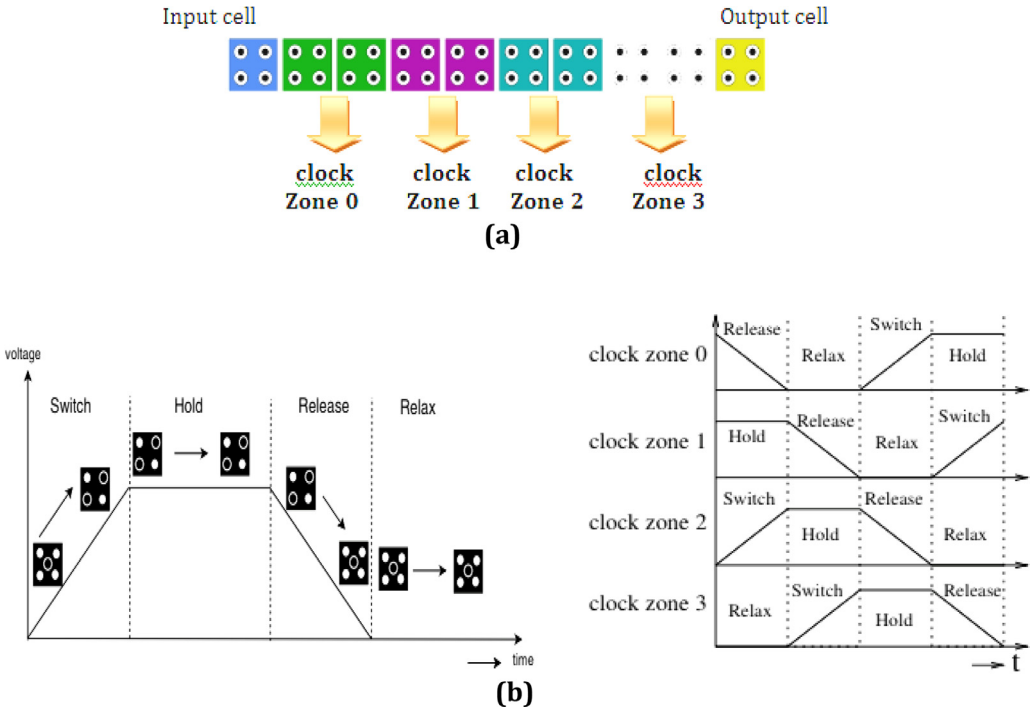


Fig. 2. (a) Clock zones of QCA cells (b) QCA clocking.

Wires in QCA, are constructed either using normal cell or rotated cell [12]. Due to its less complexity, normal cell as shown in Fig. 1(b) are preferred over compared to rotated cell [16]. The polarization state of cells gets changed when input is applied at one end of the wire. Based on the polarization [11] either logic '0' or logic '1' will be a transmitted horizontally or vertically.

2.2. QCA clocking

Two ways of Clocking is performed: zone clocking and continuous clocking. The input is directed towards the output precisely under zone clocking. The propagation delay in QCA circuits is reduced far by assigning the clock zones to different parts of the circuits which will change the potential barrier between quantum dots. As shown in Fig. 2(a) there are four clock zones [1,10] in QCA circuits are clock zone 0, clock zone 1, clock zone 2, and clock zone 3 whose phase differs by 90°. The cells with identical color are assigned the same clocking zone. Accordingly there are four phases [18] in QCA circuits namely switch, hold, and release and relax phase [8] respectively as shown in Fig. 2(b).

Clocking in QCA is used to control the polarization state of cells. In a circuit designed using QCA, the overall delay is proportional to the number of zones within the path with the longest delay.

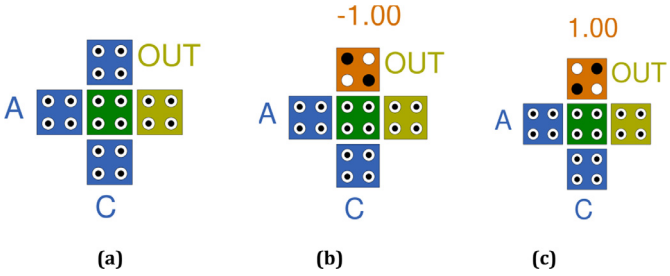


Fig. 3. (a) Majority voter gate (b) AND gate (c) OR gate.

2.3. QCA logic gates

Designing the QCA circuit generally requires an Inverter, QCA wire and a three-input Majority Voter gate [16]. The signal propagates in QCA wire as a result of the electricity interlinkage between cells. A Majority Voter gate has five cells. Among five, three cells works as input cells and one cell works as output cell as given in Fig. 3(a). The middle cell is called as device cell (8) and its logic operation depend on logic of input cells. The equation given in

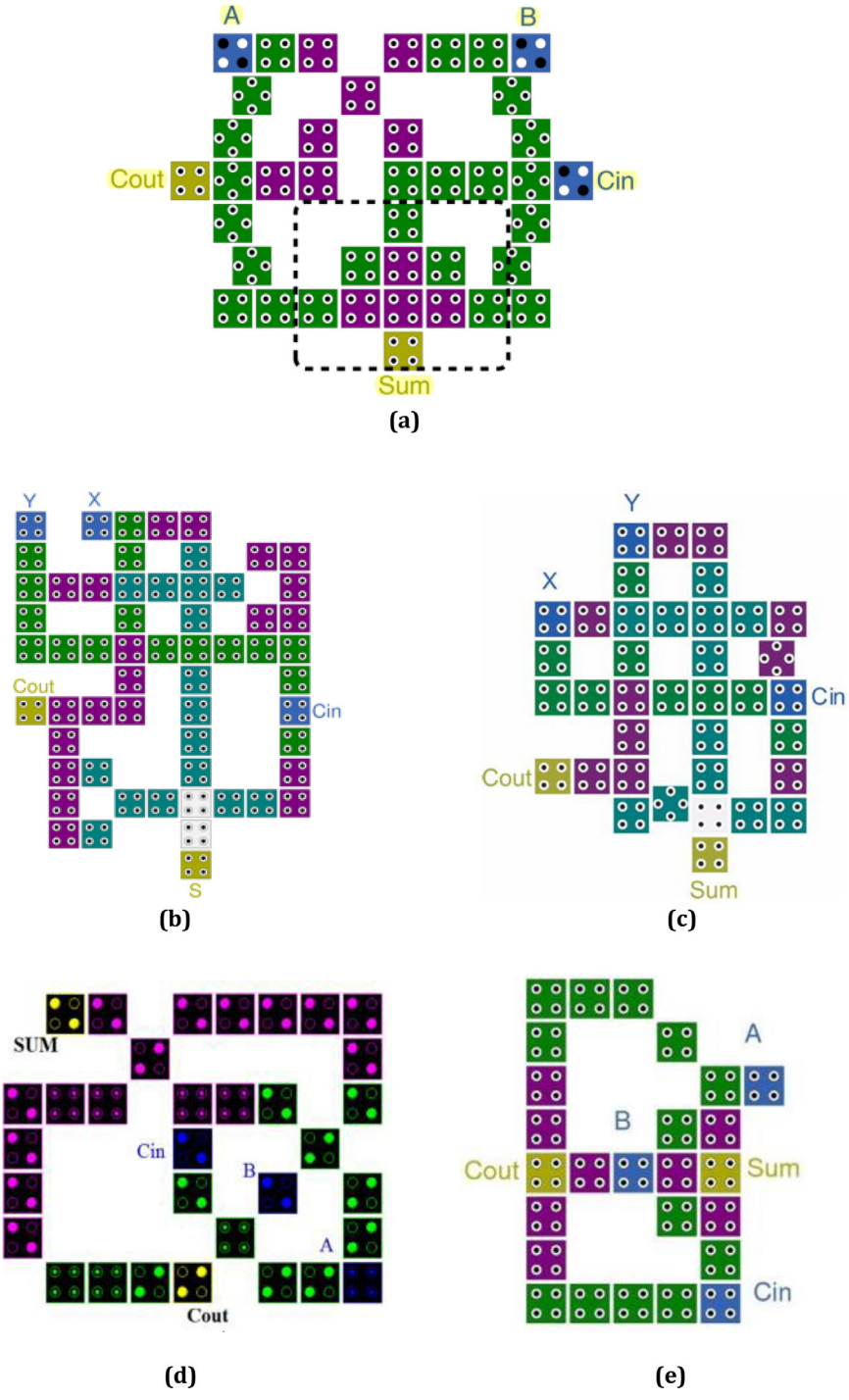


Fig. 4. QCA layout of earlier designs (a) In (3) (b) In (6) (c) In (7) (d) In (9) (e) In (22).

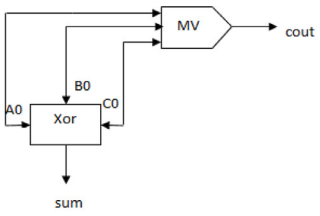
(1) explains the Boolean logic of Majority Voter gate.

$$MV(A,B,C) = F = (A^*B) + (B^*C) + (C^*A) \quad (1)$$

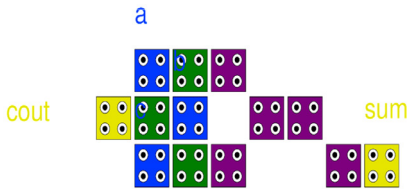
Where A, B, C are inputs and F is the output. With Majority Voter gate, AND gate is constructed as shown in Fig. 3(b). Among the three input cells of the AND gate, one cell is having a fixed polarization PL = -1. Logical function implementation of AND gate is Y = A * B. Also a Majority Voter gate is used to construct an OR-gate as shown in Fig. 3(c). Among the three input cells, one cell is having a fixed polarization PL = +1. Logic function for OR gate implementation is, Y = A + B.

3. Existing designs

Trailokya and Ashutosh (3) designed a one-bit Full adder which consists of three-input XOR gate and a three-input majority gates. This design incorporates a QCA cell count of about 40 cells as shown within the Fig. 4(a). An increase in the QCA cell count ends up in an increase of the area and delay of the design. Abedi and Jaberipur [6] designed a Full adder that has 59 QCA cells and delay of 1 clock phases as shown within the Fig. 6(b). Mersede and Keivan (7) designed a Full adder that requires three majority and two inverter gates. The adder in this design comprises of 37 QCA



(a)



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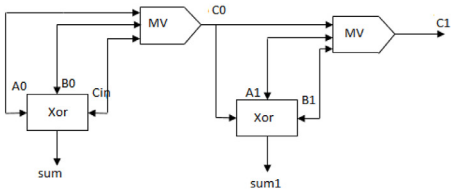
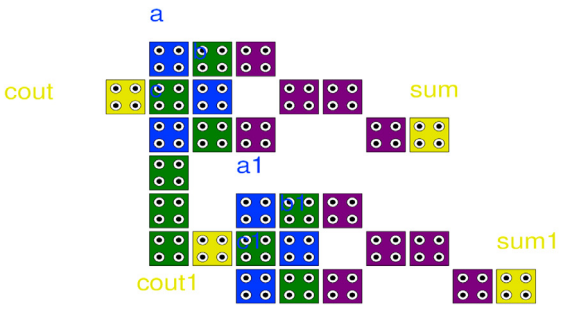
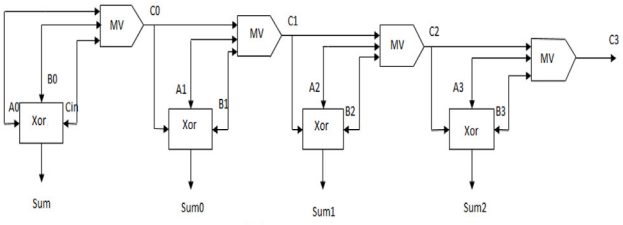


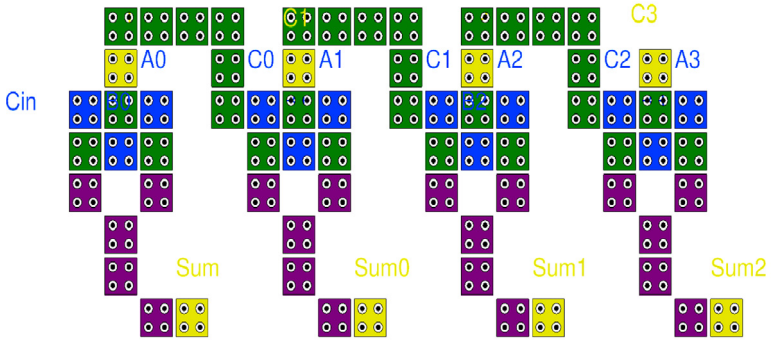
(c)



(d)



(e)



(f)

Fig. 5. (a) Schematic diagram of 1-bit full adder (b) 1-bit full adder (c) Schematic diagram of 2-bit RCA (d) Layout of 2-bit RCA (e) Schematic diagram for 4-bit RCA (f) Layout of 4-bit RCA.

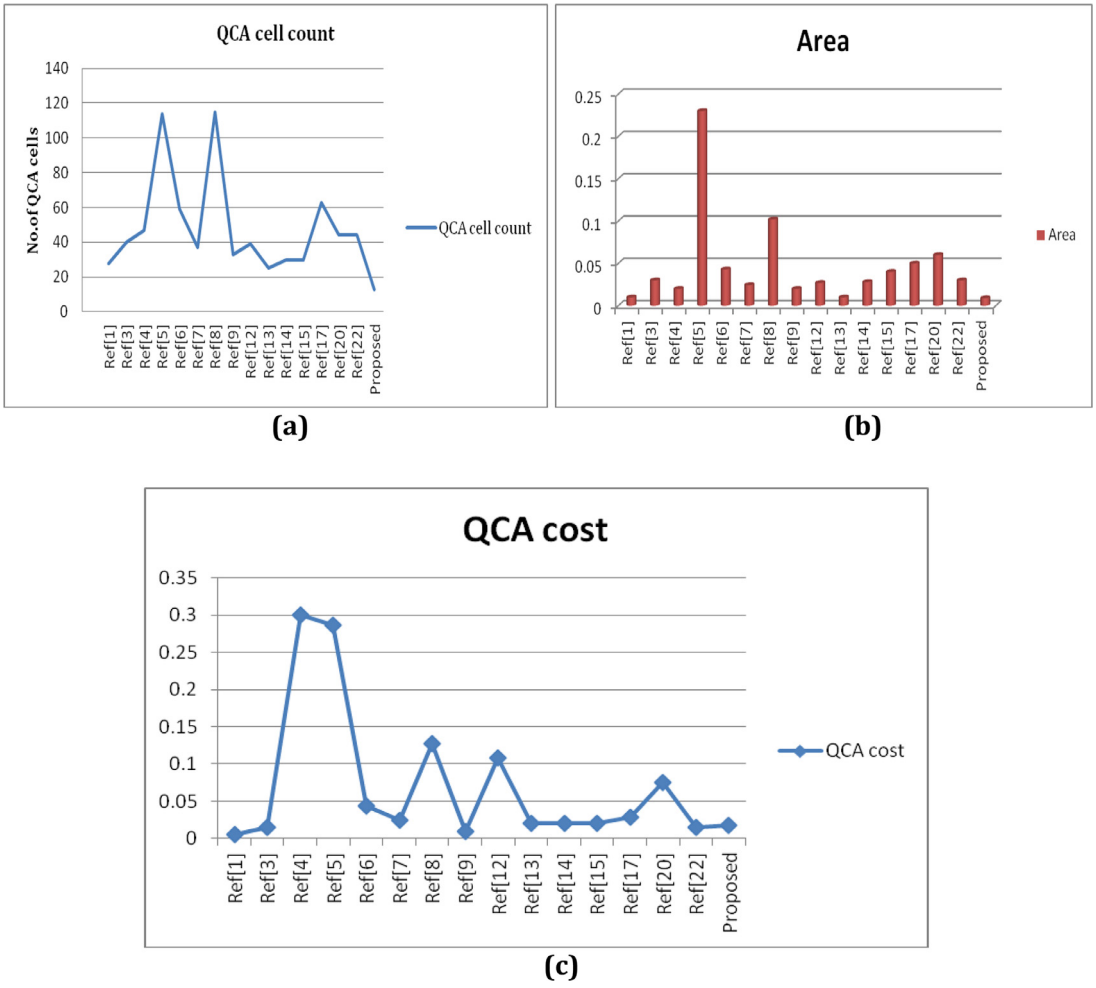


Fig. 6. Comparison of 1-bit full adder (a) QCA cell count (b) Area (c) QCA cost.

cells which require more than two clock phases for generating the carry and sum outputs as shown within the Fig. 6(c). Hamid and Abdalhossein (9) designed a 1-bit QCA full adder that has 33 QCA cells and delay of 2 clock phases as shown within the Fig. 6(d). Shahram and Ali [22] designed a Full adder that has 26 QCA cells and delay of 2 clock phases as shown within the Fig. 6(e).

4. Proposed 1-bit full adder design

Full adder is the basic element in performing all arithmetic and logical operations in ALU of a processor. To obtain an efficient architecture in terms of latency, area and delay here a coplanar implementation of Full adder has been designed which is given in Fig. 5(a). Coplanar crossover is preferred over multilayer crossover because properly aligned regular QCA cells and 45° rotated cells that do not interact with each other could be used. Also the complex circuits could be realized easily using coplanar crossover. This adder comprises of an inverter and a Majority Voter gate. So, minimum number of logic gates has been preferred over here which minimize the QCA cell count and delay. Let the three inputs of full adder are A_0, $B_{0,}$ and C_i and their corresponding outputs are Sum and Carry. The inputs are given to the full adder using three-input MV gate.

The sum output of full adder are derived as per Eqs (2)–(4). Finally derived equations representing the sum and carry output of full adder are given in (5), (6) and (7).

$$Sum = A_0{}'B_0{}'C_0 + A_0B_0C_0{}' + A_0B_0C_0 + A_0B_0{}'C_0{}' \tag{2}$$

$$Sum = A_0{}'\left(B_0{}'C_0 + B_0C_0{}'\right) + A_0\left(B_0C_0 + B_0{}'C_0{}'\right) \tag{3}$$

$$Sum = A_0{}'(B_0 \oplus C_0) + A_0(B_0 \oplus C_0)' \tag{4}$$

$$Sum = A_0 \oplus B_0 \oplus C_0 \tag{5}$$

$$C_{out} = MV(A_0, B_0, C_0) \tag{6}$$

$$C_{out} = (A_0B_0) + (B_0C_0) + (C_0A_0) \tag{7}$$

The adder proposed here requires only thirteen QCA cells with two clock phases which was not yet achieved in previous design. The area required for the proposed full adder is about 0.009 μm^2 which reinforces the implementation of the design. This design attains the lowest latency owing to the less count of QCA cells. The QCA layout is shown in Fig. 5(b).

5. Proposed higher adder circuit

The proposed Full adder is very simple in implementing higher adder designs. Using this Full adder, higher adders like 2-bit and 4-bit RCA (Ripple Carry Adder) has been designed with reduced number of QCA cells that stands completely different from the earlier designs.

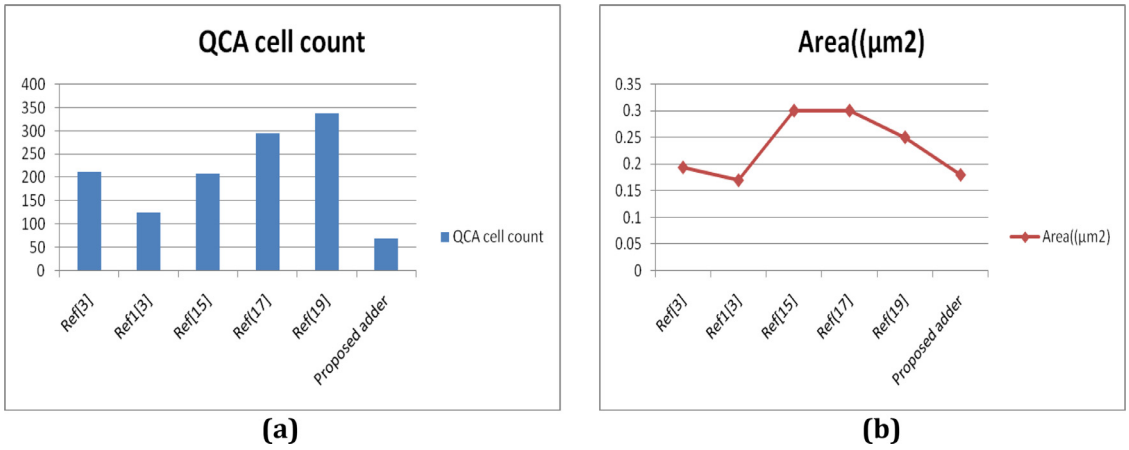


Fig. 7. Comparison of 4-bit RCA (a) QCA cell count (b) Area.

Table 1
One-bit full adder: a comparison.

Reference	QCA Cell Count	Area(µm^2)	Delay (Clock Phase)	Application	Cost(Area*Latency)
[1]	28	0.01	2	Multilayer	0.0050
[3]	40	0.03	05	Coplanar	0.015
[4]	47	0.02	15	Multilayer	0.3
[5]	114	0.23	1.25	Coplanar	0.287
[6]	59	0.043	1	Coplanar	0.043
[7]	37	0.0245	1	Coplanar	0.0245
[8]	115	0.1020	1.25	Coplanar	0.1275
[9]	33	0.02	0.5	Coplanar	0.01
[12]	39	0.027	4	Coplanar	0.108
[13]	25	0.01	2	Coplanar	0.02
[14]	30	0.028	0.75	Coplanar	0.021
[15]	30	0.04	0.5	Coplanar	0.02
[17]	63	0.05	0.75	Coplanar	0.028
[20]	44	0.06	1.25	Coplanar	0.075
[22]	44	0.03	0.5	Coplanar	0.015
Proposed	13	0.009	2	Coplanar	0.018

Table 2
4-bit RCA: comparison.

Reference	QCA Cell Count	Area(µm^2)	Delay (Clock Phase)	Application	Cost(Area*Latency)
[3]	212	0.194	05	Coplanar	0.97
[14]	125	0.17	5	Multilayer	0.85
[15]	209	0.3	1.25	Coplanar	0.375
[17]	295	0.3	1.5	Coplanar	0.45
[19]	339	0.25	1.75	Coplanar	0.437
Proposed	70	0.18	5	Coplanar	0.9

In 2-bit RCA, only two Majority Voter gates and two inverter gates are needed to design the architecture. The schematic diagram and layout of a 2-bit and 4-bit RCA (Ripple Carry Adder) are given in Fig. 5(c), (d), (e) and (f) respectively. Similarly by providing three inputs A_n, B_n and C_n to the n-bit Full adder, an n-bit RCA can be designed. The equation for the carry (C_{n+1}) and sum (S_n) output of n-bit Full adder is carried out by (8), (9) and (10)

$$C_{n+1} = MV(A_n, B_n, C_n) \tag{8}$$

$$C_{n+1} = (A_nB_n) + (B_nC_n) + (C_nA_n) \tag{9}$$

$$S_n = A_n \oplus B_n \oplus C_n \tag{10}$$

The proposed 4-bit RCA has four Majority voter gate (MV) and four QCA XOR Gates to implements its function Here the circuit needs 60 QCA cells to design a 4-bit RCA and the eventual outputs are produced after certain latency.

6. Performance evaluation

QCA Designer version 2.0.3 tool is taken into account as effective in coming up with the QCA layout of adder design. To check the proficiency of proposed adders with existing adders, parameters like delay, area and Quantum cost has been considered and compared as given in Table 1. It addresses the assessment among the designs of proposed 1- bit Full adders and prior designs. From the comparison, it seems that our proposed adder has attained less number of QCA cells. Also it is esteemed that this adder yields higher capability in terms of area and delay as estimated by comparison chart given in Fig. 6(a), (b) and (c).

Table 2 shows the comparison of 4-bit RCA with the earlier designs. The proposed RCA design shows the exceptional performance than the multilayer design in various parameters such as latency, area and cell count. Also it is esteemed that this adder yields higher capability in terms of area and delay as estimated by comparison chart given in Fig. 7(a) and (b).

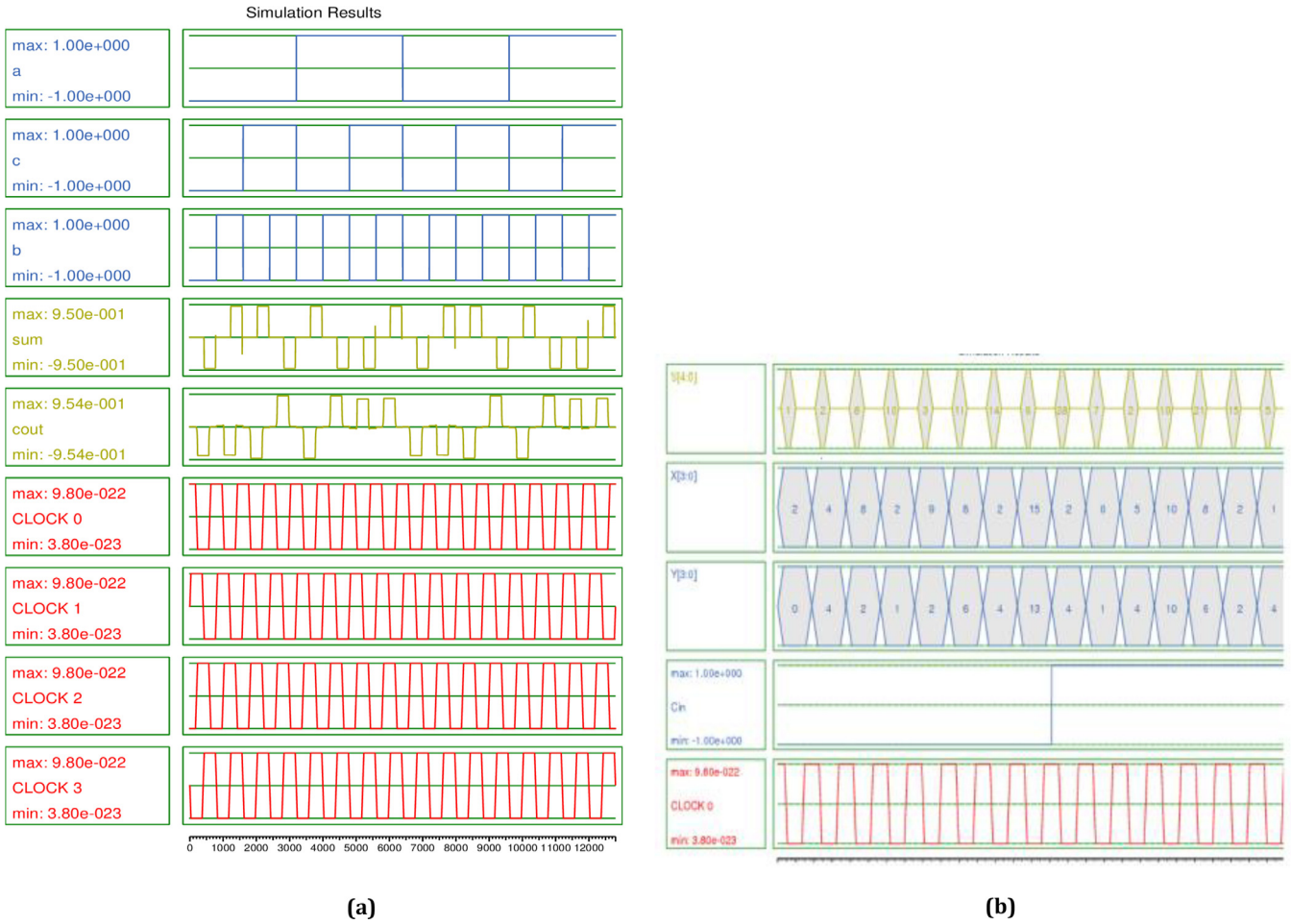


Fig. 8. (a) Simulation result of one-bit full adder (b) Simulation result of 4-bit ripple carry adder.

7. Simulation results

Simulation is performed for the proposed Adder using QCA Designer tool version 2.0.3 [21]. Fig. 8(a) gives the simulation output for the proposed adder. From the simulation results, we infer that for the input condition $A_0 = 0$, $B_0 = 1$ and $C_{in} = 1$, Outputs are Sum = 0 and $C_{out} = 1$ which yields the precision of the proposed design. The area of one-bit Full adder is about 0.09 μm^2 and therefore the latency is concerning of 2 clock cycles. Fig. 8(b) explores the simulation results of the proposed 4-bit RCA. Area of 4-bit RCA is about 0.18 $\mu m^2$and the delay is concerning 5 clock cycles.

8. Conclusion

The novel QCA architecture for 1-bit Full adder is established over here. Then High-speed adders like 4- bit RCA has been designed employing this novel full adder layout. In comparison with the recently published adder architecture, it is proved that our research work achieves less number of cell counts and less area with accurate simulation results. The simulation results show that our proposed work has achieved over 55% enhancement in the number of cells when analyzed with the existing design. In future, high speed adders which play an important role in multiplier designs could be designed and its computational performance could be improved further.

Declaration of Competing Interest

There is no conflict of Interest.

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