Implementation of 4-Bit RCA using Quantum Dot Cellular Automata Tool and Mentor Graphics Tool

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1. Abstract:

QCA technology is a new platform, which is a transistor less and wire-less technology, hence it is one of the best alternatives to CMOS technology for developing low power and high- speed digital circuits at nano-scale level. The limitations of CMOS technology such as large number of transistors and wire connections in a small area was overcome by QCA technology. Therefore, we have chosen the QCA technology. Adder is a basic architecture in constructing all digital circuits. First, a full adder is designed in both QCA as well as Mentor Graphics which has improved performance in propagation delay and cell count. Then with the help of 4 full adders a 4-Bit Ripple Carry Adder is implemented in QCA and compared the results with the existing RCA in QCA. From the comparison, it is found that the proposed ripple carry adder has better performance than the existing adder circuits.

Keywords:

QCA Designer Tool, Mentor Graphics Tool, Full adder, Ripple Carry Adder.

2. Introduction:

2.1 Quantum dot Cellular Automata-

(QCA) is a new platform which is wireless and transistor less technology, so it is also called as one of the alternatives to CMOS technology. QCA is used for implementing complex VLSI architecture and developing low-power, high speed digital circuits at nano-scale level compared to CMOS. The limitations of CMOS technology such as high integration density within small area due to large number of transistors and wire connections between them was overcome by QCA technology. In this technology, the binary information could be transmitted through Coulombic repulsion between the neighbouring QCA cells. Here, the binary value 0 or 1 is encoded through the reconfigurations of electrons in the quantum dots of QCA cells.

QCA based circuits are constructed using QCA cells. The basic device consists of four quantum dots arranged in a square with two excess electrons that tend to repel each other, resulting in two stable configurations. The square shape QCA cells comprises of four quantum dots with two dots occupied by electrons. These electrons reside over in the diagonal corner of the cell due to coulombic repulsion of force between them. Tunnelling of electrons between the quantum dots results

in two polarized states. These states namely PL = −1 and PL = + 1 represents logic value ‘0’ and ‘1’. Wires in QCA, are constructed either using normal cell or rotated cell. Due to its less complexity, normal cell as shown in are preferred over compared to rotated cell. The polarization state of cells gets changed when input is applied at one end of the wire. Based on the polarization either logic ‘0’ or logic ‘1’ will be a transmitted horizontally or vertically. QCA is a classical digital device that represents data as charge configuration rather than charge flow. Data is passed in QCA by arranging electrons along diagonals, with cells tending to assume the same configuration as their neighbours.

2.1.1 QCA WIRE:

The QCA wire is the one of the most important part of the design. The wire is used for communication purpose, Same in QCA the wire is used for passing the input or output. The wire in QCA will used for the passing of data. The data passing will play a major role because the input must be passed from one cell to another so that the circuit will work.

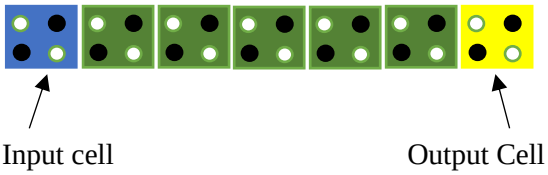


Fig 2.1: QCA Wire

The wire will pass the data from one cell to another cell. The cell will work by arranging the cells by each other in a line. The input is shown as an electron form the electron will decide the data whether it is 0 or 1 when the electron is clockwise then it is logic 0 and if the electron is anticlockwise then it is logic 1.

Fig 2.2: Logic 0 and Logic 1

2.1.2 Majority Voter Gate:

The majority voter (MV) gate is a basic logic element in QCA. It's a universal block in QCA technology that can form AND and OR gates. Designing the QCA circuit requires an Inverter, QCA wire and a three-input Majority Voter gate. A Majority Voter gate has five cells. Among five, three cells work as input cells and one cell works as output cell as given in. The middle cell is called as device cell and its logic operation depend on logic of input cells.

- QCA mainly works on Majority gate.
- A majority gate consists of 5cells
- A cell consists of 4 Quantum dots

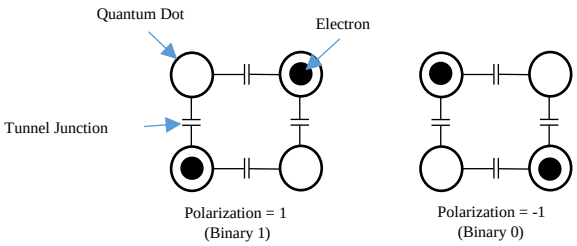


Fig 2.3: QCA cellular polarity

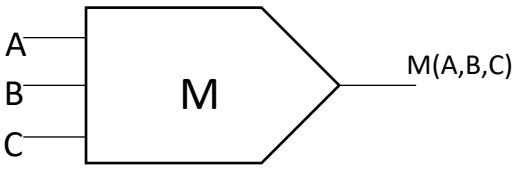


Fig 2.4: Symbol of Majority Gate

- A majority gate consists of 5 cells
- Where Orange color represents Fixed polarization
- Blue color represents Input
- Yellow color represents Output

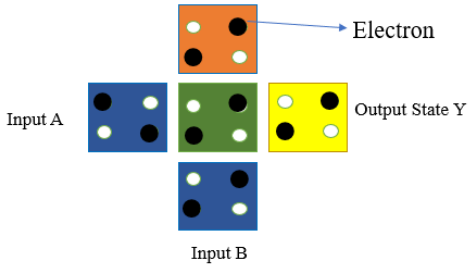


Fig 2.5: Majority Voter Gate

2.1.3 Clocking in QCA:

Clocking in QCA is used to control the polarization state of cells and passing the data. Two ways of Clocking is performed: zone clocking and continuous clocking. There are four types of clock zones in QCA named as clock zone 0, clock zone 1, clock zone 2, and clock zone 3 whose phase differs by 90 °. The cells with identical colour are assigned the same clocking zone. QCA will protect the design from delay so we use a clock. The clock will pass data from the small clock to the high clock condition.

- Clock 0 - Green
- Clock 1 - Violet
- Clock 2 - Blue (Lite)
- Clock 3 – White

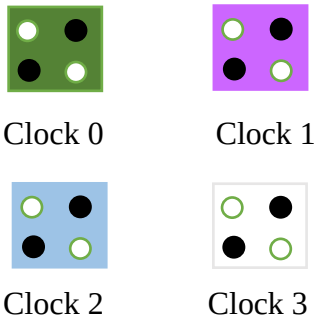


Fig 2.6: Clocking in QCA

As shown in the figure there are four phases in QCA circuits namely switch, hold, and release and relax phase respectively.

Four clocks are,

- Clock 0 is for “Switch”
- Clock 1 is for “Hold”
- Clock 2 is for “Release”
- Clock 3 is for “Relax”

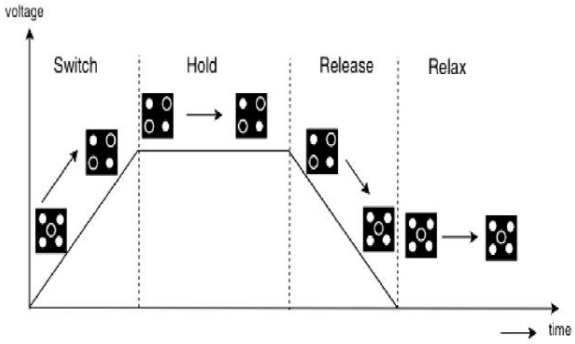


Fig 2.7: Clock Zones of QCA Cells

2.2 Mentor Graphics-

Mentor Graphics is one of the vendors of VLSI design tools and a supplier of Electronic Design Automation (EDA) tools, providing software and hardware design solutions that enable companies to develop better electronic products faster and more cost-effectively.

- This includes schematic entry tools for traditional designs and HDL (Hardware Description Language) entry tools for digital designs using languages like Verilog, VHDL, and System Verilog.
- Mentor Graphics offers synthesis tools that convert RTL (Register Transfer Level) descriptions of digital circuits into gate-level representations. This step optimizes the design for area, power, and timing constraints while preserving its functionality.

3. Literature Survey:

1. Angizi, Alkaldy, Bagherzadeh, and Navi introduced a novel and robust single-layer wire crossing approach for exclusive XOR and sum of products logic design utilizing quantum-dot cellular automata (QCA) with 495 cell count and 0.68 area.

This research addresses the challenge of implementing efficient wire crossing techniques in QCA-based logic circuits and contributes to the development of reliable and scalable QCA architectures for digital logic design. Also, this study highlights the ongoing efforts to optimize QCA-based systems for low-power and high-performance applications, laying the foundation for future advancements in nanotechnology.

2. Hashemi and Navi presented a novel and robust quantum-dot cellular automata (QCA) full-adder design with 442 cell count and 1 area.

This research contributes to advancing the field of QCA-based arithmetic circuitry by introducing innovative approaches to full-adder implementation. By addressing the challenges of robustness and reliability in QCA circuits, their work paves the way for more practical and their study underscores the importance of developing reliable building blocks for QCA-based systems, highlighting the ongoing efforts to overcome technological limitations in nanoscale computing.

3. Hashemi, Tehrani, and Navi proposed an efficient full-adder design using quantum-dot cellular automata (QCA) with 308 cells and 0.29 area. This research contributes to the optimization of QCA-based arithmetic circuits, aiming to enhance their efficiency and reliability. By introducing novel techniques for full-adder implementation they address the growing demand for high-performance computing systems in the field of quantum computing. Their work underscores the significance of efficient circuit design methodologies in overcoming the inherent challenges of QCA technology.

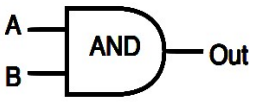
4. La brado and Thapliyal investigated the design of adder and subtractor circuits within the framework of majority logic-based field-coupled QC Anano computing with 295 cell count and 0.3 area. Their work, contributes to advancing the field of quantum-dot cellular automata (QCA) by exploring novel computing paradigms. Their study underscores the ongoing exploration of alternative computing architectures beyond traditional CMOS technologies, highlighting the potential of QCA nano computing for future computing applications.

5. Abedi, Jaberipur, and Sangsefidi proposed a coplanar full adder design in quantum-dot cellular automata (QCA) using clockzone-based crossover with 262 cell count and 0.208 area. This research contributes to advancing the field of QCA-based arithmetic circuitry by introducing innovative techniques for full adder implementation. By leveraging clock zone-based crossover, Abedi et al. aim to enhance the performance and scalability of QCA adders, addressing the growing demand for efficient computing architectures in nanotechnology-driven systems.

4. Designing of Logic Gates:

4.1: AND Gate-

The AND gate is a basic digital logic gate that implements from mathematical logic - AND gate behaves according to the truth table. A HIGH output (1) results only if all the inputs to the AND gate are HIGH (1). If not all inputs to the AND gate are HIGH, LOW output results.



A	B	Out
0	0	0
0	1	0
1	0	0
1	1	1

Fig 4.1: Symbol and Truth Table of AND Gate

If the polarity of one of the inputs is set given as a constant, for example, if P = -1, an AND gate is made, and if the polarity of one of the inputs is given as P = + 1, an OR gate will be made.

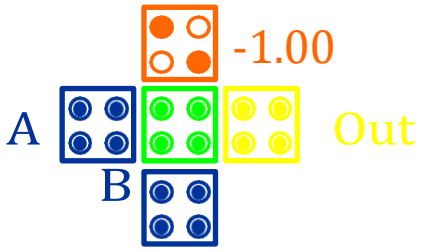
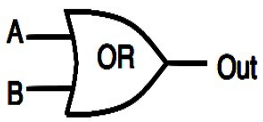


Fig 4.2: AND gate in QCA

4.2: OR Gate-

The OR gate is a digital logic gate that implements logical disjunction. The OR gate outputs "true" if any of its inputs are "true" otherwise, it outputs "false".



A	B	Out
0	0	0
0	1	1
1	0	1
1	1	1

Fig 4.3: Symbol and Truth Table of AND Gate

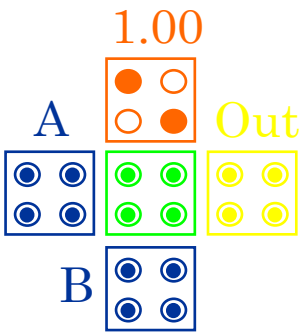
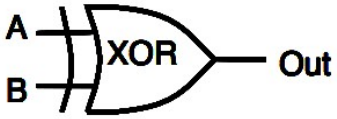


Fig 4.4: OR gate in QCA

4.3: XOR Gate-

XOR gate is a digital logic gate that gives a true output when the number of true inputs is odd. An XOR gate implements an exclusive or () from mathematical logic; that is, a true output results if one, and only one, of the inputs to the gate is true.



A	B	C	Out
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Fig 4.5: Symbol and Truth Table of XOR Gate

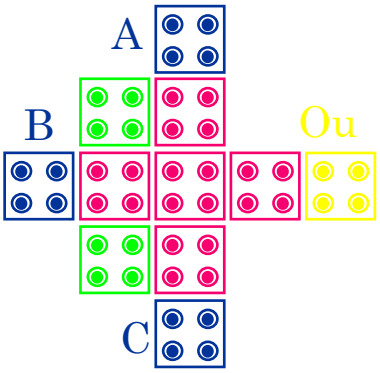


Fig 4.6: XOR gate in QCA

5. Existing Design:

The Existing Technology is of designing Full adder using Quantum Dot Cellular Automata (QCA) tool which consists of three-input XOR gate and a three-input majority gates. Using this Full adder, higher adders like 4-bit RCA (Ripple Carry Adder) has been designed with the area of 0.208, cell count-262, Delay that has 1.75. An increase in the QCA cell count ends up in an increase of the area and delay of the design.

5.1: Full Adder Implementation Using QCA-

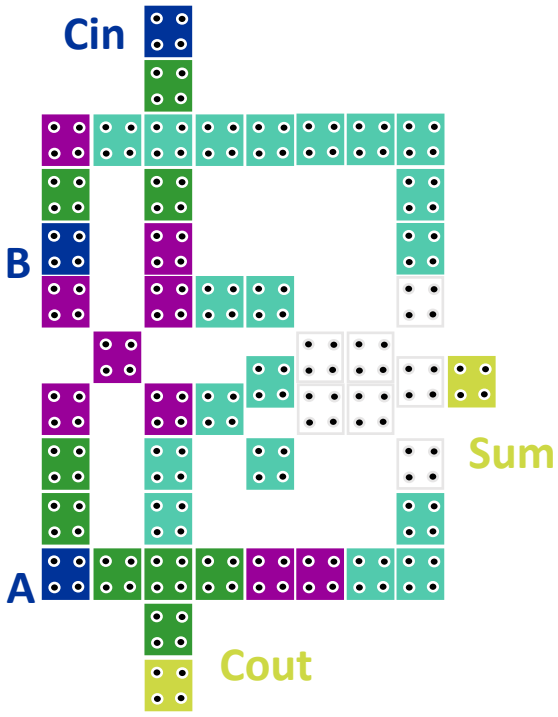


Fig 5.2: Full Adder Layout In QCA

5.2: 4-Bit Ripple Carry Adder Implementation in QCA

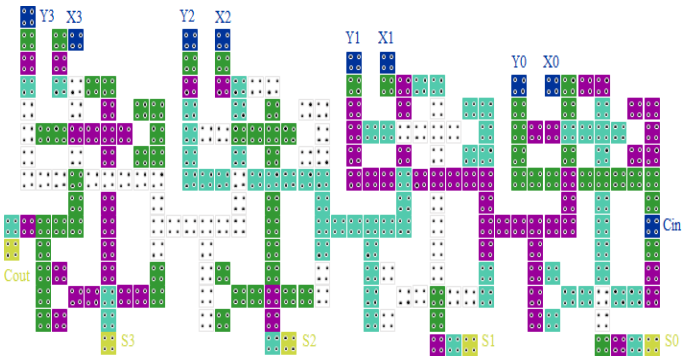


Fig 5.3: Layout Of 4-Bit Ripple Carry Adder in QCA

Disadvantages:

- Decreasing the amount of consumed space in RCA designed by QCA technology
- Reducing the complexity and latency in RCA designed by QCA technology
- Decreasing the number cells in RCA designed by QCA technology.

6. Proposed Design:

6.1: Designing of 4-Bit Ripple Carry Using QCA Tool-

Full adders and RCA circuits are fundamental units in logical circuits and digital arithmetic operations. RCA's layout is designed and implemented simply, but it is quite slow since each full adder has to wait for the calculated carry bit from the previous one. To overcome this problem, we can reduce the delay in RCAs by decreasing the delay of full adders.

So, we have proposed the 4-bit Ripple Carry Adder (RCA) with four full adders using QCA tool with less cell count and delay compared to Existing Technique.

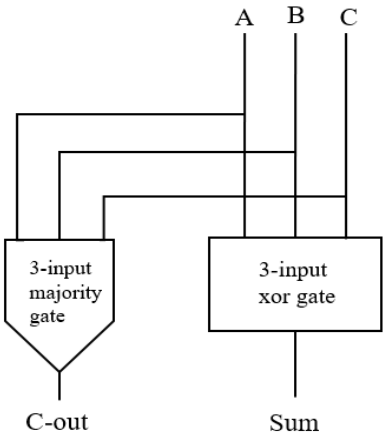


Fig 5.4: Block diagram of Full Adder in QCA

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig 5.5: Truth Table of Full Adder

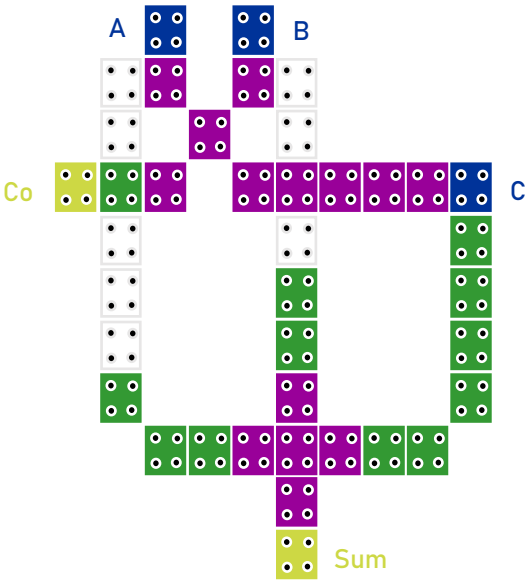


Fig 5.6: Full Adder Circuit in QCA

Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is carried which is C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM. It is a combinational logic circuit.

Full Adder is the basic element in performing all the arithmetic and logical operations in ALU of a processor. To obtain an efficient architecture in terms of latency, area and delay here the implementation of Full adder has been designed. In many fields the Adder plays an important role and are commonly found in many building blocks of microprocessors digital signal processing chips, Multipliers, ALU and Shift registers.

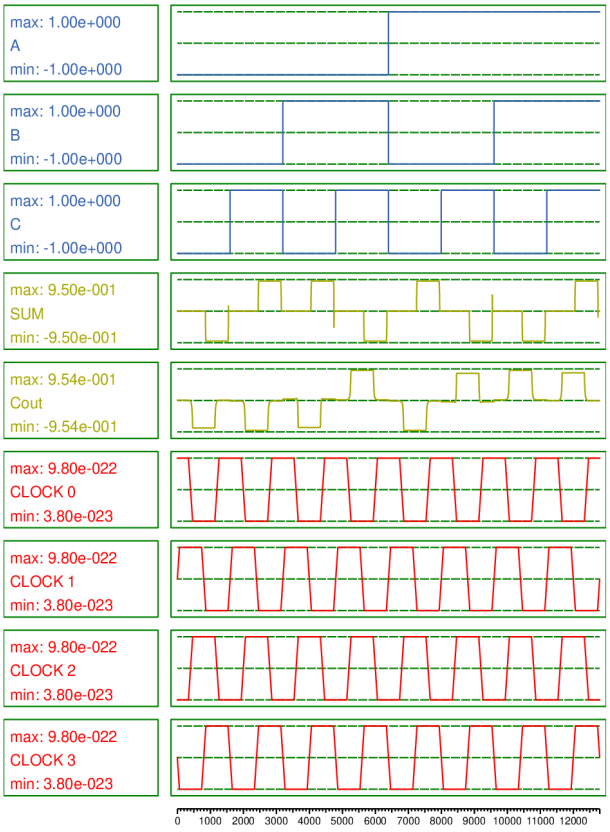


Fig 5.7: Simulation Result of Full Adder

A structure of multiple full adders is cascaded in a manner to gives the results of the addition of an n bit binary sequence. This adder includes cascaded full adders in its structure so the carry will be generated at every full adder stage in a ripple-carry adder circuit. These carry output at each full adder stage is forwarded to its next full adder and there applied as a carry input to it.

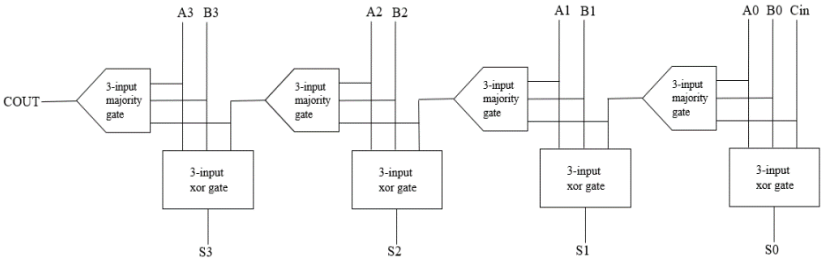


Fig 5.8: Block Diagram Of 4-Bit RCA in QCA

	A				B				Sum				Carry
Cin	A3	A2	A1	A0	B3	B2	B1	B0	S3	S2	S1	S0	Cout
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	1	0	0	1	0	0
0	0	0	1	0	0	0	1	0	0	1	0	0	0
0	0	0	1	1	0	0	1	1	0	1	1	0	0
0	0	1	0	0	0	1	0	0	1	0	0	0	0
0	0	1	0	1	0	1	0	1	1	0	1	0	0
0	0	1	1	0	0	1	1	0	1	1	0	0	0
0	0	1	1	1	0	1	1	1	1	1	1	0	0
0	1	0	0	0	1	0	0	0	0	0	0	0	1
0	1	0	0	1	1	0	0	1	0	0	1	0	1
0	1	0	1	0	1	0	1	0	0	1	0	0	1
0	1	0	1	1	1	0	1	1	0	1	1	0	1
0	1	1	0	0	1	1	0	0	1	0	0	0	1
0	1	1	0	1	1	1	0	1	1	0	1	0	1
0	1	1	1	0	1	1	1	0	1	1	0	0	1
0	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Fig 5.9: Truth Table Of 4-Bit RCA

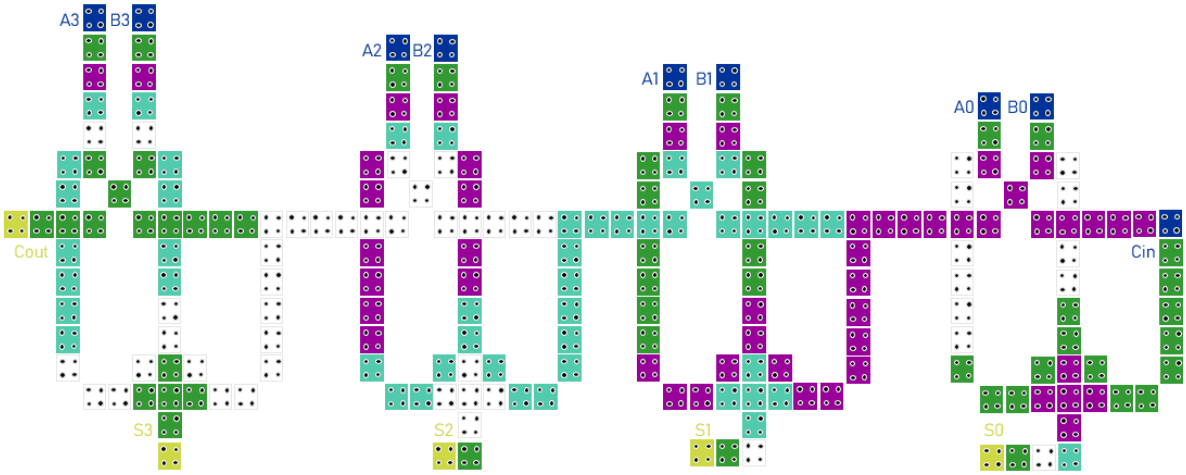


Fig 5.10: 4-Bit RCA Circuit in QCA

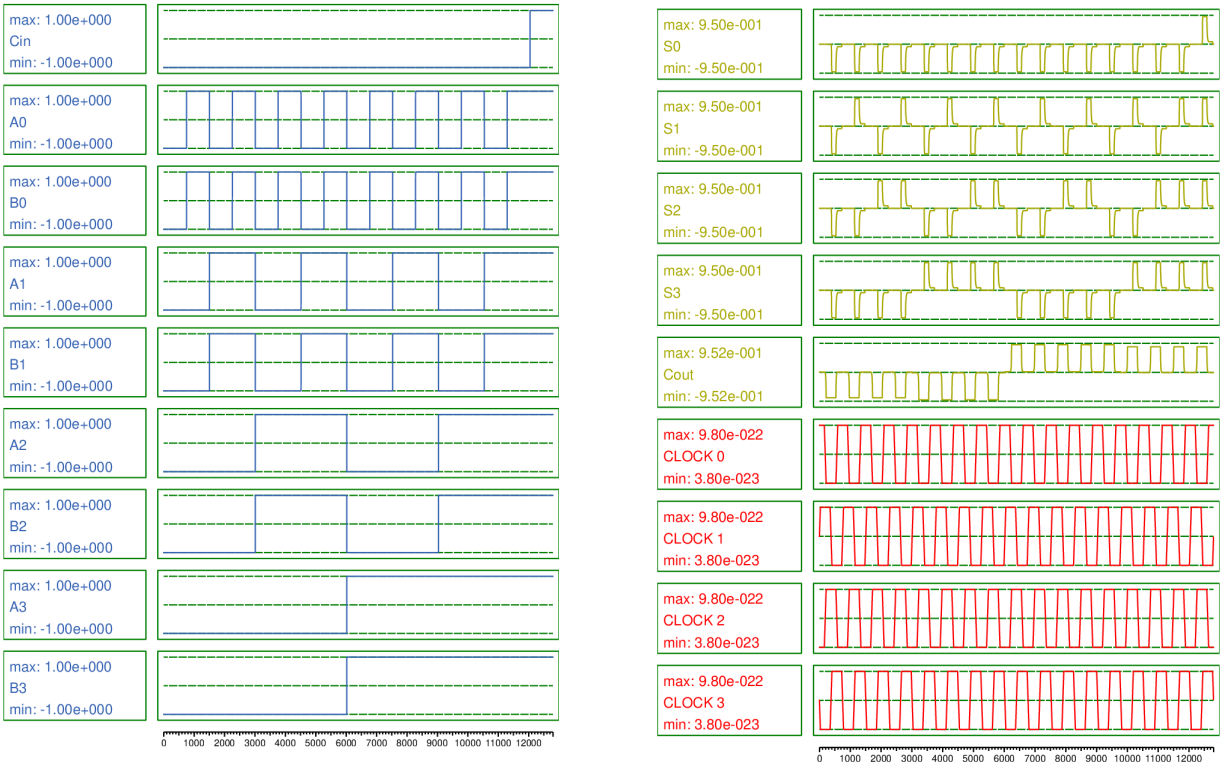


Fig 5.11: Simulation Result of 4-Bit RCA in QCA

6.1: Designing of 4-Bit Ripple Carry Using Mentor Graphics Tool-

As we know that QCA is called as one of the alternative of CMOS Technology for developing low-power, high speed digital circuits. To prove that QCA is one of the best tool compared to CMOS technology we have also implemented the 4bit Ripple carry Adder in Mentor graphics tool as well.

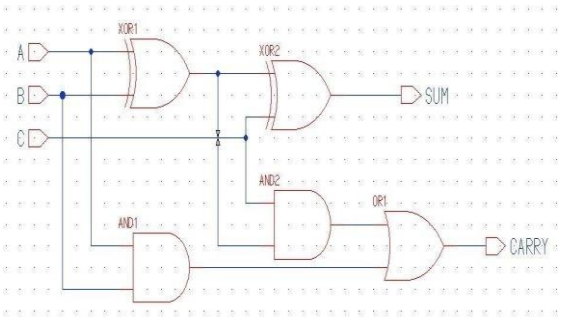


Fig 6.1: Full Adder Schematic

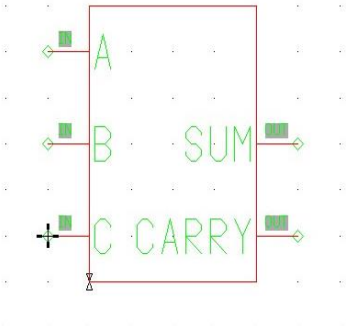


Fig 6.2: Full Adder Symbol

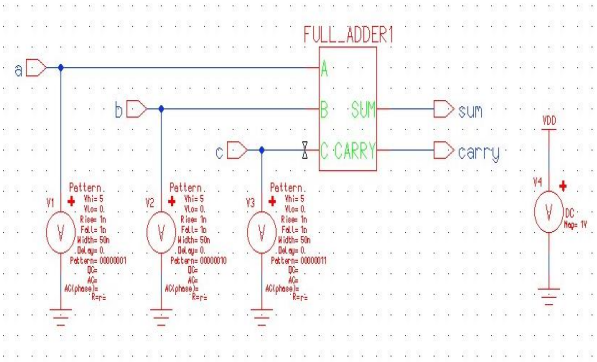


Fig 6.3: Full Adder Test Bench

After designing Full Adder in Mentor Graphics Tool, we got its Test Bench which is now required to design 4-bit RCA.

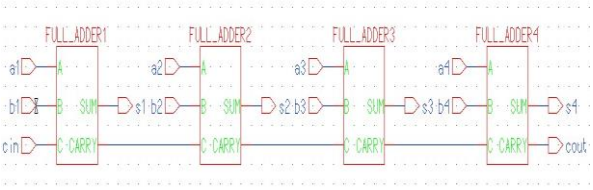


Fig 6.4: RCA Schematic

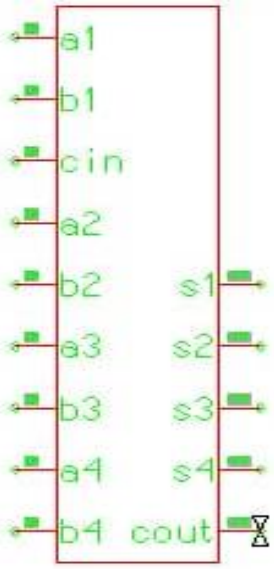


Fig 6.5: RCA Symbol

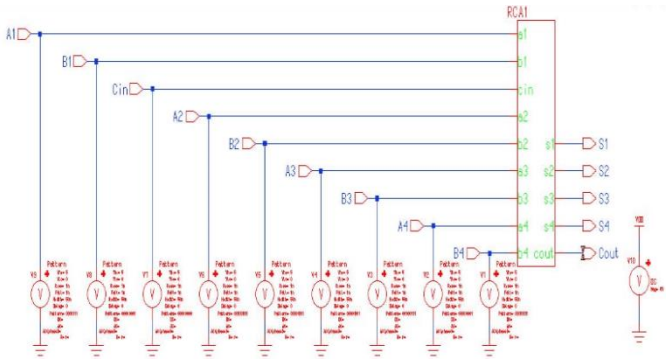


Fig 6.6: RCA Test Bench

Now that the 4-Bit RCA test bench has been created let's see the simulated results that are been generated.

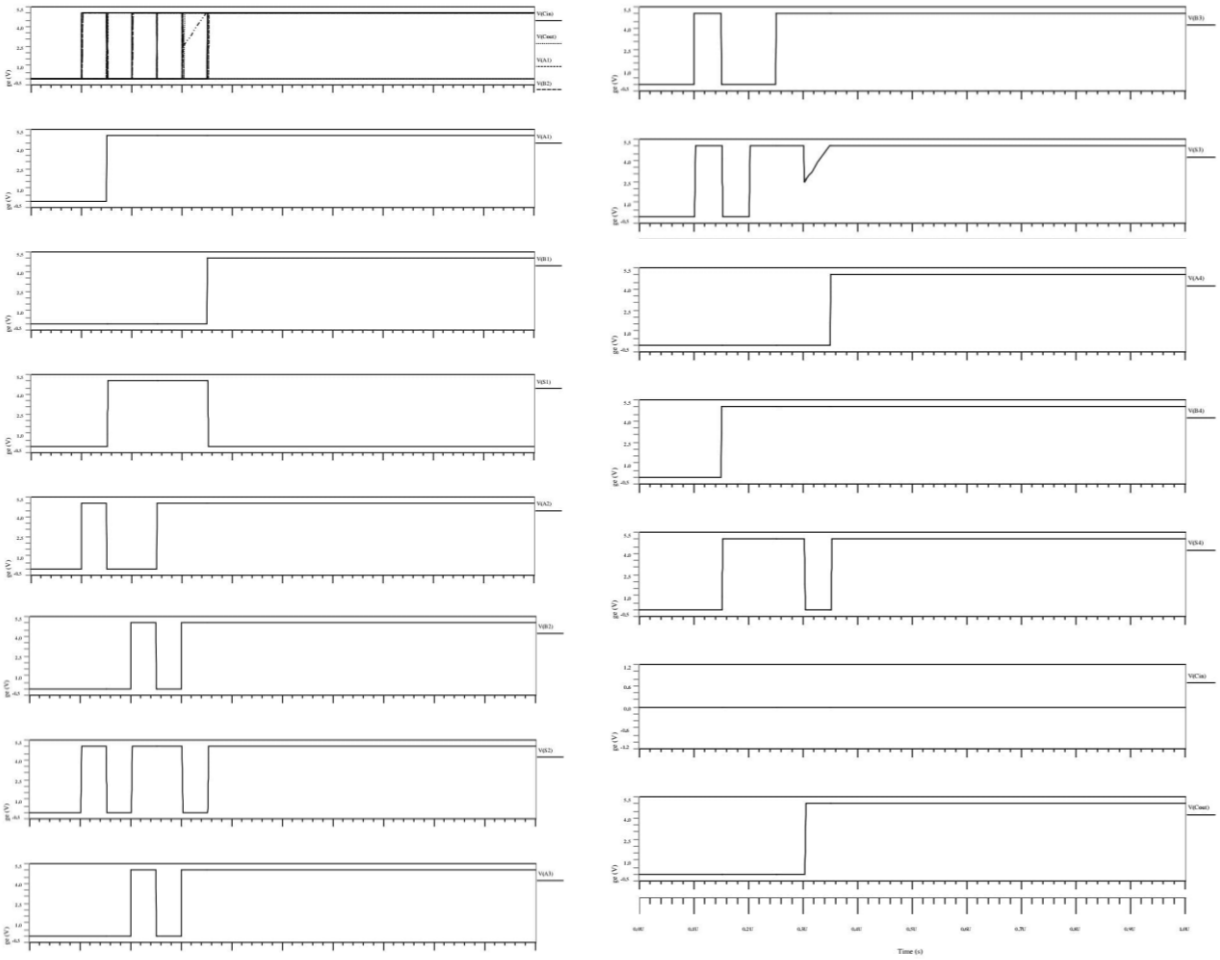


Fig 6.7: Output Generation of Four Bit RCA in Mentor Graphics

7. Conclusion:

	EXISTING CIRCUIT	PROPOSED CIRCUIT
AREA	0.208	0.3
CELL COUNT	262	208
DELAY	1.75	1.25

Table 7.1: Comparison between Existing and proposed Circuit

Parameters	Full Adder in Mentor Graphics	Full Adder in QCA
Area	9 μm^2	0.06 μm^2
Transistor Count/ QCA Cell Count	28	39

Table 7.2: Comparison between parameter for Full Adder in Mentor Graphics and QCA

Parameters	RCA in Mentor Graphics	RCA in QCA
Area	34 μm^2	0.34 μm^2
Transistor Count/ QCA Cell Count	112	208

Table 7.3: Comparison between parameters for RCA in Mentor graphics & QCA

The below bar charts shows the comparison between the parameters of existing and proposed circuits, which includes parameters such as area, cell count and delay.

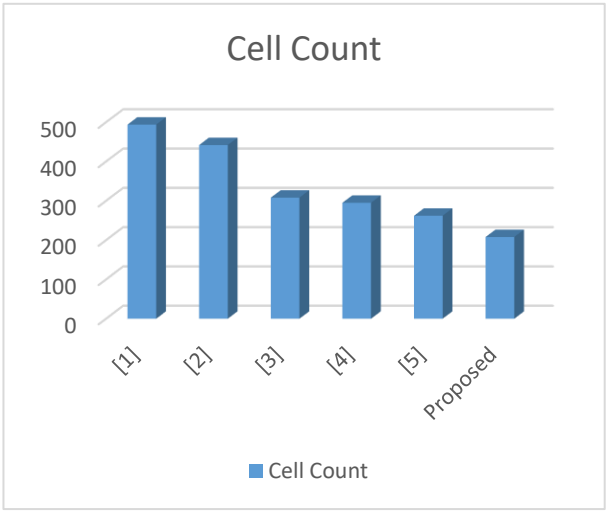


Fig 7.4: Cell count comparison between existing and proposed methods

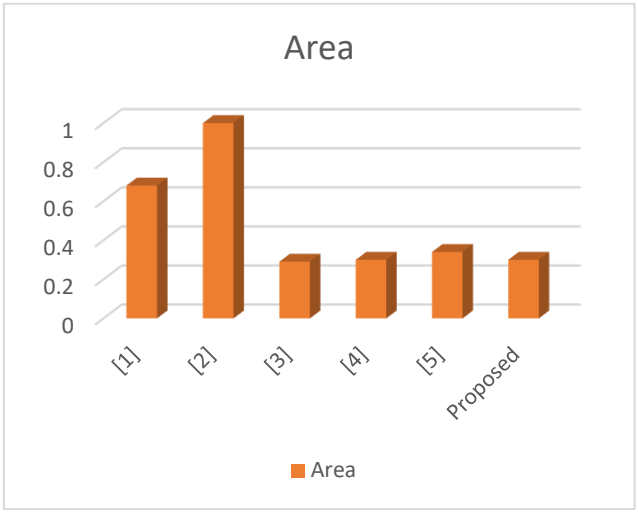


Fig 7.5: Area Comparison between existing and proposed methods

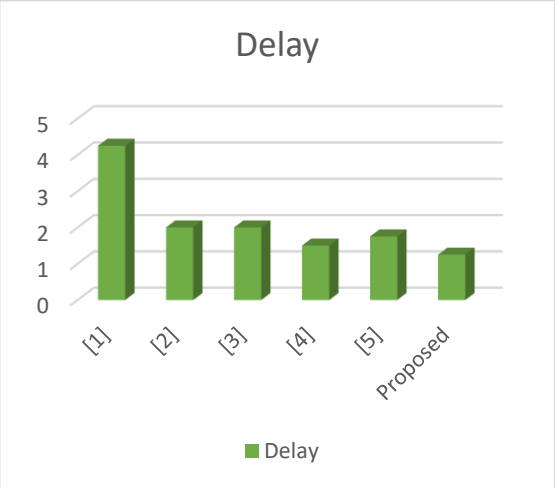


Fig 7.6: Delay comparison between existing and proposed methods

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