A Project Report on

Very Large Scale Integration (VLSI)

An Internship Report submitted in partial fulfillment of the

Requirements for the award of the degree of

BACHELOR OF TECHNOLOGY

in

ELECTRONICS AND COMMUNICATION ENGINEERING

Submitted by

Harsha Devara

Reg No: 20P31A04J4

Under the esteemed supervision of

Mr. T. Anjaiah, M.Tech, (Ph.D)

Associate Professor

ADITYA COLLEGE OF ENGINEERING & TECHNOLOGY

An AUTONOMOUS Institution

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Aditya Nagar, ADB Road, Surampalem-533 437

(2023-2024)

CERTIFICATE

Department Of Electronics and Communication Engineering

This is to certify that the Internship report entitled "**VLSI**" is being submitted by Harsha Devara **(20P31A04J4).** In partial fulfillment of the requirements for award of the B.Tech degree in Electronics and Communication Engineering of the academic year 2023-2024.

Internship Guide

Mr. T. Anjaiah, M. Tech, (Ph.D)

Associate Professor

Dept. of ECE

Head of the Department

Dr.R.V.V,Krishna, M.Tech, Ph.D

Professor & HOD

Dept. of ECE

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Ph: +91 99591 76665
Email: office@acet.ac.in
Website: www.acet.ac.in

INSTITUTE VISION AND MISSION

VISION:

To induce higher planes of learning by imparting technical education with

- International standards
- Applied research
- Creative Ability
- Value based instruction and to emerge as a premiere institute

MISSION:

Achieving academic excellence by providing globally acceptable technical education by forecastingtechnology through

- Innovative Research and development
- Industry Institute Interaction
- Empowered Manpower

PRINCIPAL

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DEPARTMENT VISION AND MISSION

Vision: To emerge as a center of excellence in education and research

Mission:

- To establish skill and learning centric infrastructure in thrust areas
- To develop Robotics and IOT based infrastructure Laboratories
- To organize events through industry institute collaborations and promote innovation
- To disseminate knowledge through quality teaching learning process.

Head of the Department

Head of the Department
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PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

Program Name: Bachelor of Technology (B.Tech) in Electronics and Communication Engineering.

PEO1: Graduates shall evolve into skilled professionals capable of handling interdisciplinary work atmosphere and excel in problem solving.

PEO2: Graduates shall inculcate the urge to progress in the chosen field of Electronics & Communication through higher education and research.

PEO3: Graduates shall ingrain professional values through Ethics based teaching learning process.

PEO4: Graduates shall exhibit leader ship skills and advance towards Entrepreneurship, Innovation and lifelong learning.

Head of the Department

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PROGRAM SPECIFIC OUTCOMES (PSOs)

Program Name: Bachelor of Technology (B.Tech) in Electronics & Communication Engineering

PSO1: Industry ready in the arena of electronics & communication, VLSI, Robotics, Embedded Systems, IOT and allied fields.

PSO2: Acquire the required ability and knowledge to design, test, verify and develop innovative electronics projects through theoretical and laboratory practice.

Head of the Department

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PROGRAM OUTCOMES (POs)

PO1. **Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2. **Problem Analysis:** Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3. **Design/Development of Solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4. **Conduct Investigations of Complex Problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5. **Modern Tool Usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with anunderstanding of the limitations.

PO6. **The Engineer and Society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7. **Environment and Sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and normsof the engineering practice.

PO9. **Individual and Team Work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effectivereports and design documentation, make effective presentations

PO11. **Project Management and Finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12. **Life-Long Learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

ACKNOWLEDGEMENT

It gives us immense pleasure to express a deep sense of gratitude to my guide **Mr. Anjaiah Talamala, M. Tech, (Ph.D),** Associate Professor, Department of ECE for whole hearted and invaluable guidance throughout the project. Without his sustained and sincere effort, this project work would not have taken this shape. He encouraged and helped us to overcome various difficulties that we have faced at various stages of our project work.

We would like to sincerely thank our Head of the department **Dr. R V V Krishna, M. Tech, Ph.D,** for providing all the necessary facilities that led to the successful completion of our project work.

We would like to take this opportunity to thank our beloved Principal **Dr. Dola Sanjay S**, **M. Tech, Ph.D,** for providing all the necessary facilities and a great support to us in completing the project work.

We would like to thank all the faculty members and the non-teaching staff of the Department of Electronics and Communication Engineering for the indirect support for helping us in completion of this project work.

Finally, we would like to thank all our friends and family members for their continuous help and encouragement.

Harsha Devara

(20P31A04J4)

INSTRUCTION TO STUDENTS

Please read the detailed Guidelines on Internship hosted on the website of AP State Council ofHigher Education **https://apsche.ap.gov.in**

1. It is mandatory for all the students to complete (240 hours) of long- term internship either physically or virtually.
2. Every student should identify the organization for internship in consultation with the College Principal/the authorized person nominated by the principal.
3. Report to the intern organization as per the schedule given by the College. You must make your own arrangements for transportation to reach the organization.
4. You should maintain punctuality in attending the internship. Daily attendance is compulsory.
5. You are expected to learn about the organization, policies, procedures, and processes by interacting with the people working in the organization and by consulting the supervisor attached to the interns.
6. While you are attending the internship, follow the rules and regulations of the intern organization.
7. While in the intern organization, always wear your College Identity Card.
8. If your college has a prescribed dress as uniform, wear the uniform daily, as you attend to your assigned duties.
9. You will be assigned a Faculty Guide from your College. He/She will be creating a WhatsApp group with your fellow interns. Post your daily activity done and/or any difficulty you encounter during the internship.
10. Identify five or more learning objectives in consultation with your Faculty Guide. These learning objectives can address:
    a. Data and Information you are expected to collect about the organization and/or industry.
    b. Job Skills you are expected to acquire.
    c. Development of professional competencies that lead to future career success.
11. Practice professional communication skills with team members, co-interns, and your supervisor. This includes expressing thoughts and ideas effectively through oral, written, and non-verbal communication, and utilizing listening skills.

12. Be aware of the communication culture in your work environment. Follow up and communicate regularly with your supervisor to provide updates on your progress with work assignments.
13. Never be hesitant to ask questions to make sure you fully understand what you need to do your work and to contribute to the organization.
14. Be regular in filling up your Program Book. It shall be filled up in your own handwriting. Add additional sheets wherever necessary.
15. At the end of internship, you shall be evaluated by your Supervisor of the intern organization.
16. There shall also be evaluation at the end of the internship by the Faculty Guide and the Principal.
17. Do not meddle with the instruments/equipment you work with.
18. Ensure that you do not cause any disturbance to the regular activities of the intern organization.
19. Be cordial but not too intimate with the employees of the intern organization and your fellow interns.
20. You should understand that during the internship program, you are the ambassador of your college, and your behavior during the internship program is of utmost importance.
21. If you are involved in any discipline related issues, you will be withdrawn from the internship program immediately and disciplinary action shall be initiated.
22. Do not forget to keep up your family pride and prestige of your college.

STUDENT'S DECLARATION

I**, HARSHA DEVARA** a student of B.Tech Program, Regd.No: **20P31A04J4** of the Department of **ELECTRONICS AND COMMUNICATION ENGINEERING,** College do hereby declare that I have completed the mandatory internship from **08/01/2024** to **19/04/2024** in **SkillDzire Organization** under the Faculty Guideship of Mr. T. ANJAIAH, M.Tech, (Ph.D), Department of **ELECTRONICS AND COMMUNICATION ENGINEERING, ADITYA COLLEGE OF ENGINEERING AND TECHNOLOGY(A).**

(Signature and Date)

OFFICIAL CERTIFICATION

This is to certify that **Harsha Devara** Reg. No. **20P31A04J4** has completed his Internship in **SkillDzire Organization** on **VLSI INTERNSHIP** under my supervision as a part of partial fulfillment of the requirement for the Degree of **B. Tech** in the Department of **ECE, ADITYA COLLEGE OF ENGINEERING & TECHNOLOGY.**

This is accepted for evaluation

Endorsements

Faculty Guide

Head of the Department

Principal

CERTIFICATE FROM INTERN ORGANIZATION

SkillDzire

CERTIFICATE OF INTERNSHIP

This is to Certify that Mr./Ms

Devara Harsha

Enrolled in the Electronics and Communication Engineering - 20P31A04J4

From College Aditya College of Engineering & Technology

of university JNTUK, Kakinada

has Successfully Completed long-term Internship programme titled

VLSI

Under SkillDzire for 240 Hours.Organized By **SkillDzire** in collaboration with **Andhra Pradesh State Council of Higher Education**.

Certificate ID: SDAP-05470

Issued On 19-Apr-2024

Approved By AICTE

Authorized Signature

CERTIFICATE FROM INTERN ORGANIZATION

This is to certify that **HARSHA DEVARA R**eg. No **20P31A04J4** of **ADITYA COLLEGE OF ENGINEERING & TECHNOLOGY** underwent internship In **SKILLDRIZE Organization** from **08/01/2024** to **19/04/2024** The overall performance of the intern during his internship is found to be **Satisfactory.**

Authorized Signatory with Date and Seal

CONTENTS

CHAPTER 1: EXECUTIVE SUMMARY

The VLSI Internship is provided by SkillDzire Organization through AICTE and APSCHE portal.

1.1 Learning Objectives of SkillDzire Organization Internship

- Understanding VLSI Fundamentals
- Design Tools and Methodologies
- RTL Coding
- Physical Design and Implementation
- Real-World Project Experience

1.2 Learning Outcomes of SkillDzire Organization Internship

- Understanding VLSI Fundamentals
- RTL Coding and Verification
- Physical Design and Layout
- Project Work and Collaboration
- Presentation and Communication Sills

1.3 A Brief Description of the Intern Organization

SkillDzire Organization is a multifaceted entity that specializes in providing professional development, training, and consultancy services. With a focus on enhancing skills and capabilities across various industries, SkillDzire offers tailored solutions to meet the specific needs of businesses and individuals alike. Their offerings may include workshops, seminars, online courses, and personalized coaching sessions designed to improve competencies, foster innovation, and drive organizational growth. SkillDzire Organization aims to empower individuals and organizations to thrive in today's dynamic and competitive landscape through continuous learning and development initiatives.

1.4 SkillDzire Organization Internship Summary

The SkillDzire Organization 's Vlsi Internship Program is a comprehensive and hands-on learningexperience designed to equip I with the skills and knowledge needed to excel in the field of vlsi. This program is open to students, recent graduates, and early-career professionals who are passionate about learning VLSI and many other core and computer technologies. The SkillDzire Organization is committed to fostering a supportive and collaborative learning environment, empowering interns to embark on successful careers in vlsi.

CHAPTER 2: OVERVIEW OF THE ORGANIZATION

2.1 Introduction of the Organization

SkillDzire Organization is a dynamic entity dedicated to fostering professional growth and development across various industries. Committed to empowering individuals and organizations, SkillDzireoffers a comprehensive range of services tailored to enhance skills, capabilities, and performance. With a focus on continuous learning and innovation, SkillDzire provides workshops, seminars, training programs, and consultancy services designed to meet the evolving needs of today's workforce. Whether it's sharpening technical skills, honing leadership abilities, or cultivating a culture of innovation, SkillDzire equips clients with the tools and knowledge necessary to excel in their respective fields.

Vision, Mission, and Values of the Organization:

2.2 Vision of the Organization

SkillDzire is an organization with a clear and ambitious mission. Their commitment is evident in their dedication to fostering entrepreneurship, promoting technology commercialization, encouraging technology adoption, and actively engaging with their community. Furthermore, SKILLDZIRE seeks to improve its financial position to ensure long-term viability and growth, demonstrating a keen awareness of the need for sustainable development.

One of SKILLDZIRE's primary commitments is to entrepreneurship. This commitment likely involves supporting startups and small businesses by providing them with resources, mentorship, and education. They recognize that entrepreneurship is a vital engine for economic growth, job creation, and innovation. By nurturing and guiding aspiring entrepreneurs, SKILLDZIRE contributes to the development of a thriving entrepreneurial ecosystem.

2.3 Mission of the Organization

Our mission is straightforward yet profound: to champion diversity in ideas, technologies, and leadership to forge a brighter future. We are committed to nurturing a dynamic and inclusive ecosystem that celebrates innovation, welcomes novel ideas, and empowers visionary leaders.

The core of our mission lies in recognizing that the world's most promising opportunities emergefrom the convergence of diverse perspectives. By fostering a platform where a rich tapestry of ideas can flourish, we aim to fuel the engines of progress, ensuring that no potential is left untapped.

We firmly believe in the power of technology as a catalyst for change. Through technology, we can address critical challenges, improve lives, and reshape industries. Our mission drives us to support and amplify those technological solutions that hold the promise of a more sustainable, inclusive, and prosperous future.

Leadership is a linchpin of our mission. We strive to identify, mentor, and elevate leaders who embody the spirit of innovation and the values of diversity and inclusion. It is through these visionary leaders that we can steer the course toward a brighter and more equitable future.

2.4 Values of the Organization

SKILLDZIRE, the driving force for change, is steadfast in its commitment to setting the global standard for inclusive economic programs tailored to empower young entrepreneurs. At the heart of this dedication lies the unwavering belief that inclusivity and knowledge are the catalysts for profound transformation.

Our pledge to provide a global standard in these programs signifies a pledge to excellence. We aim to create a model that not only meets but surpasses international benchmarks, ensuring that young entrepreneurs worldwide have access to the highest quality resources and support.

Central to this mission is the principle of knowledge accessibility. We recognize that knowledge is the cornerstone of success. By granting our members access to a wealth of valuable content, we equip them with the tools needed to enhance their delivery models. This empowerment, in turn, translates into superior outcomes for young entrepreneurs under their guidance.

SKILLDZIRE is committed to providing the global standard in inclusive economic programmers for young entrepreneurs. This ensures members are able to access content to improve the quality of theirdelivery models, which in turn improves outcomes for young entrepreneurs.

CHAPTER 3: INTERNSHIP PART

3.1 INTRODUCTION:

SKILLDZIRE is a dynamic and forward-thinking organization dedicated to catalyzing positive change through entrepreneurship, technology, and community engagement. Established with a visionary mission, SKILLDZIRE is committed to providing inclusive economic programs for young entrepreneurs, setting a global standard in the realm of economic development.

At the core of SKILLDZIRE's mission is a resolute belief in the transformative power of youth- led entrepreneurship. SKILLDZIRE recognizes that young entrepreneurs possess the innovation, energy,and potential to shape the future. By fostering their growth and providing them with resources and mentorship, SKILLDZIRE seeks to be the catalyst for a new generation of successful and socially conscious business leaders.

SKILLDZIRE is more than an organization; it's a movement that champions diversity and inclusion. The organization is dedicated to supporting a diverse array of ideas and technologies, recognizing that innovation flourishes in an environment that embraces differences. By empowering leaders who embody these principles, SKILLDZIRE envisions a world where opportunities are not bound by traditional barriers but are accessible to all.

3.2 VLSI CATALYST

VLSI stands for Very Large-Scale Integration, which pertains to the process of creating integrated circuits (ICs) by combining thousands or millions of transistors onto a single chip.

3.2.1 Logic Design:

Logic design is a fundamental aspect of digital circuit design, focusing on the creation and optimization of logical circuits that process binary information (0s and 1s). At its core, logic design involves the systematic arrangement of logic gates to perform specific functions and tasks. Logic gates, such as AND, OR, NOT, NAND, and NOR gates, are the building blocks of digital circuits. They manipulate binary signals according to predefined logic rules. Through the strategic combination of these gates, complex digital systems can be constructed to execute various operations, ranging from basic arithmetic to complex data processing.

3.2.2 Latches and Flipflops:

In VLSI (Very Large-Scale Integration) design, latches and flip-flops are fundamental building blocks used to store and control digital data. In VLSI design, both latches and flip-flops play critical roles in storing and controlling digital data within sequential logic circuits. They are used in various applications such as register files, memory elements, state machines, and control units. Designers choose between latches and flip-flops based on factors such as timing requirements, power consumption, area constraints, and design complexity.

3.2.3 Mealy Machine:

Mealy Machines are widely used in digital system design for their ability to model complex behaviors and efficiently implement sequential logic circuits. They offer flexibility in specifying outputbehavior based on both current states and input signals, making them suitable for a wide range of applications. In VLSI design, Mealy Machines are often implemented using hardware description languages (HDLs) like Verilog or VHDL and synthesized into physical hardware components.

3.2.4 UART:

UART (Universal Asynchronous Receiver/Transmitter) is a fundamental building block used for serial communication between digital systems. UARTs are commonly integrated into microcontrollers, microprocessors, FPGAs (Field Programmable Gate Arrays), and other integrated circuits to enable communication with external devices such as sensors, displays, and other peripherals. In VLSI design, UART modules can be implemented using hardware description languages (HDLs) like Verilog or VHDL and synthesized into physical hardware components.

3.2.5 SDA & SCL (Serial Data Line & Serial Clock Line):

SDA (Serial Data Line) and SCL (Serial Clock Line) are essential signals used in the I2C (Inter-Integrated Circuit) communication protocol, a widely used serial communication protocol in embedded systems, microcontrollers, and integrated circuits. SDA and SCL lines are essential for communication between devices in I2C networks, enabling efficient and reliable data exchange in various applications, including sensor interfacing, EEPROM (Electrically Erasable Programmable Read-Only Memory) communication, and control interfaces. These lines play a critical role in the implementation of I2C- compatible designs.

CHAPTER 4: WEEKLY REPORTS

4.1 ACTIVITY LOG FOR THE FIRST WEEK

Day & Date	A Brief description of the daily activity	Learning Outcome	Person-In-Charge Signature
08-01-2024	On the first day of the internship, I gain a fundamental understanding of VLSI technology, including its definition, components, and key characteristics.	Introduction to Basics of VLSI Technology	
09-01-2024	I explored the historical development of VLSI technology, identifying key milestones and technological advancements that have shaped its evolution.	Evolution of VLSI Technology	
10-01-2024	I grasp the critical role of VLSI technology in shaping the landscape of modern electronics, elucidating its contributions to the development of advanced computing systems, communication devices, and embedded systems.	Significance of VLSI in Modern Electronics	
11-01-2024	I explored the diverse range of applications for VLSI technology across various industries, including healthcare, automotive, and IoT, recognizing its pervasive influence in driving innovation and technological advancement.	Applications of VLSI Technology Across Industries	
12-01-2024	I recognized the interdisciplinary nature of VLSI system design, gaining insights into its intersections with fields such as computer science, electrical engineering	Interdisciplinary Nature of VLSI System Design	
13-01-2024	Engaged with real-world case studies and practical examples of VLSI system design	Case Studies and Practical Insights	

4.1.1 WEEKLY REPORT

WEEK – 1 (From Dt: 08/01/2024 **to Dt:**13/01/2024)

Objective of the Activity Done:

I introduced myself to the new internship "VLSI". In 1st week I learnt key concepts of VLSI.

Detailed Report:

Week 1 marks the beginning of our journey into Very Large-Scale Integration (VLSI) system design. This week serves as an introduction to the foundational concepts and principles that underpin VLSI technology. I will delve into the basics of VLSI technology, understanding its significance in modern electronics and semiconductor industries. From its origins to its current state of advanced integration, I will explore the evolution of VLSI technology, gaining insights into the key milestones and technological advancements that have shaped the field. Moreover, this week provides a panoramic view of the diverse applications of VLSI technology across various industries, including telecommunications, consumer electronics, automotive, and aerospace. Through real-world examples and case studies, I will witness the transformative impact of VLSI technology on enhancing performance, reducing power consumption, and enabling new functionalities in electronic devices and systems. In addition to exploring thepractical applications of VLSI technology, I will also gain insights into its interdisciplinary nature. They will discoverhow VLSI system design intersects with fields such as computer science, electrical engineering, and materials science. Additionally, I will explore the interdisciplinary nature of VLSI system design, understanding its intersections with fields such as computer science, electrical engineering, and materials science. Through engaging lectures and interactive discussions, I will gain a comprehensive understanding of the interdisciplinary nature of VLSIsystem design, fostering cross-disciplinary insights and collaborations.

4.2 ACTIVITY LOG FOR THE SECOND WEEK

Day & Date	A brief description of the daily activity	Learning Outcome	Person-In-Charge Signature
15-01-2024	I learned about the fundamental building blocks of digital circuits: logic gates. I understand the basic operations and truth tables of popular logic gates such as AND, OR, NOT, NAND, and NOR gates.	Solid understanding of the functions and characteristics of different logic gates	
16-01-2024	I delve into Boolean algebra, the mathematical framework behind digital logic design. I learned about Boolean operators, laws, and theorems, enabling them to manipulate logical expressions effectively.	Ability to manipulate and simplify logical expressions effectively.	
17-01-2024	I explored how logic gates are implemented using electronic components such as transistors. I understand the relationship between logic gates and transistor circuits.	Insight into the physical implementation of logic gates.	
18-01-2024	I learned about combinational logic circuits, which produce output based solely on their current input. I analyzed different types of combinational circuits and their applications.	Ability to analyze and design simple combinational logic circuits.	
19-01-2024	I explored advanced topics in combinational logic design, such as multiplexers, decoders, and encoders. I engaged in practical design exercises and projects	Application of combinational logic design to real-world problems.	
20-01-2024	Last Day of this week, I revised all the topics covered in this week	Demonstrate proficiency in combinational logic design principles.	

4.2.1 WEEKLY REPORT

WEEK – 2 (From Dt: 15/01/2024 **to Dt:** 20/01/2024)

Objective of the Activity Done:

In this week I covered the topics from combination Logic Design and did some hands-on exercises forexperience.

Detailed Report:

In Week 2, I delve into the fundamentals of combinational logic design, a crucial aspect of VLSI system design. This week focuses on understanding the building blocks of digital circuits and the principles governing their operation. I explore various logic gates such as AND, OR, NOT, NAND, and NOR gates, understanding their truth tables and logical operations. I delve into the core principles of combinational logic design, starting with an exploration of Boolean algebra—the mathematical framework that underpins digital logic. They will learn how to manipulate logical expressions using Boolean operators and theorems, gaining proficiency in simplifying complex Boolean functions. Next, I explore the essential components of combinational logic circuits, including logic gates and their corresponding truth tables. Through hands-on exercises and practical examples, I develop the skills to analyze and design basic logic circuits, understanding how different combinations of logic gates perform specific functions. Moreover, I learn about Boolean algebra, a mathematical framework for analyzing and designing digital circuits. Through hands-on exercises and problem-solving tasks, I gain proficiency in simplifying Boolean expressions, implementing logic functions, and designing combinational circuits using logic gates. Throughout the week, I apply their knowledge to practical design exercises and projects, gaining insights into the process of designing and optimizing combinational logic circuits for specific applications. By the end of the week, I have a solid understandingof combinational logic design principles and be ready to tackle more complex design challenges in subsequent weeks.

4.3 ACTIVITY LOG FOR THE THIRD WEEK

Day & Date	A brief description of the daily activity	Learning Outcome	Person- In-Charge Signature
22-01-2024	In Week 3, I started by exploring flip-flops, the foundational elements of sequential circuits. They delve into the operation and behavior of key flip-flop types like D, JK, and T through interactive tutorials.	Able to differentiate between different types of flip-flops and understand their individual functionalities and applications in sequential logic circuits.	
23-01-2024	I delved deeper into sequential storage elements with a focus on registers. Through hands-on exercises, they explore the design and implementation of register-based circuits, learning how registers contribute to data processing, storage, and retrieval in VLSI systems.	Able to design and analyze register-based circuits, understanding their role in storing and manipulating digital data in sequential logic systems.	
24-01-2024	I learned about various types of counters, their architectures, and applications such as frequency division and event counting.	Design and analyze counters for specific applications, understanding timing considerations and clocking strategies involved in counter design.	
25-01-2024	Through guided exercises and practical examples, I learned to design and analyze FSMs, understanding their applications in tasks such as sequence detection, pattern recognition, and control logic implementation.	Design and analyze basic finite-state machines, applying them to solve various sequential logic problems.	
27-01-2024	I delved into optimization strategies to reduce the number of states and transitions in FSMs, enhancing their efficiency and performance.	Apply advanced design techniques to optimize the efficiency and performance of finite-state machines, enabling them to tackle complex sequential logic problems effectively.	

4.3.1 WEEKLY REPORT

WEEK – 3 (From Dt: 22/01/2024 **to Dt:** 27/01/2024**)**

Objective of the Activity Done:

I learned about the concepts of sequential logic circuits like Flip Flops, Registers, Counters.

Detailed Report:

Week 3 marks a pivotal juncture in our exploration as we delve into the intricate realm of sequential logic design. Building upon the foundation laid in combinational logic, I embark on a journey to comprehend the complexities of sequential circuits and finite-state machines. I immerse themselves in the fundamental components of sequential logic, starting with flip-flops, the building blocks of sequential circuits. Through interactive tutorials and hands-on exercises, I grasp the operation and behavior of various types of flip-flops, including D, JK, and T flip- flops, and learn how these elements contribute to the storage and manipulation of digital data. Furthermore, I delve into the concept of registers, sequential storage elements capable of holding multiple bits of data. They explore the design and implementation of register-based circuits, understanding their role in data processing, storage, and retrieval in VLSI systems. Additionally, I delve into counters, sequential circuits tasked with generating a predefined sequence of states. By understanding the operation of counters, I gain insights into applications such as frequency division, event counting, and timing generation in digital systems. Moreover, I explore the concept of finite-state machines (FSMs), powerful models used to represent and control the behavior of sequential systems. Through guided exercises and practical examples, I learn to design and analyze FSMs, understanding their applications in tasks suchas sequence detection, pattern recognition, and control logic implementation. As I navigate through Week 3, they confront timing considerations, clocking strategies, and hazards inherent in sequential logic design. Armed with this knowledge, I am poised to tackle the challenges of designing intricate sequential circuits in VLSI systems, laying the groundwork for advanced exploration in subsequent weeks.

4.4 ACTIVITY LOG FOR THE FOURTH WEEK

Day & Date	A Brief description of the daily activity	Learning Outcome	Person-In-Charge Signature
29-01-2024	I embarked on their journey into synchronous logic design by gaining an understanding of the foundational concepts of synchronous sequential circuits and clocked systems.	Fundamental understanding of synchronous logic design principles	
30-01-2024	I delved deeper into the intricacies of clocked systems and the role of clock signals in synchronizing operations within digital circuits.	acquire proficiency in designing clocked systems and interpreting the behavior of synchronous circuits synchronized to a clock signal.	
31-01-2024	The focus of Day 3 shifts to clock domain crossing, where participants explore techniques for ensuring seamless communication between different clock domains within a VLSI system.	Develop expertise in managing clock domain crossing challenges and applying synchronization	
01-02-2024	Developed into synchronization techniques essential for mitigating metastability and ensuring reliable operation in synchronous systems.	Gain proficiency in implementing synchronization techniques to mitigate metastability and enhance the robustness of synchronous systems.	
02-02-2024	Day 5 is dedicated to hands-on design projects, where participants apply their knowledge and skills to real-world design scenarios.	Ability to apply synchronous logic design principles and synchronization techniques to practical design projects,	
03-02-2024	The final day of the week is devoted to wrap-up and reflection, allowing participants to consolidate my learning and reflect on their experiences throughout the week.	understanding of synchronous logic design, laying the groundwork for further exploration of advanced topics in VLSI system design.	

4.4.1 WEEKLY REPORT

WEEK – 4 (From Dt: 29/01/2024 **to Dt:** 03/02/2024)

Objective of the Activity Done:

I understood the concepts of Synchronous Logic Design like synchronization Techniques, Clock Domain crossing.

Detailed Report:

Week 4 represents a pivotal stage in our journey through VLSI system design as we delve into the intricate realm of synchronous logic design. Building upon the fundamental concepts of combinational and sequential logic, I immerse themselves in the principles and techniques that underpin synchronous circuits. Central to Week 4 is the exploration of synchronous sequential circuits, where I deepen their understanding of circuits synchronized to a clock signal. Through engaging lectures and interactive tutorials, I unravel the operation and behavior of clocked registers, state machines, and synchronous data paths. They grasp the significance of clock signals in coordinating the timing ofoperations within VLSI systems, ensuring reliable and predictable behavior. I delve into the intricacies of designing synchronous circuits that synchronize operations with a global clock signal. They explore techniques for clock domain crossing, ensuring seamless communication between different clock domains within a VLSI system. Moreover, I gain insights into synchronization techniques essential for mitigating metastability and ensuring robust operation in synchronous systems. Through hands-on exercises and design projects, I apply my knowledge to real- world design scenarios, designing synchronous logic circuits and analyzing their performance. They gain practical insights into the challenges of clock domain crossing and synchronization, equipping them with the skills to address timing-related issues in VLSI system design. As I navigate through Week 4, they acquire a comprehensive understanding of synchronous logic design, laying a solid foundation for the synthesis and optimization of synchronous circuits in VLSI systems. This week's exploration sets the stage for advanced studies in timing analysis, clock distribution, and high-performance digital design in subsequent weeks.

4.5 ACTIVITY LOG FOR THE FIFTH WEEK

Day & Date	A brief description of the daily activity	Learning Outcome	Person -In-Charge Signature
05-02-2024	I was introduced to the concept of asynchronous logic design, exploring its significance in VLSI system design and its fundamental differences from synchronous design.	understanding the basics of asynchronous circuits, identifying the limitations of synchronous clocking.	
06-02-2024	I delved into the realm of asynchronous sequential circuits, learning about their behavior and operation. Key topics covered include flip-flop design without clock signals, state transitions.	grasping the principles of asynchronous sequential circuit design and recognizing their applications in VLSI systems.	
07-02-2024	The focus shifts to understanding hazards and race conditions in asynchronous circuits. I learned to identify these timing-related issues, explore their causes, and understand their impact on circuit behavior.	recognizing hazards and race conditions in asynchronous designs, analyzing their effects, and developing strategies to mitigate them effectively.	
08-02-2024	Participants explore handshaking protocols as a crucial aspect of asynchronous communication. They learn about various handshaking techniques and their applications.	understanding the principles of handshaking protocols, selecting appropriate protocols for different applications	
09-02-2024	The focus shifts to state encoding techniques in asynchronous circuit design. Participants learn about different encoding methods, such as one-hot encoding and binary encoding	Mastering state encoding techniques, evaluating their advantages and disadvantages	
10-02-2024	Engaged in hands-on design challenges and practical exercises to apply my knowledge of asynchronous logic design	gaining practical experience in asynchronous circuit design, honing problem-solving skills.	

4.5.1 WEEKLY REPORT

WEEK –5 (From Dt: 05/02/2024 **to Dt:** 10/02/2024**)**

Objective of the Activity Done:

I covered the topics of Asynchronous Logic Design like Asynchronous Sequential Circuits,Hazard Detection, Race Conditions, Handshaking Protocols, State Encoding Techniques

Detailed Report:

In Week 5, our focus shifts to the realm of asynchronous logic design, a cornerstone of VLSI system design characterized by circuits that operate without reliance on a global clock signal. I embark on a journey to understand the intricacies of asynchronous circuits, exploring fundamental principles and design techniques essential for robust and reliable operation in the absence of synchronous clocking. Central to Week 5 is the exploration of asynchronous sequential circuits, where I delve into the behavior and operation of circuits that rely on local timing signals for operation. Through interactive tutorials and engaging discussions, I gain insights into the challenges posed by hazardsand race conditions in asynchronous designs. They learn how to identify and mitigate these timing-related issues to ensure correct functionality and avoid unintended behavior. I explore various techniques for designing asynchronous circuits that exhibit reliable and predictable behavior. They delve into the intricacies of handshaking protocols, which govern communication between asynchronous components, ensuring proper synchronization and data exchange. Additionally, I learn about state encoding techniques, which play a crucial role in achieving robustness and efficiency in asynchronous circuit designs. Through hands-on design challenges and practical exercises, I apply their knowledge to real-world design scenarios, designing and analyzing asynchronous logic circuits. They gain practical experience in addressing timing issues unique to asynchronous designs, equipping them with the skills to design asynchronous circuits that meet stringent performance and reliability requirements. As I navigate through Week 5, they acquire a deep understanding of asynchronous logic design, laying the groundwork for advanced studies in high-performance asynchronous circuit design and optimization. This week's exploration empowers I to harness the full potential of asynchronous logic in the design of complex VLSI systems, paving the way for innovative solutions in modern electronic design.

4.6 ACTIVITY LOG FOR THE SIXTH WEEK

Day & Date	Brief description of the Daily activity	Learning Outcome	Person-In-Charge Signature
12-02-2024	Week 6 started by diving into the fundamental principles of latches and flip-flops, gaining insights into their operation and significance in VLSI system design.	Understand the basic principles underlying latches and flip-flops	
13-02-2024	On Day 2, I delve deeper into the principles governing the behavior of latches. Through in-depth discussions and examples, I explored the operation, timing characteristics, and functionality of latches in digital circuits.	Gain a thorough understanding of the operation and timing characteristics of latches	
14-02-2024	Day 3 focuses on the principles of flip-flops, another essential type of memory element in VLSI design. I learned about the operation, timing characteristics, and types of flip-flops.	Understand the operation and timing characteristics of flip-flops.	
15-02-2024	dedicate Day 4 to exploring the various types of latches and flip-flops in detail. I learned about the distinctive features, advantages, and limitations of D, JK, and T flip-flops	Understand the unique features and characteristics of D, JK, and T flip-flops	
16-02-2024	Day 5 focuses on the practical applications of latches and flip-flops in digital circuit design. Hands-on labs provide participants with practical experience in designing and analyzing memory elements for diverse applications.	Apply latches and flip-flops in practical digital circuit design scenarios. Gain hands-on experience through labs and design projects.	
17-02-2024	The final day of Week 6 is dedicated to recapitulating the key concepts and insights gained throughout the week.	Recapitulate the key concepts and principles of latches and flip-flops.	

4.6.1 WEEKLY REPORT

WEEK – 6 (From Dt: 12/02/2024 **to Dt:** 17/02/2024**)**

Objective of the Activity Done:

I spent more time in this week to know about Memory Element topics like Principles of Latches and Flip-Flops, Operation, Timing Characteristics, Types of Latches and Flip-Flops (D, JK, T), Applications in Digital Circuits

Detailed Report:

Week 6 immerses I in the realm of latches and flip-flops, indispensable memory elements integral to VLSI system design. This week's exploration focuses on understanding the fundamental principles, operation, and applications of these essential building blocks in digital circuits. I embark on a comprehensive journey to grasp the intricate workings of latches and flipflops, essential components for storing and processing digital information in VLSI systems. Through interactive lectures and hands-on activities, I delve into the underlying principles governing the behavior of latches and flip-flops, gaining insights into their role as key memory elements. The week unfolds withan exploration of the distinctive characteristics and functionalities of various types of latches and flip-flops, including D flip-flops, JK flip-flops, and T flip-flops. I examine the unique features and performance attributes of each type, understanding their suitability for different applications in VLSI design contexts. Moreover, I delve into the practical aspects of designing and analyzing memory elements using latches and flip-flops. Through hands-on labs and design projects, I acquire valuable experience in implementing memory elements for diverse applications, ranging from data storage and buffering to synchronization and state retention. As I progress through Week 6, they not only gain a deep understanding of the theoretical foundations of latches and flip-flops but also acquire practical skills in their application within VLSI systems. This immersive exploration sets the stage for I to tackle more advanced topics in memory design, empowering them to design efficient and reliable memory structures for complex VLSI systems.

4.7 ACTIVITY LOG FOR THE SEVENTH WEEK

Day & Date	Brief description of the dailyactivity	Learning Outcome	Person-In-Charge Signature
19-02-2024	I was introduced to Complex Programmable Logic Devices (CPLDs), including Programmable Logic Arrays (PLAs), Programmable Array Logic (PAL), and Programmable Read-Only Memory (PROM).	Understand the basic architecture of CPLDs	
20-02-2024	Through interactive lectures and discussions, I gain insights into the internal structure and functionality of each type of CPLD, exploring how they are programmed	Analyze the internal structure of PLAs, PALs, and PROMs.	
21-02-2024	This session focuses on various programming methods employed in CPLDs, including hardware description languages (HDLs) such as Verilog and VHDL, as well as schematic-based design tools.	Gain proficiency in writing HDL code for CPLD design.	
22-02-2024	I explored the design of combinatorial logic circuits within CPLDs, learning how to implement logic functions using AND, OR, and NOT gates.	Gain practical experience in implementing logic functions using CPLDs.	
23-02-2024	This session focuses on sequential logic design within CPLDs, covering topics such as flip-flops, counters, and state machines. Learned how to design and implement sequential logic circuits using CPLDs	Learn to design flip-flops, counters, and state machines using CPLDs.	
24-02-2024	I was engaged in hands-on labs and design projects aimed at applying their knowledge and skills in CPLD design and programming	Gain hands-on experience in implementing complex logic functions using CPLDs.	

4.7.1 WEEKLY REPORT

WEEK – 7 (From Dt: 19/02/2024 **to Dt:** 24/02/2024**)**

Objective of the Activity Done:

I learned about the Design of CPLDs like Programmable Logic Arrays (PLAs), Programmable Array Logic (PAL), Programmable Read-Only Memory (PROM), Architectures, Programming Methods, Applications in Digital Design.

Detailed Report:

Week 7 delves into the intricate realm of Complex Programmable Logic Devices (CPLDs), versatile integrated circuits pivotal in VLSI system design for realizing complex logic functions. This week's focus is on understanding the architectures, programming methodologies, and diverse applications of CPLDs, including Programmable Logic Arrays (PLAs), Programmable Array Logic (PAL), and Programmable Read-Only Memory (PROM). I embark on an enlightening journey to unravel the inner workings of CPLDs and their constituent elements. Through interactive lectures and comprehensive discussions, I gain a profound understanding of the architectural features and operational principles of PLAs, PALs, and PROMs, discerning their roles as programmable logic components in VLSI designs. The week progresses with an exploration of various programming methods employed in CPLDs, enabling I to grasp the techniques for configuring and customizing CPLDs to implement specific logic functions. I delve into the intricacies of combinatorial and sequential logic design within CPLDs, mastering the art of designing efficient and scalable logic circuits tailored to diverse application requirements. Moreover, I engage in hands-on labs and design exercises aimed at honing their skills in CPLD design and programming. Through practical experimentation and guided projects, I gain invaluable experience in implementing complex logic functions using CPLDs, thereby solidifying their proficiency in leveraging these versatile devices in VLSI system design. As Week 7 draws to a close, I emerge equipped with a comprehensive understanding of CPLD architectures, programming methodologies, and design techniques. Their newfound expertise empowers them to tackle intricate logic design challenges and harness the full potential of CPLDs in realizing sophisticated logic functions within VLSI systems.

4.8 ACTIVITY LOG FOR THE EIGTH WEEK

Day & Date	Brief description of the daily activity	Learning Outcome	Person- In-Charge Signature
26-02-2024	I was introduced to the fundamental concepts of memory devices and their significance in VLSI systems. I explored the basic principles of memory operation and learn about the different types of memory devices, including RAM, ROM, SRAM, and DRAM	Understand the importance of memory devices in VLSI systems.	
27-02-2024	The focus shifts to Random Access Memory (RAM), where I delved into its architecture, operation, and various types. I explored the differences between volatile and non-volatile memory	Understand the distinction between volatile and non-volatile memory.	
28-02-2024	I explored Read-Only Memory (ROM) in detail, examining its principles, functionalities, and types. I learned about (PROM), ROM (EPROM), and (EEPROM).	Understand the various types of ROM and their applications.	
29-02-2024	The day is dedicated to Static Random Access Memory (SRAM), where participants explore its structure, operation, and advantages.	Understand the advantages and applications of SRAM in VLSI design.	
01-03-2024	I delved into Dynamic Random Access Memory (DRAM), understanding its principles, challenges, and advancements. I explored the architecture of DRAM cells, refresh cycles, and data retention mechanisms.	learned about the advancements in DRAM technology and its applications in VLSI design.	
02-03-2024	The final day focuses on advanced memory technologies and emerging trends shaping the memory design landscape. Participants explore non-volatile memories, 3D-stacked memories, and neuromorphic memories, gaining insights into their implications for VLSI system performance and innovation.	Gain insights into the future direction of memory technologies and their impact on the semiconductor industry.	

4.8.1 WEEKLY REPORT

WEEK – 8 (From Dt: 26/02/2024 **to Dt:** 02/03/2024**)**

Objective of the Activity Done:

I spent this week learning advanced concepts Memory devices that are Random Access Memory (RAM), Read-Only Memory (ROM), Static Random Access Memory (SRAM), Dynamic Random Access Memory (DRAM), Principles of Operation, Architectures, Applications, Advanced Memory Technologies, Emerging Trends

Detailed Report:

In Week 8, our exploration of advanced digital design delves into the realm of memory devices, indispensable components within VLSI systems tasked with storing and retrieving data. This week's focus is on comprehensively understanding the intricacies of various memory technologies, including Random Access Memory (RAM), Read-Only Memory (ROM), Static Random Access Memory (SRAM), and Dynamic Random Access Memory (DRAM). I embark on a captivating journey through the inner workings of memory devices, unraveling theiroperational principles, architectural designs, and diverse applications across VLSI system design. Through engaging lectures and interactive discussions, I gain deep insights into the unique characteristics and functionalities of each memory type, discerning their roles as critical components in VLSI systems. The week unfolds with a detailed exploration of the principles governing memory device operation, including data access methods, read and write operations, and memory cell architectures. I delve into the intricacies of RAM, ROM, SRAM, and DRAM technologies, grasping the nuances of their structural designs and operational efficiencies in real-world applications. Moreover, I delve into advanced memory technologies and emerging trends shaping the landscape of memory design.Through insightful discussions and case studies, I gain a forward-looking perspective on the latest advancements in memory technologies, including nonvolatile memories, 3D-stacked memories, and neuromorphic memories, among others. As Week 8 draws to a close, I emerge equipped with a profound understanding of memory device architectures, operational principles, and advanced technologies. Their newfound expertise empowers them to tackle complex memory design challenges and harness the full potential of memory subsystems in driving innovation and performance in VLSI systems.

4.9 ACTIVITY LOG FOR THE NINETH WEEK

Day & Date	Brief description of the Daily activity	Learning Outcome	Person- In-Charge Signature
04-03-2024	I gain an understanding of the overall VLSI system design flow, including its importance in semiconductor design.	Grasping the sequential stages involved in conceiving, designing, and validating VLSI systems.	
05-03-2024	I explored various design methodologies such as top-down, bottom-up, and concurrent methodologies. I had also delved into the concept of design abstraction levels, understanding how VLSI designs are structured hierarchically.	Understanding the strengths and limitations of different design methodologies and navigating between abstraction levels effectively.	
06-03-2024	Focused on the initial stages of the VLSI system design flow, including specification and architectural design. I learned about the objectives, methodologies, and tools employed in these stages.	Gaining insights into capturing design requirements and defining system architecture effectively.	
07-03-2024	I delved into the logic design and physical design stages of the VLSI system design flow. I learned about the techniques and tools used for logic synthesis, floor planning, placement, and routing.	Understand how to translate architectural specifications into logic designs and optimize physical layouts for performance and efficiency.	
08-03-2024	I explored the critical role of verification and validation in the VLSI design flow. I learned about rigorous testing and simulation techniques to ensure design correctness and functionality.	mastering verification and validation techniques at each stage of the design flow, mitigating risks, and optimizing design performance.	
09-03-2024	I engaged in hands-on labs and simulation exercises to apply my knowledge of the VLSI system design flow. I practiced verifying and validating VLSI designs.	Honing their skills in navigating the design flow methodically and efficiently.	

4.9.1 WEEKLY REPORT

WEEK – 9 (From Dt: 04/03/2024 **to Dt:** 09/03/2024**)**

Objective of the Activity Done:

I spent this week learning about VLSI Design Flow that includes Design Methodologies, Design Abstraction Levels, Design Flow Stages, Verification and Validation

Detailed Report:

Understanding the VLSI system design flow is crucial for navigating the complex landscape of semiconductor design effectively. In this segment, I will embark on a comprehensive exploration of the VLSI system design flow, gaining insights into the sequential stages involved in conceiving, designing, and validating VLSI systems. The journey begins with an overview of design methodologies, wherein I learn about various approaches to VLSI system design, including top-down, bottom-up, and concurrent methodologies. Through interactive discussions and case studies, I gain a nuanced understanding of the strengths and limitations of each methodology, enabling themto select the most suitable approach for their design projects. Next, I delve into the concept of design abstraction levels, understanding how VLSI designs are hierarchically structured into different abstraction layers, ranging from system-level descriptions to gate-level implementations. Through practical examples and design exercises, I learn how to navigate between abstraction levels, ensuring design consistency and integrity throughout the design process. The core of the module focuses on the sequential stages of the VLSI system design flow, including specification, architectural design, logic design, physical design, and verification. I gain insights into each stage's objectives, methodologies, and tools employed, enabling them to navigate the design flow methodically and efficiently.

By the conclusion of the module, I emerge equipped with a comprehensive understanding of the VLSI system design flow, empowered to navigate the intricacies of semiconductor design with confidence and proficiency. Their newfound expertise enables them to leverage advanced design methodologies, abstraction techniques, and verification strategies to drive innovation and excellence in VLSI system design.

4.10 ACTIVITY LOG FOT TENTH WEEK

Day & Date	Brief description of the Daily activity	Learning Outcome	Person-In-Charge Signature
11-03-2024	Participants are introduced to Mealy machines, their significance in sequential logic control, and their ability to generate output based on both current states and inputs.	Grasping the basic principles of Mealy machines and recognizing their versatility in various VLSI system design tasks.	
12-03-2024	I learned deeper into Mealy machine operation, learning how these machines transition between states in response to input signals. Through interactive lectures and practical examples, I understand the mechanisms governing state transitions	Mastering the operation principles of Mealy machines and constructing state transition diagrams to represent their behavior accurately.	
13-03-2024	This session focuses on the intricacies of output generation in Mealy machines. Participants explore how the current state and input signals influence the output produced by the machine.	Understanding the relationship between states, inputs, and outputs in Mealy machines and applying this knowledge to design complex control logic.	
14-03-2024	I engaged in interactive tutorials and design challenges that reinforce their understanding of Mealy machine design principles and applications.	Honing problem-solving abilities and gaining confidence in applying Mealy machine concepts to real-world scenarios.	
15-03-2024	In this hands-on session, I worked on a design project focused on sequence detection using Mealy machines.	Applying Mealy machine concepts to practical design tasks and implementing sequence detection algorithms effectively.	
16-03-2024	The final day of the week is dedicated to analysis and review. I reflected on my learning journey throughout the week, discussed challenges encountered, and share insights gained from the experience.	Understanding of Mealy machine design principles, reflecting on practical application experiences,	

4.10.1 WEEKLY REPORT

WEEK – 10 (From Dt: 11/03/2024 **to Dt:** 16/03/2024**)**

Objective of the Activity Done:

I spent this week learning Mealy Machines with concepts of Mealy Machine Operation, StateTransition Diagrams, Output Generation

Detailed Report:

In Week 10, I delve into the realm of Mealy machines, an integral component of sequential logic control in VLSI system design. Mealy machines are finite-state machines characterized by their ability to generate output based on both current states and inputs, making them versatile tools for a wide range of applications. This week's curriculum begins with a comprehensive exploration of Mealy machine operation, wherein I gain a deep understanding of how these machines transition between states in response to input signals. Through interactive lectures and practical examples, I learn to construct state transition diagrams, visual representations that elucidate the behavior of Mealy machines and their response to different input sequences. Furthermore, I delve into the intricacies of output generation in Mealy machines, understanding how the current state and input signals determine the output produced by the machine. Through hands-on exercises and design projects, I gain practical experience in designing Mealy machines to perform tasks such as sequence detection, pattern recognition, and control logic implementation. Throughout the week, I engage in interactive tutorials and design challenges that reinforce their understanding of Mealy machine design principles and applications. By the end of the week, I emerge equipped with the knowledge and skills to design and analyze Mealy machines effectively, empowering them to tackle complex sequential logic control tasks in VLSI system design with confidence and proficiency.

4.11 ACTIVITY LOG FOT ELEVENTH WEEK

Day & Date	Brief description of the Daily activity	Learning Outcome	Person - In-Charge Signature
18-03-2024	I was introduced to the concept of UART communication and its significance in VLSI systems. I learned about the asynchronous nature of data transmission.	Understanding the role of UART in serial data transmission.	
19-03-2024	I learned about framing techniques used in UART communication to delineate data packets. I studied the structure of UART frames, including start and stop bits	Understanding framing techniques in UART communication.	
20-03-2024	I focused on baud rate generation in UART communication, which synchronizes data transmission rates between sender and receiver.	Explored clocking mechanisms for baud rate synchronization.	
21-03-2024	I dissected the architecture of UART modules, examining their internal components and understanding their roles in facilitating data exchange.	Identified and understand the roles of internal components.	
22-03-2024	I dived into UART protocol specifications, including configurations for start and stop bits, parity checking mechanisms, and error detection techniques.	Learned about parity checking mechanisms and error detection techniques.	
23-03-2024	I engaged in hands-on labs and design exercises aimed at reinforcing their understanding of UART implementation techniques.	Gaining proficiency in configuring UART parameters.	

4.11.1 WEEKLY REPORT

WEEK – 11 (From Dt: 18/03/2024 **to Dt:** 23/03/2024**)**

Objective of the Activity Done:

I spent this week learning about UART includes UART Operation, Framing, Baud RateGeneration, Error Detection

Detailed Report:

Week 11 shines a spotlight on the Universal Asynchronous Receiver-Transmitter (UART), a cornerstone communication interface in VLSI systems renowned for its role in facilitating serial data transmission. UART plays a pivotal role in enabling devices to communicate seamlessly with one another, making it an indispensable component in various electronic systems. Throughout this week, I embark onan immersive journey into the intricacies of UART operation. They begin by unraveling the foundational principles behind UART communication, including the asynchronous nature of data transmission, framing techniques for delineating data packets, and baud rate generation for synchronizing data transmission rates between sender and receiver. I delve deep into the architecture of UART modules, dissecting their internal components and understanding their roles in facilitating reliable data exchange. They explore UART protocol specifications, including start and stop bit configurations, parity checking mechanisms, and error detection techniques, essential for ensuring data integrity during transmission. Moreover, I engage in hands-on labs and design exercises aimed at reinforcing their understanding of UART implementation techniques. Through practical experimentation, I gain invaluable experience in designing and integrating UART interfaces into VLSI systems, honing their skills in configuring UART parameters, managing data flow, and troubleshooting communication issues. By the conclusion of Week 11, I emerge equipped with a comprehensive understanding of UART functionality and implementation strategies. Armed with practical skills and theoretical knowledge, they are primed to leverage UART interfaces effectively in VLSI system design, enabling seamless and reliable serial communication in a diverse array of electronic applications.

4.12 ACTIVITY LOG FOT TWELFTH WEEK

Day & Date	Brief description of the Daily activity	Learning Outcome	Person-In-Charge Signature
25-03-2024	I was introduced to the Advanced Peripheral Bus (APB) architecture, its significance in VLSI systems, and its role in connecting peripheral devices to the system bus. I learned about the basic principles underlying APB operation	Understand the importance of APB architecture in VLSI systems.	
26-03-2024	I learned about APB master architecture, exploring its internal components and functionalities essential for orchestrating communication with peripheral devices. I learned about register access protocols for read and write operations	Understand the internal components and functionalities of APB master architecture.	
27-03-2024	I engaged in hands-on tutorials focusing on configuring APB master modules and setting up bus parameters.	Developed proficiency in designing APB master interfaces and configuring data transfer protocols.	
28-03-2024	I continued with hands-on tutorials, focusing on implementing efficient data transfer protocols in APB master interfaces. I worked on design projects aimed at reinforcing their comprehension of APB operation principles and implementation strategies.	Gain hands-on experience in designing and implementing APB master interfaces in real-world scenarios.	
29-03-2024	I analyzed case studies and real-world application examples showcasing the use of APB master interfaces in VLSI system design.	Gained insight into best practices and implementation strategies	
30-03-2024	On the last day, I reviewed key concepts covered throughout the training program and reflect on my learning journey, identifying areas for further improvement and advancement.	Reviewed and reinforce key concepts covered throughout the training program.	

4.12.1 WEEKLY REPORT

WEEK – 12 (From Dt: 25/03/2024 **to Dt:** 30/03/2024**)**

Objective of the Activity Done:

I learned about the topics of APB Master where topics like APB Operation Principles, BusProtocols, Timing Diagrams, Transaction Types are included.

Detailed Report:

In Week 12, I dive into the realm of Advanced Peripheral Bus (APB) architecture, a pivotal interface widely employed in VLSI systems to connect peripheral devices to the system bus. APB architecture plays a critical role in facilitating efficient communication between the central processing unit (CPU) and peripheral devices, enabling seamless interaction and data exchange within VLSI systems. Throughout this week, I embark on an exploratory journey into the intricate workings of APB operation. They delve into the fundamental principles underpinning APB architecture, including bus protocols governing data transmission, timing diagrams illustrating signal transitions, and various transaction types dictating communication patterns between master and slave devices. I gain a comprehensive understanding of APB master architecture, unraveling its internal components and functionalities essential for orchestrating communication with peripheral devices. They explore register access protocols governing read and write operations, arbitration mechanisms ensuring fair access to the bus, and error handling techniques for maintaining data integrity. Moreover, I engage in hands-on tutorials and design projects designed to reinforce their comprehension of APB master interfaces. Through practical exercises, I hone their skills in designing APB master modules, configuring bus parameters, and implementing efficient data transfer protocols. By the culmination of Week 12, I emerge equipped with a profound understanding of APB operation principles and implementation strategies. Empowered with practical skills and theoretical knowledge, they are poised to leverage APB master interfaces adeptly in VLSI system design, facilitating seamless communication and interoperability between central processing units and peripheral devices in a diverse array of electronic applications.

4.13 ACTIVITY LOG FOT THIRTEENTH WEEK

Day & Date	Brief description of the Daily activity	Learning Outcome	Person-In-Charge Signature
01-04-2024	I received an overview of ALU architecture, understanding its role as a fundamental component in VLSI systems.	Understand the role of ALU in VLSI systems.	
02-04-2024	I explored arithmetic circuits within the ALU, focusing on operations such as addition, subtraction, multiplication, and division. I learned about various algorithms and techniques employed to perform arithmetic operations efficiently.	Learned algorithms and techniques for performing arithmetic operations.	
03-04-2024	I delved into logic circuits within the ALU, covering bitwise operations, comparisons, and conditional branching.	Gained proficiency in designing logic circuits for executing logical manipulations.	
04-04-2024	I explored the intricacies of instruction set design for the ALU, understanding the repertoire of operations supported and the corresponding instruction formats used to encode operands and operations.	Understand the components of instruction set design for the ALU.	
05-04-2024	I delved into performance optimization techniques for the ALU, including parallel processing, pipelining, and hardware acceleration. I understand how these techniques enhance computational efficiency	Uderstand the principles of parallel processing, pipelining, and hardware acceleration.	
05-04-2024	I engaged in hands-on labs and design exercises, applying the theoretical concepts learned throughout the week to practical implementation.	Gained proficiency in optimizing ALU design for performance, area, and power efficiency.	

4.13.1 WEEKLY REPORT

WEEK – 13 (From Dt: 01/04/2024 **to Dt:** 06/04/2024**)**

Objective of the Activity Done:

I learned about ALU (Arithmetic Logic Unit) topics like ALU Architecture, Instruction SetDesign, Arithmetic and Logic Operations

Detailed Report:

In Week 13, I immerse themselves in the intricacies of the Arithmetic Logic Unit (ALU), acornerstone component within VLSI systems tasked with executing arithmetic and logic operations. As the computational powerhouse of digital systems, the ALU plays a pivotal role in performing fundamental mathematical calculations and logical manipulations essential for a myriad of applications. Throughout this week, I embark on a comprehensive exploration of ALU architecture, delving into its internal structure, organization, and operation principles. They dissect the various components comprising an ALU, including arithmetic circuits for addition, subtraction, multiplication, and division, as well as logic circuits for bitwise operations, comparisons, and conditional branching. Moreover, I delve into the intricacies of instruction set design, elucidating the repertoire of operations supported by the ALU and the corresponding instruction formats used to encode operands and operations. They explore strategies for optimizing ALU performance, including parallel processing techniques, pipelining, and hardware acceleration, to meet the computational demands of modern VLSI systems. Through a series of hands-on labs and design exercises, I translate theoretical concepts into practical implementation, synthesizing ALU modules with support for various data formats, precision levels, and operation modes. They acquire proficiency in designing ALU architectures tailored to specific application requirements, optimizing for performance, area, and power efficiency. By the conclusion of Week 13, I emerge with a deep understanding of ALU design principles and methodologies, equipped with the skills to architect, implement, and integrate ALU modules into VLSI systems for high-performance computation and data processing. Armed with this knowledge, they are primed to tackle complex computational tasks and drive innovation in diverse fields ranging from embedded systems and digital signal processing to artificial intelligence and scientific computing

4.14 ACTIVITY LOG FOR FOURTEENTH WEEK

Day & Date	Brief description of the Daily activity	Learning Outcome	Person-In-Charge Signature
08-04-2024	I was introduced to the Inter-Integrated Circuit (I2C) communication protocol, understanding its significance in VLSI systems. I learned about the basic principles of I2C, including the roles of SDA and SCL lines	Understand the fundamental concepts of I2C communication and recognize its applications in integrated circuit design.	
09-04-2024	I learned about the operational mechanisms of the I2C protocol, exploring how SDA and SCL lines coordinate data transmission between devices.	understand the sequence of events in I2C communication and identifying the components involved in data transfer.	
10-04-2024	I learned about addressing schemes in the I2C protocol, including 7-bit and 10-bit addressing modes. I understand how addressing enables communication between multiple devices on the same bus.	Mastering the concepts of device addressing and implementing addressing schemes in I2C communication.	
11-04-2024	I explored data transfer protocols in the I2C communication, including write and read operations, repeated start conditions, and multi-byte transfers. I learned how data is formatted and transferred between master and slave devices.	Understand data transfer protocols and implement them in I2C communication interfaces.	
12-04-2024	I delved into advanced topics such as bus arbitration and collision detection in the I2C protocol. I learned how multiple devices contend for control of the bus	Understand bus arbitration strategies and implementing collision detection mechanisms in I2C interfaces.	
13-04-2024	On the last day, I explored techniques to minimize latency and overhead while maximizing communication efficiency.	Developed skills in optimizing I2C communication interfaces and applying them to design projects in VLSI systems.	

4.14.1 WEEKLY REPORT

WEEK – 14 (From Dt: 08/04/2024 **to Dt:** 13/04/2024**)**

Objective of the Activity Done:

I spent this week learning about: SDA & SCL (Serial Data Line & Serial Clock Line) includes Inter-Integrated Circuit (I2C) Communication Protocol, Bus Arbitration, Addressing, Data Transfer Protocols

Detailed Report:

In Week 14, I embark on a deep dive into the intricacies of the Serial Data Line (SDA) andSerial Clock Line (SCL), pivotal components that underpin the Inter-Integrated Circuit (I2C) communication protocol within VLSI systems. As fundamental elements of I2C communication, SDA and SCL facilitate seamless inter-device communication, enabling efficient data exchange between integrated circuits. Throughout this week, I unravel the principles of the I2C communication protocol, delving into its operational mechanisms, addressing schemes, and data transfer protocols. They explore the intricate dance between the SDA and SCL lines, understanding how these signals coordinate the transmission of data between I2C master and slave devices with precision and reliability. Moreover, I delve into advanced topics such as bus arbitration, where multiple devices contend for control of the communication bus, and collision detection mechanisms ensure data integrity and protocol compliance. They examine strategies for efficient addressing and data transfer, optimizing communication efficiency while minimizing latency and overhead. Through a series of interactive tutorials and design projects, I gain hands-on experience in designing I2C master and slave interfaces, synthesizing their theoretical understanding into practical implementation. They develop a nuanced understanding of the timing characteristics, protocol constraints, and error-handling mechanisms inherent in I2C communication, equipping them with the skills to design robust and resilient communication interfaces for VLSI systems. By the conclusion of Week 14, I emerge with a profound appreciationfor the role of SDA and SCL in facilitating seamless communication within VLSI systems. Empowered with practical insights and design expertise, they are well-equipped to tackle the challenges of integrating I2C interfaces into complex VLSI architectures, ensuring reliable serial communication and interoperability across interconnected devices.

4.15 ACTIVITY LOG FOT FIFTEENTH WEEK

Day & Date	Brief description of the Daily activity	Learning Outcome	Person - In-Charge Signature
15-04-2024	I was introduced to the fundamental concepts of histogram framers, their role in digital imaging and signal processing applications, and their importance in VLSI systems.	Understand the basic principles of histogram framers, their applications in real-world scenarios.	
16-04-2024	I learned about the operational principles of histogram framers, including data sampling, quantization, and histogram generation.	Comprehensive understanding of how histogram framers' function, the processes involved in data sampling and quantization	
17-04-2024	On this day, I explored different quantization algorithms used in histogram framers and strategies for optimizing dynamic range.	Understand the intricacies of quantization algorithms, techniques for optimizing dynamic range to preserve image fidelity	
18-04-2024	I learned about the design considerations involved in designing histogram framer modules capable of accommodating diverse image formats, pixel depths, and processing modes.	Understand the design requirements for histogram framer modules, including considerations for image format compatibility, pixel depth optimization, and processing mode flexibility.	
19-04-2024	On the final day, I reflected on my learning journey and consolidate my understanding of histogram framer operation, design considerations, and integration strategies. Through group discussions and practical exercises, I applied my knowledge to real-world design scenarios, reinforcing my skills in VLSI system design.	Ability to effectively design and deploy histogram framer modules in diverse VLSI applications, with confidence and proficiency.	

4.15.1 WEEKLY REPORT

WEEK – 15 (From Dt: 15/04/2024 **to Dt:** 19/04/2024**)**

Objective of the Activity Done:

I spent this week learning advanced concepts of Histogram Framer like: Operation Principles of Histogram Framers, Data Sampling, Quantization, Histogram Generation

Detailed Report:

In the culminating week of our journey through VLSI system design, I delve into the intricate realm of histogram framers, specialized components essential for digital imaging and signal processing applications. With a laser focus on real-world applications, I gain a comprehensive understanding of the principles and practicalities of integrating histogram framers into VLSI systems. Week 15 serves as a synthesis of the theoretical and practical knowledge acquired throughout the course, providing I with the tools and techniques necessary to design and deploy histogram framer modules effectively. Through a combination of theoretical discussions, hands-on labs, and design projects, I explore the operational nuances of histogram framers, from data sampling and quantization to histogram generation. In particular, I examine the intricacies of designing histogram framer modules capable of accommodating diverse image formats, pixel depths, and processing modes. They delve into the intricacies of quantization algorithms, exploringstrategies for optimizing dynamic range and preserving image fidelity in various processing scenarios. Moreover, I engage in practical exercises aimed at integrating histogram framer modules into VLSI systems for real-time image processing and analysis. By applying their theoretical understanding to real-world design challenges, I hone their design skills and gain practical insights into the complexities of integrating histogram framers into VLSI architectures. As I navigate the final week of the course, they emerge with a comprehensive understanding of histogram framer operation, design considerations, and integration strategies. Equipped with practical expertise and theoretical insights, I am poised to tackle the challenges of designing and deploying histogram framer modules in diverse VLSI applications, from digital cameras to image processing pipelines, with confidence and proficiency

CHAPTER 5: OUTCOMES DESCRIPTION

5.1 Work Environment I have Experienced

Foundations, such as the SkillDzire Organization, serve as catalysts for change, often supportingand empowering grassroots initiatives, social entrepreneurs, and community-driven projects. Their workis not solely defined by the financial assistance they provide but also by the expertise, knowledge, and networks they bring to the table. Foundations create an environment where innovation, research, and solutions can flourish.

One of the most remarkable aspects of nonprofit work is the dedication and passion of those involved. People choose to work in these organizations not for personal gain but for the fulfillment of their mission. They are motivated by a shared sense of purpose, and it is this dedication that often leads to innovative solutions, partnerships, and an unwavering commitment to social and environmental causes. They are the embodiment of what's possible when individuals and communities unite in the pursuit of a better world. The work of organizations like the SkillDzire Organization reminds us that even in the face of daunting global issues, positive change is not only possible but is actively being pursued by passionate individuals and organizations committed to making a difference.

5.2 Real time technical skills I have experienced

In a Skill Dzire VLSI internship, participants can expect to gain hands-on experience with various real-timetechnical skills relevant to the field of VLSI (Very Large-Scale Integration) design. Here are some specific technical skills that interns might experience during the internship:

1. **VLSI Design Tools Proficiency:** Interns will gain practical experience with industry-standard VLSIdesign tools such as Cadence, Synopsys, or Mentor Graphics. They will learn how to use these tools fortasks such as schematic capture, simulation, synthesis, place and route, and physical verification.
2. **RTL Coding:** Interns will learn and practice RTL (Register Transfer Level) coding using hardware description languages (HDLs) such as Verilog or VHDL. They will gain hands-on experience writing RTLcode to describe digital circuits and systems.

3. **Simulation and Verification**: Interns will gain experience with simulation and verification techniques toensure the correctness and functionality of their designs. This may include functional simulation, timing simulation, and formal verification methods**.**

4. **Physical Design:** Interns will learn about physical design techniques for VLSI chips, including floor planning, placement, routing, and layout. They will gain hands-on experience using physical design tools tooptimize chip area, performance, and power consumption.

5. **Timing Analysis and Optimization:** Interns will learn about timing analysis techniques to ensure that their designs meet timing constraints and performance goals. They will gain practical experience optimizingdesigns for timing closure.

6. **Low Power Design:** Interns will learn about low power design techniques for VLSI circuits, including power gating, clock gating, voltage scaling, and other power optimization strategies. They will gain hands- on experience implementing these techniques in their designs.

7. **Design for Testability (DFT):** Interns will learn about DFT principles and methodologies to ensure thetestability and manufacturability of their designs. They will gain practical experience with scan insertion, ATPG (Automatic Test Pattern Generation), and other DFT techniques.

5.3 Managerial skills you have acquired

5.1.1 Communication skills:

This is big one. I improved my communication skills a lot than before. While speaking to my mentor or to the Salesforce Org I have been through speaking in English made my communication skill practice and better than before.

5.1.2 An appetite for learning

Curiosity motivated me to investigate and study the platform. It made me more engaged in real time work experience.

5.4 How I improved my communication skills

I am a communicative person who established an outstanding rapport with others. I am able to listen deeply to people, to help them, to share my experience with them. Many of them tell me I am a good listener and when I talk, they usually listen to me. I understand how peopleinterpret my communicative style and I am able to avoid misunderstanding. I sometimes handlechildren's hassles effectively.

People usually understand my thoughts and I can understand theirs. The tone of my voicesometimes communicates how I feel about my partner. Determining a communication problemis not very hard for me and I am often able to resolve it. I usually speak in a gentle manner, to give an impression of kindness. I often stay calm in tense situations. I can express my feelings and tell people close to me how much I care about them. My relationship with my family is fullof emotion and devotion. Many people think I am a friendly and expansive person. I often knowhow to cooperate with them and they usually do what I want them to do.

However, I have not always been so successful. I was shy when I was younger and did not speak with assertion. It was hard for me to express my thoughts; it was hard for others to know how I felt about something. Later, I improved my communication skills. During my experience, I began to speak louder and people could understand me. I listened to others more carefully. I learned that it is important to avoid passive style of communication. I also learned to speak with more assertion because my own opinion is as important as the opinion of other people.

5.5 Group Discussion:

In group discussion I have interacted with my friends who are doing the same internship. I actively participate in the discussion and we went through different question in the discussion I have actively discuss about learning objectives I had a great time with group discussion.

5.6 Participation in teams:

In participate in group will make us so supportive and also, we can have the team support to know about the problems we don’t know so I also active in team participation and also knowingabout unknow things and tell them the known things.

5.7 Contribution as a team member:

As a team member I discussed about the topics and I also explain the things which I have learned and also getting knowledge by asking my doubts with my team mates. I have contributedthat by telling the unknow questions by knowing.

5.8 Technological developments I have observed, and which are relevant to the subject area of training:

Technological advancements in the field of VLSI design have significantly influenced the landscape of semiconductor industry. Continuous progress in semiconductor manufacturing processes has led to smaller process nodes, enabling higher transistor density, improved performance, and lower power consumption. Moreover, the integration of AI and machine learning techniques in VLSI design has opened up new possibilities for optimization and automation. The trend towards heterogeneous integration and 3D IC integration offers opportunities to combine different semiconductor technologies into single chips or packages, while advanced packaging technologies like FOWLP and SiP contribute to compact and high- performance device designs. Power management and energy efficiency remain crucial considerations, driving the adoption of low-power design methodologies and dynamic voltage scaling. Additionally, with cybersecurity threats on the rise, ensuring the security and trustworthiness of VLSI designs has become increasingly important, prompting exploration into hardware security primitives and secure design methodologies. Lastly, the nascent field of quantum computing poses both challenges and opportunities for VLSI designers, with potential implications for the design of quantum circuits and error correction techniques. These developments shape the curriculum and training in VLSI internships, ensuring that participants are equipped with the latest knowledge and skills to address current and future challenges in semiconductor design.

Student Self Evaluation of the Long-Term Internship

Student's Name: Harsha Devara

Registration No: 20P31A04J4

Term of Internship: 15 Weeks **From:** 08/01/2024 **To:** 19/04/2024

Date of Evaluation:

- Please rate your performance in the following areas:
- **Rating Scale:** 1 is lowest and 5 is highest rank
- **Letter grade of CGPA calculation to be provided**

1	Oral communication	1	2	3	4	5
2	Written communication	1	2	3	4	5
3	Proactiveness	1	2	3	4	5
4	Interaction ability with community	1	2	3	4	5
5	Positive Attitude	1	2	3	4	5
6	Self-confidence	1	2	3	4	5
7	Ability to learn	1	2	3	4	5
8	Work Plan and organization	1	2	3	4	5
9	Professionalism	1	2	3	4	5
10	Creativity	1	2	3	4	5
11	Quality of work done	1	2	3	4	5
12	Time Management	1	2	3	4	5
13	Understanding the Community	1	2	3	4	5
14	Achievement of Desired Outcomes	1	2	3	4	5
15	**OVERALL PERFORMANCE**	**1**	**2**	**3**	**4**	**5**

Date: **Signature of the Student**

Evaluation by the Supervisor of the Intern Organization

Student's Name: Harsha Devara

Registration No: 20P31A04J4

Term of Internship: 15 Weeks **From:** 08/01/2024 **To:** 19/04/2024

Date of Evaluation:

Organization Name & Address:

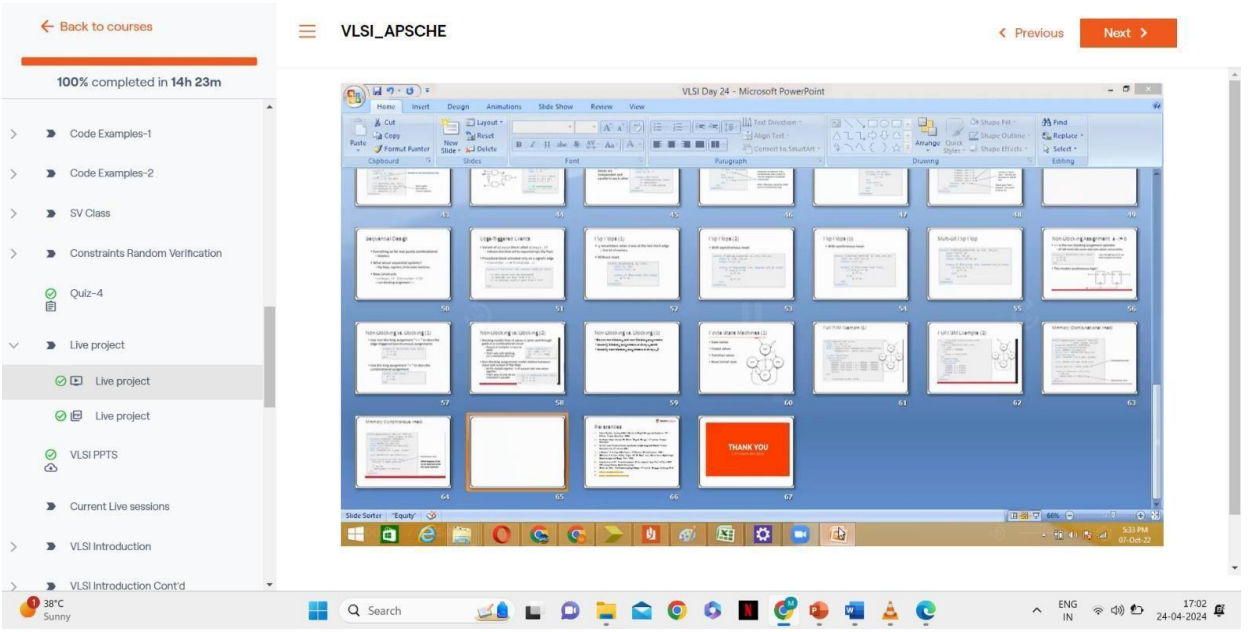
Name & Address of the Supervisor with Mobile Number:

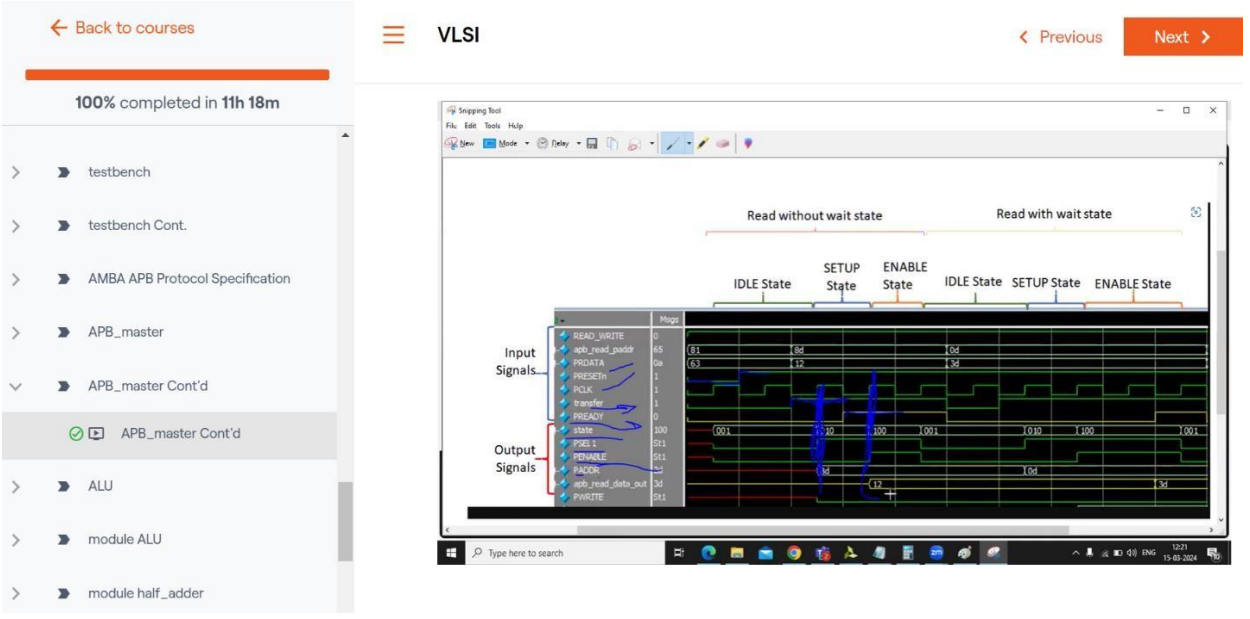
- Please rate the student's performance in the following areas:
- Please note that your evaluation shall be done independent of the student's self- evaluation
- Rating Scale: 1 is lowest and 5 is highest rank

1	Oral communication	1	2	3	4	5
2	Written communication	1	2	3	4	5
3	Proactiveness	1	2	3	4	5
4	Interaction ability with community	1	2	3	4	5
5	Positive Attitude	1	2	3	4	5
6	Self-confidence	1	2	3	4	5
7	Ability to learn	1	2	3	4	5
8	Work Plan and organization	1	2	3	4	5
9	Professionalism	1	2	3	4	5
10	Creativity	1	2	3	4	5
11	Quality of work done	1	2	3	4	5
12	Time Management	1	2	3	4	5
13	Understanding the Community	1	2	3	4	5
14	Achievement of Desired Outcomes	1	2	3	4	5
15	**OVERALL PERFORMANCE**	**1**	**2**	**3**	**4**	**5**

Date: **Signature of the Supervisor**

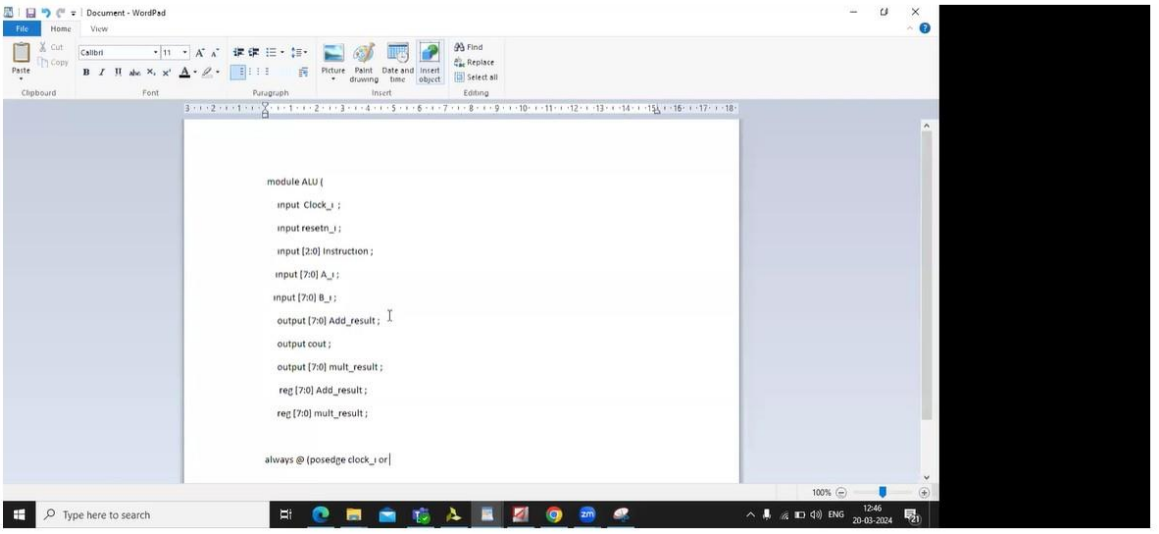
5.8.1 PHOTOS & VIDEO LINKS



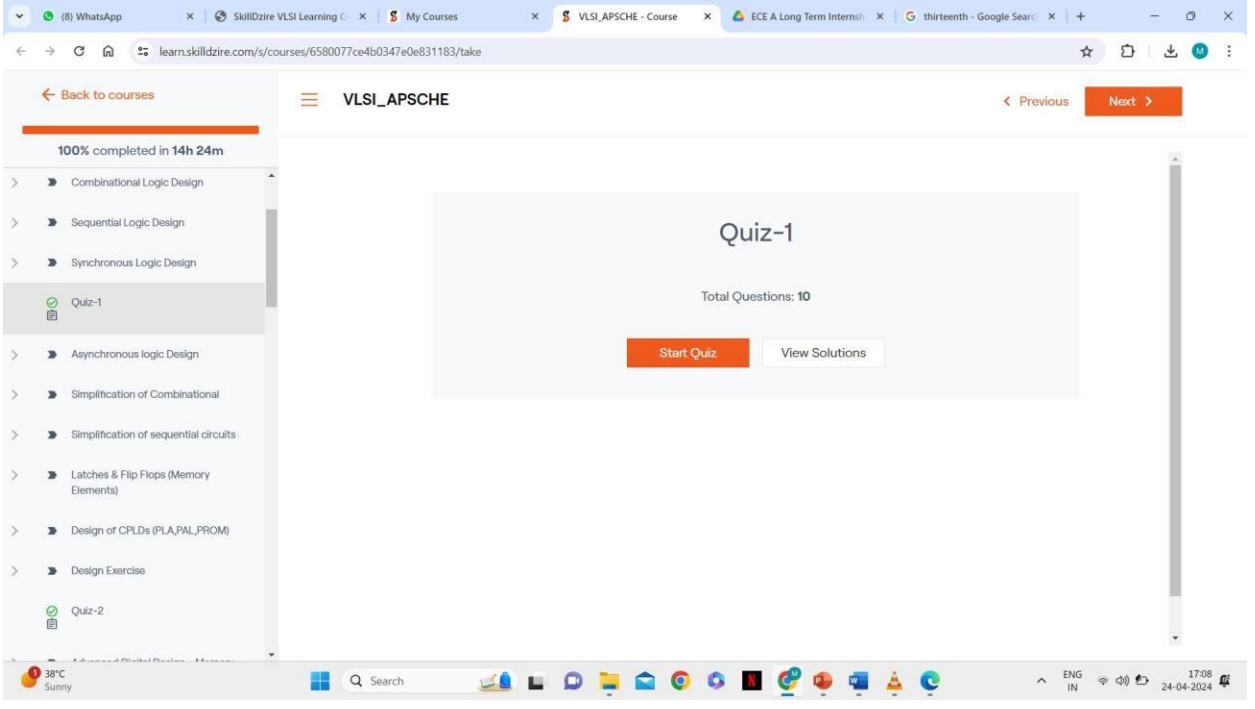


VLSI

Previous Next



module ALU



EVALUATION

Internal Evaluation for Short Term Internship (On-site/Virtual)

Objectives:

- To integrate theory and practice.
- To learn to appreciate work and its function towards the future.
- To develop work habits and attitudes necessary for job success.
- To develop communication, interpersonal and other critical skills in the future job.
- To acquire additional skills required for the world of work.

Assessment Model:

- There shall only be internal evaluation.
- The Faculty Guide assigned is in-charge of the learning activities of the students and for the comprehensive and continuous assessment of the students.
- The assessment is to be conducted for 100 marks.
- The number of credits assigned is 4. Later the marks shall be converted into grades and grade points to include finally in the SGPA and CGPA.
- The weightings shall be:
    - Activity Log 25 marks
    - Internship Evaluation 50marks
    - Oral Presentation 25 marks
- Activity Log is the record of the day-to-day activities. The Activity Log is assessed on an individual basis, thus allowing for individual members within groups to be assessed this way. The assessment will take into consideration the individual student's involvement in the assigned work.
- While evaluating the student's Activity Log, the following shall be considered –

  a. The individual student's effort and commitment.

  b. The originality and quality of the work produced by the individual student.

  c. The student's integration and co-operation with the work assigned.

  d. The completeness of the Activity Log.
- The Internship Evaluation shall include the following components and based on Weekly Reports and Outcomes Description

    a. Real Time Technical Skills acquired.
    b. Managerial Skills acquired.
    c. Improvement of Communication Skills.
    d. Team Dynamics
    e. Technological Developments recorded.

MARKS STATEMENT

(To be used by the Examiners)

INTERNAL ASSESSMENT STATEMENT

Name Of the Student:

Programme of Study:

Year of Study:

Group:

Register No/H.T.No:

Name of the College:

University:

Sl.No	***Evaluation Criterion***	***Maximum Marks***	***Marks Awarded***
1.	Activity Log	25	
2.	Internship Evaluation	50	
3.	Oral Presentation	25	
	GRAND TOTAL	100	

Date: Signature of the Faculty Guide

Certified by

Date: Signature of the Head of the Department/Principal

Seal