sync_signal

Description

This core is used to cross clock domains: to take an asynchronous signal (or synchronous to a different clock domain) and to synchronize it into your clock domain, so you can use the signal safely without the dangers of metastability. All external inputs to an FPGA should pass through a sync_signal core. This core can also be used to pass signals between clock domains inside of an FPGA, in case you are unlucky enough to require multiple clock domains.

Verilog Template

```
sync_signal #(
    WIDTH=1)
sync_signal_inst (
    .clk(clk),  // input
    .in(in),    // input [WIDTH-1:0]
    .out(out)); // output [WIDTH-1:0]
);
```

Specifications

Parameters

Parameter WIDTH is the width of the input and output signals.

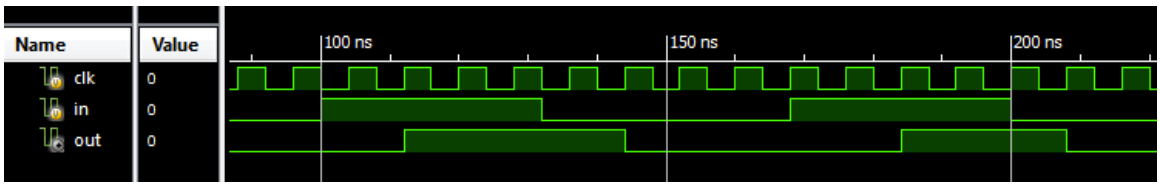
Inputs

- clk: clock
- in [WIDTH]: signal from the asynchronous domain

Outputs

- out [WIDTH]: synchronized signal in the clock domain of clk

Waveform



Requirements

Language for Synthesis: Verilog 2001

Synthesis Tool: Xilinx XST 13.2
Language for Verification: Verilog 2001
Verification Tool: Xilinx ISIM 13.2

References

[1] http://www.fpga4fun.com/CrossClockDomain.html
[2] http://web.mit.edu/6.111/www/f2006/handouts/labs/lab3.html

Contact Info

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