sync_reset

Description

This module is similar to sync_signal in that it is used to cross clock domains. However, this module is specialized for active-high resets. When the asynchronous input reset signal is asserted, the reset is immediately propagated to the output. When the asynchronous input reset signal is deasserted, it takes N clock cycles for the synchronizer flip-flop pipeline to feed a zero to the output. The single parameter N gives the number of synchronization flip-flops, and hence the delay from when the asynchronous input reset signal is deasserted to when the synchronous output reset signal is deasserted.

Verilog Template

```
sync_reset #(
    .N(2))
sync_reset_inst (
    .clk(clk),                          // input
    .rst(rst),                          // input
    .sync_reset_out(sync_reset_out)); // output
);
```

Specifications

Parameters

N: number of synchronization flip-flops, must be at least 2

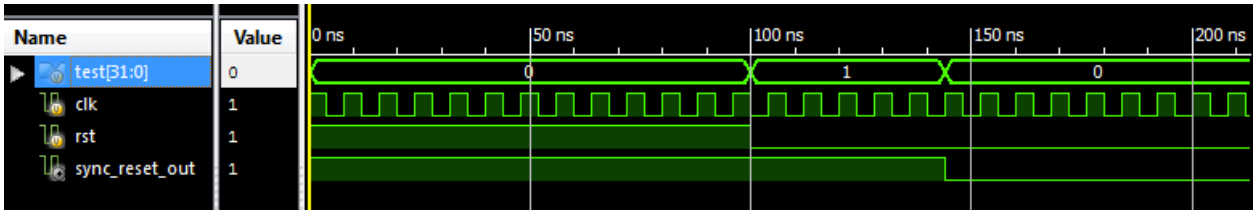
Inputs

- clk: clock
- rst: asynchronous, active-high reset input

Outputs

- sync_reset_out: synchronous, active-high reset output

Waveform



Requirements

Language for Synthesis: Verilog 2001
Synthesis Tool: Xilinx XST 13.2
Language for Verification: Verilog 2001
Verification Tool: Xilinx ISIM 13.2

References

[1] http://www.fpga4fun.com/CrossClockDomain.html
[2] http://web.mit.edu/6.111/www/f2006/handouts/labs/lab3.html

Contact Info

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