# timer

## Description

This is a very simple timer with the number of clock ticks specified during instantiation. The timer can be armed and rearmed, and also enabled and disabled. When the timer fires, the fire output signal stays asserted until either arm is asserted or en is deasserted.

## Verilog Template

```
timer #(
    .TIMER_PERIOD_NS(80),
    .CLOCK_PERIOD_NS(8))
timer_inst (
    .arm(arm),  // input
    .clk(clk),  // input
    .en(en),    // input
    .fire(fire) // output
);
```

## Specifications

### Parameters

TIMER_PERIOD_NS is the amount of time taken for the timer to expire once armed. Units are in nanoseconds. Default value is 80ns.

CLOCK_PERIOD_NS is the period of the common clock. Units are in nanoseconds. Default value is 8ns (125MHz).

NTICKS is the number of clock ticks to count until the timer expires. Default value is TIMER_PERIOD_NS / CLOCK_PERIOD_NS. This value can be specified directly in case the clock period is not an integral number of nanoseconds.

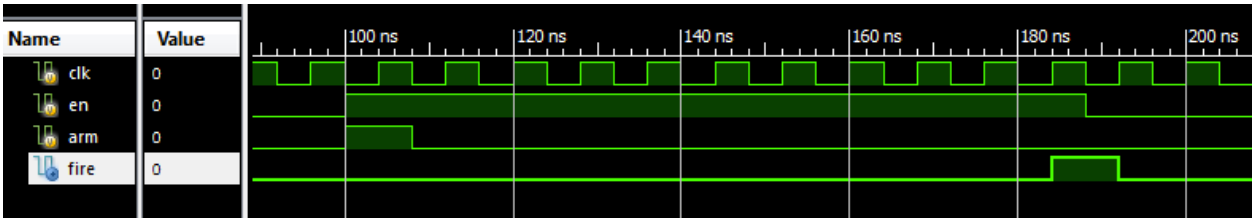
### Inputs

- arm: resets the timer
- clk: clock
- en: enables the timer

### Outputs

- fire: asserted when the timer expires and when en is asserted, cleared when arm is asserted

## Waveform




## Requirements

Language for Synthesis: Verilog 2001
Synthesis Tool: Xilinx XST 13.2
Language for Verification: Verilog 2001
Verification Tool: Xilinx ISIM 13.2

## Contact Info

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