async_muller_c_element

Description

This Muller C-element is an asynchronous latch. It is often used to indicate that two or more asynchronous cores are ready.

Verilog Template

```
async_muller_c_element #(
    .WIDTH(2))
async_muller_c_element_inst (
    .in(in),  // input [WIDTH-1:0]
    .out(out) // output
);
```

Specifications

Parameters
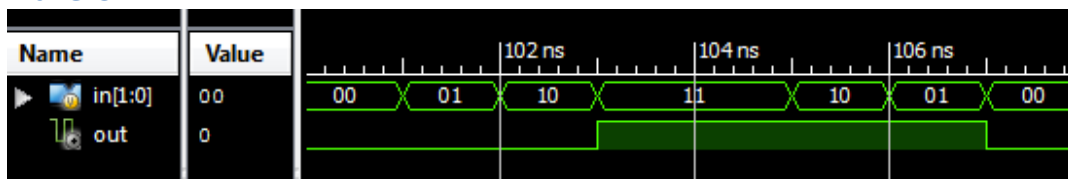
WIDTH is the width of the input.

Inputs

- in [WIDTH]: ready signals from other asynchronous cores

Outputs

- out: 0 if all inputs are 0, or 1 if all inputs or 1, otherwise latches its current output

Waveform

Requirements

Language for Synthesis: Verilog 2001
Synthesis Tool: Xilinx XST 13.2
Language for Verification: Verilog 2001
Verification Tool: Xilinx ISIM 13.2

References

[1] https://en.wikipedia.org/wiki/C-element
[2] http://tams-www.informatik.uni-hamburg.de/applets/hades/webdemos/16-flipflops/70-cgate/muller-cgate3.html

Contact Info

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