edge_detector

Description

Detects rising or falling signal edges and asserts the proper output for a single clock cycle tick. Edge detectors are important building blocks for a variety of digital communication circuits. This implementation uses a Moore machine to delay the output by one clock cycle.

Verilog Template

```
edge_detector
edge_detector_inst (
    .clk(clk),                  // input
    .in(in),                    // input
    .negedge_out(negedge_out), // output
    .posedge_out(posedge_out)  // output
);
```

Specifications

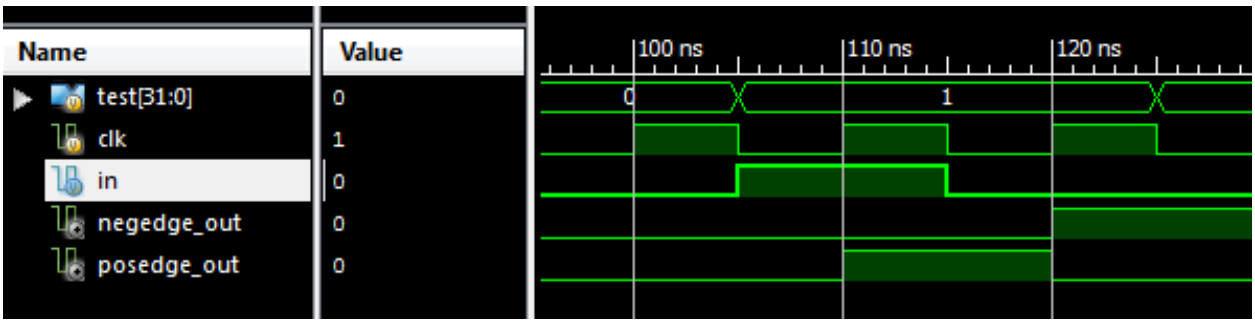
Inputs

- clk: clock
- in: slowly-varying input signal from which to detect edges

Outputs

- negedge_out: asserted for one clock cycle after a falling signal edge has been detected
- posedge_out: asserted for one clock cycle after a rising signal edge has been detected

Waveform



Requirements

Language for Synthesis: Verilog 2001
Synthesis Tool: Xilinx XST 13.2
Language for Verification: Verilog 2001
Verification Tool: Xilinx ISIM 13.2

Contact Info

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