**edge\_detector**

# Description

Detects rising or falling signal edges and asserts the proper output for a single clock cycle tick. Edge detectors are important building blocks for a variety of digital communication circuits. This implementation uses a Moore machine to delay the output by one clock cycle.

# Verilog Template

edge\_detector

edge\_detector\_inst (

.clk(clk), // input

.in(in), // input

.negedge\_out(negedge\_out), // output

.posedge\_out(posedge\_out) // output

);

# Specifications

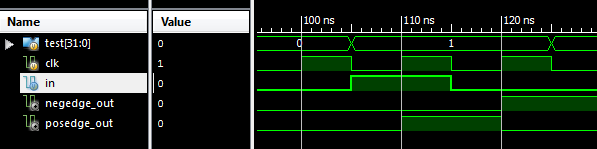
## Inputs

* clk: clock
* in: slowly-varying input signal from which to detect edges

## Outputs

* negedge\_out: asserted for one clock cycle after a falling signal edge has been detected
* posedge\_out: asserted for one clock cycle after a rising signal edge has been detected

## Waveform



# Requirements

Language for Synthesis: Verilog 2001

Synthesis Tool: Xilinx XST 13.2

Language for Verification: Verilog 2001

Verification Tool: Xilinx ISIM 13.2

# Contact Info

Nathan Farrington

<http://nathanfarrington.com>