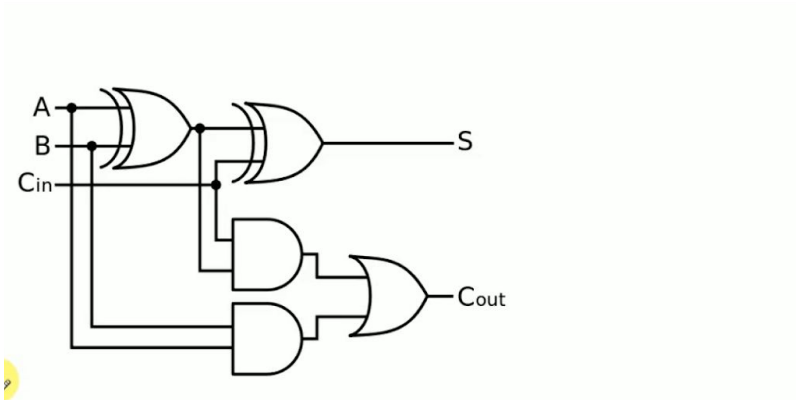
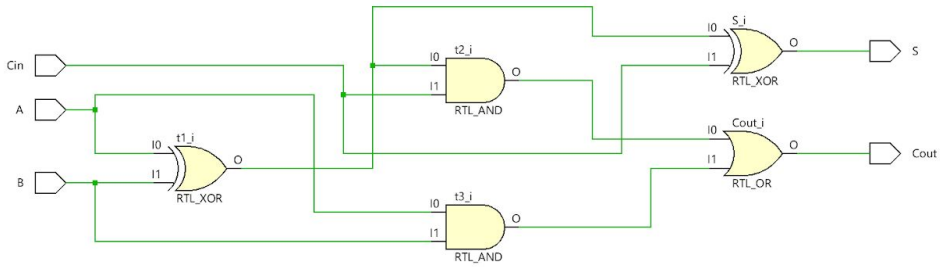
Modeling: data flow model
Schematic: (logic level diagram)



Input ports : A,B, Cin
Output ports : S, Cout
Nets **:** t1 (A xor B), t2 (t1 and Cin), t3 (b and a)
Waveforms :

RTL analysis Schematic:



Synthesis schematic: