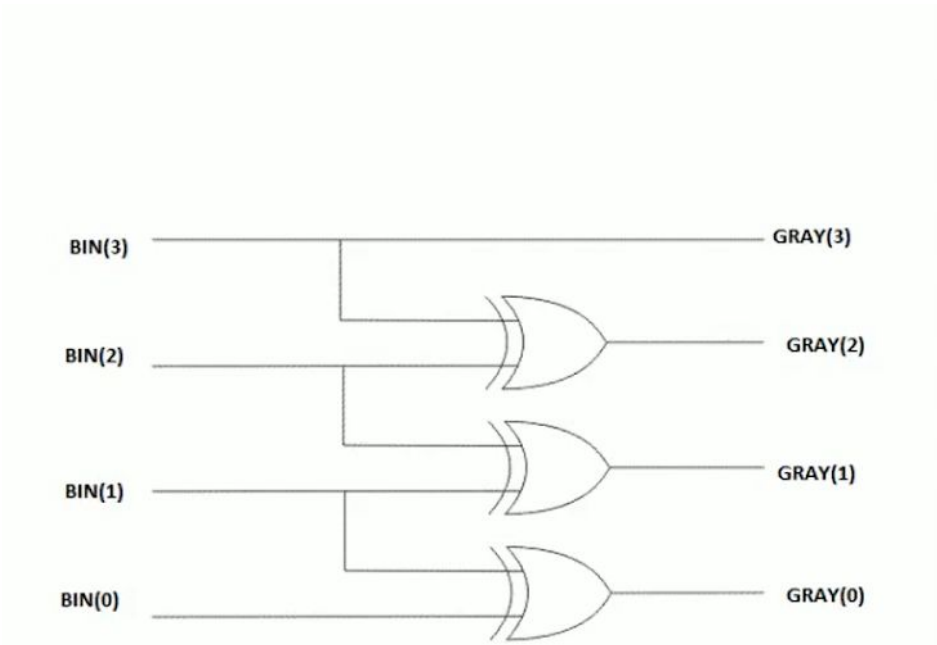
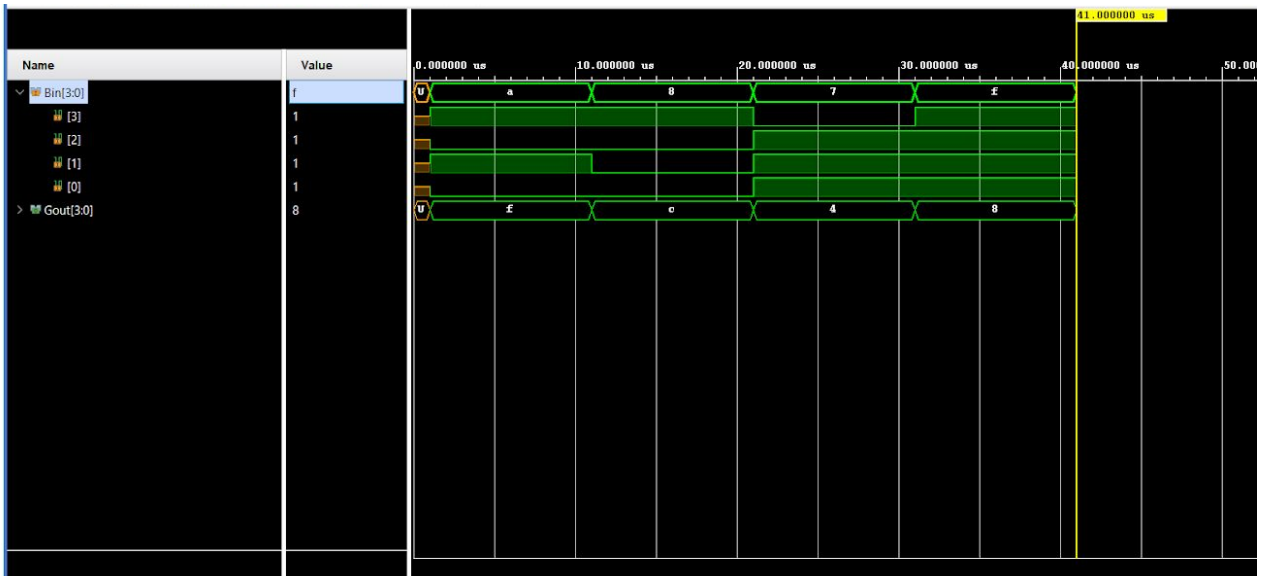
Binary to Gray RTL design

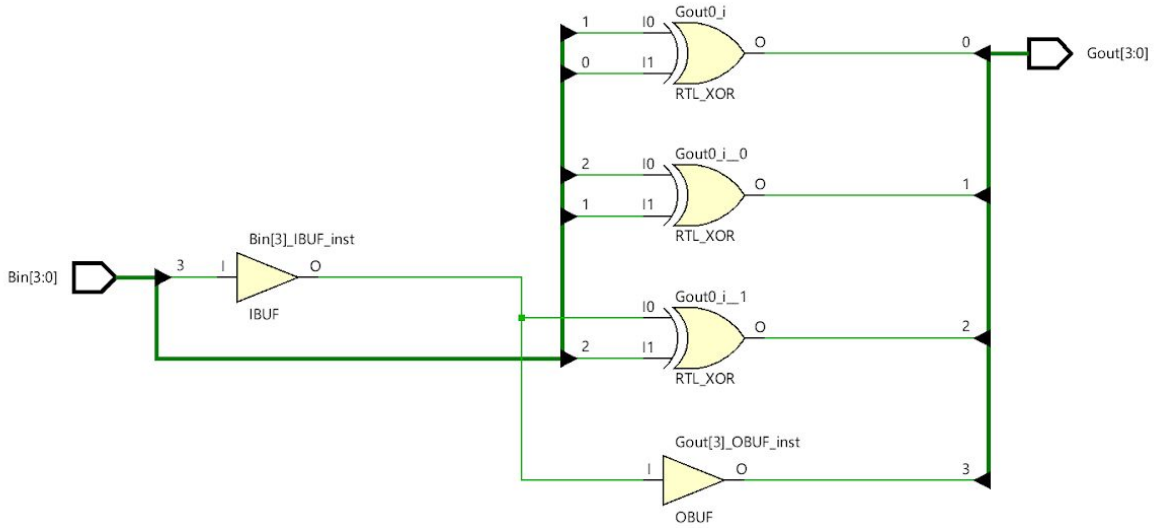
Modeling: data flow model
Schematic: (logic level diagram)



Input ports : Bin[3];
Output ports : Gray[3];
Nets **:** NA
Waveforms :



RTL analysis Schematic:



Synthesis schematic: