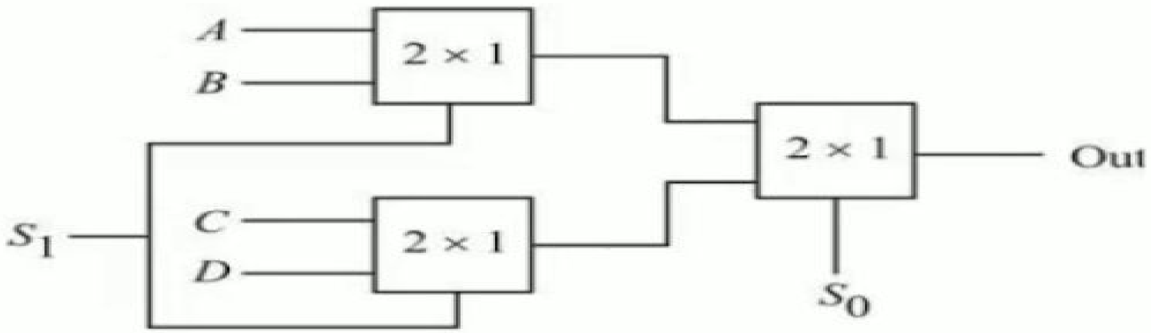
STRUCTURAL MODELLING
MUX 4 : 1 USING 2:1 MUX

RTL schematic :

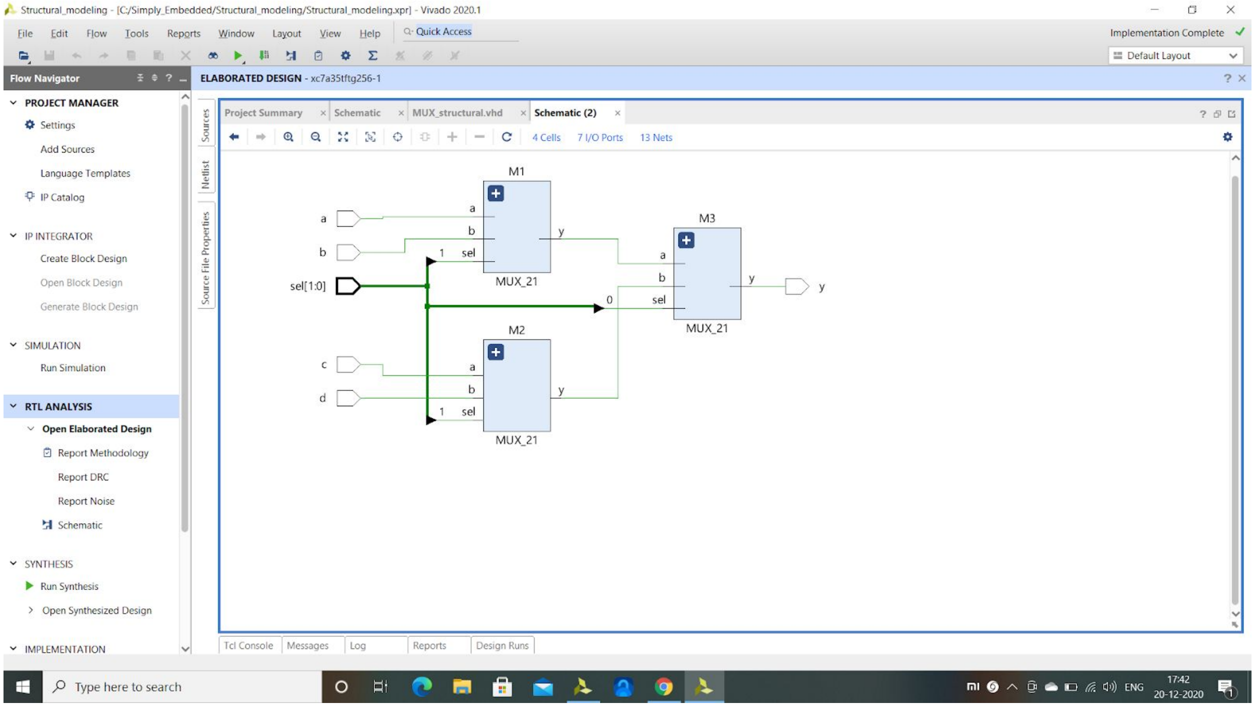


S_0	S_1	Out
0	0	A
0	1	B
1	0	C
1	1	D

Code:

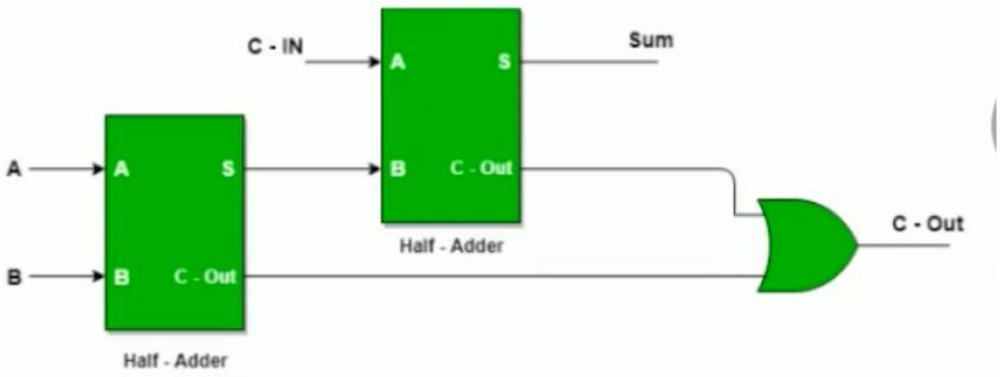
```
entity MUX_21 is
Port (
a,b,sel : in std_logic;
y       : out std_logic
 );
end MUX_21;

architecture Behavioral of MUX_21 is

begin
process
begin
if(sel = '1') then
  y <= a;
else
  y <= b;
end if;
end process;
end Behavioral;
---------------------------------------------------------------------------end---------------------------
-------------------------------------------------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity MUX_41 is
Port (
a,b,c,d : in std_logic;
sel     : in std_logic_vector ( 1 downto 0);
y       : out std_logic
 );
end MUX_41;

architecture Behavioral of MUX_41 is
component
MUX_21 is
Port (
a,b,sel : in std_logic;
y       : out std_logic
 );
end component;
signal t1: std_logic;
signal t2: std_logic;
begin
M1: MUX_21  port map(a=>a,b=>b,sel=>sel(1),y=>t1);
M2: MUX_21  port map(a=>c,b=>d,sel=>sel(1),y=>t2);
M3: MUX_21  port map(a=>t1,b=>t2,sel=>sel(0),y=>y);
end Behavioral;
```

RTL schematic:



FULL ADDER USING HALF ADDER

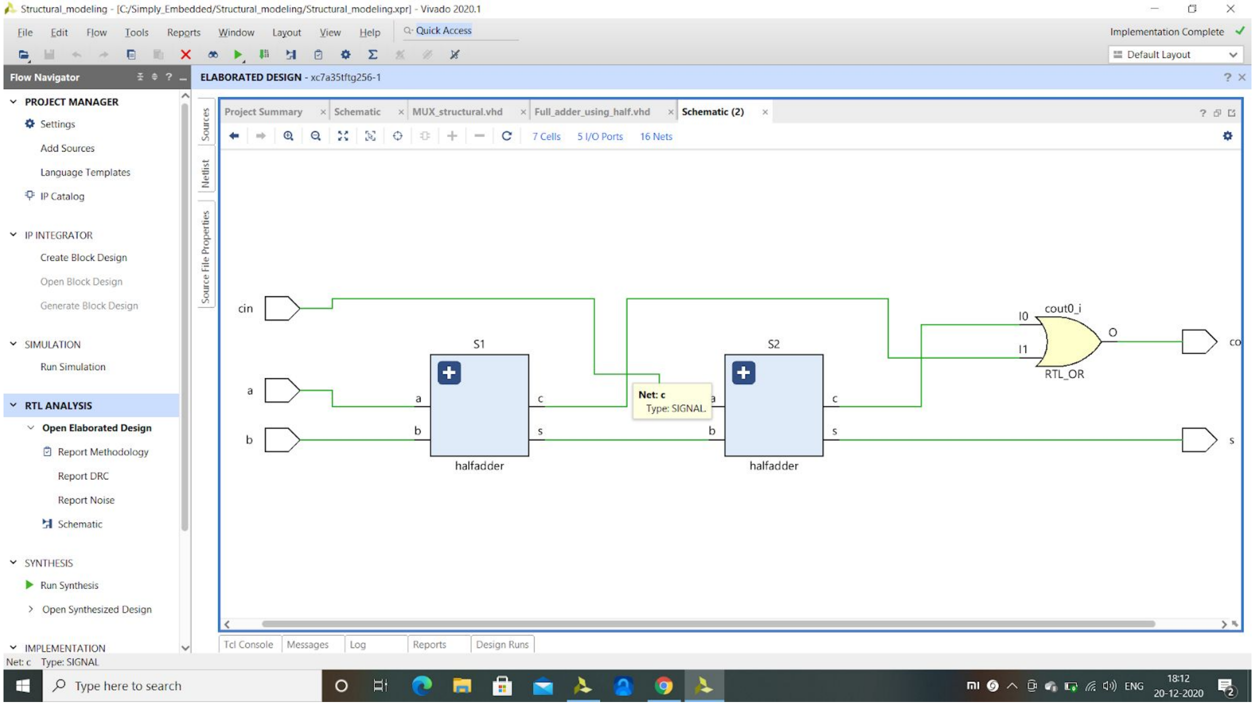
Schematic:



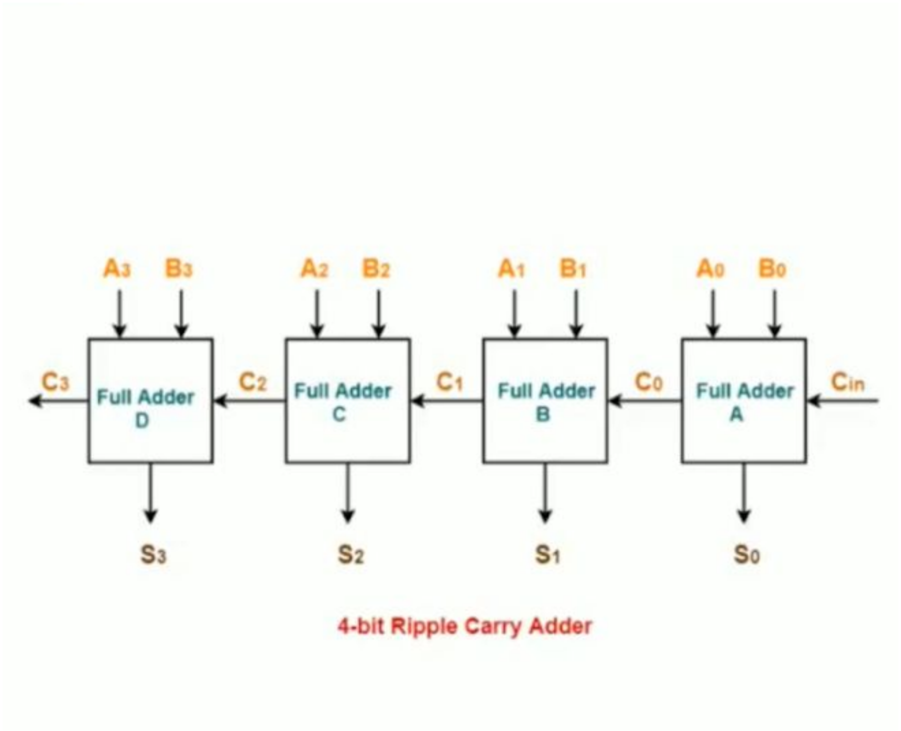
Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity halfadder is
Port (
a,b : in std_logic;
c,s : out std_logic

 );
end halfadder;

architecture Behavioral of halfadder is

begin
c <= a and b;
s <= a xor b;

end Behavioral;
-------------------
-----------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity fulladder is
Port (
a,b,cin : in std_logic;
cout,s    : out std_logic

 );
end fulladder;

architecture Behavioral of fulladder is
component halfadder is
Port (
a,b: in std_logic;
c,s : out std_logic

 );
end component;
signal t1 : std_logic;
signal t2 : std_logic;
signal t3 : std_logic;
begin
S1 : halfadder port map(a=>a,b=>b,c=>t3,s=>t1);
S2 : halfadder port map(a=>cin,b=>t1,c=>t2,s=>s);
cout <= t2 or t3;
cout <= t2 or t3;
end Behavioral;
```

RTL schematic:



Four bit adder Schematic:



4-bit Ripple Carry Adder

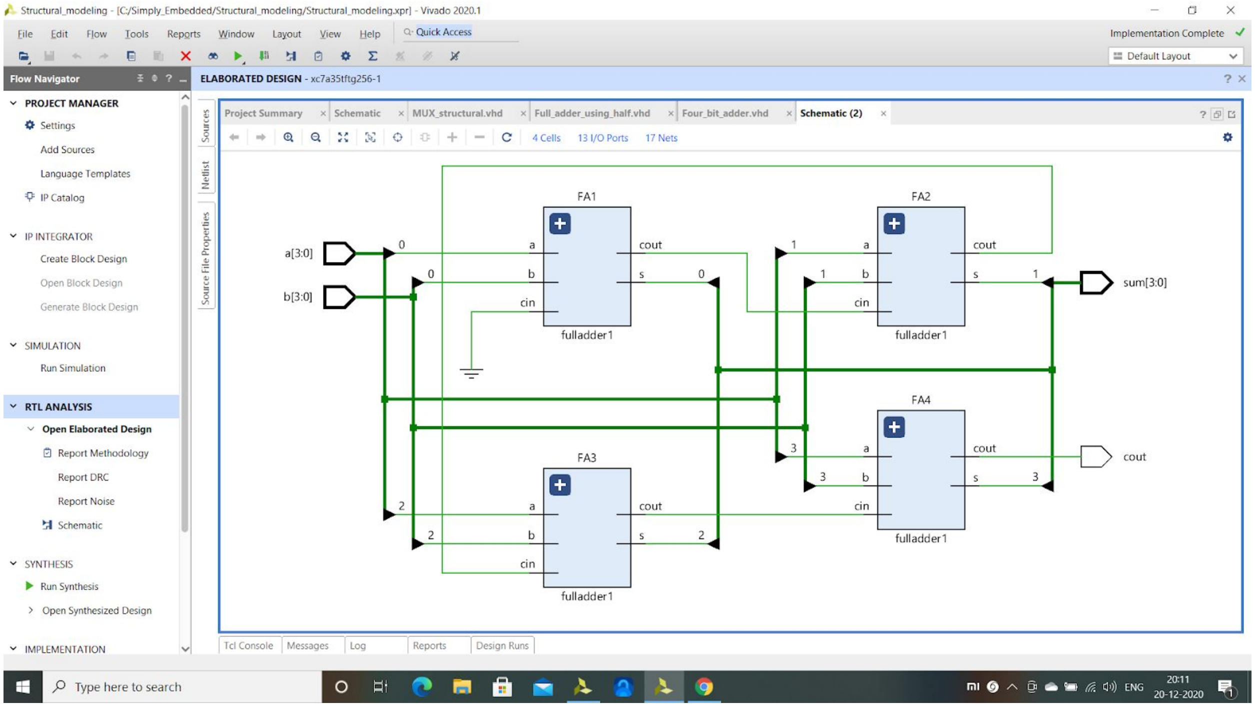
Code:

```
entity halfadder1 is
Port (
a,b : in std_logic;
c,s : out std_logic

 );
end halfadder1;

architecture Behavioral of halfadder1 is

begin
c <= a and b;
s <= a xor b;

end Behavioral;
-------------------
-----------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity fulladder1 is
Port (
a,b,cin : in std_logic;
cout,s    : out std_logic
```

```
 );
end fulladder1;

architecture Behavioral of fulladder1 is
component halfadder1 is
Port (
a,b: in std_logic;
c,s : out std_logic

 );
end component;
signal t1 : std_logic;
signal t2 : std_logic;
signal t3 : std_logic;
begin
S1 : halfadder1 port map(a=>a,b=>b,c=>t3,s=>t1);
S2 : halfadder1 port map(a=>cin,b=>t1,c=>t2,s=>s);
cout <= t2 or t3;
cout <= t2 or t3;
end Behavioral;
------------------------
-----------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity fourbitadder is
Port (
a,b : in std_logic_vector (3 downto 0);
sum    : out std_logic_vector (3 downto 0);
cout   : out std_logic

 );
end fourbitadder;

architecture Behavioral of fourbitadder is
component fulladder1 is
Port (
a,b,cin : in std_logic;
cout,s    : out std_logic

 );
end component;
signal cin,c0,c1,c2 : std_logic:='0';
begin
```

```
FA1 : fulladder1 port map(a=>a(0),b=>b(0),cin=>cin,cout=>c0,s=>sum(0));
FA2 : fulladder1 port map(a=>a(1),b=>b(1),cin=>c0,cout=>c1,s=>sum(1));
FA3 : fulladder1 port map(a=>a(2),b=>b(2),cin=>c1,cout=>c2,s=>sum(2));
FA4 : fulladder1 port map(a=>a(3),b=>b(3),cin=>c2,cout=>cout,s=>sum(3));

end Behavioral;
```

RTL schematic:


Structural_modeling - [C:/Simply_Embedded/Structural_modeling/Structural_modeling.xpr] - Vivado 2020.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete
Default Layout
Flow Navigator
ELABORATED DESIGN - xc7a35tftg256-1
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Sources
Netlist
Source File Properties
Project Summary
Schematic
MUX_structural.vhd
Full_adder_using_half.vhd
Four_bit_adder.vhd
Schematic (2)
4 Cells
13 I/O Ports
17 Nets
FA1
FA2
FA3
FA4
a[3:0]
b[3:0]
sum[3:0]
cout
a
b
cin
cout
s
fulladder1
0
1
2
3
Tcl Console
Messages
Log
Reports
Design Runs
Type here to search
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