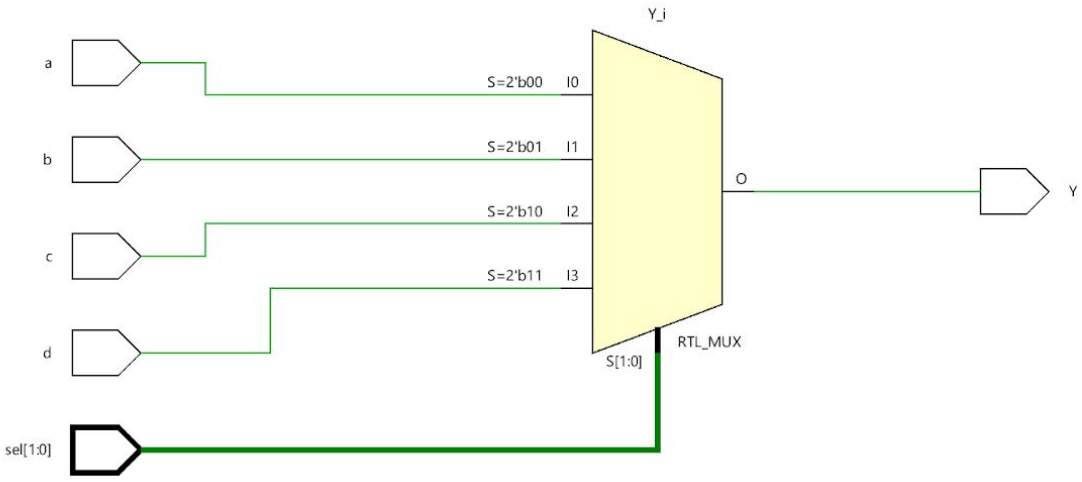
Conditional statement example
Selected Concurrent Statement

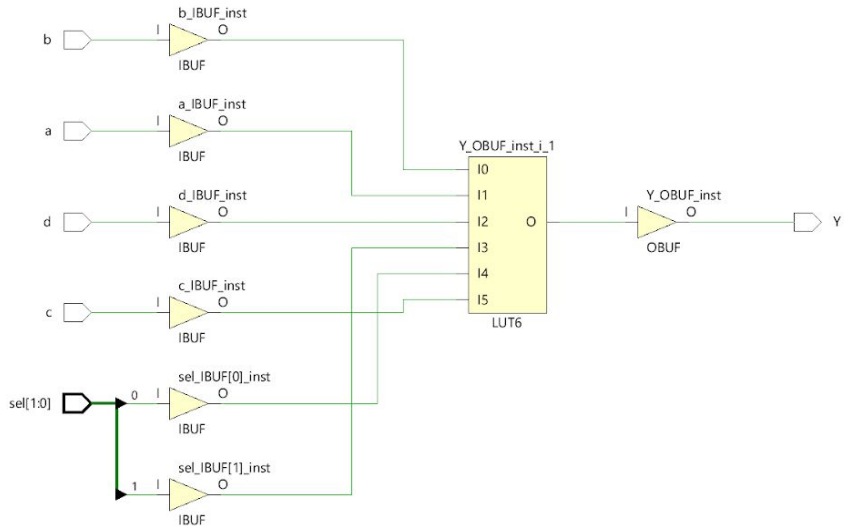
Modeling: Behavioural moeling
Entity : 4:1 mux;
Input ports : A,B,C,D. Sel
Output ports : Y
Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Selected is
Port (
a,b,c,d : in std_logic;
sel   : in bit_vector(1 downto 0);
Y     : out std_logic
);
end Selected;
architecture Behavioral of Selected is
begin
with sel select
Y <= a when "00",
     b when "01",
     c when "10",
     d when "11";
end Behavioral;
```

RTL analysis Schematic:



Synthesis schematic:



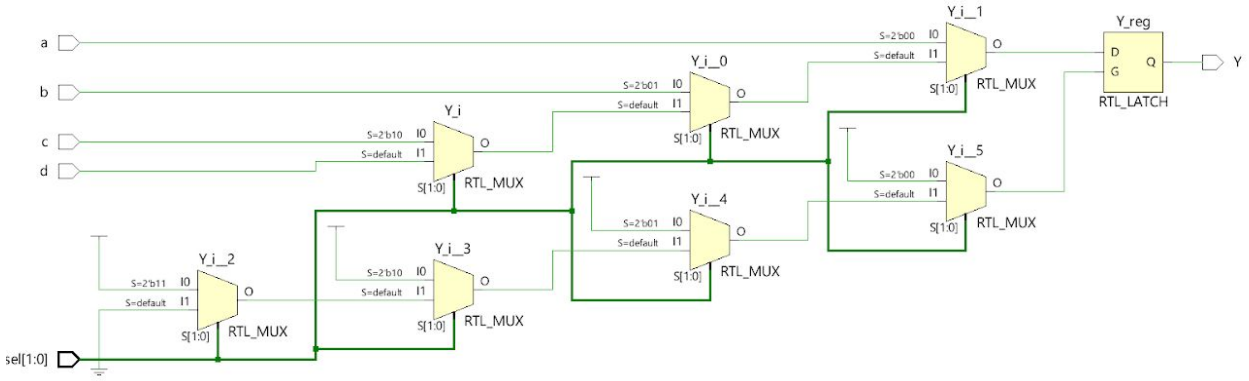
Conditional concurrent statement (with latch)

Modeling: Behavioural moeling
Entity : 3:1 mux;
Input ports : a,b,c,sel1,sel2
Output ports : Y
Waveforms :
Code:

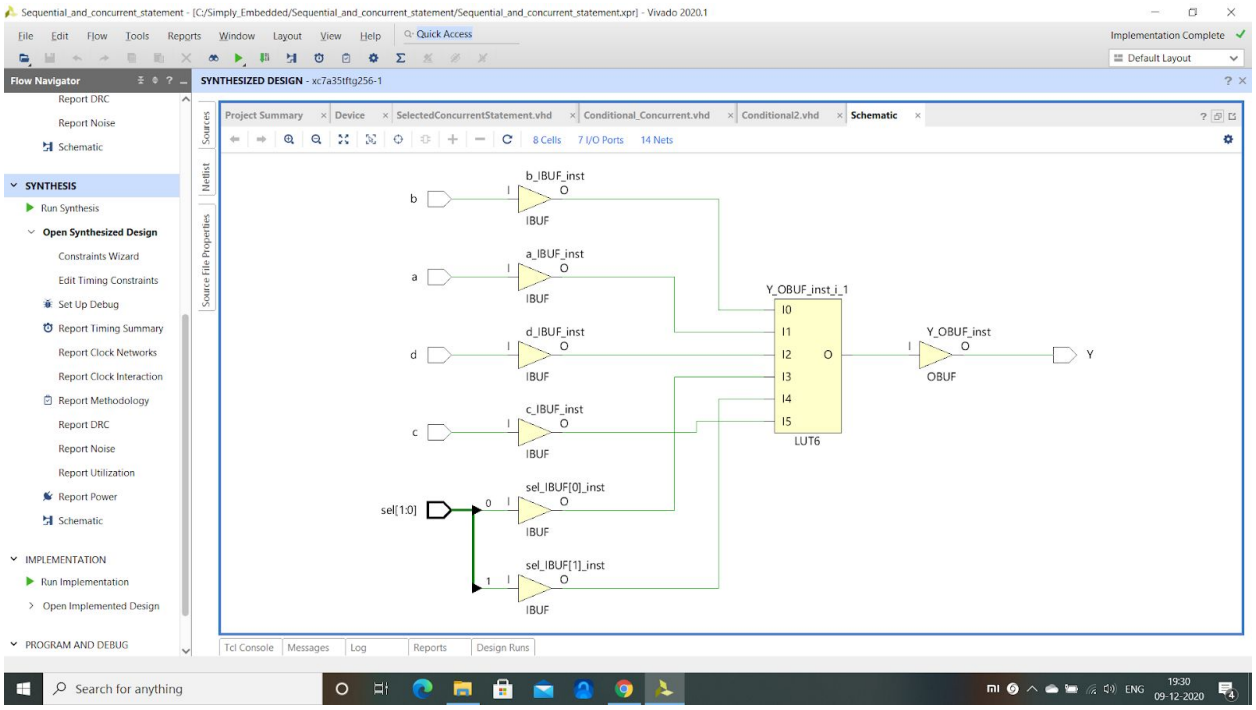
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Conditional2 is
Port (
a,b,c,d: in std_logic;
sel  : in std_logic_vector(1 downto 0);
Y        : out std_logic
 );
 end Conditional2;

architecture Behavioral of Conditional2 is

begin
Y <= a when sel = "00" else
     b when sel = "01" else
```

```
    c when sel = "10" else
    d when sel = "11";

end Behavioral;
```

RTL analysis Schematic:



Synthesis schematic:

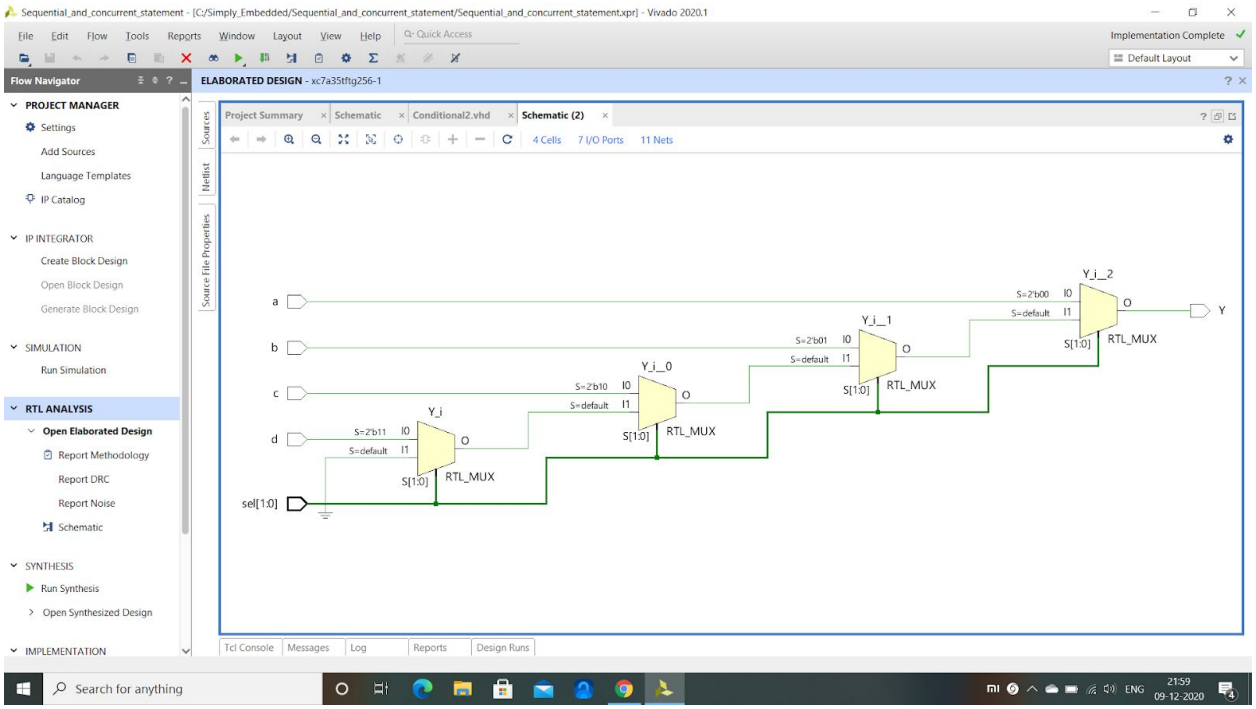


Conditional concurrent statement (without latch)

Modeling: Behavioural moeling
Entity : 3:1 mux;
Input ports : a,b,c,sel1,sel2
Output ports : Y
Code:

```
entity Conditional2 is
Port (
a,b,c,d: in std_logic;
sel  : in std_logic_vector(1 downto 0);
Y        : out std_logic
 );
 end Conditional2;

architecture Behavioral of Conditional2 is

begin
Y <= a when sel = "00" else
     b when sel = "01" else
     c when sel = "10" else
     d when sel = "11" else
     '0';

end Behavioral;
```

RTL analysis Schematic:



Note: formation of latch is undesirable a statement similar to ‘default’ was added to avoid latch formation

Synthesis schematic: