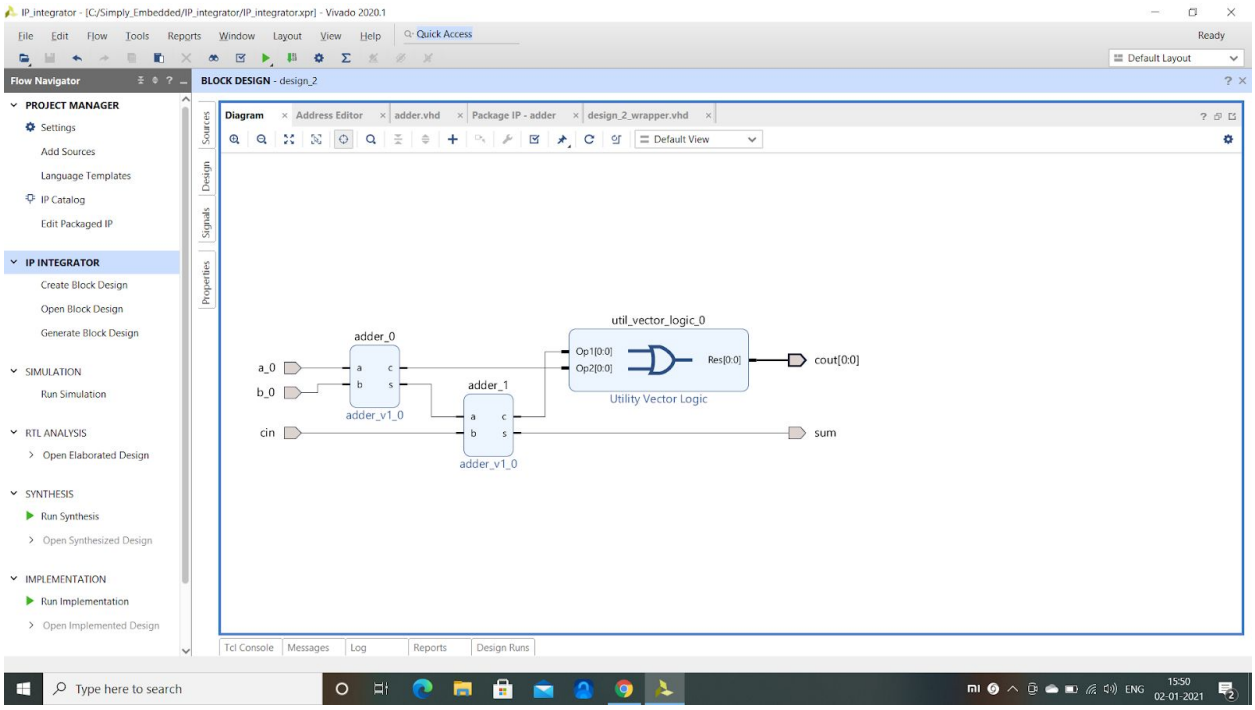
Design of Full adder using IP

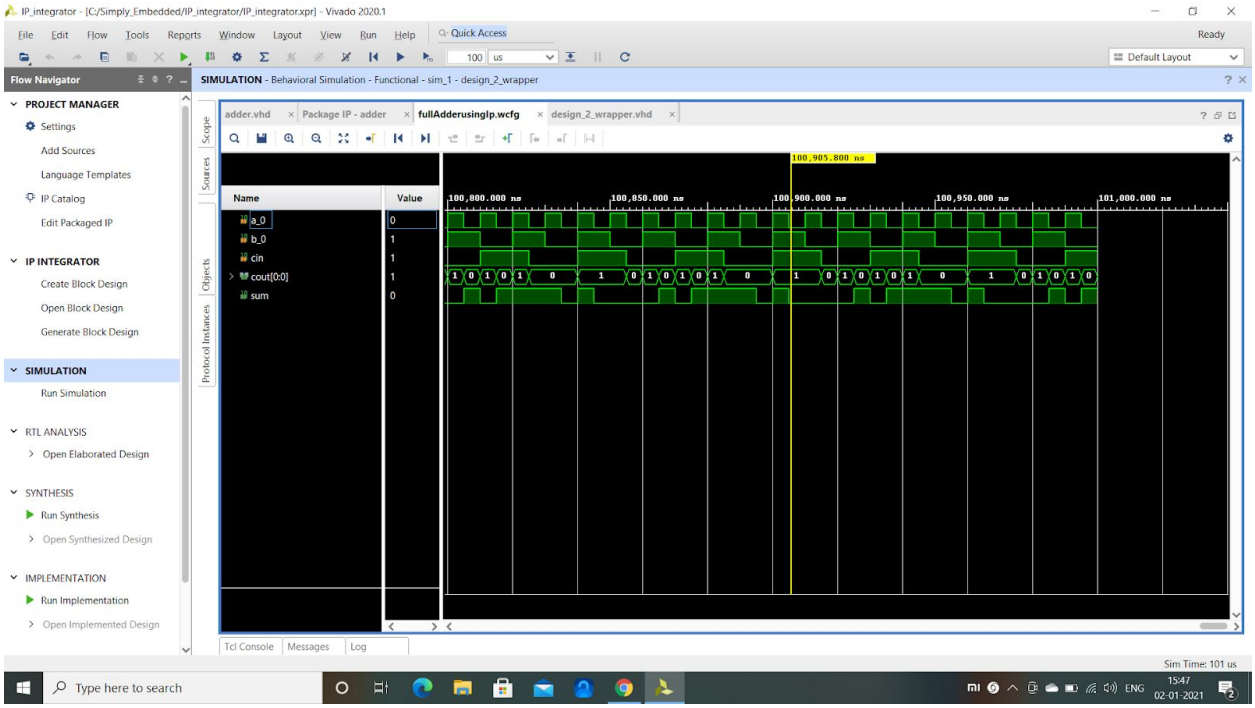
Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity adder is
    Port ( a,b : in STD_LOGIC;
           c,s : out STD_LOGIC);
end adder;

architecture Behavioral of adder is

begin

s <= a xor b;
c <= a and b;
end Behavioral;
```

Circuit (IP): Full adder using Half adder and vector logic ip



Waveform:


IP_integrator - [C:/Simply_Embedded/IP_integrator/IP_integrator.xpr] - Vivado 2020.1
File Edit Flow Tools Reports Window Layout View Run Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
Edit Packaged IP
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
SIMULATION - Behavioral Simulation - Functional - sim_1 - design_2_wrapper
adder.vhd
Package IP - adder
fullAdderusingIp.wcfg
design_2_wrapper.vhd
Scope
Sources
Objects
Protocol Instances
Name
Value
a_0
b_0
cin
cout[0:0]
sum
100,905.800 ns
100,800.000 ns
100,850.000 ns
100,900.000 ns
100,950.000 ns
101,000.000 ns
Tcl Console
Messages
Log
Sim Time: 101 us
Type here to search
ENG
15:47
02-01-2021