Gowin YunYuan Software

Release Note

RN100-1.9.2.02BetaE, 10/31/2019

Disclaimer

Contents

1 About This Release

The release contents of YunYuan software V1.9.2.02Beta are as follows:

- Devices supported: GW1NRF-4B, GW1NSR-4C;
- Update of the supported device: ES and production versions of GW1NS-2C/GW1NS-2/GW1NSE-2C/GW1NSR-2 are supported respectively;
- IP soft core updated: PCI Target, I3C HDR, Integer Multiply Divider, FFT;
- The constraint syntax of CLOCK_LOC supported, and non clock routing can be configured;
- Programmer supports the downloader of Digital HS2;
- Check the changes of the bitstream file and update the device list when Programmer is opened.

For the complete functions and enhancements of this release, please refer to 2 Function and Enhancement Summary.

Note!

Gowin Synthesis tool is required to support 32-bit system.

2 Function and Enhancement Summary

The table below summarizes the functions and enhancements.

Function	Description
YunYuan Software: V1.9.2.02Beta	
Functions	● Devices supported: GW1NRF-4B, GW1NSR-4C; ● The constraint syntax of CLOCK_LOC supported; ● Programmer supports the downloader of Digital HS2.
Enhancements	● Update of the supported device: ES and production versions of GW1NS-2C/GW1NS-2/GW1NSE-2C/GW1NSR-2 are supported respectively; ● IP soft core updated: PCI Target, I3C HDR, Integer Multiply Divider, FFT; ● Check the changes of the bitstream file and update the device list when Programmer is opened.

3 Platform Supported

The software is supported on the platforms listed below:

Windows	Windows 7/8/10(32bit/64 bit) Windows XP/7（32bit）
Linux	Centos6.8/7.0/7.5(64 bit) Ubuntu 18.04 LTS

4 Ports

Port No.	Port Type	Port Description
36545	User-defined protocol port	Used to communicate with JTAG SERVER for the GAO (Gowin Analyzer Oscilloscope) display.
36546	User-defined protocol port	Used to communicate with JTAG SERVER for the GAO (Gowin Analyzer Oscilloscope) display.
10559	User-defined protocol port	The license server port of the Gowin software back-end tool.
27020	TCP port	The license server port of the Gowin software front end tool “synplifyPro”.

5 Environment Variables Setting

LM_LICENSE_FILE Environment Variables Setting

1. Node-Locked license variable value: The license files location, such as: "D:\Synopsys\license.txt";
2. Floating license variable value: license files location, such as: 27020@192.168.31.220. “192.168.31.220” is the IP address of starting the floating license.

6 Document

The released software manuals are listed in the table below. You can download the PDF manuals and/or read them at the Gowin website.

Document	Usage
SUG100-2.0E_Gowin YunYuan Software User Guide.pdf	PDF
SUG101-1.8E_Gowin Design Constraints Guide.pdf	PDF
SUG114-1.9E_Gowin Analyzer Oscilloscope User Guide.pdf	PDF
SUG282-1.7E_Gowin Power Analyzer User Guide.pdf	PDF
SUG283-1.9E_Gowin Primitive User Guide.pdf	PDF
SUG284-1.8E_Gowin IP Core Generator User Guide.pdf	PDF

7 Known Issues

The following issues will be fixed in the next version.

1. It is not available to generate IP soft core using the GAO and IP Core in a 32-bit system for the time being;
2. Hierarchy display function does not support VHDL design analysis. When VHDL design is added, ERROR information will be reported in IDE output window, but it does not affect synthesis by synplifyPro.
   ERROR: Hierarch cannot support VHDL;
3. GowinSynthesis does not support VHDL design synthesis. When synthesis contains VHDL design, ERROR information will be reported in IDE output window. Please use synplifyPro to synthesise.
   Error (EXT3044): Analyze: cannot read format VHDL in this product
   Error (EXT0304): Fail to analyze the input design file;
4. Try to reduce the number of capture signals and capture depth if there are any problems with the GAO capturing. If the problem still exists, please contact GOWINSEMI technical support;
5. For DSP RTL design synthesis, the synthesis tool does not support the followings. If there are synthesis problems, please contact GOWINSEMI technical support;
   - ALU54D does not support ACCLOAD_REG mapping in the asynchronous mode;
   - The MULTALU36X18/MULTADDALU18X18 outputs may not be synthesized to mode 2 when passing through registers.


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