Gowin FPGA Products Slave SPI Configuration Manual

Slave SPI Configuration Mode

Before start, please refer to the section of SSPI, UG290, Gowin FPGA Products Pragramming Configuration Manual.

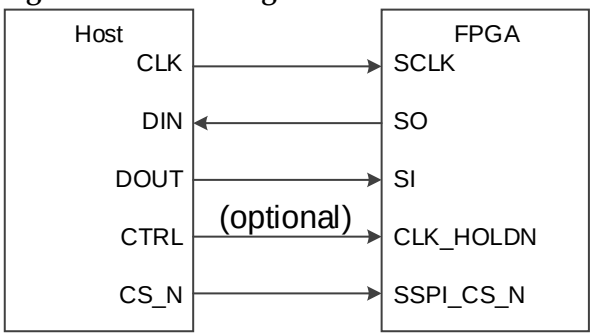
In the slave SPI mode, FPGA is as the attached device. The Gowin FPGA products are configured by the external Host via SPI.

Table 1 SSPI Mode Pins

Pin Name	I/O	Description
RECONFIG_N	I, internal weak pull-up	Low level pulse: Clear SRAM and Start GowinCONFIG from external and internal storage configuration **Note!** Programming in hang and high level.
READY	O	High level: The device can currently be programmed and configured. Low level: Programming configuration for the device is prohibited. **Note!** Programming in hang and high level.
DONE	O	High level: Device successfully programmed and configured. Low level: Programming or configuration failed. **Note!** Programming in hang and high level.
MODE[2:0]	I, internal weak pull-up	MODE=001 refers to SSPI configuration mode, READY rising edge sampling.
SCLK	I	Input clock.
CLKHOLD_N	I, internal weak pull-up	High level: SPI operation corresponding to SCLK is valid. Low level: SPI operation corresponding to SCLK is invalid.
SO	O	Output data.
SI	I	Input data.
SSPI_CS_N	I, internal weak pull-up	Enable signal, active level.

The connection diagram for configuring the GW1N series of FPGA products via SSPI is shown in Figure 1.

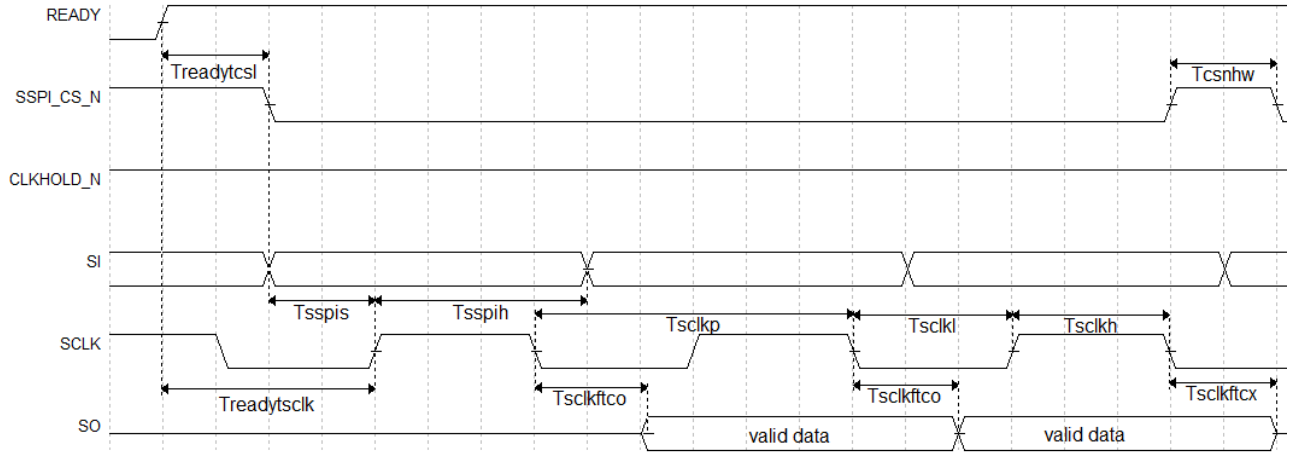
Figure 1: SSPI Configuration Mode Connection Diagram



Note!

Figure 1 shows the minimum system diagram of the SSPI MODE. The value of the SSPI MODE is "001".

Figure 2: SSPI Configuration Timing



Note!

Data input please confirm to MSB (Most Significant Bit First).

Table 2: SSPI Configuration Timing Parameters

Name	Description	Min.	Max.
T_{sclkp}	SCLK clock period	15 ns	-
T_{sclkh}	SCLK clock high time	7.5 ns	-
T_{sclkl}	SCLK clock low time	7.5 ns	-
T_{sspis}	SSPI PORT setup time	2 ns	-
T_{sspih}	SSPI PORT hold time	0 ns	-
$T_{sclkftco}$	Time from SCLK falling edge to output	-	10 ns
$T_{sclkftcx}$	Time from SCLK falling edge to high impedance	-	10 ns
T_{csnhw}	CSN high time	25 ns	-
$T_{readytcsl}$	Time from READY rising edge to CSN low	TBD	
$T_{readytsclk}$	Time from READY rising edge to first SCLK edge	TBD	-

Note!

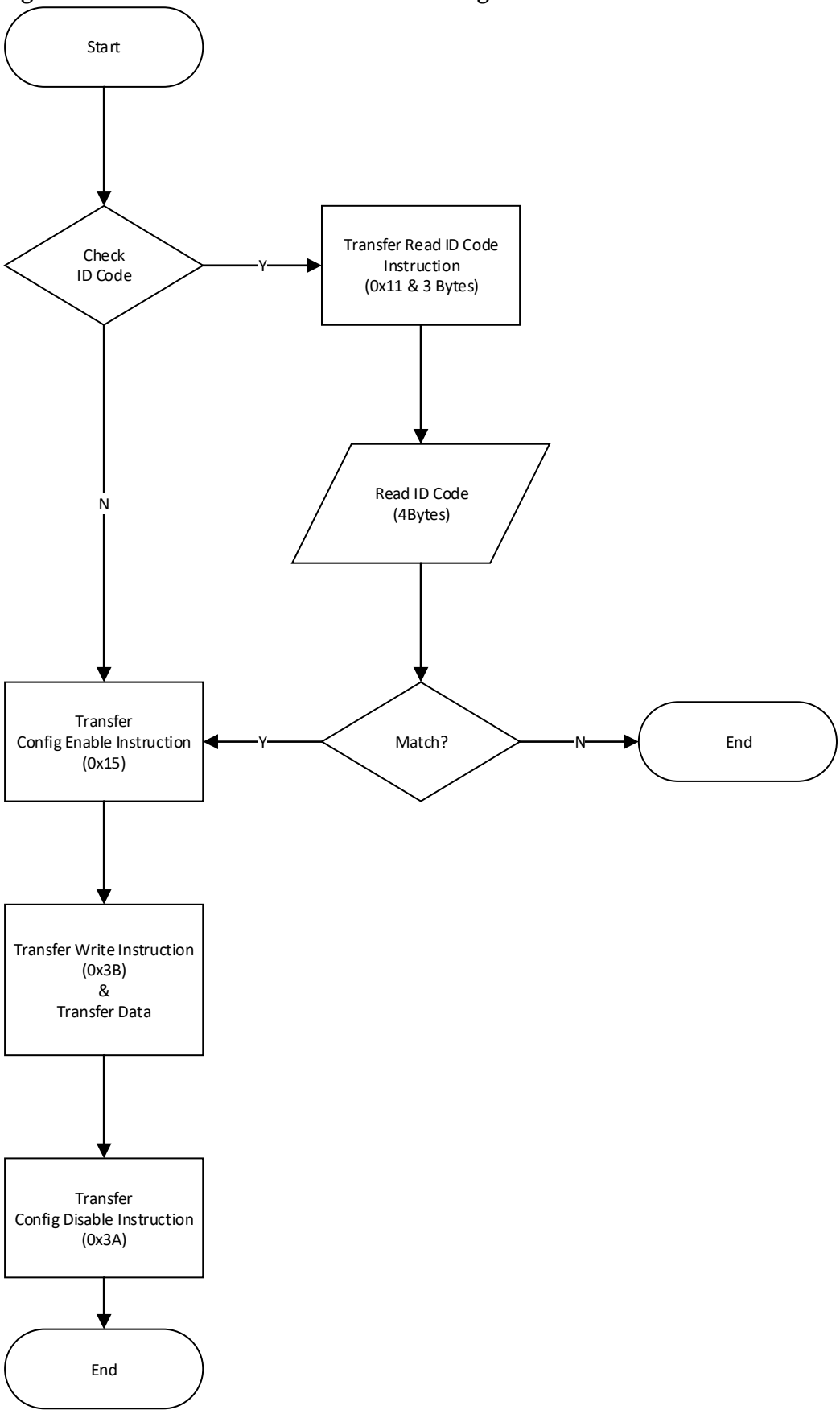
Other than the power requirements, the following conditions need to be met to use the SSPI configuration mode:

- Enable SSPI port.
- Set RECONFIG_N as “NON-RECOVERY”.
- Initiate new program.
- Power-on again or provide one low pulse on programming pin RECONFIG_N.

Configuration Process

In Slave SPI mode, only the SRAM can be configured via SPI or by reading the ID information on ID CODE\USER CODE\STATUS CODE in the SRAM. Flash or external memory devices cannot be configured.

Figure 3: Process Schematic for the SSPI Configuration FPGA SRAM



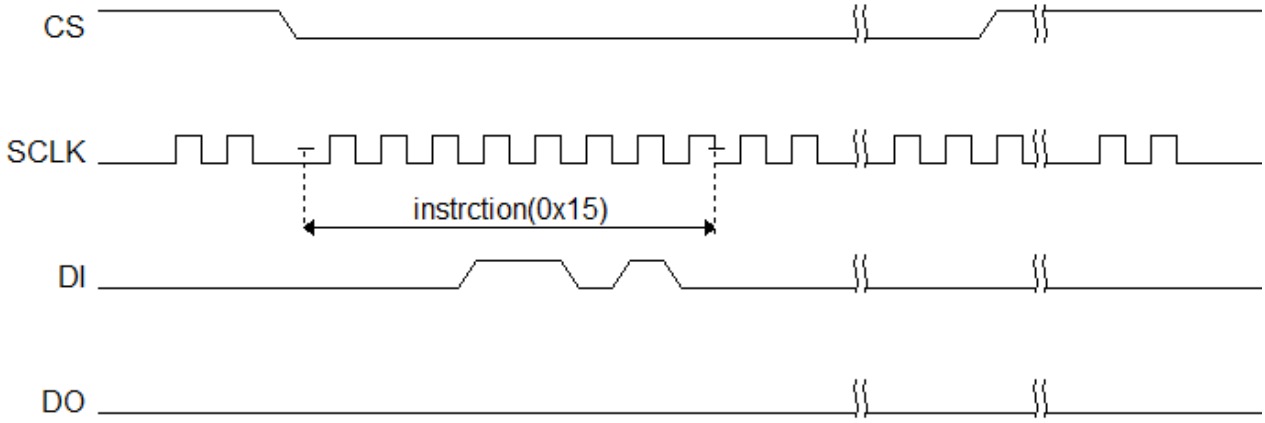
Instruction and Timing

An instruction includes four bytes, which consist of one instruction byte and three information bytes. If no information byte is specified, the information byte may be replaced by 0x0 or 0xFF.

Config Enable (0x15)

Before configuring the SRAM (write features), enter the programe mode using the Write Enable (0x15) instruction to receive write data WriteData (0x3B) instructions.

Figure 4: Write Enable (0x15) Timing



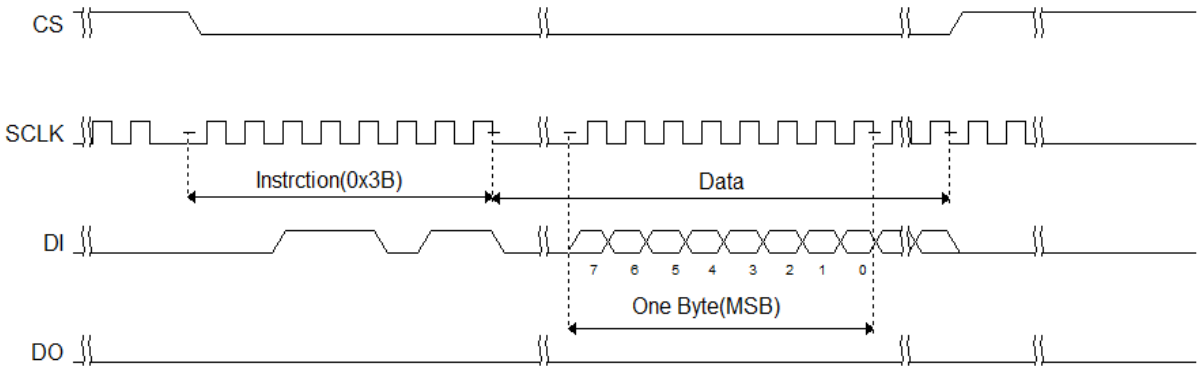
Note!

SCLK dirve rule. In CS high level, more than two clocks are needed to give SCLK to dirive FPGA to recognize CS signal. Sending other instructions also confirm to this rule.

Write Data (0x3B)

The fs file is sent directly to the FPGA device following the WriteData(0x3B) instruction.

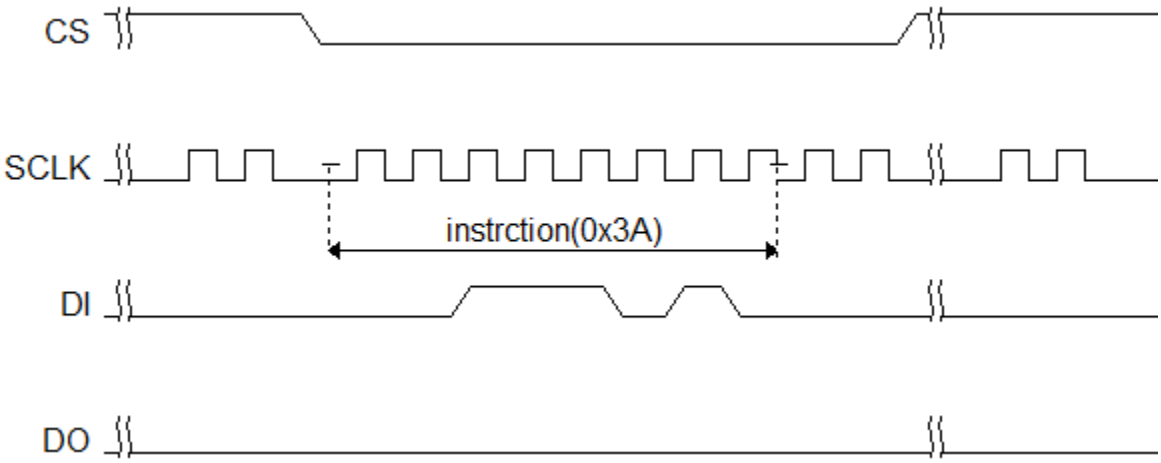
Figure 5: Write Enable (0x3B) Timing



Config Disable (0x3A)

After sending the data, exit the program mode using Write Disable. After exiting, the device can be awakened to start working.

Figure 6: Config Disable (0x3A) Timing



Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

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Revision History

Date	Version	Description
04/14/2017	1.0E	Initial version published.
12/06/2017	1.1E	Process schematic of SSPI configuration FPGA SRAM updated and instruction information added.
10/10/2018	1.2E	Description of CS and instruction added.

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