Gowin YunYuan Software

Release Note

RN100-1.9.1Beta, 5/27/2019

Disclaimer

Revision History

Date	Version	Description
2/8/2018	1.0E	● Initial version 1.8.0Beta1released; ● The GAO optimized ; ● The simplified version GAO added; ● IP supported by IP Core Generator; ● Known issues updated; ● GW1N-2 / GW1N-4 PBGA256M package supported; ● GW1N-6/GW1N-9 WLCSP64 package supported; ● The synthesis of initial reg values supported by SynplifyPro .
4/20/2018	1.1E	● Software Version 1.8.0Beta released; ● TCK pins multiplexing supported; ● External SDRAM of SDRAM controller supported; ● When IP Core Generator generates I3C IP, support click "Cancel > OK"; ● Tabs in BSRAM initialization files supported by IP Core Generator; ● The OSC clock used as a default analysis clock supporting the timing analyzing; ● IDES16 and OSER16 supported by GW1N-6/GW1N-9/GW1NR-9 ; ● Jtagserver to support Korean Operating System in GAO upgraded; ● The value range of GPA VCC/VCCX updated; ● Programmer optimized and the known issues updated.
5/18/2018	1.2E	● Software Version 1.8.0.01Beta released; ● IP Core Generator, MIPI RX supporting 1:16, MIPI TX supporting 16:1; ● The I/O error count in SDRAM Controller updated when the SDRAM Controller is used; ● When IP Core Generator generates MIPI TX and configures LP mode on data lane 0~3, the problem that only LP data0 is generated is fixed; ● The value range of GPA VCCX updated.
6/1/2018	1.3E	● Software Version 1.8.0.02Beta released; ● MODE pin multiplexing supported; ● The devices GW1N-4B/GW1NR-4B supporting background programming functions added.
8/29/2018	1.4E	● Software Version 1.8.1Beta released; ● Products: GW1NS-2C, GW1NS-2 supported; ● Packages: GW1NR-LV4MG81, GW2A-18-PBGA256, GW2A-18-MBGA196, GW1N-9-UBGA256, GW1N-6-UBGA256, and GW2A-18-QFN88 supported; ● IP: FFT, 1:2 DDR3, 1:4 DDR3, pSRAM, Cordic, Complex Multiplier, Divide, and I3C DDR eXtension supported; ● Part number selection on the software interface supported; ● The output of .csv and .vcd files on the GAO interface supported; ● GW1N-9 supporting background programming; ● The mi files of Address-hex format on the memory interface of BSRAM supported; ● The Gowin programmer supporting MCU bin files; ● Open the project with IDE automatically when double-click on the gprj file.
9/18/2018	1.4.1E	● Software Version 1.8.1.01Beta released;

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		● The ID CODE issue in 4K version B updated; ● The issue that the FPGA stops working after the programmer switches to MCU JTAG; ● The environment variable GOWIN_HOME removed, the issue of stuck installation solved, and multiple versions can be installed at the same time.
10/22/2018	1.5E	● Software Version 1.8.2Beta released; ● Products: GW1NZ-1, GW1NSR-2C supported; ● Part Number list updated; ● MIPI BUF supported; ● The software output report file format unified; ● Gowin Programmer supports SRAM data readback, the BSRAM added by default.
11/23/2018	1.6E	● Software Version 1.8.3Beta released; ● Products: GW1NSR-2C, GW1NSR-2 supported; ● GW1N-6ES, GW1N-9ES and GW1NR-9ES devices removed; ● Part Number list updated; ● pSRAM and Gowin_EMPU supported; ● The I/O properties of the GW1NZ-1 updated; ● The INPUT of the GW1N-4, GW1N-4B, GW1NR-4, and GW1NR-4B supporting the OVERDRIVE/UNDERDRIVE MODE.
1/10/2019	1.7E	● Software Version 1.8.4Beta released; ● New IPs supported: RISCV N25 and CAN; ● IP functions updated: Gowin_EMPU, MIPI, PSRAM, and DDRx; ● IP classification updated; Complex Multiplier, CORDIC, and DIVIDER; ● Known issues fixed.
1/25/2019	1.701E	● Software Version 1.8.4.01Beta released; ● GW2A-18 devices input buf to connect multiple input iologic supported; ● IP Core RISCV N25 default Setting updated;
2/21/2019	1.8E	● Software Version 1.9.0Beta released; ● GowinSynthesis, an integrated tool independently developed by Gowin supported; ● The display waveform interface of the GAO optimized. ● IP: FDAF, BASIC FIR Filter, Triple Speed Ethernet MAC XCORR, NLMSAF and Integer Multiply-Divider supported； ● 32 bit system supported; ● Known issues fixed.
3/27/2019	1.801E	● Software Version 1.9.0.01Beta released; ● IP: PSRAM Memory Interface, DDR3 Memory Interface and MIPI updated; ● IP: Advanced FIR Filter and PSRAM Memory Interface 2CH released; ● GW1N-9/GW1NR-9 bi-directional MIPI_IBUF dynamic configuration resistor supported; ● New packages: GW1N-9-EQ144 and GW2AR-18-EQ176 supported; ● Kown issues fixed.
5/5/2019	1.802E	● Software Version 1.9.0.02Beta released; ● IP soft core Gowin_EMPU_M1 released; ● IP hard core Gowin_EMPU updated; ● IP soft core DDR, DDR2 updated; ● New package GW2A-18-PBGA256C supported; ● The timing fuse setting of GW2A-18/GW2AR-18 BSRAM A and

Date	Version	Description
		B ports working at the same time optimized; ● Input IO of all devices to connect multiple input iologic functions supported ● Programmer fixing Spi Program in Bscan Failed issues; ● MCU mode, MCU programming and AC.bin programming added on programmer interface; ● --run 22 (programming mcu firmware) operation closed and mcu 27, 28 and 29 operations added by programmer_cli; ● programmer_cli adding -o/--output parameters to output redirect.
5/27/2019	1.9E	● Software Version 1.9.1Beta released; ● New device supported: GW1N-1S, FN32; ● New packages supported: GW1N-9-MG196, GW1NR-9-MG100, GW2A-18-EQ144; ● Speeds supported: GW2A-55/GW2A-18-PG484-A6, C9, GW1N-9-MG160-C7; ● PN of GW2A-UV devices deleted; ● BandGap supported in GW1NZ-1 to reduce power dissipation further; ● IDE supports the output message redirect. Users can press F1 to redirect and find the message content; ● GAO and Programmer added on the tool bar; ● Stop function supported during IDE running; ● Recovering the previous running state supported when a project is reopened using IDE; ● The IDE interface supports hierarchy display and set top module functions for project designs; ● GAO is supported on a Linux system; ● GAO supports to sort trigger signals and sampling signals by dragging and dropping; ● “Value” in the “Match Unit” configuration view of GAO supports decimal numbers; ● GAO wave display interface supports full screen and the “Ctrl+F” shortcut; ● IP core supports the generation of SSRAM module hard core; ● New IP released: HyperRAM memory Interface; ● IP RAM based shift register supports to generate testbench automatically; ● Comments added for the bitstream binary files, with a .binx suffix; ● Known issues fixed.

Contents

1 About This Release

The main release contents of YunYuan software V1.9.1Beta are as follows:

- New device supported: GW1N-1S, FN32;
- New packages supported: GW1N-9-MG196, GW1NR-9-MG100, GW2A-18-EQ144;
- Speeds supported: GW2A-55/GW2A-18-PG484-A6, C9, GW1N-9-MG160-C7;
- PN of GW2A-UV devices deleted;
- BandGap supported in GW1NZ-1 to reduce power dissipation further;
- IDE supports the output message redirect. Users can press F1 to redirect and find the message content;
- GAO and Programmer added on the tool bar;
- Stop function supported during IDE running;
- Recovering the previous running state supported when a project is reopened using IDE;
- The IDE interface supports hierarchy display and set top module functions for project designs;
- GAO is supported on a Linux system;
- GAO supports to sort trigger signals and sampling signals by dragging and dropping;
- “Value” in the “Match Unit” configuration view of GAO supports decimal numbers;
- GAO wave display interface supports full screen and the “Ctrl+F” shortcut;
- IP core supports the generation of SSRAM module hard core;
- New IP released: HyperRAM memory Interface;
- IP RAM based shift register supports to generate testbench automatically;
- Comments added for the bitstream binary files, with a .binx suffix.

For the complete functions and enhancements of this release, please refer to 2Function and Enhancement Summary.

Note!

Gowin Synthesis tool is required to support 32-bit system.

2Function and Enhancement Summary

The following table summarizes the functions and enhancements:

Function	Description
Place and routing tool: V1.9.0.02Beta	
Functions	● New device supported: GW1N-1S, FN32; ● New packages supported: GW1N-9-MG196, GW1NR-9-MG100, GW2A-18-EQ144; ● Speeds supported: GW2A-55/GW2A-18-PG484-A6, C9, GW1N-9-MG160-C7; ● IP core supports the generation of SSRAM module hard core; ● New IP released: HyperRAM memory Interface; ● IP RAM based shift register supports to generate testbench automatically; ● Comments added for the bitstream binary files, with a .binx suffix.
Enhancements	● PN of GW2A-UV devices deleted; ● BandGap supported in GW1NZ-1 to reduce power dissipation further; ● IDE supports the output message redirect. Users can press F1 to redirect and find the message content; ● GAO and Programmer added on the tool bar; ● Stop function supported during IDE running; ● Recovering the previous running state supported when a project is reopened using IDE; ● The IDE interface supports hierarchy display and set top module functions for project designs; ● GAO is supported on a Linux system; ● GAO supports to sort trigger signals and sampling signals by dragging and dropping; ● “Value” in the “Match Unit” configuration view of GAO supports decimal numbers; ● GAO wave display interface supports full screen and the “Ctrl+F” shortcut;

3 Platform Supported

The software is supported on the platforms listed below:

Windows	Windows 7/8/10(64 bit) , Windows XP/7（32bit）
Linux	Centos6.8/7.0/7.5(64 bit)

4 Ports

Port No.	Port Type	Port Description
36545	User-defined protocol port	Used to communicate with JTAG SERVER for the GAO (Gowin Analyzer Oscilloscope) display.
36546	User-defined protocol port	Used to communicate with JTAG SERVER for the GAO (Gowin Analyzer Oscilloscope) display.
10559	User-defined protocol port	The license server port of the Gowin software back-end tool.
27020	TCP port	The license server port of the Gowin software front end tool “synplifyPro”.

5 Environment Variables Setting

LM_LICENSE_FILE Environment Variables Setting

1. Node-Locked license variable value: The license files location, such as: "D:\Synopsys\license.txt";
2. Floating license variable value: license files location, such as: 27020@192.168.31.220. “192.168.31.220” is the IP address of starting the floating license.

6 Document

The released software manuals are listed in the table below. You can download the PDF manuals and/or read them at the Gowin website.

Document	Usage
SUG100-1.7_Gowin YunYuan Software User Guide.pdf	PDF
SUG101-1.7_Gowin Design Constraints Guide.pdf	PDF
SUG114-1.8_Gowin Analyzer Oscilloscope User Guide.pdf	PDF
SUG282-1.7_Gowin Power Analyzer User Guide.pdf	PDF
SUG283-1.8_Gowin Primitive User Guide.pdf	PDF
SUG284-1.8_Gowin IP Core Generator User Guide.pdf	PDF

7 Known Issues

The following issues will be fixed in the next version.

1. It is not available to generate IP soft core using the GAO and IP Core in a 32-bit system for the time being;
2. Try to reduce the number of capture signals and capture depth if there are any problems with the GAO capturing. If the problem still exists, please contact GOWINSEMI technical support;
3. Hierarchy display function does not support VHDL design systhesis. When VHDL design is added, ERROR information will be reported in the IDE output window, but it does not affect synplifyPro to synthesize. ERROR: analyze: cannot read format VHDL in this product;
4. GowinSynthesis does not support VHDL design synthesis. When synthesis contains VHDL design, the IDE output window will report the following Error information.
   Error (EXT3044) : Analyze: cannot read format VHDL in this product
   Error (EXT0304) : Fail to analyze the input design file;
5. For DSP rtl design synthesis, the synthesis tool does not support the followings. If the synthesis problem exists, please contact GOWINSEMI technical support;
   - ALU54D does not support ACCLOAD_REG mapping in the asynchronous mode;
   - The MULTALU36X18/MULTADDALU18X18 outputs may not be synthesized into mode 2 when passing through registers.
6. For the BSRAM usage notes, please refer to *Gowin B-SRAM User Guide* at GOWINSEMI website.


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