Gowin YunYuan Software

Release Note

RN100-2.0E, 08/21/2019

Disclaimer

Revision History

Date	Version	Description
08/21/2019	2.0E	Initial version published.

Contents

1 About This Release

The release contents of YunYuan software V1.9.2Beta are as follows:

- Package supported: GW2A-18-UG324;
- Devices supported: GW1N-4S, GW1NS-4;
- IP soft core released: FLASH Controller 1.0, Gowin_picoRV32, Scaler, CSC, PCI;
- IP soft core updated: Advanced FIR, Gowin_EMPU_M1, DDR3;
- IP hard core released: BANDGAP, rPLL, PLLVR, rSDP, rROM;
- GAO supports multiple AO cores and optimization;
- Software interface and built-in editor optimized;
- Project added in the menu bar and options of Archive Project, Restore Archived Project, Device, Configuration, and Design Summary supported;
- The synthesis of BSRAM in GowinSynthesis optimized;
- jtagserver.exe updated in Programmer;
- Programmer supports the user flash initialization of GW1N-1. Data format only supports hexadecimal or binary, and address format supports hexadecimal.

For the complete functions and enhancements of this release, please refer to 2Function and Enhancement Summary.

Note!

Gowin Synthesis tool is required to support 32-bit system.

2Function and Enhancement Summary

The following table summarizes the functions and enhancements:

Function	Description
YunYuan Software: V1.9.2Beta	
Functions	● Devices supported: GW1N-4S, GW1NS-4; ● Package supported: GW2A-18-UG324; ● IP soft core released: FLASH Controller 1.0, Gowin_picoRV32, Scaler, CSC, PCI, GW1NS-4 M3; ● IP hard core released: BANDGAP, rPLL, PLLVR, rSDP, rROM; ● IDE supports UserFlash initialization file generation; ● Project added in the menu bar and options of Archive Project, Restore Archived Project, Device, Configuration, and Design Summary supported; ● Supports set VHDL library; ● Software has an own code editor and supports the function of highlighting selected key words; ● The voltage of bank0 of the 9k top layer bankVccio is greater than 1/2 of the voltage of Bank1/bank3; ● GowinSynthesis supports matching and synthesis based on device resources.
Enhancements	● IP updated: Advanced FIR, Gowin_EMPU_M1, DDR3; ● Language(verilog/vhdl) added in IP configuration of Soft IP Core; ● GAO supports multiple AO cores; ● gao_analyzer waveform display interface signal supports rename operation; ● The GAO configuration interface supports displaying the number of BSRAM resources used by GAO; ● gao_analyzer integrates the download function of programmer; ● It needs not to resynthesize GAO if its configuration is not modified; ● MIPI TX/RX IP supports generating testbench; ● All devices support input IOType UD/OD, such as LVCMOS18UD33; ● GowinSynthesis optimizes BSRAM synthesis; ● The quality and runtime of GowinSynthesis optimized; ● jtagserver.exe updated in Programmer; ● Programmer supports user flash initialization of GW1N-1.

Function	Description
	Data format only supports hexadecimal or binary, and address format supports hexadecimal.

3 Platform Supported

The software is supported on the platforms listed below:

Windows	Windows 7/8/10(32bit/64 bit) Windows XP/7（32bit）
Linux	Centos6.8/7.0/7.5(64 bit) Ubuntu 18.04 LTS

4 Ports

Port No.	Port Type	Port Description
36545	User-defined protocol port	Used to communicate with JTAG SERVER for the GAO (Gowin Analyzer Oscilloscope) display.
36546	User-defined protocol port	Used to communicate with JTAG SERVER for the GAO (Gowin Analyzer Oscilloscope) display.
10559	User-defined protocol port	The license server port of the Gowin software back-end tool.
27020	TCP port	The license server port of the Gowin software front end tool “synplifyPro”.

5 Environment Variables Setting

LM_LICENSE_FILE Environment Variables Setting

1. Node-Locked license variable value: The license files location, such as: "D:\Synopsys\license.txt";
2. Floating license variable value: license files location, such as: 27020@192.168.31.220. “192.168.31.220” is the IP address of starting the floating license.

6 Document

The released software manuals are listed in the table below. You can download the PDF manuals and/or read them at the Gowin website.

Document	Usage
SUG100-1.8_Gowin YunYuan Software User Guide.pdf	PDF
SUG101-1.7_Gowin Design Constraints Guide.pdf	PDF
SUG114-1.9_Gowin Analyzer Oscilloscope User Guide.pdf	PDF
SUG282-1.7_Gowin Power Analyzer User Guide.pdf	PDF
SUG283-1.8_Gowin Primitive User Guide.pdf	PDF
SUG284-1.8_Gowin IP Core Generator User Guide.pdf	PDF

7 Known Issues

The following issues will be fixed in the next version.

1. It is not available to generate IP soft core using the GAO and IP Core in a 32-bit system for the time being;
2. Hierarchy display function does not support VHDL design analysis. When VHDL design is added, ERROR information will be reported in IDE output window, but it does not affect synthesis by synplifyPro.
   ERROR: Hierarch cannot support VHDL;
3. GowinSynthesis does not support VHDL design synthesis. When synthesis contains VHDL design, ERROR information will be reported in IDE output window. Please use synplifyPro to synthesise.
   Error (EXT3044): Analyze: cannot read format VHDL in this product
   Error (EXT0304): Fail to analyze the input design file;
4. Try to reduce the number of capture signals and capture depth if there are any problems with the GAO capturing. If the problem still exists, please contact GOWINSEMI technical support;
5. For DSP RTL design synthesis, the synthesis tool does not support the followings. If there are synthesis problems, please contact GOWINSEMI technical support;
   - ALU54D does not support ACCLOAD_REG mapping in the asynchronous mode;
   - The MULTALU36X18/MULTADDALU18X18 outputs may not be synthesized to mode 2 when passing through registers.


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