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ME 333
Homework 9

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1. Pros :-

→ Interrupts can be faster than polling. ie, polling uses more CPU cycles than an ISR.
→ In polling, some events may be overlooked, if more than one event occurs before the polling code executes.
→ Generally, polling execution takes more time.

Cons :-

→ Polling is preferable if the event is expected occur at a time and is not random.
→ Stack and memory management issues may occur like data 'corruptions'.

4. a). The ISR function will be tended to first and then return to normal execution.

b). The ISR at priority level 4 will be tended to first and then the ISR with priority level 2.

c). Again, the ISR at priority level 4 subpriority level 2 will be executed first. Subpriority levels do cause the current running ISR to be interrupted.

d). The current ISR will be interrupted by the priority level 6 ISR.

5. a). The first thing the CPU does when an interrupt is generated, is to save the contents of the internal CPU registers into the RAM. Once the ISR is completed, the "context" is copied back to the registers to continue normal execution.

b). When an interrupt occurs, the CPU switched to an extra set of registers called shadow register set and once the ISR is completed, the CPU switches back to the original unchanged registers.

8. a). IEC0SET = 0x0100 ; // or 0b1 << 8
IFS0CLR = 0x0100 ;
IPC2CLR = 0x001F ; // clears priority and
// sub-priority, if they were
// set something before.
IPC2SET = 0x0016 ; // or 0b000010110

b). IEC1SET = 0x8000; // or 0b1 << 15
IFS1CLR = 0x8000;
IPC8CLR = 0x1F << 24;
IPC8SET = 0x19 << 24;

cj. IEC2SET = 0x0010;
IFS2CLR = 0x0010;
IPC12CLR = 0x1F << 8; // not neccessary
IPC12SET = 0x11 << 8;

dj. IEC0SET = 0x0800;
IFS0CLR = 0x0800;
IPC2CLR = 0x1F << 24;
IPC2SET = 0x000E << 24;
INTCONSET = 0x0004; // or 0b0100

13. 0x00010008; // (0b1 << 16) | (0b1 << 3)