High-Speed Multipliers and Adders in Xilinx Vivado (Self-Project)

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Introduction :

Arithmetic circuits form the backbone of digital systems, particularly in processors, DSP blocks, and high-performance computing applications. Efficient multiplier and adder designs are crucial in reducing computational delay and improving throughput in modern VLSI and FPGA implementations. In this project, high-speed multipliers (16-bit Dadda and Wallace) and parallel prefix adders (32-bit Brent-Kung and Kogge-Stone) were implemented using Xilinx Vivado. These architectures were chosen for their proven efficiency in minimizing delay, optimizing hardware resources, and achieving scalability for larger word lengths. The goal of the project was to design, synthesize, and analyze these arithmetic circuits on FPGA to evaluate their performance in terms of speed and area utilization.

Specifications & Design Overview :

- **Arithmetic Adders :**
  - Inputs : 2, each 32-bit wide
  - **Brent-Kung** : Implemented as a **parallel prefix adder** with logarithmic depth **(O(log n))** and **minimal fan-out**.
  - **Kogge-Stone** : Implemented as a high-performance **parallel prefix adder** with the **fastest carry propagation**.
- Arithmetic Multipliers : **8 bits**
  - Inputs : 2, each 16-bit wide
  - **Dadda** : Implemented based on a **column compression scheme** that reduces the height of partial products using carry-save adders.
  - **Wallace** : Constructed using a **tree-based reduction of partial products** with faster carry-save addition.

Block Diagrams :

32-bit Brent-Kung Adder :

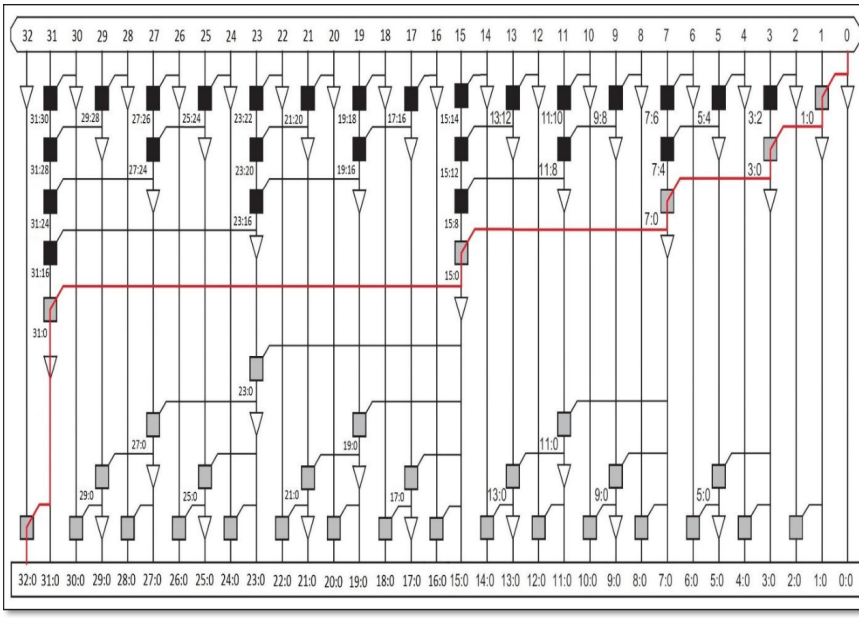

Figure 1: Block Diagram for 32-bit Brent-Kung Adder

32-bit Kogge-Stone Adder :

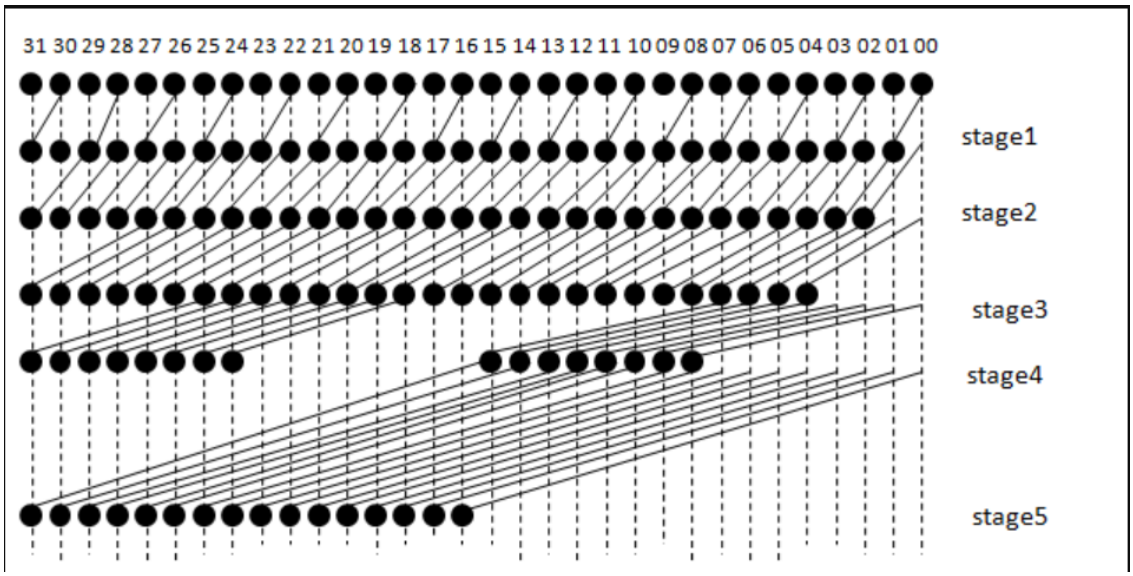

Figure 2: Block Diagram for 32-bit Kogge-Stone Adder

16-bit Dadda Multiplier :

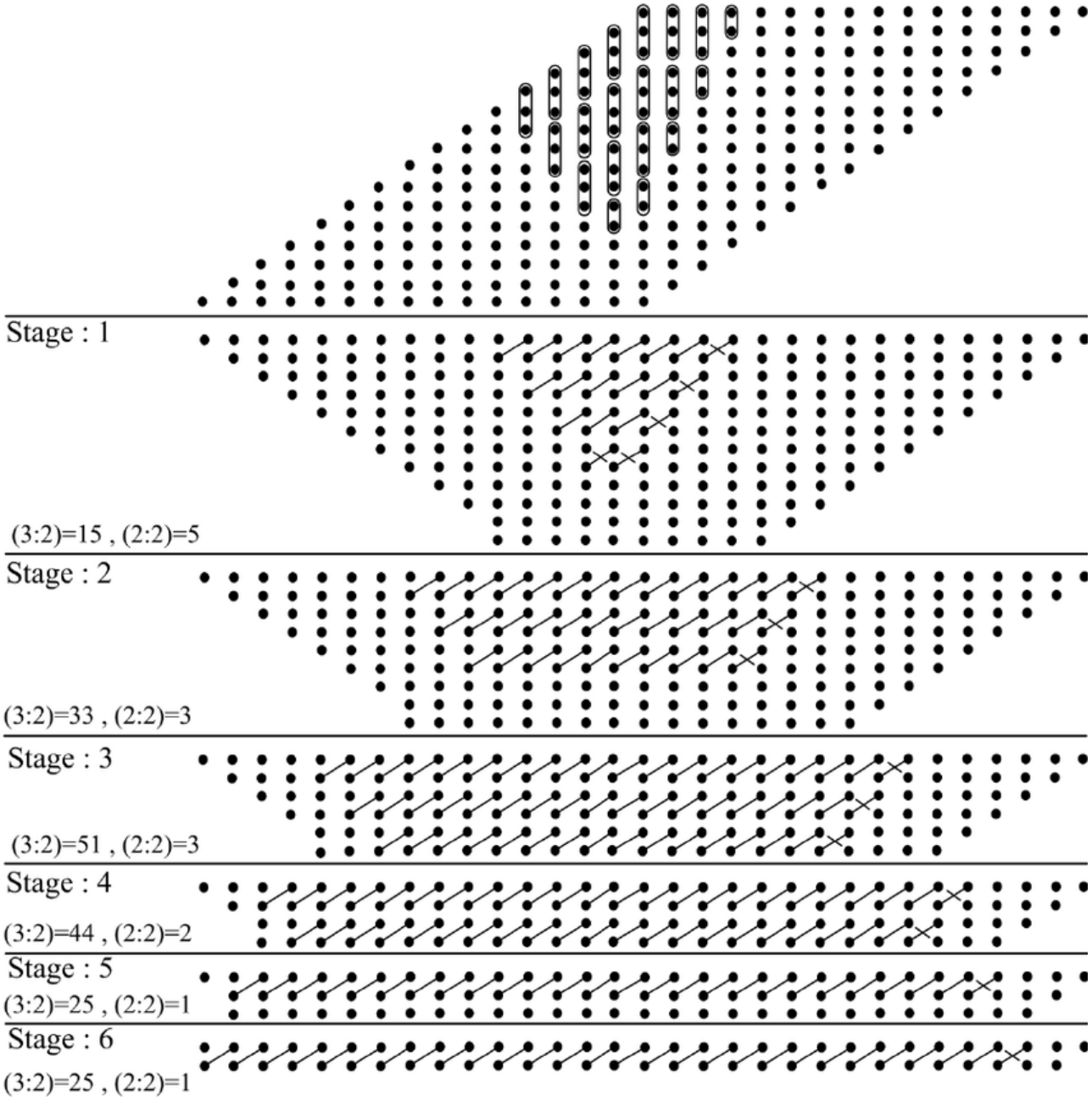

Figure 3: Block Diagram for 16-bit Dadda Multiplier

16-bit Wallace Multiplier :

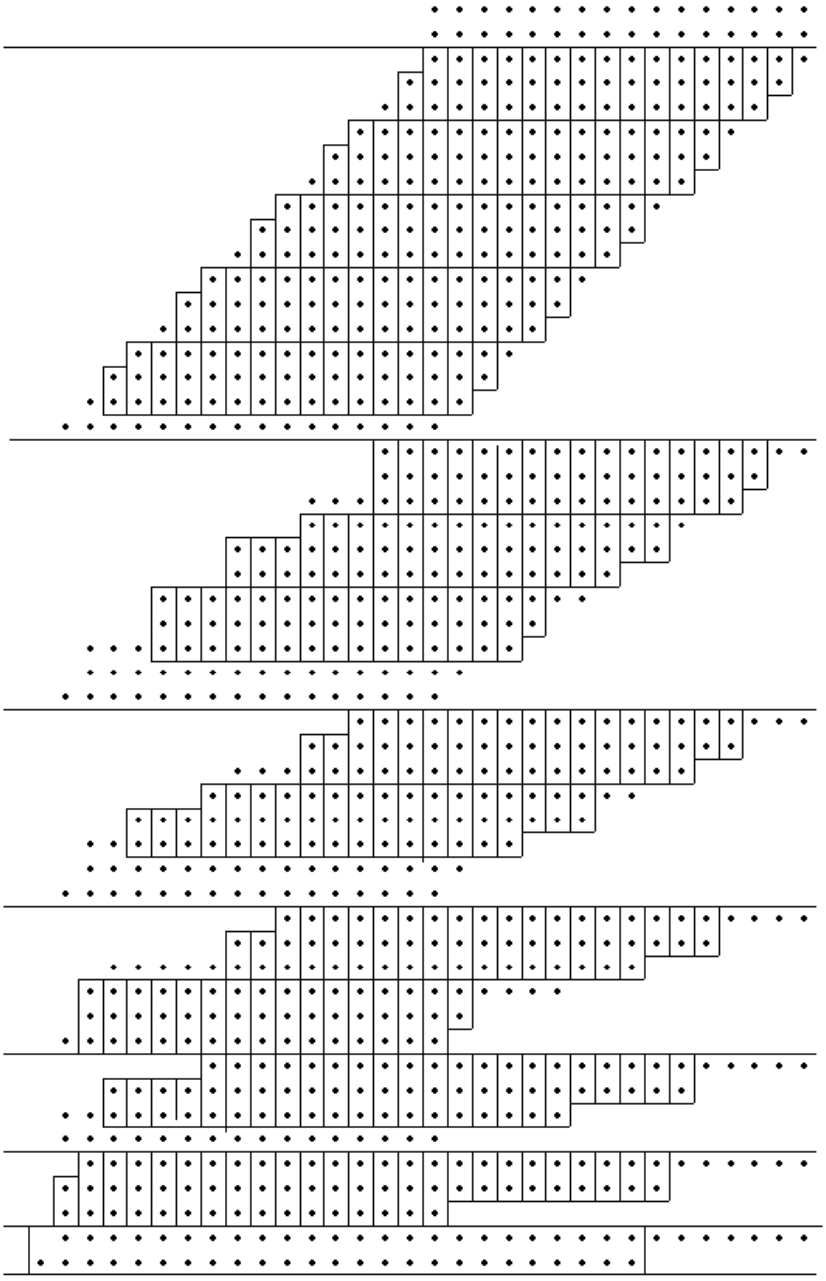

Figure 4: Block Diagram for 16-bit Wallace Multiplier

Simulation Results :

Figure 5: Simulation Results for Multipliers

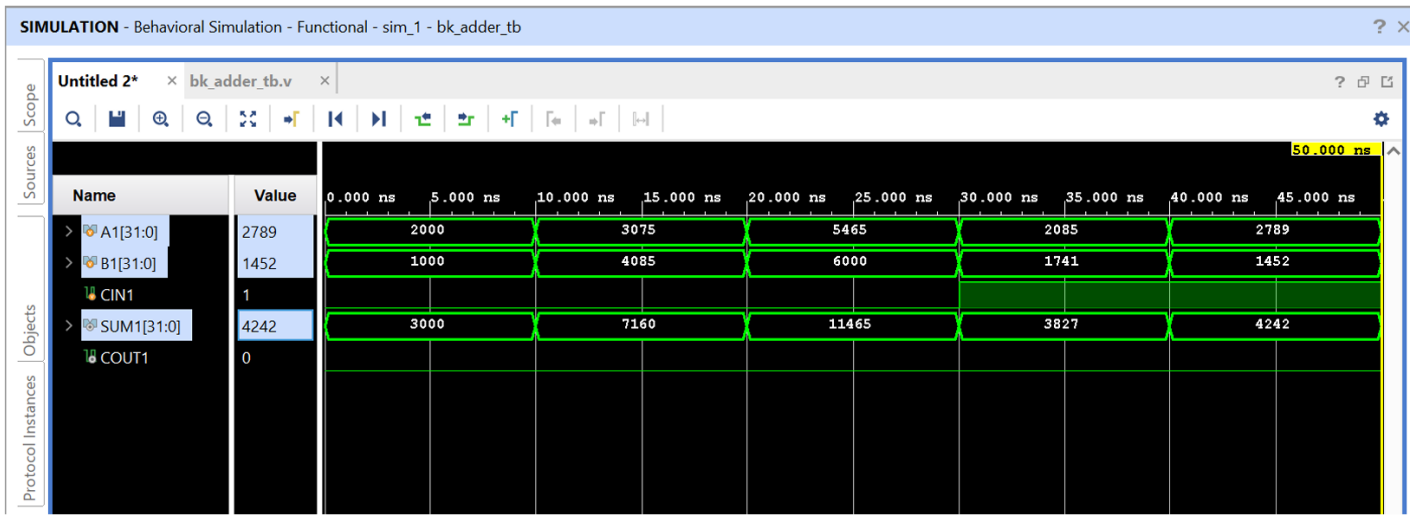

Figure 6: Simulation Results for Adders

Conclusion :

- The 16-bit Dadda and Wallace multipliers showcased reduced computation delay through partial product reduction techniques.
- The 32-bit Brent-Kung and Kogge-Stone adders provided efficient carry computation using parallel prefix structures.
- Such implementations are fundamental in optimizing the datapath of processors and can be further extended to larger word sizes or integrated into arithmetic logic units (ALUs) for RISC-V or DSP applications.