

* Records of Revision *

Rev.	Page	Description of changes	Date	prepared by
0	All	Original Release	11.10.21	Wu Tao
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☑ 一般事项 特殊事项内容:	□ 特殊事项		

Model	BTL434880-W518L	2/30	PRODUCT SPECIFICATION



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1. Features

The features of BTL434880-W518L are as follows

* Display mode : TFT 16.7M Colors, Transmissive, Normally Black

* Driving Condition : 480x3Ch-Source / 800Ch-Gate

* Connection :ZIF Type

* LCD Driver & Control IC

:NT35510(NOVATEK)

* Back Light : White LED Back Light (8 Chips in Serial)

* MPU Interface : 16 \, 18 \, 24bits RGB interface

* Type of Surface Contion

:Clear Type

2. Mechanical Specifications

Item		Specification	Unit
Resolution	Main	480(x RGB) x 800	Dot
Resolution	Sub	NA	Dot
LCM Outline Deme	nsion	61.96x104.5x2.0(Typ)	mm
Active Area (M. v. II)	Main	56.16(H)X 93.6(V)	
Active Area (W × H)	Sub	NA	mm
Divol Ditab (M v II)	Main	0.039 x 0.117	
Pixel Pitch (W x H)	Sub	NA	mm
Viewing Direction	Main	Wide View	Olalask
(Human Eye)	Sub	NA	O'clock
Gray Scale Inversion	Main	Wide View	O'clock
Direction (Contrast Ratio)	Sub	NA	(Rubbing Direction)
Weight		TBD	g

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3. Absolute Maximum Ratings

(Ta=25°C Note1)

Items	Symbol	Min.	Max.	Unit	Remark
Logic voltage	l _{ovcc}	-0.3	3.3	V	
Analog voltage	V _{cc}	-0.3	4.6	V	
Input signal voltage	V _{IN}	-0.3	IOVCC+0.5	V	
LED forward current	I _{LED}	-	25	mA	For each LED
Operation temeprature	T _{OPR}	-20	70	${\mathbb C}$	
Storage temperature	T _{STG}	-30	80	${\mathbb C}$	
Humidity (ambient		Ta≤60°C	90% F	RH Max.	

Note1: Device is subject to be damaged permanently,

if stresses beyond those absolute maximum ratings listed above.

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4. Electrical Characteristics

Main Ta=25℃

Iten	าร	Symbol	Min.	Тур.	Max.	Unit	Remark
Logic voltage		IOVCC	1.65	1.8	3.3	V	
Anolog(Power) voltage		VCC	2.72	2.8	2.88	V	
Gate	High level	V _{GH}	12	-	18	V	Note 4
voltage	Low level	V _{GL}	-6	-	-13.5	V	Note 1
Input signal	High level	V _{IH}	0.7*VDDI	-	VDDI	V	
voltage	Low level	V _{IL}	VSS	-	0.3×VCC	V	
current con	sumption	lcc	-	30	45	mA	Note 2

Note 1) The value can be adjusted by software to optimize display quality Note 2) Display Black Pattern

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5. Recommended Software Setting Value (LDI: NT35510)

		9 14146 (221: 111		
#Enable Page1	# VGMN/VGSN	REGW 0xD127,0x52	REGW 0xD221,0xD5	REGW 0xD31B,0x3D
REGW 0xF000,0x55	REGW 0xBD00,0x00	REGW 0xD128,0x03	REGW 0xD222,0x03	REGW 0xD31C,0x02
REGW 0xF001,0xAA	REGW 0xBD01,0x80	REGW 0xD129,0x6B	REGW 0xD223,0x09	REGW 0xD31D,0x75
REGW 0xF002,0x52	REGW 0xBD02,0x00	REGW 0xD12A,0x03	REGW 0xD224,0x03	REGW 0xD31E,0x02
REGW 0xF003,0x08		REGW 0xD12B,0x8D	REGW 0xD225,0x28	REGW 0xD31F,0xB1
REGW 0xF004,0x01	# VCOM=-0.1	REGW 0xD12C,0x03	REGW 0xD226,0x03	REGW 0xD320,0x02
	REGW 0xBE00,0x00	REGW 0xD12D,0xA2	REGW 0xD227,0x52	REGW 0xD321,0xD5
# AVDD: manual,	REGW 0xBE01,0x2F	REGW 0xD12E,0x03	REGW 0xD228,0x03	REGW 0xD322,0x03
REGW 0xB600,0x34	·	REGW 0xD12F,0xBB	REGW 0xD229,0x6B	REGW 0xD323,0x09
REGW 0xB601,0x34	#R+	REGW 0xD130,0x03	REGW 0xD22A,0x03	REGW 0xD324,0x03
REGW 0xB602,0x34	REGW 0xD100,0x00	REGW 0xD131,0xC1	REGW 0xD22B,0x8D	REGW 0xD325,0x28
	REGW 0xD101,0x37	REGW 0xD132,0x03	REGW 0xD22C,0x03	REGW 0xD326,0x03
REGW 0xB000,0x0C	REGW 0xD102,0x00	REGW 0xD133,0xC1	REGW 0xD22D,0xA2	REGW 0xD327,0x52
REGW 0xB001,0x0C	REGW 0xD103,0x53		REGW 0xD22E,0x03	REGW 0xD328,0x03
REGW 0xB002,0x0C	REGW 0xD104,0x00	#G+	REGW 0xD22F,0xBB	REGW 0xD329,0x6B
# AVEE: manual, -6V	REGW 0xD105,0x79	REGW 0xD200,0x00	REGW 0xD230,0x03	REGW 0xD32A,0x03
REGW 0xB700,0x24	REGW 0xD106,0x00	REGW 0xD201,0x37	REGW 0xD231,0xC1	REGW 0xD32B,0x8D
REGW 0xB701,0x24	REGW 0xD107,0x97	REGW 0xD202,0x00	REGW 0xD232,0x03	REGW 0xD32C,0x03
REGW 0xB702,0x24	REGW 0xD108,0x00	REGW 0xD203,0x53	REGW 0xD233,0xC1	REGW 0xD32D,0xA2
	REGW 0xD109,0xB1	REGW 0xD204,0x00		REGW 0xD32E,0x03
REGW 0xB100,0x0C	REGW 0xD10A,0x00	REGW 0xD205,0x79	#B+	REGW 0xD32F,0xBB
REGW 0xB101,0x0C	REGW 0xD10B,0xD5	REGW 0xD206,0x00	REGW 0xD300,0x00	REGW 0xD330,0x03
REGW 0xB102,0x0C	REGW 0xD10C,0x00	REGW 0xD207,0x97	REGW 0xD301,0x37	REGW 0xD331,0xC1
	REGW 0xD10D,0xF4	REGW 0xD208,0x00	REGW 0xD302,0x00	REGW 0xD332,0x03
#Power Control for	REGW 0xD10E,0x01	REGW 0xD209,0xB1	REGW 0xD303,0x53	REGW 0xD333,0xC1
VCL	REGW 0xD10F,0x23	REGW 0xD20A,0x00	REGW 0xD304,0x00	
REGW 0xB800,0x34	REGW 0xD110,0x01	REGW 0xD20B,0xD5	REGW 0xD305,0x79	#R-
REGW 0xB200,0x00	REGW 0xD111,0x49	REGW 0xD20C,0x00	REGW 0xD306,0x00	REGW 0xD400,0x00
# VGH: Clamp Enable,	REGW 0xD112,0x01	REGW 0xD20D,0xF4	REGW 0xD307,0x97	REGW 0xD401,0x37
REGW 0xB900,0x34	REGW 0xD113,0x87	REGW 0xD20E,0x01	REGW 0xD308,0x00	REGW 0xD402,0x00
REGW 0xB901,0x34	REGW 0xD114,0x01	REGW 0xD20F,0x23	REGW 0xD309,0xB1	REGW 0xD403,0x53
REGW 0xB902,0x34	REGW 0xD115,0xB6	REGW 0xD210,0x01	REGW 0xD30A,0x00	REGW 0xD404,0x00
	REGW 0xD116,0x02	REGW 0xD211,0x49	REGW 0xD30B,0xD5	REGW 0xD405,0x79
REGW 0xB300,0x08	REGW 0xD117,0x00	REGW 0xD212,0x01	REGW 0xD30C,0x00	REGW 0xD406,0x00
REGW 0xB301,0x08	REGW 0xD118,0x02	REGW 0xD213,0x87	REGW 0xD30D,0xF4	REGW 0xD407,0x97
REGW 0xB302,0x08	REGW 0xD119,0x3B	REGW 0xD214,0x01	REGW 0xD30E,0x01	REGW 0xD408,0x00
	REGW 0xD11A,0x02	REGW 0xD215,0xB6	REGW 0xD30F,0x23	REGW 0xD409,0xB1
# VGL(LVGL):	REGW 0xD11B,0x3D	REGW 0xD216,0x02	REGW 0xD310,0x01	REGW 0xD40A,0x00
REGW 0xBA00,0x14	REGW 0xD11C,0x02	REGW 0xD217,0x00	REGW 0xD311,0x49	REGW 0xD40B,0xD5
REGW 0xBA01,0x14	REGW 0xD11D,0x75	REGW 0xD218,0x02	REGW 0xD312,0x01	REGW 0xD40C,0x00
REGW 0xBA02,0x14	REGW 0xD11E,0x02	REGW 0xD219,0x3B	REGW 0xD313,0x87	REGW 0xD40D,0xF4
# VGL_REG(VGLO)	REGW 0xD11F,0xB1	REGW 0xD21A,0x02	REGW 0xD314,0x01	REGW 0xD40E,0x01
REGW 0xB500,0x08	REGW 0xD120,0x02	REGW 0xD21B,0x3D	REGW 0xD315,0xB6	REGW 0xD40F,0x23
REGW 0xB501,0x08	REGW 0xD121,0xD5	REGW 0xD21C,0x02	REGW 0xD316,0x02	REGW 0xD410,0x01
REGW 0xB502,0x08	REGW 0xD122,0x03	REGW 0xD21D,0x75	REGW 0xD317,0x00	REGW 0xD411,0x49
# VGMP/VGSP:	REGW 0xD123,0x09	REGW 0xD21E,0x02	REGW 0xD318,0x02	REGW 0xD412,0x01
REGW 0xBC00,0X00	REGW 0xD124,0x03	REGW 0xD21F,0xB1	REGW 0xD319,0x3B	REGW 0xD413,0x87
REGW 0xBC01,0x80	REGW 0xD125,0x28	REGW 0xD220,0x02	REGW 0xD31A,0x02	
REGW 0xBC02,0X00	REGW 0xD126,0x03			
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REGW 0xD417,0x00 REGW 0xD418,0x02	REGW 0xD510,0x01 REGW 0xD511,0x49	REGW 0xD609,0xB1 REGW 0xD60A,0x00	REGW 0xF002,0x52 REGW 0xF003,0x08	REGW 0xFF03,0x01
REGW 0xD419,0x3B	REGW 0xD512,0x01	REGW 0xD60B,0xD5	REGW 0xF004,0x00	#REGW 0xF304,0x11
REGW 0xD41A,0x02	REGW 0xD513,0x87	REGW 0xD60C,0x00		#EGW 0xF306,0x10
REGW 0xD41B,0x3D	REGW 0xD514,0x01	REGW 0xD60D,0xF4	# RGB I/F Setting	#REGW 0xF408,0x00
REGW 0xD41C,0x02	REGW 0xD515,0xB6	REGW 0xD60E,0x01	REGW 0xB000,0x08	
REGW 0xD41D,0x75	REGW 0xD516,0x02	REGW 0xD60F,0x23	REGW 0xB001,0x05	
REGW 0xD41E,0x02	REGW 0xD517,0x00	REGW 0xD610,0x01	REGW 0xB002,0x02	#REGW 0x3a00,0x77
REGW 0xD41F,0xB1	REGW 0xD518,0x02	REGW 0xD611,0x49	REGW 0xB003,0x05	
REGW 0xD420,0x02	REGW 0xD519,0x3B	REGW 0xD612,0x01	REGW 0xB004,0x02	REGW 0x1100
REGW 0xD421,0xD5	REGW 0xD51A,0x02	REGW 0xD613,0x87		DELAY 120
REGW 0xD422,0x03	REGW 0xD51B,0x3D	REGW 0xD614,0x01	## SDT:	
REGW 0xD423,0x09	REGW 0xD51C,0x02	REGW 0xD615,0xB6	REGW 0xB600,0x05	REGW 0x2900
REGW 0xD424,0x03	REGW 0xD51D,0x75	REGW 0xD616,0x02		
REGW 0xD425,0x28	REGW 0xD51E,0x02	REGW 0xD617,0x00	## Gate EQ:	
REGW 0xD426,0x03	REGW 0xD51F,0xB1	REGW 0xD618,0x02	REGW 0xB700,0x70	
REGW 0xD427,0x52	REGW 0xD520,0x02	REGW 0xD619,0x3B	REGW 0xB701,0x70	
REGW 0xD428,0x03	REGW 0xD521,0xD5	REGW 0xD61A,0x02		
REGW 0xD429,0x6B	REGW 0xD522,0x03	REGW 0xD61B,0x3D	## Source EQ:	
REGW 0xD42A,0x03	REGW 0xD523,0x09	REGW 0xD61C,0x02	REGW 0xB800,0x01	
REGW 0xD42B,0x8D	REGW 0xD524,0x03	REGW 0xD61D,0x75	REGW 0xB801,0x05	
REGW 0xD42C,0x03	REGW 0xD525,0x28	REGW 0xD61E,0x02	REGW 0xB802,0x05	
REGW 0xD42D,0xA2	REGW 0xD526,0x03	REGW 0xD61F,0xB1	REGW 0xB803,0x05	
REGW 0xD42E,0x03	REGW 0xD527,0x52	REGW 0xD620,0x02		
REGW 0xD42F,0xBB	REGW 0xD528,0x03	REGW 0xD621,0xD5	# Inversion: Column	
REGW 0xD430,0x03	REGW 0xD529,0x6B	REGW 0xD622,0x03	inversion (NVT)	
REGW 0xD431,0xC1	REGW 0xD52A,0x03	REGW 0xD623,0x09	REGW 0xBC00,0x00	
REGW 0xD432,0x03	REGW 0xD52B,0x8D	REGW 0xD624,0x03	REGW 0xBC01,0x00	
REGW 0xD433,0xC1	REGW 0xD52C,0x03	REGW 0xD625,0x28	REGW 0xBC02,0x00	
	REGW 0xD52D,0xA2	REGW 0xD626,0x03		
#G-	REGW 0xD52E,0x03	REGW 0xD627,0x52	# BOE's Setting	
REGW 0xD500,0x00	REGW 0xD52F,0xBB	REGW 0xD628,0x03	(default)	
REGW 0xD501,0x37	REGW 0xD530,0x03	REGW 0xD629,0x6B	REGW 0xCC00,0x03	
REGW 0xD502,0x00	REGW 0xD531,0xC1	REGW 0xD62A,0x03	REGW 0xCC01,0x50	
REGW 0xD503,0x53	REGW 0xD532,0x03	REGW 0xD62B,0x8D	REGW 0xCC02,0x50	
REGW 0xD504,0x00	REGW 0xD533,0xC1	REGW 0xD62C,0x03		
REGW 0xD505,0x79		REGW 0xD62D,0xA2	# Display Timing:	
REGW 0xD506,0x00	#B-	REGW 0xD62E,0x03	REGW 0xBD00,0x01	
REGW 0xD507,0x97	REGW 0xD600,0x00	REGW 0xD62F,0xBB	REGW 0xBD01,0x00	
REGW 0xD508,0x00	REGW 0xD601,0x37	REGW 0xD630,0x03	REGW 0xBD02,0x07	
REGW 0xD509,0xB1	REGW 0xD602,0x00	REGW 0xD631,0xC1	REGW 0xBD03,0x31	
REGW 0xD50A,0x00	REGW 0xD603,0x53	REGW 0xD632,0x03	REGW 0xBD04,0x00	
REGW 0xD50B,0xD5	REGW 0xD604,0x00	REGW 0xD633,0xC1		
REGW 0xD50C,0x00	REGW 0xD605,0x79			

NOTE: BOE requires the customer to follow the above instructions strictly. If customer would like to change the above instructions, the customer should inform BOE and get re-check from BOE, or the customer will be responsible for any unexpected result because of the change.

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6. Back Light System Characteristics

Ta=25°C

Items	Symbol	Min.	Тур.	Max.	Unit	Remark
Forward current	lf	-	20	25	mA	Note1
Forward voltage	Vf	3.0	-	3.4	٧	Note1
B/L Power consumption	P _{BL}	-	-	680	mW	Note2

Note 1: The Driving conditon is defined for each LED chip.

Note 2: The B/L Power consumption is defined for the backlight module.the schematic drawing of the backlight module as the figure.

BLU CIRCUIT DIAGRAM

Ref. Total power consumpation(max) depends on LED current/ LED driver efficiency, etc.

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7. Optical Characteristics

Transmissive Mode

Ta=25℃

-									
It	em	Sy	mbol	Min.	Тур.	Max.	Unit	Condition	Note
			Ø=0° (X1)	70	80	-			
Vie	ewing	Δ	Ø=180° (X2)	70	80	-			Note2
A	ngle	O	Ø=90° (Y1)	70	80	-	deg.	Cr > 10	Notez
		$\theta = \frac{\sqrt{(x,y)}}{\sqrt{y}} = $	70	80	-				
	ast ratio missive)		Cr	-	800	-	=	$\theta = 0$ $\emptyset = 0$	Note1 Note4
Respo	nse Time	Tı	r + Tf	-	30	55	ms	$\theta = 0$ $\emptyset = 0$	Note3
CIE	R		(x,y)	0.61, 0.29	0.65, 0.33	0.69,0.37			
Coordi	G	((x,y)	0.27, 0.58	0.31, 0.62	0.35, 0.66		$\theta = 0$	
- nate	В		(x,y)	0.1, 0.01	0.14, 0.05	0.18,0.09		$\emptyset = 0$	
	W	((x,y)	0.25, 0.28	0.29, 0.32	0.33,0.36			
Brig	htness		L	300	350	-	cd/m2	20mA/LED	Note5
Unif	ormity			80	-	-		20mA/LED	Note6

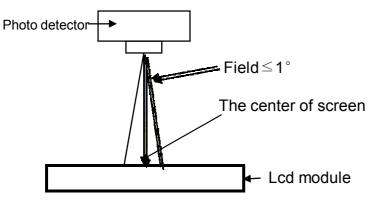
^{*} Ø = 0 $^{\circ}\,$, Ø = 90 $^{\circ}\,$,Ø = 180 $^{\circ}\,$,Ø = 270 $^{\circ}\,\,$ means viewing direction.

^{*} B/L is turned on.

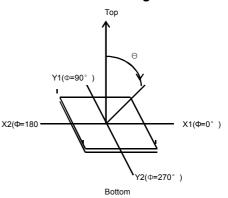


The optical characteristics should be measured in dark room, and after 5 minutes operation, the measurment begin.

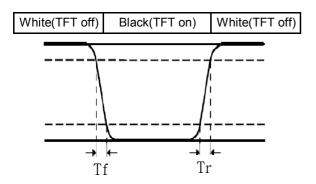
Note1. Definition of Measure System



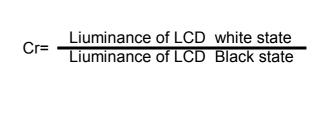
Note2. Definition of Angle O.



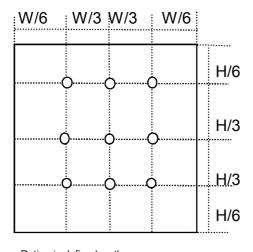
Note3. Definition of Response Time



Note4.definition of contrast ratio



Note 5. Measuring Point(9 Points) (WxH)



Note 6. definition of Uniformity

Uniformity= max. Liuminance of measurede point max. Liuminance of measurede poin

Rating is defined as the average brightness inside the viewing area

Model

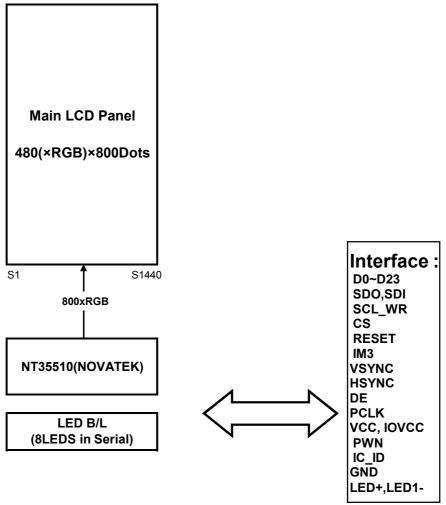
BTL434880-W518L

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8. Block Diagram



Select the MPU interface mode as listed below:

IM3	IM2	IM1	IM0	SRAM	Register
Χ	0	0	0	80-series 8-bit MPU interface, D[7:0]	80-series 8-bit MPU interface, D[7:0]
Χ	0	0	1	80-series 16-bit MPU interface, D[15:0]	80-series 16-bit MPU interface, D[15:0]
Χ	0	1	0	80-series 24-bit MPU interface, D[23:0]	80-series 24-bit MPU interface, D[23:0]
0	0	1	1	RGB interface, D[23:0]	SPI, SDI/SDO serial data, SCL rising trigger
1	0	1	1	RGB interface, D[23:0]	SPI, SDI/SDO serial data, SCL falling trigger
Χ	1	0	0	RGB interface, D[23:0]	I2C interface, I2C_SDA serial data
Χ	1	0	1	MIPI DSI, HSSI_D0_P/N, HSSI_D1_P/N	MIPI DSI, HSSI_D0_P/N, HSSI_D1_P/N
0	1	1	0	MDDI, HSSI_D0_R/N, HSSI_D1_R/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N SPI, SDI/SD0 serial data, SCL rising trigger
1	1	1	0	MDDI, HSSI_D0_P/N, HSSI_D1_P/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N SPI, SDI/SDO serial data, SCL falling trigger
Х	1	1		MDDI, HSSI_D0_P/N, HSSI_D1_P/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N 12C interface, I2C_SDA serial data

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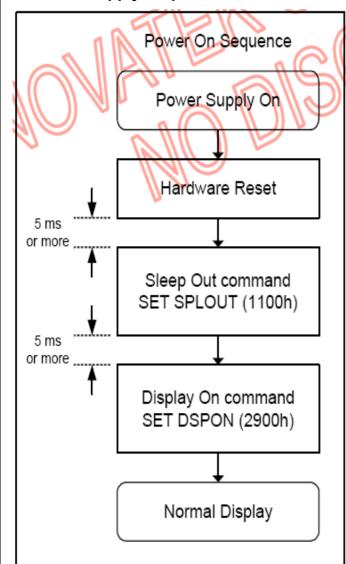
9. Interface Pin Assignment

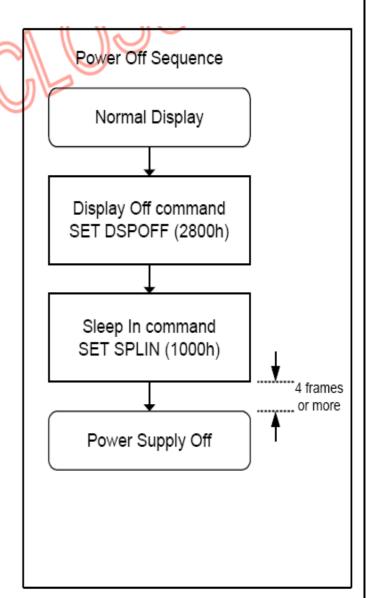
		4551 <u>4</u> 1111111111	
NO.	SYMBOL	Description	I/O
1	GND	Ground	Power supply I
2	VLED+	LED Anode	Power supply I
3	VLED-	LED Cathode	Power supply I
4	VDD	Power supply 2.8V	Power supply I
5	IOVCC	Power supply 1.8V	Power supply I
6	SD0	Serial data output pin	0
7	SDI	Serial data input pin	I
8	GND	Ground	Power supply I
9	SCLK		I
		Serial data clock input pin	I
10	CS	Chip select	
11	IM3	For serial interface, RGB+SPI interface and MDDI+SPI	I
12	RESET	RESET	I
13	R0	data bus	I/O
14	R1	data bus	I/O
15	R2	data bus	I/O
16	R3	data bus	I/O
17	R4	data bus	I/O
18	R5	data bus	I/O
19	R6	data bus	I/O
20	R7	data bus	I/O
21	GO	data bus	I/O
22	G1	data bus	I/O
23	G2	data bus	I/O
24	G3	data bus	I/O
25	G4	data bus	I/O
26	G5	data bus	I/O I/O
27 28	G6 G7	data bus	I/O
29	B0	data bus	I/O
30	В1	data bus	I/O
31	B2	data bus	I/O
32	B3	data bus	I/O
33	B4	data bus	I/O
34	B5	data bus	I/O
35	В6	data bus	I/O
36	B7	data bus	I/O
37	ENABLE	Serial enable signal	I
38	GND	Ground	Power supply I
39	PCLK	Data-Clock	I
40	GND	Ground	Power supply I
41	HSYNC	Horizontal Synchronous Signal	I
42	VSYNC	Vertical Synchronous Signal	I
43	IC_ID	Chip ID code	I
44	LEDPWM	LEDPWM CONTROL	0
45	GND	Ground	Power supply I

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10. Power Supply Sequence







11. Read/Write Timing characteristics (RGB+SPI I/F)

1) RGB Read/Write Timing

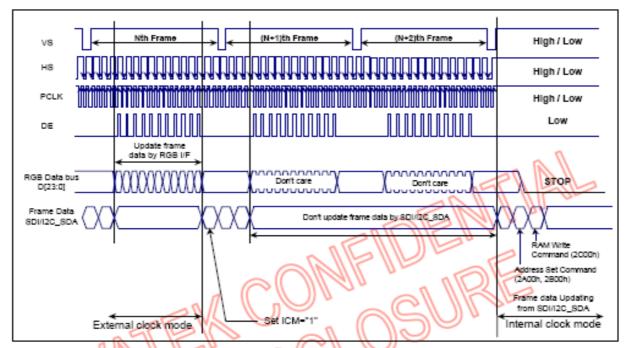


Fig. 5.8.4 RGB with SPI Timing Sequence (Enter Internal Clock Mode, ICM="1")

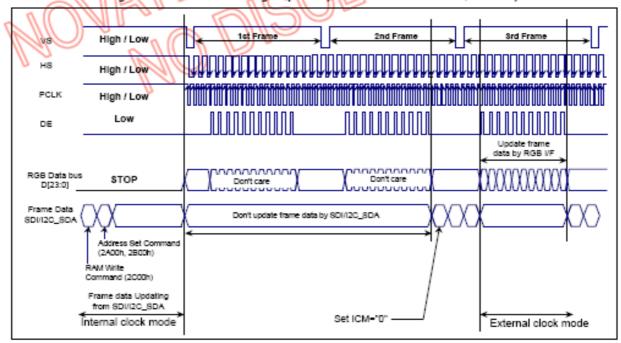


Fig. 5.8.5 RGB with SPI Timing Sequence (Exit Internal Clock Mode, ICM="0")

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2) SPI Read/Write Timing Transmission Byte Transmission Byte CIEX (Host to Driver IC) (SCL (Stoot to Other IC) (Riving Edge, 1863 = 0) (CL (Host to Other IC) (Falling Edge, 1863 = 1) JUUL ſТТТ ···· (***) SDO (Driver IC to Host) CSX (Host to Driver IC) SCL (Most to Driver IC) Riving Edge, IM3 = 0) JUUL SCL (Host to Driver IC) (Falling Edge 1913 - 1) ĴŨŨ (Heat to Driver IC) (Delver IC to Host) High High-Z High-Z High-Z R/W = 0 for Whiting Command / Address D/CX = 0 for Command / Address Trans H/L = 0 for Command / Address Low By JUUL (Host to Driver IC) (Riving Edge, IM3 = 0) SCL (Host to Driver IC) (Falling Edge, IM) = 1) ſŢŢŢ SDI (Host to Driver IC) High-Z High-Z Fig. 5.1.5 Serial bus protocol for register write mode Transmission Byte Transmission Byte SCL (Most to Driver IC) (Rhing Edge, IM3 = 0) IJIJ SCL (Host to Driver IC) falling Edge, IM3 = 1.111SDI (Host to Driver IC) High-Z յլյլ ſŪŢŪ (Host to Driver IC) (Falling Edge, IM3 *1) (Heat to Driver IC) TO THE CONTROL OF THE High-Z High-Z Transmission Byte-Thansmission Dyte CISX (Host to Driver IC) SCL (Host to Driver IC) (Riving Edgs, 1963 = 0) ПП SCL (Host to Oriver IC) falling Edge, IM3 = ĵIJŢŢ High-Z SDO (Driver IC to Host) High-Z High-Z (ata)(ata)(ata)(ata)(ata)(ata)(ata)

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Fig. 5.1.6 Serial bus protocol for register read mode



2) Reset Timing characteristics

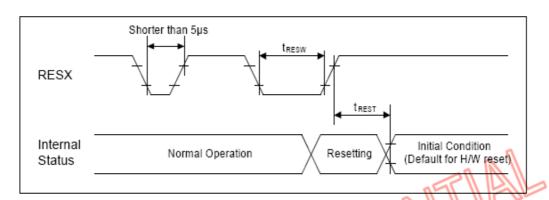
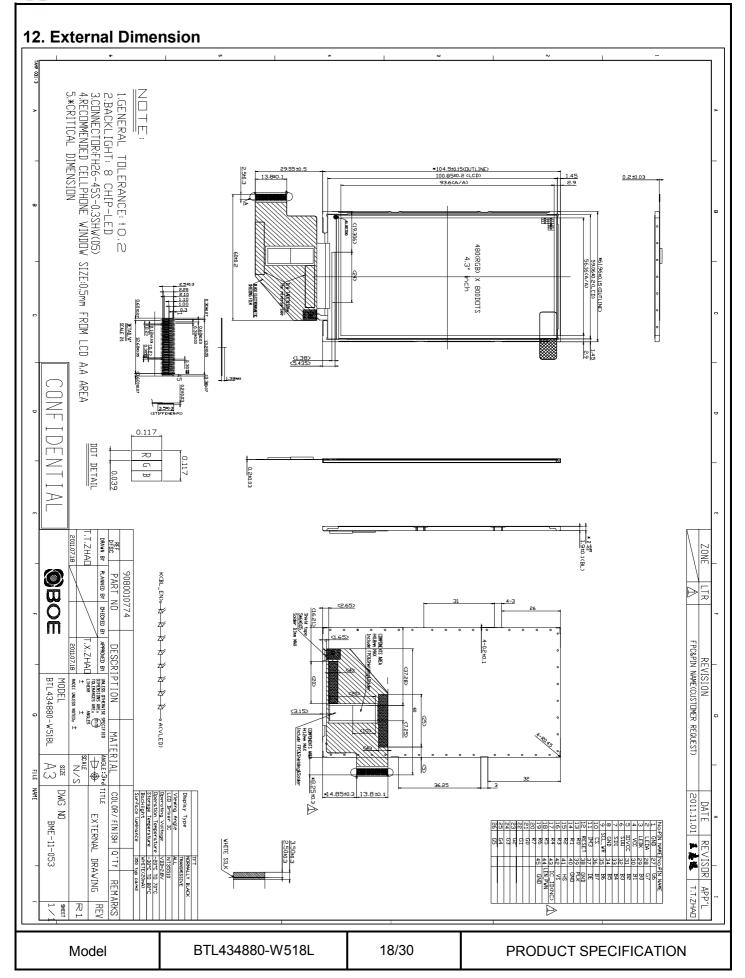


Fig. 7.6.12 Reset input timing

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

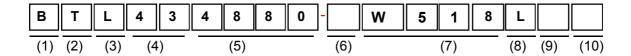
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
	tresw	Reset "L" pulse width (Note 1)	10	יט - ת	,	μs	
RESX	toror	Reset complete time (Note 2)		0	200	ms	When reset applied during Sleep In Mode
	trest	Reset complete unite (Note 2)	ā		720	ms	When reset applied during Sleep Out Mode







13. COLOR LCD MODULE NUMBERING SYSTEM



- (1) B: BHL
- (2) Drive System

C: CSTN T: TFT E: OLED M: MONO

(3) Product Status

L: LCD Model F: FOG Model G: COG Model P: PANEL Model C: CELL Model

(4) Display size(精确到小数点后1位,四舍五入)

(5) Resolution

Number of Row Dots * Number of column Dots(前两位有效)

(6) Viewing Direction

Nil: 6 H U: 12 H L: 9 H R: 3 H W: Wide view E: 其他

- (7) Serial Number (*001-9999: 按照产品状态,各类产品序列号实行大排行处理,*为0时省略不写)
- (8) Back Light

Nil:Without backlight + Reflective H:CCFL + Translective

T:Without backlight + Transflective E:LED Frontlight + Reflective

F:CCFL Frontlight + Reflective D:LED + Transflective

L:LED + Transmissive

(9)DUAL LCD

Nil: Single LCD M:MONO C:CSTN T:TFT O:OLED

(10)TOUCH PANEL

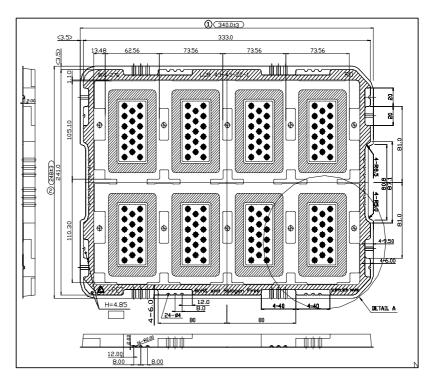
Nil:Without TP P:with TP

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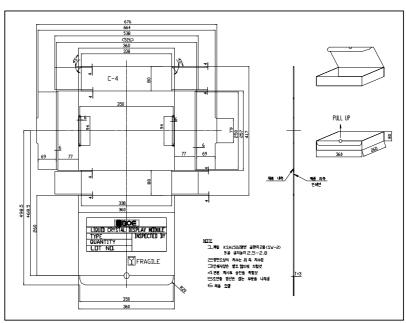
14. Package Terms

1、Tray Size L:340mm W:248mm (8pcs LCM/Tray)



2、Inner BOX Size L:360mm W:260mm H:80mm

(7pcs Tray) / Inner Box)



Inner Box Drawing

PRODUCT SPECIFICATION	20/30	BTL434880-W518L	Model
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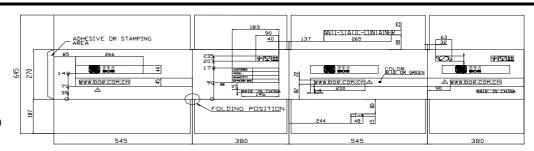


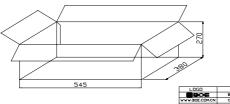
3、Out BOX Size

L: 545mm

W: 380mm H: 270mm

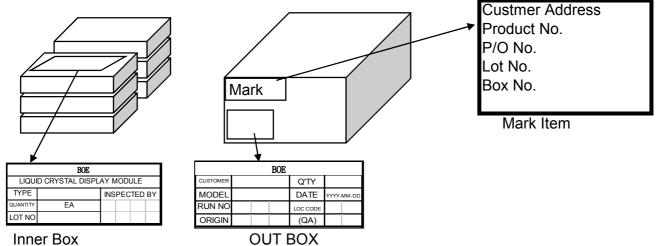
(6pcs Inner / Out)





NOTE 1.MATERIAL: KSA 1531,DW2(T=8mm) 2.DRAWING DIMESIONS ARE EQUAL TO OUTSIDE DIMENSION. 3.INNER BOXCC-4) ARRANGEMENT: 3STEPS X2ROWS 4.MARKS ARE REFER TO SEPERATE CONSULTATION.

4. Packing label content



5. Packing notice

- [1]Sub LCD should be placed upwardly while in the tray.
- [2] Every seven full trays with a blank one while twining twice on both sides by adhesive tape.
- [3]. Every tray should be put crossedly.

6. Product label

[1] There should be Logo and product modle of BOE on FPC ASS'Y.

7、Packing Q'ty list

			INNER BOX	TRAY	MODULE
OUT BOX			6	42	288
	INNER E	зох	1	7	48
		TRAY	-	1	8

Model BTL434880)-W518L 21/30	PRODUCT SPECIFICATION
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