

\*\*\*\*\*DRAFT\*\*\*\*\*

## **Adapting the ICOBOARD ZIPCPU to the CATBOARD**

06/05/18

\*\*\*\*\*DRAFT\*\*\*\*\*

The following information is from <https://github.com/ZipCPU/zipcpu/blob/master/doc/spec.pdf>

### **Introduction**

*The goal of the ZipCPU was to be a very simple CPU. You might think of it as a poor man's alternative to the OpenRISC architecture. You might also think of it as an Open Source microcontroller. For this reason, all instructions have been designed to be as simple as possible, and the base instructions are all designed to be executed in one instruction cycle per instruction, barring pipeline stalls.<sup>1</sup> Indeed, even the bus has been simplified to a constant 32-bit width, with no option for more or less. This has resulted in the choice to drop push and pop instructions, pre-increment and post-decrement addressing modes, the integrated memory management unit (MMU), and more*

*For those who like buzz words, the ZipCPU is:*

*A 32-bit CPU: All registers are 32-bits, addresses are 32-bits, instructions are 32-bits wide, etc.*

*A RISC CPU. There is no microcode for executing instructions. All instructions are designed to be completed in one clock cycle.*

*A Load/Store architecture. (Only load and store instructions can access memory.)*

*Wishbone compliant. All peripherals are accessed just like memory across this bus.*

*A Von-Neumann architecture. The instructions and data share a common bus.*

*A pipelined architecture, having stages for Prefetch, Decode, Read-Operand, a combined stage containing the ALU, Memory, Divide, and Floating Point units, and then the final Write-back stage. See Fig. 1.1 for a diagram of this structure.*

*Completely open source, licensed under the GPL.<sup>3</sup>*

OpCode	A-Reg	Instruction		Sets CC
5'h00	SUB	Subtract		Y
5'h01	AND	Bitwise And		
5'h02	ADD	Add two numbers		
5'h03	OR	Bitwise Or		
5'h04	XOR	Bitwise Exclusive Or		
5'h05	LSR	Logical Shift Right		
5'h06	LSL	Logical Shift Left		
5'h07	ASR	Arithmetic Shift Right		
5'h08	BREV	Bit Reverse B operand into result		N
5'h09	LDILO	Load Immediate Low		
5'h0a	MPYUHI	Upper 32 of 64 bits from an unsigned 32x32 multiply		Y
5'h0b	MPYSHI	Upper 32 of 64 bits from a signed 32x32 multiply		
5'h0c	MPY	32x32 bit multiply		
5'h0d	MOV	Move OpB into Ra		N
5'h0e	DIVU	R0-R13	Divide, unsigned	Y
5'h0f	DIVS	R0-R13	Divide, signed	
5'h10	CMP	Compare (Ra-OpB) to zero		Y
5'h11	TST	Test (AND w/o setting result)		
5'h12	LW	Load a 32-bit word from memory (OpB) into Ra		N
5'h13	SW	Store a 32-bit word from Ra into memory at (OpB)		
5'h14	LH	Load 16-bits from memory (OpB) into Ra, clear upper 16 bits		
5'h15	SH	Store the lower 16-bits of Ra into memory at (OpB)		
5'h16	LB	Load 8-bits from memory (OpB) into Ra, clear upper 24 bits		
5'h17	SB	Store the lower 8-bits of Ra into memory at (OpB)		
5'h18/9	LDI	Load 23-bit signed immediate		N
5'h1a	FPADD	R0-R13	Floating point add	Y
5'h1b	FPSUB	R0-R13	Floating point subtract	
5'h1c	FPMPY	R0-R13	Floating point multiply	
5'h1d	FPDIV	R0-R13	Floating point divide	
5'h1e	FPI2F	R0-R13	Convert integer to floating point	
5'h1f	FPF2I	R0-R13	Convert floating point to integer	
5'h1c	BREAK	None(15)		N
5'h1d	LOCK	None(15)		
5'h1e	SIM	None(15)		
5'h1f	NOOP	None(15)		

Table 2.2: ZipCPU OpCodes

***“export PATH=/home/pi/zipcpu/sw/install/cross-tools/bin:/home/pi/autofpga/sw/:\$PATH”***

***“cd catzip”***

***“make clean”***

***“make” This creates the 2 executeables arm-netpport & arm-wbregs used to communicate with the FPGA.in files for download to FPGA***

***In additon compiles the***

***The rtl has several folders basic, uart,catzip, leddigits, pptest, switch\_leds, and sdram where \*.bin files are created.***

***The sw/host has 2 executeables arm-netpport & arm-wbregs used to communicate with the FPGA.***

- 20180605-build.v
- 20180605-cat.tjz
- auto-data
  - bkram.txt
  - board.h
  - board.ld
  - buserr.txt
  - clock.txt
  - dlyarbiter.txt
  - global.txt
  - gpio.txt
  - hbconsole.txt
  - legalgen.txt
  - main\_tb.cpp
  - main.v
  - Makefile
  - pic.txt
  - pwrcount.txt
  - regdefs.cpp
  - regdefs.h
  - rtl.make.inc
  - testb.h
  - toplevel.v
  - version.txt
  - wbuconsole.txt
  - zipbones.txt
- diff060418.txt
- doc
  - Makefile
  - remotefpga.odt
  - remotefpga.pdf
  - src
    - gpl-3.0.tex
  - zipcpu.odt
  - zipcpu.pdf
- Makefile
- mkdatev.pl
- README.md
- rtl
  - basic
    - blinky.bin
    - blinky.pcf
    - blinky.v
    - clktest.bin

- *clktest.pcf*
- *clktest.v*
- *dimmer.bin*
- *dimmer.pcf*
- *dimmer.v*
- *Makefile*
- *notes.txt*
- *pmodtest.bin*
- *pmodtest.pcf*
- *pmodtest.v*
- *catzip*
  - *auto.mk*
  - *builddate.v*
  - *catzip.pcf*
  - *cpu*
    - *busdelay.v*
    - *cpudefs.v*
    - *cpuops.v*
    - *dblfetch.v*
    - *div.v*
    - *icontrol.v*
    - *idecode.v*
    - *memops.v*
    - *pfcache.v*
    - *pipemem.v*
    - *prefetch.v*
    - *wbarbiter.v*
    - *wdbblpriarb.v*
    - *wbamac.v*
    - *wbpriarbiter.v*
    - *wbwatchdog.v*
    - *zipbones.v*
    - *zipcounter.v*
    - *zipcpu.v*
    - *zipjiffies.v*
    - *zipsystem.v*
    - *ziptimer.v*
  - *cpudefs.h*
  - *dbg.png*
  - *design.h*
  - *flashconfig.v*
  - *hdr.png*
  - *icozip.pcf*
  - *leds.png*
  - *main.v*
  - *Makefile*
  - *memdev.v*
  - *obj-arm*
    - *Vmain\_\_ALL.a*
    - *Vmain\_\_ALLcls.cpp*
    - *Vmain\_\_ALLcls.d*
    - *Vmain\_\_ALLcls.o*

- Vmain\_\_ALLsup.cpp
- Vmain\_\_ALLsup.d
- Vmain\_\_ALLsup.o
- Vmain\_classes.mk
- Vmain.cpp
- Vmain\_\_Dpi.cpp
- Vmain\_\_Dpi.h
- Vmain.h
- Vmain.mk
- Vmain\_\_Syms.cpp
- Vmain\_\_Syms.h
- Vmain\_\_Trace.cpp
- Vmain\_\_Trace\_\_Slow.cpp
- Vmain\_\_ver.d
- Vmain\_\_verFiles.dat

- pbsw.png
- rtcdate.v
- rxuartlite.v
- rxuart.v
- simple.log
- spio.v
- sw.png
- testmain.v
- toplevel.v
- txuartlite.v
- txuart.v
- ufifo.v
- wbgpio.v
- wbpwmaudio.v
- wbqspiflash.v
- wbscopc.v
- wbscope.v
- wbubus

- wbconsole.v
- wbubus.v
- wbucompactlines.v
- wbucompress.v
- wbuconsole.v
- wbudecompress.v
- wbudeword.v
- wbuexec.v
- wbufifo.v
- wbuidleint.v
- wbuinput.v
- wbuoutput.v
- wbureadcw.v
- wbusixchar.v
- wbutohex.v

- clktest.asc

- hexbus

- console.v
- hbbus.v

- **hbconsole.v**
- **hbdechex.v**
- **hbdeword.v**
- **hbexec.v**
- **hbgenhex.v**
- **hbidle.v**
- **hbints.v**
- **hbnewline.v**
- **hbpack.v**
- **leddigits**
  - **leddigits.pcf**
  - **leddigits.v**
  - **Makefile**
- **Makefile**
- **pmodleds**
  - **ledbouncer.pcf**
  - **ledbouncer.v**
  - **ledwalker.pcf**
  - **ledwalker.v**
  - **Makefile**
- **pport**
  - **ppio.v**
  - **pport.v**
  - **ufifo.v**
  - **wbpport.v**
- **pptest**
  - **hellopp.bin**
  - **hellopp.blif**
  - **hellopp.pcf**
  - **hellopp.v**
  - **linepp.bin**
  - **linepp.blif**
  - **linepp.pcf**
  - **linepp.v**
  - **Makefile**
  - **speech.hex**
  - **speechpp.bin**
  - **speechpp.blif**
  - **speechpp.pcf**
  - **speechpp.v**
- **sdram**
  - **Makefile**
  - **sdram.pcf**
  - **sdram.v**
- **switch\_leds**
  - **Makefile**
  - **switch\_leds.pcf**
  - **switch\_leds.v**
- **uart**
  - **helloworld.bin**
  - **helloworld.pcf**
  - **helloworld.v**

- *Makefile*
- *notwkg\_speechfifo.png*
- *README.md*
- *speechfifo.bin*
- *speechfifo.pcf*
- *speechfifo.v*
- *speechfifo.v.notwkg*
- *speechfifo.v.wkg*
- *speech.hex*
- *wkg\_speechfifo.png*
- *sim*
  - *verilated*
    - *automaster\_tb.cpp*
    - *byteswap.cpp*
    - *byteswap.h*
    - *dblpipecmdr.cpp*
    - *dblpipecmdr.h*
    - *hellopp.cpp*
    - *linepp.cpp*
    - *main\_tb.cpp*
    - *Makefile*
    - *memsim.cpp*
    - *memsim.h*
    - *obj-arm*
      - *depends.txt*
      - *verilated.o*
      - *verilated\_vcd\_c.o*
      - *xdepends.txt*
    - *port.h -> ../../sw/host/port.h*
    - *pportsim.cpp*
    - *pportsim.h*
    - *qspiflashsim.cpp*
    - *qspiflashsim.h*
    - *regdefs.h*
    - *speechpp.cpp*
    - *tags*
    - *tbclock.h*
    - *testb.h*
    - *twoc.cpp*
    - *twoc.h*
    - *uartsim.cpp*
    - *uartsim.h*
    - *zipelf.cpp*
    - *zipelf.h*
- *sim-err.txt*

Initial testing

06/05/18

cd catzip/rtl/catzip

```
sudo config_cat catzip.bin This programs the FPGA
```

```
cd catzip/sw/host
```

```
./arm-netpport
```

```
Listening on port 8363
```

```
Listening on port 8364
```

```
cd catzip/sw/host
```

```
./arm-wbregs version
```

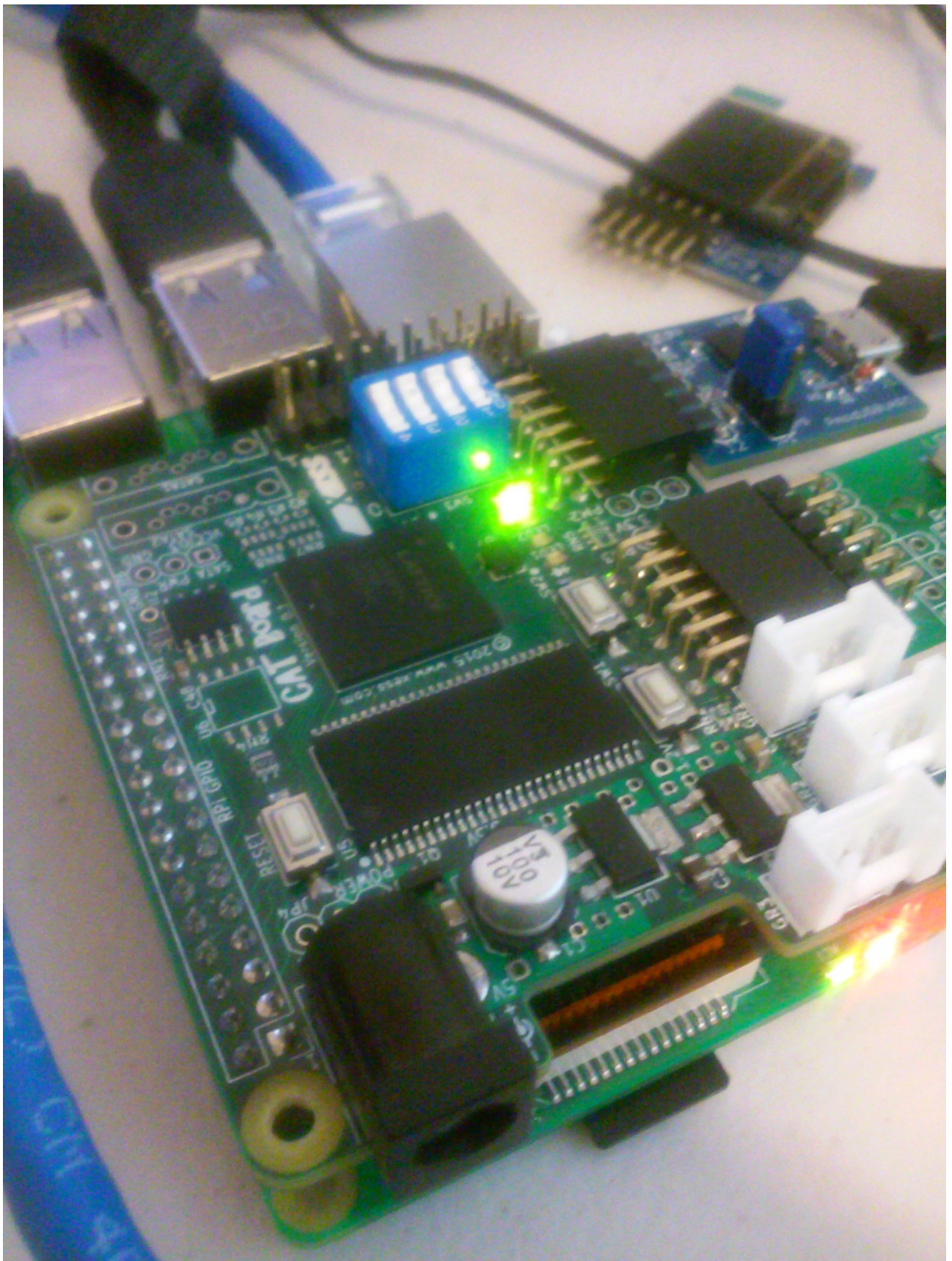
```
00001010 ( VERSION) : [....] 20180605
```

```
1st Led on
```

```
/arm-wbregs gpio 0x00010001
```

```
00001008 ( GPIO)-> 00010001
```





1st Led off

```
./arm-wbregs gpio 0x00010000
```

```
00001008 ( GPIO)-> 00010000
```

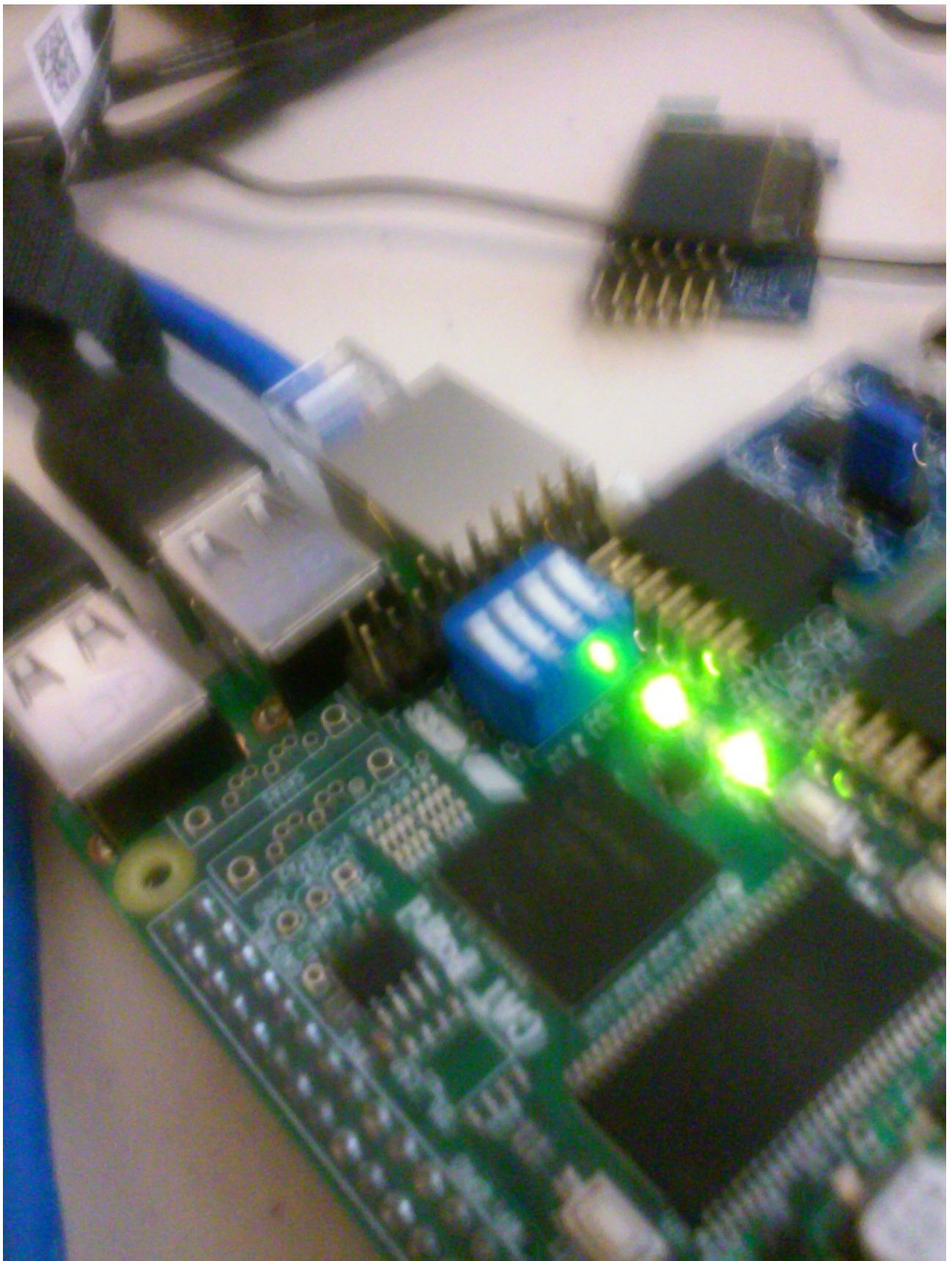
2n led on

```
./arm-wbregs gpio 0x00020002
```

```
00001008 ( GPIO)-> 00020002
```







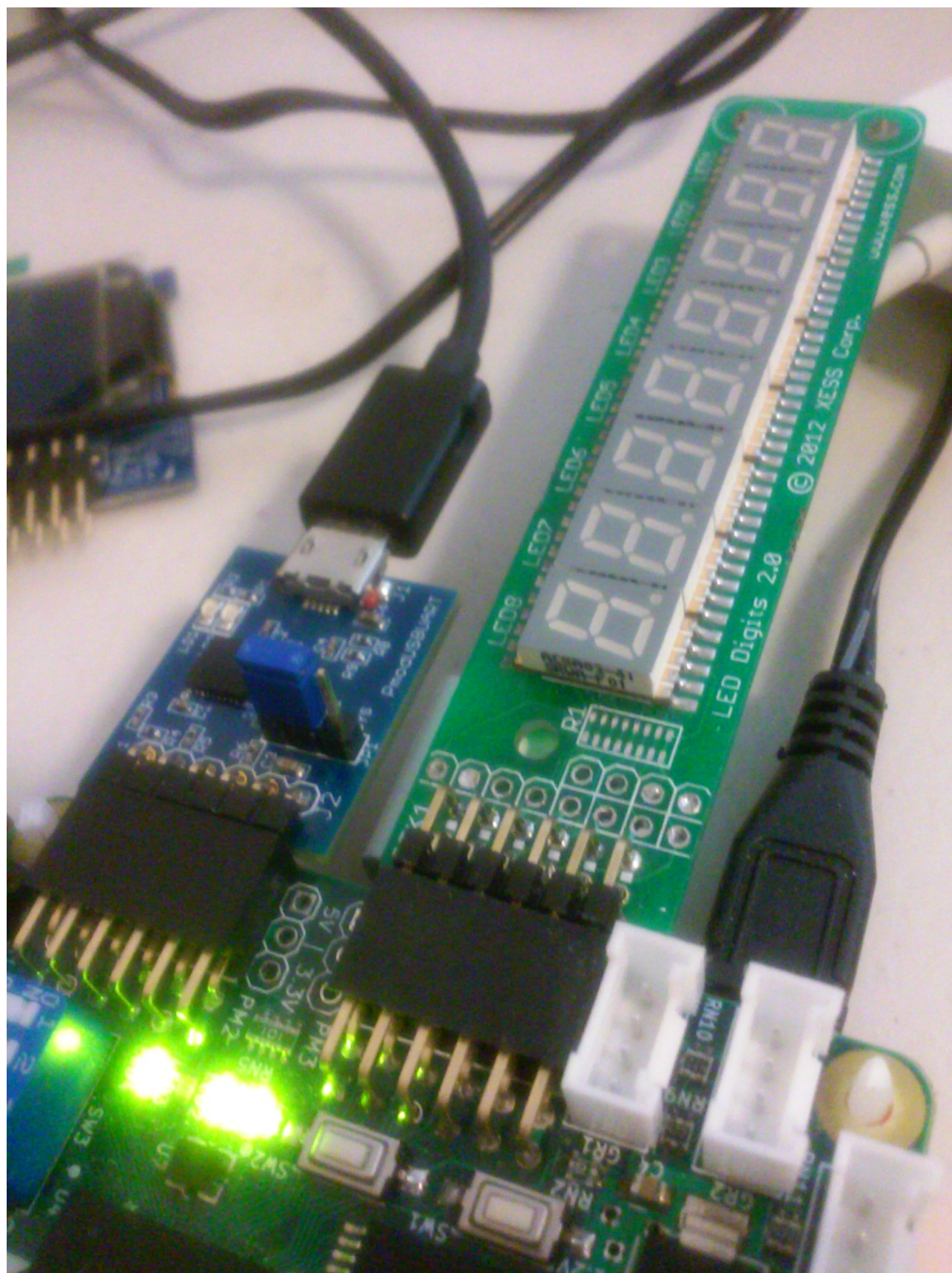
2nd led off

```
./arm-wbregs gpio 0x00020000  
00001008 ( GPIO)-> 00020000
```

3<sup>rd</sup> led on

```
./arm-wbregs gpio 0x00040004  
00001008 ( GPIO)-> 00040004
```





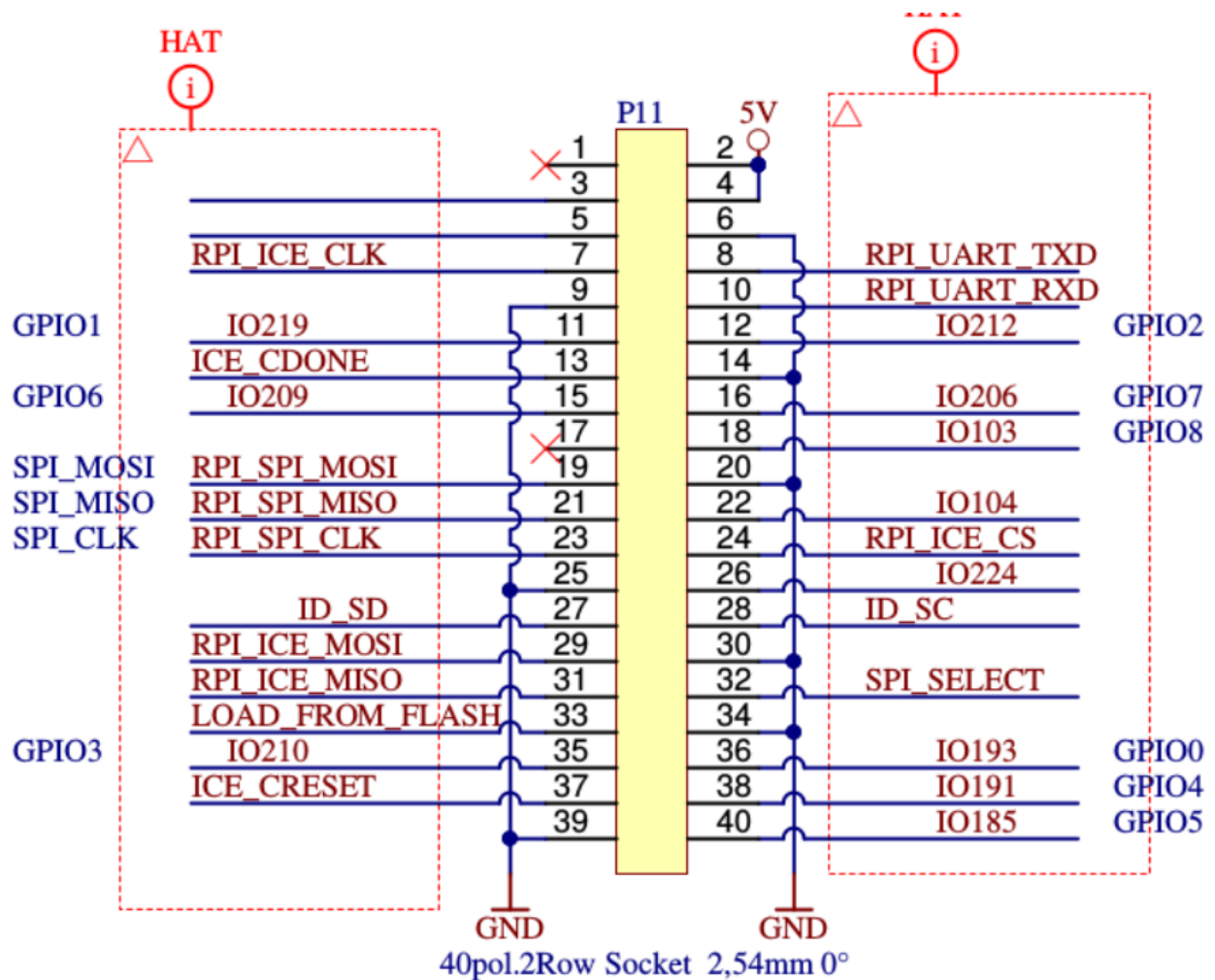
3<sup>rd</sup> led off

```
./arm-wbregs gpio 0x00040000  
00001008 ( GPIO)-> 00040000
```

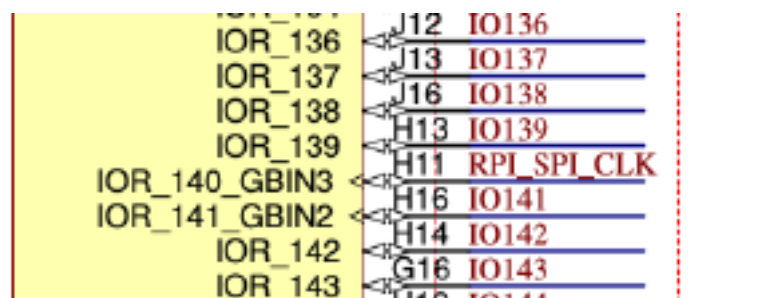
```
./arm-wbregs 0x2000 0x01  
00002000 ( RAM)-> 00000001  
pi@pi3-5:~/catzip/sw/host $ ./arm-wbregs ram  
00002000 ( RAM) : [...] 00000001  
pi@pi3-5:~/catzip/sw/host $ ./arm-wbregs 0x2000 0x02  
00002000 ( RAM)-> 00000002  
pi@pi3-5:~/catzip/sw/host $ ./arm-wbregs ram  
00002000 ( RAM) : [...] 00000002
```

```
./arm-wbregs pic  
00001004 ( PIC) : [...] 00000003
```

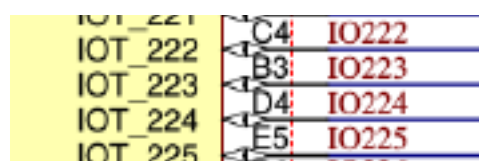
```
./arm-wbregs ufifo  
00000804 ( UFIFO) : [ @?@. ] 403f4000  
ICOBBOARD RPi
```



RPI\_SPI\_CLK H11 Pin 23 Pi icoboard

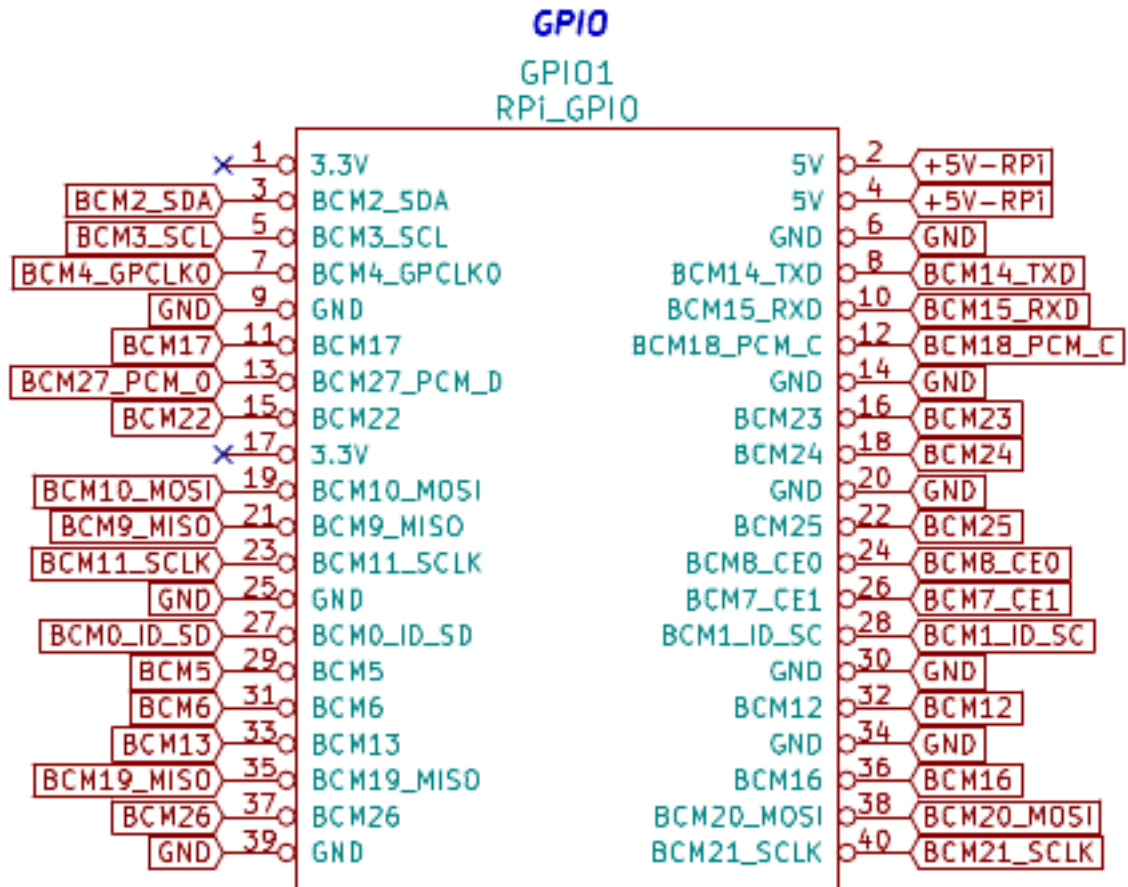


rpi\_cs D4 IOT\_224 Pin 26 Pi icoboard



CATBOARD RPi



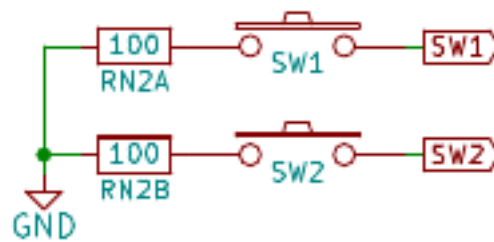


CATBOARD connection to FPGA pins PMOD 2 & PMOD 3 push button switches, dip switch, and leds.

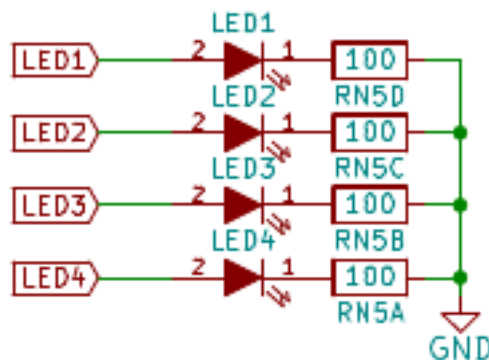


GR3-IO1	C14	IOT_168
PM3-A4	B15	IOT_169
PM3-A3	D13	IOT_170
GR2-IO1	B14	IOT_171
GR2-IO1	C12	IOT_172
GR3-IO2	E11	IOT_173
SW1	C13	IOT_174
PM3-B4	A16	IOT_176
PM3-B3	A15	IOT_177
PM3-B3	B13	IOT_178
GR2-IO2	E10	IOT_179
GR2-IO2	C11	IOT_180
PM3-A2	D11	IOT_181
PM3-B1	B12	IOT_182
PM3-B1	B10	IOT_183
PM3-B2	B11	IOT_184
GR1-IO1	C10	IOT_185
PM3-A1	A10	IOT_186
PM3-A1	A11	IOT_187
GR1-IO2	D10	IOT_190
GR1-IO2	C9	IOT_191
GR1-IO2	E9	IOT_192
LED1	D9	IOT_193
LED1	A9	IOT_194
LED1	F9	IOT_196
USER_CLK	C8	IOT_197_GBIN1
SW2	F7	IOT_198_GBIN0
SW2	B9	IOT_199
LED2	D8	IOT_200
LED2	B8	IOT_203
LED3	A7	IOT_205
LED3	C7	IOT_206
LED4	B7	IOT_207
PM2-A4	B6	IOT_208
DIPSW1	C6	IOT_209
PM2-B4	D7	IOT_210
PM2-B4	A6	IOT_211
PM2-B3	D6	IOT_212
PM2-B3	A5	IOT_213
PM2-A3	B5	IOT_214
PM2-A3	E6	IOT_215
PM2-B2	B4	IOT_216
PM2-B1	A2	IOT_218
PM2-A1	D5	IOT_219
DIPSW2	C5	IOT_220
DIPSW3	C4	IOT_221
PM2-A2	B3	IOT_222
PM2-A2	D4	IOT_223
PM2-A2	D4	IOT_224
DIPSW4	C3	IOT_225
DIPSW4	D3	IOT_226
+3.3V	A13	IOT_227
		VCCIO_0[4]

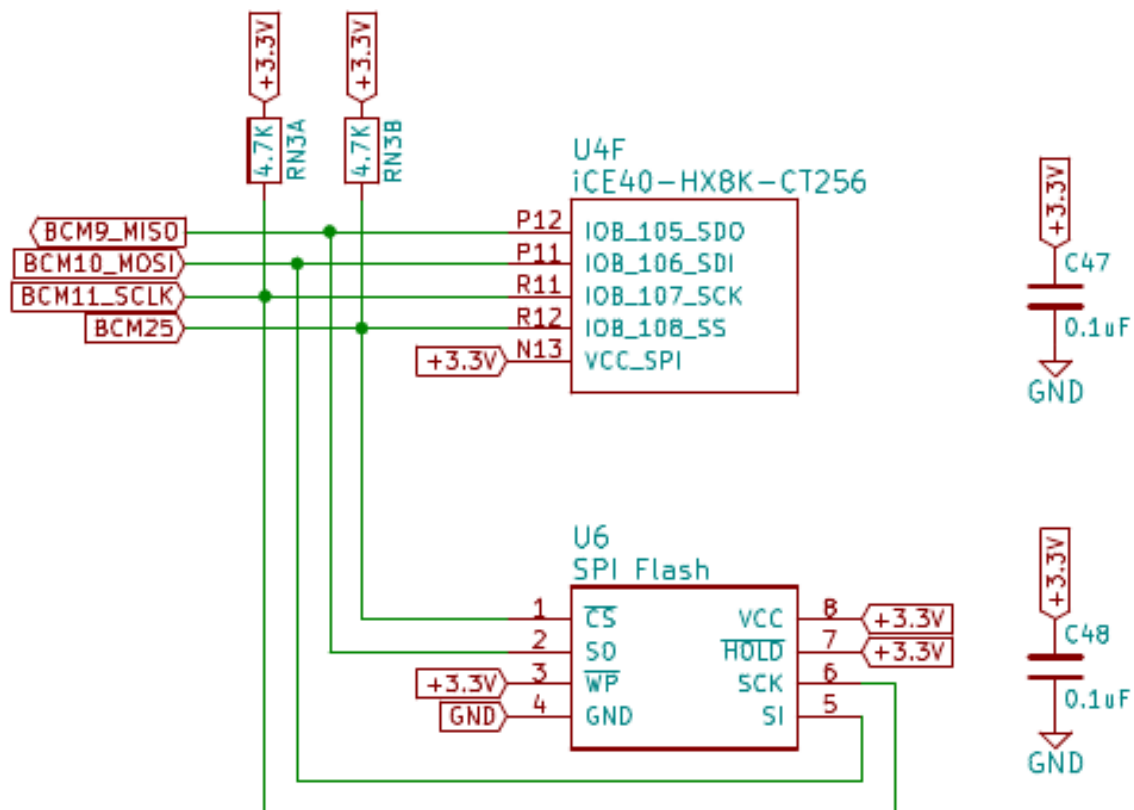
CATBOARD sw1 & sw2



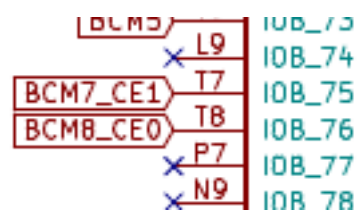
CATBOARD leds



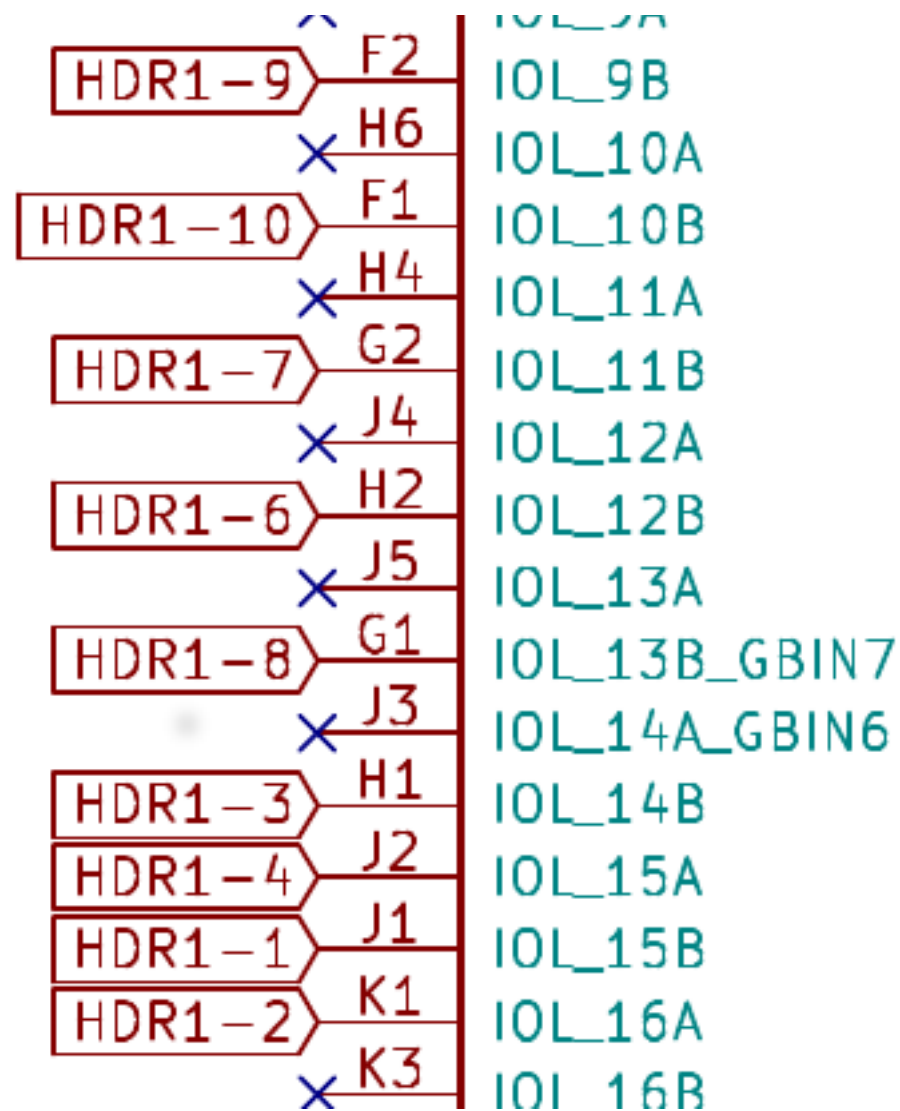
BCM11\_SCLK Pin 23 CATBOARD



BCM7\_CE1 Pin 26 CATBOARD



CATBOARD



- 2.) The 2<sup>nd</sup> issue is the PMOD connections to FPGA are different.
- 3.) Third, I do not have a Digilent PMOD 4 push button switch module.
- 4.) The 4<sup>th</sup> issue is the PHASE LOCK LOOP difference.

Post on #yosys

*Pin C8 is my USER\_CLK comes from a 100MHz osc. It is connected to IOT\_197\_GBIN1 on HX8K. When I try using it for as an input to PLL I get the fatal error: bad constraint on `i\_clk': no PLL at pin C8.*

*Can only certain pins be used as inputs to PLL?*

*daveshah*

*develonepi3: use the SB\_PLL40\_CORE instead of SB\_PLL40\_PAD variant (and REFERENCECLK in instead of PACKAGEPIN)*

```
set_io clk_100mhz C8 #R9
```

```
set_io pmod1_1 A11 #D8
```

```
set_io pmod1_2 B12 #B9
```

```
set_io pmod1_3 B14 #B10
```

```
set_io pmod1_4 B15 #B11
```

```
# 654321 catboard # 654321 icoboard
```

```
# xxxxxx PMOD3 A # xxxxxx PMOD1 A
```

```
# xxxxxx PMOD3 B # xxxxxx PMOD1 B
```

```
# 654321 # 654321
```

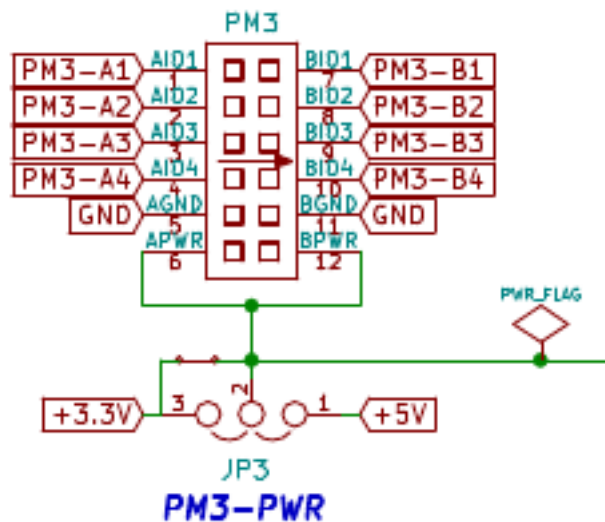
```
#
```

```
set_io pmod1_7 B10 #B8
```

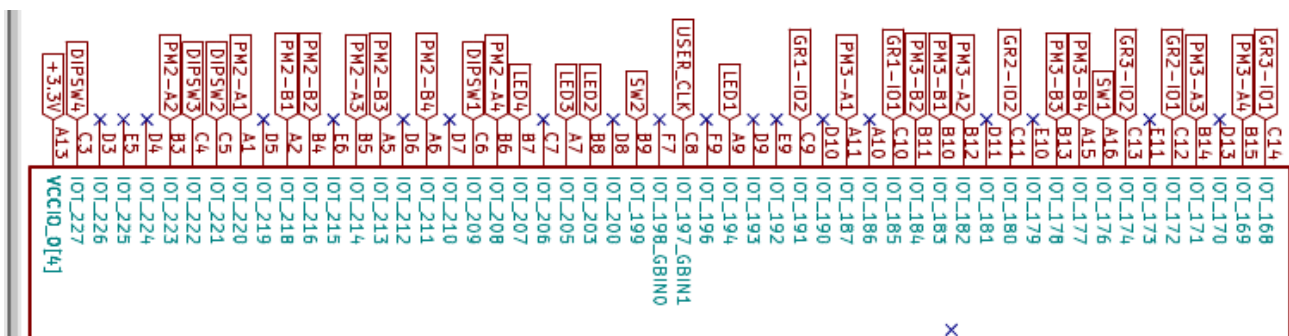
```
set_io pmod1_8 B11 #A9
```

```
set_io pmod1_9 B13 #A10
```

```
set_io pmod1_10 A15 #A11
```



CATBOARD connection to FPGA pins PMOD 2 & PMOD 3 push button switches, dip switch, and leds.



In top.v

```
module top(clk_100mhz, pmod1_1, pmod1_2, pmod1_3, pmod1_4, pmod1_7, pmod1_8,  
  pmod1_9, pmod1_10, pmod2_7, pmod2_8, pmod2_9, pmod2_10, rpi_sck, rpi_cs,  
  rpi_mosi);
```

```
input rpi_sck, rpi_cs, rpi_mosi;
```

```
rpi_sck
```

```
rpi_cs
```

```
rpi_mosi
```

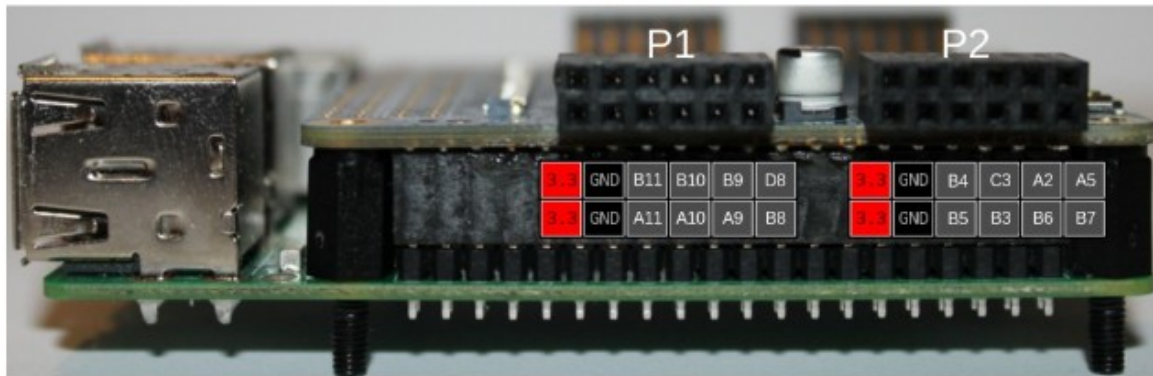
```
spi_ram_slave spi_ram_slave(clk, rpi_sck, rpi_cs, rpi_mosi,
```

```
  ram_addr, ram_data, ram_wr);
```

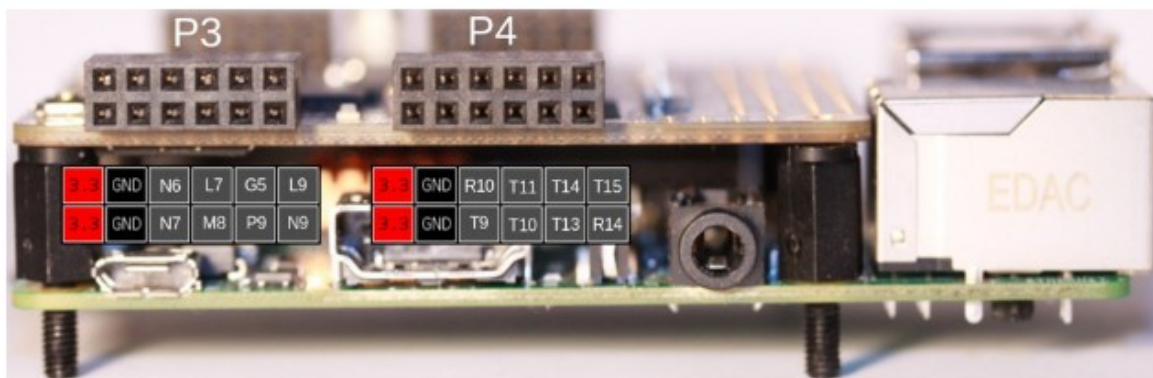
```
module spi_ram_slave(clk, sck, cs, mosi, ram_addr, ram_data, ram_wr);
```

```
PMOD pin out on icoboard
```

Pinout Pmod P1 and P2



Pinout PMOD P3 and P4



```
"lrwxrwxrwx 1 root staff 34 May 18 20:10 /usr/local/bin/config_cat ->
/home/pi/catboard_yosys/config_cat"
```

```
#!/bin/bash
```

```
# A script to configure Lattice iCE40 FPGA by SPI from Raspberry Pi
#
# Copyright (C) 2015 Jan Marjanovic <jan@marjanovic.pro>
#
# This program is free software: you can redistribute it and/or modify
# it under the terms of the GNU General Public License as published by
# the Free Software Foundation, either version 3 of the License, or
# (at your option) any later version.
#
# This program is distributed in the hope that it will be useful,
# but WITHOUT ANY WARRANTY; without even the implied warranty of
# MERCHANTABILITY or FITNESS FOR A PARTICULAR PURPOSE. See the
# GNU General Public License for more details.
#
# You should have received a copy of the GNU General Public License
# along with this program. If not, see <http://www.gnu.org/licenses/>.
```

```
echo ""
```

```
if [ $# -ne 1 ]; then
    echo "Usage: $0 FPGA-bin-file "
    exit 1
fi
```

```
if [ $EUID -ne 0 ]; then
    echo "This script must be run as root" 1>&2
    exit 1
fi
```

```
if [ ! -d /sys/class/gpio/gpio25 ]; then
    echo "GPIO 25 not exported, trying to export..."
    echo 25 > /sys/class/gpio/export
    if [ ! -d /sys/class/gpio/gpio25 ]; then
        echo "ERROR: directory /sys/class/gpio/gpio25 does not exist"
        exit 1
    fi
else
    echo "OK: GPIO 25 exported"
fi
```

```
if [ ! -d /sys/class/gpio/gpio17 ]; then
    echo "GPIO 17 not exported, trying to export..."
    echo 17 > /sys/class/gpio/export
    if [ ! -d /sys/class/gpio/gpio17 ]; then
        echo "ERROR: directory /sys/class/gpio/gpio17 does not exist"
        exit 1
    fi
fi
```



```

    fi
else
    echo "OK: GPIO 17 exported"
fi

if [ ! -d /sys/class/gpio/gpio22 ]; then
    echo "GPIO 22 not exported, trying to export..."
    echo 22 > /sys/class/gpio/export
    if [ ! -d /sys/class/gpio/gpio22 ]; then
        echo "ERROR: directory /sys/class/gpio/gpio22 does not exist"
        exit 1
    fi
else
    echo "OK: GPIO 22 exported"
fi

echo ""
if [ -e /dev/spidev0.0 ]; then
    echo "OK: SPI driver loaded"
else
    echo "spidev does not exist"

    lsmod | grep spi_bcm2708 >& /dev/null

    if [ $? -ne 0 ]; then
        echo "SPI driver not loaded, try to load it..."
        modprobe spi_bcm2708

        if [ $? -eq 0 ]; then
            echo "OK: SPI driver loaded"
        else
            echo "Could not load SPI driver"
            exit 1
        fi
    fi
fi

echo ""
echo "Setting GPIO directions"
echo out > /sys/class/gpio/gpio25/direction
cat /sys/class/gpio/gpio25/direction
echo out > /sys/class/gpio/gpio22/direction
cat /sys/class/gpio/gpio22/direction
echo in > /sys/class/gpio/gpio17/direction
cat /sys/class/gpio/gpio17/direction

echo "Setting output to low"
echo 0 > /sys/class/gpio/gpio25/value
cat /sys/class/gpio/gpio25/value

#echo ""
#echo "Please reset the iCE40 FPGA board"

```

```
#echo "Press any key..."  
#read
```

```
echo "Reseting FPGA"  
echo 0 > /sys/class/gpio/gpio22/value  
cat /sys/class/gpio/gpio22/value  
echo 1 > /sys/class/gpio/gpio22/value  
cat /sys/class/gpio/gpio22/value
```

```
echo "Checking DONE pin"  
cat /sys/class/gpio/gpio17/value
```

```
echo "Continuing with configuration procedure"  
dd if=$1 of=/dev/spidev0.0
```

```
echo -e "\x0\x0\x0\x0\x0\x0\x0" > /dev/spidev0.0
```

```
echo "Setting output to high"  
echo 1 > /sys/class/gpio/gpio25/value  
cat /sys/class/gpio/gpio25/value
```

```
echo "Checking DONE pin"  
cat /sys/class/gpio/gpio17/value
```

```
"cd otl-icoboard-pmodeledrgb-demo/stream-tool/"
```

```
"ffmpeg -f v4l2 -i /dev/video0 -s 96x64 -f rawvideo -pix_fmt rgb565 - | ./stream-tool"
```