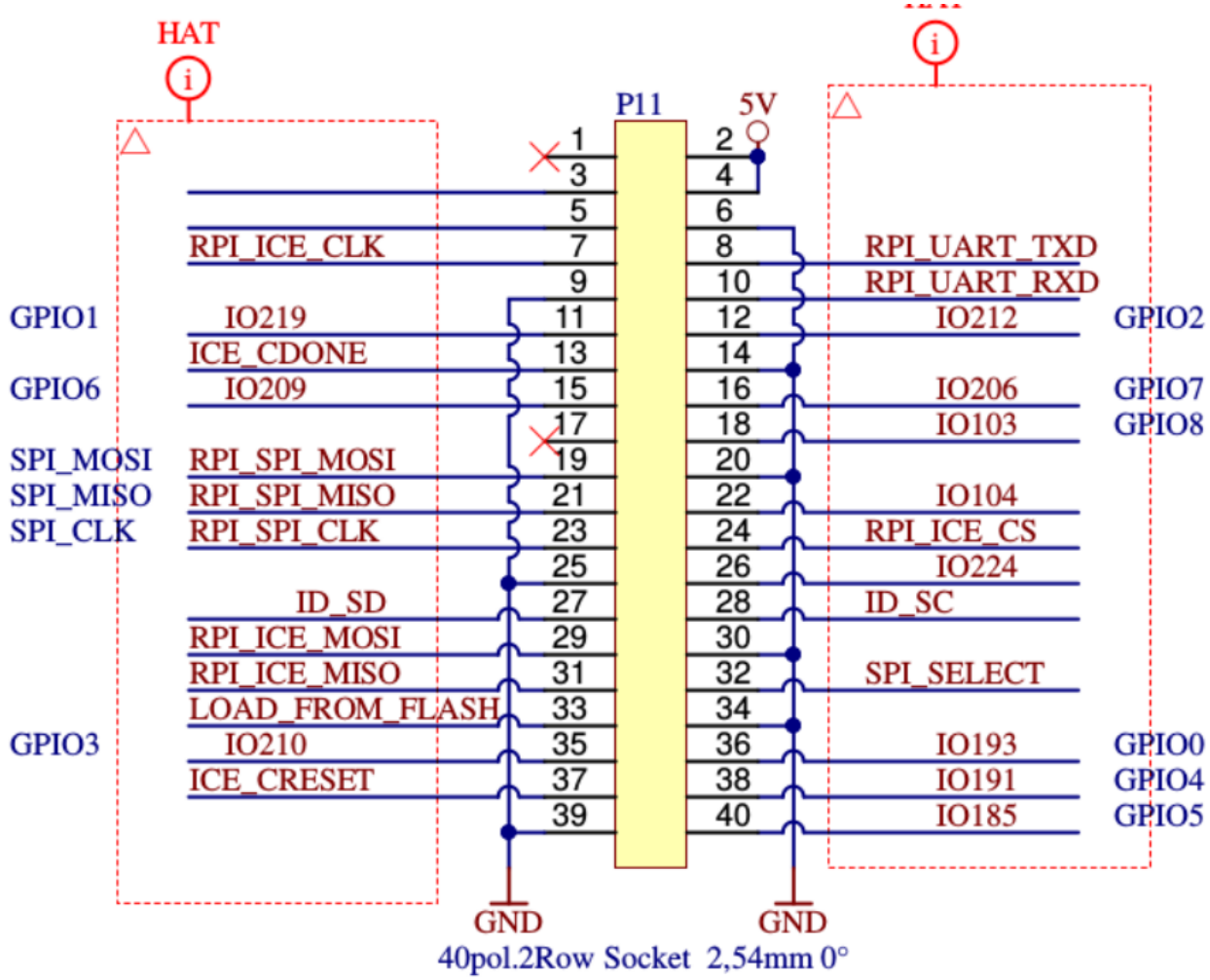
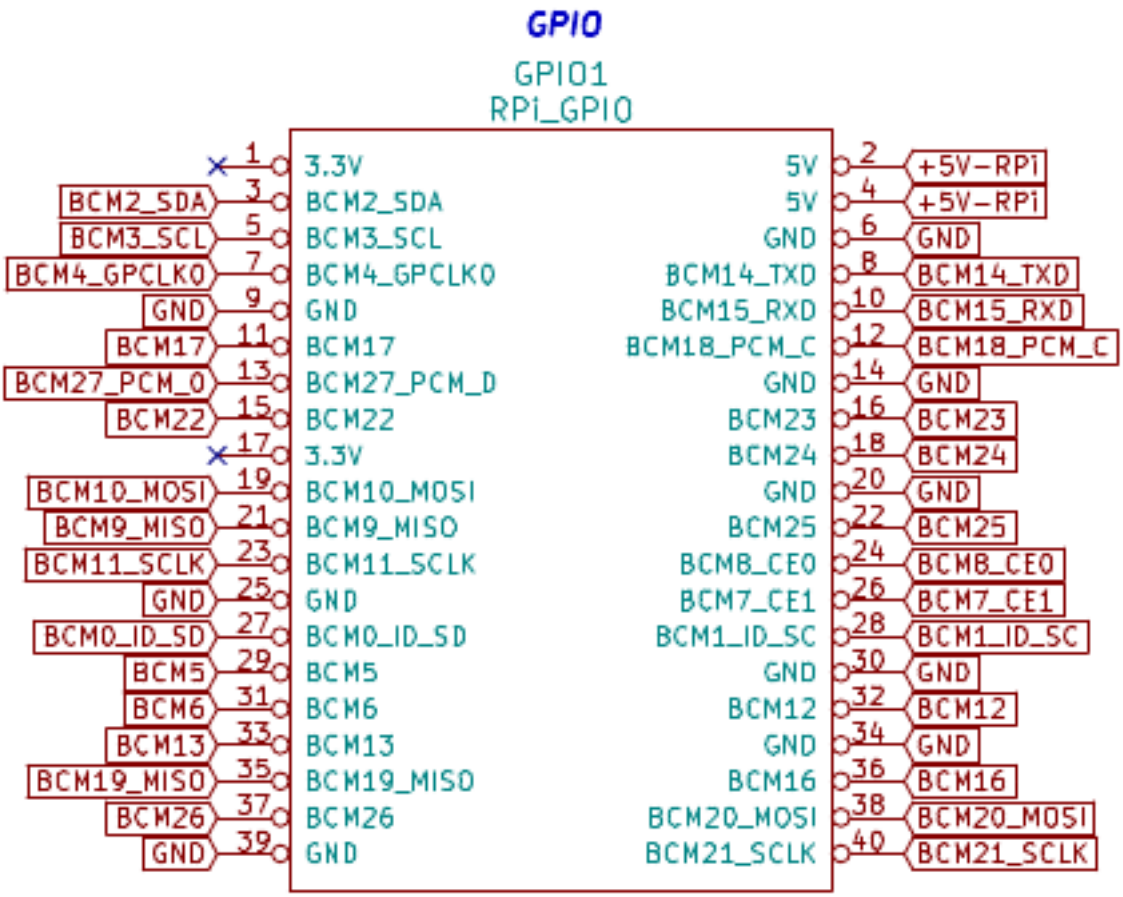
Testing Verilog on the CATBOARD
on RPi Zero with CATBOARD
05/18/18

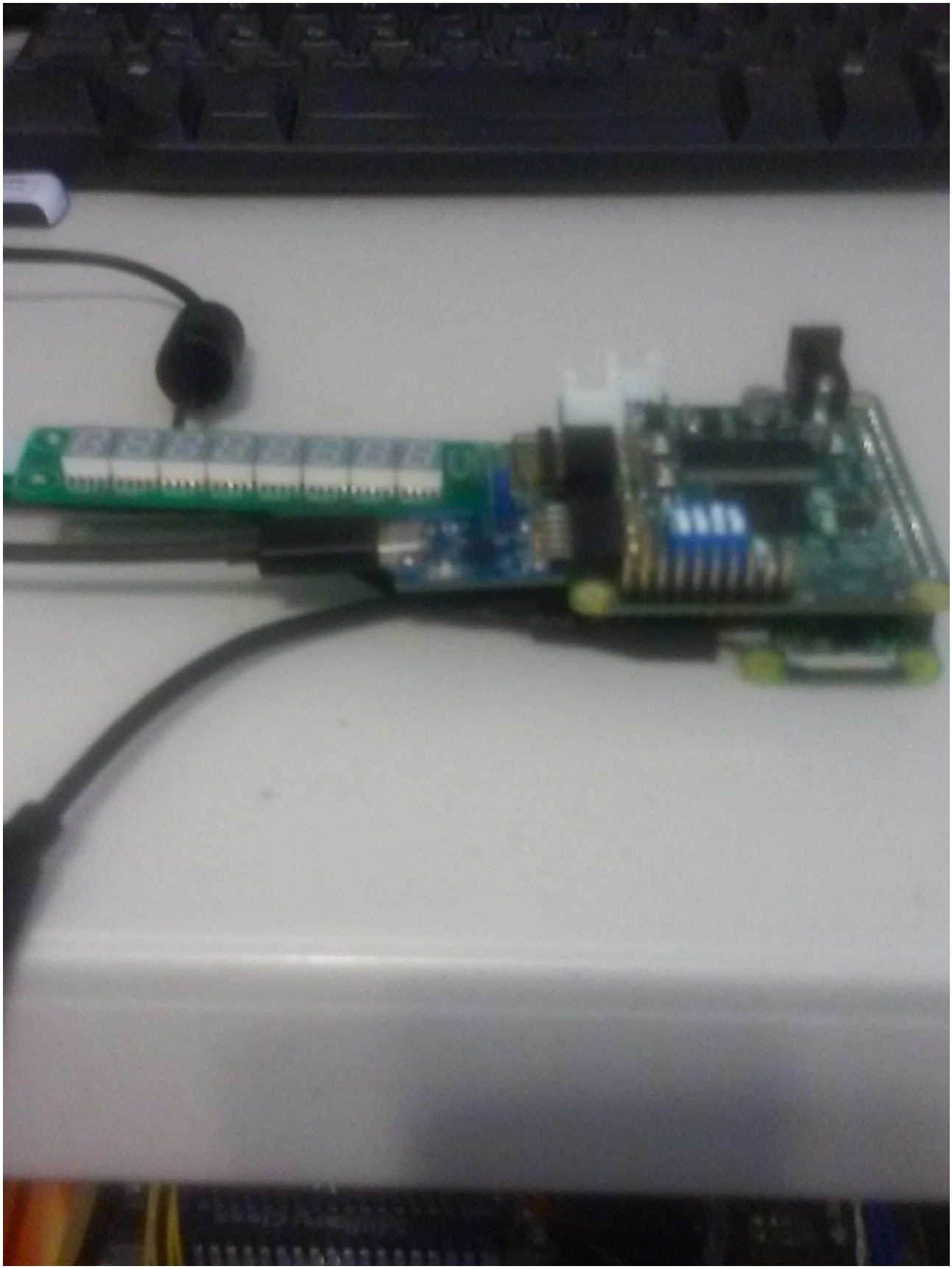
A Pizero with CATBOARD FPGA. The CATBOARD provides 2 PMOD connector and a 20 pin with 3.3 v & Grd and 18 I/Os.

ICOBARD RPI



CATBOARD RPI


GPIO
GPIO1
RPi_GPIO
1
3.3V
3
BCM2_SDA
BCM2_SDA
5
BCM3_SCL
BCM3_SCL
7
BCM4_GPCLK0
BCM4_GPCLK0
9
GND
GND
11
BCM17
BCM17
13
BCM27_PCM_D
BCM27_PCM_D
15
BCM22
BCM22
17
3.3V
19
BCM10_MOSI
BCM10_MOSI
21
BCM9_MISO
BCM9_MISO
23
BCM11_SCLK
BCM11_SCLK
25
GND
GND
27
BCM0_ID_SD
BCM0_ID_SD
29
BCM5
BCM5
31
BCM6
BCM6
33
BCM13
BCM13
35
BCM19_MISO
BCM19_MISO
37
BCM26
BCM26
39
GND
GND
2
5V
+5V-RPi
4
5V
+5V-RPi
6
GND
GND
8
BCM14_TXD
BCM14_TXD
10
BCM15_RXD
BCM15_RXD
12
BCM18_PCM_C
BCM18_PCM_C
14
GND
GND
16
BCM23
BCM23
18
BCM24
BCM24
20
GND
GND
22
BCM25
BCM25
24
BCM8_CE0
BCM8_CE0
26
BCM7_CE1
BCM7_CE1
28
BCM1_ID_SC
BCM1_ID_SC
30
GND
GND
32
BCM12
BCM12
34
GND
GND
36
BCM16
BCM16
38
BCM20_MOSI
BCM20_MOSI
40
BCM21_SCLK
BCM21_SCLK



Using a Pizero to program the FPGA.
Most of Verilog was written by Dan Gisselquist, Ph.D. from Gisselquist Technology, LLC. He is working with the ICOBARD which is a HX8K Lattice FPGA like the CATBOARD. The Verilog and C++ software is found at

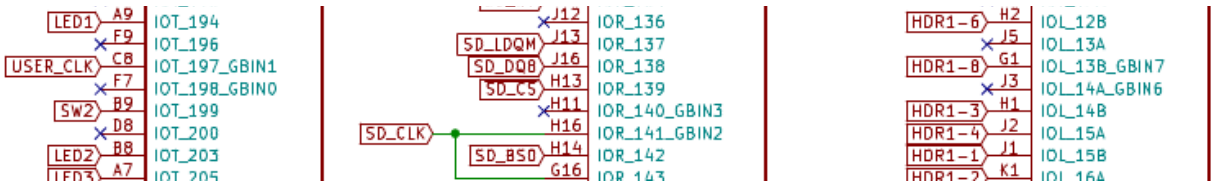
URL: https://github.com/develone/catzip.git

```
File  Edit  Tabs  Help
1
pi@pizero-1:~/catzip/rtl $ sudo config_cat pptest/speechpp.bin

OK: GPIO 25 exported
OK: GPIO 17 exported
OK: GPIO 22 exported

OK: SPI driver loaded

Setting GPIO directions
out
out
in
Setting output to low
0
Reseting FPGA
0
1
Checking DONE pin
0
Continuing with configuration procedure
263+1 records in
263+1 records out
135100 bytes (135 kB, 132 KiB) copied, 0.108344 s, 1.2 MB/s
Setting output to high
1
Checking DONE pin
1
pi@pizero-1:~/catzip/rtl $
```

In the speechpp.pcf set_io i_clk R9. Pin R9 on the icoboard ICE_CLK is connected to IOB_81_GBIN5 on the right side of the image below.

Trying to chg set_io i_clk R9 # 100 MHz clock
To C8 USER_CLK was causing the following error
fatal error: bad constraint on 'i_clk': no PLL at pin C8

Post on #yosys
Pin C8 is my USER_CLK comes from a 100MHz osc. It is connected to IOT_197_GBIN1 on HX8K. When I try using it for as an input to PLL I get the fatal error: bad constraint on `i_clk': no PLL at pin C8.
Can only certain pins be used as inputs to PLL?
daveshah
develonepi3: use the SB_PLL40_CORE instead of SB_PLL40_PAD variant (and REFERENCECLK in instead of PACKAGEPIN)
on the left side of the image below.



The verison of speechpp.bin uses a PPL to reduce the 100MHz Oscilator down to 66MHz.

```
wire    clk_66mhz, pll_locked;
SB_PLL40_CORE #(
        .FEEDBACK_PATH("SIMPLE"),
        .DELAY_ADJUSTMENT_MODE_FEEDBACK("FIXED"),
        .DELAY_ADJUSTMENT_MODE_RELATIVE("FIXED"),
        .PLLOUT_SELECT("GENCLK"),
        .FDA_FEEDBACK(4'b1111),
        .FDA_RELATIVE(4'b1111),
        .DIVR(4'd8),          // Divide by (DIVR+1)
        .DIVQ(3'd4),          // Divide by 2^(DIVQ)
        .DIVF(7'd94),         // Multiply by (DIVF+1)
        .FILTER_RANGE(3'b001)
) plli (
        .REFERENCECLK   (i_clk       ),
        .PLLOUTCORE     (clk_66mhz   ),
        .LOCK           (pll_locked  ),
```

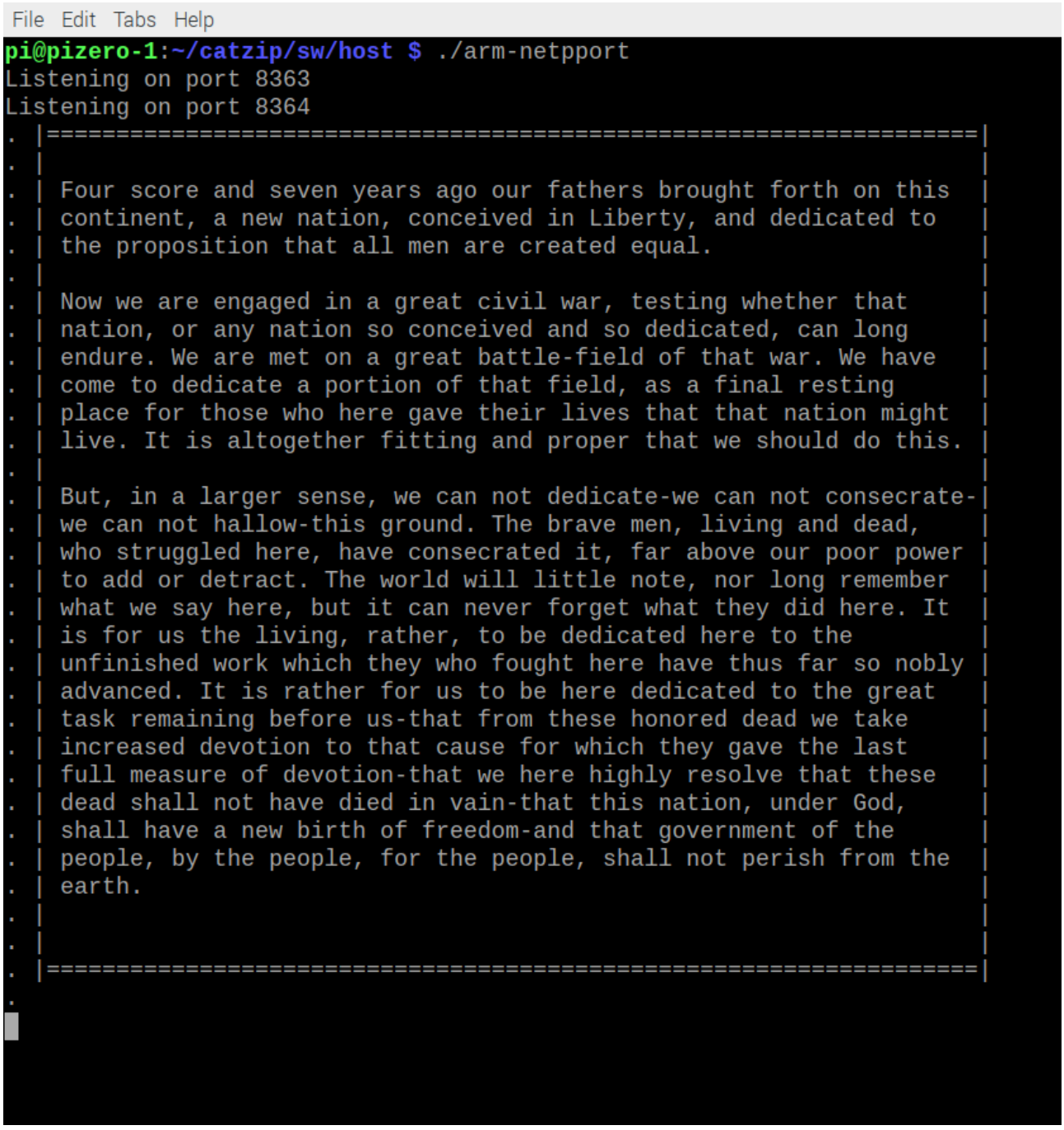
```
        .BYPASS     (1'b0     ),
        .RESETB     (1'b1     )
    );
    assign  s_clk = clk_66mhz;
```

The ICOBOARD used ***SB_PLL40_PAD since a different GBIN was used,***

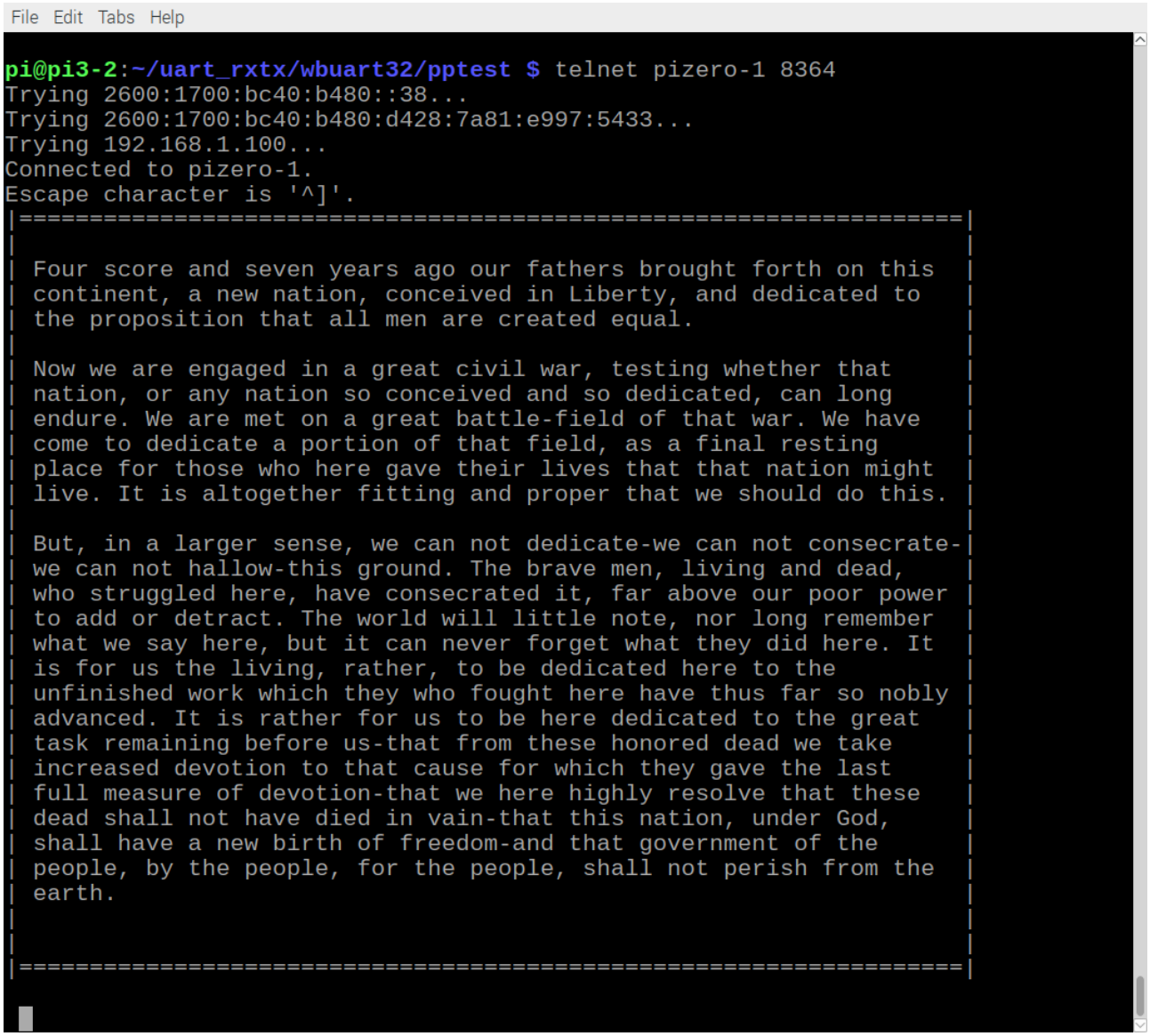
Running ***"arm-netpport"*** on pizero-1 which receives the data from the FPGA in parallel using 11 gpio pins
Maps pins on FPGA to Pins on Rpi. These pins were different on the ICOBOARD.

```
set_io i_clk    C8

set_io o_ledg[0] A9
set_io o_ledg[1] B8
set_io o_ledr   B7

set_io  i_pp_dir    R3
set_io  i_pp_clk    T8

set_io io_pp_data[0] R4
set_io io_pp_data[1] T3
set_io io_pp_data[2] T13
set_io io_pp_data[3] T6
set_io io_pp_data[4] T5
set_io io_pp_data[5] P9
set_io io_pp_data[6] T9
set_io io_pp_data[7] T11

set_io o_pp_clkfb   T7

#  define RASPI_DIR 28 //BCM20  PIN 38, GPIO.28 IOB_59  R3
#  define RASPI_CLK 10 //BCM8   PIN 24, GPIO.10, IOB_75 T8

#  define RASPI_D0 27 //BCM16   PIN 36, GPIO.27, IOB_63 R4
#  define RASPI_D1 24 //BCM19   PIN 35, GPIO.24, IOB_61 T3
#  define RASPI_D2 0 //BCM17    PIN 11, GPIO.0 ,IOB_94  T13

#  define RASPI_D3 21 //BCM5   PIN  29,GPIO.21 ,IOB_73  T6

#  define RASPI_D4 22 //BCM6    PIN 31,GPIO.22 ,IOB_69  T5
#  define RASPI_D5 4 //BCM23    PIN 16,GPIO.4, IOB_83   P9

#  define RASPI_D6 5 //BCM24    PIN 18, GPIO.5, IOB_79  T9
#  define RASPI_D7 1  //BCM18   pin 12, GPIO.1, IOB_89  T11
#  define RASPI_D8 11 //BCM7    PIN 26, GPIO.11, IOB_75 T7

#define READ_FROM_ICO   0
#define WRITE_TO_ICO    1
```

The file ***"speech.hex"*** is read by the FPGA and sent to the pizero.



In addition, a remote host, using telnet can receive the data being sent from the FPGA. The command ***"telnet pizero-1 8364***


File Edit Tabs Help
pi@pi3-2:~/uart_rxtx/wbuart32/pptest $ telnet pizero-1 8364
Trying 2600:1700:bc40:b480::38...
Trying 2600:1700:bc40:b480:d428:7a81:e997:5433...
Trying 192.168.1.100...
Connected to pizero-1.
Escape character is '^]'.
Four score and seven years ago our fathers brought forth on this continent, a new nation, conceived in Liberty, and dedicated to the proposition that all men are created equal.
Now we are engaged in a great civil war, testing whether that nation, or any nation so conceived and so dedicated, can long endure. We are met on a great battle-field of that war. We have come to dedicate a portion of that field, as a final resting place for those who here gave their lives that that nation might live. It is altogether fitting and proper that we should do this.
But, in a larger sense, we can not dedicate-we can not consecrate-we can not hallow-this ground. The brave men, living and dead, who struggled here, have consecrated it, far above our poor power to add or detract. The world will little note, nor long remember what we say here, but it can never forget what they did here. It is for us the living, rather, to be dedicated here to the unfinished work which they who fought here have thus far so nobly advanced. It is rather for us to be here dedicated to the great task remaining before us-that from these honored dead we take increased devotion to that cause for which they gave the last full measure of devotion-that we here highly resolve that these dead shall not have died in vain-that this nation, under God, shall have a new birth of freedom-and that government of the people, by the people, for the people, shall not perish from the earth.