

*****Default*****

Catboard-Pipelinec vga-pong
&
vga-pll
03/04/25

*****Default*****

This checkout of PipelineC repo was noted in the pico-ice repo on 02/17/25 and documented

<https://raw.githubusercontent.com/develone/pico-ice/refs/heads/test-dev-100424/myDocs/Pipelinec-rebuild-tests/built-files.txt>

```
devel@pi5-70:~/PipelineC $ git checkout 6161
```

Note: switching to '6161'.

You are in 'detached HEAD' state. You can look around, make experimental changes and commit them, and you can discard any commits you make in this state without impacting any branches by switching back to a branch.

If you want to create a new branch to retain commits you create, you may do so (now or later) by using -c with the switch command. Example:

```
git switch -c <new-branch-name>
```

Or undo this operation with:

```
git switch -
```

Turn off this advice by setting config variable advice.detachedHead to false

HEAD is now at 6161654 Merge branch 'JulianKemmerer:master' into test-dev

```
git clone https://github.com/develone/Catboard-Pipelinec.git
```

```
cd Catboard-Pipelinec/vga-pong/examples/pico-ice/
```

```
devel@pi5-70:~/Catboard-Pipelinec/vga-pong/examples/pico-ice/
```

```
ice_makefile_pipelinec
```

```
$ make clean
```

```
rm -f lextab.py
```

```
rm -f yacctab.py
```

```
rm -f pll_clk_mhz.h
```

```
rm -f -r pipelinec_output
```

```
rm -f pipelinec.log
```

```
rm -f pll.v
```

```
rm -f *.json *.asc *.bin *.uf2
```

```
rm -f yosys_stderr.log
rm -f dfu_util.log
devel@pi5-70:~/Catboard-PipelineC/vga-pong/examples/pico-ice/
ice_makefile_pipelinec $
```

```
make pipelinec
echo "#define PLL_CLK_MHZ 25.0\n" > pll_clk_mhz.h
/home/devel/PipelineC/src/pipelinec pong_top.c --top pipelinec_top --out_dir
pipelinec_output --comb --no_synth > pipelinec.log
devel@pi5-70:~/Catboard-PipelineC/vga-pong/examples/pico-ice/
ice_makefile_pipelinec $
```

```
make gateway.bin
/home/devel/oss-cad-suite/bin/icepll -q -i 100 -o 25.0 -m -f pll.v
/home/devel/oss-cad-suite/bin/yosys -l simple.log -q -m ghdl -p "ghdl --std=08 -
frelaxed `cat pipelinec_output/vhdl_files.txt` -e pipelinec_top; read_verilog -sv
top.sv pll.v; synth_ice40 -top top -json gateway.json" 2> yosys_stderr.log
/home/devel/oss-cad-suite/bin/nextpnr-ice40 -l nextpnr.log -q --randomize-seed
--hx8k --package ct256 --pcf ice40.pcf --json gateway.json --asc gateway.asc --
freq 25.0
/home/devel/oss-cad-suite/bin/icepack gateway.asc gateway.bin
devel@pi5-70:~/Catboard-PipelineC/vga-pong/examples/pico-ice/
ice_makefile_pipelinec $
```

```
rsync -avl --delete /home/devel/Catboard-PipelineC pi4-28:~/
```

```
devel@pi4-28:~/Catboard-PipelineC/vga-pong/examples/pico-ice/
ice_makefile_pipelinec $ sudo ../../../../utils/config_cat gateway.bin
```

```
GPIO 25 not exported, trying to export...
GPIO 17 not exported, trying to export...
GPIO 22 not exported, trying to export...
```

```
OK: SPI driver loaded
```

```
Setting GPIO directions
```

```
out
```

```
out
```

```
in
```

```
Setting output to low
```

```
0
```

```
Reseting FPGA
```

```
0
```

```
1
```

```
Checking DONE pin
```

0

Continuing with configuration procedure

263+1 records in

263+1 records out

135100 bytes (135 kB, 132 KiB) copied, 0.0282328 s, 4.8 MB/s

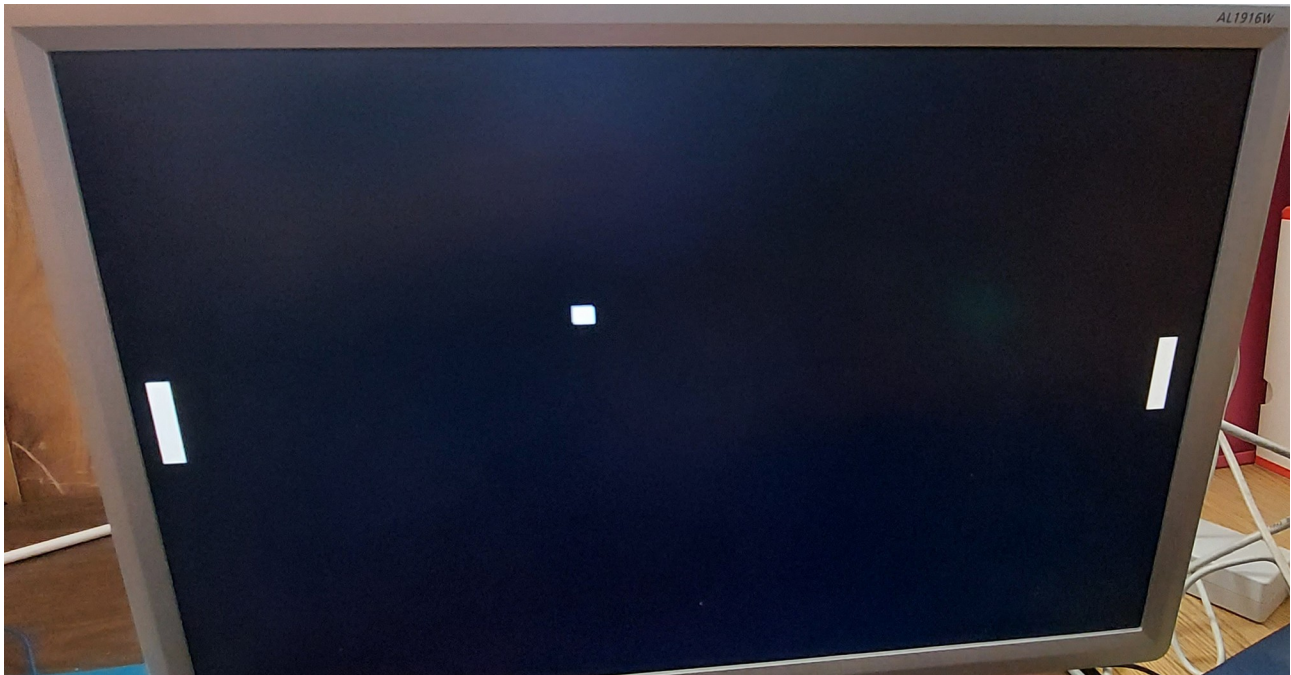
Setting output to high

1

Checking DONE pin

1

Xx



```
devel@pi4-28:~ $ minicom myusb0
```

Welcome to minicom 2.8

OPTIONS: I18n

Port /dev/ttyUSB0, 13:29:20

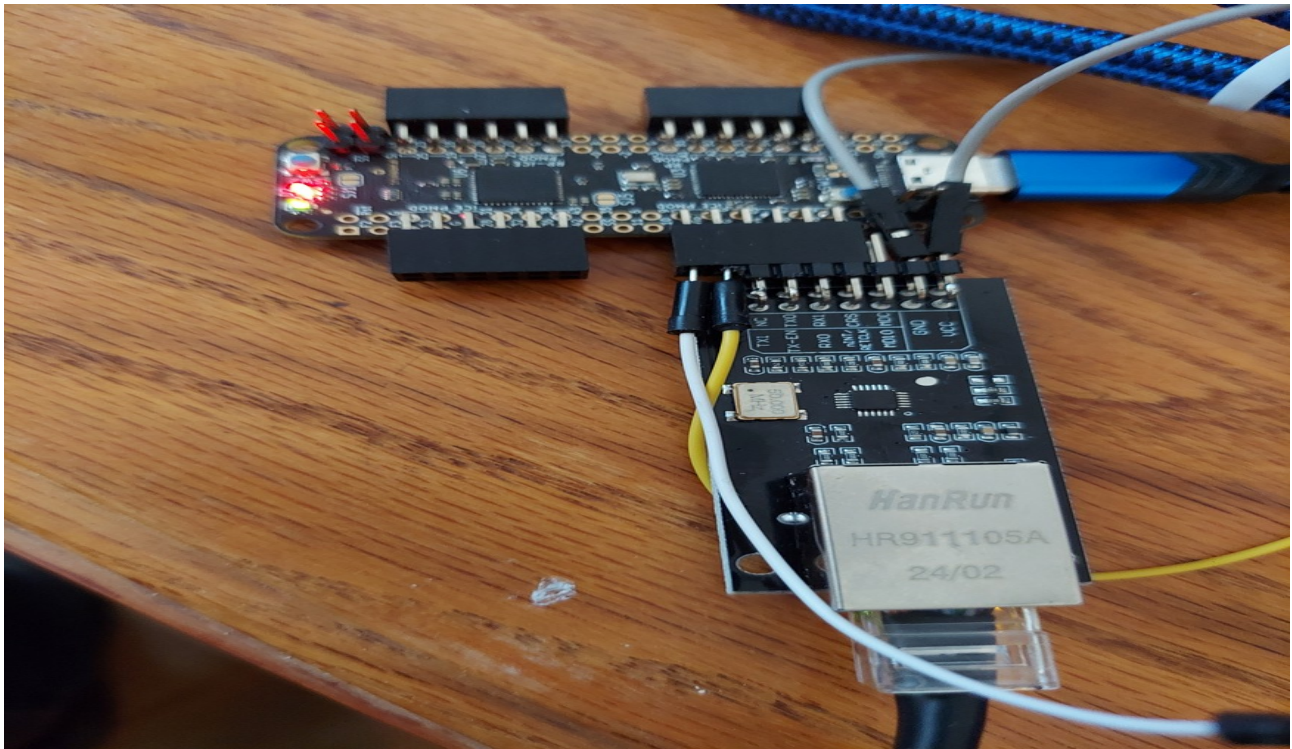
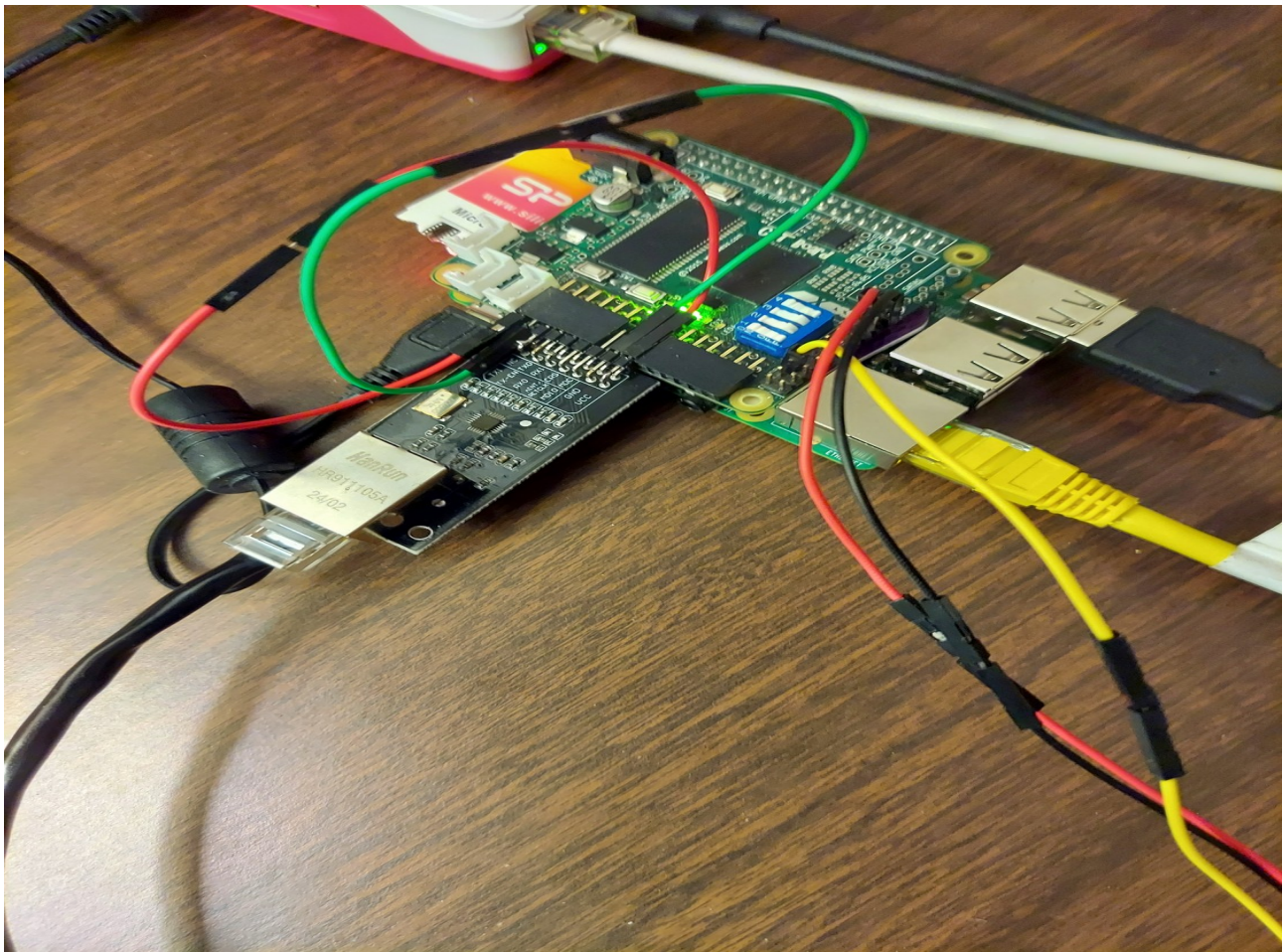
Press CTRL-A Z for help on special keys



xx

The pmods needed for vga-pong are reversed on the catboard pmod2 pmo3. This was noted when the pmod-ethernet was tested.




$$X_x$$


The following was from the Catboard-Pipelinec/doc/vga-pong/nextpnr.log

Info: Device utilisation:

Info: ICESTORM_LC: 999/ 7680 13%

Info: ICESTORM_RAM: 0/ 32 0%
Info: SB_IO: 20/ 256 7%
Info: SB_GB: 7/ 8 87%
Info: ICESTORM_PLL: 1/ 2 50%
Info: SB_WARMBOOT: 0/ 1 0%