*******************Default*****************
Catboard-PipelineC compiled pi5-70 executed on pi3-28
10/26/25

*******************Default*****************

Below is a Raspberry Pi3 with Catboard iCE40HX8K FPGA.
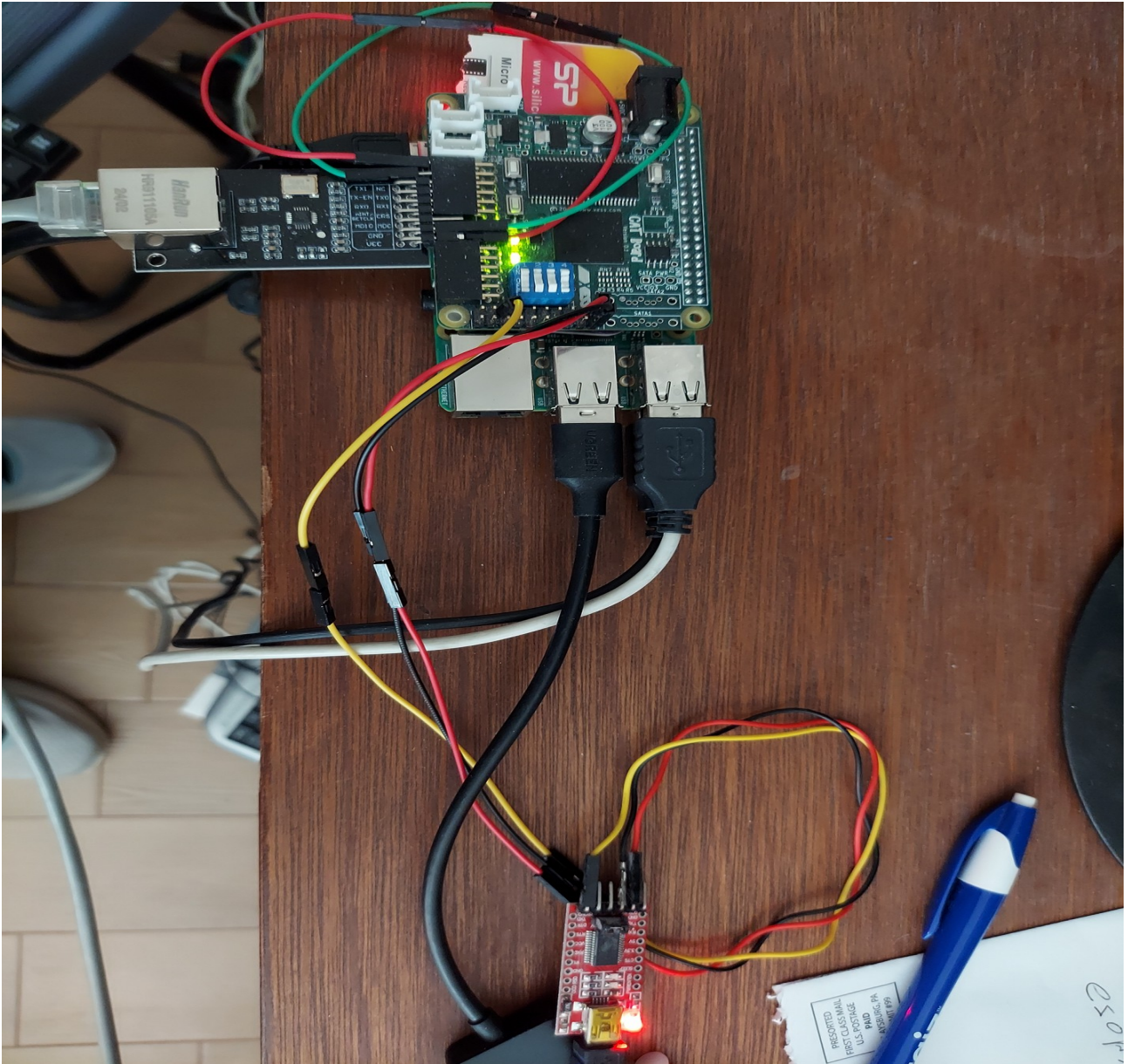
The image above has FTDI2USB which currently is not providing a uart-echo.

Note: Both the host running devel@pi3-28:~/Catboard-Pipelinec/pmod-ethernet/examples/net $ sudo ./work_test and the pmod-ethernet need to be on eth0.

devel@pi5-70:~/PipelineC $ git log

commit 422abd8ec3496d109e1153989ac848503e1292fe (HEAD -> test-dev, origin/test-dev)
Merge: ba22d9f 0213aad
Author: develone <develone@sbcglobal.net>
Date: Thu Apr 24 15:12:02 2025 -0600

    Merge branch 'JulianKemmerer:master' into test-dev

devel@pi5-70:~/PipelineC $ git branch -a
* test-dev
  test-dev-050125
  remotes/origin/HEAD -> origin/master
  remotes/origin/master
  remotes/origin/test-dev
  remotes/origin/test-dev-050125
  remotes/origin/test-dev-060125
  remotes/origin/test-dev-091125

devel@pi3-28:~/Catboard-Pipelinec/pmod-ethernet/examples/catboard/ice_makefile_pipelinec $
cat build.sh
#!/bin/bash
make clean
make pipelinec TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"
make gateware.bin TOP_NAME=ethernet_top NEXTPNR_ARGS="--pre-pack eth_clocks.py"
#rsync -avl --delete ~/Catboard-Pipelinec pi4-28:~/

devel@pi3-28:~/Catboard-Pipelinec/pmod-ethernet/examples/net $ less fpga_mac.h
// Network, big endian, byte order
// MAC0 is most signficant byte
// MAC5 is least signficant byte
// "0:1:2:3:4:5"
#define FPGA_MAC0   0xA0
#define FPGA_MAC1   0xB1
#define FPGA_MAC2   0xC2
#define FPGA_MAC3   0xD3
#define FPGA_MAC4   0xE4
#define FPGA_MAC5   0xF5

uint8_t FPGA_MAC_BYTES[6] = {FPGA_MAC0, FPGA_MAC1, FPGA_MAC2, FPGA_MAC3,
FPGA_MAC4, FPGA_MAC5};

#define FPGA_MAC uint8_array6_be(FPGA_MAC_BYTES)

devel@pi3-28:~/Catboard-Pipelinec/pmod-ethernet/examples/net $ less eth_sw.c
// Mostly taken from https://gist.github.com/austinmarton/

#include <arpa/inet.h>
#include <linux/if_packet.h>
#include <stdio.h>
#include <string.h>
#include <stdlib.h>

```
#include <sys/ioctl.h>
#include <sys/socket.h>
#include <net/if.h>
#include <netinet/ether.h>

#ifndef FPGA_MAC0
#include "fpga_mac.h"
#endif
#ifndef DEFAULT_IF
//#define DEFAULT_IF    "enx0050b6248f73"
#define DEFAULT_IF      "eth0"
```

devel@pi3-28:~/Catboard-Pipelinec/pmod-ethernet/examples/catboard/ice_makefile_pipelinec $
ifconfig
eth0: flags=4419<UP,BROADCAST,RUNNING,PROMISC,MULTICAST> mtu 1500
      inet 192.168.12.209 netmask 255.255.255.0 broadcast 192.168.12.255
      inet6 fdfe:5e6c:2e69:98de:f2b9:e386:e7ce:86b3 prefixlen 64 scopeid 0x0<global>
      inet6 2607:fb90:cb15:c699:61bc:9fd7:70fa:81b prefixlen 64 scopeid 0x0<global>
      inet6 fdfe:5e6c:2e69:98de:6fba:5181:4089:e8cd prefixlen 128 scopeid 0x0<global>
      inet6 fe80::d4f7:df23:b089:bd09 prefixlen 64 scopeid 0x20<link>
      ether b8:27:eb:ad:a6:2c txqueuelen 1000 (Ethernet)
      RX packets 8325 bytes 675788 (659.9 KiB)
      RX errors 0 dropped 0 overruns 0 frame 0
      TX packets 1311 bytes 155570 (151.9 KiB)
      TX errors 0 dropped 0 overruns 0 carrier 0 collisions 0

devel@pi3-28:~ $ cd
Catboard-Pipelinec/pmod-ethernet/examples/catboard/ice_makefile_pipelinec/
devel@pi3-28:~/Catboard-Pipelinec/pmod-ethernet/examples/catboard/ice_makefile_pipelinec $
sudo ../../../../utils/config_cat gateware.bin

OK: GPIO 25 exported
OK: GPIO 17 exported
OK: GPIO 22 exported

OK: SPI driver loaded

Setting GPIO directions
out
out
in
Setting output to low
0
Reseting FPGA
0
1
Checking DONE pin
0
Continuing with configuration procedure
263+1 records in
263+1 records out

135100 bytes (135 kB, 132 KiB) copied, 0.0382421 s, 3.5 MB/s
Setting output to high
1
Checking DONE pin
1
pmod-eth-rx

devel@pi3-28:~ $ cd Catboard-Pipelinec/pmod-ethernet/examples/net/
devel@pi3-28:~/Catboard-Pipelinec/pmod-ethernet/examples/net $ sudo ./work_test
CPU threads: 1
n 'work()'s: 1
Total tx bytes: 8
Total rx bytes: 4
CPU took 0.002205 seconds to execute
CPU iteration time: 0.002205 seconds
CPU bytes per sec: 5441.847551 B/s
FPGA took 0.001194 seconds to execute
FPGA iteration time: 0.001194 seconds
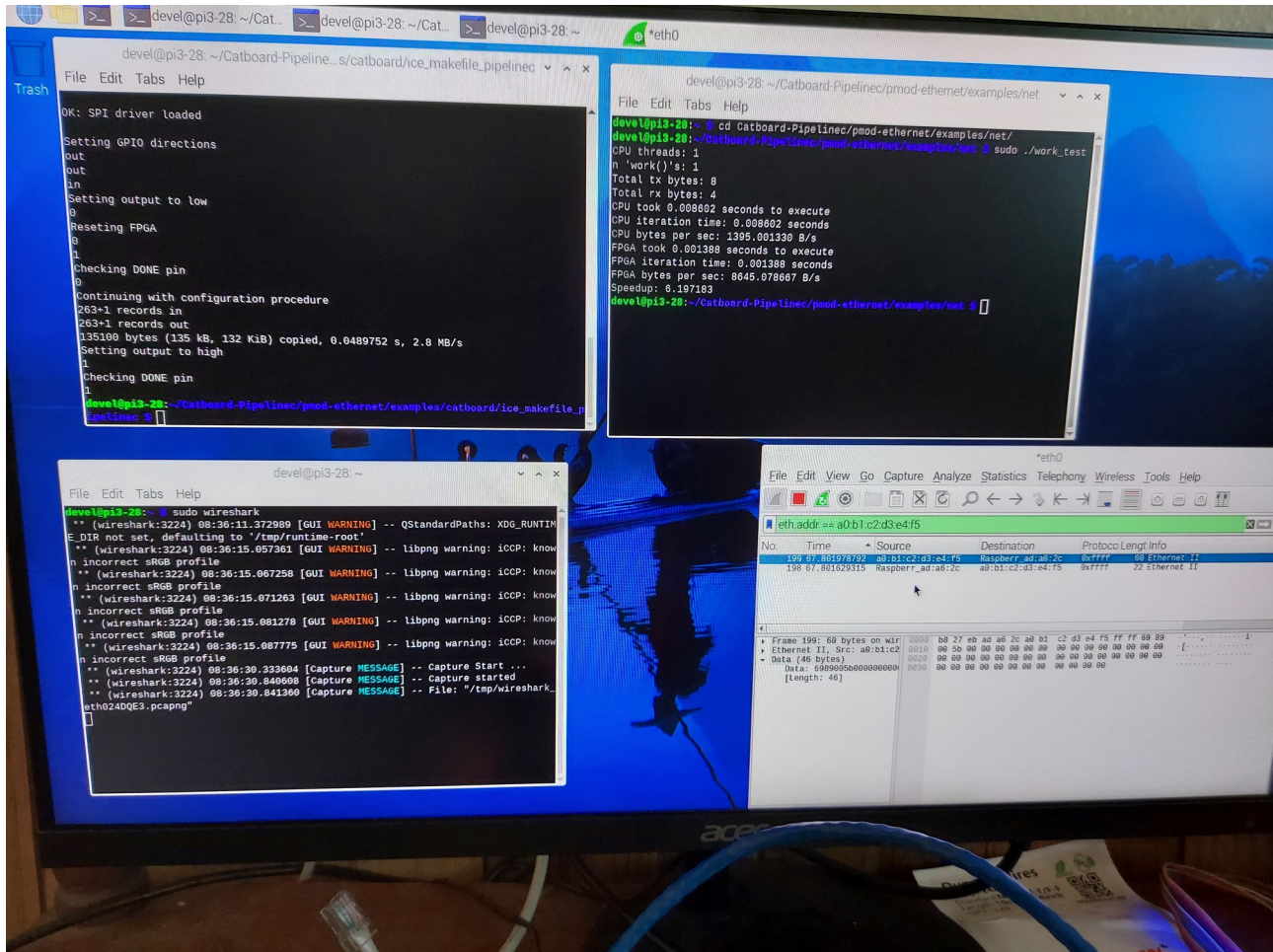FPGA bytes per sec: 10050.249201 B/s
Speedup: 1.846845

pmpd-eth-rx
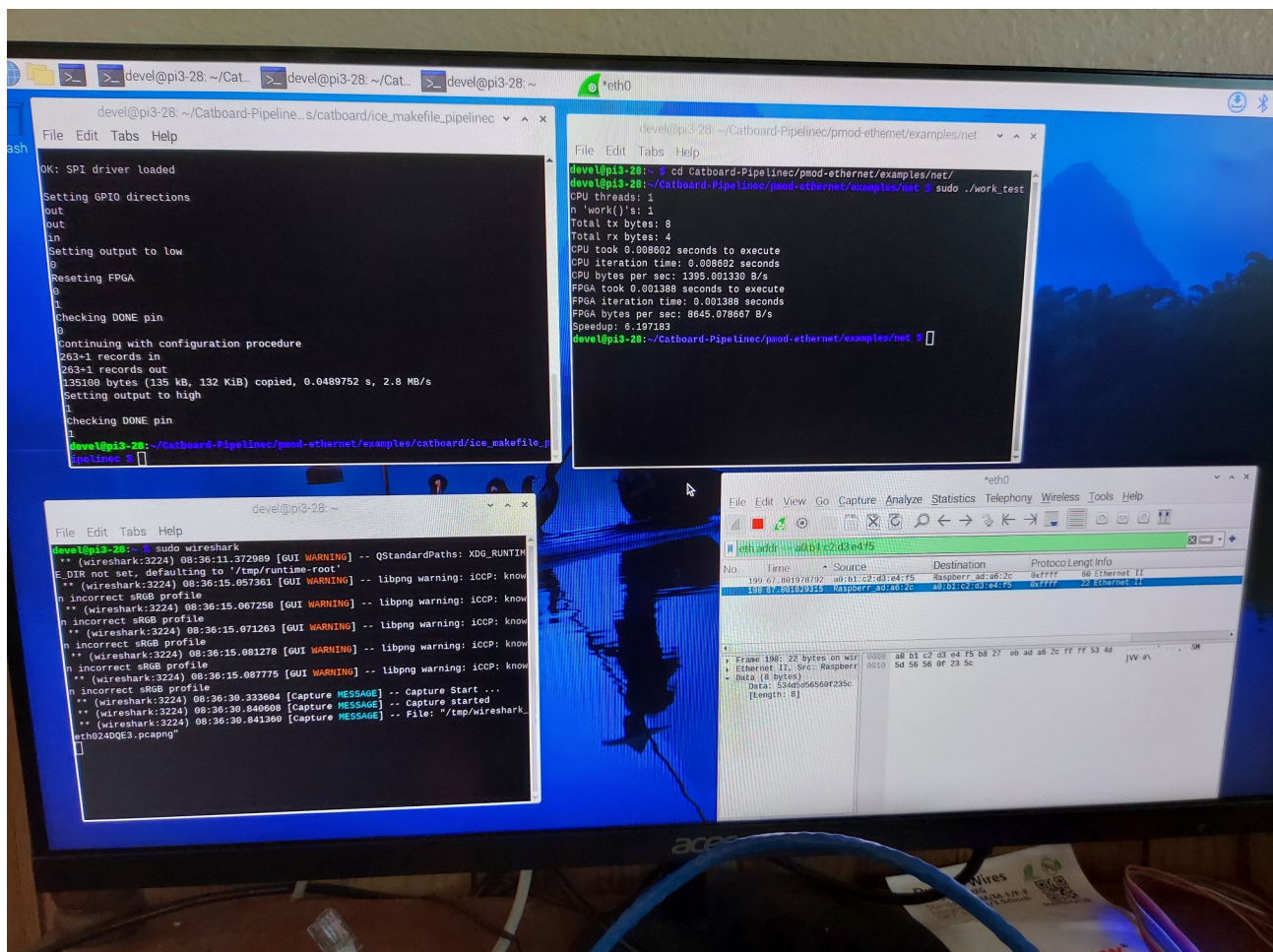
pmod-eth-tx

Lower right hand wireshark pmod-eth=txt