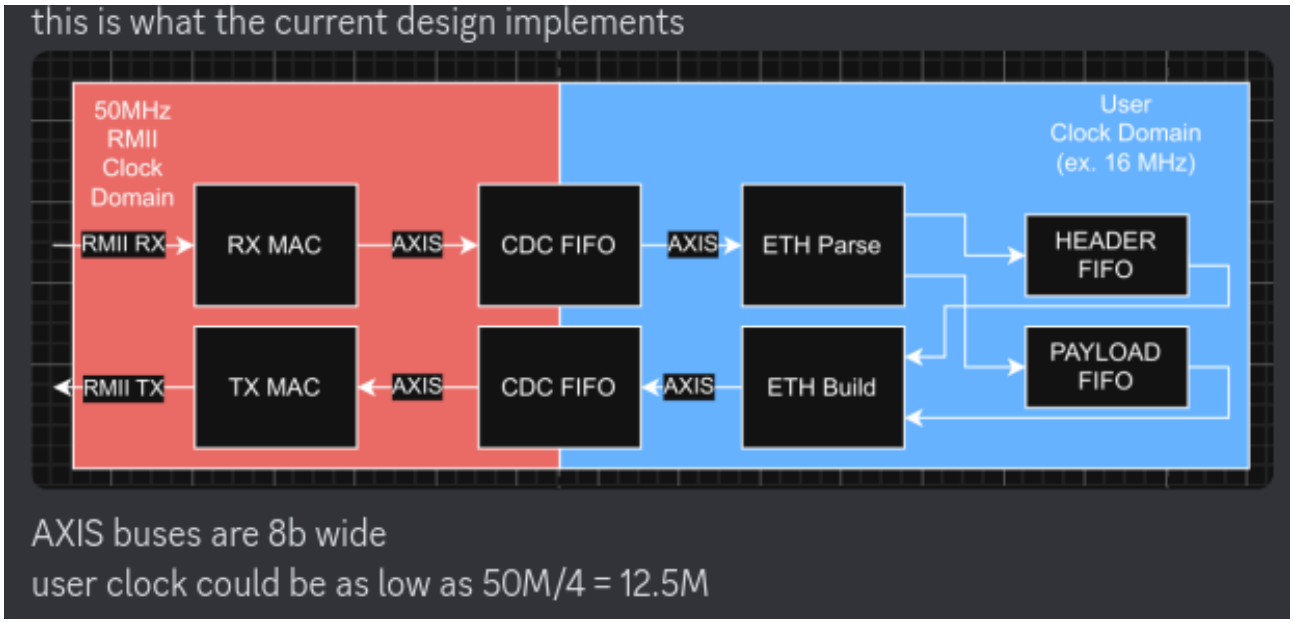
**********Default**********

Catboard-Pipelinec
PMOD-Ethernet
02/2025

**********Default**********

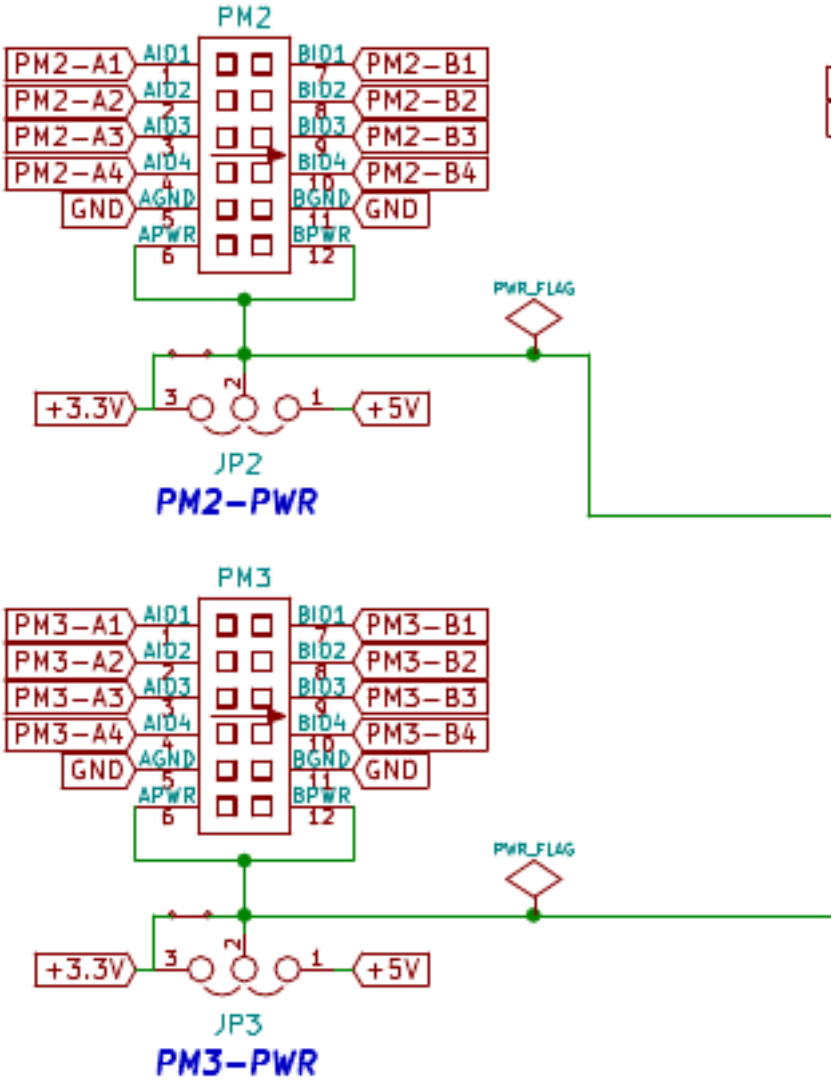


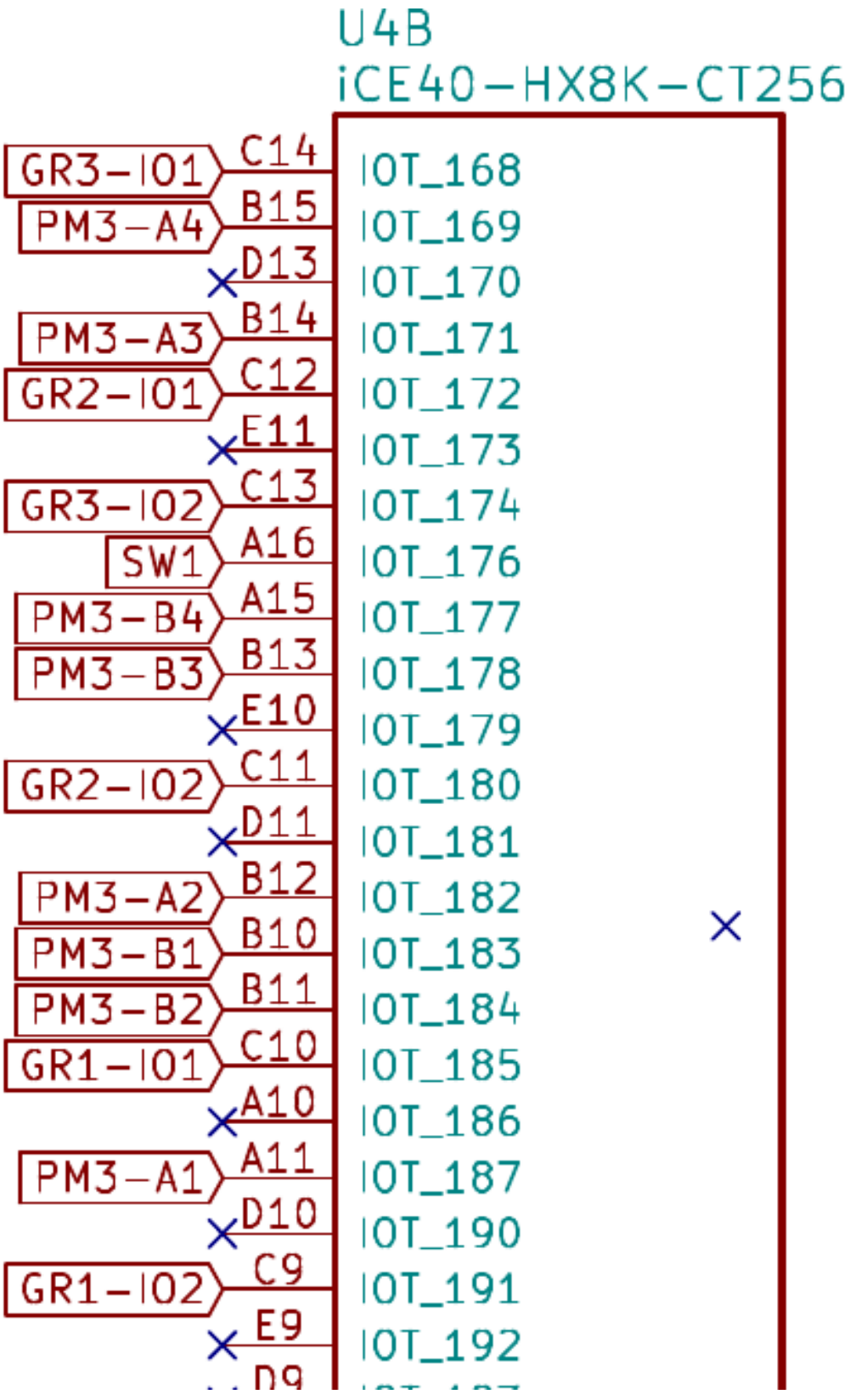
pico-ice 12MHz Catboard 100MHz
pmod-ether 25MHz

```
/**
 * PLL configuration
 *
 * This Verilog header file was generated automatically
 * using the icepll tool from the IceStorm project.
 * It is intended for use with FPGA primitives SB_PLL40_CORE,
 * SB_PLL40_PAD, SB_PLL40_2_PAD, SB_PLL40_2F_CORE or SB_PLL40_2F_PAD.
 * Use at your own risk.
 *
 * Given input frequency:       100.000 MHz
 * Requested output frequency:   25.000 MHz
 * Achieved output frequency:    25.000 MHz
 */

.FEEDBACK_PATH("SIMPLE"),
.DIVR(4'b0000),                 // DIVR =  0
.DIVF(7'b0000111),   // DIVF =  7
.DIVQ(3'b101),                  // DIVQ =  5
.FILTER_RANGE(3'b101)    // FILTER_RANGE = 5
```

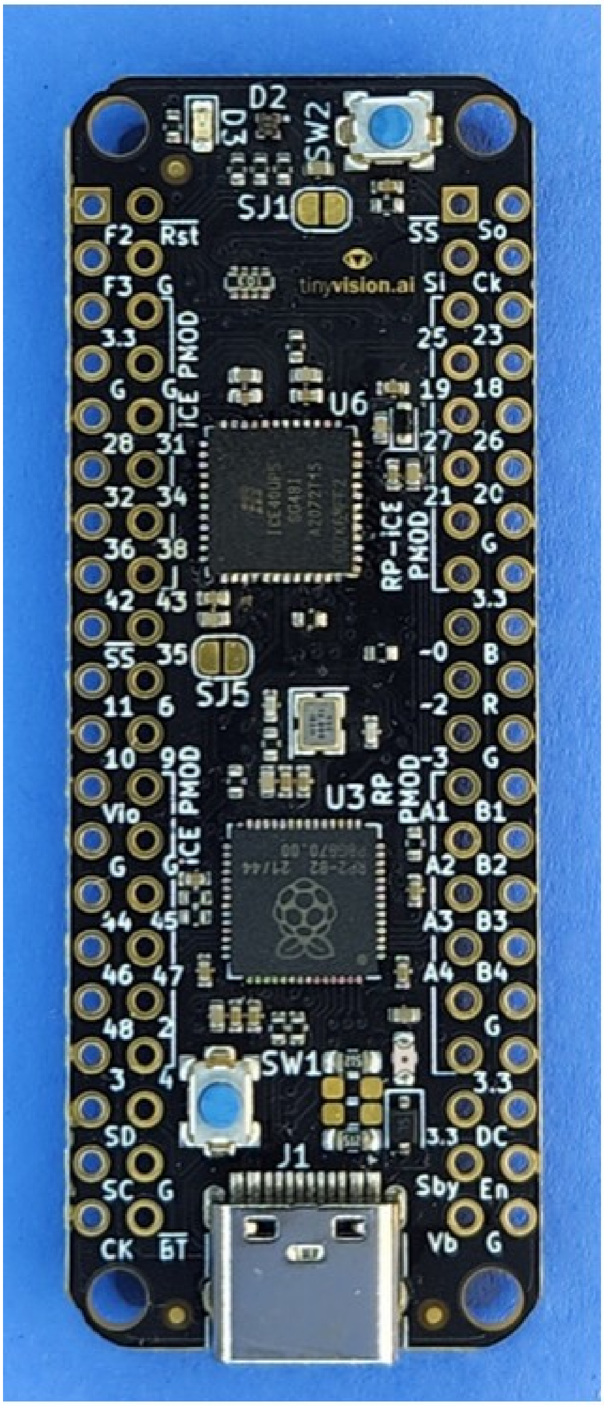
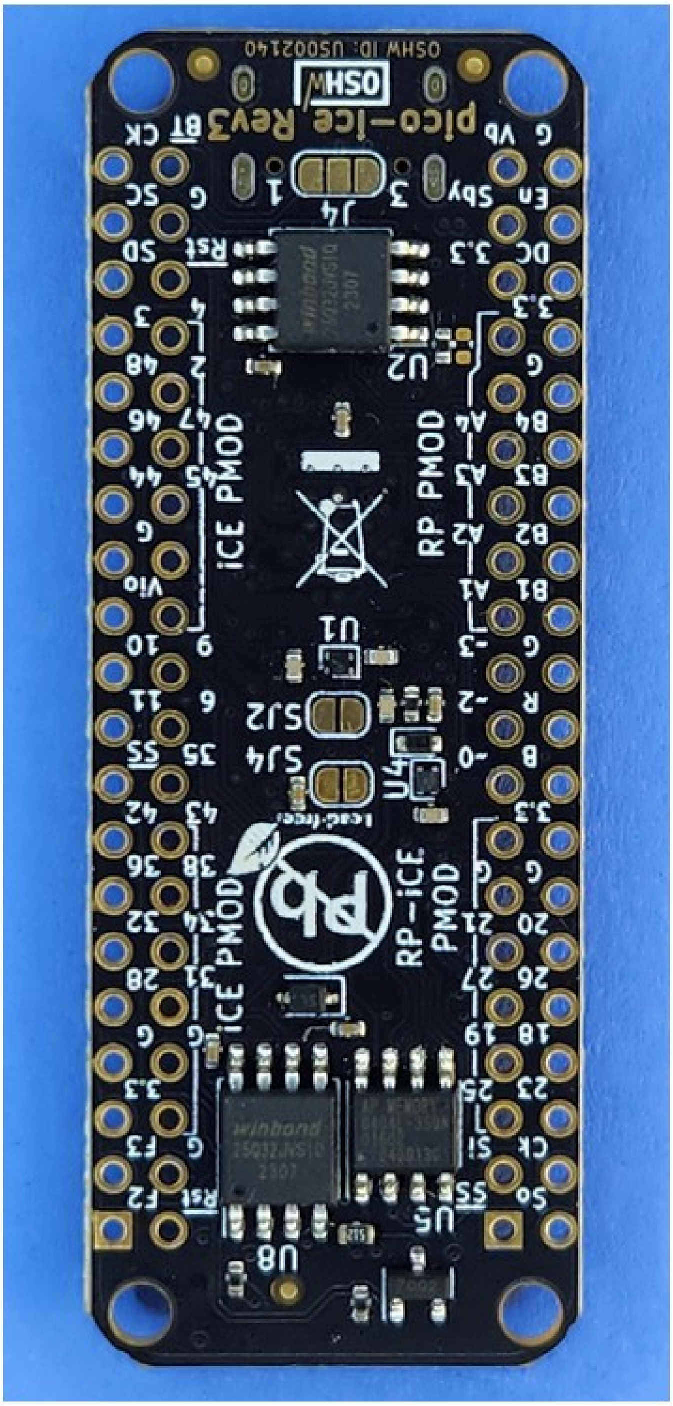
pico-ice to catboard
PMOD0A

```
set_io -nowarn ICE_45 45
set_io -nowarn ICE_47 47
set_io -nowarn ICE_2 2
set_io -nowarn ICE_4 4

# PMOD0B
set_io -nowarn ICE_44 44
set_io -nowarn ICE_46 46
set_io -nowarn ICE_48 48
set_io -nowarn ICE_3 3


# pin definitions
set_io d7_o A15
set_io d0_o A11
set_io d5_o B13
set_io d6_o B15
set_io d2_o B12
set_io d3_o B11
set_io d1_o B10
set_io clk_i C8
set_io d4_o B1
```




U4B
iCE40-HX8K-CT256
GR3-IO1
C14
IOT_168
PM3-A4
B15
IOT_169
D13
IOT_170
PM3-A3
B14
IOT_171
GR2-IO1
C12
IOT_172
E11
IOT_173
GR3-IO2
C13
IOT_174
SW1
A16
IOT_176
PM3-B4
A15
IOT_177
PM3-B3
B13
IOT_178
E10
IOT_179
GR2-IO2
C11
IOT_180
D11
IOT_181
PM3-A2
B12
IOT_182
PM3-B1
B10
IOT_183
PM3-B2
B11
IOT_184
GR1-IO1
C10
IOT_185
A10
IOT_186
PM3-A1
A11
IOT_187
D10
IOT_190
GR1-IO2
C9
IOT_191
E9
IOT_192

xx


tinyvision.ai
ICE PMOD
RP-ICE PMOD
RP PMOD
U6
U3
SW1
SW2
SJ1
SJ5
J1
D2
D3

OSHW ID: US002140
pico-ice Rev3
ICE PMOD
RP PMOD
RP-ICE PMOD
U1
U2
U4
U5
U8
J4
SJ2
SJ4
lead-free

xx