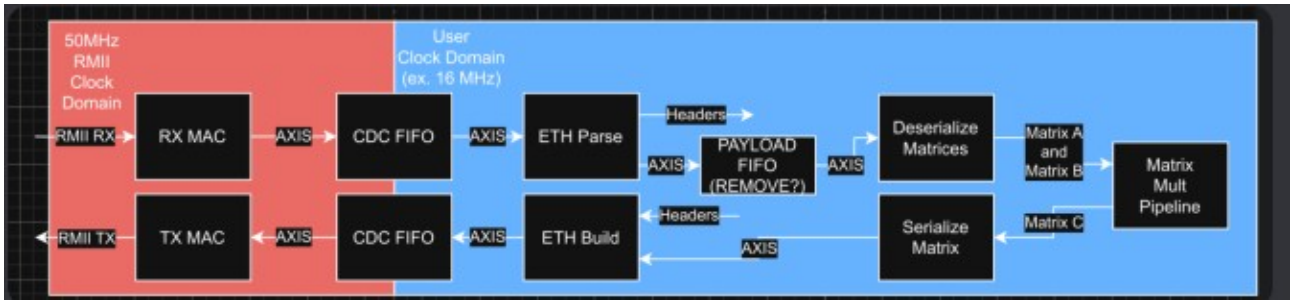
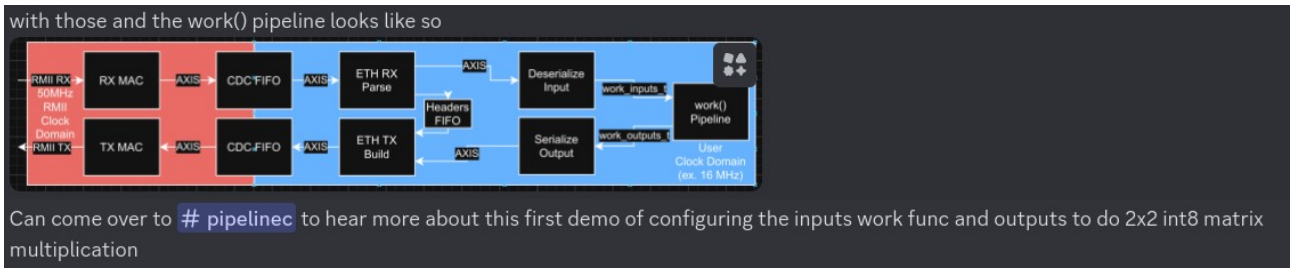
**********Default**********

Catboard-Pipelinec
PMOD-Ethernet
03/07/25

**********Default**********

The current image which does work in the form matrix multiply.





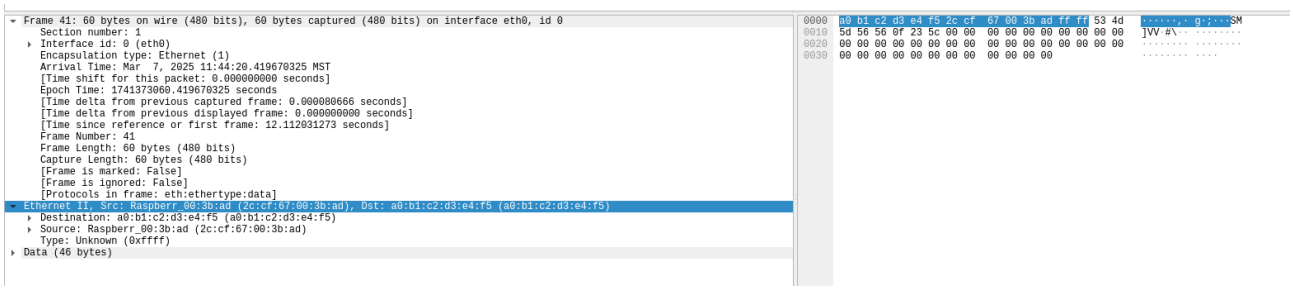
Tested 02/28/25 in PipelineC repo.

devel@pi5-70:~/Catboard-Pipelinec/pmod-ethernet/examples/net $ ./compile-work_test.sh
In file included from work_test.c:30:
work.h:26:10: **fatal error:** type_bytes_t.h/work_inputs_t_bytes_t.h/work_inputs_t_bytes.h: No such file or directory
  26 | #include **"type_bytes_t.h/work_inputs_t_bytes_t.h/work_inputs_t_bytes.h"**
     | ^~~~~~~
compilation terminated.

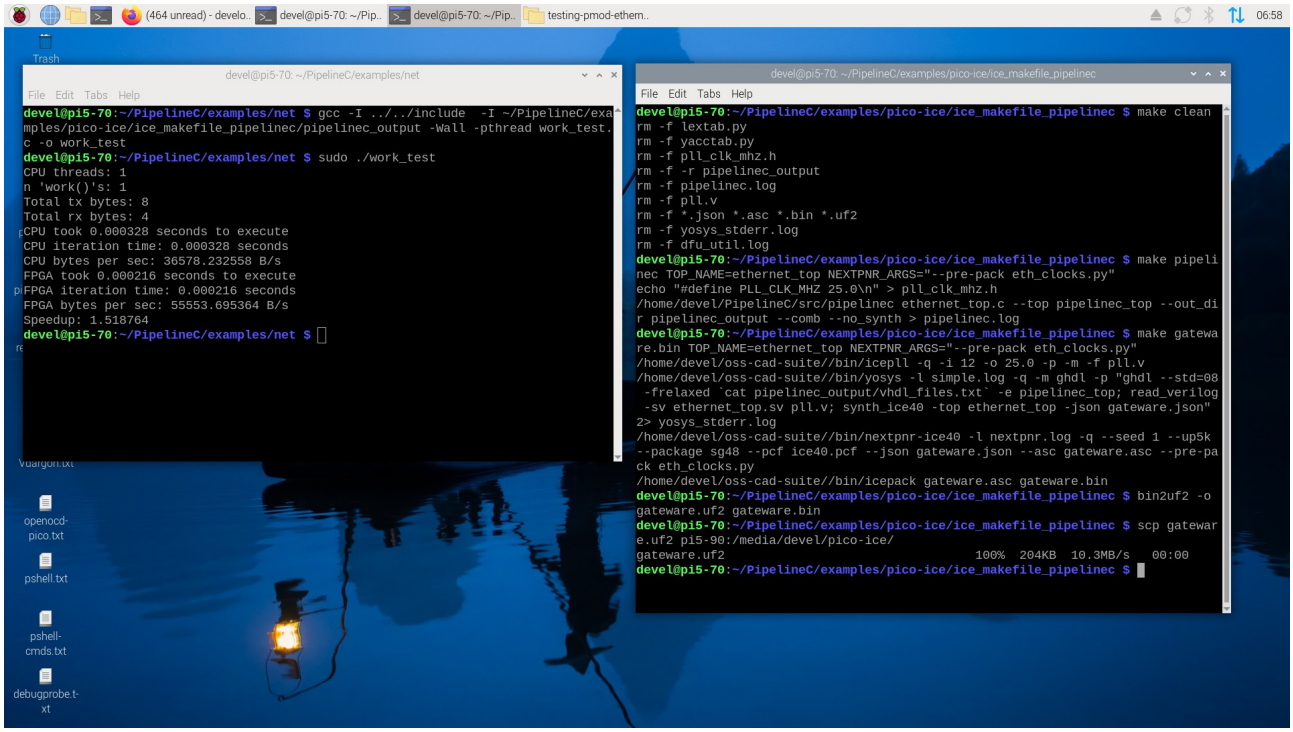
devel@pi5-70:~/Catboard-Pipelinec/pmod-ethernet/examples/catboard/ice_makefile_pipelinec $ ./build.sh
rm -f lextab.py
rm -f yacctab.py
rm -f pll_clk_mhz.h
rm -f -r pipelinec_output
rm -f pipelinec.log
rm -f pll.v
rm -f *.json *.asc *.bin *.uf2
rm -f yosys_stderr.log

```
rm -f dfu_util.log
echo "#define PLL_CLK_MHZ 25.0\n" > pll_clk_mhz.h
/home/devel/PipelineC/src/pipelinec ethernet_top.c --top pipelinec_top --out_dir pipelinec_output --
comb --no_synth > pipelinec.log
/home/devel/oss-cad-suite//bin/icepll -q -i 100 -o 25.0  -m -f pll.v
/home/devel/oss-cad-suite//bin/yosys -l simple.log -q -m ghdl -p "ghdl --std=08 -frelaxed `cat
pipelinec_output/vhdl_files.txt` -e pipelinec_top; read_verilog -sv ethernet_top.sv pll.v;
synth_ice40 -top ethernet_top -json gateware.json" 2> yosys_stderr.log
/home/devel/oss-cad-suite//bin/nextpnr-ice40 -l nextpnr.log -q --randomize-seed --hx8k --package
ct256 --pcf ice40.pcf --json gateware.json --asc gateware.asc --pre-pack eth_clocks.py
/home/devel/oss-cad-suite//bin/icepack gateware.asc gateware.bin

devel@pi4-28:~/Catboard-Pipelinec/pmod-ethernet/examples/catboard/ice_makefile_pipelinec $
~/Catboard-Pipelinec/prg-cat1.sh

OK: GPIO 25 exported
OK: GPIO 17 exported
OK: GPIO 22 exported

OK: SPI driver loaded

Setting GPIO directions
out
out
in
Setting output to low
0
Reseting FPGA
0
1
Checking DONE pin
0
Continuing with configuration procedure
263+1 records in
263+1 records out
135100 bytes (135 kB, 132 KiB) copied, 0.0274133 s, 4.9 MB/s
Setting output to high
1
Checking DONE pin
1
devel@pi5-70:~/Catboard-Pipelinec/pmod-ethernet/examples/net $ ./compile-work_test.sh

devel@pi5-70:~/Catboard-Pipelinec/pmod-ethernet/examples/net $ sudo ./work_test
CPU threads: 1
n 'work()'s: 1
Total tx bytes: 8
Total rx bytes: 4
CPU took 0.000278 seconds to execute
CPU iteration time: 0.000278 seconds
CPU bytes per sec: 43166.078902 B/s
FPGA took 0.000180 seconds to execute
FPGA iteration time: 0.000180 seconds
```

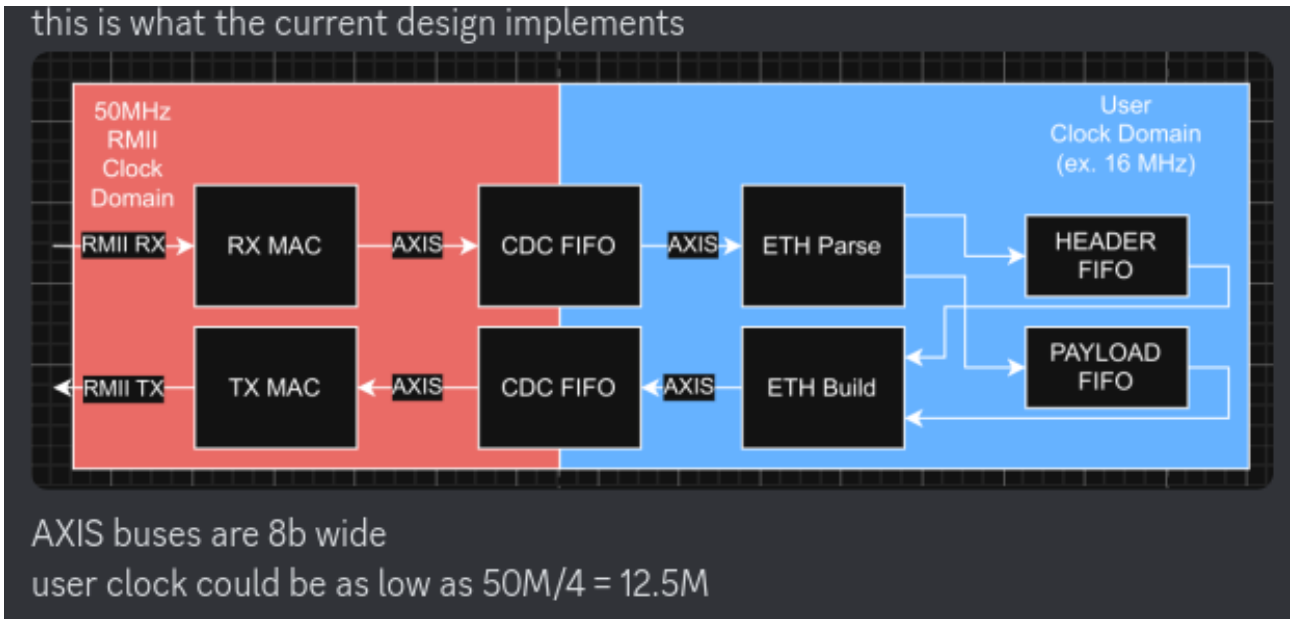
FPGA bytes per sec: 66664.434437 B/s
Speedup: 1.544371

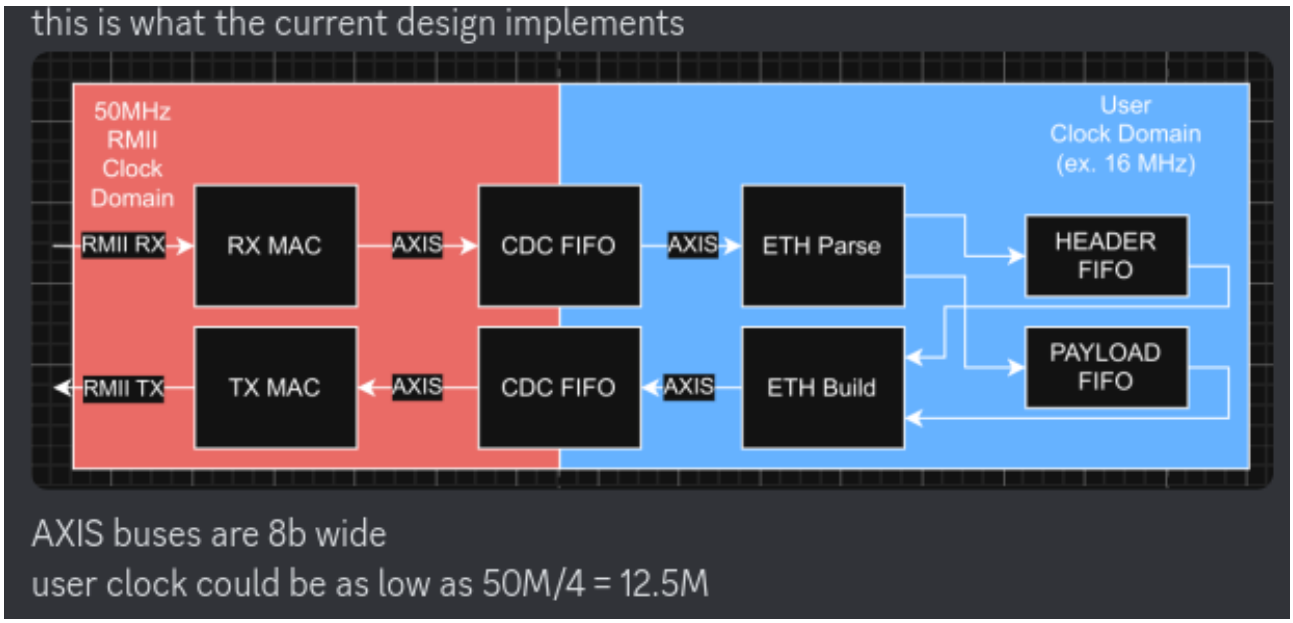


The work_test.c is dependent on the successful build of gateware.bin see Appendix A.



This image was loopback tested on 02/17/25





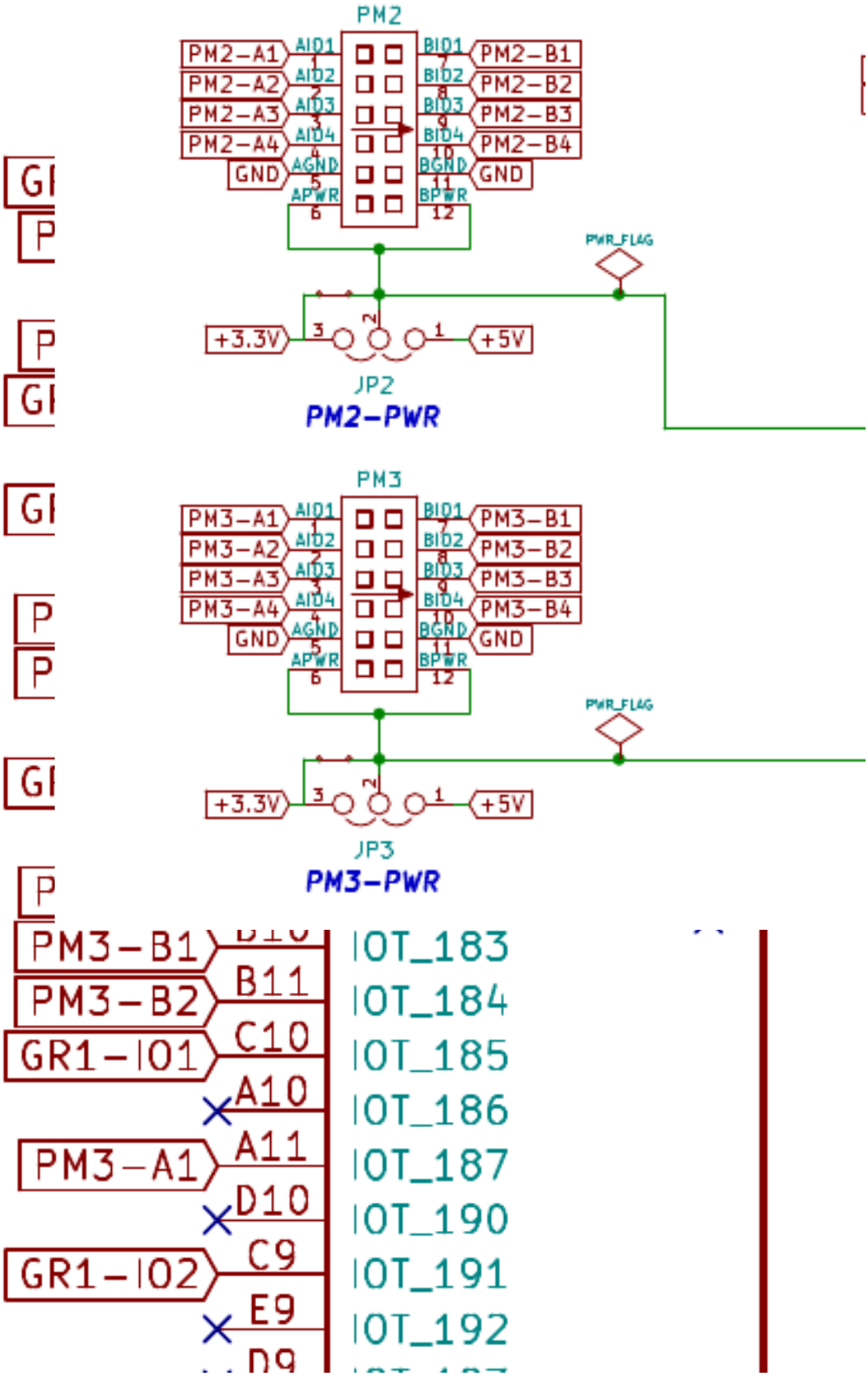
pico-ice 12MHz Catboard 100MHz
pmod-ether 25MHz

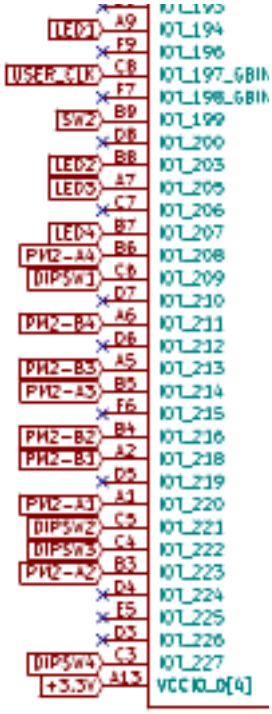
```
/**
 * PLL configuration
 *
 * This Verilog header file was generated automatically
 * using the icepll tool from the IceStorm project.
 * It is intended for use with FPGA primitives SB_PLL40_CORE,
 * SB_PLL40_PAD, SB_PLL40_2_PAD, SB_PLL40_2F_CORE or SB_PLL40_2F_PAD.
 * Use at your own risk.
 *
 * Given input frequency:       100.000 MHz
 * Requested output frequency:   25.000 MHz
```

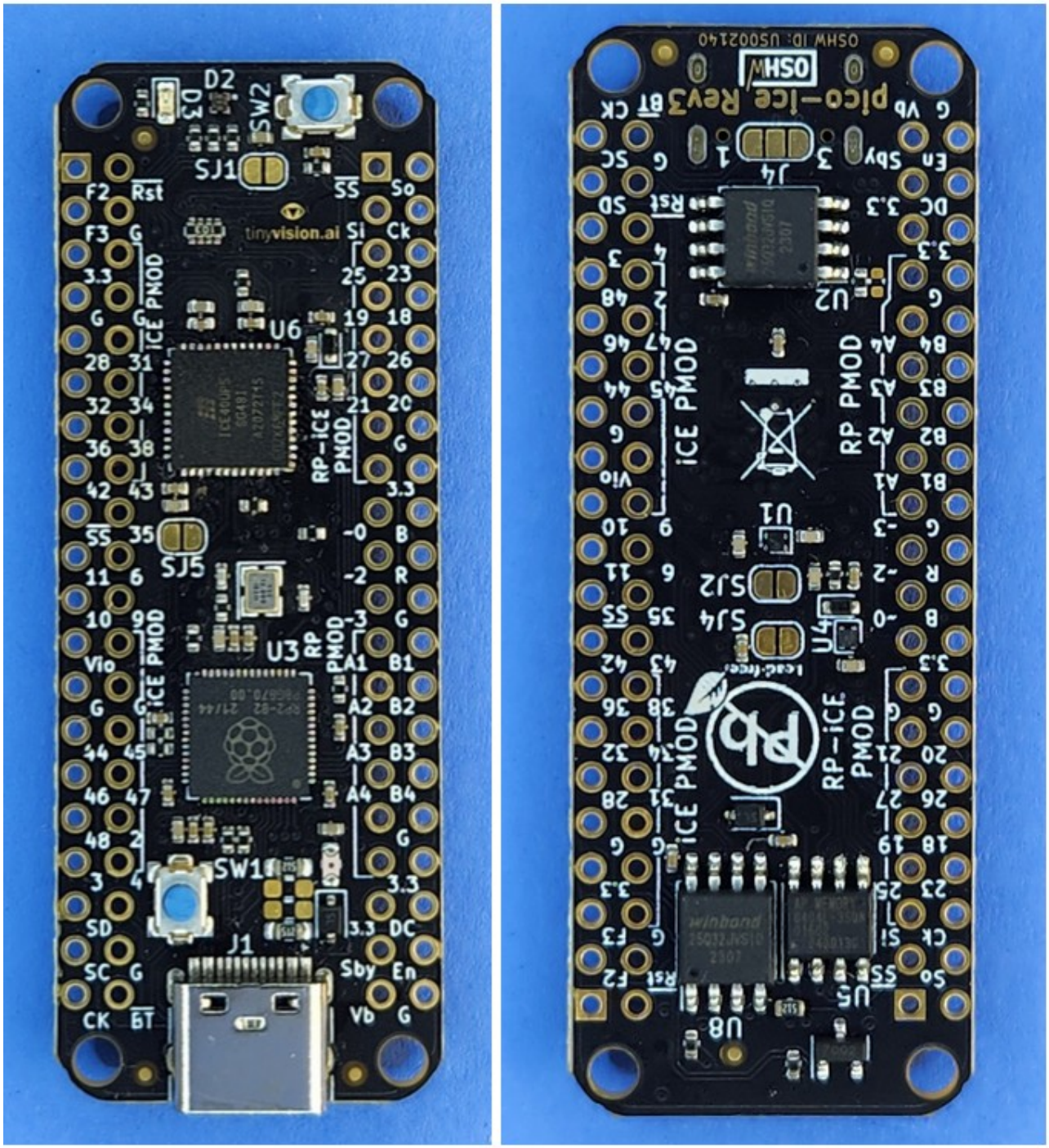
```
 * Achieved output frequency:    25.000 MHz
 */

.FEEDBACK_PATH("SIMPLE"),
.DIVR(4'b0000),                 // DIVR =  0
.DIVF(7'b0000111),   // DIVF =  7
.DIVQ(3'b101),                  // DIVQ =  5
.FILTER_RANGE(3'b101)    // FILTER_RANGE = 5
```

pico-ice to catboard

```
# PMOD0A
set_io -nowarn ICE_45 B15 #PM3-A4 345
set_io -nowarn ICE_47 B14 #PM3-A3 47
set_io -nowarn ICE_2 B12 #PM3-A2 2
set_io -nowarn ICE_4 A11 #PM3-A1 4

# PMOD0B
set_io -nowarn ICE_44 A15 #PM3-B4 44
set_io -nowarn ICE_46 B13 #PM3-B3 46
set_io -nowarn ICE_48 B11 #PM3-B2 48
set_io -nowarn ICE_3 B10 #PM3-B1 3

# PMOD1A
set_io -nowarn ICE_31 B6 #PM2-A4 31
set_io -nowarn ICE_34 A5 #PM2-A3 34
set_io -nowarn ICE_38 B3 #PM2-A2 38
set_io -nowarn ICE_43 A1 #PM2-A1 43

# PMOD1B
set_io -nowarn ICE_28 A6 #PM2-B4 28
set_io -nowarn ICE_32 A5 #PM2-B3 32
set_io -nowarn ICE_36 B4 #PM2-B2 36
set_io -nowarn ICE_42 A2 #PM2-B1 42
```

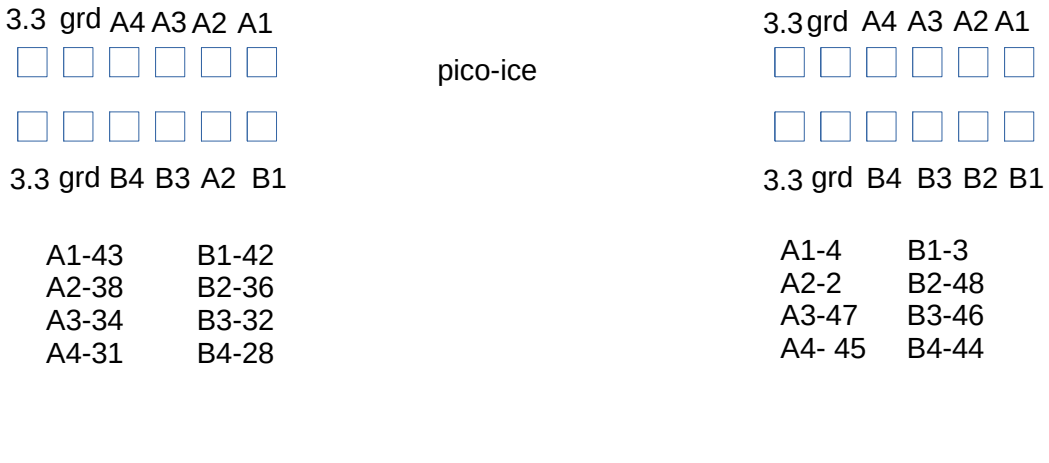

PM2
PM2-A1
PM2-A2
PM2-A3
PM2-A4
GND
AID1
AID2
AID3
AID4
AGND
APWR
BID1
BID2
BID3
BID4
BGND
BPWR
PM2-B1
PM2-B2
PM2-B3
PM2-B4
GND
PWR_FLAG
+3.3V
+5V
JP2
PM2-PWR
PM3
PM3-A1
PM3-A2
PM3-A3
PM3-A4
PM3-B1
PM3-B2
PM3-B3
PM3-B4
JP3
PM3-PWR
PM3-B1
B11
IOT_183
PM3-B2
B11
IOT_184
GR1-IO1
C10
IOT_185
A10
IOT_186
PM3-A1
A11
IOT_187
D10
IOT_190
GR1-IO2
C9
IOT_191
E9
IOT_192

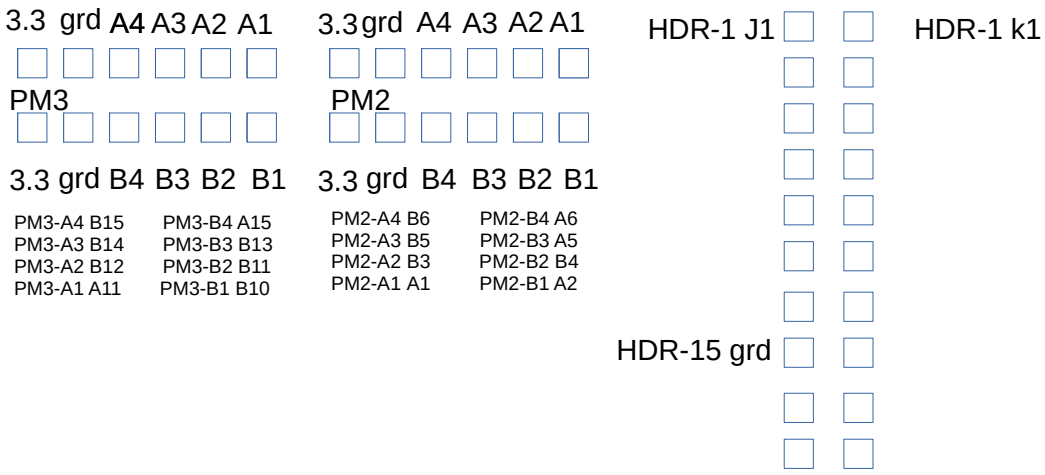

LED1
A9
IO1_194
F9
IO1_196
USER_CLK
C8
IO1_197_GBIN
F7
IO1_198_GBIN
SW2
B9
IO1_199
D8
IO1_200
LED2
B8
IO1_203
LED3
A7
IO1_205
C7
IO1_206
LED4
B7
IO1_207
PMI2-A4
B6
IO1_208
DIPSW1
C6
IO1_209
D7
IO1_210
PMI2-B4
A6
IO1_211
D6
IO1_212
PMI2-B3
A5
IO1_213
PMI2-A5
B5
IO1_214
F6
IO1_215
PMI2-B2
B4
IO1_216
PMI2-B1
A2
IO1_218
D5
IO1_219
PMI2-A1
A1
IO1_220
DIPSW2
C5
IO1_221
DIPSW3
C4
IO1_222
PMI2-A2
B3
IO1_223
D4
IO1_224
E5
IO1_225
D3
IO1_226
DIPSW4
C3
IO1_227
+3.3V
A13
VCCIO_D[4]



devel@pi5-70:~/Catboard-Pipelinec/pmod-ethernet/ice_makefile_pipelinec $ make clean
rm -f lextab.py
rm -f yacctab.py
rm -f pll_clk_mhz.h
rm -f -r pipelinec_output
rm -f pipelinec.log
rm -f pll.v
rm -f *.json *.asc *.bin *.uf2
rm -f yosys_stderr.log
rm -f dfu_util.log
devel@pi5-70:~/Catboard-Pipelinec/pmod-ethernet/ice_makefile_pipelinec $ make pipelinec TOP_NAME=ethernet_top
echo "#define PLL_CLK_MHZ 25.0\n" > pll_clk_mhz.h

/home/devel/PipelineC/src/pipelinec ethernet_top.c --top pipelinec_top --out_dir pipelinec_output --comb --no_synth > pipelinec.log
devel@pi5-70:~/Catboard-Pipelinec/pmod-ethernet/ice_makefile_pipelinec $ make gateware.bin TOP_NAME=ethernet_top
/home/devel/oss-cad-suite//bin/icepll -q -i 100 -o 25.0 -p -m -f pll.v
/home/devel/oss-cad-suite//bin/yosys -l simple.log -q -m ghdl -p "ghdl --std=08 -frelaxed `cat pipelinec_output/vhdl_files.txt` -e pipelinec_top; read_verilog -sv ethernet_top.sv pll.v; synth_ice40 -top ethernet_top -json gateware.json" 2> yosys_stderr.log
/home/devel/oss-cad-suite//bin/nextpnr-ice40 -l nextpnr.log -q --randomize-seed --hx8k --package ct256 --pcf ice40.pcf --json gateware.json --asc gateware.asc --freq 25.0
ERROR: PLL 'pll_inst.uut' PACKAGEPIN SB_IO 'clk_12p0$sb_io' is not connected to any PLL BEL
ERROR: Packing design failed.
0 warnings, 2 errors
make: *** [Makefile:40: gateware.bin] Error 255





Ver 0.1
03/01/25

Appendix A

```
#pragma once
#include "type_bytes_t.h/int8_t_bytes_t.h/int8_t_bytes.h"
#define work_inputs_t_SIZE 8

void work_inputs_t_to_bytes(work_inputs_t* x, uint8_t* bytes)
{
size_t pos = 0;
// matrix0
size_t matrix0_dim_0;
for(matrix0_dim_0=0;matrix0_dim_0<2;matrix0_dim_0=matrix0_dim_0+1){
size_t matrix0_dim_1;
for(matrix0_dim_1=0;matrix0_dim_1<2;matrix0_dim_1=matrix0_dim_1+1){
 int8_t_to_bytes(&(x->matrix0[matrix0_dim_0][matrix0_dim_1]), &(bytes[pos]));
 pos = pos + 1; // not sizeof()
}
}
// matrix1
size_t matrix1_dim_0;
for(matrix1_dim_0=0;matrix1_dim_0<2;matrix1_dim_0=matrix1_dim_0+1){
size_t matrix1_dim_1;
for(matrix1_dim_1=0;matrix1_dim_1<2;matrix1_dim_1=matrix1_dim_1+1){
 int8_t_to_bytes(&(x->matrix1[matrix1_dim_0][matrix1_dim_1]), &(bytes[pos]));
 pos = pos + 1; // not sizeof()
}
}

}

void bytes_to_work_inputs_t(uint8_t* bytes, work_inputs_t* x)
```

```
{
size_t pos = 0;
// matrix0
size_t matrix0_dim_0;
for(matrix0_dim_0=0;matrix0_dim_0<2;matrix0_dim_0=matrix0_dim_0+1){
size_t matrix0_dim_1;
for(matrix0_dim_1=0;matrix0_dim_1<2;matrix0_dim_1=matrix0_dim_1+1){
 bytes_to_int8_t(&(bytes[pos]), &(x->matrix0[matrix0_dim_0][matrix0_dim_1]));
 pos = pos + 1; // not sizeof()
}
}
// matrix1
size_t matrix1_dim_0;
for(matrix1_dim_0=0;matrix1_dim_0<2;matrix1_dim_0=matrix1_dim_0+1){
size_t matrix1_dim_1;
for(matrix1_dim_1=0;matrix1_dim_1<2;matrix1_dim_1=matrix1_dim_1+1){
 bytes_to_int8_t(&(bytes[pos]), &(x->matrix1[matrix1_dim_0][matrix1_dim_1]));
 pos = pos + 1; // not sizeof()
}
}

}
```