

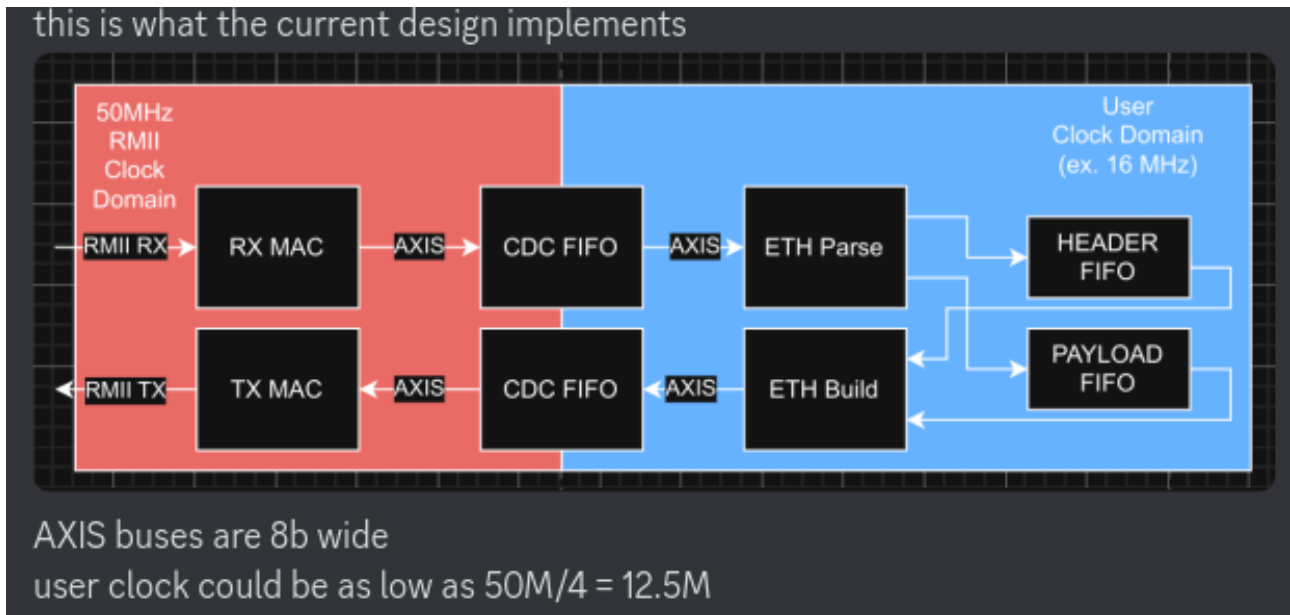
\*\*\*\*\*Default\*\*\*\*\*

## Catboard-Pipelinec

### PMOD-Ethernet

02/21/25

\*\*\*\*\*Default\*\*\*\*\*



pico-ice 12MHz Catboard 100MHz  
pmod-ether 25MHz

```
/**
 * PLL configuration
 *
 * This Verilog header file was generated automatically
 * using the icepll tool from the IceStorm project.
 * It is intended for use with FPGA primitives SB_PLL40_CORE,
 * SB_PLL40_PAD, SB_PLL40_2_PAD, SB_PLL40_2F_CORE or SB_PLL40_2F_PAD.
 * Use at your own risk.
 *
 * Given input frequency:    100.000 MHz
 * Requested output frequency: 25.000 MHz
 * Achieved output frequency: 25.000 MHz
 */
```

```
.FEEDBACK_PATH("SIMPLE"),
.DIVR(4'b0000),           // DIVR = 0
.DIVF(7'b0000111),       // DIVF = 7
.DIVQ(3'b101),           // DIVQ = 5
.FILTER_RANGE(3'b101)    // FILTER_RANGE = 5
```

pico-ice to catboard  
# PMOD0A

```

set_io -nowarn ICE_45 45
set_io -nowarn ICE_47 47
set_io -nowarn ICE_2 2
set_io -nowarn ICE_4 4

```

# PMOD0B

```

set_io -nowarn ICE_44 44
set_io -nowarn ICE_46 46
set_io -nowarn ICE_48 48
set_io -nowarn ICE_3 3

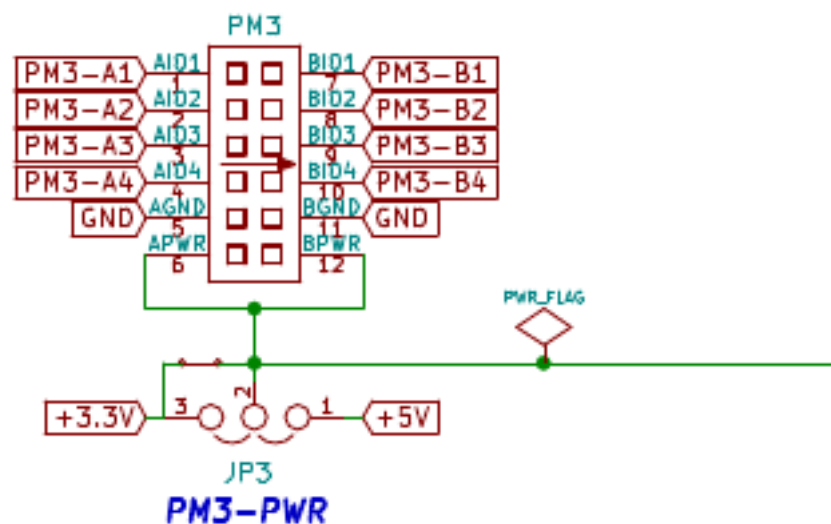
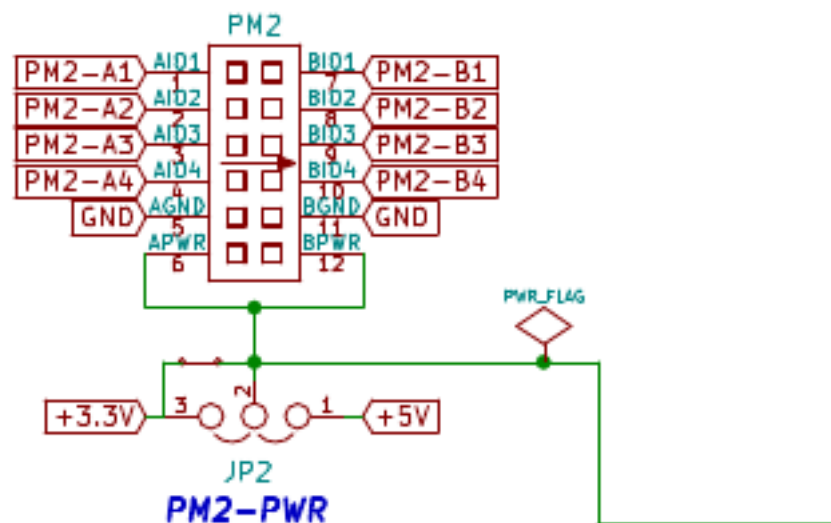
```

# pin definitions

```

set_io d7_o A15
set_io d0_o A11
set_io d5_o B13
set_io d6_o B15
set_io d2_o B12
set_io d3_o B11
set_io d1_o B10
set_io clk_i C8
set_io d4_o B1

```



# U4B iCE40-HX8K-CT256

GR3-I01	C14	IOT_168	
PM3-A4	B15	IOT_169	
	D13	IOT_170	
PM3-A3	B14	IOT_171	
GR2-I01	C12	IOT_172	
	E11	IOT_173	
GR3-I02	C13	IOT_174	
SW1	A16	IOT_176	
PM3-B4	A15	IOT_177	
PM3-B3	B13	IOT_178	
	E10	IOT_179	
GR2-I02	C11	IOT_180	
	D11	IOT_181	
PM3-A2	B12	IOT_182	
PM3-B1	B10	IOT_183	
PM3-B2	B11	IOT_184	
GR1-I01	C10	IOT_185	
	A10	IOT_186	
PM3-A1	A11	IOT_187	
	D10	IOT_190	
GR1-I02	C9	IOT_191	
	E9	IOT_192	
	D9	IOT_193	

×

	X	A9	K7_193
LED1	X	F9	K7_194
	X	F9	K7_196
USER_CLK	X	C8	K7_197_681H
	X	F7	K7_198_681H
SW2	X	B9	K7_199
	X	D8	K7_200
LED2	X	B8	K7_203
LED3	X	A7	K7_205
	X	C7	K7_206
LED4	X	B7	K7_207
PH2-A4	X	B6	K7_208
DIPSW1	X	C8	K7_209
	X	D7	K7_210
PH2-B4	X	A6	K7_211
	X	D6	K7_212
PH2-B3	X	A5	K7_213
PH2-A5	X	B5	K7_214
	X	F6	K7_215
PH2-B2	X	B4	K7_216
PH2-B1	X	A2	K7_218
	X	D5	K7_219
PH2-A3	X	A1	K7_220
DIPSW2	X	C5	K7_221
DIPSW3	X	C4	K7_222
PH2-A2	X	B3	K7_223
	X	D4	K7_224
	X	F5	K7_225
	X	D3	K7_226
DIPSW4	X	C3	K7_227
+3.3V	X	A13	VCCIO_0[4]

