Simulations with iverilog and for testing HDL designs

A test verilog code is used to test the design (see counter_tb.v & counter_tb_vcd.v below).
File counter.v

```
module counter(out, clk, reset);

  parameter WIDTH = 8;

  output [WIDTH-1 : 0] out;
  input        clk, reset;

  reg [WIDTH-1 : 0]   out;
  wire         clk, reset;

  always @(posedge clk)
    out <= out + 1;

  always @reset
    if (reset)
      assign out = 0;
    else
      deassign out;

endmodule // counter
```

File counter_tb.v

```
module test;

  /* Make a reset that pulses once. */
  reg reset = 0;
  initial begin
     # 17 reset = 1;
     # 11 reset = 0;
     # 29 reset = 1;
     # 11 reset = 0;
     # 100 $stop;
  end

  /* Make a regular pulsing clock. */
  reg clk = 0;
  always #5 clk = !clk;

  wire [7:0] value;
  counter c1 (value, clk, reset);

  initial
     $monitor("At time %t, value = %h (%0d)",
```

```
            $time, value, value);
endmodule // test
```

The following command “iverilog -o my_design counter_tb.v counter.v” creates the “my_design”. In Appendix A. File generated with the iverilog command “iverilog -o my_design counter_tb.v counter.v” is found.

The following command “vvp my_design” will simulate the counter.v verilog file.

```
At time                  0, value = xx (x)
At time                 17, value = 00 (0)
At time                 35, value = 01 (1)
At time                 45, value = 02 (2)
At time                 55, value = 03 (3)
At time                 57, value = 00 (0)
At time                 75, value = 01 (1)
At time                 85, value = 02 (2)
At time                 95, value = 03 (3)
At time                105, value = 04 (4)
At time                115, value = 05 (5)
At time                125, value = 06 (6)
At time                135, value = 07 (7)
At time                145, value = 08 (8)
At time                155, value = 09 (9)
At time                165, value = 0a (10)
** VVP Stop(0) **
** Flushing output streams.
** Current simulation time is 168 ticks.
```

Adding a few lines to the file counter_tb.v to dump the results to a vcd file that can be used with GTKWave.

```
initial
 begin
   $dumpfile("test.vcd");
   $dumpvars(0,test);
 end
```

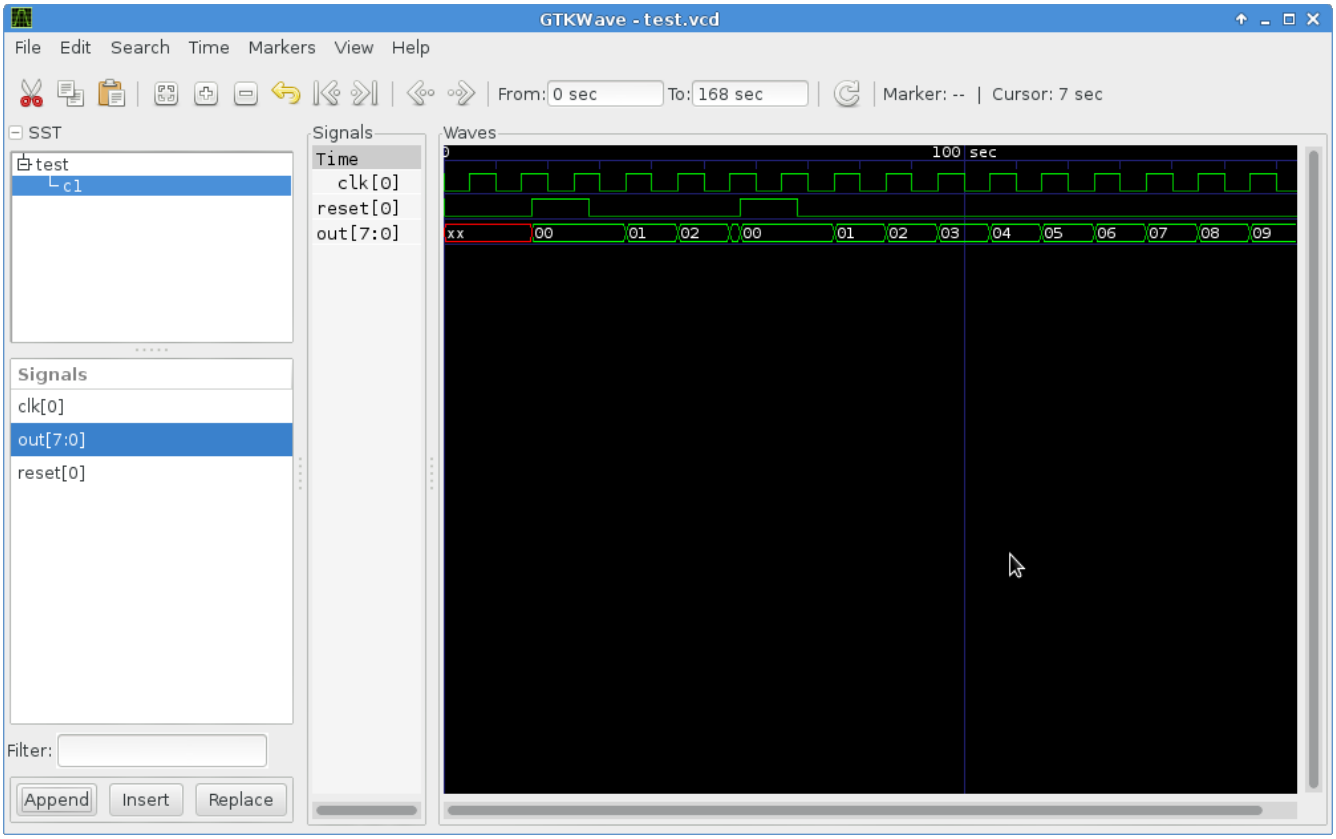
The file counter_tb_vcd.v

```
module test;
initial
 begin
   $dumpfile("test.vcd");
   $dumpvars(0,test);
 end

 /* Make a reset that pulses once. */
 reg reset = 0;
 initial begin
    # 17 reset = 1;
    # 11 reset = 0;
    # 29 reset = 1;
    # 11 reset = 0;
```

```
    # 100 $stop;
  end

  /* Make a regular pulsing clock. */
  reg clk = 0;
  always #5 clk = !clk;

  wire [7:0] value;
  counter c1 (value, clk, reset);

  initial
    $monitor("At time %t, value = %h (%0d)",
             $time, value, value);
endmodule // test
```

The following command “iverilog -o my_design_vcd counter_tb_vcd.v counter.v” creates the “my_design_vcd”. In Appendix B. File generated with the iverilog command “iverilog -o my_design_vcd counter_tb_vcd.v counter.v” is found.

Now the results of the simulation can be viewed with GTKWave.



Appendix A. File generated with the iverilog command “iverilog -o my_design counter_tb.v counter.v”.

```
#! /usr/local/bin/vvp
```

```
:ivl_version "0.9.7 " "(v0_9_7-7-g9b38de5)";
:vpi_time_precision + 0;
:vpi_module "system";
:vpi_module "v2005_math";
:vpi_module "va_math";
S_0x1edd730 .scope module, "test" "test" 2 1;
 .timescale 0 0;
v0x1f112a0_0 .var "clk", 0 0;
v0x1f11370_0 .var "reset", 0 0;
v0x1f11420_0 .net "value", 7 0, v0x1f11160_0; 1 drivers
S_0x1f01060 .scope module, "c1" "counter" 2 18, 3 1, S_0x1edd730;
 .timescale 0 0;
P_0x1eff2c8 .param/l "WIDTH" 3 3, +C4<01000>;
v0x1f01180_0 .net "clk", 0 0, v0x1f112a0_0; 1 drivers
v0x1f11160_0 .var "out", 7 0;
v0x1f11200_0 .net "reset", 0 0, v0x1f11370_0; 1 drivers
E_0x1edd3a0 .event edge, v0x1f11200_0;
E_0x1f01150 .event posedge, v0x1f01180_0;
    .scope S_0x1f01060;
T_0 ;
    %wait E_0x1f01150;
    %load/v 8, v0x1f11160_0, 8;
    %mov 16, 0, 24;
    %addi 8, 1, 32;
    %ix/load 0, 8, 0;
    %assign/v0 v0x1f11160_0, 0, 8;
    %jmp T_0;
    .thread T_0;
    .scope S_0x1f01060;
T_1 ;
    %wait E_0x1edd3a0;
    %load/v 8, v0x1f11200_0, 1;
    %jmp/0xz  T_1.0, 8;
    %cassign/v v0x1f11160_0, 0, 8;
    %jmp T_1.1;
T_1.0 ;
    %deassign v0x1f11160_0, 0, 8;
T_1.1 ;
    %jmp T_1;
    .thread T_1, $push;
    .scope S_0x1edd730;
T_2 ;
    %set/v v0x1f11370_0, 0, 1;
    %end;
    .thread T_2;
    .scope S_0x1edd730;
T_3 ;
    %delay 17, 0;
    %set/v v0x1f11370_0, 1, 1;
```

```
    %delay 11, 0;
    %set/v v0x1f11370_0, 0, 1;
    %delay 29, 0;
    %set/v v0x1f11370_0, 1, 1;
    %delay 11, 0;
    %set/v v0x1f11370_0, 0, 1;
    %delay 100, 0;
    %vpi_call 2 10 "$stop";
    %end;
    .thread T_3;
    .scope S_0x1edd730;
T_4 ;
    %set/v v0x1f112a0_0, 0, 1;
    %end;
    .thread T_4;
    .scope S_0x1edd730;
T_5 ;
    %delay 5, 0;
    %load/v 8, v0x1f112a0_0, 1;
    %inv 8, 1;
    %set/v v0x1f112a0_0, 8, 1;
    %jmp T_5;
    .thread T_5;
    .scope S_0x1edd730;
T_6 ;
    %vpi_call 2 21 "$monitor", "At time %t, value = %h (%0d)", $time, v0x1f11420_0, v0x1f11420_0;
    %end;
    .thread T_6;
# The file index is used to find the file name in the following table.
:file_names 4;
    "N/A";
    "<interactive>";
    "counter_tb.v";
    "counter.v";
```

Appendix B. File generated with the iverilog command "iverilog -o my_design_vcd counter_tb_vcd.v counter.v".

```
#! /usr/local/bin/vvp
:ivl_version "0.9.7 " "(v0_9_7-7-g9b38de5)";
:vpi_time_precision + 0;
:vpi_module "system";
:vpi_module "v2005_math";
:vpi_module "va_math";
S_0x237fab0 .scope module, "test" "test" 2 1;
 .timescale 0 0;
v0x23b3ab0_0 .var "clk", 0 0;
v0x23b3b80_0 .var "reset", 0 0;
v0x23b3c30_0 .net "value", 7 0, v0x23b3970_0; 1 drivers
```

```
S_0x23a3510 .scope module, "c1" "counter" 2 23, 3 1, S_0x237fab0;
 .timescale 0 0;
P_0x23a1778 .param/l "WIDTH" 3 3, +C4<01000>;
v0x23a3630_0 .net "clk", 0 0, v0x23b3ab0_0; 1 drivers
v0x23b3970_0 .var "out", 7 0;
v0x23b3a10_0 .net "reset", 0 0, v0x23b3b80_0; 1 drivers
E_0x237f720 .event edge, v0x23b3a10_0;
E_0x23a3600 .event posedge, v0x23a3630_0;
    .scope S_0x23a3510;
T_0 ;
    %wait E_0x23a3600;
    %load/v 8, v0x23b3970_0, 8;
    %mov 16, 0, 24;
    %addi 8, 1, 32;
    %ix/load 0, 8, 0;
    %assign/v0 v0x23b3970_0, 0, 8;
    %jmp T_0;
    .thread T_0;
    .scope S_0x23a3510;
T_1 ;
    %wait E_0x237f720;
    %load/v 8, v0x23b3a10_0, 1;
    %jmp/0xz  T_1.0, 8;
    %cassign/v v0x23b3970_0, 0, 8;
    %jmp T_1.1;
T_1.0 ;
    %deassign v0x23b3970_0, 0, 8;
T_1.1 ;
    %jmp T_1;
    .thread T_1, $push;
    .scope S_0x237fab0;
T_2 ;
    %vpi_call 2 4 "$dumpfile", "test.vcd";
    %vpi_call 2 5 "$dumpvars", 1'sb0, S_0x237fab0;
    %end;
    .thread T_2;
    .scope S_0x237fab0;
T_3 ;
    %set/v v0x23b3b80_0, 0, 1;
    %end;
    .thread T_3;
    .scope S_0x237fab0;
T_4 ;
    %delay 17, 0;
    %set/v v0x23b3b80_0, 1, 1;
    %delay 11, 0;
    %set/v v0x23b3b80_0, 0, 1;
    %delay 29, 0;
    %set/v v0x23b3b80_0, 1, 1;
```

```
    %delay 11, 0;
    %set/v v0x23b3b80_0, 0, 1;
    %delay 100, 0;
    %vpi_call 2 15 "$stop";
    %end;
    .thread T_4;
    .scope S_0x237fab0;
T_5 ;
    %set/v v0x23b3ab0_0, 0, 1;
    %end;
    .thread T_5;
    .scope S_0x237fab0;
T_6 ;
    %delay 5, 0;
    %load/v 8, v0x23b3ab0_0, 1;
    %inv 8, 1;
    %set/v v0x23b3ab0_0, 8, 1;
    %jmp T_6;
    .thread T_6;
    .scope S_0x237fab0;
T_7 ;
    %vpi_call 2 26 "$monitor", "At time %t, value = %h (%0d)", $time, v0x23b3c30_0, v0x23b3c30_0;
    %end;
    .thread T_7;
# The file index is used to find the file name in the following table.
:file_names 4;
    "N/A";
    "<interactive>";
    "counter_tb_vcd.v";
    "counter.v";
```